國 立 交 通 大 學

光電工程研究所

博 士 論 文

低溫多晶矽薄膜電晶體元件特性
應用於光感測器之研究

Study on Characterization of Low-Temperature
Poly-Silicon Thin Film Transistor for
Optical Sensor Application

研 究 生： 郭 彥 甫
指導教授： 戴 亞 翔 博士

中 華 民 國 九 十 九 年 九 月

低溫多晶矽薄膜電晶體元件特性應用於光感測器之研究

Study on Characterization of Low-Temperature Poly-Silicon Thin Film Transistor for Optical Sensor Application

研 究 生：郭 彥 甫　　Student: Yan-Fu Kuo

指導教授：戴 亞 翔 博士　　Advisor: Dr. Ya-Hsiang Tai

國 立 交 通 大 學

光電工程研究所

博 士 論 文

A Dissertation

Submitted to the Institute of Electro-Optical Engineering

Department of Photonics College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

in Electro-Optical Engineering

September 2010

Hsinchu, Taiwan, Republic of China

中 華 民 國　九 十 九　年　九　月

低溫多晶矽薄膜電晶體元件特性
應用於光感測器之研究

研 究 生: 郭 彥 甫　　指導教授: 戴 亞 翔 博士

國 立 交 通 大 學

光電工程研究所

摘要

本論文探討低溫多晶矽薄膜電晶體元件特性應用於光感測器之研究。由於在薄膜電晶體的 SPICE 電路模型中，並沒有對應的光漏電流模型可供模擬；同時，傳統定義暗態電流與照光電流比例的光敏感性參數並不適合用作分析光漏電機制。因此，本論文首先提出以 Unit-Lux-Current (ULC) 參數來分析元件的光效應行為。此參數反應的是單位光通量致光電流的能力並且與元件的暗態電流無關。光漏電流的成因是由於空間電荷區產生額外的載子所致。根據加諸於半導體的電場導致庫倫位障降低的 Poole-Frenkel 效應與聲子共振穿隧效應；在橫向空乏區與閘極-汲極重疊空乏區產生的光漏電流行為以及與活化能相關的溫度等效應，都有詳細於文中所提出的物理模型與能帶圖解釋探討。而後也提出此光漏電參數的相關場效應與溫度效應的方程式去進一步研究其光漏電機制。

接著本論文也探討光效應與直流偏壓所額外產生不均勻缺陷的關係。由於矽材料能帶結構是屬於非直接能隙，根據動量守恆原理，矽材料吸收光所產生過多的電子-電洞對無法在價電帶與傳導帶直接複合，而是傾向透過能隙間的缺陷態

作複合的動作。我們研究直流偏壓狀態下多晶矽薄膜電晶體主要的兩大劣化機制，熱載子效應與自發熱效應，這樣的劣化所導致的光漏電流亦會嚴重影響我們在設計感測電路時的困難度。當光照在經過熱載子劣化後的元件，在空乏區域裡的多數電子-電洞對從這些因熱載子劣化而額外存在的淺態能階(Tail state)中產生。而當元件經過自發熱劣化後，矽薄膜層因高溫釋放氫造成斷鍵而形成了深態能階(Deep state)，而又因為此能階分佈在能隙的中間處，對矽材料來說，它同時也提供了照光產生電子-電洞對最有效率的複合中心。在本論文中我們利用這兩種劣化情況去探討因缺陷所導致的相關光漏電行為，同時也修改缺陷非勻狀態的薄膜電晶體所對應的光漏電方程式。這些經驗方程式的建立將有助於模型化與模擬低溫多晶係薄膜電晶體電路操作在直流偏壓劣化後的光效應行為分析。

接下來由於低溫多晶矽薄膜電晶體是上閘極結構，操作時它同樣會受到來自高強度環境背光源的影響而導致光漏電流的發生。基本上能夠採用正面照光的方式分析背面照光的光漏電流。然而不同的是，當光的來源為背光時，會有大量的電子-電洞對產生在元件多晶矽薄膜層的底部。因此將會有殘留過量的電洞累積因而形成正電位通道。在本文中我們同樣也探討背光致光漏電流的各式偏壓效應、溫度以及缺陷密度等影響因子。同時，我們利用缺陷在能階的分佈與背光導致電流關係的新觀點進一步去確認先前研究所未見之自發熱效應淺態能階的存在與位置，進而建立元件完整且正確的劣化模型。

本論文最後也提出了低溫多晶矽薄膜電晶體自我閘極遮蔽的三維嵌入光偵測的概念。這個系統利用了光源相對閘極汲極側與閘極源極側的正反向量測來建立感測方向，因而提供元件在照光下感測的不匹配特性。由於此概念並未改變元件製作流程，是可以期待整合至面板的偵測系統的。接者提出利用低溫多晶矽薄膜電晶體設計的一個源極隨耦態的電路去做環境光的感測。同時各種可能產生的元件變動性被考慮並利用統計性與補償電路的方式校正，此系統同樣也有著能整合至面板偵測系統的潛力。

Study on Characterization of Low-Temperature Poly-Silicon Thin Film Transistor for Optical Sensor Application

Student: Yan-Fu Kuo **Advisor: Dr. Ya-Hsiang Tai**

Department of Photonics & Institute of Electro-optical Engineering,

College of Electrical and Computer Engineering

National Chiao Tung University

Abstract

This work focuses on the characterization of low-temperature poly-silicon thin film transistor for sensor application. Due to in the SPICE models of TFT, there is no photo leakage current model for simulation. Meanwhile, photosensitivity ($R_{L/D}$) defined as the ratio of the current under illumination to the current in the dark is not proper to be used to analyze photo leakage mechanism. Thus, a new parameter, Unit-Lux-Current (ULC) is firstly used to analyze the effects of illumination on LTPS TFTs. It reflects the ability of photo leakage current induced per unit-photo flux and independent of the dark current. The amount of the photo current should be associated with the carrier generation in the space charge region. Based on the Poole-Frenkel effect lowering of a Coulombic barrier and phonon-assisted tunneling due to the electric field applied to a semiconductor, the ULC can be taken into account both the

leakage current induced in the lateral depletion and in the gate-drain overlap depletion regions. We further take into account the temperature effect of ULC. The temperature effect can be identified by activation energy. An equation is provided to properly describe model for mechanism ULC behavior under various bias and temperature conditions for further exploration of photo leakage mechanism.

Then we focus on the relation between photosensitivity and additional non-uniform defects. The energy-band structure of Si material is indirect band-gap. The excess electron-hole pairs induced by the absorption of light would not be recombined from band to band directly due to the momentum conservation principle. Thus silicon is more likely to recombine through localized traps. We investigate the two main degradation mechanisms for the poly-Si TFTs under DC operation, namely the hot carrier effect and the self heating effect. Due to such degradation, the photo-induced leakage current is strongly influenced which is difficultly designed for sensing circuits. When the LTPS TFT devices after hot carrier stress are under optical illumination, the numerous electron-hole pairs from additionally created shallow tail states are generated in the lateral depletion region. Then devices after self heating stress, the high temperature in the poly-Si film can release hydrogen and cause plenty of dangling bonds as deep states. These deep states near mid level, in the lateral depletion region, can recombine the electron-hole pairs generated by irradiation. In this work, we apply both stress conditions deliberately to manipulate the defect-related photo behaviors and modify ULC equations in TFTs. The empirical equation of ULC provides a potential modeling for simulation of LTPS TFT circuitry considering the photo effect after DC stress.

Next, because LTPS TFTs are top gate structure, it is suffer from undesirable photo leakage current under a high back illumination environment. We can analyze such photo-induced current like as front light case. However, when the light is emitted

from back-light, plenty of electron-hole pairs are generated in the bottom of poly-Si film. Therefore, the residual excess holes are accumulated in the poly-Si film to form the floating body with a positive channel potential. We also present detail studies on the factors that affect the photo leakage current like bias condition, temperature, and defect states of the LTPS TFTs. Meanwhile, we provide new insight which use energy level of trap defect behaviors connected with photo induced current to further make sure the existence of tail state after self heating degradation. Furthermore, a more accurate model after self-heating degradation is proposed.

A three dimensional embedded optical sensor employs low temperature poly-silicon thin film transistor which used gate metal shielding by itself characteristics was proposed. The system connect with forward and reverse measurements can be used to set up sensing direction. It provides sensing disparity characteristics of adopted devices under illumination. It's expected the integration of sensing system onto the panel without extra components sensors and extra change in the fabrication process. Then a circuit of source follower type based on the LTPS TFTs which can sense the illumination condition is proposed to be used as an ambient light sensor. Some kinds of variation effect can be calibrated by statistical and compensation circuit methods. This approach would provide the possibility for the light sensor array integrated in the pixels with the same device of LTPS TFTs.

誌謝

執筆至此，求學之路即將抵達一個終站，回顧求學歷程的點滴，心中真的是百感交集。在交大博士班修業的這些年裡，首先我想感謝我的指導教授戴亞翔博士。由於老師的用心指導與耐心協助，讓我受益良多並且不斷成長，在研究路上因而走得更平穩踏實，進而順利完成論文。除此之外，也感謝老師在生活上的貼心鼓勵，設身處地體諒與包容學生遇到的困難，教導自己如何看待、度過人生中所面對的波折，在這裡要先對老師致上誠摯的謝意。另外，也要感謝張鼎張及劉伯村兩位教授在專業領域上的指導與協助，兩位老師積極的態度與對研究的熱忱，讓我獲益匪淺，對學生的關心與幫助，同樣也是讓我倍感窩心。還有論文口試委員的趙天生、黃乙白和莊敏宏教授於百忙之中前來給予指導，提供許多寶貴的意見，讓我的論文能夠更趨完善。

接著要感謝實驗室的弘緯、震鑠及興華學長，和曾經一起同甘共苦的夥伴們，同實驗室的士哲、隔壁實驗室的皓彥、一德和士欽，感謝大家的鼓勵協助與彼此打氣，讓我在研究上感到迷惑時能找到方向，能繼續擁有研究的熱忱以及挑戰夢想的堅持；也要感謝實驗室學弟妹：允翔、枷彬、漢清、國珮、騰瑞、紹文在過去所提供的幫助；祿盛和志融，讓我後期的資料能夠順利完成。以及其他的碩士班學弟妹，感謝過去曾和大家共同度過的歡樂時光。還有好友嘉軒的支持與鼓勵，旭銘、天浩、文化、沈謙等好友的陪伴，讓我在忙碌的研究生活中，增添許多歡笑的色彩，豐富了我的生活，謝謝你們帶給我的每個精彩與回憶。

最後，這一刻的喜悅我想獻給我摯愛的父母，感謝我的父母多年來辛苦的栽培與教誨，總是在背後默默的支持我、適時給予我關心、鼓勵與肯定，給我力量完成學業。能夠完成這篇論文，我由衷地感謝我的家人。

僅將此文獻給所有我愛的師長、家人與好友

彥甫 2010 誌於風城交大

Contents

Chinese Abstract ---------- i

English Abstract ---------- iii

Acknowledgment ---------- vi

Contents ---------- vii

Figure Captions ---------- ix

Table Captions ---------- xv

Chapter 1 Introduction

1.1 General Background ---------- 01

1.2 Motivation ---------- 02

1.3 Thesis Organization ---------- 04

Chapter 2 Experimental

2.1 Device Fabrication ---------- 11

2.2 Experimental Procedures ---------- 12

2.3 Extraction Methods of Device Parameters ---------- 13

Chapter 3 Photosensitivity Analysis of Low-Temperature Poly-Si Thin Film Transistor Based on Unit-Lux-Current

3.1 Introduction ---------- 19

3.2 Classification and Characterization of Photosensitivity ---------- 20

3.3 Insight of Photosensitivity ---------- 22

3.4 Conclusion ---------- 26

Chapter 4 Dependence of Photosensitive Effect on the Defects Created by DC Stress for LTPS TFTs

4.1 Introduction ---------- 45

4.2 Electrical Degradation of Poly-Si TFT under DC Stress ---------- 46

4.3 Insight of Defect-Related Photosensitivity ---------- 48

4.4 Conclusion ---------- 53

Chapter 5 Investigation of Backlight Sensing in Poly-Si TFTs

5.1 Introduction ---------- 71

5.2 Experimental Procedures ---------- 72

5.3 Results and Discussions ---------- 72

5.4 Conclusion ---------- 79

Chapter 6 Characterization of Thin film Transistor for Optical Sensor Application

6.1 Three-Dimension Poly Silicon Interaction Display ---------- 101

6.2 Sensing Circuits of Source Follower Type using LTPS TFTs---- 103

6.3 Light Sensor for Detecting Uniformity of Backlight Intensity -- 111

6.4 Conclusion ---------- 112

Chapter 7 Conclusions and Suggestions for Future Work ---------- 133

References ---------- 135

Vita ---------- 147

Publication List ---------- 148

Figure Captions

Chapter 1

Fig. 1-1 (a) Model for the crystal structure of polysilicon films. (b) The charge distribution within the crystallite and at the grain boundary. (c) The energy band structure of the polysilicon crystallites.----------06

Fig. 1-2 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling. ----07

Fig. 1-3 The poly-Si density of states distribution. ----------08

Fig. 1-4 The figure illustrating the structure of this dissertation. ----------09

Chapter 2

Fig. 2-1 The cross-section views of n-channel LTPS TFTs with LDD structure. --15

Fig. 2-2 The photo leakage current and the power variation spectrum of the light source. ----------16

Fig. 2-3 Emission spectrum of a phosphor-based white LED. ----------17

Chapter 3

Fig. 3-1 Photograph of the special U-shaped TFT with an arrow indicating the scanning path of the illumination beam. ----------28

Fig. 3-2 The drain current of the U-shaped TFT with the distance that the illumination beam scanning along the channel direction.----------29

Fig. 3-3 The I_D-V_G transfer characteristics under illumination from dark to 31320 lux. ----------30

Fig. 3-4 Gate bias dependence of LTPS TFT photo currents and dark currents in off region. ---------- 31

Fig. 3-5 The relationship between leakage current and illumination intensity under different bias conditions. ---------- 32

Fig. 3-6 Gate bias effect on Unit-Lux-Current at different drain biases. ---------- 33

Fig. 3-7 Drain bias effect on Unit-Lux-Current at different gate biases. ---------- 34

Fig. 3-8 The second component of Unit-Lux-Current (ULC_2) versus drain bias at different gate voltages. ---------- 35

Fig. 3-9 The calculated and experimental data of drain bias effect on Unit-Lux Current at different gate biases. ---------- 36

Fig. 3-10 Temperature effect on photo leakage current of LTPS TFT. ---------- 38

Fig. 3-11 Drain bias dependence of Unit-Lux-Current at different temperatures. --- 39

Fig. 3-12 The second component of Unit-Lux-Current (ULC_2) versus drain bias with different temperatures. ---------- 40

Fig. 3-13 Dependence of factors α and β on temperatures. ---------- 41

Fig. 3-14 A proposed model of ULC mechanism for LTPS TFT. ---------- 42

Fig. 3-15 Photo leakage current variation among different devices. ---------- 43

Chapter 4

Fig. 4-1 The profile of Joule heat generated in the channel for the device under self heating stress. ---------- 55

Fig. 4-2 The comparison for the heat transfer coefficients of the films for the poly-Si TFTs. ---------- 56

Fig. 4-3 The I_{ds}-V_{gs} transfer characteristics under different illumination conditions for (a) conventional LDD and (b) only one-side LDD device structures.---57

Fig. 4-4 The I_{ds}-V_{gs} transfer characteristics with 1V drain voltage before and after (a) hot carrier stress and (b) self heating stress under different illumination conditions.---58

Fig. 4-5 (a) Normalized Unit-Lux-Current and mobility at V_{ds}=0.6V and 10V with hot carrier stress times. (b) Normalized ULC and threshold voltage at V_{ds}=0.6V and 10V with self heating stress times. ---59

Fig. 4-6 Drain bias effect on Unit-Lux-Current with different hot carrier stress times.---60

Fig. 4-7 (a) The first component (ULC_1) and (b) the second component (ULC_2) of Unit-Lux-Current versus drain bias with different hot carrier stress times.---61

Fig. 4-8 Dependence of fitting factors A_1.A_2 and B_1, B_2 on hot carrier stress. ---62

Fig. 4-9 Drain bias effect on Unit-Lux-Current with different self heating stress times.---63

Fig. 4-10 (a) The first component (ULC_1) and (b) the second component (ULC_2) of Unit-Lux-Current versus drain bias with different self heating stress times.---64

Fig. 4-11 Dependence of fitting factors A_1.A_2 and B_1, B_2 on self heating stress. ---65

Fig. 4-12 A proposed hot carrier degradation model of ULC mechanism for TFTs.---66

Fig. 4-13 The photo leakage current spectrum of the light source in the range of 350-750 nm at lower bias after hot carrier stress.---67

Fig. 4-14 A proposed self heating degradation model of ULC mechanism for

TFTs.---------- 68

Fig. 4-15 The photo leakage current spectrum of the light source in the range of 350-750 nm at lower bias after self heating stress. ---------- 69

Chapter 5

Fig. 5-1 The cross section of device under back light illumination. ---------- 81

Fig. 5-2 The transmission rate and absorption rate of LED light source. ---------- 82

Fig. 5-3 Distribution of electron-hole pairs in the poly-Si of TFTs. ---------- 84

Fig. 5-4 The Explanation of current flow of poly-Si under back light illumination.---------- 85

Fig. 5-5 Relationship between leakage current and illumination intensity under different bias conditions. ---------- 86

Fig. 5-6 (a) Drain bias effect on Unit-Lux Current at different gate biases. (b) Gate bias effect on Unit-Lux Current at different drain biases. ---------- 87

Fig. 5-7 Experiment data (symbols) and empirical formula (solid lines). ---------- 88

Fig. 5-8 Drain bias dependence of Unit-Lux Current at different temperature. ---- 90

Fig. 5-9 Iillum measured at V_{gs}=-5V, V_{ds}=3V dependence on the illumination intensity before and after 1000 seconds of hot carrier or self heating stress with (a) forward and (b) reverse measurements. ---------- 92

Fig. 5-10 Drain bias dependence of ULC at different hot carrier stress times measured in the forward mode.---------- 93

Fig. 5-11 Drain bias dependence of ULC at different hot carrier stress times measured in the reverse mode. ---------- 94

Fig. 5-12 The I_{ds}-V_{gs} transfer characteristics of TFTs with (a) forward and (b) reverse measurements in saturation region 5V drain voltage under different back illumination conditions for self heating stress. ---------- 95

Fig. 5-13 Drain bias dependence of ULC at different self heating stress times measured in the forward mode.---------- 96

Fig. 5-14 Drain bias dependence of ULC at different self heating stress times measured in the reverse mode. ---------- 97

Fig. 5-15 The normalized (a) gate-to-drain capacitance C_{gd} and (b) gate-to-source capacitance C_{gs} curves before and after stress with different frequencies.---
---------- 98

Fig. 5-16 The cross section views of degradation model in TFT structure under hot carrier and self heating stress conditions. ---------- 99

Chapter 6

Fig 6-1 The I_D-V_G transfer characteristics under illumination from dark to 31320 lux. (Figure insert) rotatable probe station experimental setup.---------- 113

Fig 6-2 Gate metal shielding by itself for poly-Si TFTs. ---------- 114

Fig 6-3 The forward and reverse measured photo currents verses negative gate bias with several incident angles under (a)5100 lux (b)20500 lux illumination conditions.---------- 115

Fig 6-4 Forward and reverse photo currents ratio verses incident angles under 5100 lux and 20600 lux illumination conditions.---------- 116

Fig 6-5 Using LTPS TFTs as oblique light sensors for three dimensional interaction display (a) Single light source (b) Multiple light sources. -- 117

Fig 6-6 Schematic diagram of proposed 2T1C light sensing circuit and its timing sequence. ---------- 118

Fig 6-7 Illumination dependence of I_D-V_D characteristic and its fitting formula.---------- 119

Fig 6-8 SPICE simulation results of TFT (W/L=20um/5um). ---------- 121

Fig 6-9 (a) The modified 2T1C light-sensing circuit model for simulation (b) its time diagram. ---------- 122

Fig 6-10 Simulation results under illumination and in the dark. ---------- 123

Fig 6-11 The comparison of the current ratio of under illumination and in the dark $R_{L/D}$ among on, subthreshold, and off region and that of current level (inset). ---------- 124

Fig 6-12 Measured waveforms of output voltages of proposed 2T1C light-sensing circuit illuminative variations from dark to 31320 lux on (a) subthreshold region and (b) off region.---------- 125

Fig 6-13 Measured output slopes of fifteen proposed light-sensing circuits in off region (dash line) and their average curve (solid line). ---------- 126

Fig 6-14 The influence of V_{th} shift operated on (a) subthreshold region (b) off region. ---------- 127

Fig 6-15 Average slopes versus illumination intensity with five samples as an average unit. ---------- 128

Fig 6-16 (a) Schematic of our proposed light-sensing circuit with compensation part and (b) time diagram. ---------- 129

Fig 6-17 Fifty times of Monte Carlo simulation results of the proposed 2T1C light-sensing circuit when V_{th} shift is ±0.5V (a) before compensation (b) after compensation. ---------- 130

Fig 6-18 (a) Simplified block diagram of digitization circuit and (b) its signal diagrams. ---------- 131

Table Captions

Chapter 3

Table 3-1 The values of fitting factors under front light illumination. ---------- 37

Chapter 5

Table 5-1 The drain bias and gate bias effects on photo leakage for LTPS TFTs. --- 83

Table 5-2 The values of fitting factors under back light illumination. ---------- 89

Table 5-3 The values of temperature fitting factors under back light illumination.---------- 91

Table 5-4 The defect information of several analyses.---------- 100

Chapter 6

Table 6-1 $I_0(L)$ and $R_0=1/A_0(L)$ at V_{GS}=0.5V with the illumination intensity variation. ---------- 120

Chapter 1

Introduction

1.1 General Background

Thin film transistor (TFT) is a metal-oxide-silicon field effect transistor (MOSFET) fabricated on an insulator substrate which are included glass substrates, flexible substrates and so on by employing all thin film constituents. Thin film transistors have been widely used as switching devices in flat panel display, such as active-matrix liquid crystal display (AMLCD) [1.1-1.4] and active-matrix organic light emitting diode (AMOLED) display [1.5-1.9]. As for the active region material, it can be mainly divided into amorphous silicon (a-Si) and poly-crystalline silicon (poly-Si) types. The hydrogenated a-Si (a-Si:H) TFT is commonly applied in large size active matrix displays (AMDS) due to its highly mature process, low manufacturing cost and good device uniformity. However, the low electron field effect mobility of a-Si TFTs limits the capability of advanced and integrated circuit. On the contrary, polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention because of their widely applications. Compare with a-Si:H TFTs, poly-Si TFT can provide higher electron mobility and its higher driving current allows smaller TFT size to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. It offers a promising solution to realize the “System on Panel” technology. Nevertheless, using excimer laser to re-crystalline a-Si active layer, poly-Si TFT can offer very high current capability. However, the laser re-crystallization process also generates plenty

of the grain boundaries in poly-Si TFT, leading to poor uniformity and very huge variation due to the narrow laser process windows for producing large grain size poly-Si TFT. The fluctuation of pulse-to-pulse laser energy and non-uniform laser beam profile make laser energy density hard to hit the super lateral regime everywhere. The random grain boundaries and traps exist in the channel region [1.10-1.12]. This will cause serious non-uniformity of brightness in AMOLED panel. Since the device-to-device uniformity is hard to control, it is essential to develop circuits to compensate the variation. The roadmap for the poly-Si TFTs are expected that as the mobility and the device performance keeps improving, the driver circuits and some special value-added functions can be formed by the use of poly-Si TFTs eventually form the system on glass (SOG) technology. This somehow proved that for the display electronics the poly-Si TFTs can replace the externally connected bond ICs and the perspective of the SOG technology is truly applicable.

1.2 Motivation

The poly-Si TFT technology has some distinct advantages but its manufacture is more complex and high cost. The major advantage of poly-Si TFT is the higher field effective mobility than that of the amorphous silicon (a-Si) based devices. The high carrier mobility and the existence of complementary pairs permit the integration of drive circuits and the smaller area of pixel transistor. The integration of drive circuits could reduce manufacturing costs, and increase the functionality of large-area microelectronics [1.13-1.14]. The smaller area of pixel transistor leads to a larger aperture ratio for a given pixel size, or enables a high resolution display for a given aperture ratio, resulting in fine image quality for mobile display. Recently, the demand

of high-end mobile electronic products such as cell phone, digital camera, GPS, mobile TV and so on is continuing to grow, so that the development of mobile displays with high resolution and high image quality is inevitable. Since most of people would like to use mobile electronic products outdoors under the sunlight, the readability in ambient illumination is a critical issue for mobile displays. To meet the requirement of superior readability under sunlight, the brightness of backlight becomes higher and higher. However, poly-Si TFTs operated in the high illumination environment exhibit substantial photo leakage current and degraded sub-threshold swing (S.S.), leading to the errors of gray level and difficulty in pixel design.

In addition, the application of circuit integration using poly-Si TFT continuously grow up as device characteristics improve further. Enlarging the grains in poly silicon layers is an effective approach for improving TFT performance. Several poly-Si re-crystallization methods based on laterally grown grains have been proposed to enlarge the grains and control the location of the grain boundaries [1.15-1.16]. In poly-Si TFT devices, however, the status of defect states at grain boundaries plays a crucial role for electrical characteristics, as shown in Fig. 1-1 and Fig. 1-2. Meanwhile, Fig. 1-3 shows the poly-Si density of states distribution. Shallow tail states are associated with strained bonds and deep states near mid-gap are associated with broken bonds. The stability of poly-Si TFT is one of the important issues for poly-Si technology. Recently, the researches about the stabilities of conventional excimer laser crystallized (ELC) poly-Si TFTs have been reported. The creation of trap states at poly-Si/gate dielectric interface or the charge trapping in the gate insulator is responsible for the degradation in electrical characteristics of poly-Si TFTs.

In this thesis, the photosensitive effect of n-type low temperature polycrystalline silicon thin-film transistors is investigated. A new index Unit-Lux-Current (ULC) characterizing the slope of the curve is introduced to discuss the photosensitivity. It is

discovered that the device photosensitivity is dependent on the gate, drain bias and temperature. Furthermore, we further use a peculiar device to demonstrate that the photo leakage current occurs in the depletion region at the drain junction. A qualitative deduction is developed to account for the photo leakage mechanism. However, the poly-Si TFTs suffer from several degradation mechanisms, such as hot carrier and self-heating effects. It was discovered that the photo-generated carrier behaviors under optical illumination are related to defect types created by different stress conditions. A model considering the relation between photosensitivity and defect is proposed to explain the anomalous illumination behaviors after device degradation. The empirical equation of ULC provides a potential modeling for simulation of LTPS TFT circuitry considering the photo effect. In addition, AMLCD requires back-light source to display input image. Poly-Si TFT operated in back illumination environment exhibits an undesired high leakage current to affect the function of pixel switch. The photo behaviors of poly-Si under back light illumination are also studied in detail. We also proposed three dimensional embedded optical sensors employs low temperature poly-silicon thin film transistor which used gate metal shielding by itself. This system provides sensing disparity characteristics of adopted devices under illumination. Meanwhile, we also proposed source follower type circuits to make ambient light sensors. Both applications are expected that the integration of sensing system onto the panel without extra novel device process development.

1.3 Thesis Organization

In this thesis, the photo behaviors of low-temperature polycrystalline silicon thin film transistors (poly-Si TFT) under front and back light illumination were studied. Furthermore, the models of electrical characteristics of poly-Si TFT under

illumination were investigated and established in detail. In addition, the photo leakage behaviors after DC stress degradation are also examined. Meanwhile, several optical sensor applications were developed in this work.

This dissertation is divided into seven chapters. It can be summarized in Fig. 1-4. The dissertation is organized in to the following chapters: In chapter 1, the general background and overview of low temperature polycrystalline silicon thin-film transistors are introduced. In chapter 2, the experimental, such as the fabrication and the measurement of the devices, is described. In chapter 3, photosensitivity analysis of low-temperature poly-Si thin film transistor based on Unit-Lux-Current is investigated. In chapter 4, dependence of photosensitive effect on the defects created by DC stress for LTPS TFTs is studied. In chapter 5, investigation of backlight sensing in Poly-Si TFTs is presented. In chapter 6, characterization of thin film transistor for optical sensor application is studied. Finally, the summarization of all experimental results in this dissertation and the suggestions for the future work are presented in chapter 7.

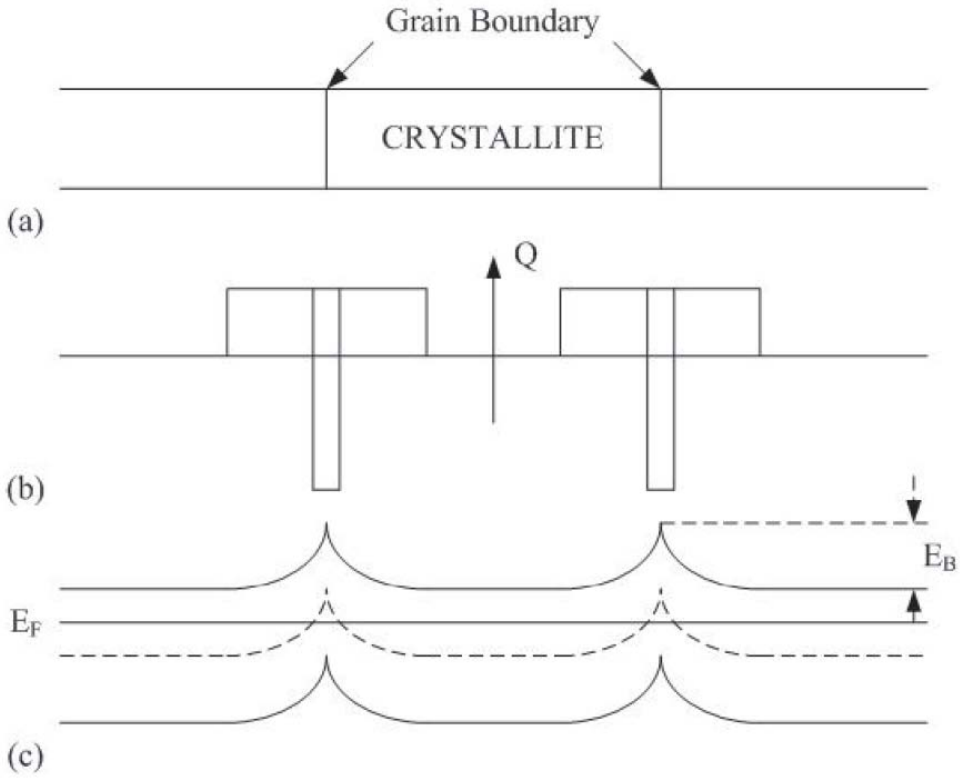


Figure 1-1 (a) Model for the crystal structure of polysilicon films. (b) The charge distribution within the crystallite and at the grain boundary. (c) The energy band structure of the polysilicon crystallites.

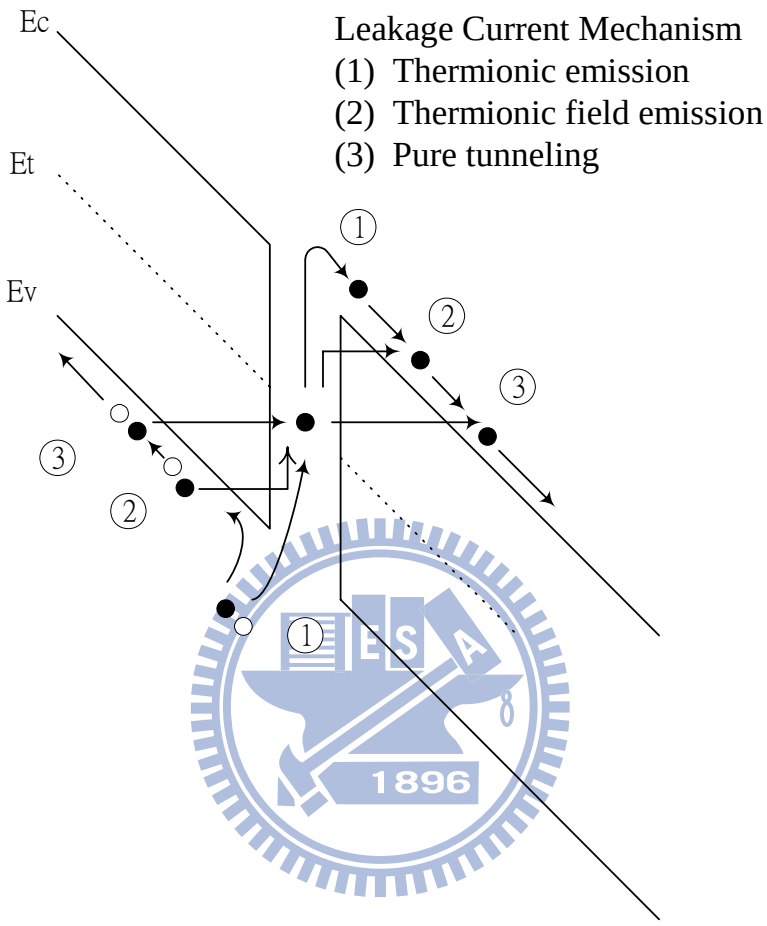


Figure 1-2 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling.

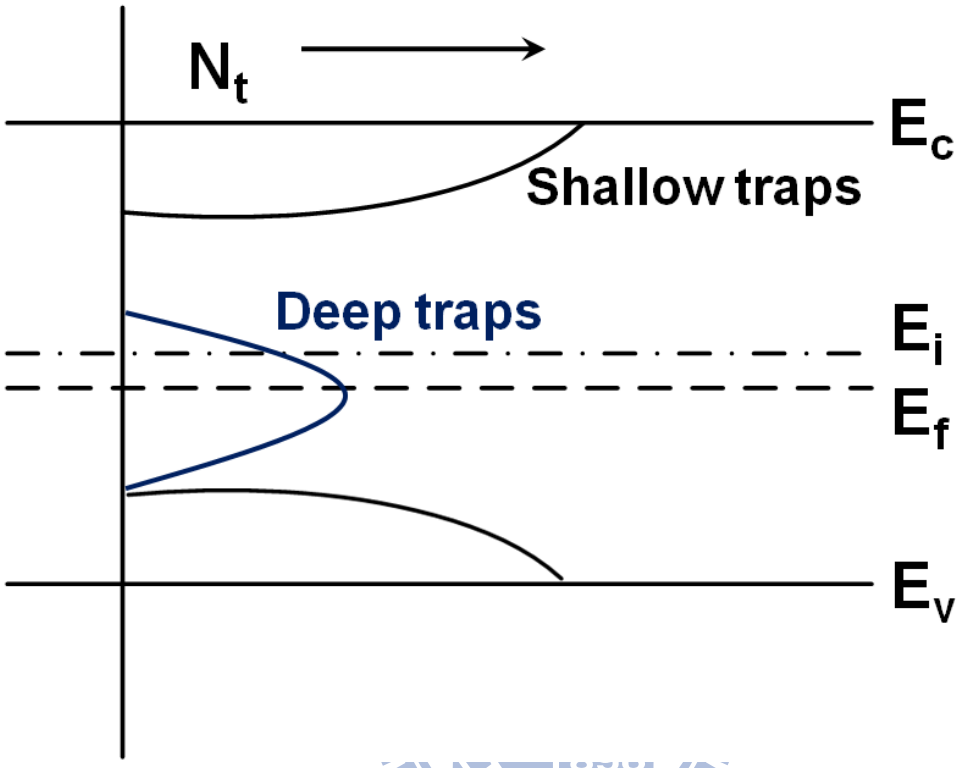


Figure 1-3 The poly-Si density of states distribution.

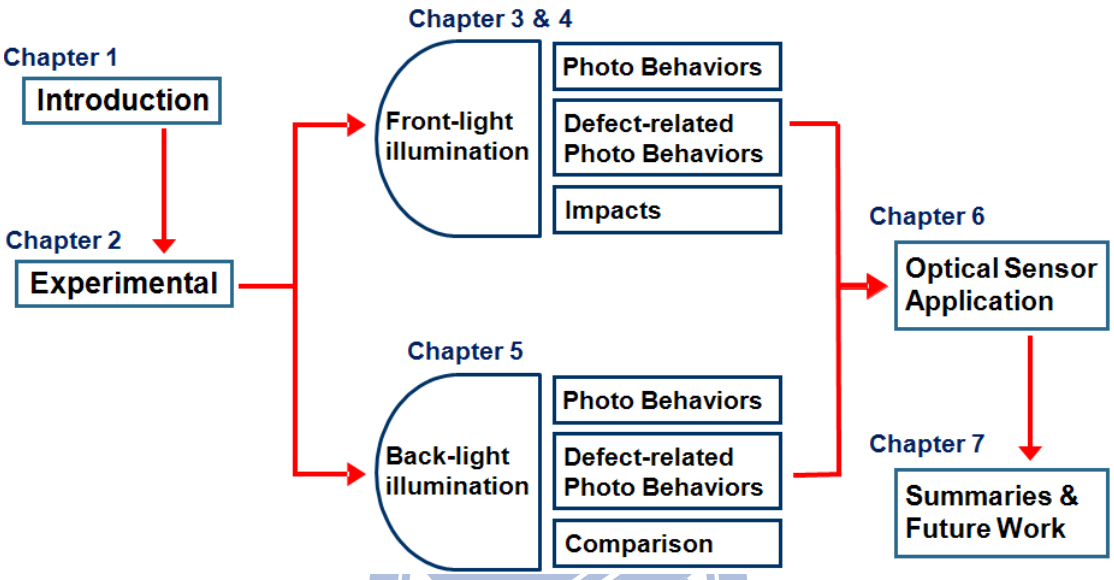


Figure 1-4 The figure illustrating the structure of this dissertation.


E S A
1896

Chapter 2

Experimental

2.1 Device Fabrication

The process flow of TFTs is described below. Top gate LTPS TFTs with width/length dimension of 20μm/5μm were fabricated using low temperature process. Firstly, the buffer oxide and a-Si:H films with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then put in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 100 nm SiO_2 was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. For n-type devices, the lightly doped drain (LDD) and the n^+ source/drain doping were formed by PH_3 implantation with dosage 2×10^{13} cm^{-2} and 2×10^{15} cm^{-2} of PH_3 respectively. The LDD implantation was self-aligned and the n^+ regions were defined with a separate mask. The LDD structure did not use on p-type devices. The p^+ source/drain doping was done by B_2H_6 self-align implantation with a dosage of 2×10^{15} cm^{-2}. Then, the interlayer of SiN_X was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work. The structure cross section view for the n-type poly-Si TFT is given in Fig. 2-1.

2.2 Equipment and Experiment Setup

In this section, the equipments to measure the device characteristics, namely the transfer behavior I_D-V_G curves and the capacitance curves, are described. In addition, the apparatus to DC stress the device is also illustrated. The I_D-V_G curves for the devices are measured by the Agilent 4156A precision semiconductor parameter analyzer. The C-V curves of the gate-to-source capacitance C_{GS} and gate-to-drain capacitance C_{GD} before and after stress with different frequencies are measured with the HP 4284A precision LCR meter. Before measuring the capacitance behavior, for every frequency the measure correction is performed with the open-circuit and short-circuit mode respectively for the needles before and after probing the electrode to eliminate the effect of the parasitic components in the surrounding and during probing. The DC stress is performed by the Agilent 4156A precision semiconductor parameter analyzer, which is the same one to measure the transfer characteristics.

The light was collimated and focused onto the device with top face white light illumination. Photo leakage current was induced by a halogen lamp irradiation stream with several neutral density filters (light intensity ranging from dark to 31320 lux) through the objective of a microscope, and the light intensity was measured by a digital luminous flux meter. Fig. 2-2 shows the photo leakage current, the power variation spectrum of the front light source in the range of 350-750nm.

The light was collimated and focused onto the device with bottom face white light illumination. However, compare with front light source we use halogen lamp irradiation, we use white light-emitting-diode (LED) as the back light source in our experiments. The white light LED backlight spectrum in the range of 350-750nm is also shown as Fig. 2-3.

2.3 Extraction Methods of Device Parameters

Three important device parameters are extracted and studied in this work: the threshold voltage V_{TH}, the sub-threshold swing S.S., and the field effect mobility μ_{FE}. Plenty methods are used to determine V_{TH}, which may be the most important parameter in application. In most of the researches on TFT, the constant current method is adopted. In this work the threshold voltage is determined by this method, which extract V_{TH} from the gate voltage at the normalized drain current I_D=10 nA for V_D=0.1V.

Sub-threshold swing S.S. (V/dec), is also a typical parameter to describe the control ability of gate toward channel. The sub-threshold swing should be ideally independent of drain voltage and gate voltage. However, in reality, the sub-threshold swing might increase with drain voltage due to short-channel effects. It might as well be affected by the serial resistance and interface traps and therefore become related to the gate voltage. In this work, it is defined as the minimum amount of gate voltage required to increase drain current by one order of magnitude.

The field effect mobility, μ_{FE}, is determined from the maximum transconductance gm at low drain voltage, which in this work 0.1 V is used. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order the first order I-V relation in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as $I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{TH})V_D - \frac{1}{2}V_D{}^2]$, where C_{ox} is the gate oxide capacitance per unit area, W is channel width, L is channel length, V_{TH} is the threshold voltage. If the drain voltage V_D is much smaller compared with (V_G-V_{TH}), then the I_D can be approximated as $I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D$ Therefore,

the electron field effect mobility can be expressed as $\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m$,where the transconductance is defined as $g_m = \frac{\partial I_D}{\partial V_G}|_{V_D=const.} = \frac{W C_{ox} \mu_{FE}}{L} V_D$

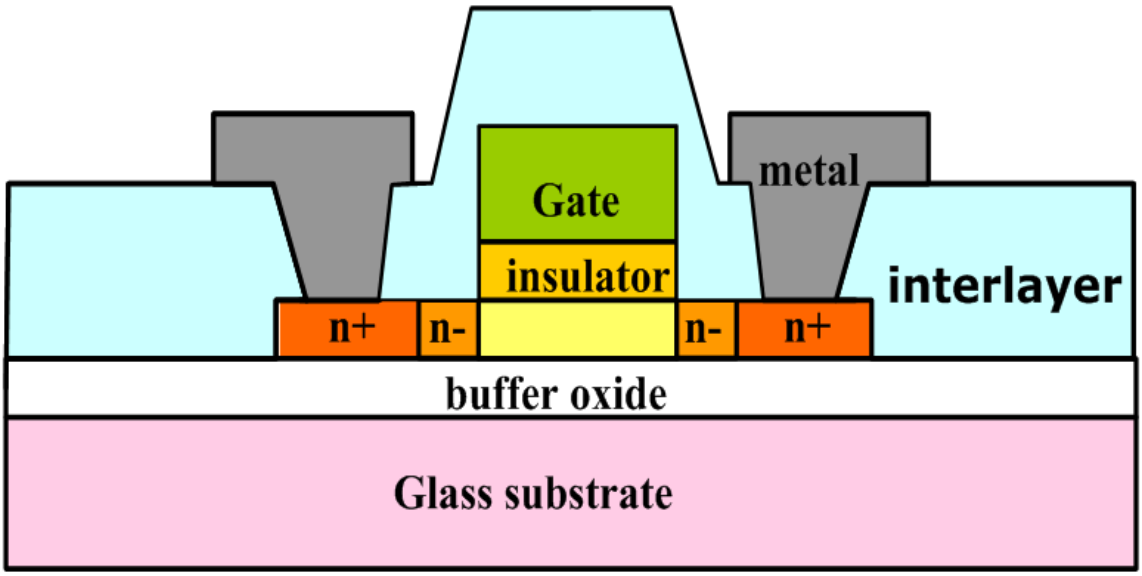


Figure 2-1 The cross-section views of n-channel LTPS TFTs with LDD structure.

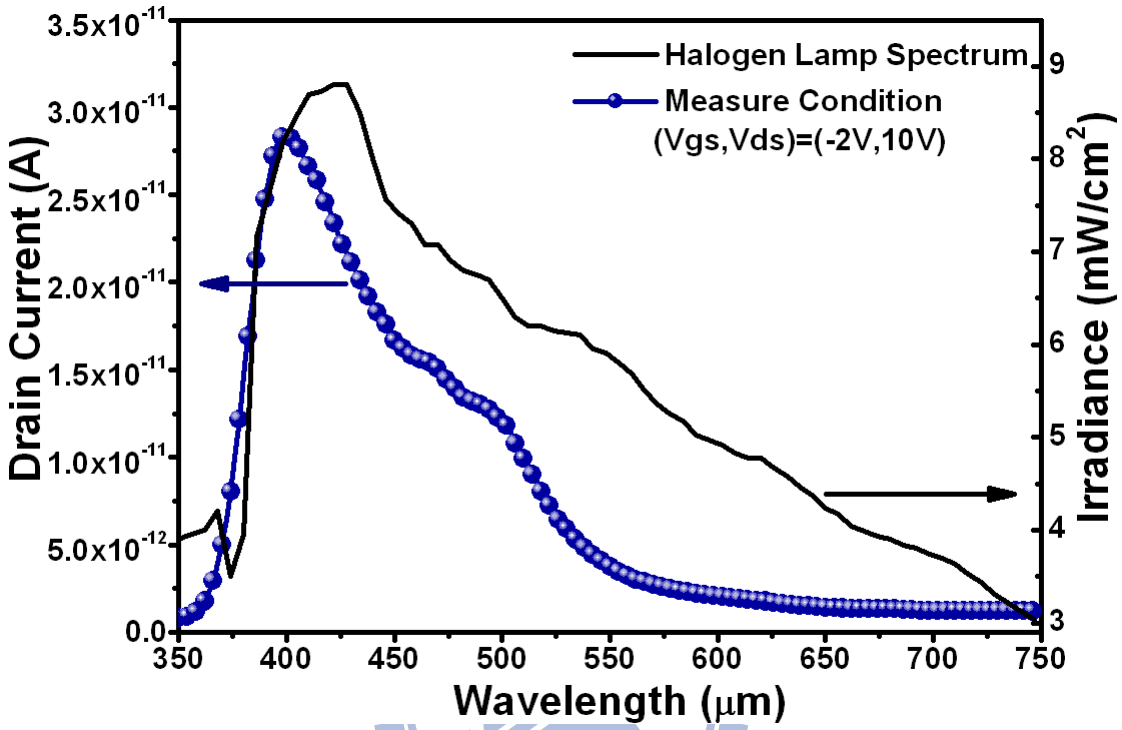


Figure 2-2 The photo leakage current and the power variation spectrum of the light source.

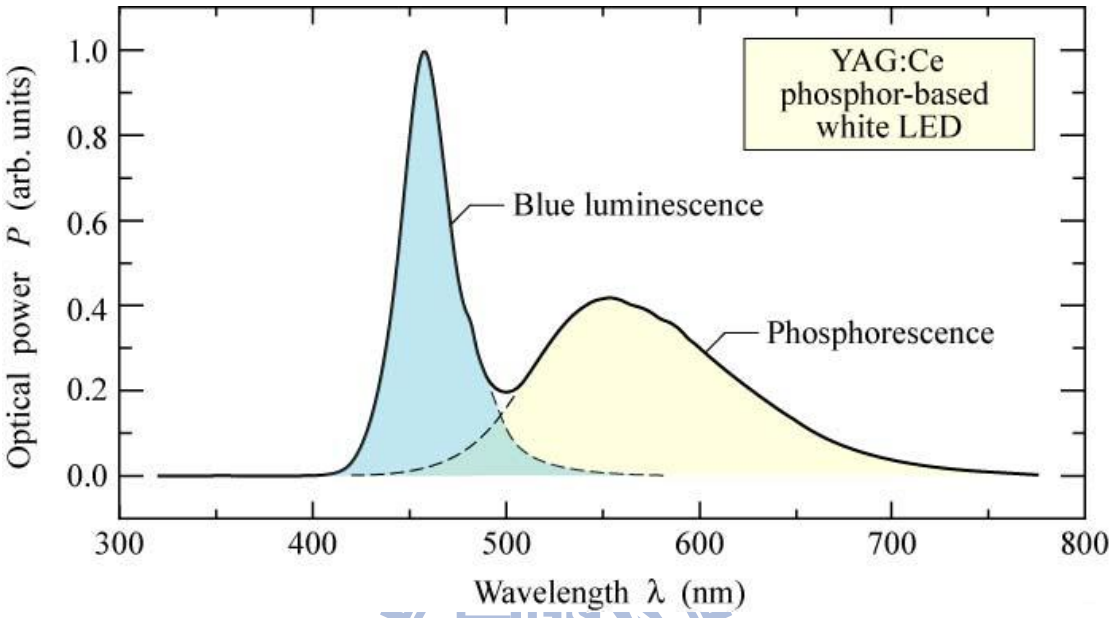


Figure 2-3 Emission spectrum of a phosphor-based white LED.


E S A
1896

Chapter 3

Photosensitivity Analysis of Low-Temperature Poly-Si Thin Film Transistor Based on Unit-Lux-Current

3.1 Introduction

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have attracted much attention for Active Matrix Liquid Crystal Display (AMLCD) and Active Matrix Organic Light Emitting Diode (AMOLED) applications due to the high mobility and the capability of realizing integrated circuits on glass. It could reduce the difficulties of the connection of the surrounding circuits and the cost of the panel [3.1]. The photosensitivity of LTPS TFTs is a significant design consideration for achieving high image quality display panels since it will affect the leakage current. Furthermore, several ambient light sensors using the off current of LTPS TFTs have been reported [3.2-3.7]. Thus, the photosensitive behavior of LTPS TFT off current is of great interest. However, this photo-induced leakage current behavior is not included in the present SPICE device model. In this work, a new parameter is used to analyze the effects of illumination on LTPS TFTs. It's dependence on the gate, drain bias and temperature. An equation is provided to properly describe ULC under various bias and temperature conditions for further exploration of photo leakage behaviors. A qualitative deduction is developed to account for the photo leakage mechanism. In addition, since LTPS TFTs suffer from huge variation owing to the diverse and complicated grain distribution in the poly-Si film [3.8], the ULC variation will also be discussed.

3.2 Classification and Characterization of Photosensitivity

3.2.1 Sensing Area Consideration

Before the mechanism of photosensitivity is discussed explicitly, it should be first examined where is the most sensitive to the illumination inside LTPS TFTs. A special layout of the TFT with U-shaped source and drain electrodes configuration is adopted in this work, as shown in Fig. 3-1. Twenty-five TFTs are arranged in parallel and separated into two groups. The upper group consists of twelve TFTs and the lower one contains thirteen TFTs. The inner electrodes (about distance 33um) of the TFTs in these two groups are shorted together and so are the outer electrodes (about distance 59um) to form the U-shaped TFT.

An irradiation optical beam with 25μm light spot radius has been used to directly shine on the device. By scanning the beam along the channel direction of U-shaped TFT, the leakage currents of the LTPS TFT are measured in two cases with the inner or the outer electrodes as drain. As shown in Fig. 3-2, anomalous two peaks of the off current are observed. When the measurement is performed with outer electrodes as drain, the distance is larger, about 66um. On the other hand, when the inner electrodes are used as the drain, the distance is shorter, about 32um. The distance between the pair peaks is consistent with device's real junction distance. It reveals the photo-induced current happens only at the drain side. Therefore, the following discussion of the photosensitivity mechanism will focus only on the drain region.

3.2.2 Definition of the index for photosensitivity and analysis

The typical I_D-V_G transfer characteristics of the LTPS TFT under illumination from dark to 31320 lux are shown in Fig. 3-3. It can be seen that the off current increases with the intensity of the incident light and it has weak gate bias dependence under

higher ambient light intensity. There are several parameters can be use to describe this behavior of the photo-induced off current. To discuss photo effect of TFTs, the previous study [3.9] used an index $R_{L/D}$ defined as the ratio of the current under illumination (I_{Total}) to the current in the dark (I_{Dark}). $R_{L/D}$ is suitable to evaluate the performance of light sensors. However, it may not be proper to be used to analyze photo leakage mechanism. As shown in Fig. 3-4, because I_{Total} is less dependent on the gate voltage, $R_{L/D}$ is mostly determined by the behavior of I_{Dark}. It can not reflect photo behaviors of TFTs. Therefore, for our discussion, it may be necessary to find another index which can eliminate the influence of I_{Dark}.

Fig. 3-5 shows the relationships between drain current and illumination intensity for several bias conditions in the off region. It can be seen that all drain currents are proportional to the amount of radiant illumination. Thus, it can be taken that the total leakage current under illumination (I_{Total}) is composed of two components: One is the leakage current that is not caused by photo illumination (I_{Dark}) which is measured under dark state. And the other part is illumination induced leakage current (I_{Illum}) which means the component induced by illumination. In this paper, we will offset I_{Dark} and only consider I_{Illum} which is defined to be the difference between I_{Total} and I_{Dark}. To analyze the photosensitivity of the LTPS TFTs in detail, we further define the slope of the curve in which the current versus illumination intensity as Unit-Lux-Current (ULC in abbreviation) to be a new index. The physical meaning of ULC is the photo leakage current induced “per unit-photo flux” and independent of the dark current. Therewith, the total off current I_{total} of LTPS TFT can be expressed as

$$I_{Total} = I_{Dark} + I_{Illum} = I_{Dark} + ULC \cdot L \qquad (3\text{-}1)$$

where L is the illumination intensity in lux.

3.3 Insight of Photosensitivity

3.3.1 Field Effects on Unit-Lux-Current

Fig. 3-6 shows gate bias dependence of ULC under different drain biases. It is obvious that ULC is change severely under higher drain voltage. Fig. 3-7 shows drain bias dependence of ULC under different gate biases. When drain voltage V_d is lower than 8V, ULC increases linearly with drain bias [3.10], and gate bias effect is negligible. However, when V_d is large enough, ULC increases with drain bias more rapidly and gate bias effect becomes significant. As shown by the arrow line in Fig. 3-7, the linear ULC curve at low drain bias can be fit, and this is one of the two components of the total ULC. This component which increases with drain bias linearly and independent of gate bias is defined as ULC_1. Then, the second component which subtracts ULC_1 from the total ULC curve is called ULC_2.

Furthermore, we plot ULC_2 in Fig. 3-8. It is apparent that the log [ULC_2] increases with drain bias linearly, indicating that ULC_2 increases with drain bias exponentially when V_d is large enough. The parallel curves of log [ULC_2] at different gate biases indicate that the dependence of gate bias is also exponential. Thus, ULC can be expressed by a linear combination of these two components as

$$ULC = ULC_1 + ULC_2 \qquad (3\text{-}2)$$

$$ULC_1 = \alpha Vd + \beta \qquad (3\text{-}3)$$

$$ULC_2 = \gamma \cdot \exp(\eta_1 Vd - \eta_2 Vg) \qquad (3\text{-}4)$$

where α, β, γ, η_1 and η_2 are all fitting parameters. α and β correspond to the linear drain voltage dependence and the zero drain bias offset of ULC_1, respectively. γ is the scaling factor of ULC_2, while η_1 and η_2 are the parameters about the exponential dependence on drain bias and negative gate bias of ULC_2. As shown in Fig.3-9, the calculated results agree with our experiment data very well. The values of fitting factors α, β, γ, η_1 and η_2 are listed in Table. 3-1.

Moreover, the mechanisms of two ULC components will be further discussed. The ULC can be taken into account both the leakage current induced in the gate-drain overlap depletion and in the lateral depletion regions [3.11]. When device is operating at the low drain voltage, the linear increase with drain bias of ULC_1 is attributed to lateral depletion region by the channel-drain junction in reverse bias. In this region, ULC_2 is negligible. When drain voltage is large enough, ULC_2 increase with drain exponentially and gate bias effect becomes significant. Several mechanisms of leakage current were discussed in previous report [3.12-3.15]. It considered that the reverse lateral depletion at drain region extends and causes gate induced drain leakage (GIDL) in gate-drain overlap depletion junction. The amount of the photo current should be associated with the carrier generation in the space charge region. By the junction reverse saturation current and GIDL, the drain current owing to the GIDL effect is also in an exponential relation. This phenomenon is similar to our case of ULC_2 component. The voltage difference between the drain and gate biases corresponds to the magnitude of electric field across the depletion region. A more negative gate bias means that the electric field would get stronger, as the same as a more positive drain bias. It suggests that larger electric field across the drain depletion region causes larger photo effect. Both drain and gate bias affects the electric field strength in the depletion region in a slightly different ways.

3.3.2 Temperature Effects on Unit-Lux-Current

We further take into account the temperature effect of ULC. Fig. 3-10 shows the illumination effect on photo leakage current at different temperatures of 25, 40, and 60^{o}C under a certain bias condition of (V_d ,V_g) = (10V, -5V). The correlation between I_{Total} and illumination intensity is still linear at various temperatures.

Drain bias dependences of ULC at different temperatures are shown in Fig. 3-11. ULC in the range of low drain bias is significantly affected by temperature. While in the higher drain bias range, the temperature effect reduces gradually. From the discussion above, we have separated the ULC intoULC_1 and ULC_2. It can be seen that ULC_1 is actually the term subject to the temperature effect. On the other hand, as shown in Fig. 3-12, ULC_2 is totally temperature independent, which means ULC_2 is the term purely induced by electric field. Therefore, ULC_1 may be induced by mechanism like excess carrier diffusion or thermionic emission and thus it has weak dependence on the electric field, especially gate bias. ULC_2 may be induced by mechanism like excess carrier drift or field emission and thus it has strong dependence on the drain and gate biases.

Since the lateral electric field is relatively small, the photo-induced current is a thermally generated current dominantly. The temperature effect on I_{Dark} can identify constant activation energy [3.16-3.17], which hints us to add the fitting factors α and β and in eq. (3-3) in the Arrhenius plot. Fig. 3-13 shows the relationship between α and β and 1/kT. These two factors increase with 1/kT exponentially and can be expressed by

$$\alpha = A \cdot \exp(-Ea_A / kT) \qquad (3\text{-}5)$$

$$\beta = B \cdot \exp(-Ea_B / kT) \qquad (3\text{-}6)$$

where Ea_A, Ea_B are the activation energies of α and β, respectively, and A, B are their corresponding fitting parameters. The fitting values of Ea_A, Ea_B, A and B are listed in the inset. By the temperature effect discussed above, it is confirmative to separate ULC into two components. ULC_1 is thermally activated and might be corresponding to the thermionic emission or carrier diffusion, while ULC_2 is independent of temperature and possible owing to field emission or carrier drift.

3.3.3 Mechanism of Unit-Lux-Current

Based on the experimental results of bias, temperature, and sensing location, a more complete mechanism of ULC is proposed to explain photosensitive effect on the leakage current of LTPS TFT. Fig. 3-14 illustrates the band diagrams under the condition of $V_g<0$ along the channel direction near the drain region at low and high drain biases. In the figure, W_d indicates the length of depletion region at the drain electrode side where electron-hole pairs can be generated under illumination in the poly-Si film. The generated electrons flow toward the drain electrode and the holes flow in the opposite direction. W_d consists of two regions. One is the high hole concentration region in the channel induced by the negative gate bias, the other is in the LDD region. The channel area is shielded by the gate metal, while the LDD region can be shined by the illumination. Based on the Poole-Frenkel effect lowering of a Coulombic barrier and phonon-assisted tunneling due to the electric field applied to a semiconductor [3.18], which enhances thermal emission and the trap-to-band field emission rate, the two components of ULC will be discuss. For the case at low drain bias with light irradiation, when the gate bias is changed, similarly to the abrupt p^+n junction, the electric field of the other part in LDD region is invariable. Thus, the gate voltage independence of the ULC_1 can be explained. As for the V_d effect, the lateral depletion region increases linearly with drain bias, corresponding to the parameter α in eq. (3). With extremely low drain bias, there is still a depletion region in LDD, in accordance with the parameter β in eq. (3). The conduction mechanism of the leakage current in the low drain field is thermal emission [3.19]. Consequently, the parameters α and of β of ULC_1 are temperature dependent.

On the other hand, for the high drain bias with light irradiation, the electric field across the lateral depletion region is large enough to fully deplete the LDD region.

Therefore, the increase of drain voltage will increase the electric field within the limited LDD length pinched by the n^+ region. In such case, the more negative gate bias will also result in the larger field with the same depletion width of the LDD region. The conduction mechanism of the leakage current at the high drain voltage is field enhanced emission in the space charge region [3.20]. The electric field dependence of ULC_2 is reflected by the slightly different values of the fitting parameters η_1 and η_2 in eq. (4).

3.3.4 Devices variation

The uniformity of LTPS TFT is always an important issue. Different devices even fabricated by the same process suffer from serious device variation, especially for the off current. For this consideration, the photo leakage currents would also vary among devices. Fig. 3-15 shows the photo leakage currents with respect to the illumination intensity of several devices on the same glass. It verifies that there is still serious device variation in the aspect of photo leakage current. The results further confirm that the mechanisms of the photosensitivity for the LTPS TFT are closely related to the different defect distribution or density in the grain boundary, alike the case of the dark off current. This issue needs to be overcome before LTPS TFTs can be practically used as the photo sensing device.

3.4 Conclusion

In this chapter, we present detail studies on the factors that affect the photo leakage current like bias condition, temperature, and defect states of the LTPS TFTs. It is found that photo leakage current always exhibits good linear dependence on

illumination intensity. Thus, a new index ULC characterizing the slope of the curve is introduced to discuss the photosensitivity. Furthermore, the mechanism of the photosensitivity for the LTPS TFTs is proposed. It relates to the width and electric field in the lateral depletion region near drain. It is also shown that ULC variation is also related to defects in the depletion region. The empirical equation of ULC provides a potential modeling for simulation of LTPS TFT circuitry considering the photo effect.

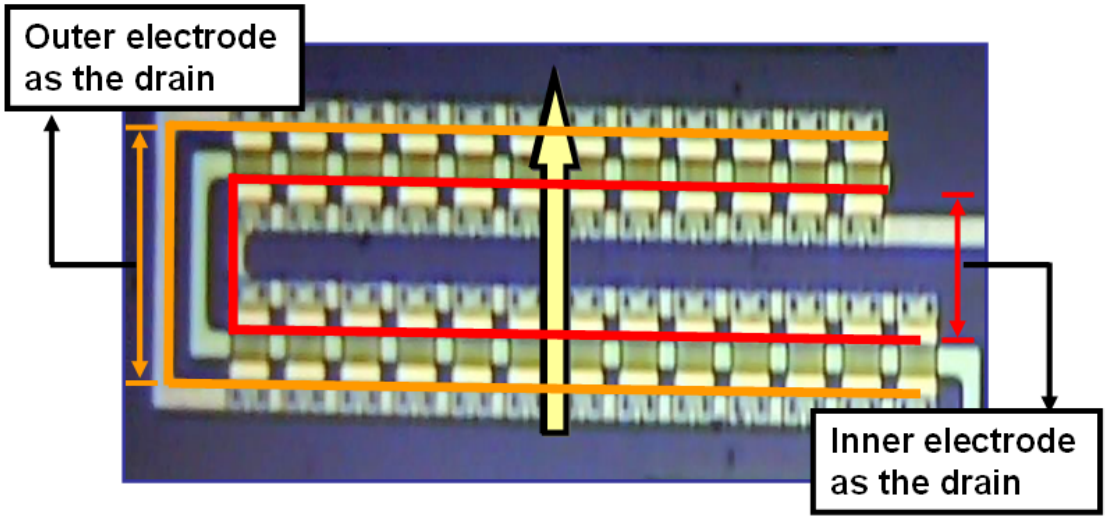


Figure 3-1 Photograph of the special U-shaped TFT with an arrow indicating the scanning path of the illumination beam.

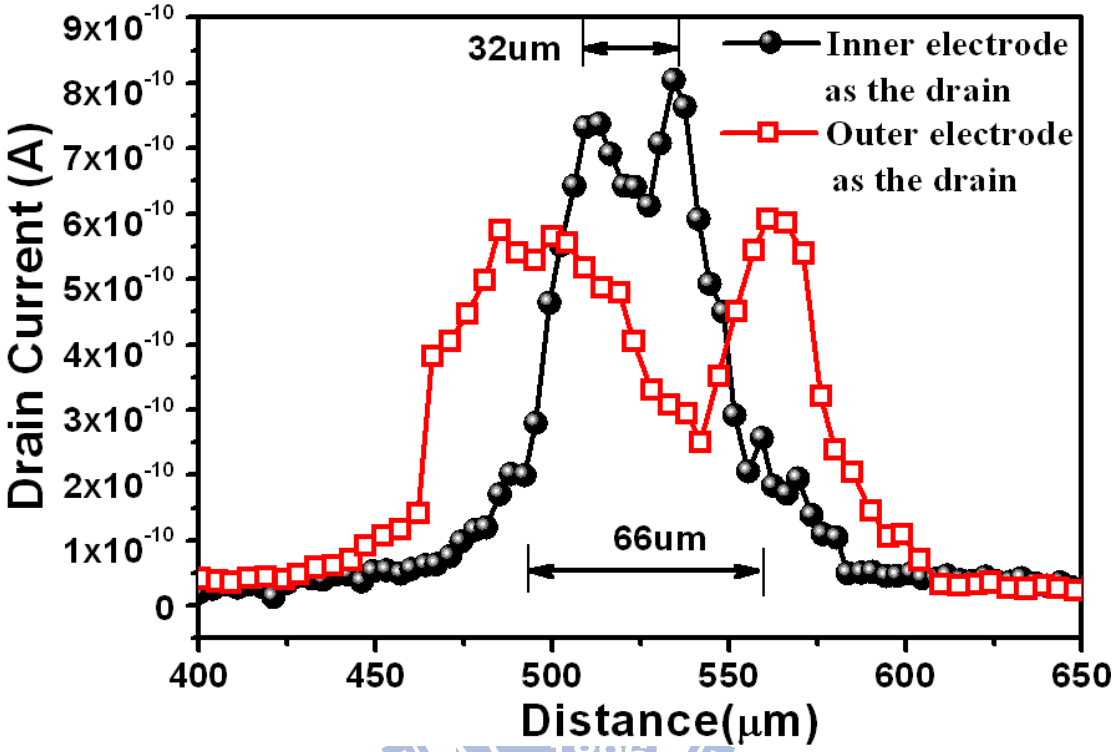


Figure 3-2 The drain current of the U-shaped TFT with the distance that the illumination beam scanning along the channel direction.

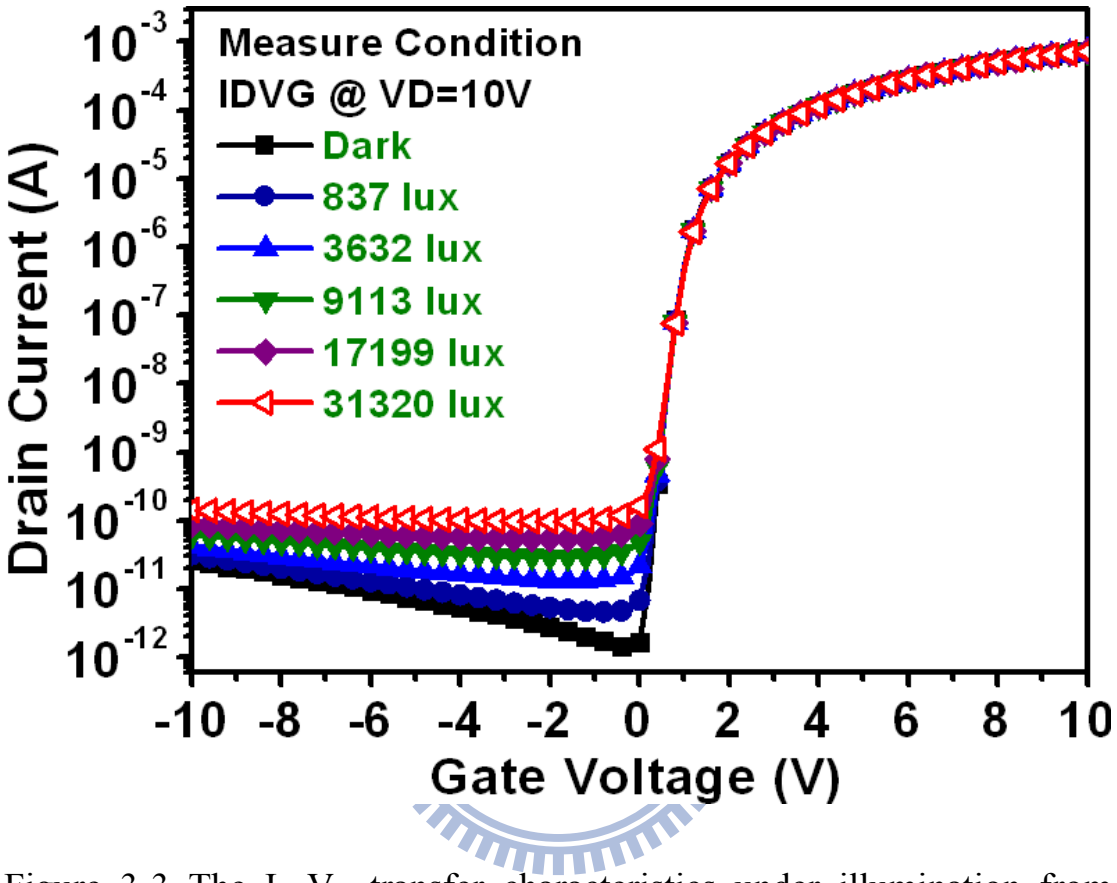


Figure 3-3 The I_D-V_G transfer characteristics under illumination from dark to 31320 lux.

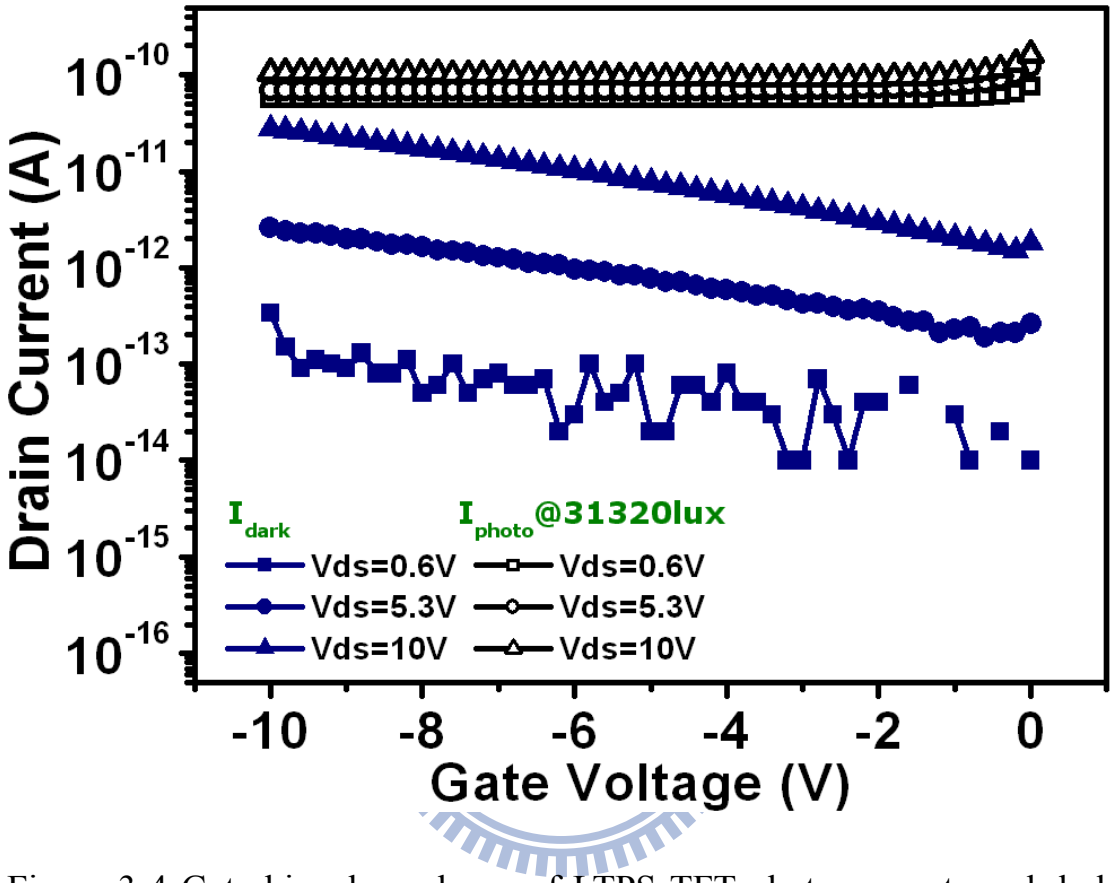


Figure 3-4 Gate bias dependence of LTPS TFT photo currents and dark currents in off region.

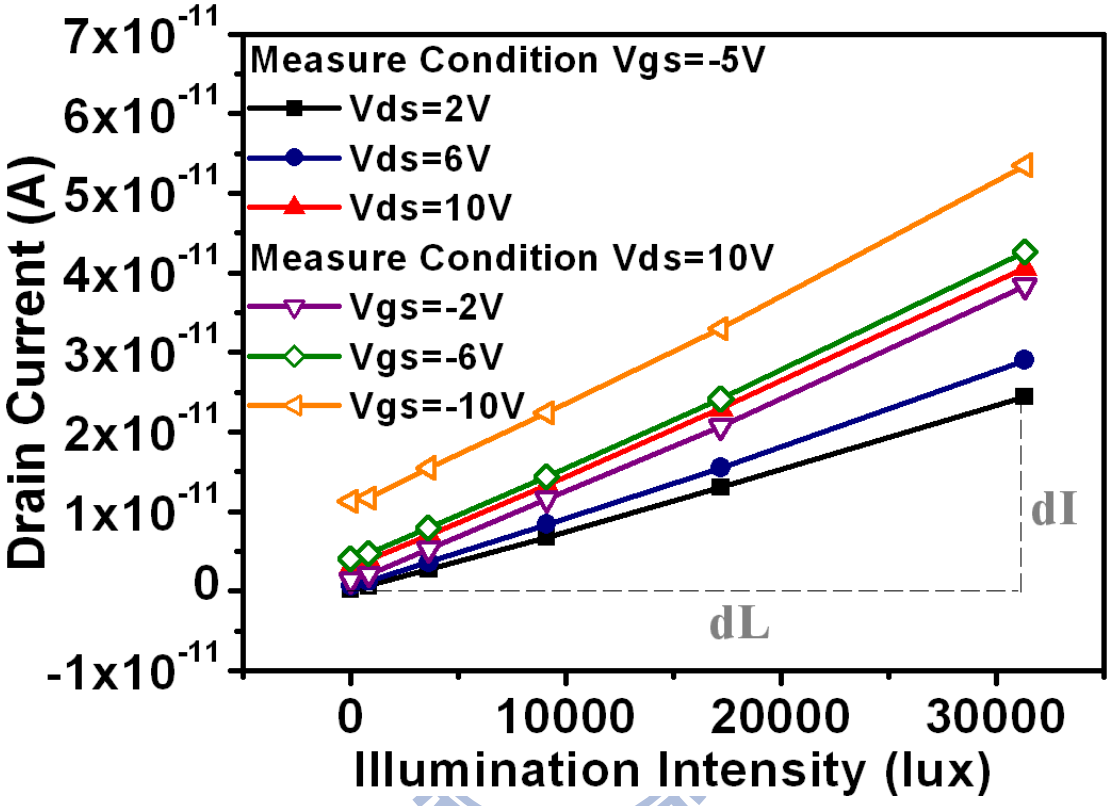


Figure 3-5 The relationship between leakage current and illumination intensity under different bias conditions.

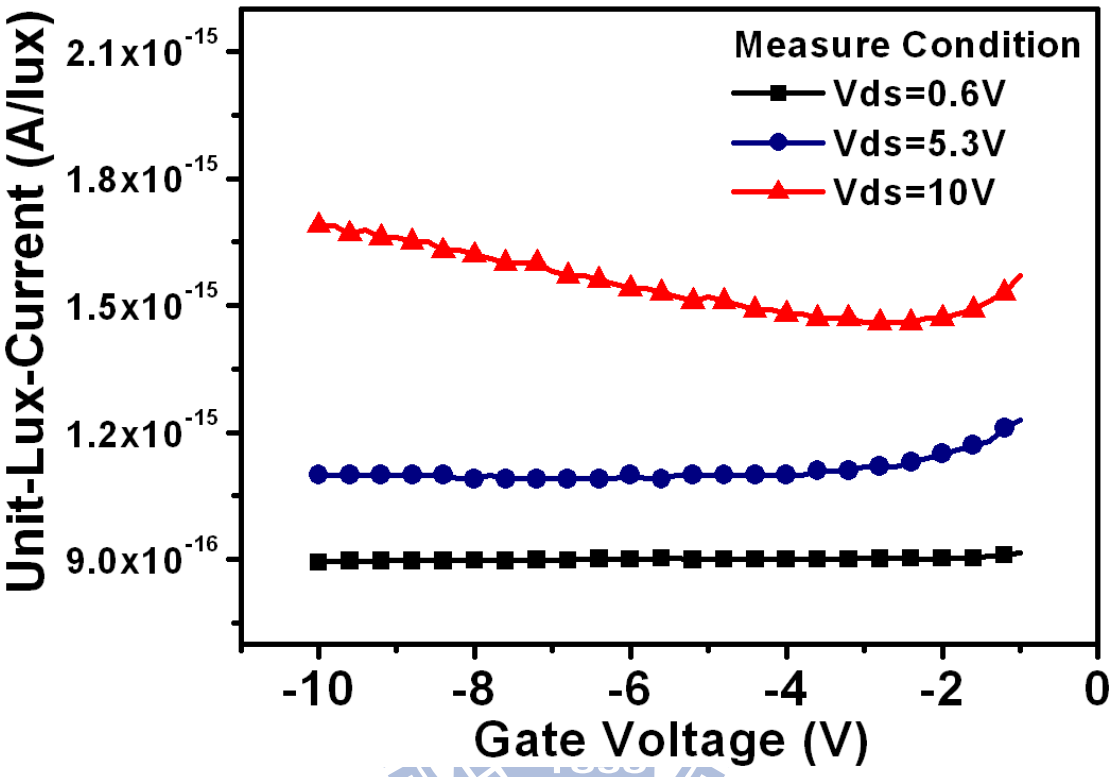


Figure 3-6 Gate bias effect on Unit-Lux-Current at different drain biases.

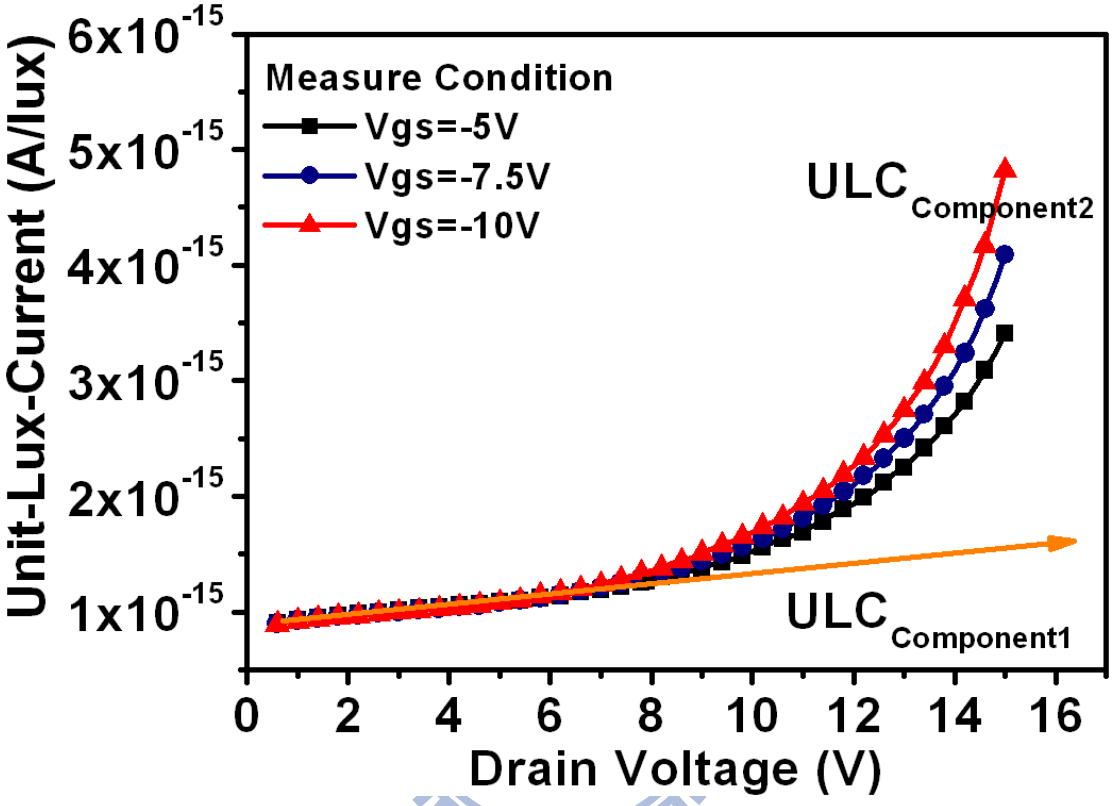


Figure 3-7 Drain bias effect on Unit-Lux-Current at different gate biases.

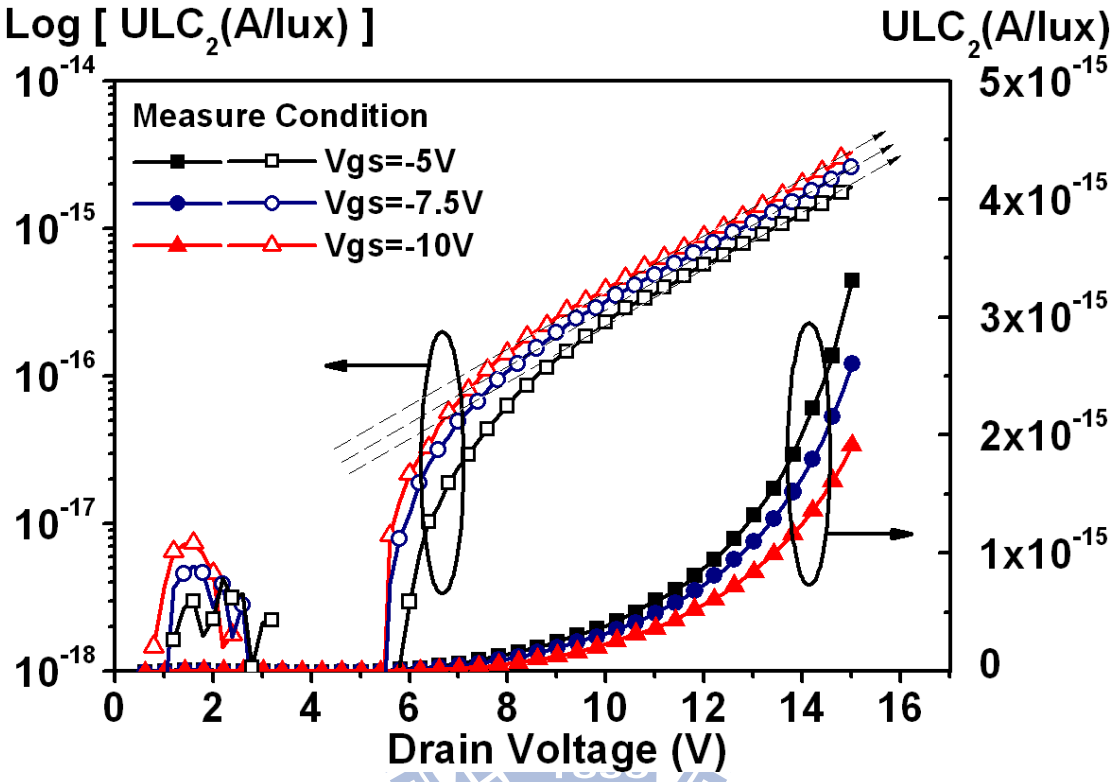


Figure 3-8 The second component of Unit-Lux-Current (ULC_2) versus drain bias at different gate voltages.

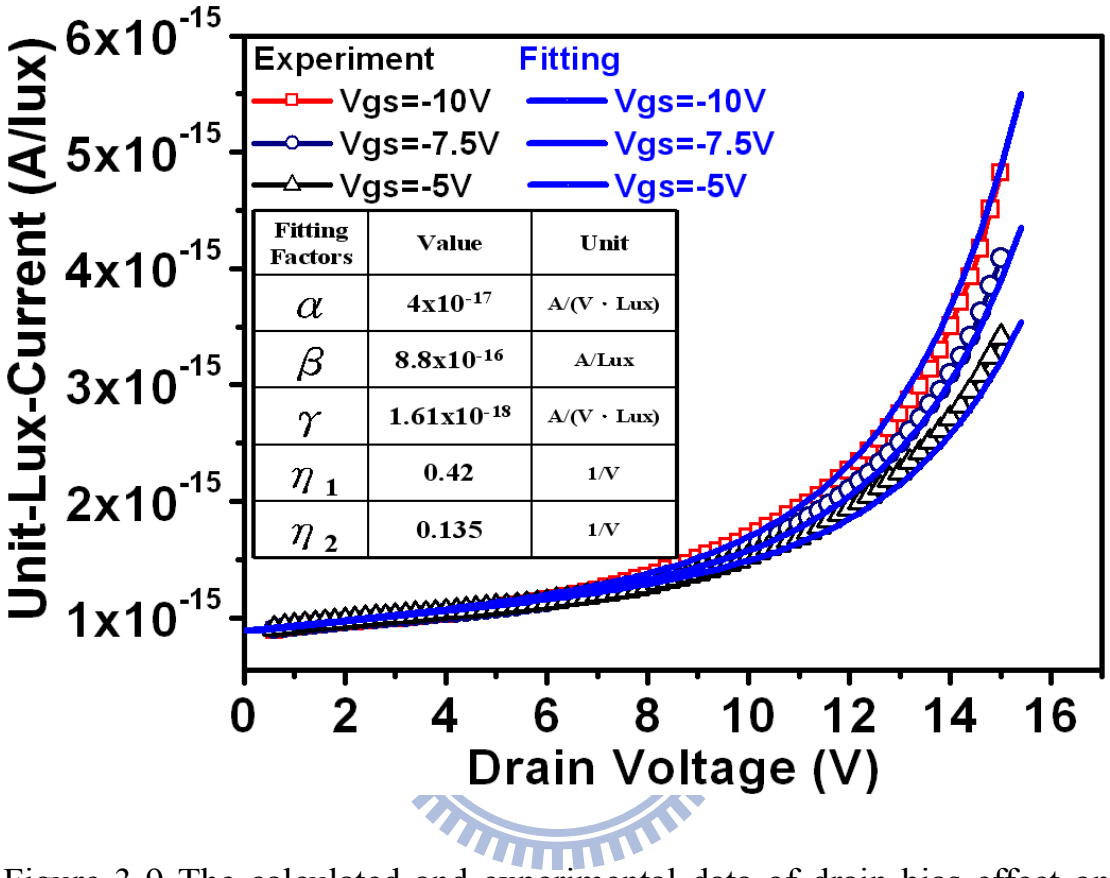


Figure 3-9 The calculated and experimental data of drain bias effect on Unit-Lux Current at different gate biases.

Fitting Factors	Value	Unit
α	4.02×10^{-17}	A/(V · Lux)
β	8.83×10^{-16}	A/(Lux)
γ	1.61×10^{-18}	A/(Lux)
η_1	0.42	1/V
η_2	0.14	1/V

Table 3-1 The values of fitting factors under front light illumination.

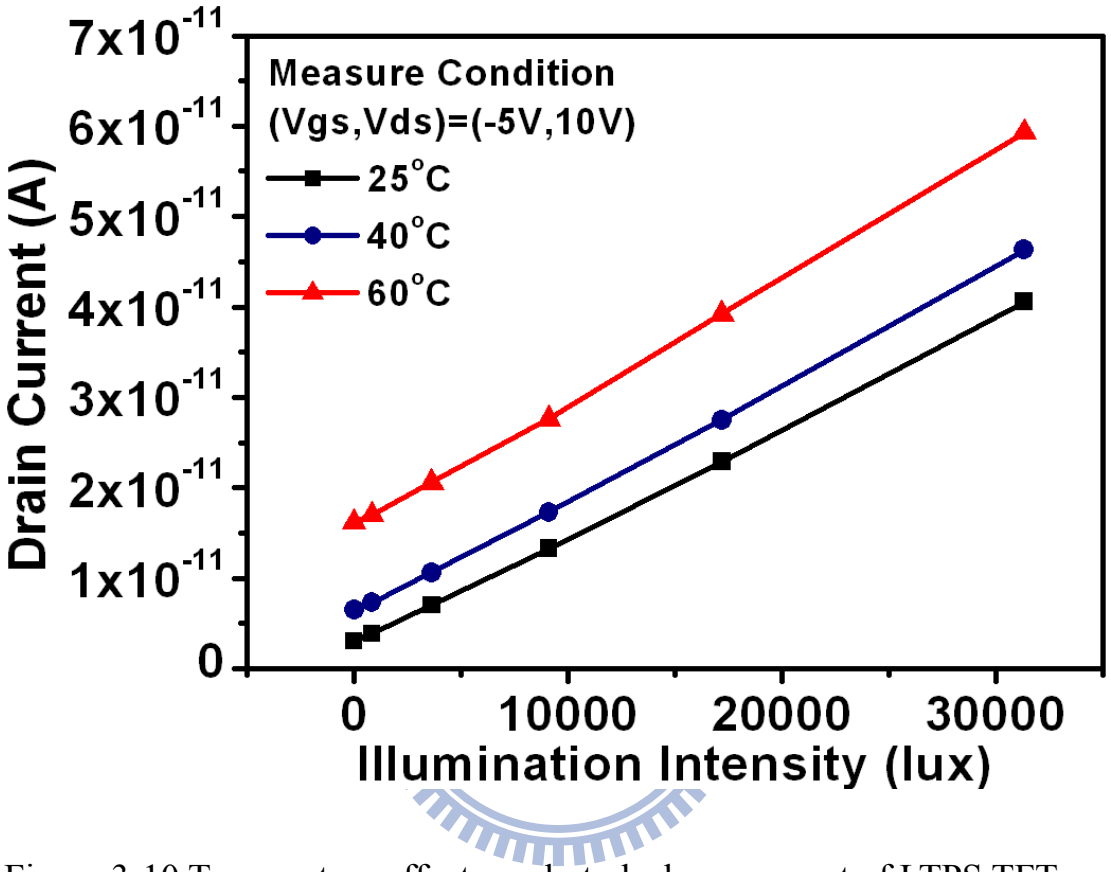


Figure 3-10 Temperature effect on photo leakage current of LTPS TFTs.

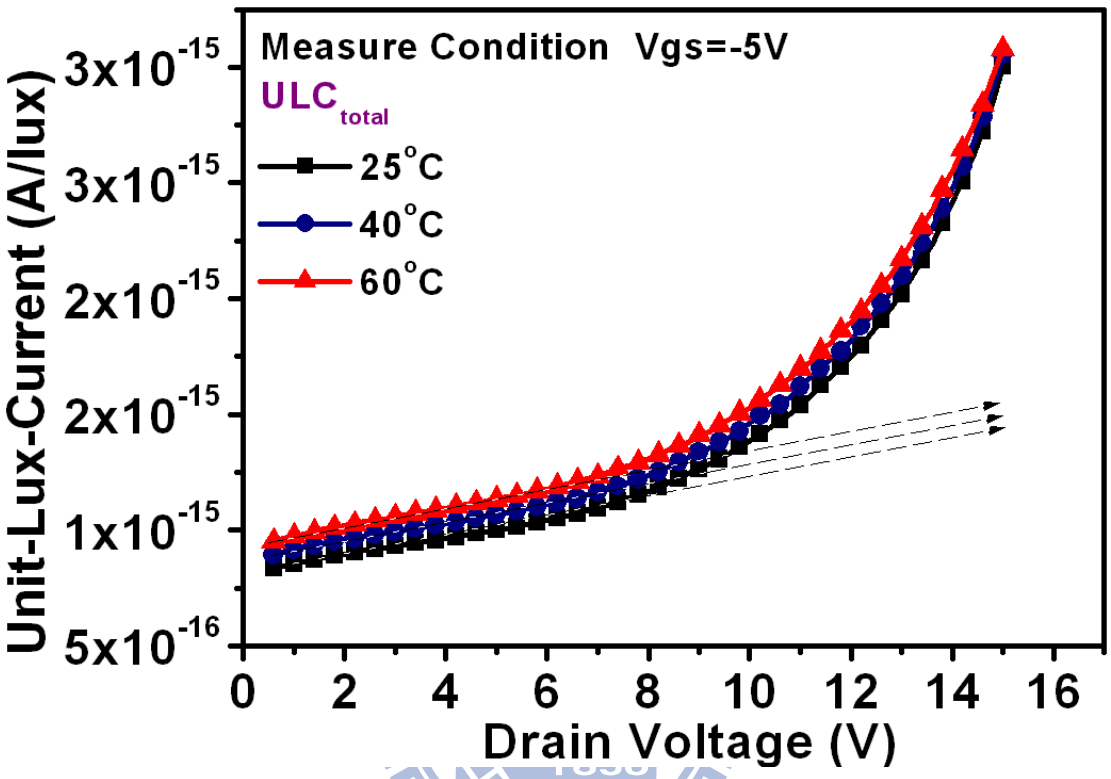


Figure 3-11 Drain bias dependence of Unit-Lux-Current at different temperatures.

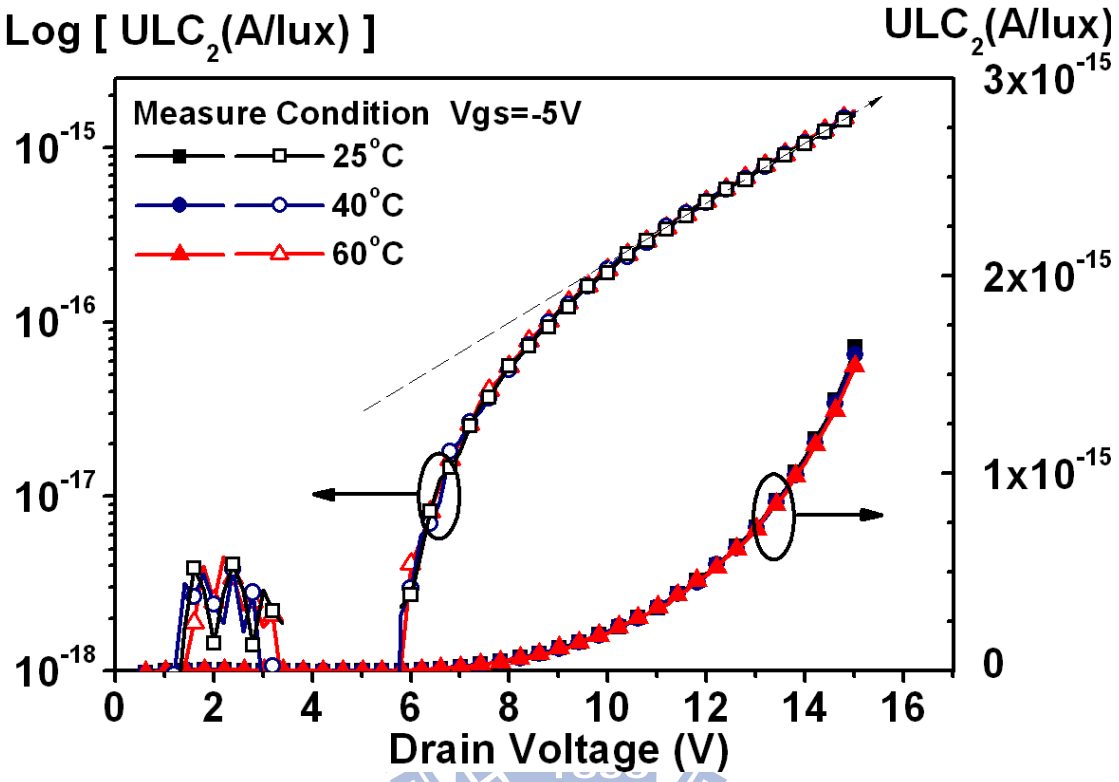


Figure 3-12 The second component of Unit-Lux-Current (ULC2) versus drain bias with different temperatures.

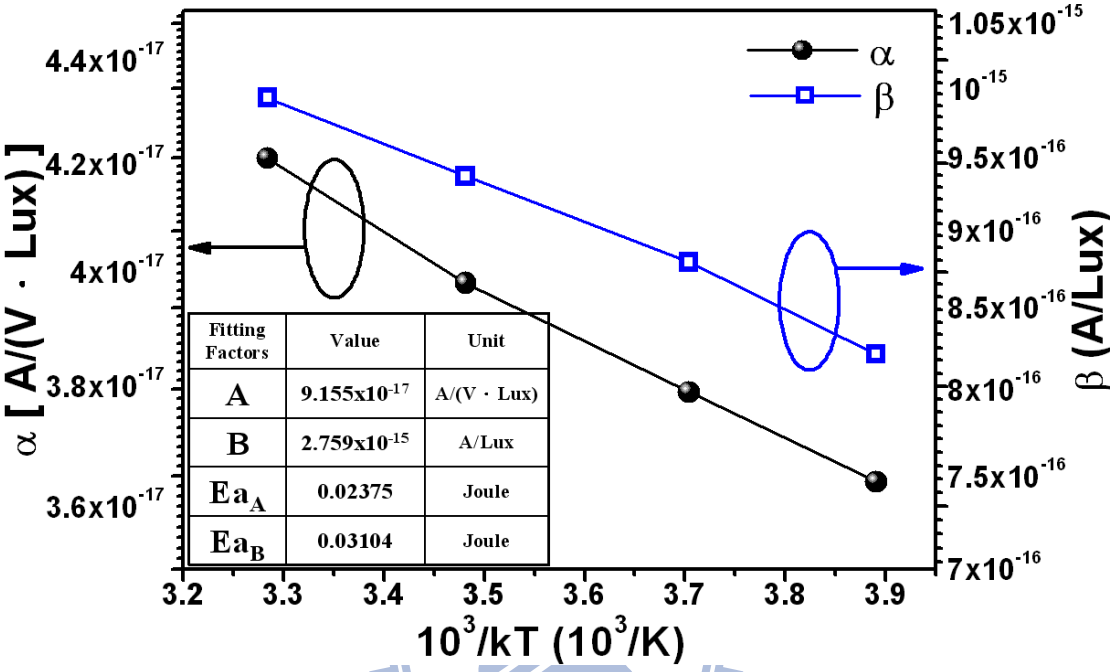


Figure 3-13 Dependence of factors α and β on temperature.

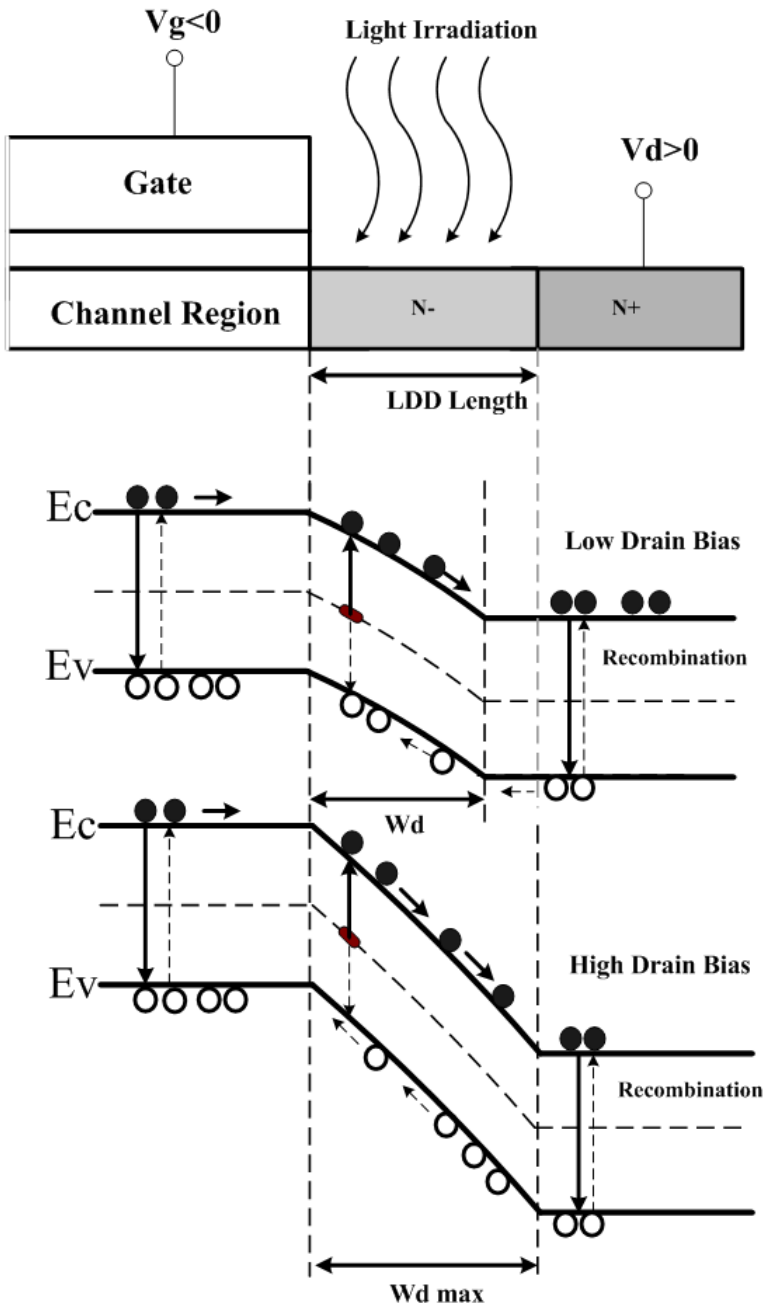


Figure 3-14 A proposed model of ULC mechanism for LTPS TFTs.

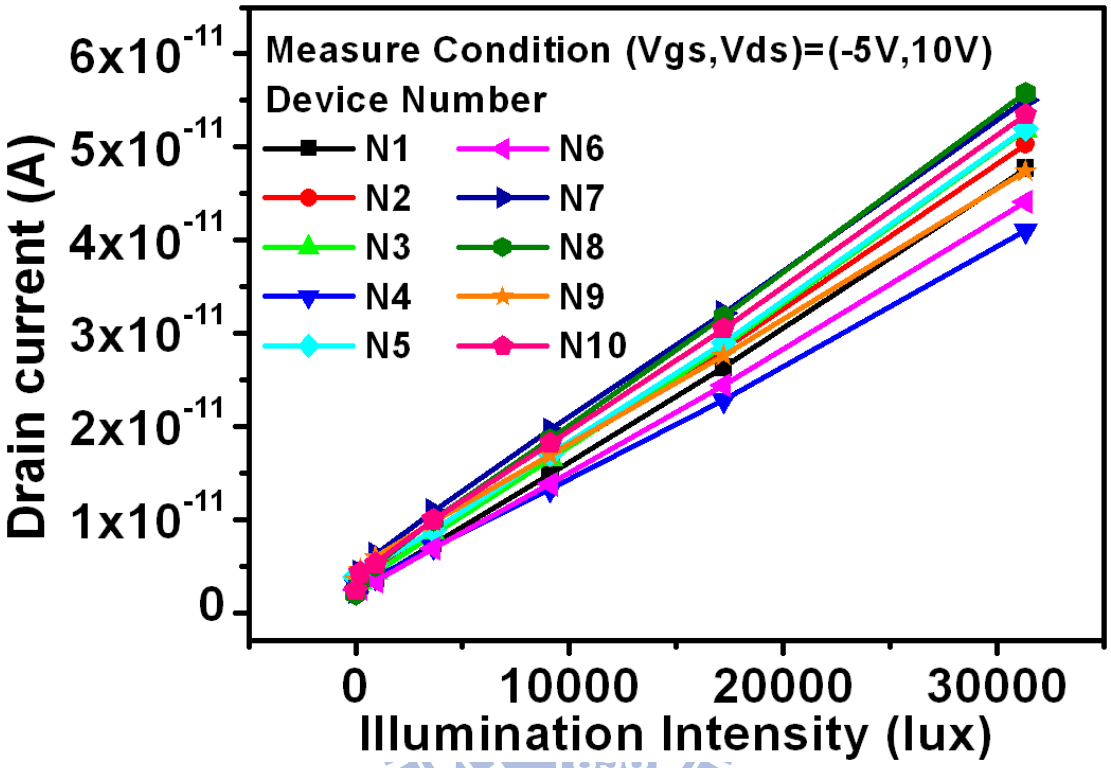


Figure 3-15 Photo leakage current variation among different devices.


E S A
1896

Chapter 4

Dependence of Photosensitive Effect on the Defects Created by DC Stress for LTPS TFTs

4.1 Introduction

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have attracted much attention for Active Matrix Liquid Crystal Display (AMLCD) and Active Matrix Organic Light Emitting Diode (AMOLED) applications due to the high mobility and the capability of realizing integrated circuits on the same glass [4.1]. For its application, several ambient light sensors using poly-Si TFTs, which is one of value-added functions for high-end flat panel display, have been reported [4.2-4.7]. The photosensitivity is a significant design consideration for achieving high image quality LCDs. However, it was reported that poly-Si TFTs suffer from several degradation mechanisms, such as hot carrier and self-heating effects [4.8]. Hot carrier effect, which was found that the degradation is related to the increase of strain bond tail states in the band gap of the poly-Si film, and damaged region, is near the drain. Self heating effect is reported interface states near the source region and the deep states in the poly-Si film near drain can be created [4.9]. It like as the SOI (Silicon on Insulator) devices, originated from the poor dissipation behavior of the substrate. As the operation voltage for V_{DS} and V_{GS} are high, the current conducting in the channel is high and the joule heat, which can be rough calculated as $P=I_{DS}*V_{DS}$, would become large and if the heat can't be dissipated in time it will be accumulated in the active region, as shown in Fig. 4-1 [4.10]. As for the main application field for poly-Si

TFTs, the devices are fabricated on glass substrates and the heat transfer coefficients for the films in the device structure are shown in Fig. 4-2 [4.11]. As can be observed in the figure, if joule heat is generated in the poly-Si film during operation, the films surrounding poly-Si film with much smaller heat transfer coefficients than poly-Si film would in turn hinder the active region from dissipating heat. Due to such degradation, the photo-induced leakage current is strongly influenced which is difficultly designed for sensing circuits. In this work, we apply both stress conditions deliberately to manipulate the defect-related photo behaviors and modify Unit-Lux-Current (ULC) [4.12] equations in TFTs. Comparatively, this work focused on how additional non-uniform defects and the photo leakage mechanism influence both lateral and gate-drain overlap depletion.

In this study, the TFTs are measured under different illumination conditions before and after bias stress. One of the stress conditions is that the drain voltage is equal to 20V and the gate voltage is 3V, which is corresponding to the hot carrier effect. The other condition of self heating stress is set to be 15V for both the gate to source voltage V_{gs} and the drain to source voltage V_{ds}.

4.2 Electrical Degradation of Poly-Si TFT under DC Stress

4.2.1 Photosensitivity Confirmation

In the previous study, it reveals the photo-induced current happens only at the drain side. To further confirm photo sensing area is mainly at the drain electrode side and photo-induced current is not affected mutually by source electrode, conventional lightly doped drain (LDD) structure and one side LDD structure of TFTs are designed for examination. Fig. 4-3 (a) and (b) show I_{ds}-V_{gs} characteristics with negative gate

bias under different illumination conditions for conventional LDD device structure and only one-side LDD device structure. It can be seen that the off current of these two types of TFTs are lifted up to the similar levels under different illumination intensities. It also reveals poly-Si TFTs leakage current occurs at the depletion region of drain junction and not influenced from source region. Therefore, the following discussion of the photosensitivity mechanism will focus only on the drain region.

4.2.2 Model Description and Analysis

In this section, we take into account, the photo leakage current induced per unit-photo flux, Unit-Lux-Current (ULC in abbreviation) [4.10] to analyze the photosensitivity of the LTPS TFTs. ULC can be expressed by a linear combination of two components, both the leakage current induced in the lateral depletion and in the gate-drain overlap depletion regions [4.13]. When device is operating at the low drain voltage, ULC is attributed to lateral depletion region by the channel-drain junction in reverse bias. When drain voltage is large enough, ULC increase considered that the reverse lateral depletion at drain region extends as gate-drain overlap depletion junction. However, the photosensitivity of the LTPS TFTs is influenced from different both defect states distribution and density in the drain depletion region. Thus, in the aspect of poly-Si TFTs under electrical stress, additional defects created close drain depletion region, ULC is drastically varied after hot carrier and self-heating degradation, consequently.

As shown in Fig. 4-4 (a) (b), the I_{ds}-V_{gs} transfer characteristics with 1V drain voltage before and after hot carrier and self heating stress under different illumination conditions. In the previous study [4.14], it is revealed that photo-induced current tendency is changed oppositely by different stress conditions in lateral depletion

region by the channel-drain junction in reverse bias. It increases in the case of hot carrier, while it decreases for self heating. Meanwhile, it correlated the photosensitivity with device parameters such as mobility or threshold voltage, on the LTPS TFTs. Fig. 4-5 (a) show normalized ULC and mobility at V_{ds}=0.6V and 10V in accordance with stress time for hot carrier stress. The variation trends have been normalized, and then we can pay attention on the tendencies of these unit parameters. As figure shown, it reveals most trap states generated by hot carrier stress are crowded near drain junction side. In contrast, normalized ULC and threshold voltage at V_{ds}=0.6V and 10V in accordance with stress time for self heating stress are compared in Fig. 4-5 (b). It demonstrates that extra defect states created by self heating stress are spread in the whole poly-Si thin film through out the channel. From above mention, non-uniformly defect distributions after dc stress cause previous ULC equations not agree with experiment data very well. Therefore, the following discussion will focus on modifying ULC equations accurately for not only lateral but also gate-drain overlap depletion.

4.3 Insight of Defect-Related Photosensitivity

4.3.1 Empirical Defect-Related Unit-Lux-Current Model

Several mechanisms of leakage current were discussed in previous report [4.15-4.18]. For the purpose of effective medium modeling characteristics, we consider poly-Si to be a material with uniformly distributed trap density. Due to the photocurrent behaviors of LTPS TFTs concern with different types of additional non-uniform defects generated from various stress conditions, we suggest an empirical defect-related Unit-Lux-Current model to describe photosensitivity of the LTPS TFT after device degradation.

For analyzing trap-assisted leakage mechanism explicitly, an index Vdx used to further divide ULC into ULC_1 and ULC_2 to individually describe the influence of lateral field and vertical field effects. At low drain bias, since the lateral electric field is relatively small, it considered that the photo-induced current is a thermally generated current dominantly. It hints us to adjust drain-bias dependence of Unit-Lux-Current model to approximately exponential forms. At higher drain bias, it considered that the reverse lateral depletion at drain region extends enhance vertical field effect and causes gate induced drain leakage (GIDL) in gate-drain overlap depletion junction. The amount of the photo current should be associated with the carrier generation in the space charge region. By the junction reverse saturation current and GIDL, the ULC_2 owing to the GIDL effect is also in an exponential relation. Base on conductivity limited by grain boundaries of semi-empirical analytical model. Thus, ULC can be modified by a linear combination of these two components as

$$ULC = ULC_1 + ULC_2 \qquad (4\text{-}1)$$

$$ULC_1 = A_1 \cdot \{\exp[B_1(Vd - Vdx)] - 1\} + \chi \qquad (4\text{-}2)$$

$$ULC_2 = A_2 \cdot \exp(-\eta \cdot Vg) \cdot \{\exp[B_2(Vd - Vdx)] - 1\} \qquad (4\text{-}3)$$

where V_{dx} is an indication boundary drain voltage which demarcated the lateral depletion and gate-drain overlap depletion region. (We can subtract ULC_1 from the total ULC curve. The rest part of the total ULC is the second component called ULC_2. The drain bias which makes Unit-Lux-Current from zero to positive point is an indication boundary.) χ is corresponding to photo leakage current induced by per unit-photo flux at V_{dx} (It is about 6.3V~6.46V before stress). A_1, A_2, B_1, B_2 and η are all fitting parameters. A_1 and A_2 are corresponded to defect-related coefficients of ULC_1 and ULC_2 respectively. B_1 and B_2 are drain voltage dependence from dc stress

per unit depletion area. η is the scaling factor of ULC_2 about the exponential dependence on negative gate bias of ULC_2.

4.3.2 Hot Carrier Effects on Unit-Lux-Current

The stress condition is that the drain voltage is equal to 12V and the gate voltage is 3V, which measured at different stress times of 1, 5, 25, 100, 500, 1000 sec to investigate the hot carrier effect on Unit-Lux-Current. The ULC at V_{gs}=-5V with different stress times is shows in Fig. 4-6. Similarly, for analyzing photosensitivity on the defects influenced by lateral and vertical field effects, we also divide ULC measurement data into two components. It can be seen that the ULC increase and distort slightly at lower drain bias with stress times. However, when device operates at higher enough drain bias, the photo-induced current is severely decreased. The calculated and experimental data of drain bias effect on Unit-Lux-Current with different hot carrier stress times are individually shown in Fig. 4-7 (a) (b). It observed the calculated results agree with our experiment data very well. Fig. 4-8 (a) (b) shows the fitting factors A_1, A_2 and B_1, B_2 of modified ULC_1 and ULC_2 equations in eq. (4-2) (4-3) at V_{gs}=-5V after hot carrier stress. It is noticed that drain voltage dependence per unit depletion area, B_1 and B_2, are raised with stress times. The tendency of defect-related coefficients, A_1 and A_2, of ULC_1 and ULC_2, are reduced with stress times. It may attribute to the photo re-excited carriers increase and carriers transit slowly by trap hopping.

4.3.3 Self Heating Effects on Unit-Lux-Current

The stress condition is that the drain voltage is set to be 15V for both V_{gs} and the

V_{ds}, which measured at different stress times of 1, 5, 25, 100, 500, 1000 sec to investigate the self heating effect on Unit-Lux-Current. The ULC at V_{gs}=-5V with different stress times is shows in Fig. 4-9. By dividing ULC measurement data into two components, it is obvious that the ULC decrease under lower drain voltage and almost the same at higher drain bias with various stress time. In view of such condition, Fig. 4-10 (a) (b) show the calculated and experimental data of drain bias effect on Unit-Lux-Current with different self heating stress times. Similarly, Fig. 4-11 (a) (b) shows the fitting factors of modified ULC_1 and ULC_2 equations in eq. (3) (4) at V_{gs}=-5V after self heating stress. It appears that, B_1 and B_2, A_1 and A_2, nearly unchanged with various stress times. Even though hot carrier and self heating stress affect the device photosensitivity in a slightly different ways, verified ULC equations are still consisted with properly the illumination behaviors after self heating stress.

4.3.4 Mechanism of Unit-Lux-Current

The According to the experimental results of two stress conditions, a more complete mechanism of defect-related ULC is proposed to explain photosensitive effect on the leakage current of LTPS TFT after dc stress.

In previous chapter, for unstressed devices, it consists of LDD region and the high hole concentration region in the channel induced by the negative gate bias. The generated electrons move along drain electrode and the holes flow toward channel direction. For the case of devices at low drain bias with light irradiation, when the gate bias is changed, channel/LDD junction is similar to the abrupt p^+n^- junction. As the lateral depletion region increases with drain bias, the ULC_1 of conduction mechanism in the low drain field is thermal emission [4.19]. On the other hand, for the high drain bias with light irradiation, the gate-drain overlap depletion region

increases with both drain and gate bias, the ULC_2 of conduction mechanism at the high drain voltage is field enhanced emission in the space charge region [4.20].

As can be seen in Fig. 4-12, the band diagrams of devices which are after hot carrier stress under the condition of $V_g<0$ along the channel direction near the drain region at low and high drain biases, respectively. When the LTPS TFT devices after hot carrier stress are under optical illumination, the numerous electron-hole pairs from additionally created shallow tail states are generated in the lateral depletion region. Therefore, the photo leakage current obviously increases due to the photo-induced carriers from the extra states created. Fig. 4-13 provides the photo leakage current spectrum of the light source in the range of 350-750 nm at lower bias after hot carrier stress. Furthermore, it observed electron-hole pairs created via shallow sub-gap to improved long wavelength absorption. Nevertheless, in the gate-drain overlap depletion region, because the channel area is shielded by the gate metal, photo excited carriers was not induced by irradiation stream. In the meanwhile, excess tail states close to conduction band and valence band make the hopping of carriers by trap-assisted and Poole-Frenkel tunneling difficultly [4.21].

Considering that poly-Si TFTs are after self heating degradation, Fig. 4-14 shows the band diagrams under the condition of $V_g<0$ along the channel direction near the drain region at high drain biases. Symbols at mid-gap of energy level are additional non-uniform defects. When devices after self heating stress, the high temperature in the poly-Si film can release hydrogen and cause plenty of dangling bonds as deep states. From Shockley-Read Hall theory of recombination, the equations are expressed as:

$$R_n = R_p = \frac{C_n C_p N_t (np - n_i^{\,2})}{C_n (n + n') + C_p (p + p')} \equiv R \qquad (4\text{-}4)$$

For simplicity, the capture rate coefficients are assumed to be the same for both

electron and holes i.e. $C_n=C_p=C$, the equation can be rewritten as:

$$R = \frac{CN_t(np - n_i^2)}{n + p + 2n_i Cosh[(E_t - E_i)/kt]} \qquad (4\text{-}5)$$

From equation (4-5), the driving force for the recombination proportion ($np\text{-}ni^2$) and trap level near mid-gap are the most efficient recombination center. These deep states near mid level, in the lateral depletion region, can recombine the electron-hole pairs generated by irradiation. Even though the photo-induced carriers might also excite due to the extra defects, the total current is eventually reduced by much recombination deep states. Fig. 4-15 provides the photo leakage current spectrum of the light source in the range of 350-750 nm at lower bias after self heating stress. It's noticed photo leakage current decreased certainly. On the other hand, in the gate-drain overlap depletion region, because hole concentration of channel/LDD junction formed abrupt p^+n^- junction are accumulated by gate electrodes. The accumulated holes captured by extra deep states in gate-drain overlap region allow hole concentration less slightly. It makes channel/LDD junction with an abrupt high-low junction (p^+pn^- junction in this case). Besides, p^+p junction form low resistance ohmic contact for majority carriers (holes). Minority carriers (electrons) therefore considered lower recombination velocity relatively. This phenomenon cause ULC2 not decrease dramatically after self heating stress.

4.4 Conclusion

In this chapter, we apply hot carrier and self heating stress conditions deliberately to correlate the photosensitivity with different types of defects on the LTPS TFTs. This analysis allows us to understand the role of different type of defects result in anomalous photo current. Furthermore, based on both trap-assisted and Poole-Frenkel

effect, a modified defect-related Unit-Lux-Current (ULC) model for TFT is proposed to explain the illumination behaviors corresponding to the defects created both dc stresses near the drain region. The empirical equation of ULC provides a potential modeling for simulation of LTPS TFT circuitry considering the photo effect after DC stress.

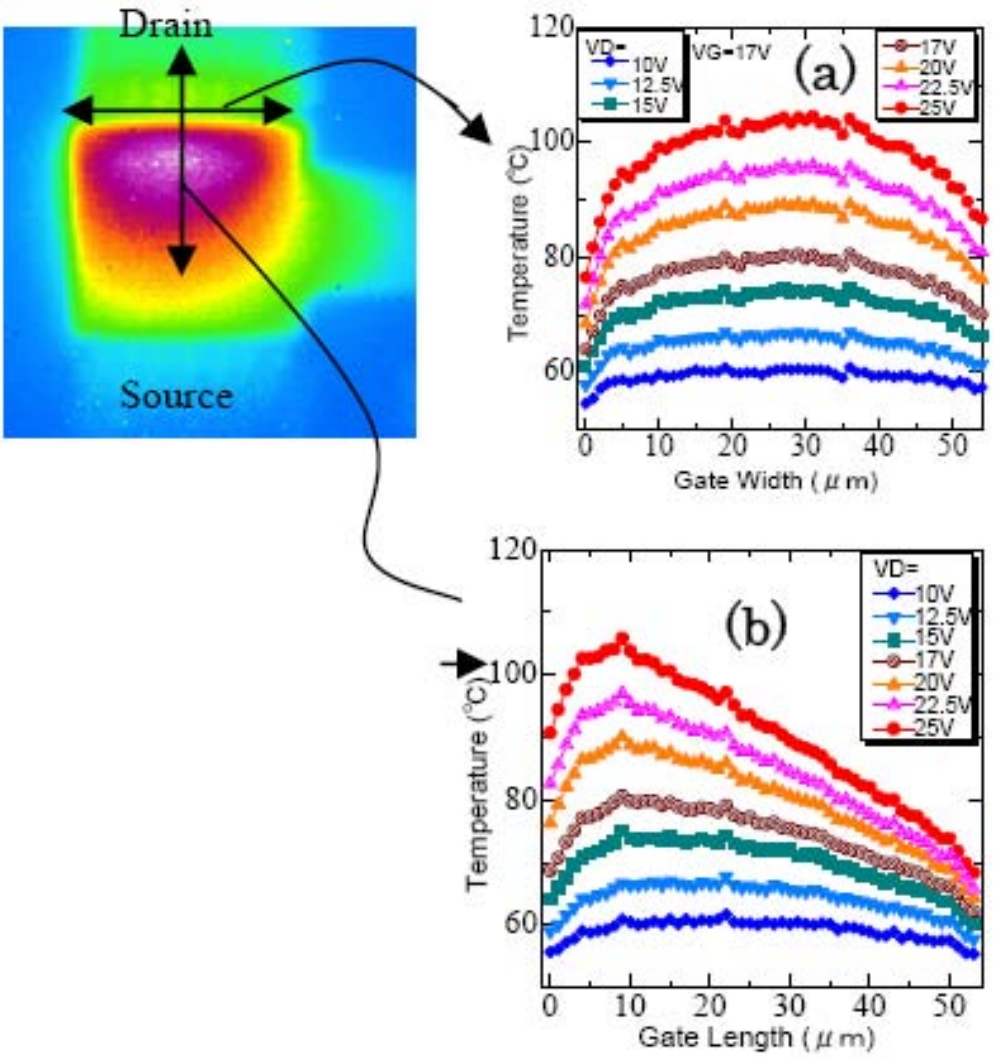


Figure 4-1 The profile of Joule heat generated in the channel for the device under self heating stress.

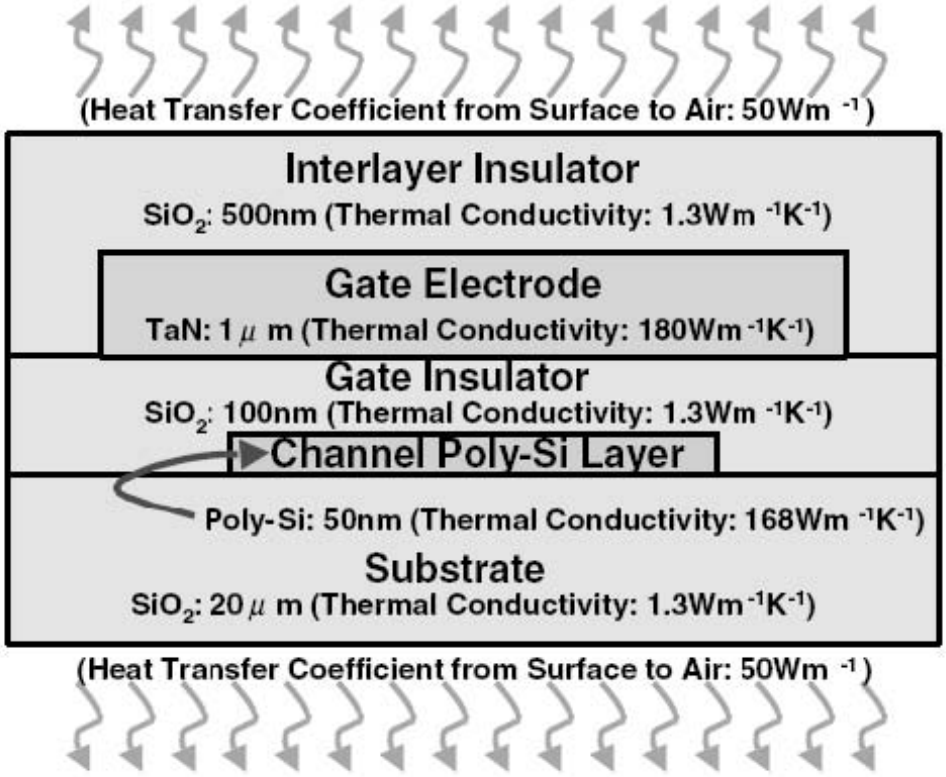
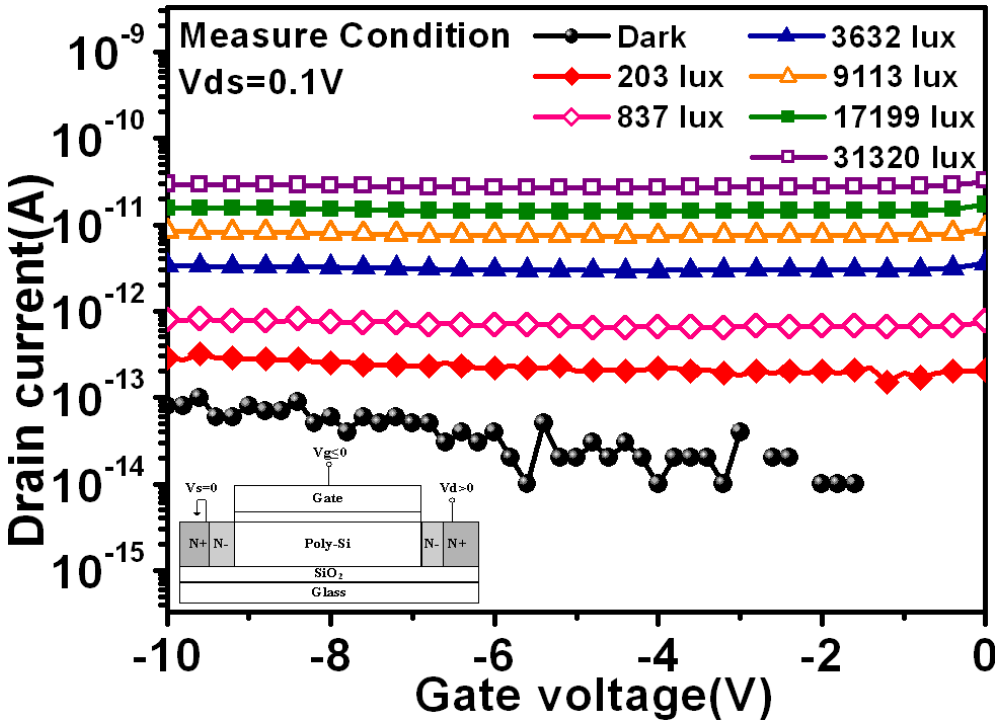
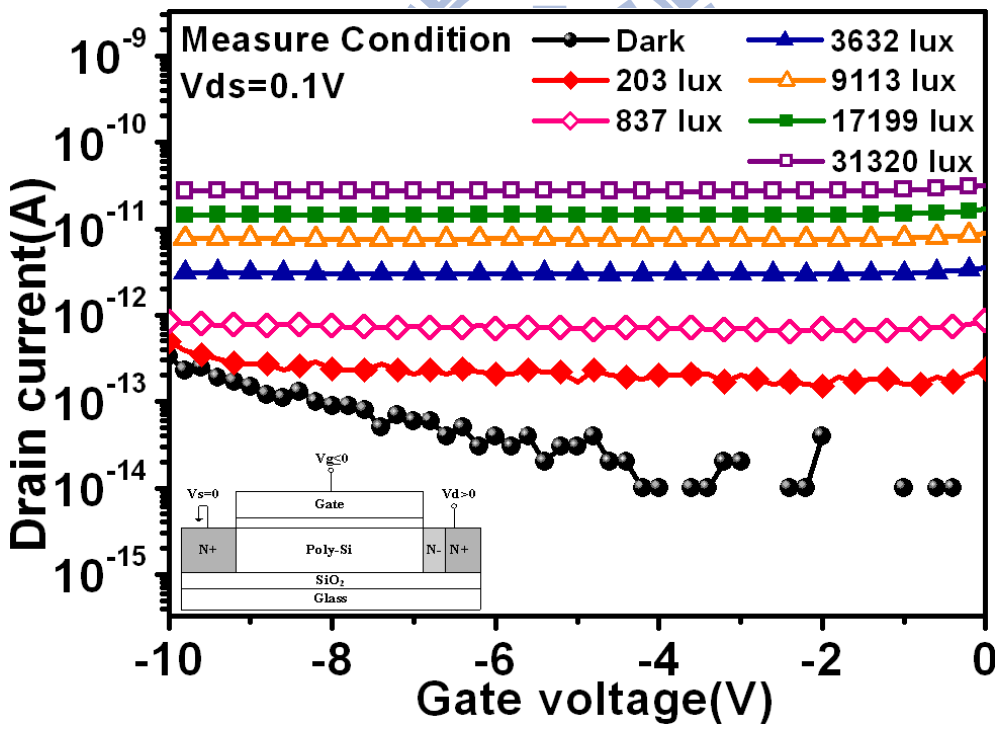


Figure 4-2 The comparison for the heat transfer coefficients of the films for the poly-Si TFTs.

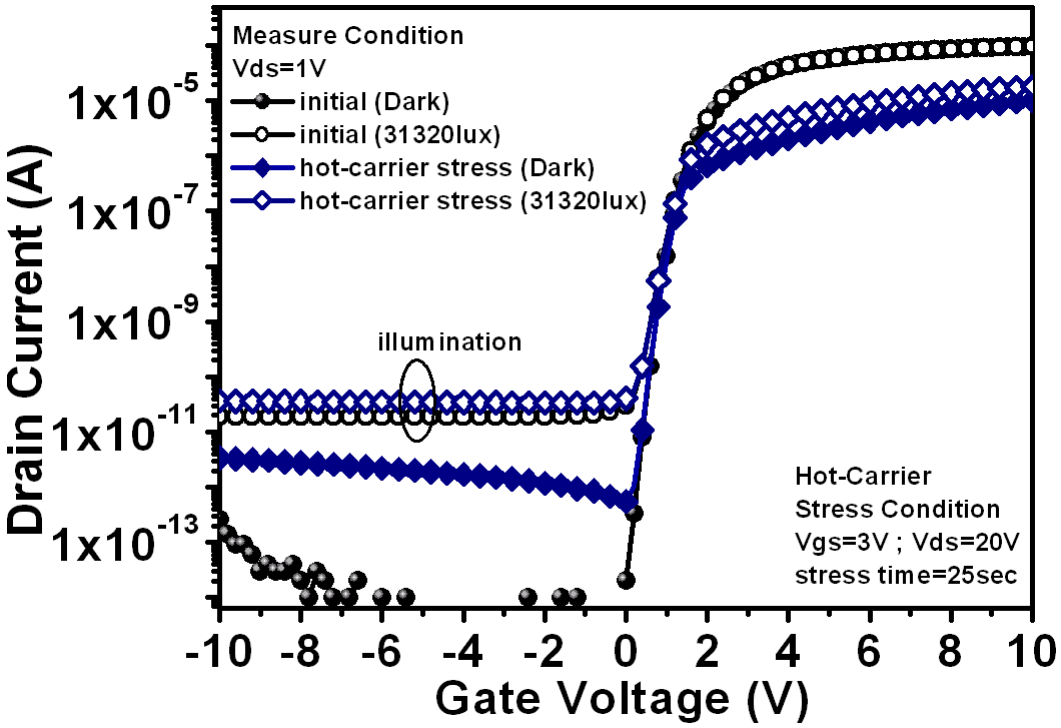


(a)

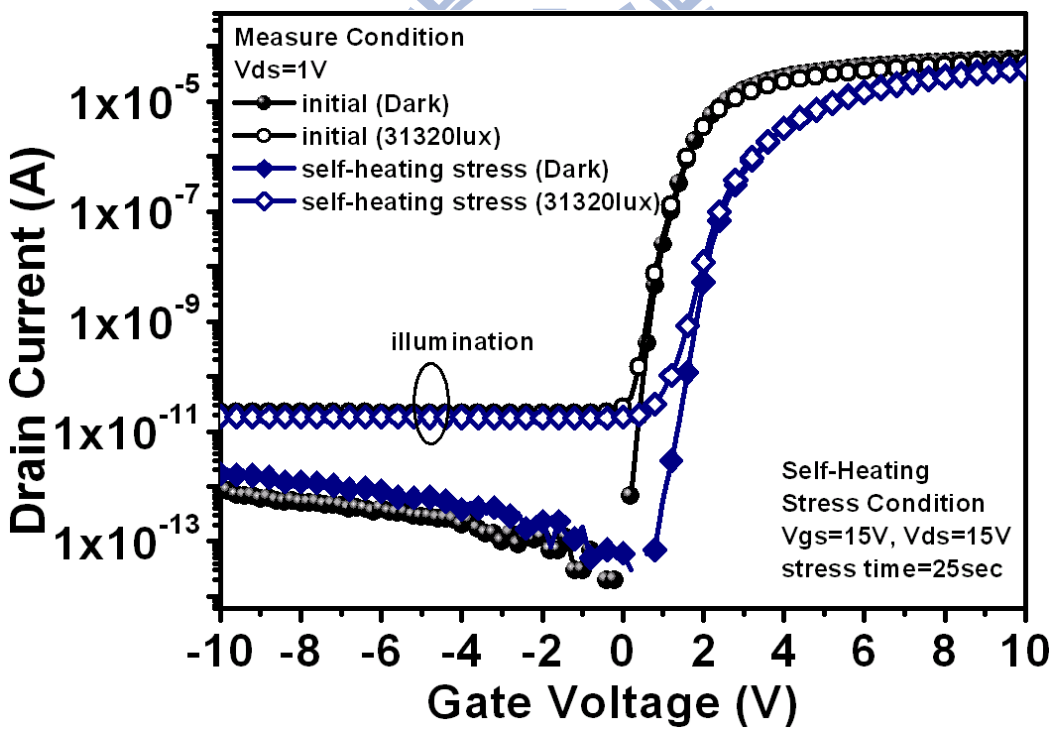


(b)

Figure 4-3 The I_{ds}-V_{gs} transfer characteristics under different illumination conditions for (a) conventional LDD and (b) only one-side LDD device structures.

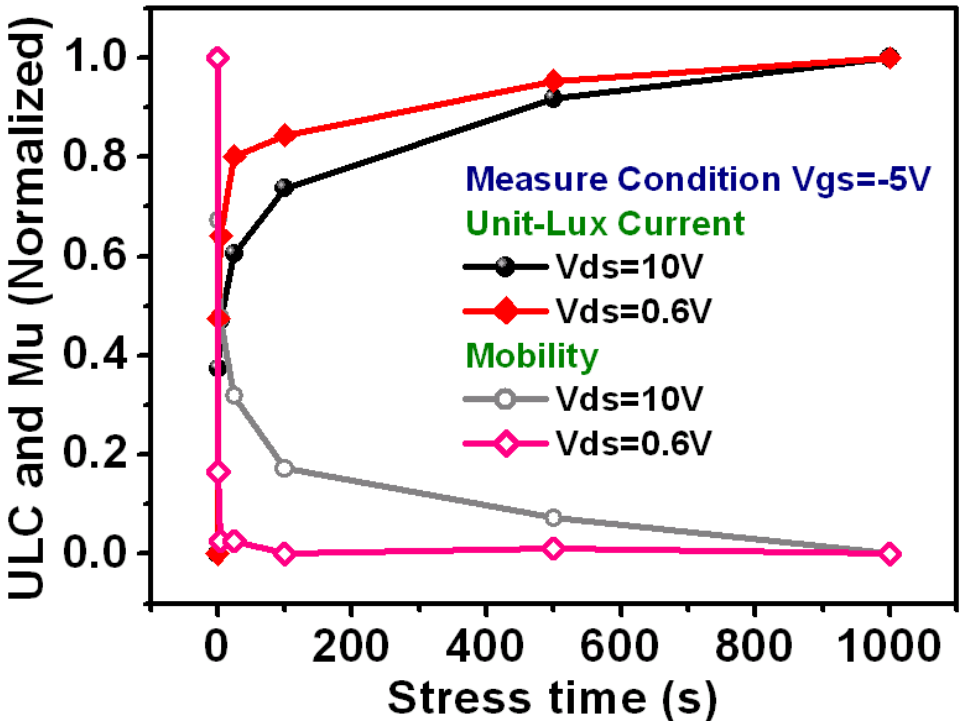


(a)

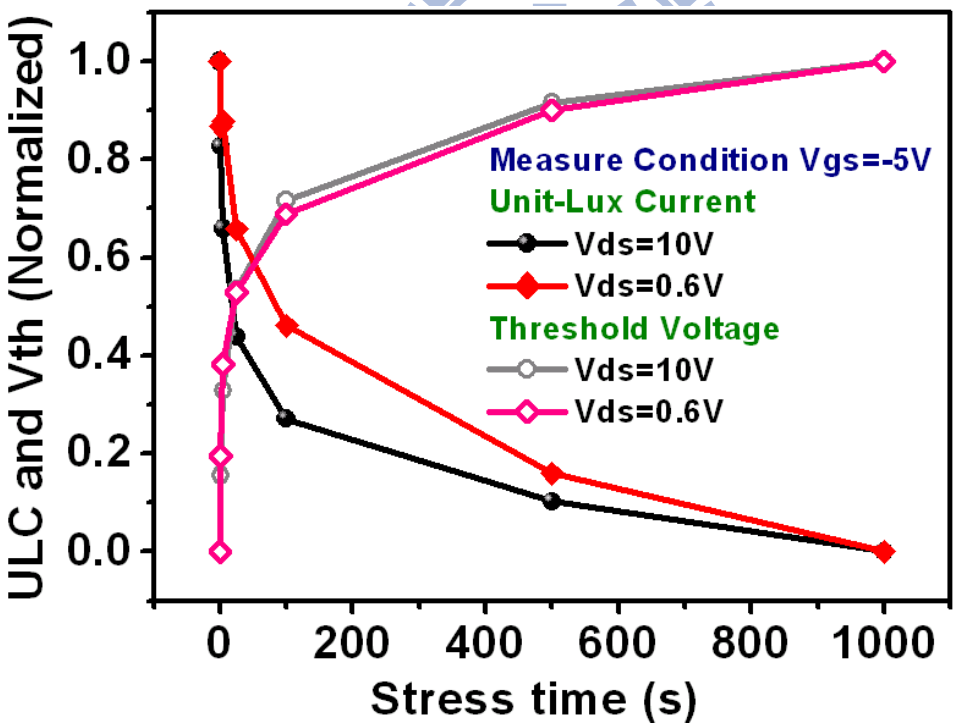


(b)

Figure 4-4 The I_{ds}-V_{gs} transfer characteristics with 1V drain voltage before and after (a) hot carrier stress and (b) self heating stress under different illumination conditions.



(a)



(b)

Figure 4-5 (a) Normalized Unit-Lux-Current and mobility at V_{ds}=0.6V and 10V with hot carrier stress times. (b) Normalized ULC and threshold voltage at V_{ds}=0.6V and 10V with self heating stress times.

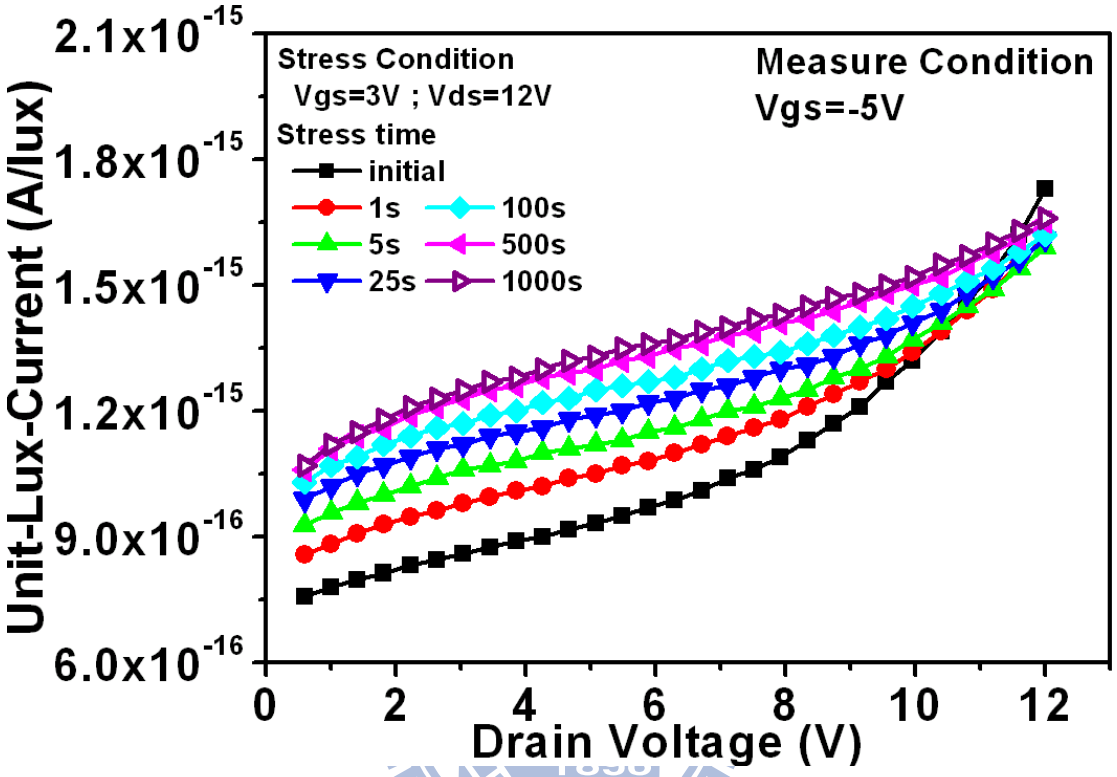
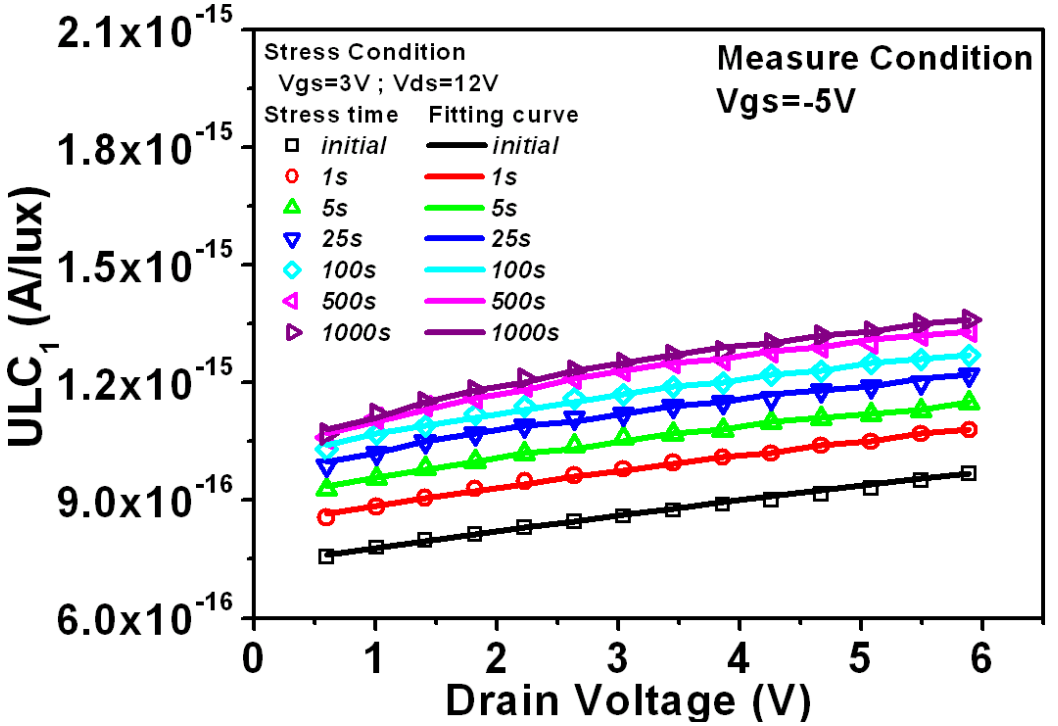
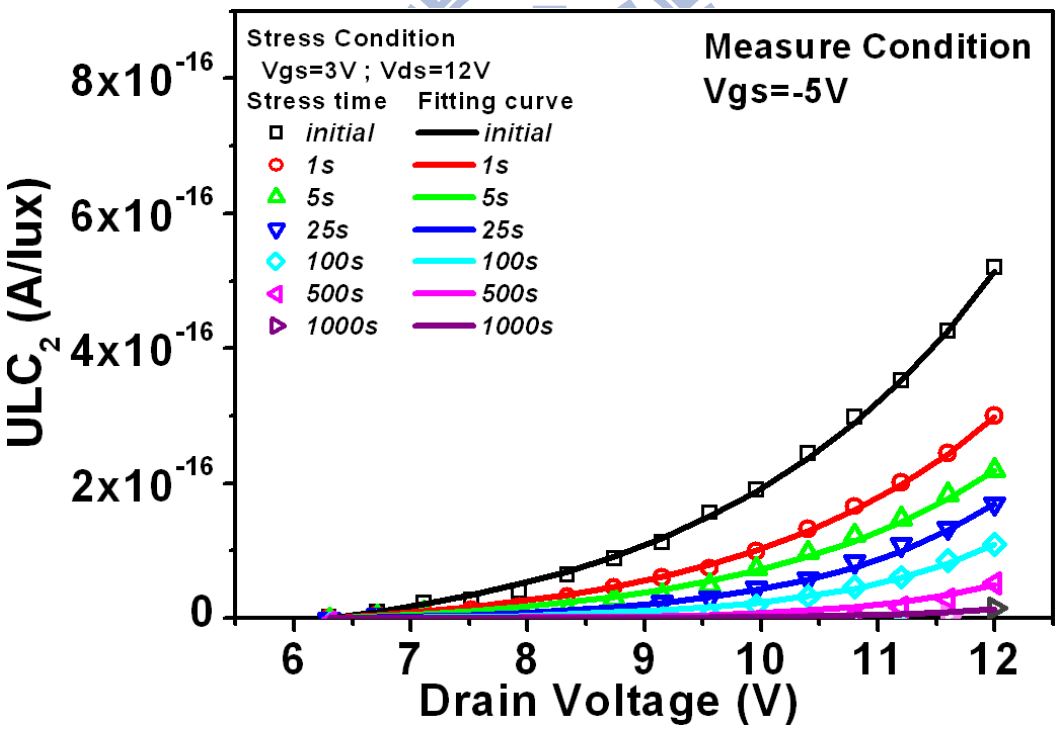


Figure 4-6 Drain bias effect on Unit-Lux-Current with different hot carrier stress times.

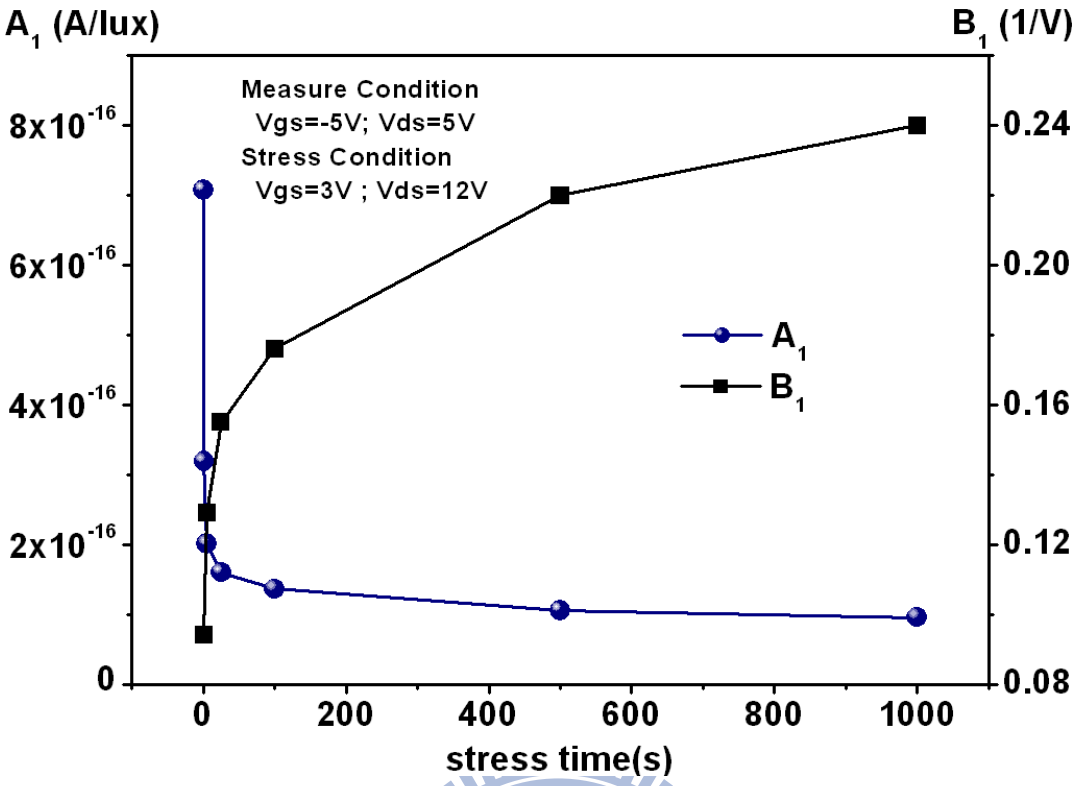


(a)

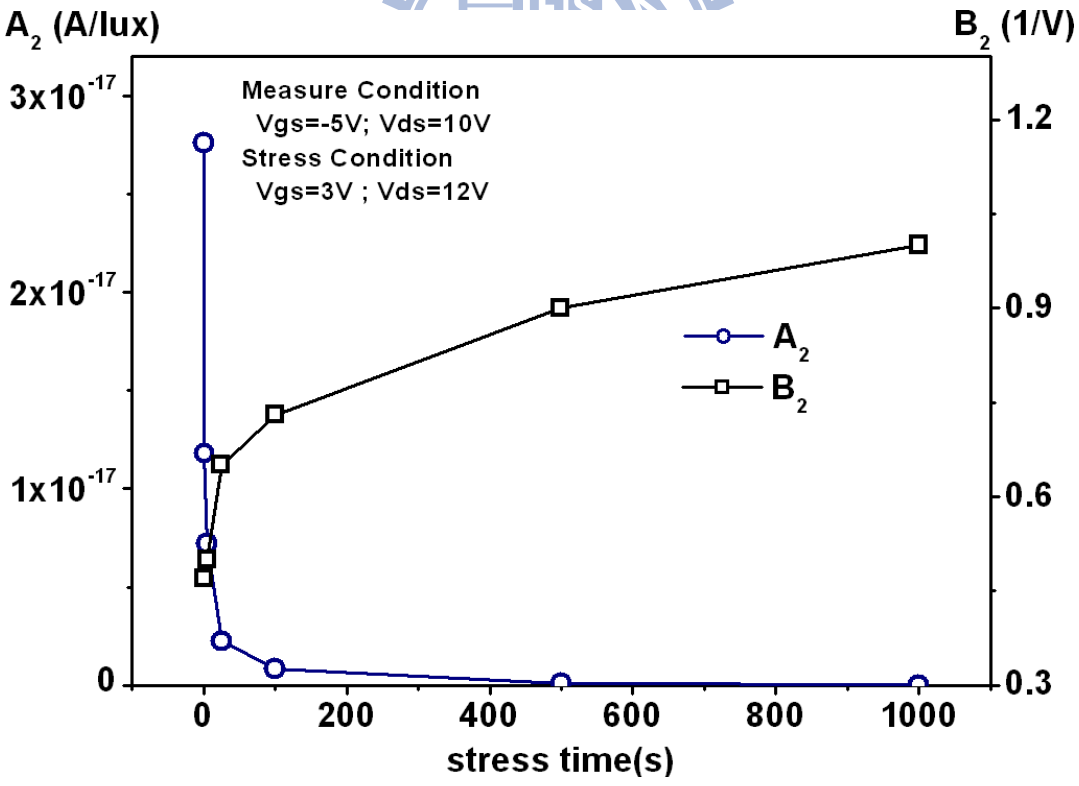


(b)

Figure 4-7 (a) The first component (ULC_1) and (b) the second component (ULC_2) of Unit-Lux-Current versus drain bias with different hot carrier stress times.



(a)



(b)

Figure 4-8 Dependence of fitting factors A_1.A_2 and B_1, B_2 on hot carrier stress.

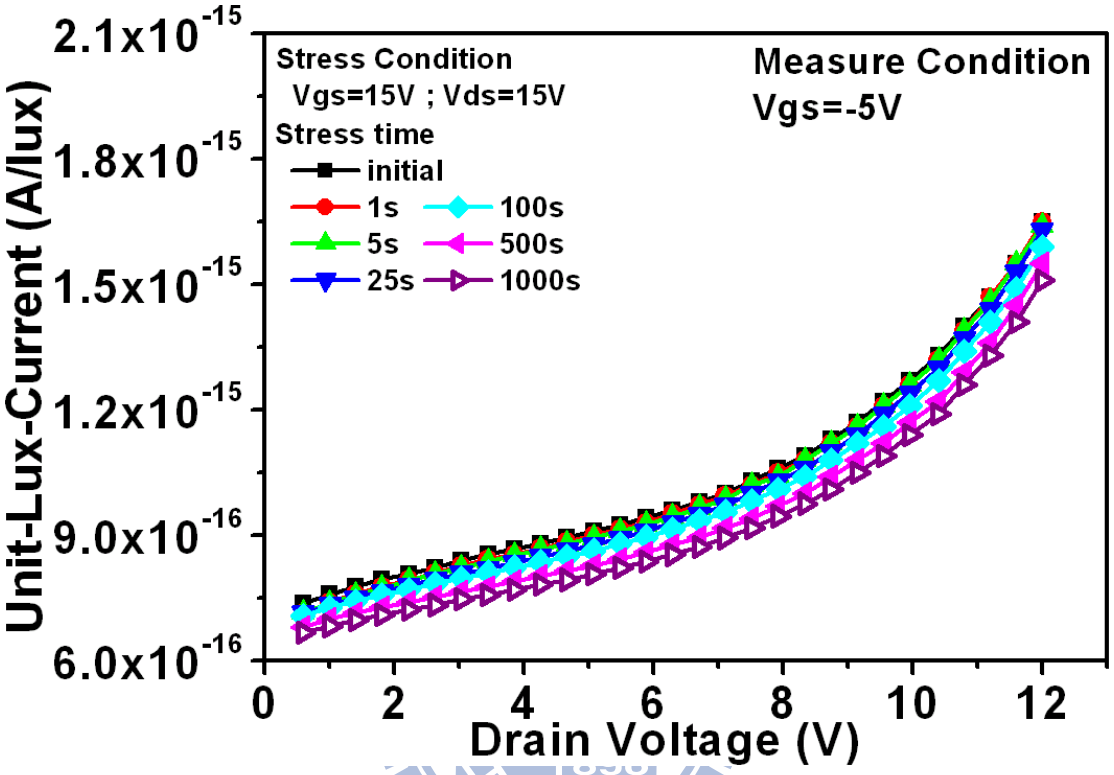
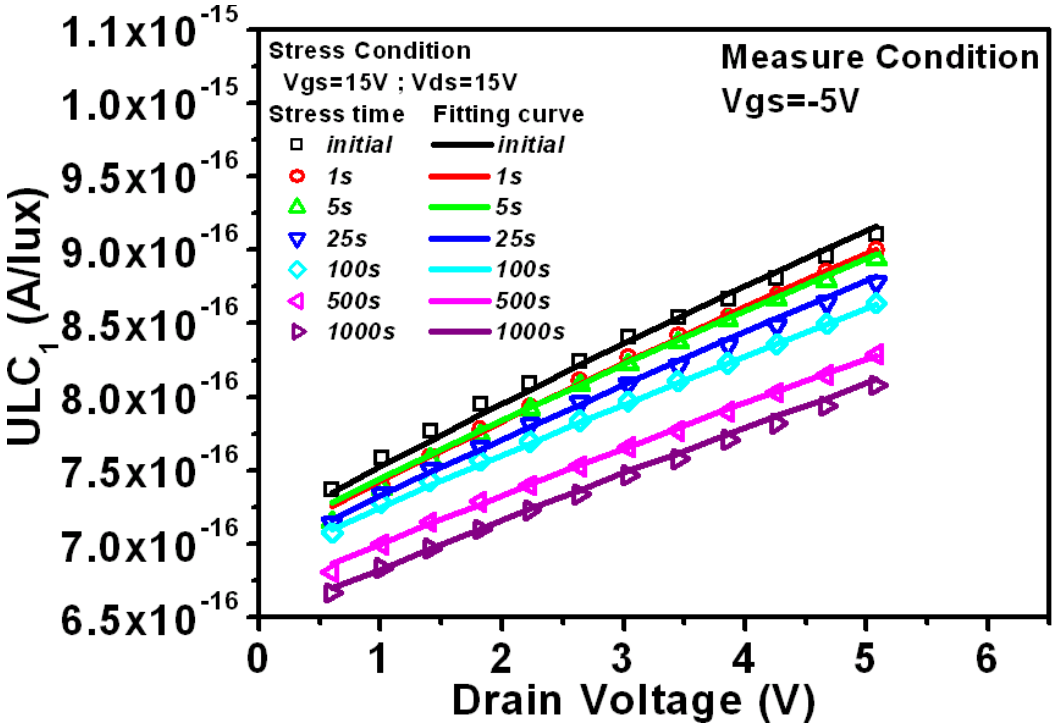
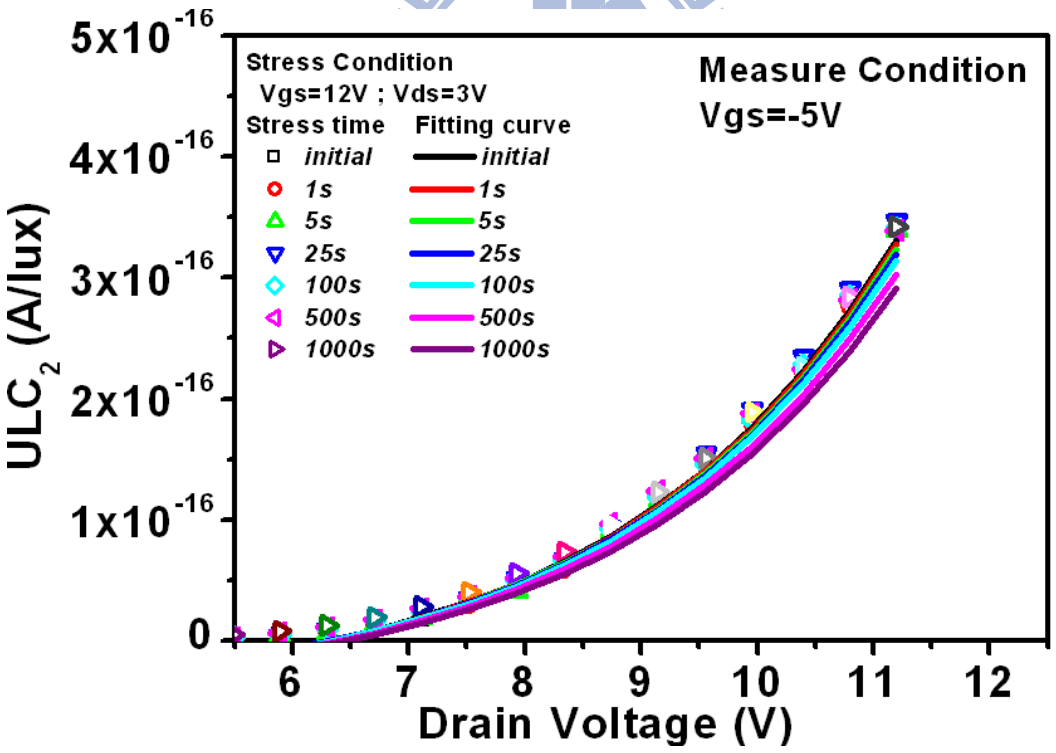


Figure 4-9 Drain bias effect on Unit-Lux-Current with different self heating stress times.

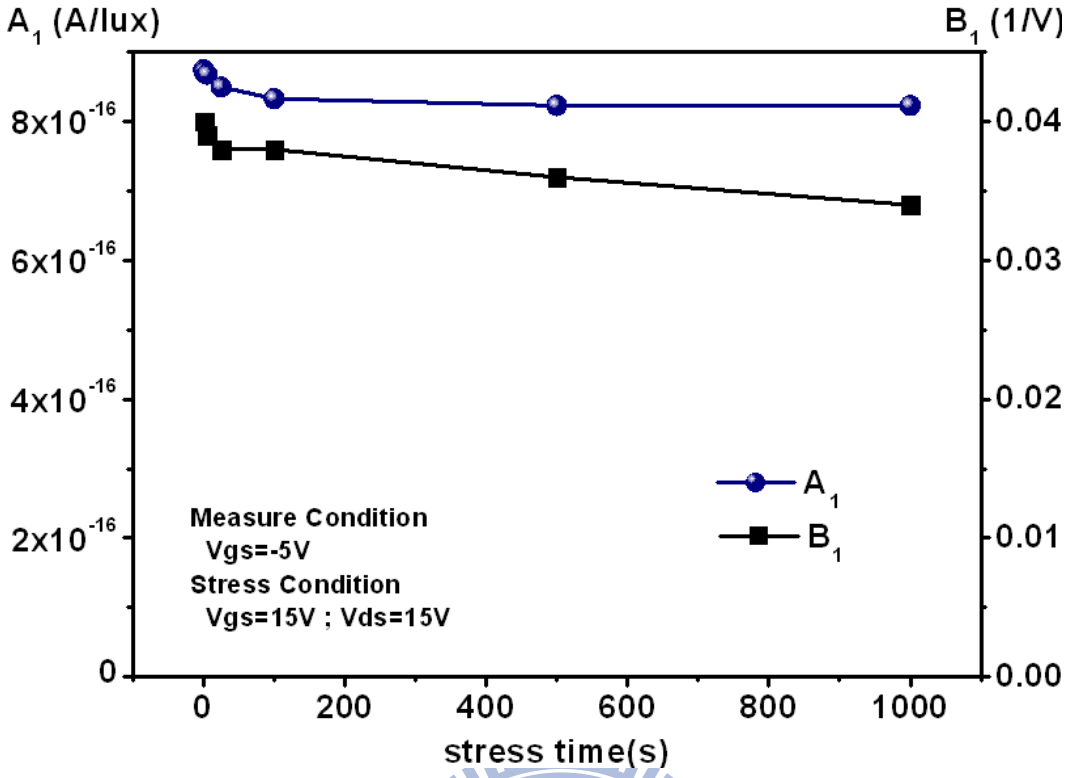


(a)

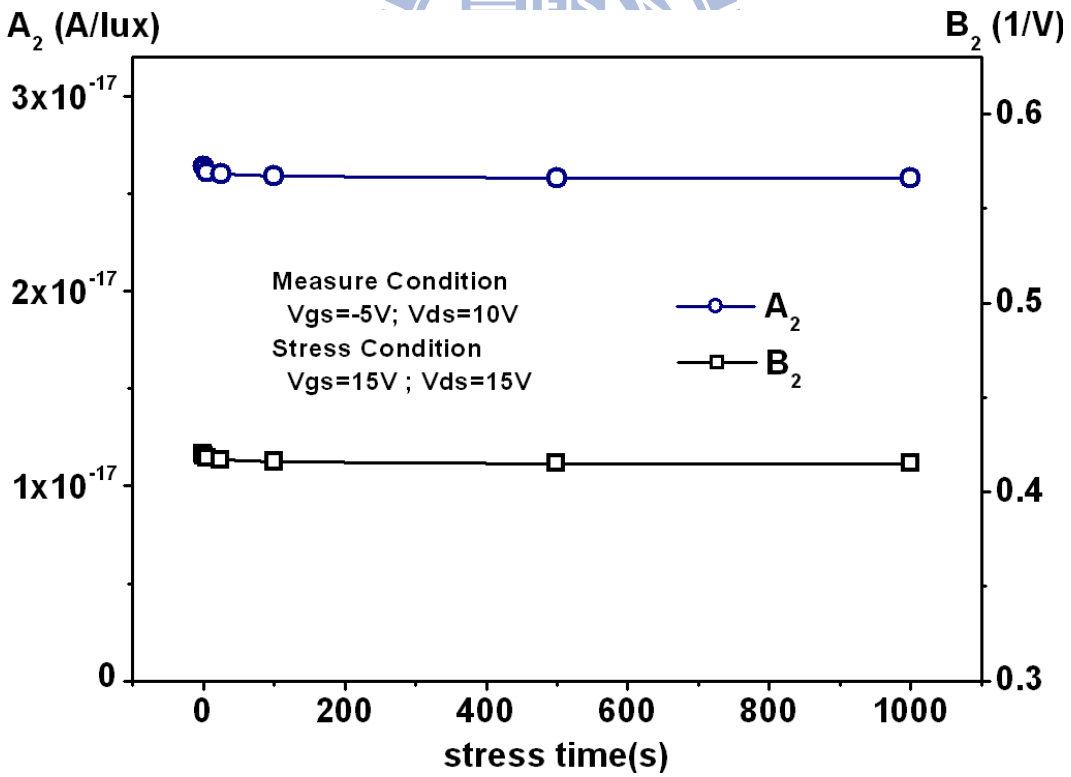


(b)

Figure 4-10 (a) The first component (ULC_1) and (b) the second component (ULC_2) of Unit-Lux-Current versus drain bias with different self heating stress times.



(a)



(b)

Figure 4-11 Dependence of fitting factors A_1.A_2 and B_1, B_2 on self heating stress.

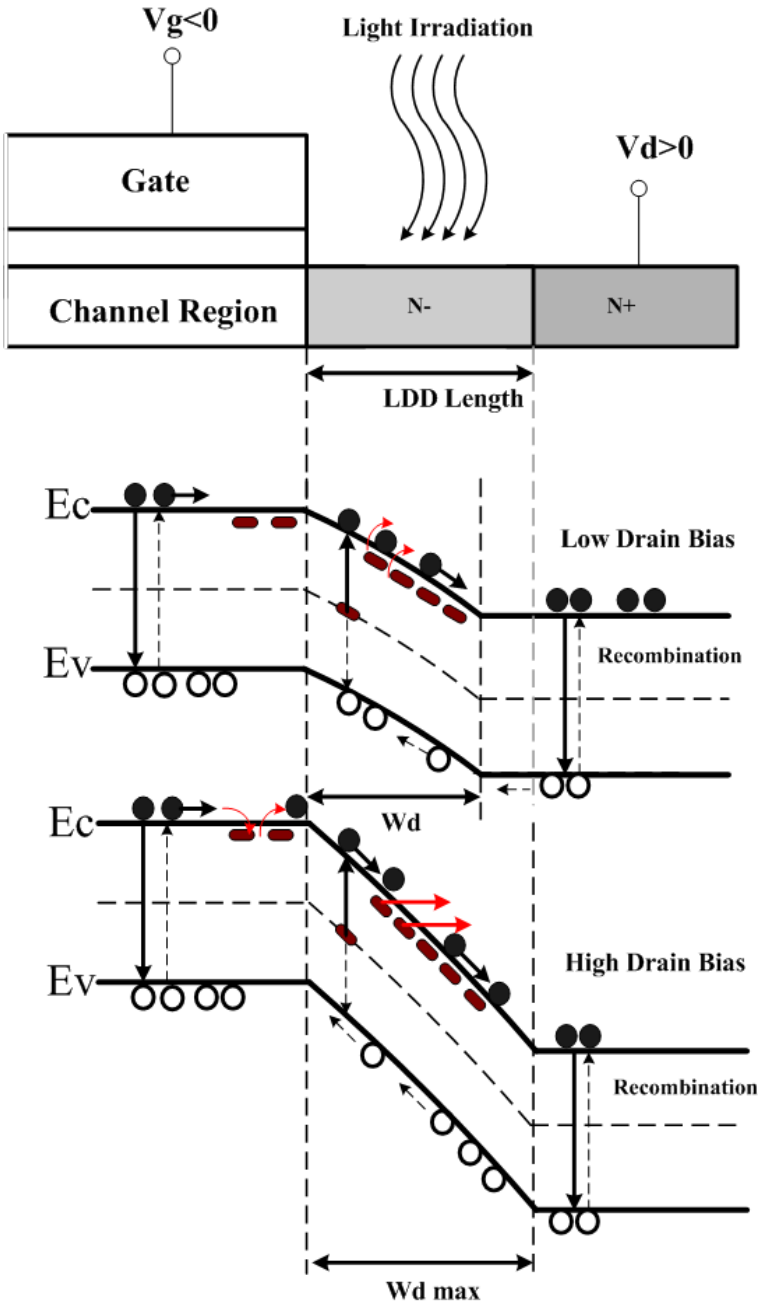


Figure 4-12 A proposed hot carrier degradation model of ULC mechanism for TFTs.

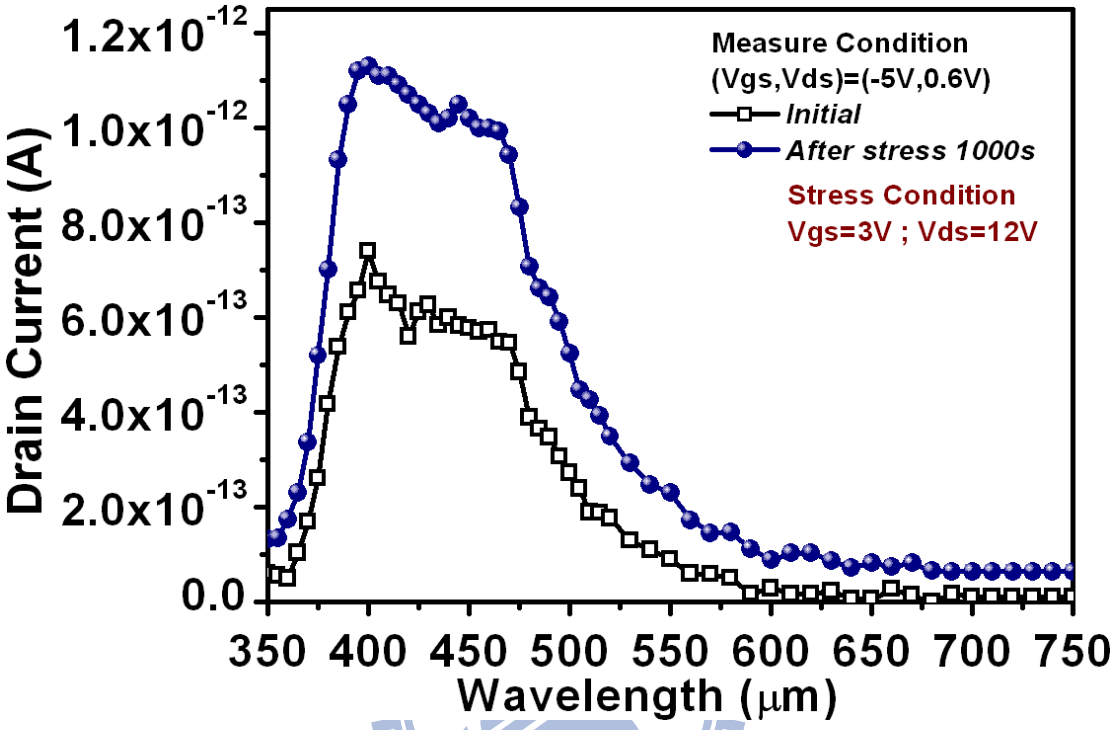


Figure 4-13 The photo leakage current spectrum of the light source in the range of 350-750 nm at lower bias after hot carrier stress.

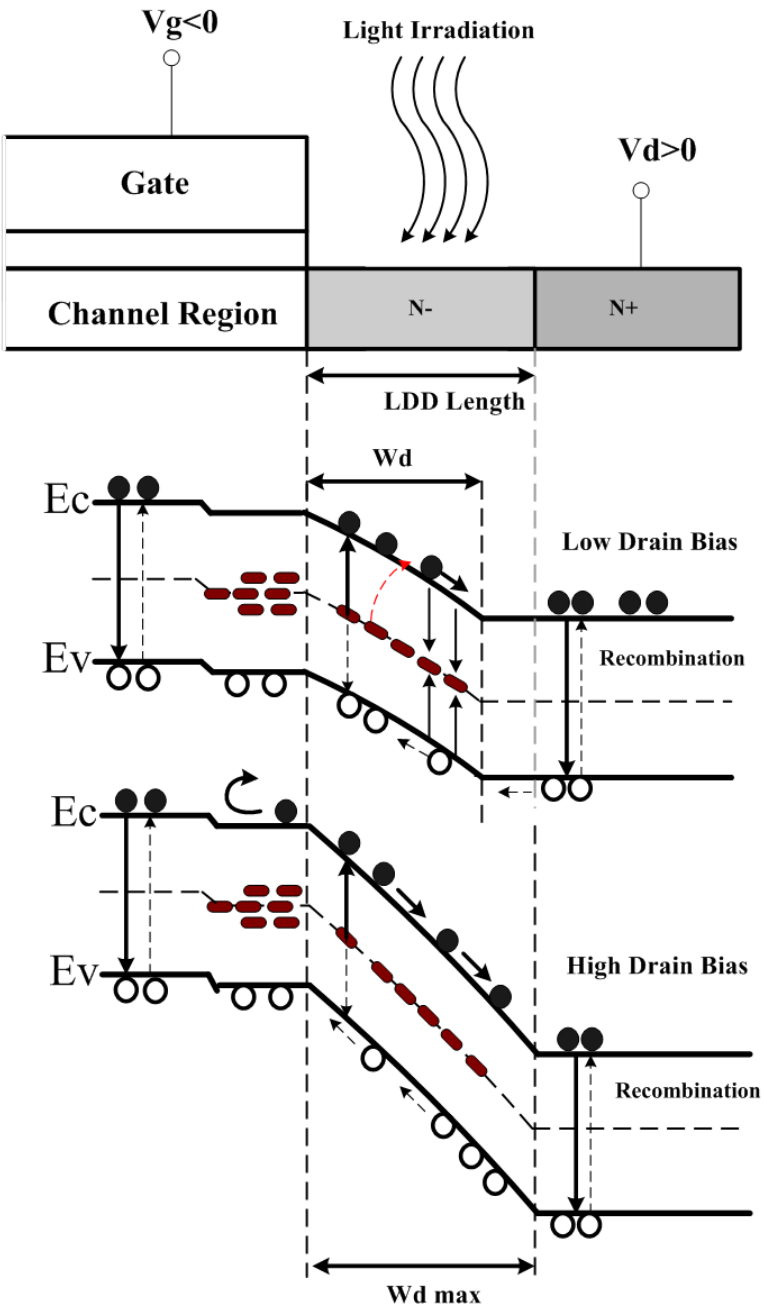


Figure 4-14 A proposed self heating degradation model of ULC mechanism for TFTs.

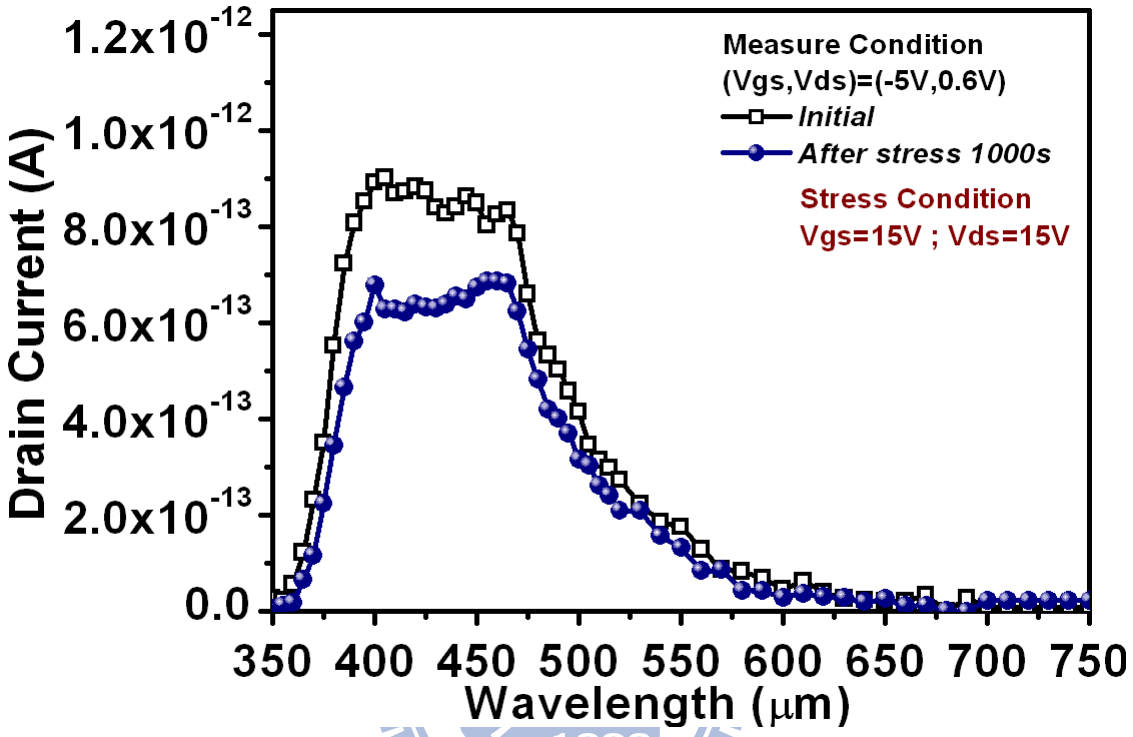


Figure 4-15 The photo leakage current spectrum of the light source in the range of 350-750nm at lower bias after self heating stress.


E S A
1896

Chapter 5

Investigation of Backlight Sensing in Poly-Si TFTs

5.1 Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) have been widely used in active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diode display (AMOLED) [5.1-5.4]. The poly-Si TFTs offer great potential for AMDs technology, due to their superior electrical characteristics over those of hydrogenated amorphous Si thin film transistors (a-Si:H TFTs). Recently, the demand of high-end mobile electronic products such as digital camera, cell phone, and mobile TV is continuing to grow up, so that the high resolution and high image quality becomes the critical issues in the development of mobile displays. Therefore, the brightness of back-light is getting higher and higher to meet the requirement for fine image quality and superior readability as people use these mobile electronic products under sunlight outdoor [5.5-5.6]. Because LTPS TFTs are top gate structures, it is suffer from undesirable photo leakage current under a high illumination environments [5.7-5.10]. However, the researches about improving the electrical characteristics in poly-Si TFTs under illumination are very few and the mechanism of photo leakage current in poly-Si TFT is still not clarified.

In our previous studies, for front light illumination experiment, we propose both unstressed devices which can be seen as “effective medium approach” and stressed devices which have additional non-uniform defects photo-induced leakage models, comparatively. In this chapter, we also use such methods to analyze photo behaviors

of LTPS TFTs when back light emitted from bottom direction.

5.2 Experimental Procedures

Nowadays, the light emitting diode (LED) is more and more used as the backlight source of liquid crystal displays (LCD) to reduce the power and module thickness. Therefore, we use LED as the back light source in our experiments. Before going on back light measurement, we would further make sure sphere of action under back illumination.

The cross section of the TFT device under back light illumination is shown in Fig. 5-1. In spite of passing through the glass substrate and probably the buffer oxide, the back light intensity is less decrease, it's due to the effect of the glass substrate and the buffer oxide on transmission is small. On the other hand, the back light is absorbed by the silicon film. According to the reference [5.11], Fig. 5-2 shows the transmission and absorption rate of light at different wavelengths after passing a silicon film with thickness of 65nm according to formula $I_v(x) = I_{vo} \exp(-\kappa x)$, where I_{vo} and $I_v(x)$ are the input intensity and the intensity at distance x, respectively, κ is the absorption coefficient, and x is the propagating distance. Based on the calculation, we know the total intensity decreases up to 10% when the light comes to the channel surface of the TFT. The photo leakage current (I_{photo}) is measured at different bias conditions to study its field effect. Table. 5-1 lists the measurement conditions of the gate and drain bias in detail. Two types of curves are measured, namely, with fixed the drain voltage (V_D) as the gate voltage (V_G) sweeping and with fixed V_G and changing V_D. In addition, the above two cases of measurement is repeated at various temperatures.

5.3 Results and Discussions

5.3.1 Physical Models

When the light is emitted from back-light, plenty of electron-hole pairs are generated in the bottom of poly-Si film. Furthermore, the energy-band structure of Si material is indirect bandgap. The excess electron-hole pairs induced by the absorption of light would not be recombined from band to band directly due to the momentum conservation principle. The numerous electron-hole pairs are accumulated in the bottom of poly-Si layer. It follows that the excess electrons flow to the drain under the positive drain bias for n-channel devices, generating the photo leakage current.

Fig. 5-3 shows model of the electron-hole pair distribution in the poly-Si of TFTs [5.10]. It assumed that Q electron-hole pairs are generated when backlight is absorbed near the glass/poly-Si interface. These electron-hole pairs either recombine at the glass/poly-Si interface or diffuse to the gate SiO_2/poly-Si interface and recombine there. We also assume the recombination speeds S_b at the glass/poly-Si interface and S_r at the poly-Si/gate SiO_2 interface. We denote the electron-hole pair concentration at the glass/poly-Si interface as N_m, and denote that at the gate SiO_2/poly-Si interface as N_s. The balance of flow at both interfaces is given by

$$Q = S_b N_m + D\frac{N_m - N_s}{t_{Si}} \quad ; \quad D\frac{N_m - N_s}{t_{Si}} = S_r N_s$$

It can obtain N_m, and N_s as

$$N_m = \frac{1+\frac{1}{S_r}\frac{D}{t_{Si}}}{1+\left(1+\frac{S_b}{S_r}\right)\frac{1}{S_b}\frac{D}{t_{Si}}}\frac{Q}{S_b}; N_s = \frac{\frac{1}{S_r}\frac{D}{t_{Si}}}{1+\left(1+\frac{S_b}{S_r}\right)\frac{1}{S_b}\frac{D}{t_{Si}}}\frac{Q}{S_b}$$

Therefore, total amount of electron-hole pairs accumulated in the channel, Q_{pair}, is given by

$$Q_{pair} = \frac{1}{2}\frac{2\frac{1}{S_r}\frac{D}{t_{Si}}}{1+\frac{1}{S_r}\frac{D}{t_{Si}}}\frac{Q}{S_b}t_{Si} = \begin{cases} \frac{Q}{2S_b}t_{Si} \rightarrow S_r >> \frac{D}{t_{Si}} \\ \frac{Q}{S_b}t_{Si} \rightarrow S_r << \frac{D}{t_{Si}} \end{cases}$$

$Q_{pair} = \frac{Q}{\gamma S_b}t_{Si}$ where γ is between 1 and 2 depending on the ratios of S_r, S_b and D/t_{Si}. Thus, the electron-hole pairs can be generated in not only drain or source junction region but also the whole channel region, so a front light case should show lower photocurrent than a back light case, from physics viewpoint.

When device is under back-light illumination, the drain current is dominated the diffused electron from source in n-type poly-Si TFTs. Therefore, it would be affected strongly by the barrier height of source. As the gate bias is applied, the barrier height of source is lower to increase the amount of electron is channel diffused from source. Base on the experimental results, a leakage model of band diagram is proposed. First, as the excess electron-hole pairs are generated under illumination with positive drain voltage, the light-induced electrons flow to drain directly, forming the photo leakage current. Therefore, the residual excess holes are accumulated in the poly-Si film to form the floating body with a positive channel potential, ΔV. Hence, the source barrier is lowered by ΔV due to the floating positive potential distributed in the channel. While the applied gate bias is swept from negative to positive directions and smaller than the threshold voltage, TFT would be operated at sub threshold region. So the source barrier would be lower again by the positive gate bias, However, the more lowering source barrier induce that the excess holes accumulated in channel are more easily diffuse to the source to reduce the positive channel potential. So that the fewer channel potential leads to a raise of source barrier. It means that the source barrier is not only controlled by applied gate bias but also affected by the floating body with positive potential, ΔV when poly-Si TFTs are under illumination.

The current components of our model are shown schematically in Fig. 5-4. The

generated electron current I_{ephoto} flows to drain terminal, the generated hole current I_{hphoto} flows to the source terminal, and the parasitic bipolar electron current I_{se} flows to the channel.

5.3.2 Electrical characteristics of Unit-Lux Current

The relationships between leakage current and illumination intensity under different bias conditions are shown in Fig. 5-5. It is clearly seen that the linearity retains under different bias conditions. Fig. 5-6 (a) and (b) demonstrate the drain bias effect and gate bias effect on ULC, respectively. It is noticed that drain bias affects the photo leakage current severely, but the change of ULC is not obvious with respect to the gate bias. Furthermore, the back light ULC equations also can be expressed like as front light ULC equations (3-2) (3-3) (3-4) case, similarly. As shown in Fig. 5-7, the empirical formula fits the experimental data very well. The values of fitting factors α, β, γ, η_1 and η_2 are listed in Table. 5-2. However, compare with Table 3-1, we can see α, β, and γ is higher than front light case and η_2 is relatively much lower than front light case. The α, β, and γ parameters are higher which is due to the electron-hole pairs can be generated in not only drain or source junction region but also the whole channel region, so a front light case should show lower photocurrent than a back light case. Meanwhile, the residual excess holes are accumulated in the poly-Si film to form the floating body with a positive channel potential, ΔV. The source barrier is not only controlled by applied gate bias but also affected by the floating body with positive potential, ΔV when poly-Si TFTs are under illumination. It results in the parameters about the exponential dependence on negative gate bias of ULC_2 for back light illumination case is lower than front light illumination case.

Drain bias dependences of ULC at different temperatures are also shown in Fig. 5-8.

ULC in the range of low drain bias is significantly affected by temperature. Since the temperature only affects the ULC_1, it is consistent with the mechanism of thermionic emission. Then, we further analyze on the temperature dependence of ULC_1. The temperature effect on I_{Dark} also can identify constant activation energy like as front light case. In the previous equations, A, B, Ea_A, and Ea_B are fitting factors, and their values are listed in Table. 5-3.

5.3.3 Photo Induced Current Analysis of Extra Defect Distribution under Electrical Stress in LTPS TFTs

In this chapter, to analyze in detail the photosensitivity of the poly-Si TFTs, we will offset I_{dark} (measured under dark state) from I_{total} (total leakage current under illumination) and only consider I_{illum} which is defined as $I_{illum}=I_{total}-I_{dark}$. Fig.5-9 (a) and (b) shows Iillum which measured at V_{gs}=-5V, Vds=3V dependence on the illumination intensity before and after 1000 seconds of hot carrier or self heating stress with forward and reverse measurements. All Iillum are proportional to the amount of radiant illumination which can be expressed by the slope.

In aspect of forward measurement, as shown in Fig.5-9 (a), we notice the slope is changed oppositely by different stress conditions. Whether light source is frontlight or backlight irradiation, it increases in the case of hot carrier and decreases for self heating. It demonstrates that photosensitivity can be higher if there are more tail states, while it exhibits a negative dependence on the number of deep states. On the other hand, for reverse measurement case, as shown in Fig.5-9 (b), the photosensitivity is almost no difference with hot carrier stress time which reflects that the non-degraded source region. However, it first noticed that the unanticipated anomalous illumination behaviors, photo current increased abruptly under backlight irradiation after

self-heating degradation. However, according to previous study [5.13], it can't be explained photo induced currents are raised due to only interface states near the source region.

First, in our hot carrier stress experiment, we stressed our devices at V_{gs}=3V, and V_{ds}=16V, and measure them at different stress times of 25, 100, 500, 1000 sec. With fixed the gate voltage as the drain voltage sweeping in the forward measurement, as shown in Fig. 5-10, we can see that the ULC increases and distorts slightly at lower drain bias with stress times. Compared to the unstressed device, the ULC_2 of the devices operating at higher enough drain bias becomes less obvious and the total ULC is smaller. On the other hand, for the reverse measurement, we can see that the ULC before and after stress remain the same, as shown in Fig. 5-11, which confirms the defects are only created near the drain side. The behaviors of ULC under back light illumination are similar to front light case.

On the other hand, in our self heating stress experiment, compare with front light illumination case, it is first notice the unanticipated photo current. Fig.5-12 (a) and (b) show the I_{ds}-V_{gs} transfer characteristics of TFTs with forward and reverse measurements in saturation region 5V drain voltage under different back illumination conditions for self heating stress. The defects information of devices near the drain and source sides can be revealed with forward and reverse configurations measurements. It can be seen that the off current of the devices can be altered by both irradiation and stress. For analyzing ULC behaviors after self heating stress, we stressed our device at V_{gs} = 15V, and V_{ds} = 15V, and measured at different stress times of 1, 5, 50, 200, 600, and 1000 sec. With fixed gate voltage as the drain voltage sweeping in the forward measurement, the ULC is shown in Fig. 5-13. Compared to the unstressed device, we can see that the ULC decreases at higher drain bias with stress time, while ULC_1 of the devices does not change significantly. On the other

hand, for the reverse measurement, as shown in Fig. 5-14, we indeed can see that the ULC increases with stress time and ULC_2 changes significantly at high drain bias.

To verify the hypothesis about the damaged regions after self heating degradation in detail, capacitance-voltage measurements were employed. Fig.5-15 (a) (b) shows the normalized gate-to-drain capacitance C_{gd} and gate-to-source capacitance C_{gs} curves before and after stress with different frequencies. Compared with the curves before stress, the stressed C_{gs} and C_{gd} curves exhibit two main changes: the positive shift for the gate voltage near the flat band voltage V_{FB} and the increase for the gate voltage just below V_{FB}. The curves of C_{gd} after self-heating stress, the stretch and shift in the positive direction for the gate voltage near flat band voltage can be explained by the increase of the deep states with higher temperature during stress. Differ from the curves of C_{gd} with higher temperature during stress, C_{gs} is attributed to another states induced by the higher local electric field. In addition, the increases of the C_{gs} and C_{gd} curves for the gate voltage smaller than V_{FB} come from the interface states which are frequency dependence, since the fixed charges would not respond to different frequencies. Moreover, the more apparent increase of C_{gs} below V_{FB} than the one of C_{gd}. It suggests of a spatial creation of interfacial states according to the electric field distribution.

Compare with above discussion, the information of photo induced current increase can be revealed that the degradation from self-heating may not only increase interface states and trap charges between poly-Si/gate oxide film but also raise the tail states in the poly-Si film. Owing to vertical electric field dominantly near source region, major carriers greatly accelerated and impacted Si/SiO_2 surface, resulting in strain bond tail states. Such tail states may exist through the channel region, which can't discover with front light irradiation due to gate metal shielding by itself and can be detect with back light irradiation.

The degradation model in TFT structure is proposed as shown in Fig.5-16 to explain roles of defects in hot carrier and self heating stress. Hot carrier effect, the photosensitivity is higher under both front and back illumination hints such additional tail states exist in LDD region near the drain. Self heating effect is found both gradational tail and interface sates which impact ionization phenomenon cause by higher electric field along poly-Si channel from source to drain region and the gradational deep states in the poly-Si film near drain can be created.

5.4 Conclusion

In this work, we present detail studies on the factors that affect the photo leakage current of the LTPS TFTs under backlight condition. Meanwhile, we correlate the photosensitivity with different types of defects by electrical stress on the LTPS TFTs. Meanwhile, the degradation of poly-Si TFTs under self-heating stress is examined via employing both C-V measurements and new partial irradiated analysis in a mutual way. The defect information of several analyses is listed in Table. 5-4. I-V analysis method, it only can reveal overall behaviors of device and what kinds of dominant defects are. C-V analysis method, it can provide roughly source and drain region information for individual devices. Photo analysis method, considering the relation between photosensitivity and additional non-uniform defect is the originality of this manuscript. Defect center behaviors which influence the photo leakage current are extremely related to energy level of trap defects. In this work, new partial irradiated strategy, compare to the previous C-V or I-V analysis methods, the merits of the proposed optical method in this manuscript are properly know what complex model of TFTs after self heating, especially, both tail and deep states are found in such stress degradation. Only this method can make sure the existence of tail state after self

heating degradation and explain photo induced currents are raised near the source region. Furthermore, a more comprehensive and accurate model considering the relation between photosensitivity and additional non-uniform defect is proposed after device degradation. This understanding of the degradation mechanisms for LTPS TFTs will be helpful in realizing system and developing photosensors on panel design.

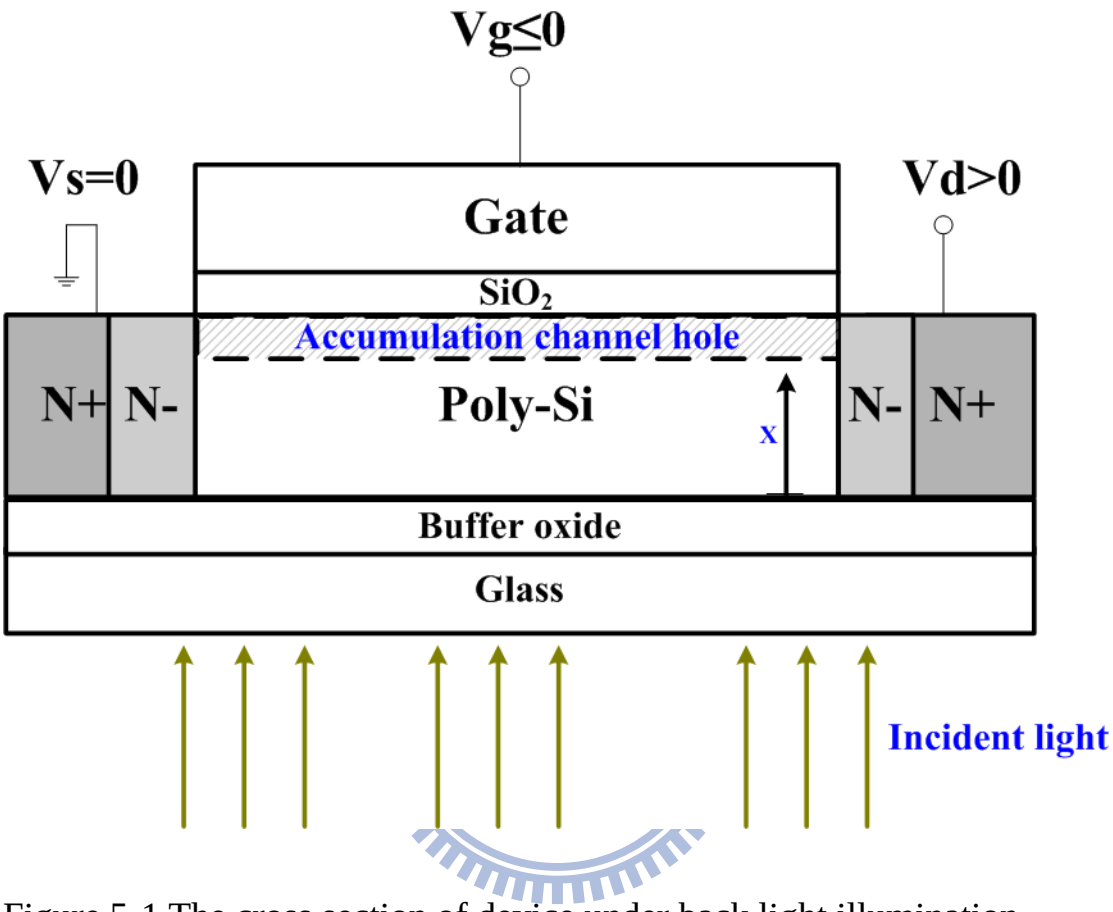


Figure 5-1 The cross section of device under back light illumination.

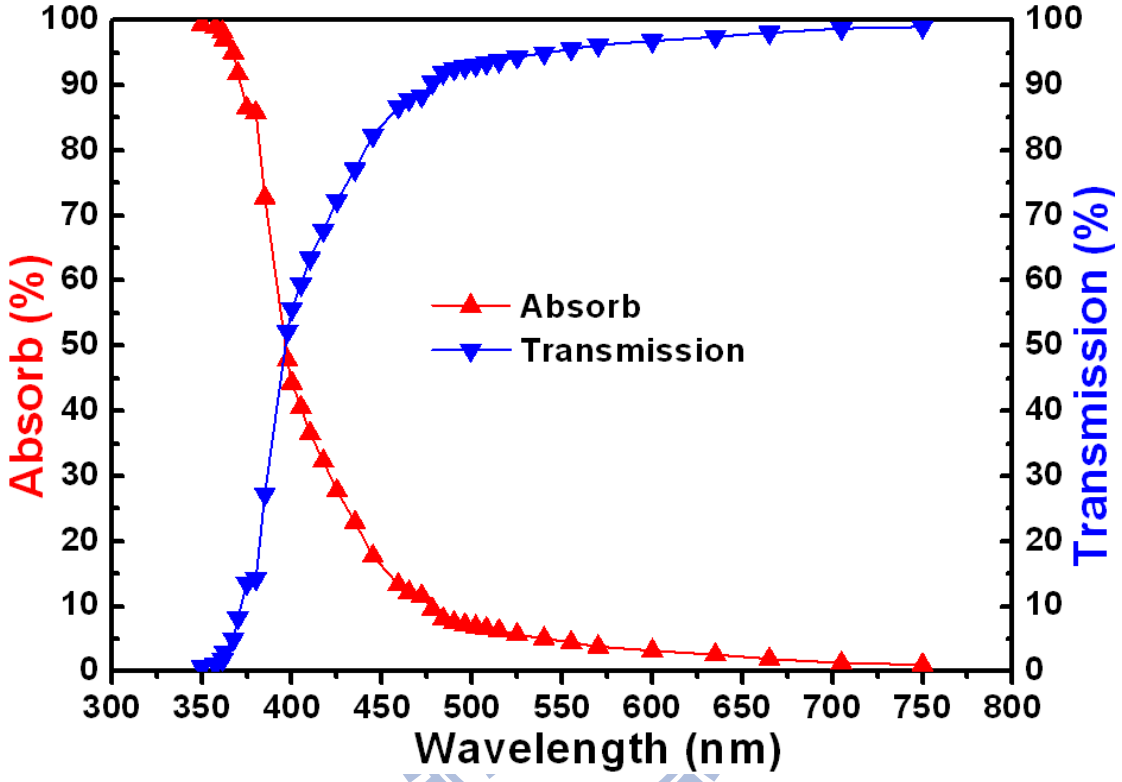


Figure 5-2 The transmission rate and absorption rate of LED light source.

EXPERIMENT	Gate Bias	Drain Bias	Illumination Intensity(lux)
VG step VD sweep	-5V	0.6V ~ 15V	0 3090 10800 19200 29900
	-7.5V		
	-10V		
VD step VG sweep	-0.8V~ -10V	0.6V	
		5.3V	
		10V	

Table 5-1 The drain bias and gate bias effects on photo leakage for LTPS TFTs.

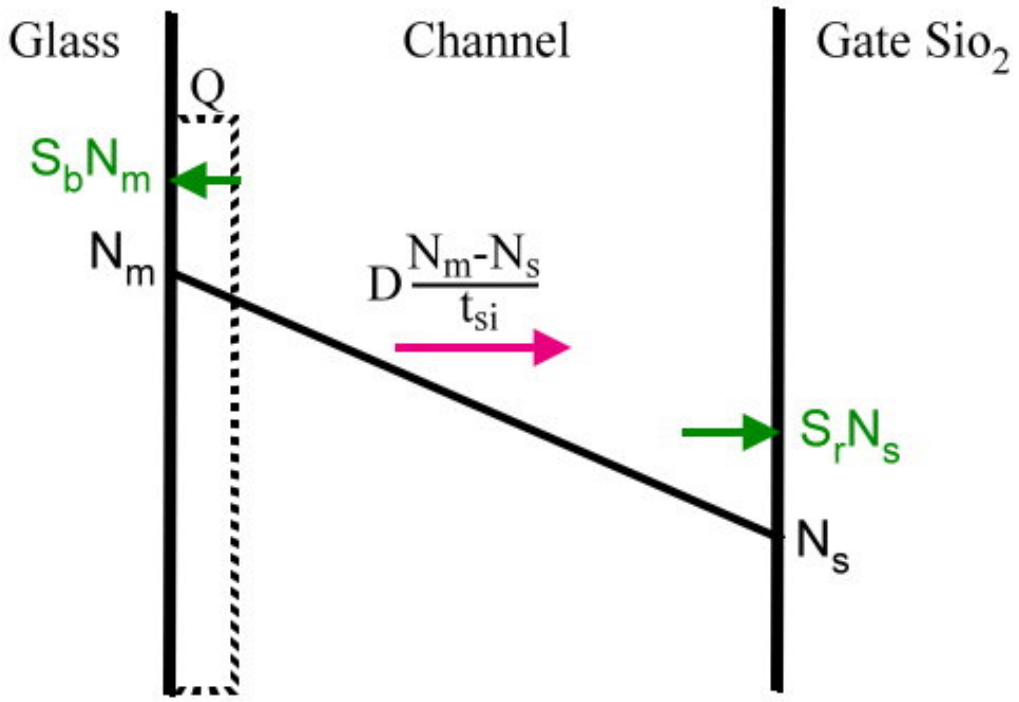


Figure 5-3 Distribution of electron-hole pairs in the poly-Si of TFTs.

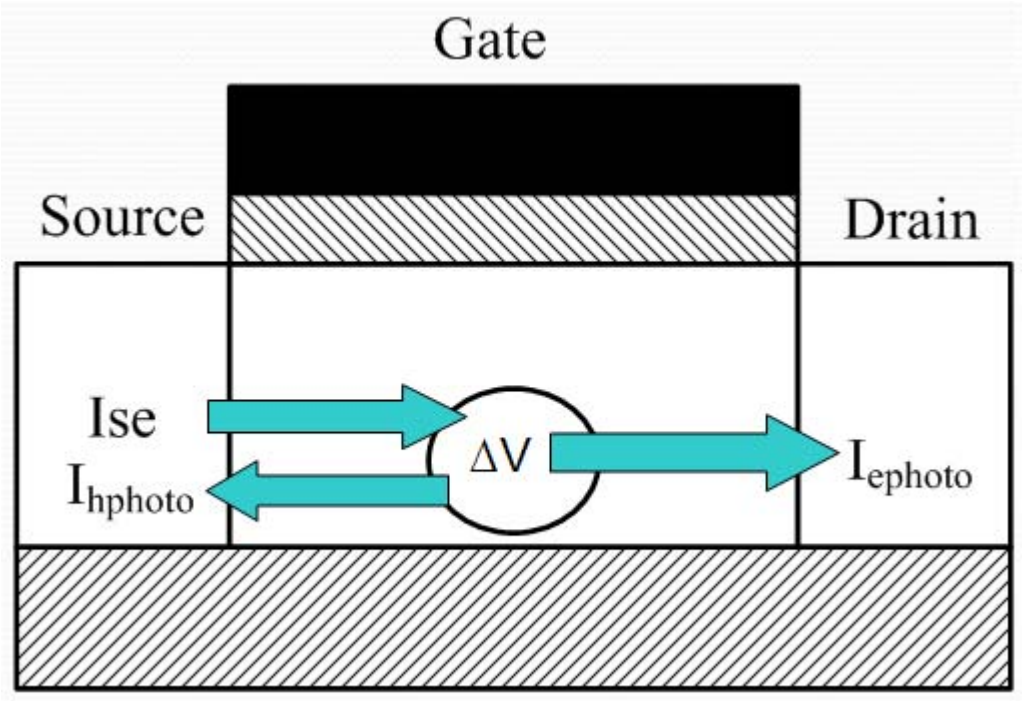


Figure 5-4 The Explanation of current flow of poly-Si under back light illumination.

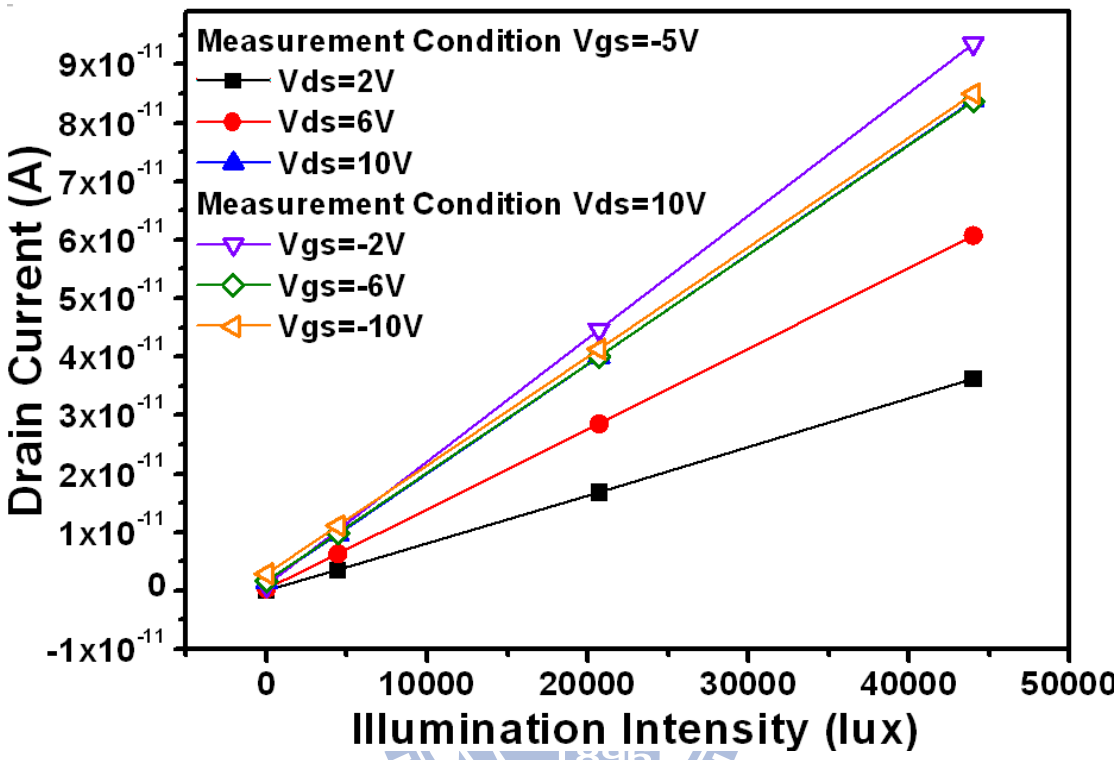
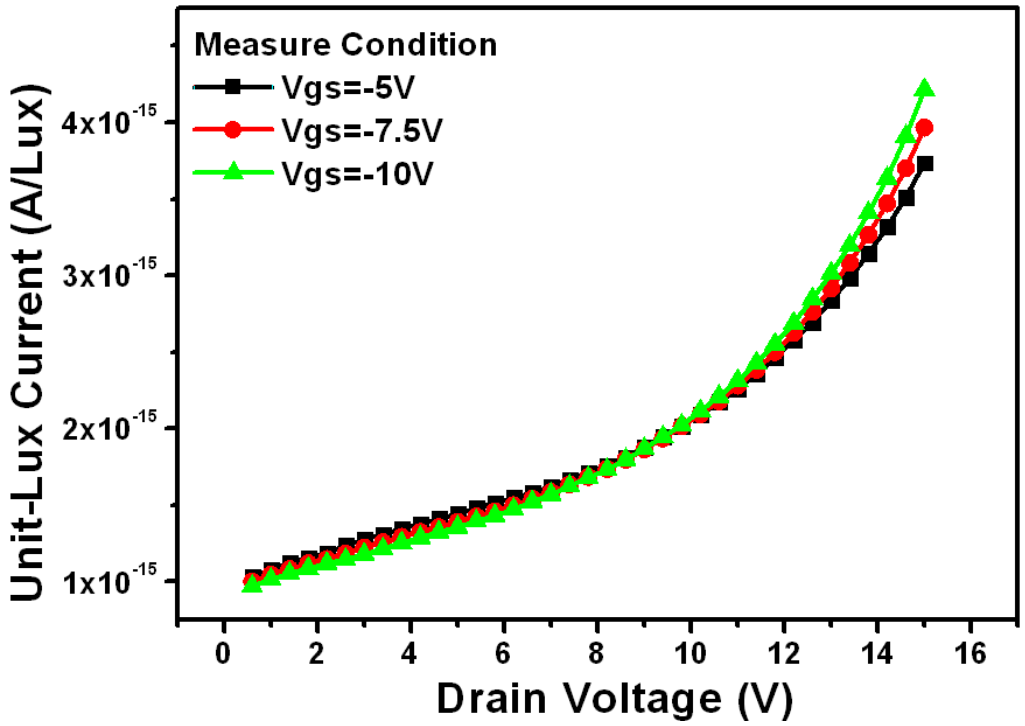
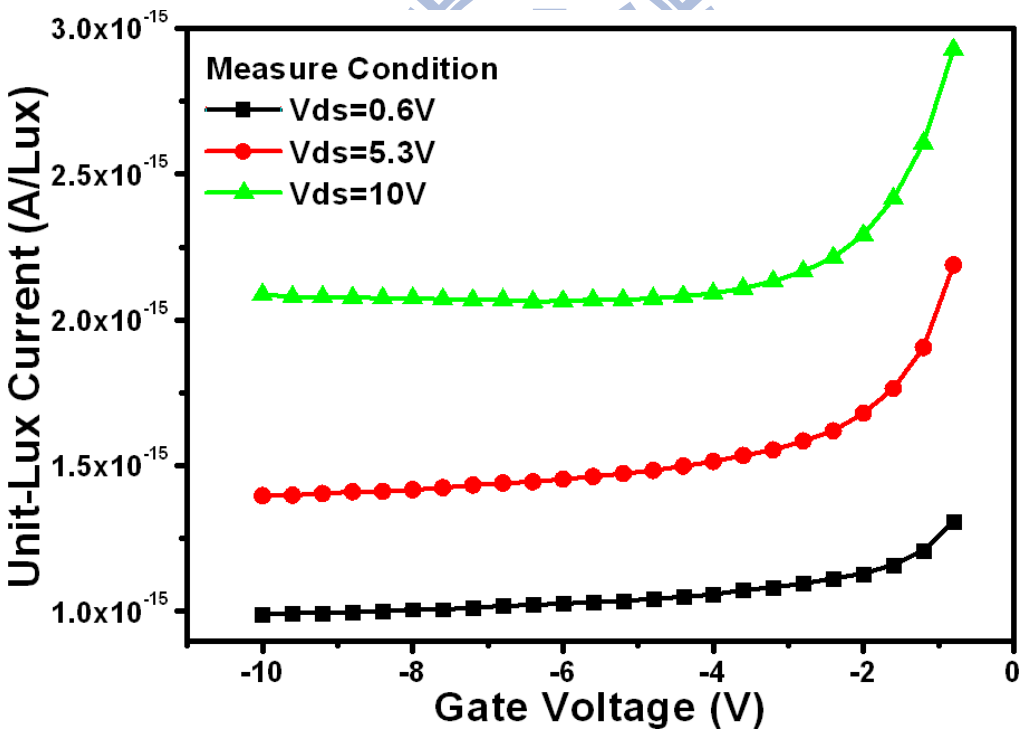


Figure 5-5 Relationship of leakage current and illumination intensity under different bias conditions.



(a)



(b)

Figure 5-6 (a) Drain bias effect on Unit-Lux Current at different gate biases. (b) Gate bias effect on Unit-Lux Current at different drain biases.

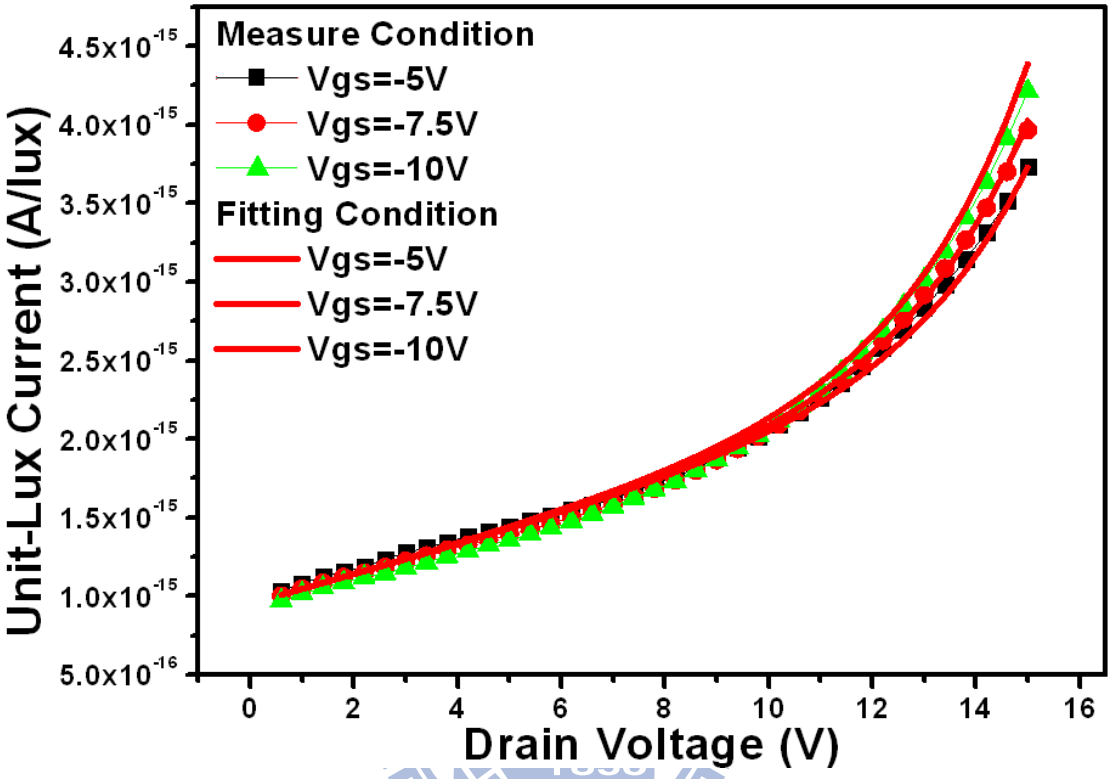


Figure 5-7 Experiment data (symbols) and empirical formula (solid lines).

Fitting Factors	Value	Unit
α	9.19×10^{-17}	A/(V · Lux)
β	9.49×10^{-16}	A/Lux
γ	2.04×10^{-18}	A/Lux
η_1	0.41	1/V
η_2	0.08	1/V

Table 5-2 The values of fitting factors under back light illumination.

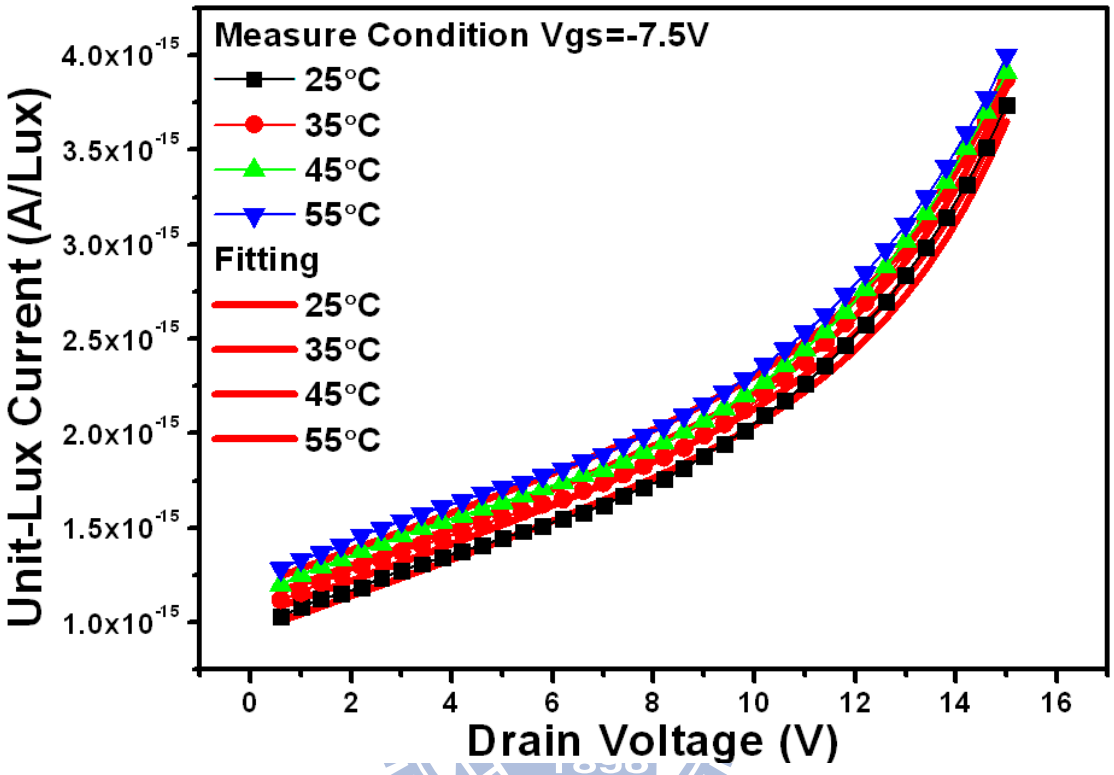
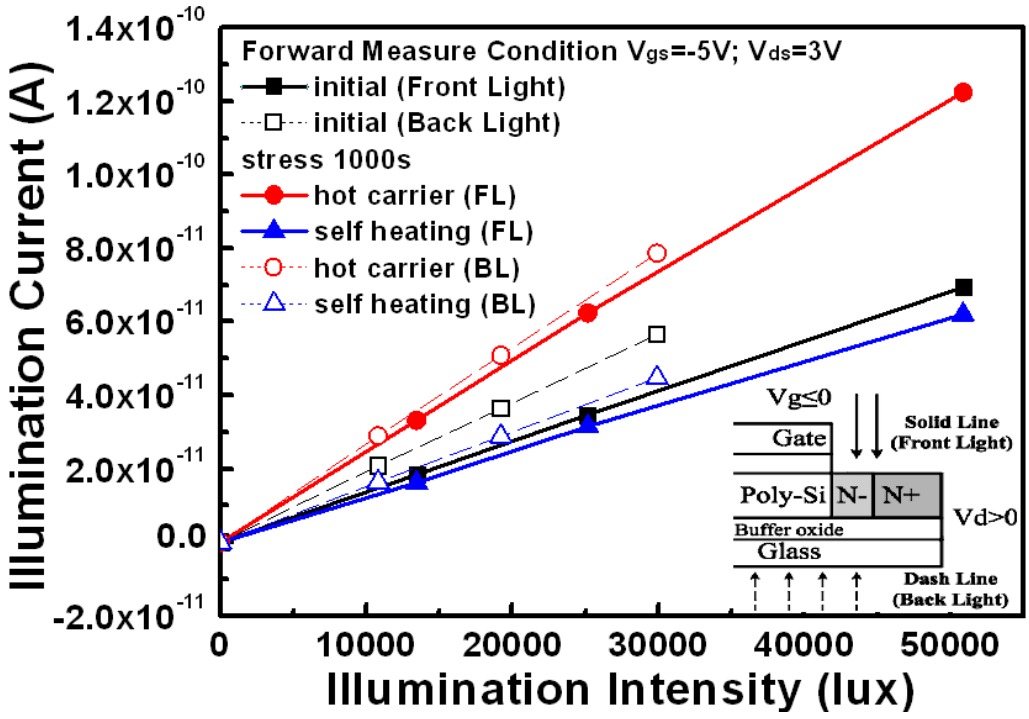


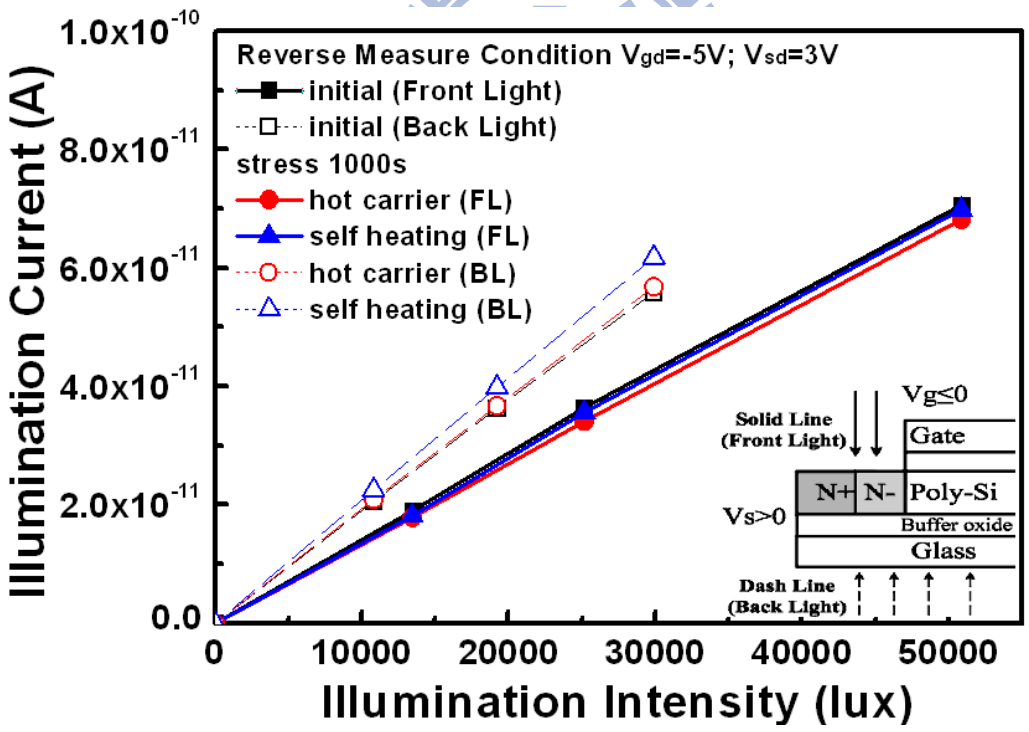
Figure 5-8 Drain bias dependence of Unit-Lux Current at different temperature.

Fitting Factors	Value	Unit
A	1.223×10^{-16}	A/(V · Lux)
B	1.086×10^{-14}	A/Lux
Ea_A	0.007	eV
Ea_B	0.063	eV

Table 5-3 The values of temperature fitting factors under back light illumination.



(a)



(b)

Figure 5-9 I_{illum} measured at V_{gs}=-5V, V_{ds}=3V dependence on the illumination intensity before and after 1000 seconds of hot carrier or self heating stress with (a) forward and (b) reverse measurements.

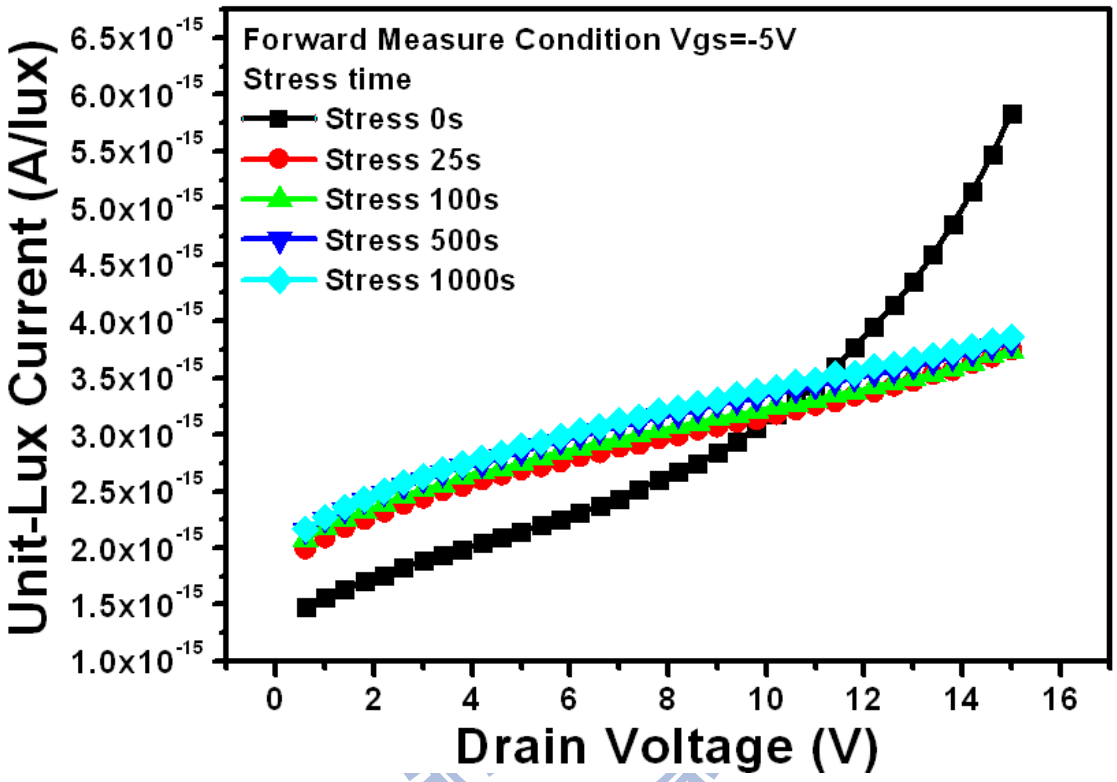


Figure 5-10 Drain bias dependence of ULC at different hot carrier stress times measured in the forward mode.

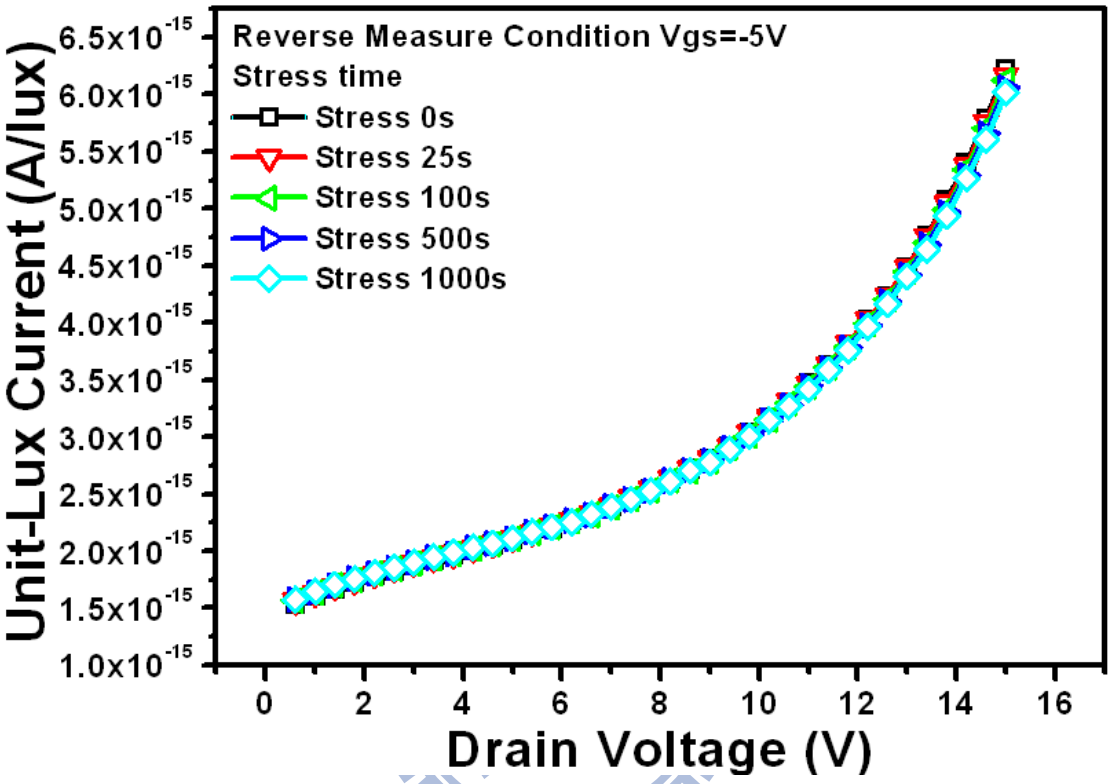
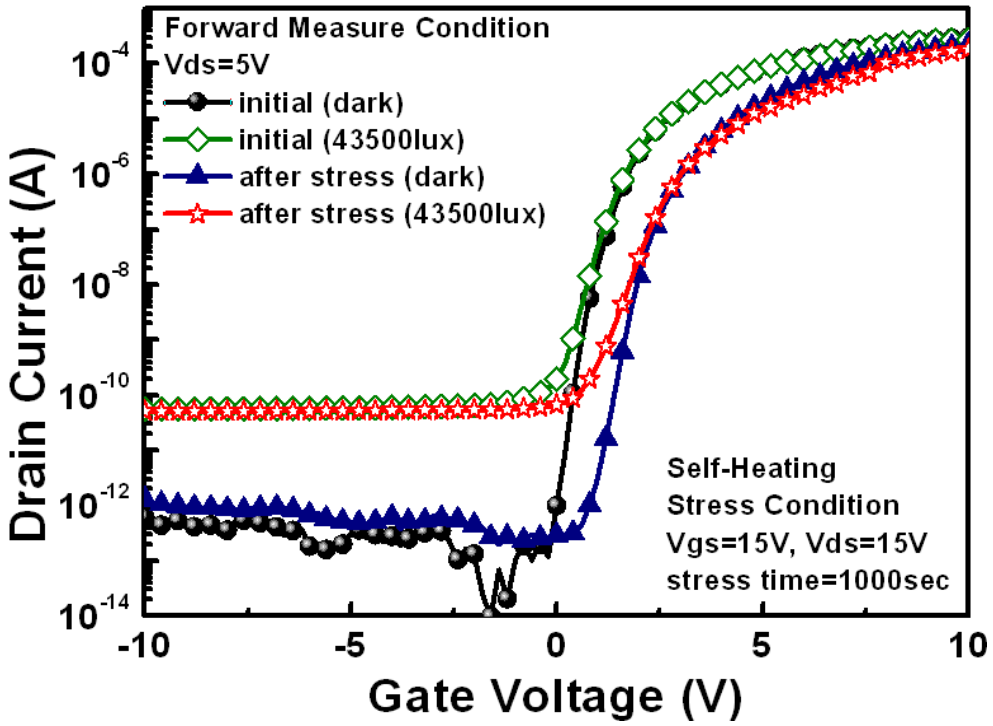
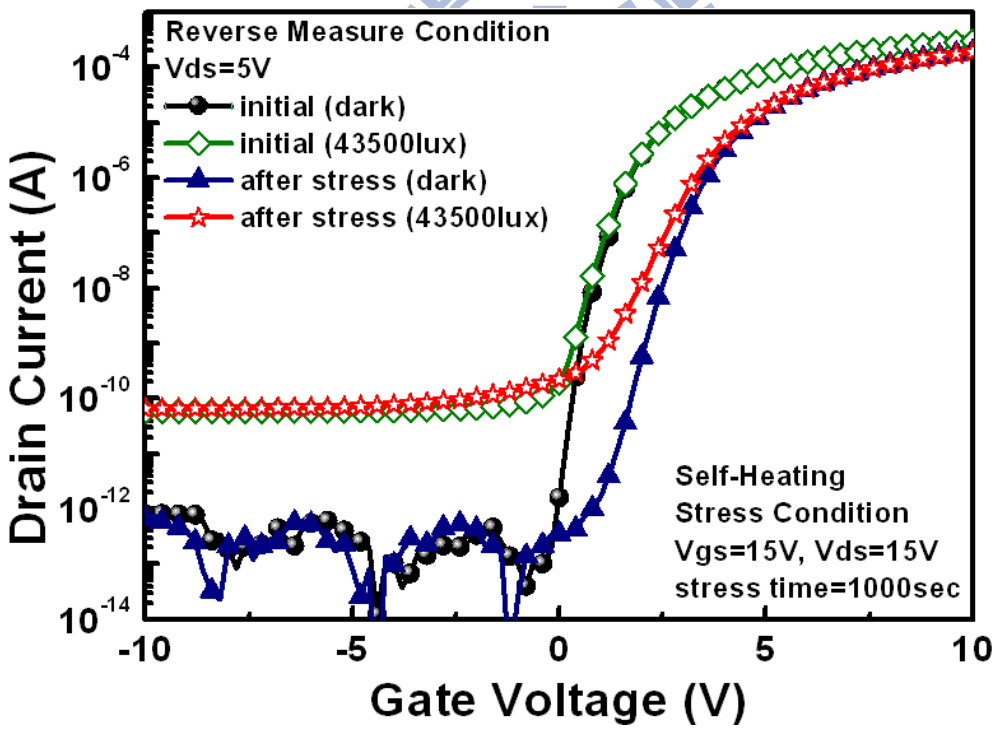


Figure 5-11 Drain bias dependence of ULC at different hot carrier stress times measured in the reverse mode.



(a)



(b)

Figure 5-12 The I_{ds}-V_{gs} transfer characteristics of TFTs with (a) forward and (b) reverse measurements in saturation region 5V drain voltage under different back illumination conditions for self heating stress.

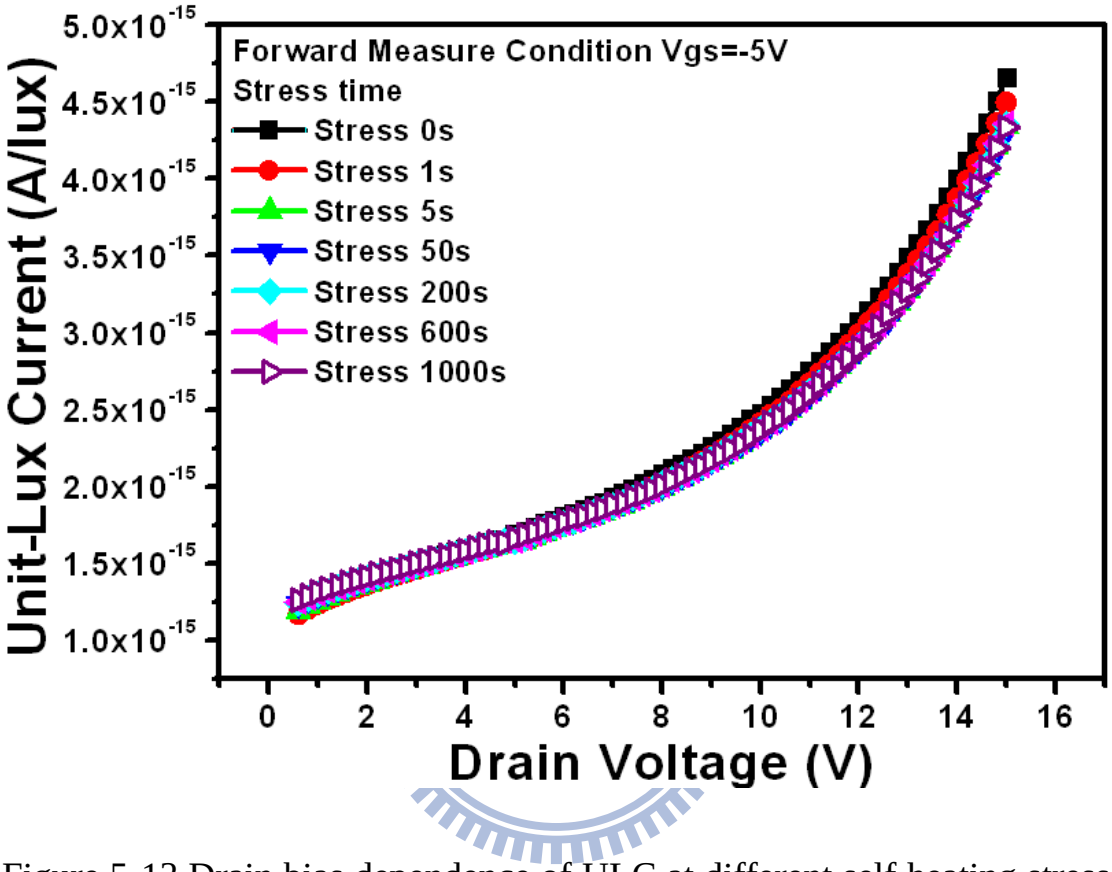


Figure 5-13 Drain bias dependence of ULC at different self heating stress times measured in the forward mode.

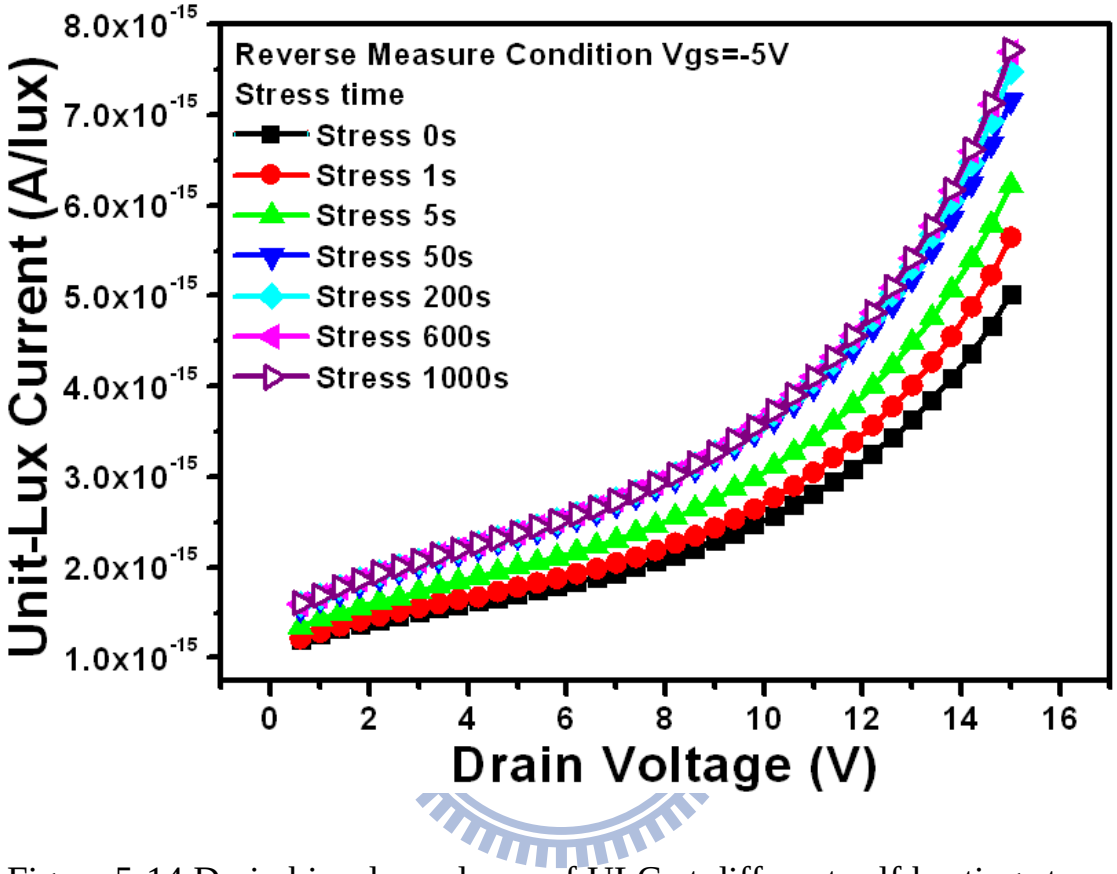
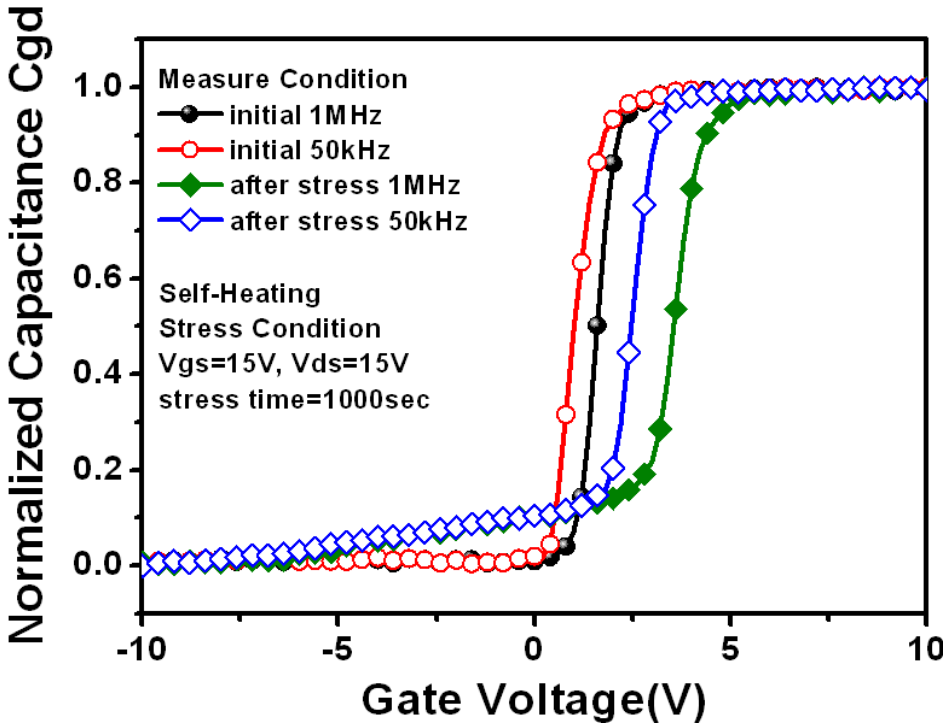
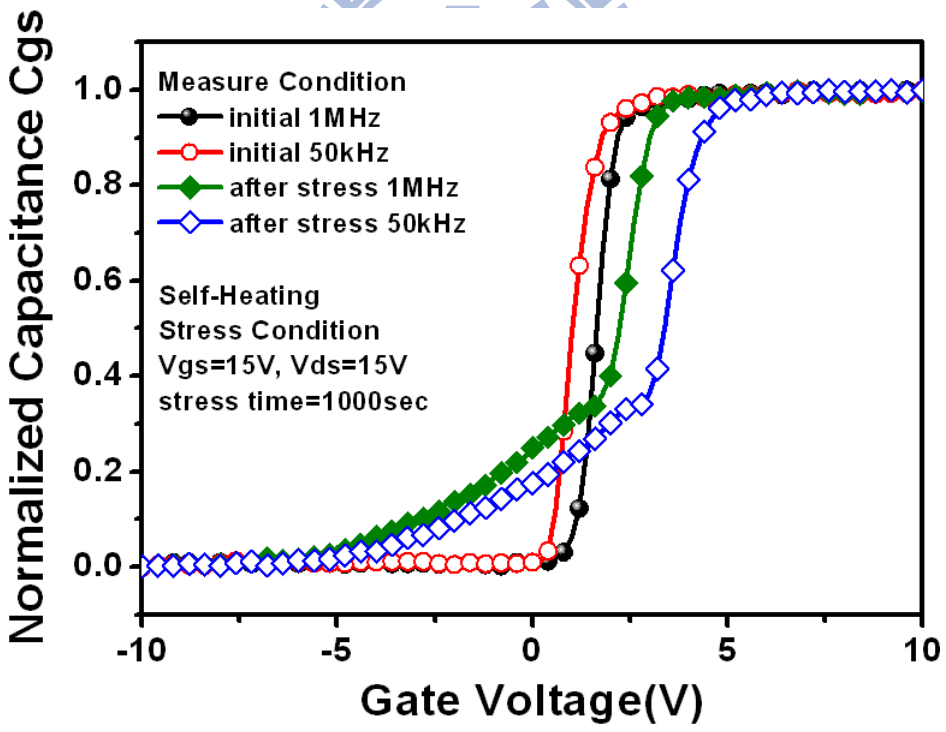


Figure 5-14 Drain bias dependence of ULC at different self heating stress times measured in the reverse mode.



(a)



(b)

Figure 5-15 The normalized (a) gate-to-drain capacitance C_{gd} and (b) gate-to-source capacitance C_{gs} curves before and after stress with different frequencies.

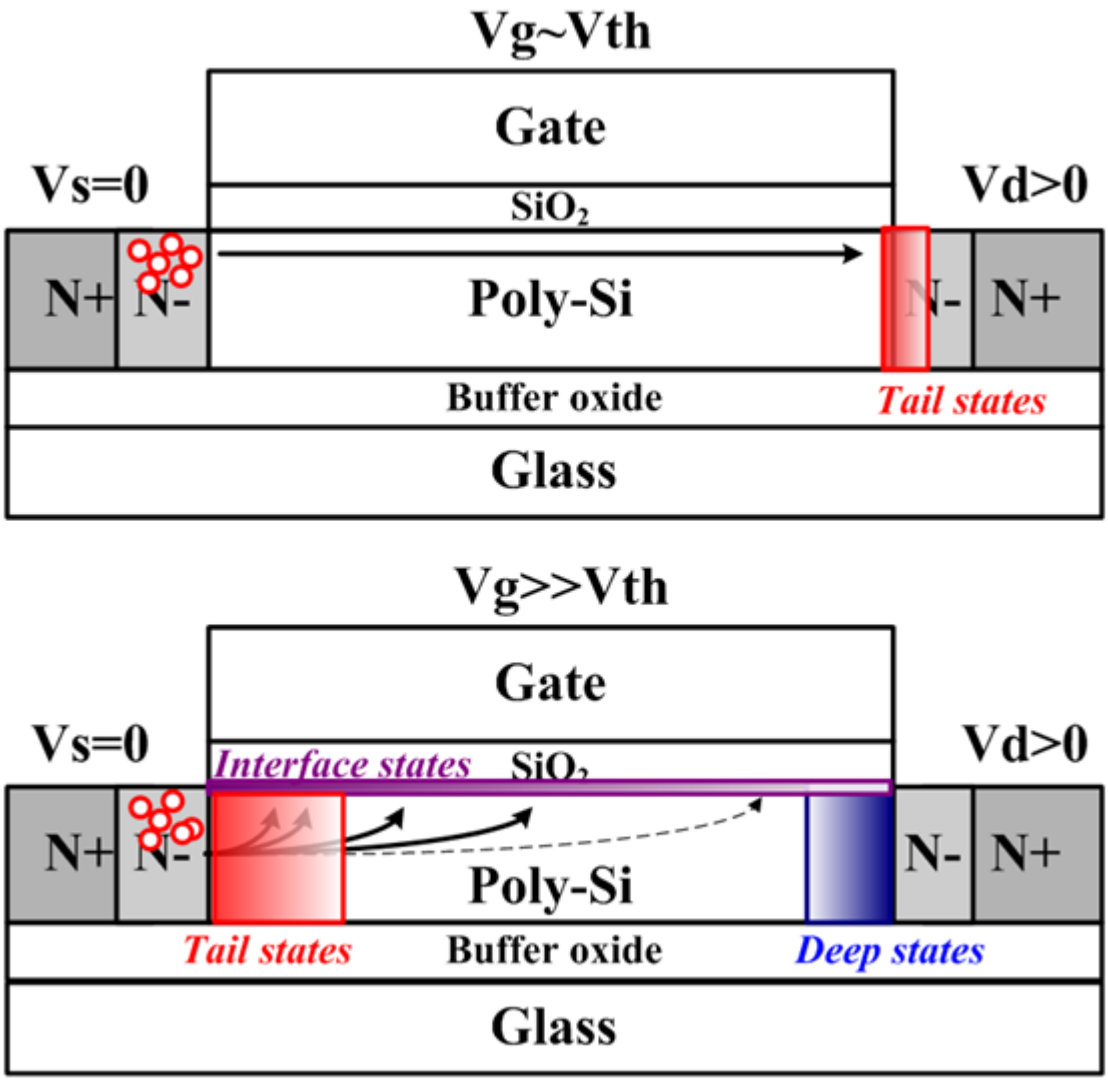


Figure 5-16 The cross section views of degradation model in TFT structure under hot carrier and self heating stress conditions.

		Hot carrier effect	Self heating effect
I-V analysis	Forward	Tail states	Deep states
	Reverse		
C-V analysis	Cgs	(none)	Interface states
	Cgd	Unknown states	Unknown states
Photo analysis	Source	(none)	Tail states*
	Drain	Tail states	Deep states

Table 5-4 The defect information of several analyses.

Chapter 6

Characterization of Thin film Transistor for Optical Sensor Application

6.1 Three-Dimension Poly Silicon Interaction Display

6.1.1 Motivation

The low temperature poly-silicon thin film transistor (LTPS TFT) is taken as a promising technology for its high mobility and the compatibility of consisting the peripheral circuits to realize the dream of system on glass (SOG). The photosensitivity is a significant consideration for achieving high image quality LCDs such as next generation three-dimensional (3D) system [6.1]. Some sensing functions using TFTs were already also demonstrated [6.2-6.4]. However, most of the conventional ambient light sensor systems were implemented by external discrete devices such as charge coupled device (CCD) sensor which cause additional cost and the design complexity. Alternatively, photo transistor based sensors allow the integration of TFT without extra change in the fabrication process. In proposed system, the system connect with forward and reverse measurements can be used to set up sensing direction. Then, the sensing disparity capability of gate metal shielding by itself photo transistor with embedded optical sensors is adaptive to capture the image near the panel.

6.1.2 Sensing Disparity Consideration of LTPS TFTs and Experiment

In this study, photo leakage current was induced by a halogen lamp irradiation stream with several neutral density filters through the objective of a microscope, and the light intensity was measured by digital luminous flux meter. The Top gate n-type poly-Si TFTs with lightly doped drain were used in the experiment. The typical I_D-V_G transfer characteristics of the LTPS TFT under illumination from dark to 31320 lux and rotatable probe station experimental setup are shown in Fig. 6-1.

It can be seen that the off current increases with the intensity of the incident light and it has weak gate bias dependence under higher ambient light intensity. Meanwhile, we use rotatable probe station to propose gate metal shielding by itself for poly-Si TFTs with top gate structures formed photosensitivity disparity structure to sense where the light comes from using forward and reverse measurement, as shown in Fig. 6-2. If light comes from left side, as Fig. 6-2 shown, the incident light partially eliminated under forward measurement and not covered under reverse

6.1.3 Results and Discussions

Fig. 6-3 (a) and (b) show forward and reverse measured photo currents verses negative gate bias with several right incident angles under 5100lux and 20500lux illumination conditions. We will offset I_{Dark} and only consider I_{Illum} which is defined to be the difference between I_{total} and I_{Dark}. It can be seen that the photo current of these two measurements are lifted up with incident angles and both are independent to gate bias. The photo current of device under reverse operated are less than forward measured. It due to the photo leakage current originating from right light illuminated and which are partially eliminated by the gate metal under reverse measurement. These results reveal such system we proposed has possibility to sense working directionality environment illumination of per pixel.

In the aspects of analyzing photo sensing sensitivity, an index the defined as the ratio of forward and reverse photo current $\alpha = I_F/I_R$ are used to evaluate the performance of light sensors. Fig. 6-4 show forward and reverse photo currents ratio verses incident angles under 5100lux and 20600lux illumination conditions. As can be seen, the tendency of sensitive ratio decreases with raising incident angles. It connects with forward and reverse measurements in saturation region can be used to guide left-right different directions of image pixels. Thus, we can choose proper forward and reverse photo current ratio to confirm oblique position, as Fig. 6-5 shown. Moreover, we take further steps to find height of object along the direction of the barrier strip for two view parallax barrier type three dimensional interaction display [6.5].

6.2 Sensing Circuits of Source Follower Type using LTPS TFTs

6.2.1 Motivation

Generally, the ambient light sensing function has been implemented using an additional chip or several components in the display module for mobile applications [6.6]. However, there are problems associated with the increase in the volume of the display module and difficulties in the manufacturing of the display module that allows light to be guided to the chip. On the other hand, if an ambient light sensing circuit is integrated to the panel even the pixel using LTPS TFTs, this can both decrease the display module volume and lower the manufacturing cost. Because the ambient light sensing device is fabricated using thin-film technology and crystallization process, the detection area, the LDD, is very thin. Moreover, the photo current of LTPS TFTs is lower than that of the photodiode used in complementary metal oxide semiconductor (CMOS) image sensor (CIS). It is very difficult to design a readout circuit that

performs very sensitively to readout such small photo leakage current. Therefore, we proposed a light sensing circuit that can convert photo leakage current to analog voltage signal and buffer the converted voltage signal to analog-to-digital converter (ADC). Measurements using the proposed light sensing circuit are performed to verify the performance of the proposed circuit.

6.2.2 Source Follower and Operation Principle

The schematic diagram of the proposed ambient light sensor and its timing diagram, as shown in Fig. 6-6, is proposed for the examine discharge process for the illumination effect. It consists of a TFT (T_1), a source follower (T_2) and a capacitor (C_S). The T_1 TFT operates as current source in the sensor, so the output current strongly depends on the electrical characteristics of the T_1. The operating principles can be described as two periods shown in the timing diagram. In a charge period (1), when gate signals become high, T_1 TFT is turned on. Thereby, a voltage difference (V_g-V_{th}) is stored in capacitor C_S. The photo-leakage current, which is determined by the intensity of the ambient light, is converted into voltage difference through discharging process. The voltage difference can be expressed as V_{gate}-V_{data}. In a discharge period (2), the gate voltage of TFT T_1 is applied so that T_1 is operating in the subthreshold region while sensing operation.

6.2.3 Simulation Method and Results

In the RPI models of TFT, there is no photo leakage current model for SPICE simulation [6.7], so we can't simulate the photo leakage current under different

illumination directly. We have to modify the simulation method according to illuminated characteristics of device. We take subthreshold region for example. Fig. 6-7 shows the illumination dependence of I_D-V_D characteristics curve; the drain current increased while the illumination intensity enhanced. We selected the approximately linear region of the I_D-V_D curve to fit the formula, which can be expressed as $I_D = I_0(L) + V_D / R_0(L)$, where I_0 (L) and 1/R_0 (L) are intercept and slope, which are illumination dependence. Therefore, we use the different current sources and resistances parallel to represent the different photo leakage currents of TFT. Table 6-1 shows the values of I_0 (L) and R_0 (L) at V_{gs}=0.5V (subthreshold region) with the illumination intensity variation. When the illumination intensity is changed, the value of I_0 (L) and R_0 are changed with it.

Fig. 6-8 shows the SPICE simulation results of TFT (W/L=20um/5um), we added a current source I_0 (L) and a resistance R_0 parallel to simulate the photo leakage current as shown in its inset. In this figure, we can see the results already can represent the photo leakage current. Consequently, we have figured out a method to modify the simulation model. Fig. 6-9(a) and 6-9(b) show the modified 2T1C light-sensing circuit model for simulation and its time diagram. We can simulate the situations of TFT under illumination and in the dark by this model. The simulation results are shown in the Fig. 6-10. We can see in this figure, as expected, the output voltage (V_{out}) is discharged by the photo leakage current of T_1. The larger the illumination intensity, the faster the discharge rate are. Its response time is around several mini seconds.

6.2.4 Results and Discussion

In Fig. 6-11 shows LTPS TFTs transfer characteristics in the dark as well as

irradiated at six different levels of illumination from the front side at V_{DS}=10V. For the three main TFT operating regimes namely, on, subthreshold, and off regime, the current level and photosensitivity are discussed. To analyze in detail the photosensitivity, we define the ratio of the TFT drain current under illumination (I_{D}_illum) to that in the dark (I_{D}_dark) as $R_{L/D} = I_{D\_illum} / I_{D\_dark}$. We chose V_{GS}=3V, 0.5V, -2V to bias device in the on, subthreshold, and off regime, respectively. We can observe a significant difference of the photosensitivity between these regimes as shown in Fig. 6-11 and current levels are shown in its inset. In subthreshold region and off region, we can see the photosensitivity is significantly higher than that in the on-state, which is almost independent of illumination intensity. Although the current level of on-state is 5 to 6 orders larger than the others, TFT has poorer $R_{L/D}$ in the on-state than those in the subthreshold and off-state. In the aspects of photosensitivity, on regime is not suitable for the light sensing application, but it is suitable for being the readout part.

Because the proposed sensor must operate with the display panel, we have to read out the output signals during the operation frequency of the display panel, 60 Hz (16.7ms). The operation frequencies of subthreshold and OFF region that we chose are 100 Hz and 10 Hz, respectively. The output voltage of the proposed circuit is measured by oscilloscope during discharge period under halogen lamp illuminative variations from 0 to 31320lux, and its waveforms are shown in Fig. 6-12(a) and 6-12(b). The discharging rate of V_{out} which is due to photo leakage can be expressed as dV/dt. Consequently, the slopes (dV/dt) of the waveforms can reflect the subthreshold or OFF current under illumination and in the dark by the equation as follow $I_{leakage}=(dV_{out}/dt) \cdot C_s$ (6-1), so that the illumination intensity can be sensed. However, in the discharge period, the photo leakage current drained away through the

T1. At the same time, the VA drops to "V_{in_low}" with time. Hence, we have to verify the accuracy of the function of the circuit. The full well capacity or saturation charge Q_{sat} is given by $Q_{sat} = C \cdot V = I \cdot t$ (6-2)

We selected the approximately linear region of the I_D-V_D curve to fit the formula, which can be expressed as $I_D = I_0(L) + A_0(L) \cdot V_D$ (6-3)

an ordinary differential equation of V_A can be expressed as

$$I_0(L) + A_0(L) \cdot V_A(t) = C_S \cdot \frac{dV_A(t)}{dt} \quad (6\text{-}4)$$

After solving the equation, we can get $V_A(t) = \alpha \cdot \exp(\frac{A_0(L)}{Cs} \cdot t) - \frac{I_0(L)}{A_0(L)}$ (6-5)

Expanding equation (6-5) by Taylor series

$$V_A(t) = \alpha \cdot [1 + \frac{A_0(L)}{C_S} t + \frac{1}{2}(\frac{A_0(L)}{C_S} t)^2 + \cdots] - \frac{I_0(L)}{A_0(L)} \quad (6\text{-}6)$$

because of our design, $\frac{A_0(L)}{C_S} << 1$ and $\alpha = V_A(0) + \frac{I_0(L)}{A_0(L)}$,

where $V_A(0)$ is the initial voltage "V_{in_high}" during discharge period. Therefore, equation (6-6) can be simplified as $V_A(t) = V_A(0) + [\frac{I_0(L)}{C_S} + \frac{A_0(L)}{C_S} \cdot V_A(0)] \cdot t$ (6-7)

Equation (6-7) shows that the *dV/dt* only depends on illumination intensity.

6.2.5 Devices Variation and Calibration

However, the device variation is always an important issue of LTPS TFTs. It is clear that for any circuit to be manufacturable, device-to-device uniformity must be controlled. Qualitatively, the uniformity of LTPS TFTs is expected to be worse than that of MOS transistors made in single-crystal materials. This is because the TFTs are composed of grains, whose number, shape, and quality could vary from device to device. Even the devices fabricated under the identical process, LTPS TFTs still have different electrical characteristics due to the influence from different numbers of the

inter-grain and intra-grain defects [6.8-6.9]. Two of the differences are significant to the sensing circuit. One is threshold voltage (V_{th}) variation which is dominant in the subthreshold region and the other one is initial off current variation. Therefore, the poly-Si TFTs are found to suffer from serious photosensitive device variation behavior which results from the diverse and complicated grain distribution in the poly-Si film.

6.2.5.1. Off Current Variation

The measured output voltages in off region of fifteen proposed light-sensing circuits on the same glass with respect to the illumination intensity and an average line of these results are shown in Fig. 6-13. We can see the results are non-uniform. With the illumination intensity increase, the error becomes larger and larger. The deviation resulting from initial off current variation will cause a significant error of output voltage of our light sensing circuit.

6.2.5.2. Threshold Voltage Shift

In order to evaluate the influence from V_{th} shift on the sensing results, we simulated the V_{th} shift by changing Vg low level. Fig. 14 (a) and (b) show the influence of V_{th} shift both on subthreshold region and off region. We can see in these figures, only a little V_{th} shift would cause a significant deviation of output voltage in the subthreshold region, as expected. The measurement error is not controllable. On the other hand, it is obvious that the impact of the V_{th} differences in the off region is slighter than that in the subthreshold region. For this reason, only the deviation of V_{th} difference of subthreshold region is considered. We propose a V_{th} shift compensation

circuit to calibrate the deviation of our sensor. We instead change V_g to simulate that if the V_{th} shifts. Thus we can evaluate the variation under V_{th} shift.

6.2.5.3. Off Current Variation Calibration Method

We try to use the statistical method to reduce the effect of off current variation. Based on the average line, the error of illumination intensity is about 4700lx and the signal to noise ratio is about 7. Where the signal to noise ratio is defined as following:

S/N=maximum illumination intensity/error (6-8)

We divided the fifteen samples into several groups, two samples, three samples, and five samples as the average units. Fig. 6-15 shows five samples as an average unit. We can clearly see that the deviation is greatly reduced after calibration using statistical method. The error of the illumination intensity is reduced to 3200lux, 2400lux, and 1200lux; and the S/N ratio is increased to 10, 13, and 26, respectively. Therefore, we can increase the resolution of the sensor. We also believe that if we use more samples average for a unit, the resolution of our sensor can be even more improved.

6.2.5.4. Threshold Voltage Shift Compensation Circuit

In a LTPS TFT circuit, V_{th} non-uniformity is always a serious issue [6.10]. In addition to the initial V_{th} difference, the degradation of the driving TFTs by the lapse of operation time will cause V_{th} shift. Therefore, it is important to compensate the V_{th} shift variation [6.11-6.12]. Fig. 6-16 (a) shows the schematic of our proposed 4T2C light-sensing circuit with compensation part and (b) its time diagram. The driving sequence consists of initialization period, compensation period, and sensing period

including charge and discharge.

In the initialization period, when V_{in}, V_S, and Φ_2 signals become "low" and V_g, Φ_1 signals become "high", and thus T_1 and SW_1 turn on, and T_2 and SW_2 turn off. Because the C_{vt} is short when SW_1 turn on and the voltages of V_A and V_S of C_S are equal, we can initialize the charges which stored in these two capacitors to be zero.

In the compensation period, when Φ_1 and V_g signals become "low" and V_S signal becomes "high", and thus SW_1 turns off. Based on the principle of charge conservation, V_B is equal to "V_{g_low}", V_A is equal to "V_{S_high}", and T_1 turns off. At the same time, Φ_2 signal becomes "high" and SW_2 turns on. The voltage of V_B will charge to "V_{A_high}" and then T1 turns on again. At this time, V_A is discharged through T1 to "V_{in_low}" and V_B follows it till the voltages of V_A and V_B are equal to the threshold voltage of T_1. Therefore, T_1 turns off and the V_{th} is stored in the C_{vt}, where V_A and V_B can be expressed as

$$V_A = V_B = V_{th} - V_{g\_low} \qquad (6\text{-}9)$$

In the first half of sensing period (charge), when Φ_2 and V_S signals become "low" and Vg signal becomes "high", the voltage of V_B will become "$V_{g\_high}+V_{th}-V_{g\_low}$" and T_1 turns on again. V_{in} signal becomes "V_{in_high}" at the same time. Because we want to operate the sensor in the approximately linear region as mentioned in previous section, we set the voltage of "V_{in_high}" to be small than 8V. Then the V_A, which is held by C_S, is charged to "V_{in_high}".

Finally, in the second half of sensing period (discharge), we want to operate the sensor in the subthreshold region, so the signal of V_g becomes "V_{g_sub}". Simultaneously, the signal of V_{in} becomes "V_{in_low}". Therefore, the V_A which is held by C_S is discharged by the photo leakage current of T_1.

The proposed threshold voltage shift compensation circuit can overcome the

variation due to V_{th} shift. Fig. 6-17 (a) and (b) show the fifty times of Monte Carlo simulation results of the proposed light-sensing circuit before and after compensation when V_{th} shift is ±0.5V. We can clearly see the variation is greatly reduced.

6.2.6 Digitization

In order to restrain the interference of noise and avoid the error due to V_{th} shift of source follower, a high accuracy ADC has been proposed. The digitization circuit is shown in Fig. 6-18 (a), which consists of two comparators, a "AND" logic gate and a counter. Two reference voltages V_{ref_1} and V_{ref_2} are used to compare with V_{out}, we can adjust the range of Vout with different signals "V_{ref_1}" and "V_{ref_2}". If $V_{out} > V_{ref\_1} > V_{ref\_2}$ or $V_{ref\_1} > V_{ref\_2} > V_{out}$, the output of logic gate C is always "0", as shown in Fig. 6-18 (b). Only when $V_{ref\_1} > V_{out} > V_{ref\_2}$, the output of logic gate C will be the clock numbers of CLK. Therefore, we can discriminate the slopes of V_{out} between different illumination intensities by counting the clock numbers. Moreover, in order to improve the resolution of the ADC, we can increase the speed of the CLK.

6.3 Light sensor for detecting uniformity of backlight intensity

For back light illumination application, low power consumption is very important. Portable consumer electronic products, such as mobile phone, PDA, always move toward a tendency of constantly reducing their power consumption because users expect that they can operate for a long time. For LCD-based products, most power consumption is attributed to backlight, accordingly, backlight power saving is considered one of the most effective ways to reduce LCD energy dissipation. In recent years, LED backlighting was sought to replace the fluorescent backlighting because

the TFT-LCDs with LED backlighting have advantages of greater efficiency, long lifetime and environmental compatibility. Since the LED backlight modules could be non-uniform in panel or degrade after a long time operation. These situations all have the same phenomenon that is the changing of backlight intensity. In this work, we also can use our back light research to propose the backlight sensor for the accurate backlight intensity. We can use the backlight sensors to detect the light intensity, and determine the intensity whether or not to achieve the value that it should be.

6.4 Conclusion

We proposed system connect with forward and reverse measurements can be used to set up sensing direction in active-matrix displays. Due to sensing disparity capability of gate metal shielding by itself, it has potential used to photo transistors with embedded optical sensors to capture three dimensional images near the panel. This system is without extra novel device process development and it is expected that the integration in the pixels with the same device of sensing system onto the panel. Meanwhile, a newly developed light sensing circuit using the identical LTPS TFTs fabrication processes has been proposed. It can perform sensing operation and trustworthy readout operation through amplifying small photo leakage current to analog voltage. Due to the poor uniformity of LTPS TFTs as experimental results shown, we also proposed calibration methods to reduce the illumination intensity error from 4700lux to 1200lux and compensate the V_{th} shift variation. On the other hand, we study on the feasibility of LTPS TFTs for light sensing application. The off region would be more appropriate for the purpose that is to accurately quantify the light intensity. Both front light researches would provide the possibility for the light sensor array integrated in the pixels with the same device of LTPS TFTs.

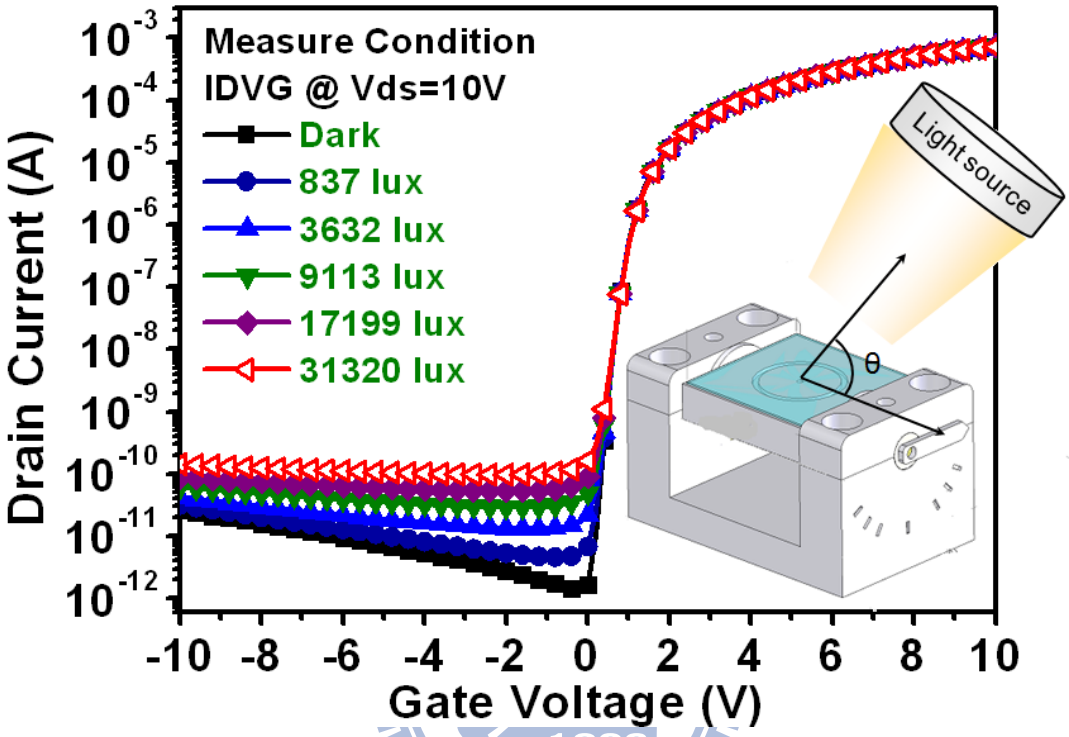


Figure 6-1 The I_D-V_G transfer characteristics under illumination from dark to 31320 lux. (Figure insert) rotatable probe station experimental setup.

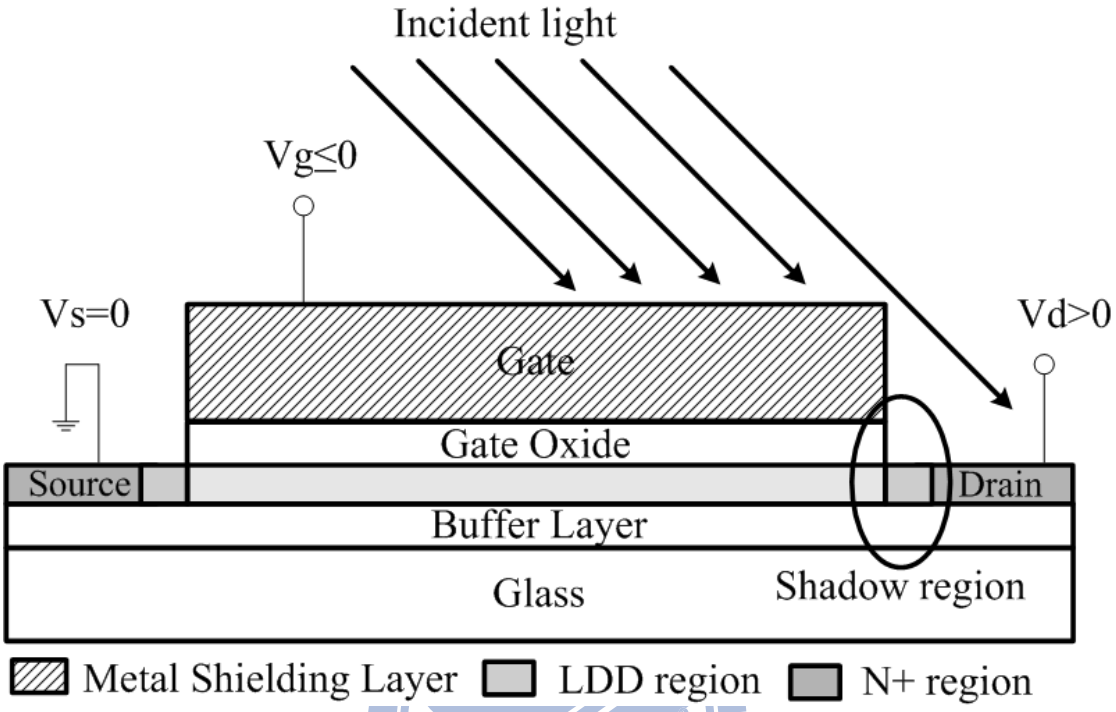
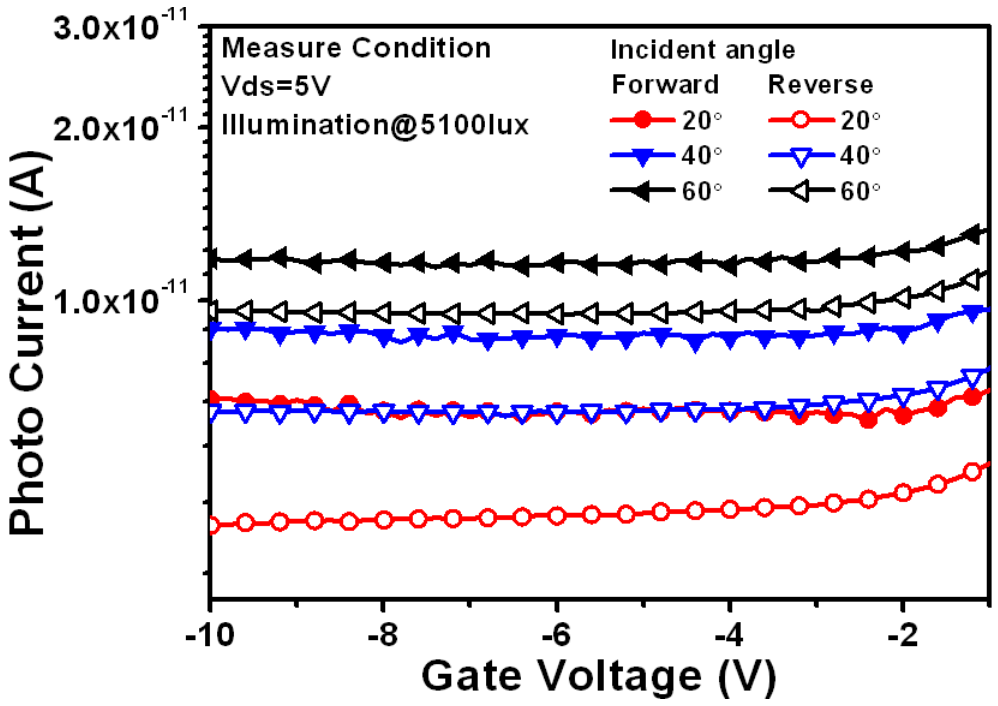
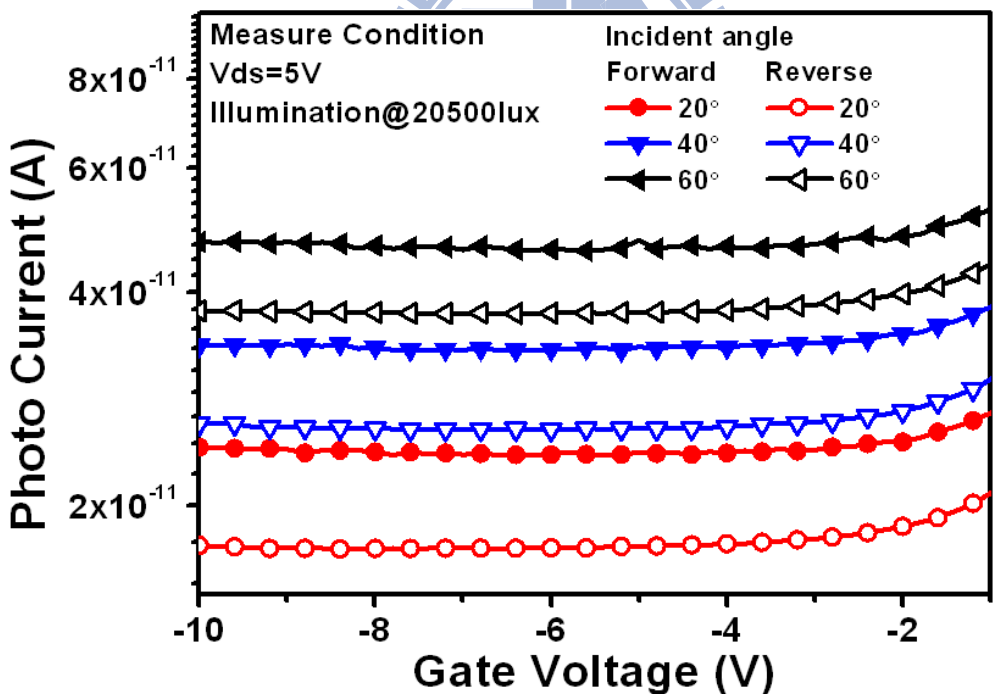


Figure 6-2 Gate metal shielding by itself for poly-Si TFTs.



(a)



(b)

Figure 6-3 The forward and reverse measured photo currents verses negative gate bias with several incident angles under (a) 5100 lux (b) 20500 lux illumination conditions.

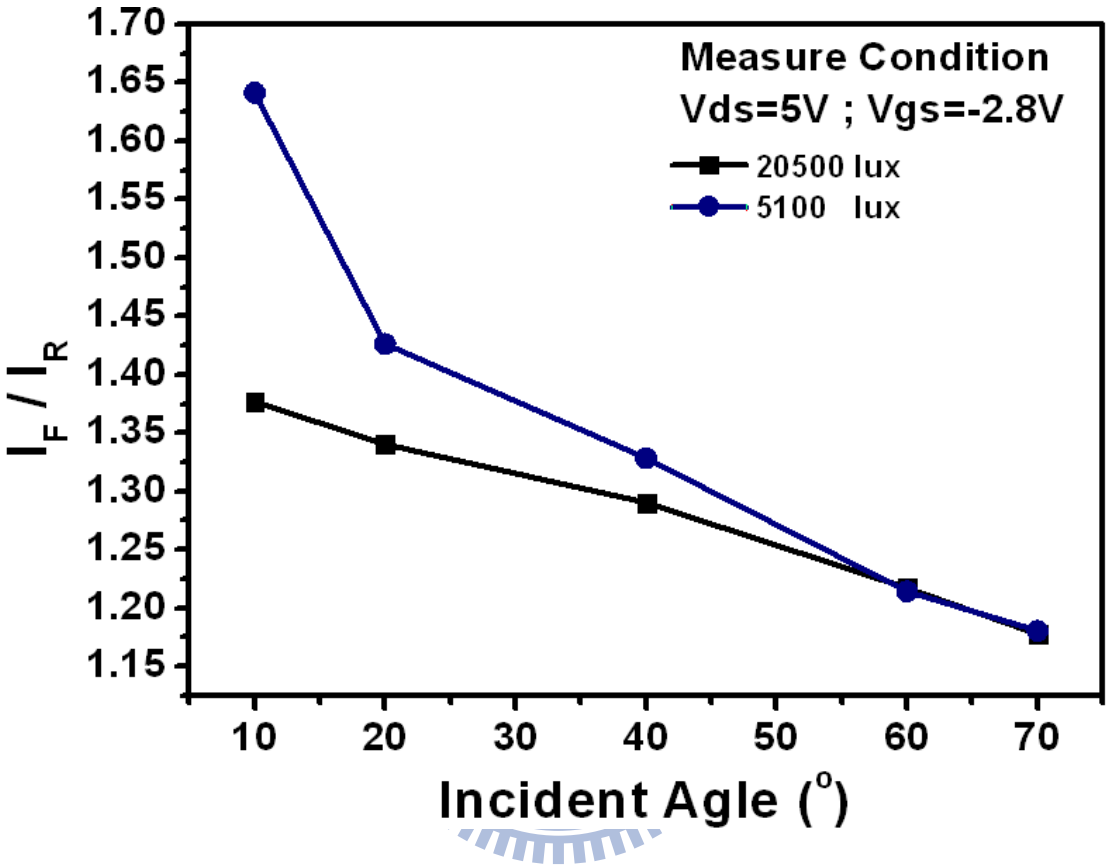


Figure 6-4 Forward and reverse photo currents ratio verses incident angles under 5100 lux and 20600 lux illumination conditions.

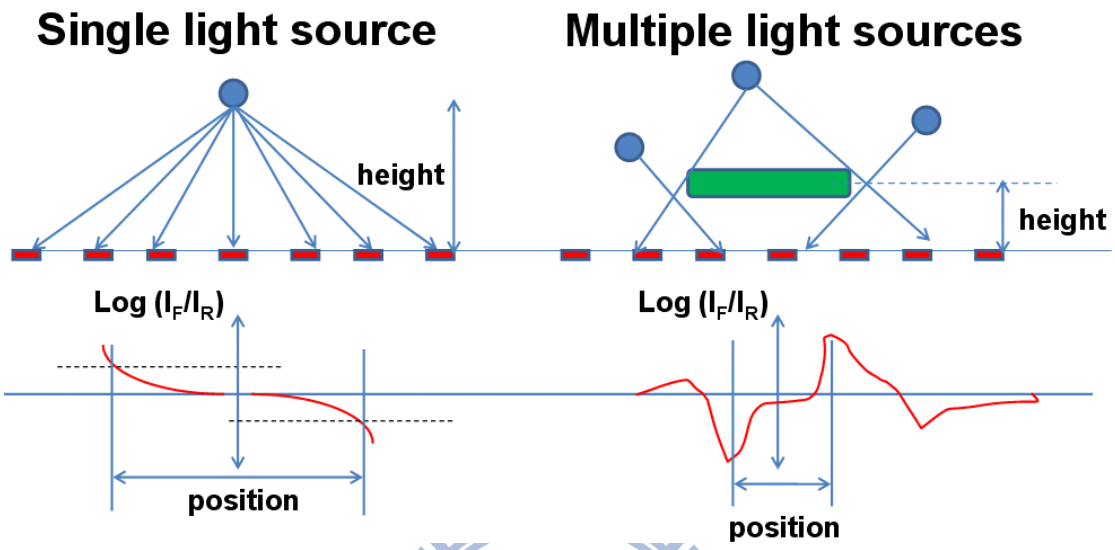


Figure 6-5 Using LTPS TFTs as oblique light sensors for three dimensional interaction display (a) Single light source (b) Multiple light sources.

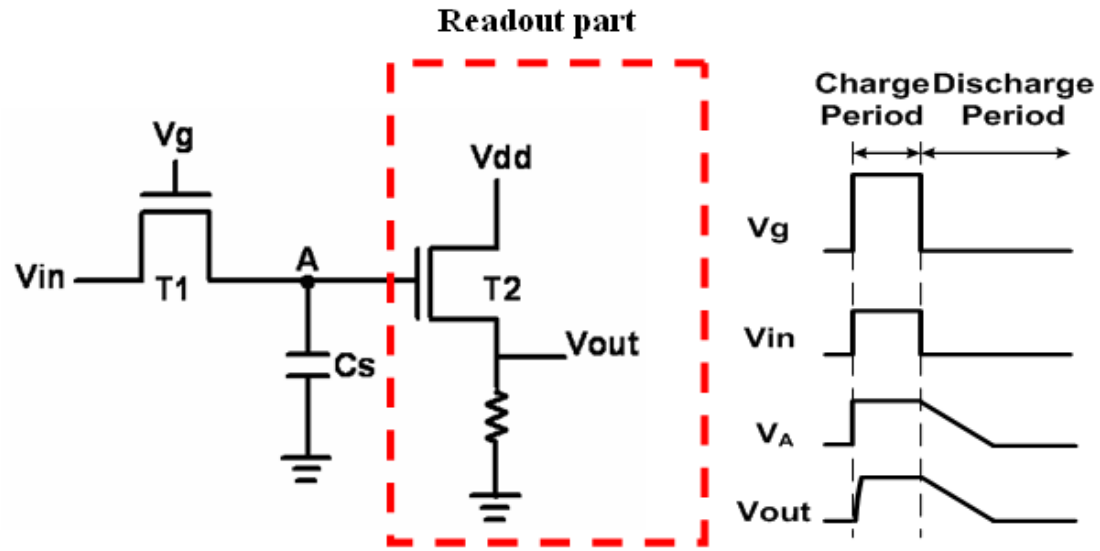


Figure 6-6 Schematic diagram of proposed 2T1C light sensing circuit and its timing sequence.

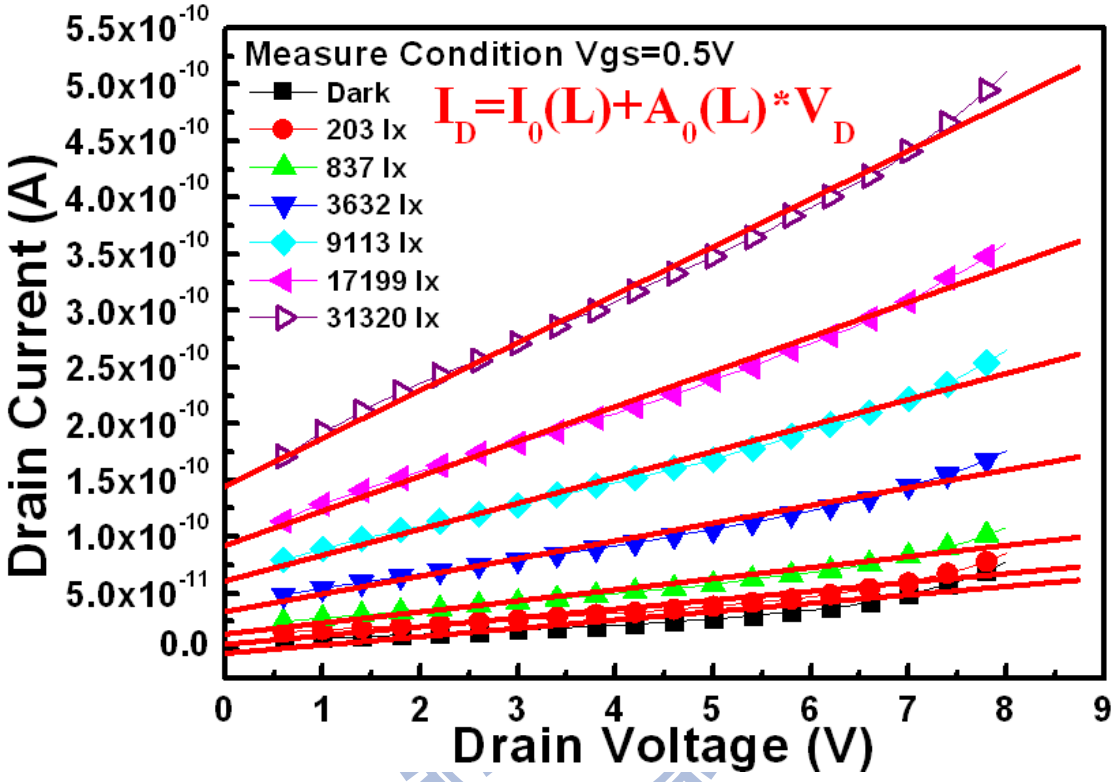
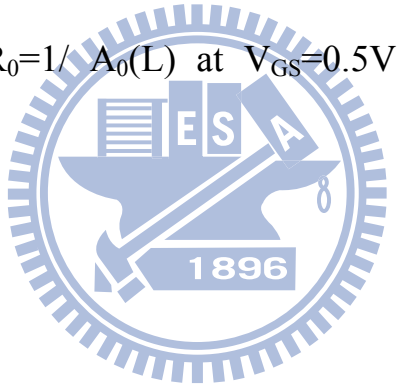


Figure 6-7 Illumination dependence of ID-VD characteristic and its fitting formula.

Brightness	I_0 (L)	$R_0=1/A_0$ (L)
Dark	2.40E-12	1.81E+11
203 lux	9.34E-12	1.58E+11
837 lux	1.80E-11	1.18E+11
3632 lux	3.82E-11	7.06E+10
9113 lux	6.59E-11	4.71E+10
17199 lux	9.80E-11	3.47E+10
31320 lux	1.52E-10	2.50E+10

Table 6-1 I_0(L) and R_0=1/ A_0(L) at V_{GS}=0.5V with the illumination intensity variation.



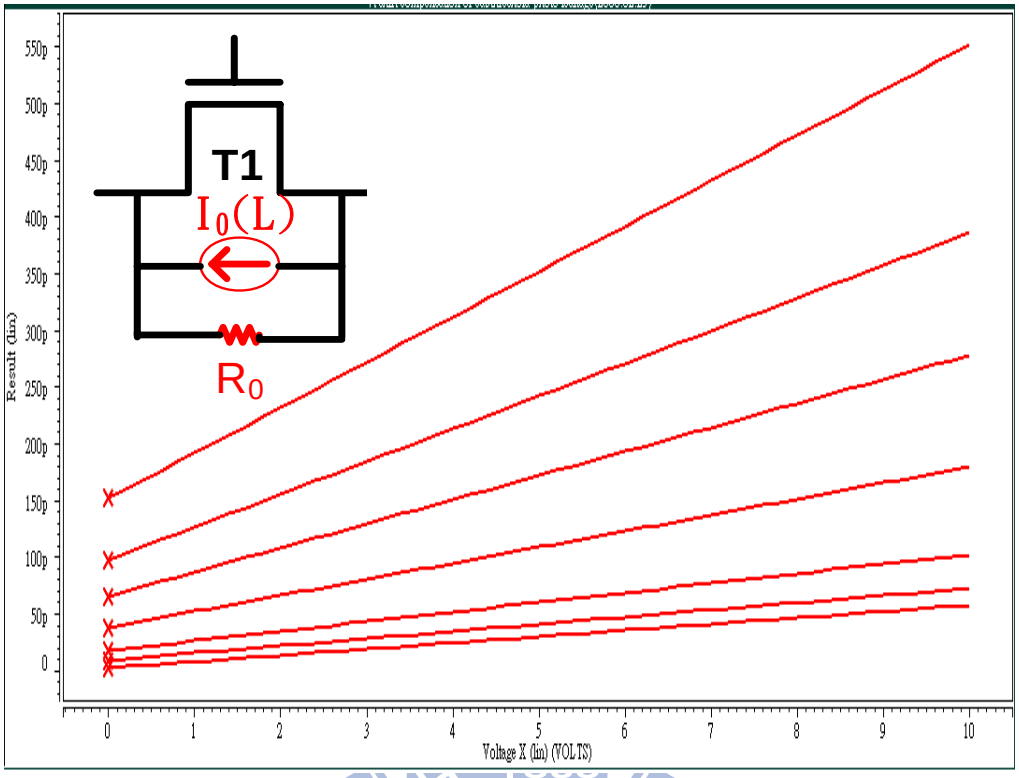


Figure 6-8 SPICE simulation results of TFT (W/L=20um/5um).

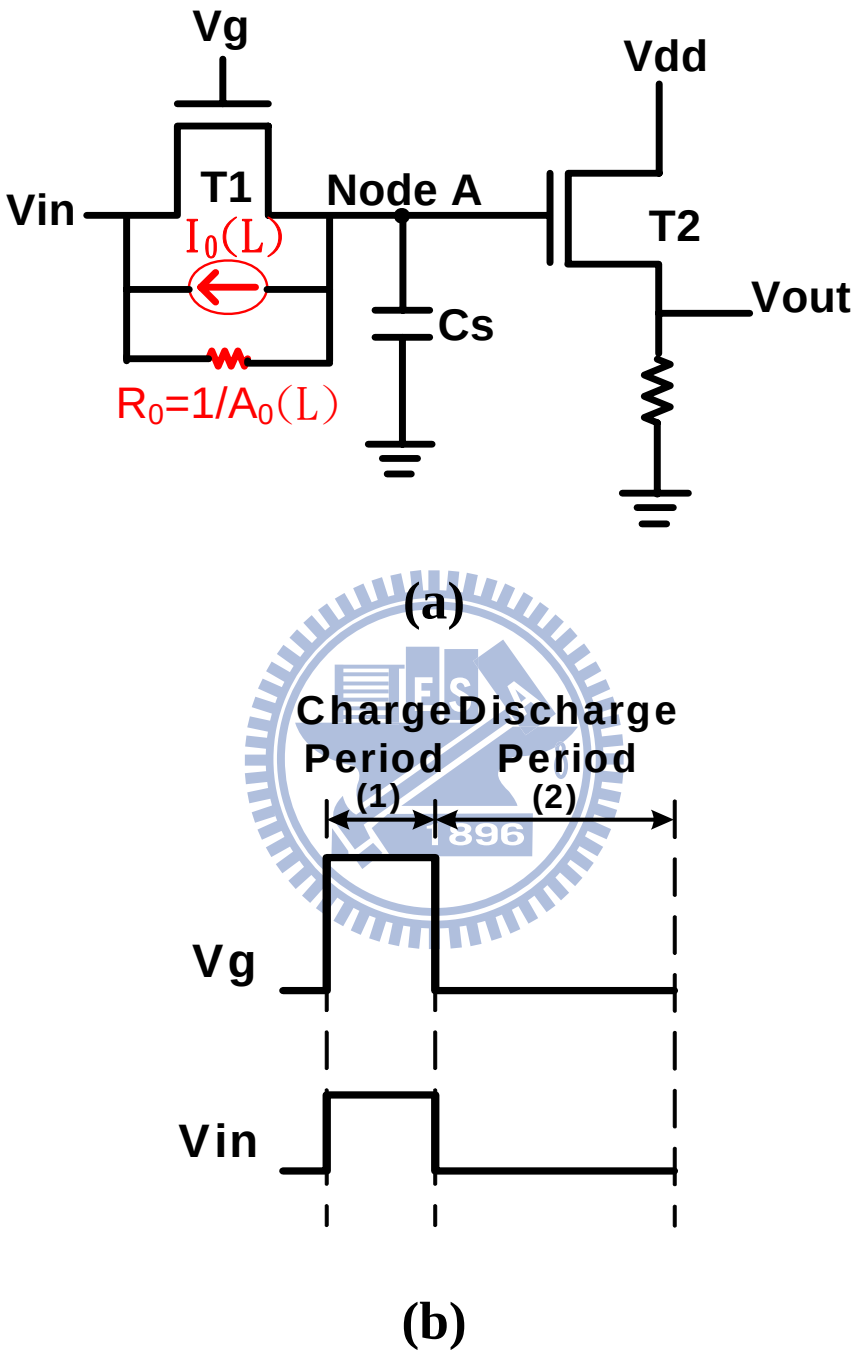


Figure 6-9 (a) The modified 2T1C light-sensing circuit model for simulation (b) its time diagram.

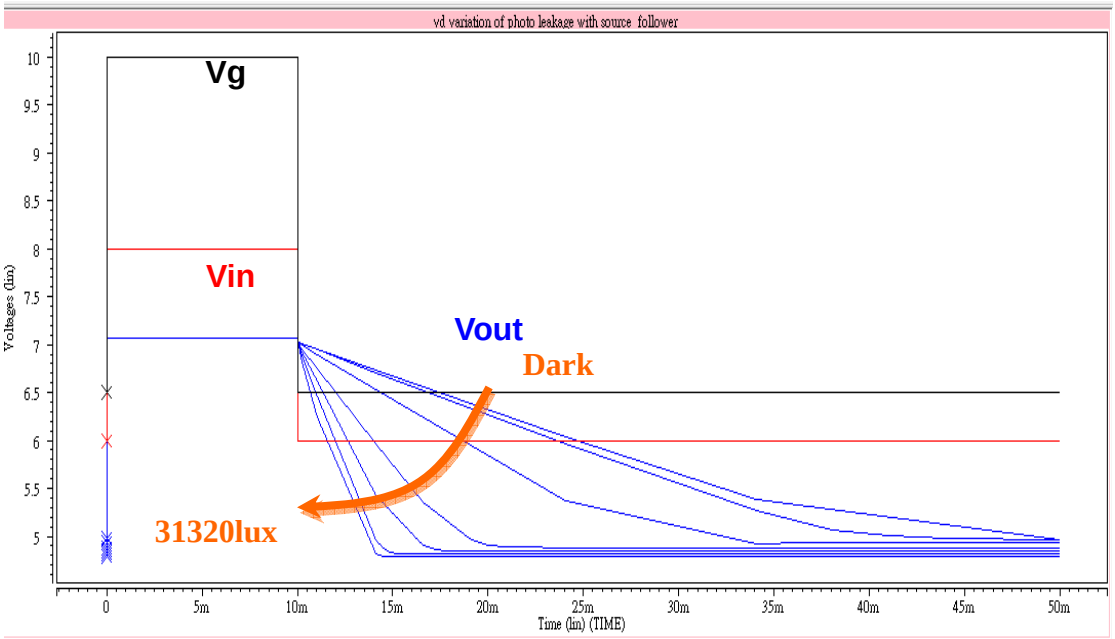


Figure 6-10 Simulation results under illumination and in the dark.

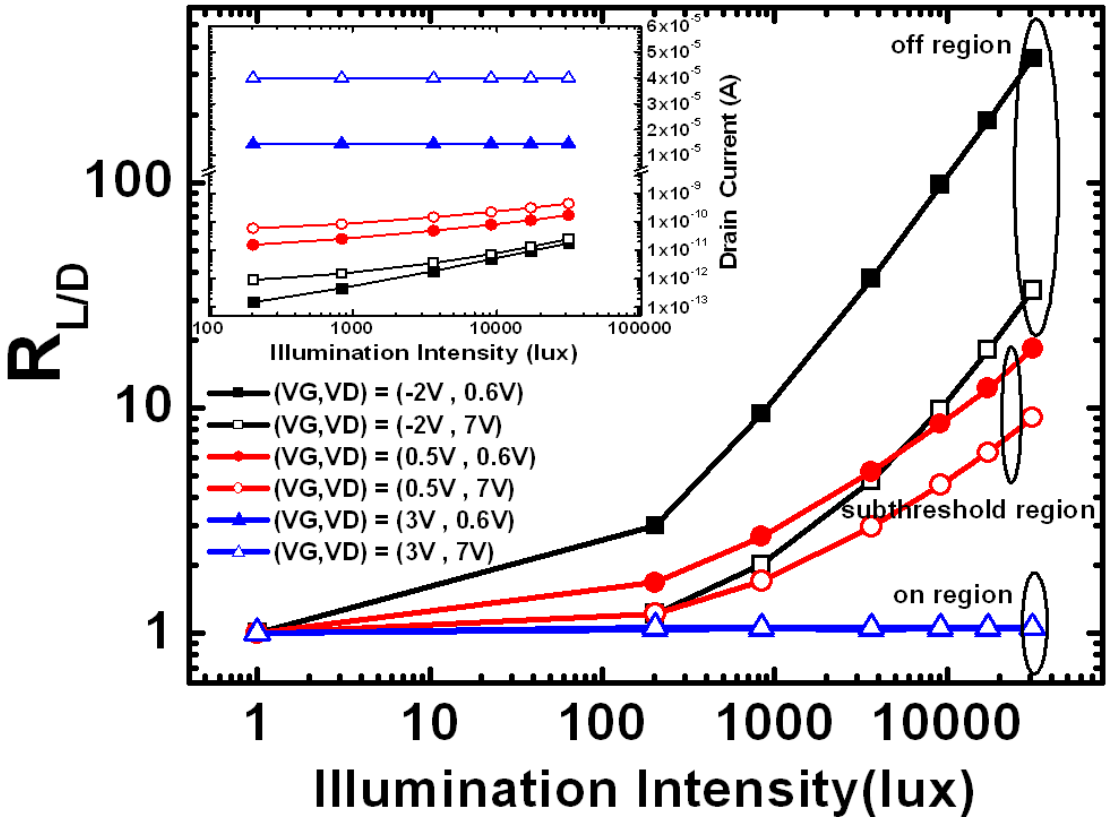
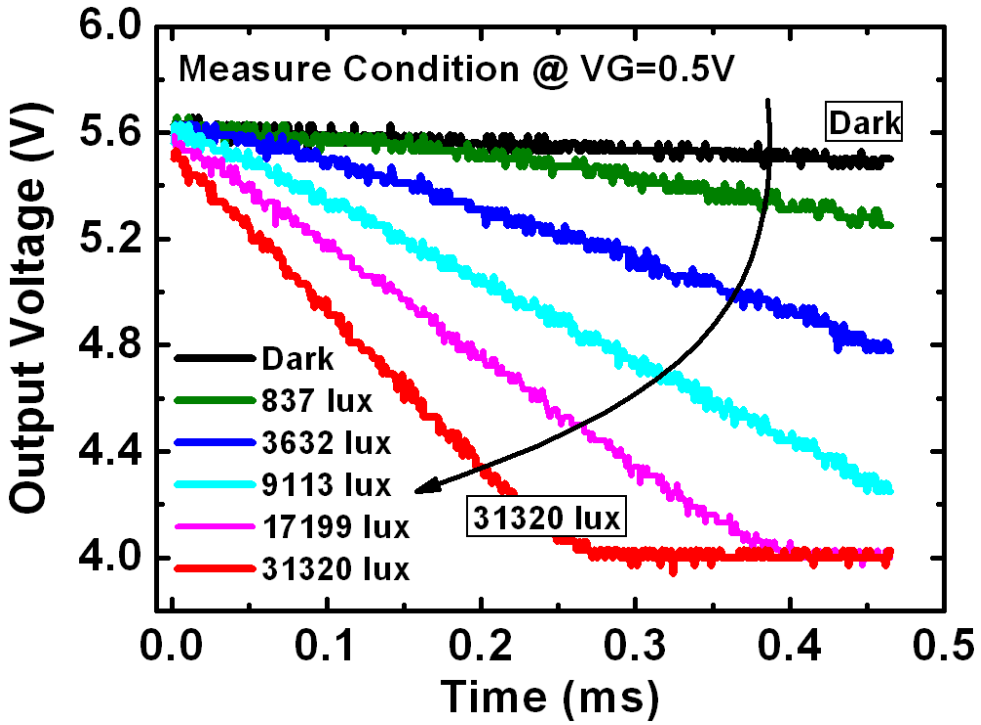
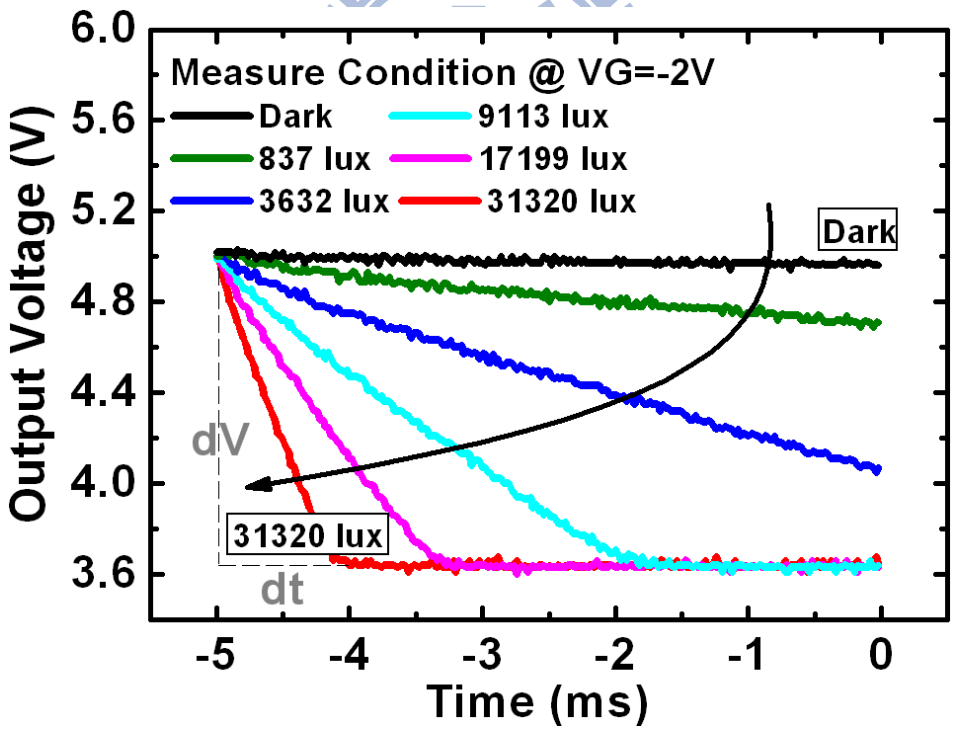


Figure 6-11 The comparison of the current ratio of under illumination and in the dark $R_{L/D}$ among on, subthreshold, and off region and that of current level (inset).



(a)



(b)

Figure 6-12 Measured waveforms of output voltages of proposed 2T1C light-sensing circuit illuminative variations from dark to 31320 lux on (a) subthreshold region and (b) off region.

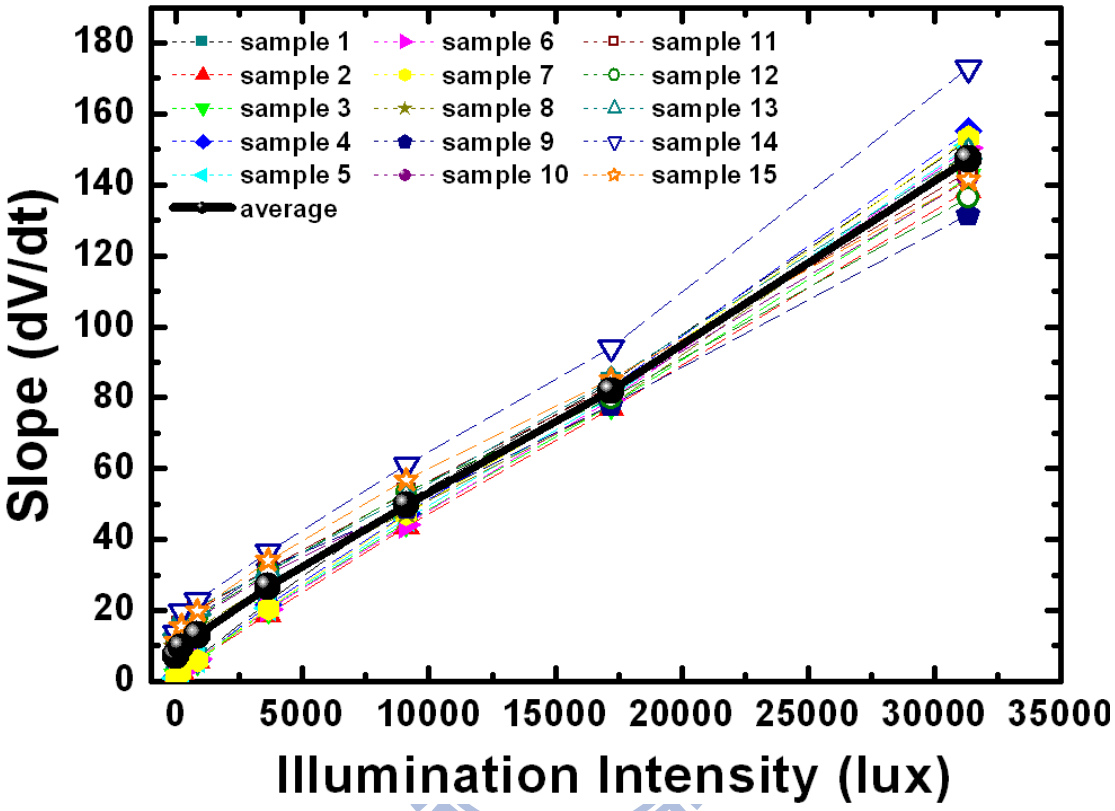
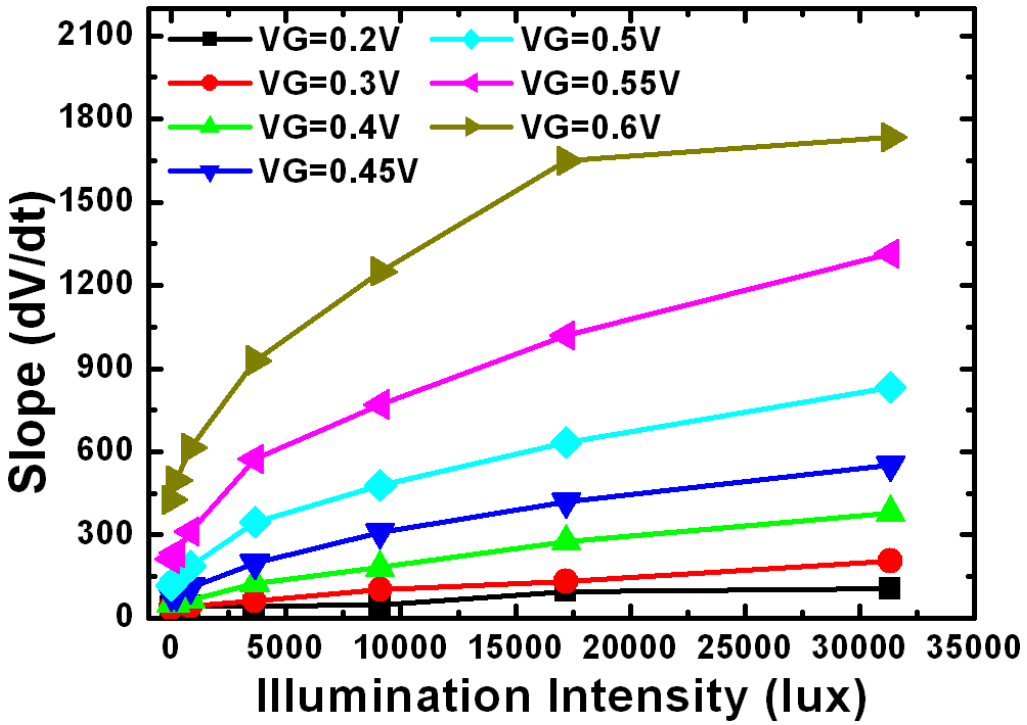
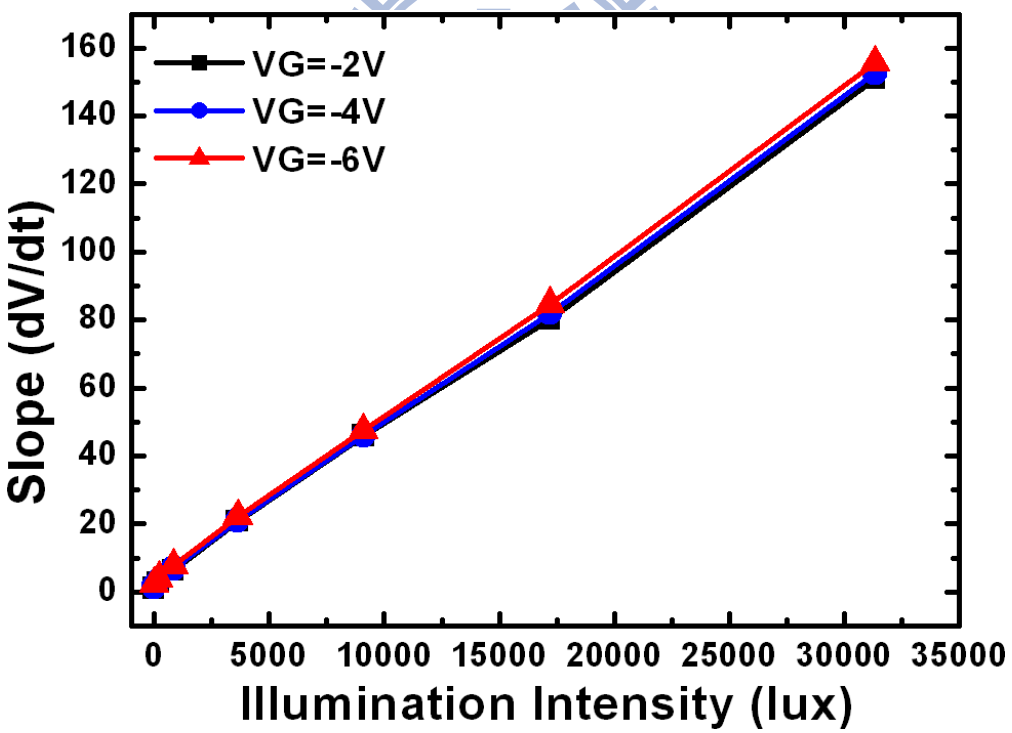


Figure 6-13 Measured output slopes of fifteen proposed light-sensing circuits in off region (dash line) and their average curve (solid line).



(a)



(b)

Figure 6-14 The influence of V_{th} shift operated on (a) subthreshold region (b) off region.

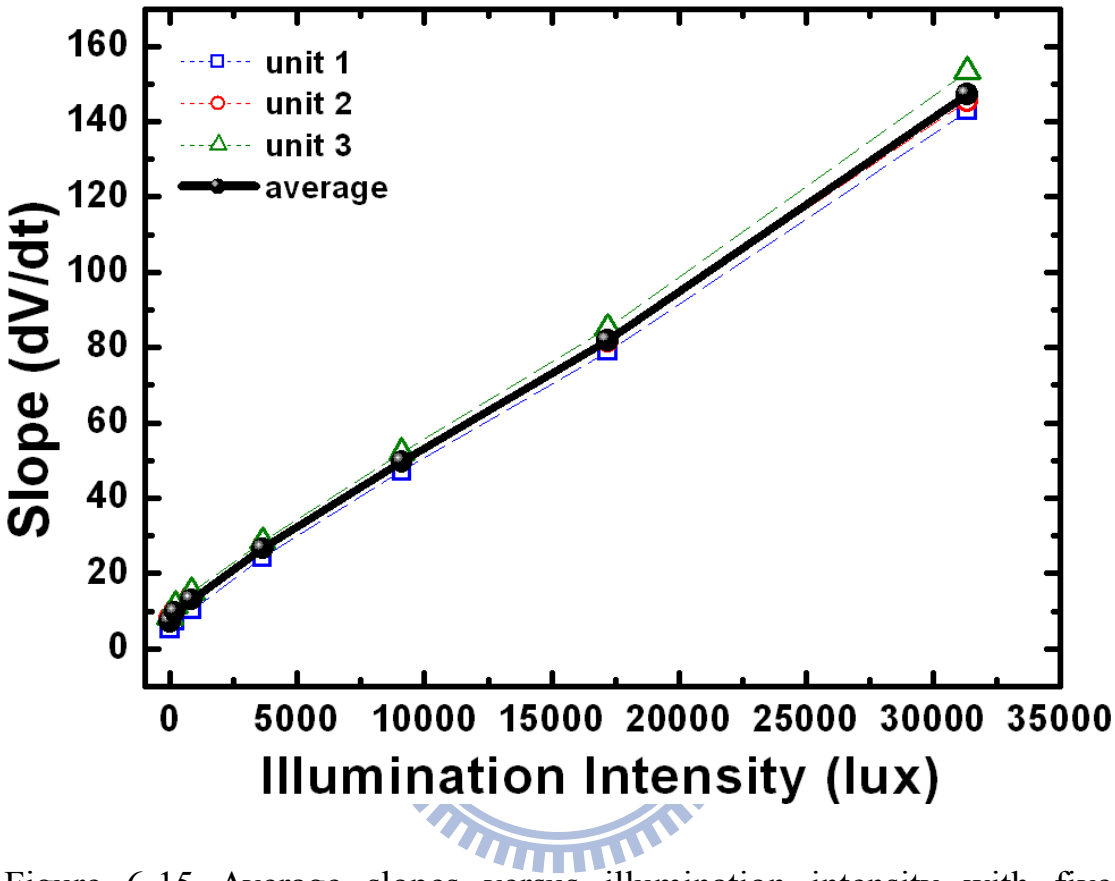


Figure 6-15 Average slopes versus illumination intensity with five samples as an average unit.

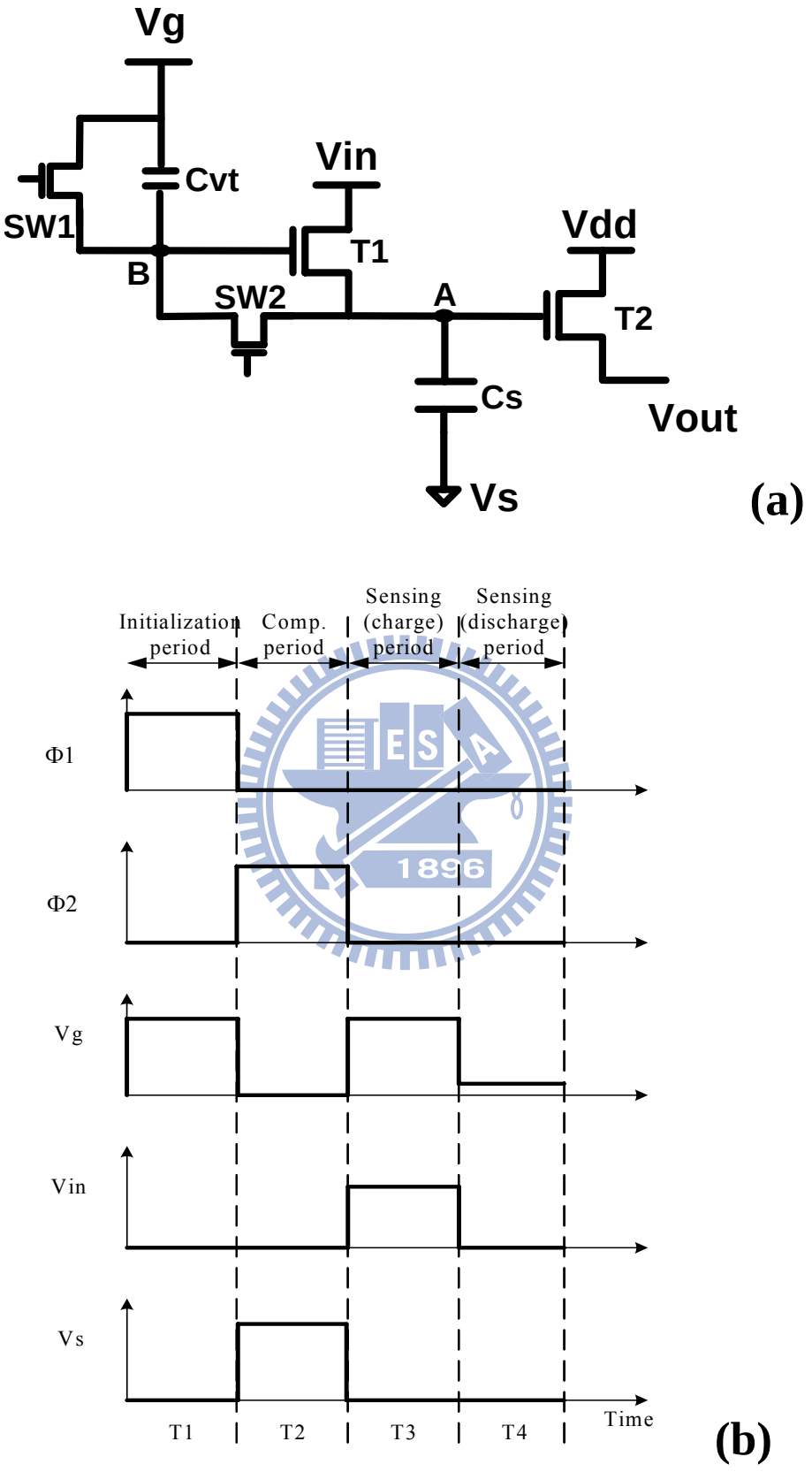
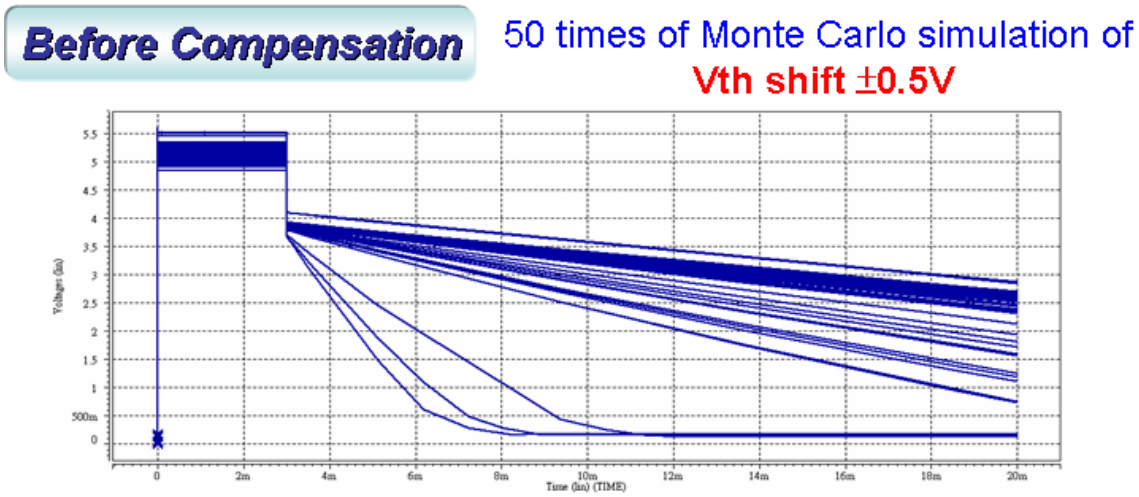
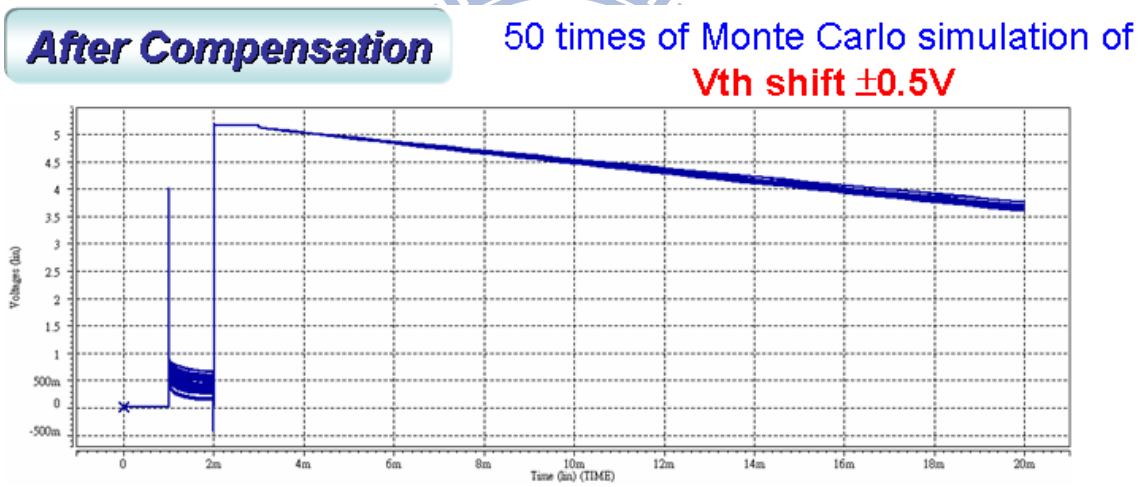


Figure 6-16 (a) Schematic of our proposed light-sensing circuit with compensation part and (b) time diagram.

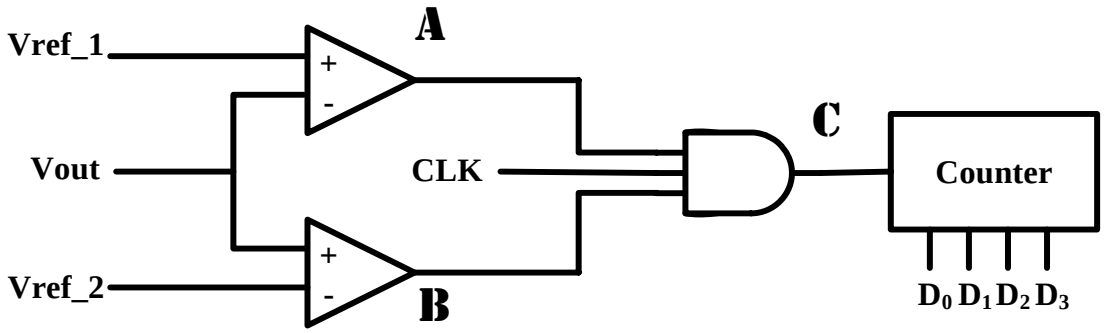


(a)

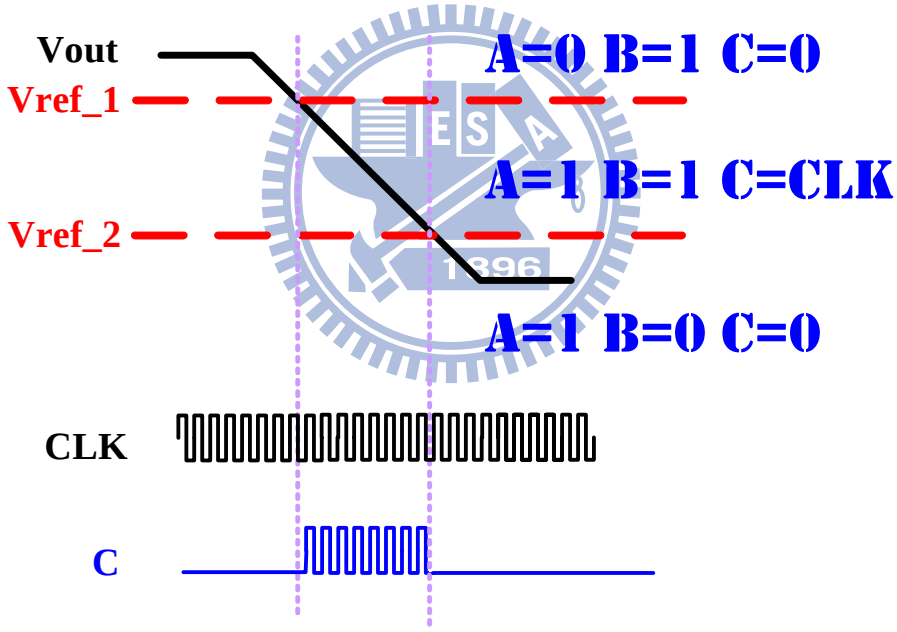


(b)

Figure 6-17 Fifty times of Monte Carlo simulation results of the proposed 2T1C light-sensing circuit when V_{th} shift is ±0.5V (a) before compensation (b) after compensation.



(a)



(b)

Fig. 6-18 (a) Simplified block diagram of digitization circuit and (b) its signal diagrams.


E S A
1896

Chapter 7

Conclusions and Suggestions for Future Work

In previous chapters, the characterizations of low-temperature poly-silicon thin film transistor for optical sensor application are studied. In chapter 3, a new photo behavior parameter Unit-Lux-Current, which is the ability of photo leakage current induced per unit-photo flux, is used to analyze the effects of illumination on LTPS TFTs. An equation is provided to properly describe ULC under various bias and temperature conditions for further exploration of photo leakage mechanism. In addition, since LTPS TFTs suffer from huge variation owing to the diverse and complicated grain distribution in the poly-Si film, the ULC variation will also be discussed. A possible future work which may try to insert such photo equations in SPICE models for design.

In chapter 4, the probable degradation cases for the device under DC operation are considered. We apply both stress conditions which are hot carrier and self heating stress deliberately to manipulate the defect-related photo behaviors and modify ULC equations in LTPS TFTs. Comparatively, this work focused on how additional non-uniform defects and the photo leakage mechanism influence both lateral and gate-drain overlap depletion. For the viewpoint of future application, the empirical adjusted equation of ULC also meanwhile provides a potential modeling for simulation of LTPS TFT circuitry.

In chapter 5, in our previous studies, under back light illumination, we propose both unstressed devices which can be seen as effective medium approach and stressed devices which have additional non-uniform defects photo-induced leakage model,

comparatively. The different characteristics of front light and back light ULC are also in comparison. Meanwhile, we provide new insight which use energy level of trap defect behaviors connected with photo induced current to further make sure the existence of tail state after self heating degradation. Furthermore, a more accurate model after self-heating degradation is proposed. Due to LTPS TFTs are top gate structures, for future sensor design consideration, such photo leakage current which suffer from back light illumination are must be amend.

In chapter 6, we study on sensor application of the low-temperature poly-silicon thin film transistor. For front light illumination application, first, a three dimensional embedded optical sensor employs low temperature poly-silicon thin film transistor which used gate metal shielding by itself characteristics was proposed. The system connect with forward and reverse measurements can be used to set up sensing direction. It provides sensing disparity characteristics of adopted devices under illumination. It's expected the integration of sensing system onto the panel without extra components sensors and extra change in the fabrication process. Then a circuit of source follower type based on the LTPS TFTs which can sense the illumination condition is proposed to be used as an ambient light sensor. Some kinds of variation effect can be calibrated by statistical and compensation circuit methods. For back light illumination application, we can use the backlight sensors to detect the uniformity of light intensity. All research would provide the possibility for the light sensor array integrated in the pixels with the same device of LTPS TFTs.

References

Chapter 1:

[1.1] A. G. Lewis, D. D. Lee, and R. H. Bruce, “Polysilicon TFT circuit design and performance,” IEEE J. Solid-State Circuits, vol. 21, pp. 1833-1842, Dec. 1992.

[1.2] D. B. Thomasson and T. N. Jackson, “Fully self-aligned tri-layer a-Si: H thin-film transistors with deposited doped contact layer,” IEEE Electron Device Letter, vol.18, pp. 397-399, Aug. 1997.

[1.3] S. Zhang, C. Zhu, J. K. O. Sin, J. N. Li, and P. K. T. Mok, “Ultra-thin elevated channel poly-Si TFT technology for fully-integrated AMLCD system on glass,” IEEE Tran. Electron Devices, vol. 47, pp. 569-575, Mar. 2000.

[1.4] J. Jang, K. M. Kim, K. S. Cho, B. K. Choo, and G. Um, “An amorphous silicon triode rectifier switching device for active-matrix liquid-crystal display,” IEEE Electron Device Letter, vol. 24, pp. 78-80, Feb. 2003.

[1.5] K. Sakariya, P. Servati, and A. Nathan, “Stability analysis of current programmed a-Si:H AMOLED pixel circuits,” IEEE Tran. Electron Devices, vol. 51, pp. 584-586, Dec. 2004.

[1.6] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, “Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic,” IEEE J. Solid-State Circuits, vol. 39, pp. 2019- 2025, Sep. 2004.

[1.7] J. H. Lee, W. Nam, B. K. Kim, H. S. Choi, Y. M. Ha, and M. K. Han, “A new poly-Si TFT current-mirror pixel for active matrix organic light emitting diode,” IEEE Electron Device Letter, vol. 27, pp. 830- 833, Oct. 2006.

[1.8] J. C. Goh, H. J. Chung, and J. Jang, “A new pixel circuit for active matrix

organic light emitting diodes," IEEE Electron Device Letter, vol. 23, pp. 544-546, Sep. 2002.

[1.9] S. H. Jung, W. J. Nam, and M. K. Han, "A new voltage-modulated AMOLED pixel design compensating for threshold voltage variation in poly-Si TFTs," IEEE Electron Device Letter, vol. 25, pp. 690- 692, Oct. 2004.

[1.10] G. A. Bhat, Z. Jin, H. S. Kwok, and M. Wong, "Effects of longitudinal grain boundaries on the performance of MILC-TFT's," IEEE Electron Device Letter, vol. 20, pp. 97- 99, Feb. 1999.

[1.11] H. L. Chen and C. Y. Wu, "An analytical grain-barrier height model and its characterization for intrinsic poly-Si thin-film transistor," IEEE Tran. Electron Devices, vol.45, pp. 2245-2247, Oct. 1998.

[1.12] T. S. Li and P. S. Lin, "On the pseudo-subthreshold characteristics of polycrystalline-silicon thin-film transistors with large grain size," IEEE Electron Device Letter, vol. 14, pp. 240-242, May 1993.

[1.13] J. I. Ohwada, M. Takabatake, Y. A. Ono, A. Mimura, and K. Ono, "Peripheral circuit integrated poly-Si TFT LCD with gray scale representation," IEEE Tran. Electron Devices, vol.36, pp. 1923-1928, Sep. 1989.

[1.14] Y. H. Tai, C. C. Pai, B. T. Chen, and H. C. Cheng, "A source-follower type analog buffer using poly-Si TFTs with large design windows," IEEE Electron Device Letter, vol. 26, pp. 811- 813, Nov. 2005.

[1.15] J. H. Jeon, M. C. Lee, K. C. Park, and M. K. Han, "A new polycrystalline silicon TFT with a single grain boundary in the channel," IEEE Electron Device Letter, vol. 22, pp. 429-431, Sep. 2001.

[1.16] C. H. Oh and M. Matsumura, "A proposed single grain-boundary thin-film transistor," IEEE Electron Device Letter, vol. 22, pp. 20-22, Jan. 2001.

Chapter 3:

[3.1] Y. H. Tai, C. C. Pai, B. T. Chen, and H. C. Cheng, “A source-follower type analog buffer using poly-Si TFTs with large design windows,” IEEE Electronics Letters, vol. 26, no. 11, pp. 881-813, Nov. 2005.

[3.2] F. Matsuki, K. Hashimoto, K. Sano, D. Yeates, J. R. Ayres, M. Edwards, and A.Steer, “Integrated ambient light sensor in LTPS AMLCDs,” in Proc. Society for Information Display, pp. 290-293, 2007.

[3.3] H. S. Lim and O. K. Kwon, “Ambient light sensing circuit using LTPS TFTs for auto brightness control,” in Dig. Tech. Workshop Active-Matrix Flat Panel Displays and Devices, pp. 21-24, 2006.

[3-4] S. Koide, S. Fujita, T. Ito, S. Fujikawa, and T. Matsumoto, “LTPS ambient light sensor with temperature compensation,” in Proc. Int. Display Workshop, pp. 689-690, 2006.

[3.5] M. Inoue and H. Ohshima, “LTPS Technologies for Advanced Mobile Display Applications,” in Dig. Tech. Workshop Active-Matrix Flat panel Displays, pp. 215-219, 2007

[3.6] C. Brown, H. Kato, K. Maeda, and B. Hadwen, “A CG Silicon System LCD with Optical Input Function,” in Proc. Int. Display Workshop, pp. 99-103, 2000.

[3.7] T. Eguchi, Y. Hiyoshi, E. Kanda, H. Sera, T. Ozawa, T. Miyazawa, and T. Matsumoto, “A 1300-dpi Optical Image Sensor Using an a-Si:H Photo Diode Array Driven by LTPS TFTs,” in Proc. Society for Information Display, pp. 1097-1100, 2007.

[3.8] W. Albert and W. Saraswat, “Strategy for modeling of variations due to grain size in polycrystalline thin-film transistors,” IEEE Transactions on Electron

Devices, vol. 47, no.5, pp. 1035-1043, 2000.

[3.9] G. J. Dominique, M. Sandrine, and K. Jerzy, “Photosensitivity of a-Si:H TFTs,” in SID Conference Record of the International Display Research Conference, pp. 407-410, 2001.

[3.10] T. Yamashita, T. Shima, Y. Nishizaki, M. Kimura, H. Hara, and S. Inoue, “Evaluation of Thin-Film Photodiodes and Development of Thin-Film Phototransistor,” Japan Journal of Applied Physics, vol. 47, pp. 1924-1929, Mar. 2008.

[3.11] W. J. Wu, R. H. Yao, S. H. Li, Y. F. Hu, W. L. Deng, and X. R. Zheng, “A compact model for polysilicon TFTs leakage current including the Poole-Frenkel effect,” IEEE Transactions on Electron Devices, vol. 54, no. 11, pp. 2975-2983, Nov. 2007.

[3.12] J. H. Chen, S. C. Wong, and Y. H. Wang, “An analytic three-terminal band-to-band tunneling model on GIDL in MOSFET,” IEEE Transactions on Electron Devices, vol. 48, no. 7, pp. 1400-14053, Jul. 2001.

[3.13] C. S. Chuang, T. C. Fung, B. G. Mullins, J. Kanicki, K. Nomura, T. Kamiya, H.Hosono, and H. P. Shieh, “Photosensitivity of Amorphous IGZO TFTs for Active-Matrix Flat-Panel Displays,” in Proc. Society for Information Display, pp. 1215-1218, 2008.

[3.14] J. R. Ayres, S. D. Brotherton, I. R. Clarence, and P. J. Dobson, “Photocurrents in poly-Si TFTs,” in IEEE Proceedings: Circuits, Devices and Systems, vol. 141, no. 1, pp 27-32, Feb. 1994.

[3.15] N. P. Papadopoulos, A. A. Hatzopoulos, D. K. Papakostas, C. A. Dimitriadis, and S. Siskos, “Modeling the impact of light on the performance of polycrystalline thin-film transistors at the sub-threshold region,” in

Microelectronics Journal, vol. 37, no. 11, p 1313-1320, Nov. 2006.

[3.16] A. Pecora, M. Schillizzi, G. Tallarida, G. Fortunato, C. Reita, and P. Migliorato, “Off-current in polycrystalline silicon thin film transistors: an analysis of the thermally generated component,” Solid-State Electronics, vol. 38, no. 4, pp. 845-850, Apr. 1995.

[3.17] O. Kikuo, A. Takashi, K. Nobutake, and M. Kenji, “Analysis of current-voltage characteristics of low-temperature-processed polysilicon thin-film transistors,” IEEE Transactions on Electron Devices, vol. 39, no. 4, pp. 792-802, Apr. 1992.

[3.18] O. K. B. Lui and P. Migliorato, “New generation-recombination model for device simulation including the Poole-Frenkel effect and phonon-assisted tunnelling,” Solid-State Electronics, vol. 41, no. 4, pp. 575-583, Apr. 1997.

[3.19] C. H. Kim, K. S. Sohn, and J. Jang, “Temperature dependent leakage currents in polycrystalline silicon thin film transistors,” Journal of Applied Physics, vol. 81, no. 12, p. 8084, Jun. 1997.

[3.20] G. Fortunato and P. Migliorato, “Determination of gap state density in polycrystalline silicon by field-effect conductance,” Applied Physics Letter, vol. 49, no. 16, pp. 1025-1027, Oct. 1986.

Chapter 4:

[4.1] Y. H. Tai, C. C. Pai, B. T. Chen, and H. C. Cheng, “A source-follower type analog buffer using poly-Si TFTs with large design windows,” IEEE Electronics Letters, vol. 26, no. 11, pp. 881-813, Nov. 2005.

[4.2] F. Matsuki, K. Hashimoto, K. Sano, D. Yeates, J. R. Ayres, M. Edwards, and A.Steer, “Integrated ambient light sensor in LTPS AMLCDs,” in Proc. Society for Information Display, pp. 290-293, 2007.

[4.3] H. S. Lim and O. K. Kwon, “Ambient light sensing circuit using LTPS TFTs for auto brightness control,” in Dig. Tech. Workshop Active-Matrix Flat Panel Displays and Devices, pp. 21-24, 2006.

[4.4] S. Koide, S. Fujita, T. Ito, S. Fujikawa, and T. Matsumoto, “LTPS ambient light sensor with temperature compensation,” in Proc. Int. Display Workshop, pp. 689-690, 2006.

[4.5] M. Inoue and H. Ohshima, “LTPS Technologies for Advanced Mobile Display Applications,” in Dig. Tech. Workshop Active-Matrix Flat panel Displays, pp. 215-219, 2007.

[4.6] C. Brown, H. Kato, K. Maeda, and B. Hadwen, “A CG Silicon System LCD with Optical Input Function,” in Proc. Int. Display Workshop, pp. 99-103, 2000.

[4.7] T. Eguchi, Y. Hiyoshi, E. Kanda, H. Sera, T. Ozawa, T. Miyazawa, and T. Matsumoto, “A 1300-dpi Optical Image Sensor Using an a-Si:H Photo Diode Array Driven by LTPS TFTs,” in Proc. Society for Information Display, pp. 1097-1100, 2007.

[4.8] T. T. Fuyuki, K. Kitajima, H. Yano, T. Hatayama, Y. Uraoka,S. Hashimoto, Y. Morita, “Thermal degradation of low temperature poly-Si TFT,” Thin Solid

Films, vol. 487, pp.216-220, 2005.

[4.9] Y. H. Tai, S. C. Huang, C. W. Lin, and H. L. Chiu, “Degradation of the capacitance voltage behaviors of the low-temperature polysilicon TFTs under DC stress,” Journal of the Electrochemical Society, vol. 154, no. 7, pp 611-618, 2007.

[4.10] Y. Uraoka, K. Kitajima, H. Yano, T. Hatayama, T. Fuyuki, S. Hashimoto, and Y. Morita, “Degradation of Low Temperature Poly-Si TFTs by Joule Heating,” IEIC Technical Report (Institute of Electronics, Information and Communication Engineers), vol. 104, no 510, pp. 71-76, 2004.

[4.11] S. Inoue, H. Ohshima, and T. Shimoda, “Analysis of Degradation Phenomenon Caused by Self-Heating in Low Temperature Processed Polycrystalline Silicon Thin Film Transistors,” Jpn. J. Appl. Phys. vol. 41, pp. 6313–6319, 2002.

[4.12] Y. H. Tai, Y. F. Kuo, and Y. H. Lee, “Photosensitivity Analysis of Low Temperature Poly-Si Thin Film Transistor Based on the Unit-Lux-Current,” IEEE Transactions on Electron Devices, vol. 56, no. 1, pp. 50-56, Jan. 2009.

[4.13] W. J. Wu, R. H. Yao, S. H. Li, Y. F. Hu, W. L. Deng, and X. R. Zheng, “A compact model for polysilicon TFTs leakage current including the Poole-Frenkel effect,” IEEE Transactions on Electron Devices, vol. 54, no. 11, pp. 2975-2983, Nov 2007.

[4.14] Y. H. Tai, Y. F. Kuo, and Y. H. Lee, “Dependence of Photosensitive Effect on the Defects Created by DC Stress for LTPS TFTs,” IEEE Electronics Letters, vol. 29, no. 12, pp. 1322-1324, Dec. 2008.

[4.15] J. H. Chen, S. C. Wong, and Y. H. Wang, “An analytic three-terminal band-to-band tunneling model on GIDL in MOSFET,” IEEE Transactions on

Electron Devices, vol. 48, no. 7, pp. 1400-14053, Jul. 2001.

[4.16] C. S. Chuang, T. C. Fung, B. G. Mullins, J. Kanicki, K. Nomura, T. Kamiya, H. Hosono, and H. P. Shieh, “Photosensitivity of Amorphous IGZO TFTs for Active-Matrix Flat-Panel Displays,” in Proc. Society for Information Display, pp. 1215-1218, 2008.

[4.17] J. R. Ayres, S. D. Brotherton, I. R. Clarence, and P. J. Dobson, “Photocurrents in poly-Si TFTs,” in IEEE Proceedings: Circuits, Devices and Systems, vol. 141, no. 1, pp 27-32, Feb. 1994.

[4.18] N. P. Papadopoulos, A. A. Hatzopoulos, D. K. Papakostas, C. A. Dimitriadis, and S. Siskos, “Modeling the impact of light on the performance of polycrystalline thin-film transistors at the sub-threshold region,” in Microelectronics Journal, vol. 37, no. 11, p 1313-1320, Nov. 2006..

[4.19] C. H. Kim, K. S. Sohn, and J. Jang, “Temperature dependent leakage currents in polycrystalline silicon thin film transistors,” Journal of Applied Physics, vol. 81, no. 12, p. 8084, Jun. 1997.

[4.20] G. Fortunato and P. Migliorato, “Determination of gap state density in polycrystalline silicon by field-effect conductance,” Applied Physics Letter, vol. 49, no. 16, pp. 1025-1027, Oct. 1986.

[4.21] O. K. B. Lui and P. Migliorato, “New generation-recombination model for device simulation including the Poole-Frenkel effect and phonon-assisted tunnelling,” Solid-State Electronics, vol. 41, no. 4, pp. 575-583, Apr. 1997.

Chapter 5:

[5.1] S. W. B. Tam and T. Shimoda, “Modelling and design of polysilicon drive circuits for OLED Displays,” in Proc. Society for Information Display, pp. 1406-1409, 2004.

[5.2] T. Serikawa, S. Shirai, A Okamoto, and S. Suyama, “Low-temperature fabrication of high-mobility poly-Si TFTs for large-area LCDs,” IEEE Transactions on Electron Devices, vol.36, pp. 1929-1933, Sep. 1989.

[5.3] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, and S. Nakano, “High mobility poly-Si TFT by a new excimer laser annealing method for large area electronics,” in IEDM Tech. Dig., pp. 563-566, 1991.

[5.4] S. I. Hsieh, H. T. Chen, Y. C. Chen, C. L. Chen, and Y. C. King, “MONOS memory in sequential laterally solidified low-temperature poly-Si TFTs,” IEEE Electron Device Letter, vol. 27, pp. 272- 274, Apr. 2006.

[5.5] S. J. Jang, Y. H. Seo, S. J. Baek, S. R. Lee, H. J. Yun, S. H. Ihm, K. H. Lee, and J. Y. Lee, “The superior readability and ultra low power consumption of mAFFS LCD by the new design,” in Proc. Society for Information Display, pp. 744-747, 2006.

[5.6] K. H. Lee, H. Y. Kim, K. H. Park, S. J. Jang, I. C. Park, and J. Y Lee, “A novel outdoor readability of portable TFT-LCD with AFFS technology,” in Proc. Society for Information Display, 2006, pp. 1079-1082.

[5.7] D. N. Yaung, Y. K. Fang, C. H. Chen, C. C. Hung, F. C. Tsao, S. G. Wuu, and M. S. Liang, “To suppress photoexcited current of hydrogenated polysilicon TFTs with low temperature oxidation of poly channel,” IEEE Electron Device Letter, vol. 22, pp. 21- 23, Jan. 2001.

[5.8] K. Kobayashi and Y. Niwano, “Photo-leakage current of poly-Si thin film transistors with offset and lightly doped drain structure,” Jpn. J. Appl. Phys., Part 1, vol. 39, pp. 5757-5761, 1999.

[5.9] K. Suzuki, F. Takeuchi, Y. Ebiko, M. Chida, and N. Sasaki, “Analytical photo leak current model of low-temperature CW laser lateral crystallization (CLC) poly-Si TFTs,” in IEDM Tech. Dig., pp. 785-788, 2004.

[5.10] J. R. Ayres, S. D. Brotherton, I. R. Clarenee, and P. J. Dobson, “Photocurrents in poly-Si TFTs,” Inst. Elec. Eng. Proc. Circuits Devices Syst., vol. 141, pp. 27–32, 1994.

[5.11] Y. Laghla, E. Scheid, H. Vergnes, and J. P. Couderc, “Electronic properties and microstructure of undoped, and B- or P-doped polysilicon deposited by LPCVD,” Solar Energy Materials and Solar Cells, vol. 48, pp. 303–314, 1997.

Chapter 6:

[6.1] Dr Nick Holliman,“3D Display System,” Department of Computer Science, University of Durham, Science Laboratories, South Road, Durham, DH1 3QJ. November 8, 2002.

[6.2] F. Matsuki, K. Hashimoto, K. Sano, D. Yeates, J. R. Ayres, M. Edwards, and A.Steer, “Integrated Ambient Light Sensor in LTPS AMLCDs,” in Proc. Society for Information Display, pp. 290-293, 2007.

[6.3] H. S. Lim and O. K. Kwon, “Ambient light sensing circuit using LTPS TFTs for auto brightness control,” in Dig. Tech. Workshop Active-Matrix Flat Panel Displays and Devices, pp. 21-24, 2006.

[6.4] T. Eguchi, Y. Hiyoshi, E. Kanda, H. Sera, T. Ozawa, T. Miyazawa, and T. Matsumoto, “A 1300-dpi Optical Image Sensor Using an a-Si:H Photo Diode Array Driven by LTPS TFTs,” in Proc. Society for Information Display, pp. 1097-1100, 2007.

[6.5] T. W. Pai, G. Z. Wang, Y. P. Huang, H. P. Shieh, and J. M. Hung, “3D Interaction Display with Embedded Optical Sensors,” in Proc. Society for Information Display, pp. 1967-1970, 2008.

[6.6] F. Matsuki, K. Hashimoto, K. Sano, D. Yeates, J. R. Ayres, M. Edwards, and A. Steer, “Integrated Ambient Light Sensor in LTPS AMLCDs,” in Proc. Society for Information Display, pp.290-293, 2007.

[6.7] G. Y. Yang, Y. G. Kim, T. S. Kim, and J. T. Kong, “S-TFT: An Analytical Model of Polysilicon Thin-Film Transistors for Circuit Simulation,” IEEE Custom Integrated Circuits Conference, pp.213-316, 2000.

[6.8] Y. Kitahara, S. Toriyama, and N. Sano, “A New Grain Boundary Model for Drift-Diffusion Device Simulations in Polycrystalline Silicon Thin-Film

Transistors,” Jpn. J. Appl. Phys. vol. 42, no. 6, pp.634-636, 2003

[6.9] C. Michael and M. Ismail, “Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits,” Amsterdam, The Netherlands: Kluwer Academic, pp.8-10, 1993.

[6.10] S. K. Hong, B. K. Kim, and Y. M. Ha, “LTPS Technology for Improving the Uniformity of AMOLEDs,” in Proc. Society for Information Display, pp.1366-1369, 2007.

[6.11] A. Nathan, G. R. Chaji, and S. J. Ashtiani, “Driving Schemes for a-Si and LTPS AMOLED Displays,” IEEE Journal of Display Technology, vol. 1, no. 2, pp.267-277, 2005.

[6.12] H. S. Lim and O. K. Kwon, “Ambient Light Sensing Circuit with Low Temperature Polycrystalline Silicon p-Intrinsic-n Diode and Source Follower for Auto Brightness Control,” Jpn. J. Appl. Phys. vol. 47, no. 3, pp.1919-1923, 2008.

簡　歷

姓　　名：郭 彥 甫

性　　別：男

出生年月日：民國 69 年 12 月 03 日

籍　　貫：台灣省新竹縣

住　　址：新竹縣竹北市大眉里9鄰中華路1483巷9號

學　　歷：

國立中山大學物理學系學士　(88.09-92.06)

國立交通大學光電工程研究所碩士班　(92.09-94.06)

國立交通大學光電工程研究所博士班　(94.09-99.08)

博士論文題目：

低溫多晶矽薄膜電晶體元件特性應用於光感測器之研究

Study on Characterization of Low-Temperature Poly-Silicon Thin Film Transistor for Optical Sensor Application

Publication List

International Journals:

[1] Ya-Hsiang Tai and **Yan-Fu Kuo**, "Statistical study on the temperature dependence of the turn-on characteristics for p-type LTPS TFTs," Solid-State Electronics, vol.51, no.8, pp.1092-1095, 2007.

[2] Ya-Hsiang Tai, **Yan-Fu Kuo**, and Yun-Hsiang Lee, "Dependence of Photosensitive Effect on the Defects Created by DC Stress for LTPS TFTs," IEEE Electron Device Letters, vol. 29, no. 12, pp. 1322-1324, Dec. 2008.

[3] Ya-Hsiang Tai, **Yan-Fu Kuo**, and Yun-Hsiang Lee, "Photosensitivity Analysis of Low Temperature Poly-Si Thin Film Transistor Based on the Unit-Lux-Current," IEEE Transactions on Electron Devices, vol 56, no 1, pp. 50-56, Jan 2009.

[4] Ya-Hsiang Tai, **Yan-Fu Kuo**, Guo-Pei Sun, "An Empirical Defect-Related Photo Leakage Current Model for LTPS TFTs Based on the Unit-Lux-Current," IEEE Transactions on Electron Devices, vol. 57, no. 5, pp. 1015- 1022, 2010.

[5] Ya-Hsiang Tai, **Yan-Fu Kuo,** Shao-Wen Yen, "Gap-type a-Si TFTs for Backlight Sensing Application," submitted to IEEE Journal of Display Technology.

[6] Ya-Hsiang Tai, **Yan-Fu Kuo**, Chih-Jung Lin, "Photo Induced Current Analysis of Extra Defect Distribution under Electrical Stress in LTPS TFTs," submitted to Electrochemical and Solid-State Letters.

International Conferences:

[1] **Yan-Fu Kuo** and Ya-Hsiang Tai, "Statistical Study on the Temperature

Dependence of the Turn-On Characteristics for p-Type LTPS TFTs," LOES, Sydney, Australia, 2005.

[2] **Yan-Fu Kuo**, Shih-Che Huang, Wei-Lun Shih, Ya-Hsiang Tai, "Dynamic stress effects on the reliability of Poly-Si TFT," International Display Manufacturing Conference and Exhibition (IDMC) pp.497-499, 2007.

[3] **Yan-Fu Kuo**, Shih-Che Huang, Yu-Te Chao, Ya-Hsiang Tai, "Capacitance Voltage Behaviors of the LTPS TFTs Before and After DC Stress Explained by the Slicing Model," International Display Manufacturing Conference and Exhibition (IDMC) pp.523-525, 2007.

[4] **Yan-Fu Kuo**, Teng-Jui Yu, Shao-Wen Yen, Ya-Hsiang Tai, "A Novel Self-Modulated Amorphous Front and Back Light Sensors System with Wide Dynamic Range for Active Matrix Displays," in Proc. Society for Information Display, 2009.

[5] **Yan-Fu Kuo**, Teng-Jui Yu, Shao-Wen Yen, Ya-Hsiang Tai, "Using Low Temperature Poly-Silicon Thin Film Transistor as oblique light sensors for 3D interaction display," in Proc. Society for Information Display, 2010.