應用於無線通訊系統之互補式金氧半雙正交接收機前置電路設計與分析

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摘要

本篇論文分別闡述兩個雙正交射頻接收機前置電路的設計方法及製作技術；兩個接收機中，一個根據國際電子電機學會所制訂的802.11a 規格做設計，另一個則針對低電壓的應用做設計。論文中包含下列三個部分：(1)主動式多相位濾波器的模型建立、設計方法與性能分析；(2)適用於 IEEE 802.11a 無線區域網路規格之雙正交接收機前置電路的設計方法與性能分析；(3)適用於低電壓應用之 1-V 2.4-GHz 雙正交接收機前置電路的設計方法與性能分析。

首先，本論文提出一個新的方法來實現互補式金氧半多相位濾波器。在單級的多相位濾波器設計中，由流經電容及電晶體的電流特性來分別實現高通及低通的功能，再經由多級的串連後，頻寬可延展至20MHz，除此之外，使用一個定轉導的偏壓電路，將可使此多相位濾波器的性能免於受到製程及溫度變化的影響，整個電路的性能可以經由HSPICE的模擬得到驗證。另外，藉由相似電流操作的特性，此電路可經由簡單的修改而操作在 1 伏特的電壓下，功率消耗也可再減為一半。經由上面所述的方法，一個四級的多相位濾波器採用了 0.25 微米的互補式金氧半製程來製作。由量測的結果可知，在 6.1MHz至30MHz的頻寬中，其對鏡像抑制比可達到 48dB，在頻率為 20MHz時電壓增益為 6.6dB，輸入端三諧交越點為 8dBm，在 2.5V的工作電壓下，其功率消耗為 11mW，晶片面積為 1162×813μm^2。

其次，本論文提出了一個可適用於IEEE 802.11a無線區域網路規

格之互補式金氧半雙正交接收機前置電路。此接收機前置電路整合了低雜訊放大器、射頻正交訊號產生器、雙正交混波器、正交壓控振盪器及主動式多相位濾波器。接收機中使用了一個單級的RLC相位轉移電路來產生所需的射頻正交訊號，雙正交混波器與正交壓控振盪器被融合在一起以達到重複使用電流的目的，而上段所述的四級多相位濾波器則被使用來濾除鏡像訊號，此接收機提供了低功率消耗、小面積及對寄生元件低靈敏度的優點。接收機採用了 0.18 微米的互補式金氧半製程來製作。量測結果顯示此接收機的雜訊指數為 8.5dB，頻寬內的增益為 16dB，最小鏡像抑制比為 50.6dB，輸入端三諧交越點為 -13dBm，在 1.8V的工作電壓下，其功率消耗為 22.4mW，晶片面積為 2×1.5mm^2。

最後，本論文提出了一個適用於低電壓應用之 1-V 2.4-GHz雙正交接收機前置電路。此接收機前置電路整合了低雜訊放大器、射頻正交訊號產生器、雙正交混波器、正交壓控振盪器及主動式多相位濾波器。在所設計的新低雜訊放大器中使用了並聯的電感電容電路來抑制同相位訊號，此電路在所需的頻率提供了高阻抗並且幾乎不佔用直流電壓，這些優點使它非常適用於低電壓的設計。在射頻正交訊號產生器的設計中除了使用一個新的單級RLC相位轉移電路，還利用交錯連接的電晶體來產生負轉導以提高輸出阻抗，如此可以提高射頻正交訊號產生器的增益並減少功率消耗。接收機採用了 0.25 微米的互補式金氧半製程來製作。量測結果顯示低雜訊放大器的雜訊指數及同相訊號抑制比分別為 5.5dB及 29dB。在 2.43GHz至 2.48GHz的頻率範圍內，接收機的最小鏡像抑制比為 30.2dB，在頻率為 2.42GHz時的電壓增益為 12dB，輸入端三諧交越點為-12dBm，壓控振盪器的頻率可調範圍為 400MHz，在 1-V的工作電壓下，其功率消耗為 34.6mW，晶片面積為 1.8×1.6mm^2。

經由模擬及量測的結果證實，本論文所提出的兩個雙正交接收機前置電路將可適用於一個全互補式金氧半電晶體的無線通訊系統中。如此將可實現一個高性能、高頻率、低功率及高整合度的行動通訊裝備。在未來將針對其他的射頻元件做整合而成為一個完整的收發器。

THE DESIGN AND ANALYSIS OF CMOS DOUBLE-QUADRATURE RECEIVER FRONT-ENDS FOR WIRELESS COMMUNICATION SYSTEMS

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ABSTRACT

In this thesis, the design methodologies and implementation techniques of two double quadrature receiver front-ends for 5-GHz IEEE 802.11a wireless local area network (IEEE 802.11a wireless LAN) and low-voltage applications are presented. There are three parts in this thesis, including (1) the modeling, design, and analysis of the active polyphase filter; (2) the design and analysis of a 5-GHz double-quadrature receiver front-end for IEEE 802.11a wireless LAN applications; (3) the design and analysis of a 1-V 2.4-GHz double-quadrature receiver front-end for low-voltage applications.

At first, a new technique to implement the transfer function of polyphase filter with CMOS active components is proposed and analyzed. In the proposed polyphase filter structure, currents mirrored from capacitors and the transistors in a single-stage are used to realize high-pass and low-pass functions, respectively. The four-stage structure expands the frequency bandwidth to more than 20MHz. Furthermore, a constant-gm bias circuit is employed to decrease the sensitivity of image rejection to temperature and process variations. HSPICE simulations are performed to confirm the

performances. With the current-mode operation, the low-voltage version of proposed active polyphase filters was designed. It can be operated at 1V power supply with similar performance but with only 50% of the power dissipation of the normal-voltage version. The proposed four-stage polyphase filter is fabricated in 0.25-μm CMOS 1P5M technology. The measured image rejection ratio is higher than -48dB at frequencies of 6.1MHz ~ 30MHz. The measured voltage gain is 6.6dB at 20MHz and the *IIP3* is 8dBm. The power dissipation is 11mW at a supplied voltage of 2.5V and the active chip area is 1162×813μm^2.

Secondly, a 5-GHz CMOS double-quadrature receiver front-end used for IEEE 802.11a wireless LAN is proposed. The receiver consists of a low-noise amplifier, an RF quadrature generator, double-quadrature mixers, a quadrature voltage-controlled oscillator, and an active polyphase filter. A new one-stage RLC phase shifter is employed to generate quadrature RF signals. Using the current reuse technique, double-quadrature mixers are merged with the quadrature VCO. The proposed active polyphase filter with four-stage structure is designed to reject the image signal. The receiver provides the advantages of low power dissipation, a small chip area, and a low sensitivity to parasitic components. The measured noise figure is 8.5dB and the gain in the channel bandwidth is above 16dB. The image rejection within the channel bandwidth exceeds 50.6dB and the *IIP3* is –13dBm. Implemented in 0.18-um CMOS technology, the power dissipation of the fabricated double-quadrature receiver is 22.4mW at a supplied voltage of 1.8V and a die area of 2×1.5 mm^2.

Finally, a 1-V 2.4-GHz CMOS double-quadrature receiver is proposed and analyzed. The double-quadrature receiver comprises a new low-noise amplifier, a new RF quadrature generator, a quadrature voltage-controlled oscillator, double-quadrature

mixers and an active polyphase filter. In the new 1-V low-noise amplifier, LC-tank is used to reject the common-mode signal. The LC-tank provides high impedance in the desired frequency and has almost zero dc voltage-drop. These characteristics make it suitable for high frequency and low-voltage design. A new one-stage RLC phase shifter is employed to realize the new RF quadrature generator where cross-couple transistors are used to generate a negative transconductance to decrease the output conductance and increase the load impedance. The gain of the RF quadrature generator thus can be enhanced and the power consumption can be reduced. The 1-V 2.4-GHz double-quadrature receiver is fabricated with 0.25-μm CMOS 1P5M technology. From the measurement results of the low-noise amplifier, the noise figure and common-mode rejection ratio are 5.5 dB and 29 dB, respectively. In the measurement of double-quadrature receiver, the measured image rejection ratio is higher than 30.2 dB at image frequencies of 2.43 GHz ~ 2.48 GHz. Furthermore, the measured voltage gain is 12 dB at 2.42 GHz and *IIP3* is –12 dBm. The tuning range of voltage-controlled oscillator is 400 MHz. The power dissipation of the 1-V 2.4-GHz double-quadrature receiver is 34.6 mW at a supplied voltage of 1V and the active chip area is 1.8×1.6 mm^2.

It is believed that the proposed two double-quadrature receiver front-ends can be applied to the design of high-performance high-frequency low-power high-integration all-CMOS wireless communication systems. Further research on the integration of other transceiver components will be conducted in the future.