CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Over the past decade, the growing demands for wireless personal mobile and cellular communication systems have led to a fast progress on the RF integrated circuit (IC) designs [1]-[6]. As more applications spring up, overcrowding and interference at lower frequency bands push applications toward higher operating frequencies, such as IEEE 802.11a wireless local area network (IEEE 802.11a Wireless LAN) [7] and high performance radio local area network type-2 (HIPERLAN2) [8] where the standards specify operation frequencies at the 5GHz. Besides, the next key requirement for users is the requirement for low overall system power consumption so that longer elapse time can be obtained between battery recharging. One effective technique of reducing power dissipation is to decrease supply voltage. Therefore, RF circuits capable of operating at low supply voltage have become an important consideration in the design of commercial systems. The continuing advance of CMOS technology into the nanometer regime has brought the unit-gain frequency f_T beyond several tens GHz and the threshold voltage V_{Th} lower than 0.5V [9]. It becomes feasible for ICs to operate at multiple GHz and low supply voltage with CMOS technology [10]. Thus high-performance high-frequency low-power high-integration all-CMOS implementation is one of the most attractive solutions for RF wireless communication systems in next decade.

A communication system consists of three functional blocks, namely, receiver, transmitter, and baseband processor. The receiver performs amplification, downconversion, and demodulation on the received signals. The transmitter performs modulation, upconversion, and transmission on the transmitted signals. The baseband processor performs both baseband signal processing and human-machine-interface processing. The performance of this communication system depends heavily on each of the building blocks. To achieve high performance and low power, these building blocks require a careful design based on the well-defined system parameters [11].

In this thesis, the research focuses on two CMOS double quadrature receiver front-ends. The first receiver operates at 5GHz and focuses on IEEE 802.11a wireless LAN standard. The second receiver operates at 2.4GHz and focuses on low-voltage applications. Several receiver architectures will be briefly reviewed in the following sections.

1.2 REVIEW ON ARCHITECTURES OF CMOS WIRELESS RECEIVER

1.2.1 Heterodyne Receiver

The heterodyne receiver [14], which is shown in Fig. 1.1, can be divided to two stages. The first stage consists of a low-noise amplifier *LNA*, an RF image-reject filter BPF_{RF}, an RF mixer $MIXER_{RF}$, and an RF VCO VCO_{RF}, The second stage consists of a channel-select filter BPF_{IF}, two IF mixers $MIXER_{IF}$, and two low-pass filter LPF_{BB}. BPF_{RF} is usually an off-chip surface acoustic wave (SAW) filter.

In the heterodyne receiver, the incoming signals are amplified by the *LNA* first

and the image signals are rejected by the second component BPF_{RF}. The reserved RF signals after the BPF_{RF} is shifted to an IF signal by the $MIXER_{RF}$ and then pass through the BPF_{IF} to remove the adjacent interferers. Finally, the channel-selected signal is demodulated into I and Q signals in baseband and the unwanted tones produced by non-linearity and high frequency noises are filtered by the LPF_{BB}. Since the intermediate frequency is a design parameter, the IF can be chosen to optimize the selectivity, signal gain, and noise figure.

In the frequency translation, both the desired signal and the image signal are mapped to the IF frequency after mixing. Although the BPF_{RF} is used to attenuate the image signal, suitable attenuation of the image may not be practical unless the IF frequency is relatively high. The trade-off is that filtering at a high IF requires more complicated filters in order to maintain selectivity. Besides, it is difficult to implement an on-chip, high-Q filter at the RF frequency. The required high-Q, high frequency band-pass filter BPF_{RF} is therefore place off-chip, thus the integrated ability of the heterodyne receiver is limited and the cost is increased. The buffer to drive the off-chip filter also consumes high power and reduces the gain of the heterodyne receiver.

1.2.2 Direct-Conversion (Homodyne, Zero-IF) Receiver

The direct-conversion receiver [18]-[22] is highly integratable. As seen from Fig. 1.2, the BPF_{RF} and IF components in the heterodyne receiver are not required in the direct-conversion receiver, this avoids the difficult to integrate.

In a direct-conversion receiver, the RF signal is mixed with a local oscillator at the carrier frequency, i.e. the frequency translation is done in a single step. Since the

IF frequency is zero, only two low-pass filters LPF_{BB} in the I/Q paths is needed to select the desired signal. Ideally there is no image frequency, and no image signals will corrupt the desired signal.

Problems in the direct-conversion receiver implementations are local oscillator leakage (LO leakage), flicker noise, and DC offsets [23]. The LO leakage may effect the sensitivity of the front-end circuits via coupling to the substrate or via the non-ideally reverse isolation of the front-end blocks. The finite reverse isolation allows the LO leakage to couple to the antenna and the radiated LO power can affect nearby receivers. At the frequency below 1MHz, the flicker noise is the dominant noise source. The flicker noise shall be considered in designing the direct-conversion receiver because the RF signal is translated to baseband directly. MOS device with large dimension can be chosen to reduce the flicker noise. Besides, the flicker noise in a PMOS is less than that in a NMOS.

DC offsets are the most significant problem in the direct-conversion receiver because the magnitudes of DC offsets are time varying and cannot be predicted. Two sources of DC offsets are shown in Fig. 1.3. As seen from Fig. 1.3, the first source is the LO leaking to the RF input then reflecting from the antenna and mixing with itself at the $MIXER_{RF}$. The second source is the large nearby interferers leaking into the VCO_{RF} and then self-mixing. The DC levels may be removed by capacitive coupling, but the signal power near DC will be lost. To reduce the signal loss, the size of used capacitors should be large enough. Some techniques using feedback loops from the baseband or the digital part are proposed to reduce effects of DC offsets, but these methods add complexities to the receiver design.

1.2.3 Image-Reject Receiver

The primary advantage of the image rejection receivers [24]-[28] is that they do not need image-reject filters. Without the image-reject filters, the IF frequency can be placed very low to reduce the design difficulty of the IF channel-select filter. Hartley [29] and Weaver [30] receivers are two traditional and common used receivers for image rejection.

Fig. 1.4 shows the block diagram and spectral flow of the Hartley receiver. As seen from Fig. 1.4, the desired signal and the image interferer are downconverted in both upper and lower paths. However, the desired signals at points *B* and *C* are in-phase, while the image interferers are 180^{o} out of phase. When the spectrum at points *B* and *C* are combined, the image interferer will be cancelled and the desired signal will be left.

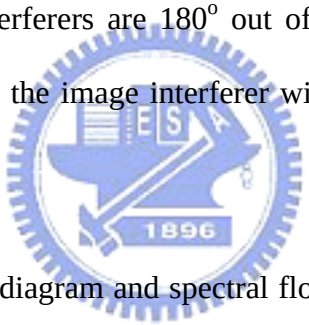


Fig. 1.5 shows the block diagram and spectral flow of the Weaver receiver. This architecture differs from the Hartley architecture in that quadrature mixers $MIXER_{IF}$ replace the 90^{o} phase shifter in the signal path. The purpose of this replacement is to perform phase shifting not on the signal path, but on the second local oscillator VCO_{IF}, which is just a single sinusoidal tone. Therefore, phase shifting accuracy can be better control.

The image rejection ratio (*IRR*) of the Hartley and Weaver topologies is limited by mismatches in branch gain, phase inaccuracy of the quadrature oscillator, and imperfect quadrature phase shifting. The *IRR* can be expected by (1.1)

$$IRR = \frac{1+(1+\varepsilon)^2 - 2(1+\varepsilon)\cos(\theta)}{1+(1+\varepsilon)^2 + 2(1+\varepsilon)\cos(\theta)} \quad (1.1)$$

where ε and θ are the gain mismatch and phase imbalance, respectively. For ε=5% and θ= 5^o the *IRR* is 26dB. Existing implementations of image rejection receivers typically achieve 30~40dB of image rejection.

1.2.4 Wideband-IF Receiver

The wideband-IF receiver [31][32] shown in Fig. 1.6 is similar to a combination of the heterodyne receiver technique and weaver image rejection.

In the heterodyne architecture, the receiver mixes the incoming RF signal with a tunable RF local oscillator and translates the desired signal to a fixed intermediate frequency. Therefore, the channel selecting is performed using RF local oscillator. The wideband-IF receiver instead uses a fixed local oscillator at the first mixing stage, the entire band of channel frequencies is translated to the fixed intermediate frequency. The second set of tunable IF local oscillators is used to select the desired channel from the band and translate it to baseband, while simultaneously rejecting the image frequencies.

Since the RF local oscillator operates at fixed-frequency oscillator, the phase noise performance of the oscillator can be optimized for the intended frequency of operation. Besides, it is possible to design the IF local oscillator with a low phase noise because it operates at a relatively low frequency. The disadvantage of the wideband-IF receiver is that all adjacent channel blocking signals are translated to baseband without filtering. Considering the linearity requirement, most of the receiver gain is therefore applied at baseband. Leaving the gain to the baseband section may

increase the noise figure of the receiver. Besides, images still interfere the desire signal for mismatches in I/Q paths at the first stage. An off-chip RF filter is required for high image rejection ratio.

1.2.5 Low-IF Receiver

The low-IF receiver [33]-[37] is shown in Fig. 1.7. Low-IF receiver combines advantages of heterodyne and direct-conversion receivers. The desired RF signals are brought close to a low intermediate frequency in a single step, which is similar to the downconversion in the direct-conversion receiver. Since the intermediate frequency is higher than DC so that DC offsets and flicker noises do not affect the desired signal. In the low-IF receiver, polyphase filters are used to filter the image so the high-Q image-reject filter is not required. Therefore, the low-IF receiver is more integratable than the heterodyne receiver because polyphase filters are operated at low intermediate frequency and can be realized on-chip.

The *IRR* of the low-IF receiver is limited by mismatches in branch gain, phase and amplitude inaccuracy of the quadrature oscillator. Fig. 1.8 shows the spectral flow in the low-IF receiver. $SIGp_{RF}$, $SIGn_{RF}$, IMp_{RF} and IMn_{RF} in Fig. 1.8 refer to the received spectrum of the desired signals and the image signals. *LOp*, *LOn* refer to the spectrum of the quadrature local oscillation signal and its crosstalk image signal. After the frequency translation, the $SIGp_{RF}$, $SIGn_{RF}$, IMp_{RF} and IMn_{RF} are downconverted to $SIGn_{IF}$, $SIGp_{IF}$, IMp_{IF} and IMn_{IF}, respectively. The image IMp_{IF} mixes with $SIGp_{IF}$ at ω_{IF} and cannot be removed by the following polyphase filters. Since mismatches in RF circuits are inevitable even in modern IC process, to achieve a high *IRR* without special techniques is not possible for the low-IF receiver.

1.2.6 Double-Quadrature Receiver

To improve the *IRR*, a modified structure name double-quadrature receiver [38]-[40] is used in this thesis. The double-quadrature receiver shifts the phase of RF signal to quadrature and then the quadrature RF signals are downconverted to IF signals by mixing with quadrature local oscillation signals. The double-quadrature receiver is less sensitivity to the I/Q unbalance of LO signals because the RF and LO signals are both put into quadrature phases. Since the RF signals are down-converted to intermediate frequency, it is also immunity from DC offset and flicker noise problems. The model of double-quadrature receiver and circuit realizations will be described in Chapter 3 and Chapter 4.

Table 1.1 lists the comparisons of receiver architecture. The heterodyne receiver can achieve the best performance because it is immunity from I/Q mismatch, DC offset and flicker noise problems. The expenses for high performance in the heterodyne receiver are high power consumption and poor integration ability. Direct-conversion receiver has the high integration and low power consumption characteristics. But high performance is difficult to achieve for the DC offset and flicker noise problems. Image-rejection, wideband-IF, and Low-IF receivers achieve better performance than direct-conversion receiver, but the unbalanced LO signals will limit the image rejection performance. Therefore, an off-chip high-Q RF filter is still required before the receiver for high image rejection ability.

The double-quadrature receiver down-converts the RF signal to intermediate frequency so it will not affected by DC offset and flicker noise. Since the RF is put into quadrature phases, the double-quadrature receiver becomes less sensitivity to the

I/Q unbalance and the off-chip high-Q RF filter is not required. To achieve a low power, high-performance, high-integration receiver for wireless communication applications, the double-quadrature architecture is chosen in this design.

1.3 ORGANIZATION OF THIS THESIS

It is the aim of this thesis to design two double-quadrature receiver front-ends, the first receiver operates at 5GHz with normal-voltage 1.8V and the second receiver operates at 2.4GHz with low supply voltage 1V. Both double quadrature receivers are fully integrated with CMOS process. The main components in the receivers include a low-noise amplifier, a RF quadrature generator, double-quadrature mixers, a quadrature voltage-controlled oscillator and a multi-stage polyphase filter.

In Chapter 2, a new broadband CMOS active polyphase filter with a wide range of operating frequencies is proposed and designed. The model of the active polyphase filter is used to analyze the mismatch effects. A constant-gm bias circuit is used to decrease the sensitivities of the filter gain and the bandwidth to temperature and process variations. The multi-stage approach commonly used in the passive RC polyphase filter is also applied to achieve the wide bandwidth. Due to the high input impedance in each stage, the proposed active polyphase filter can avoid the gain degradation between pairs of stages when connected in cascade. Thus, power-consuming buffers are not required and the required power in the proposed multi-stage active polyphase filter is reduced significantly. The design methodology for the proposed active polyphase filter is given. HSPICE simulation is performed to verify the functions of the circuits. Finally, the experimental results are summarized.

In Chapter 3, a 5-GHz CMOS receiver front-end used for IEEE 802.11a wireless

LAN is proposed. Double-quadrature architecture is used to improve the image rejection performance. The model of the double-quadrature architecture and the analysis for the image rejection performance of double-quadrature receiver are described. In the circuit realizations, a new single-stage frequency-adjustable RLC phase shifter circuit is used to realize the RF quadrature generator. The single-stage quadrature generator can generate accurate quadrature signals without high power consumption and noise figure degradation. A current reuse technique by merging the double-quadrature mixers with the quadrature voltage-controlled oscillator is used in this design. Finally, the proposed multi-stage active polyphase filter is used to reject the image.

In this chapter, the operations of the IEEE 802.11a wireless LAN are presented and the required design parameters are calculated from the standard. HSPICE and SpectreRF simulations are performed to verify the performances of the double-quadrature receiver and the experimental results are summarized.

In Chapter 4, a double-quadrature receiver front-end that operates at 1-V supply voltage is designed and analyzed in 0.25-um CMOS technology. In the circuit realization, an LC-tank working as a source degenerator is used in the low-noise amplifier to suppress common-mode signals. The LC-tank provides high impedance for common-mode signal in the desired RF range. Almost zero dc voltage-drop makes LC-tank suitable for low-voltage low-noise amplifier to improve the common-mode rejection ability. A new RLC phase shifter circuit is used to realize the RF quadrature generator. Compared to the RLC phase shifter in Chapter 3, the new RF quadrature generator has less sensitive to resistance variation. Besides, cross-couple transistors are added to increase the load impedance to enhance the gain and thus reduce the

power consumption. To increase the voltage headroom in double-quadrature mixers and the quadrature voltage-controlled oscillator, the current reuse technique is not used herein. In Chapter 5, conclusions and future work are given.

Table 1.1 Comparison of receiver architectures

	Heterodyne	Direct-Conversion	Image-Rejection	Wideband-IF	Low-IF	Double-Quadrature
Performance	Good	Poor	Mediate	Mediate	Mediate	Mediate
DC-offset	No	Yes	No	No	No	No
1/f noise	No	Yes	No	No	No	No
Balance I/Q	Not required	Accurate	Accurate	Accurate	Accurate	Mediate
Image Rejection	Good	Not required	Mediate	Mediate	Mediate	Good
Integration ability	Poor	Good	Mediate	Mediate	Mediate	Good
Power dissipation	High	Low	Low	High	Low	Low

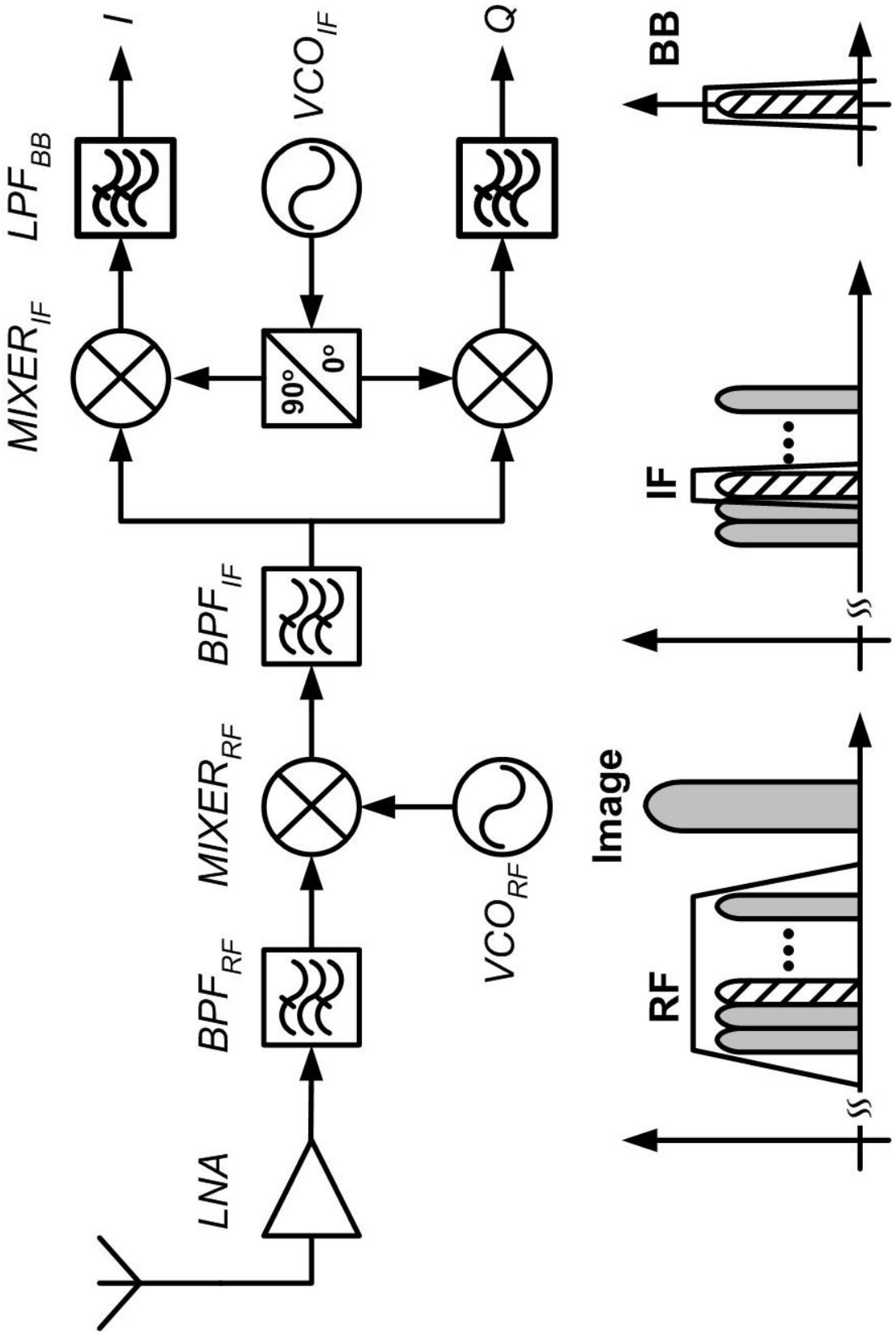


Fig. 1.1 Block diagram of the heterodyne receiver.

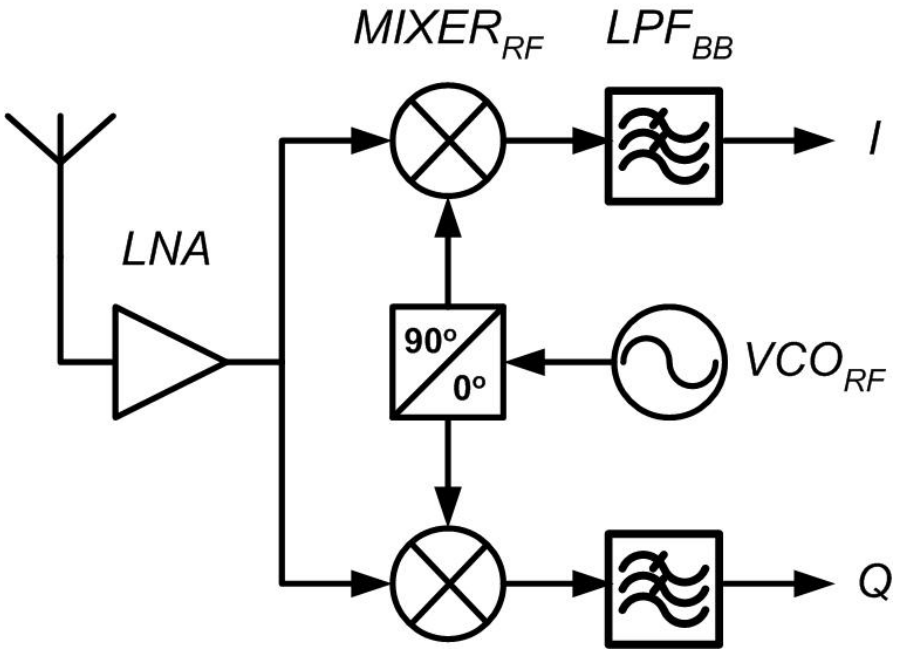


Fig. 1.2 Block diagram of the direct-conversion receiver.

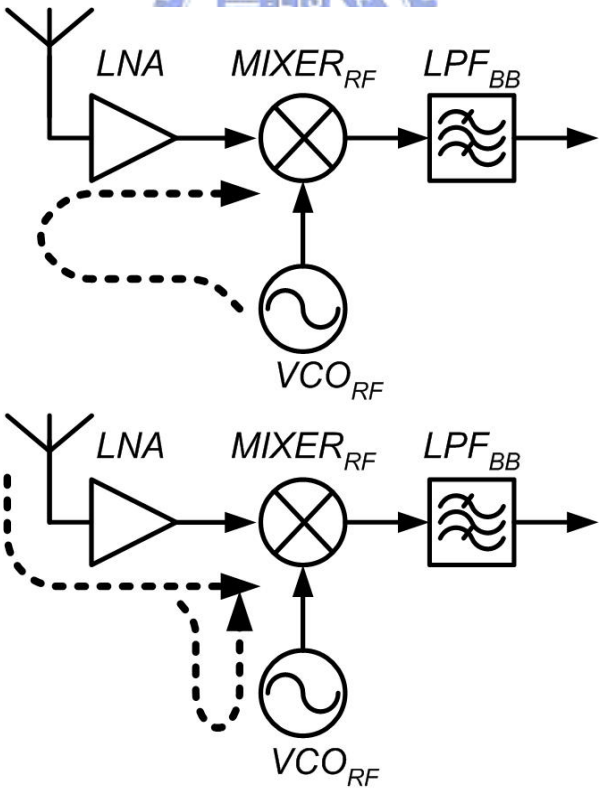


Fig. 1.3 Two sources of DC offsets in the direct-conversion receiver.

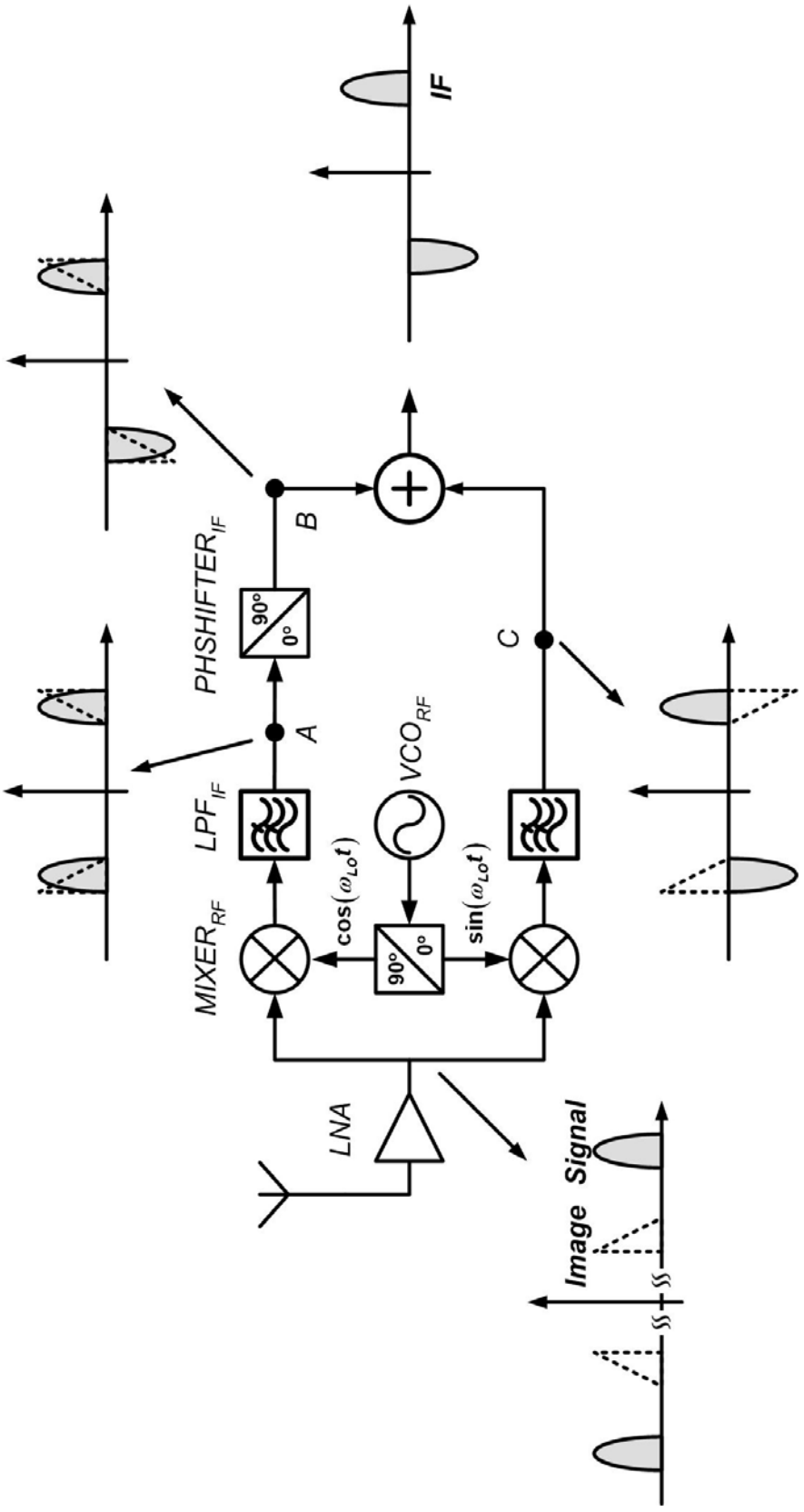


Fig. 1.4 Block diagram and the spectral flow of Hartley image-reject receiver.

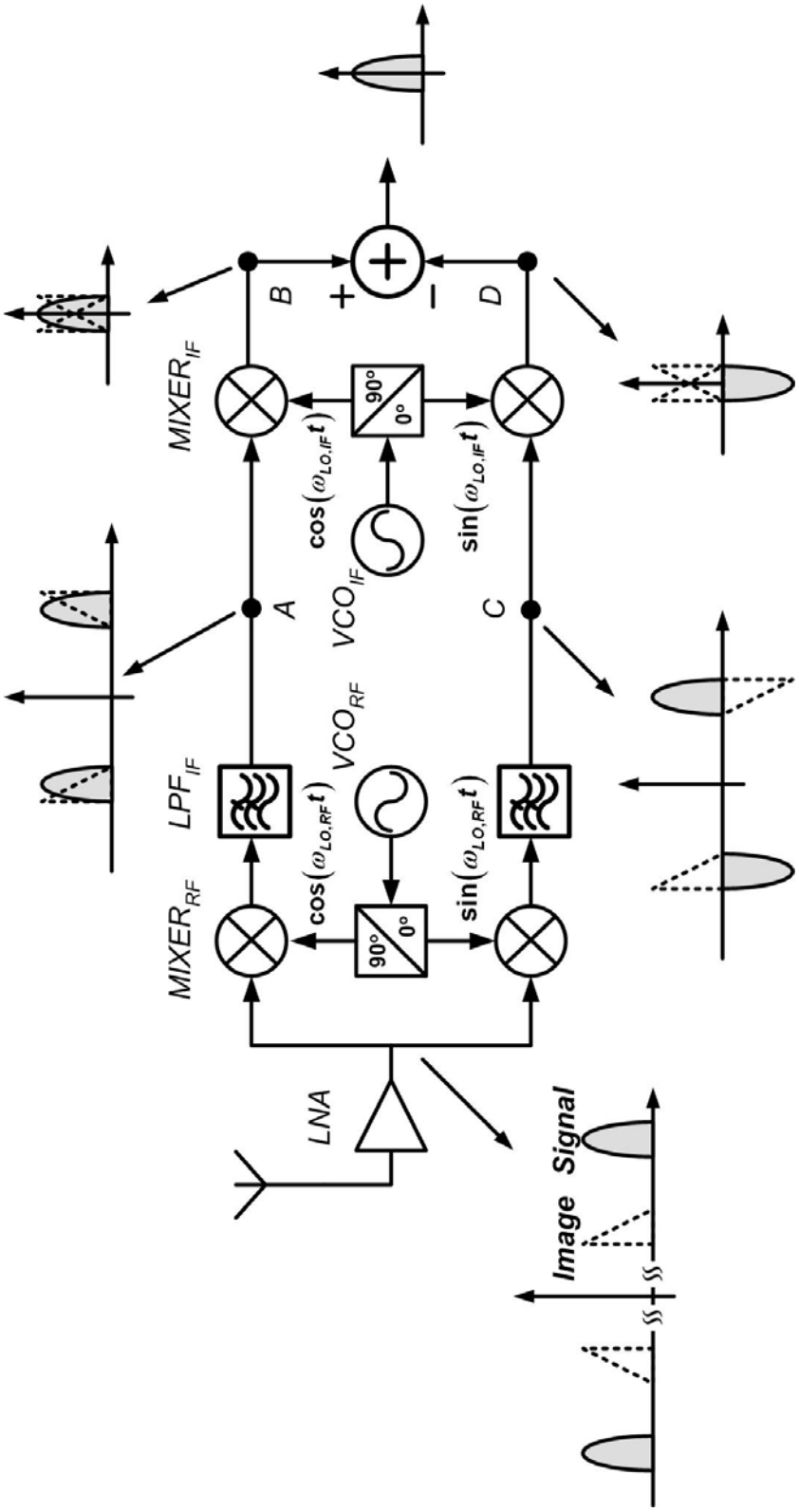


Fig. 1.5 Block diagram and the spectral flow of Weaver image-reject receiver.

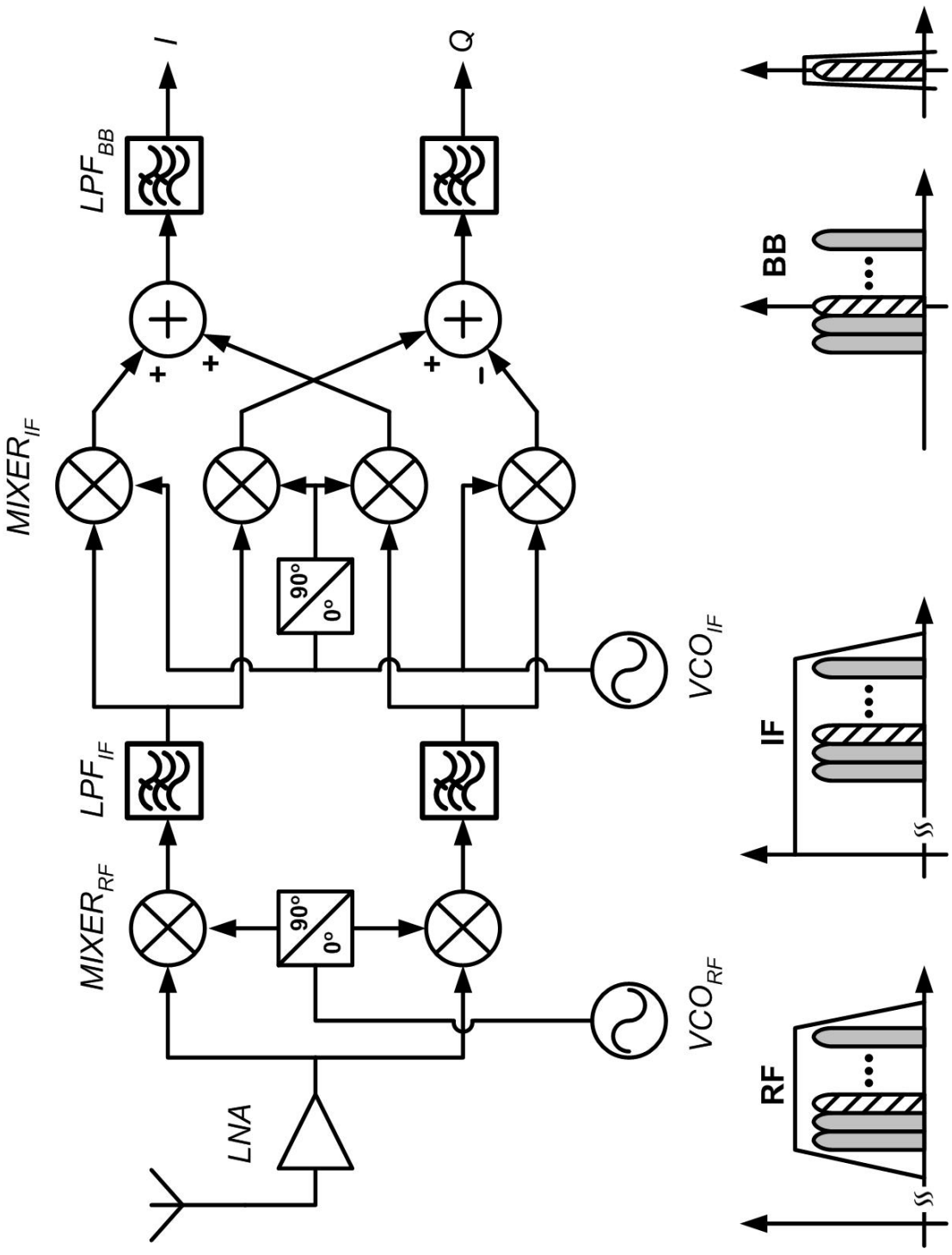


Fig. 1.6 Block diagram of the wideband-IF receiver.

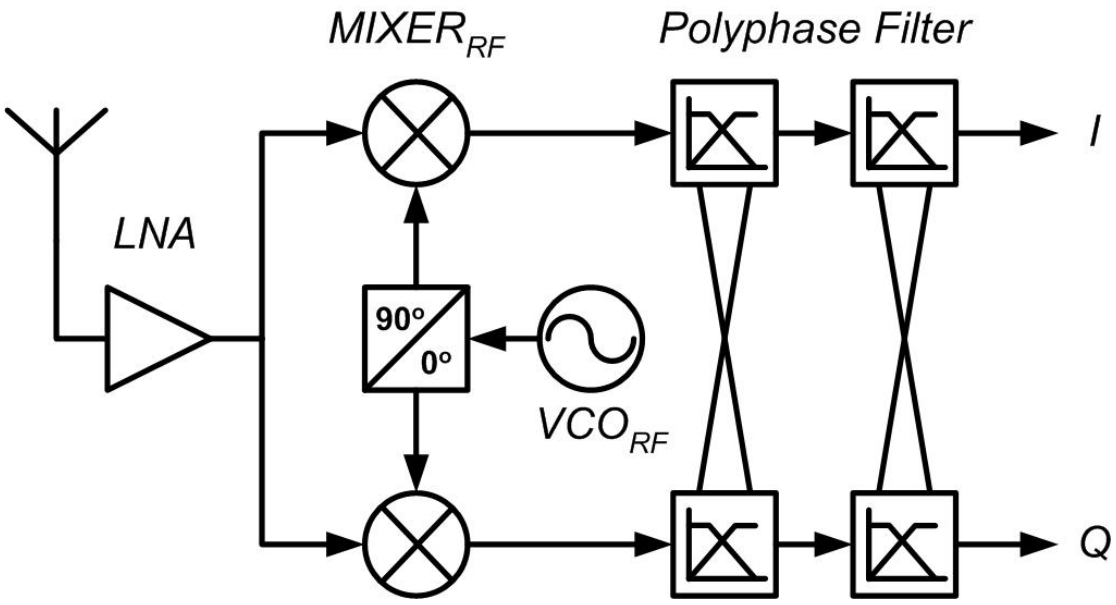
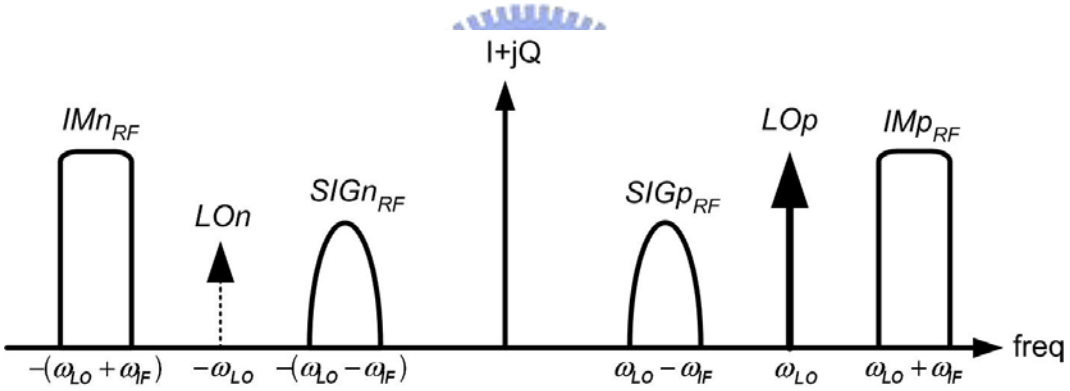


Fig. 1.7 Block diagram of the low-IF receiver.



$$LOp \otimes (SIGn_{RF} + IMn_{RF}) + LOn \otimes (SIGp_{RF} + IMp_{RF})$$

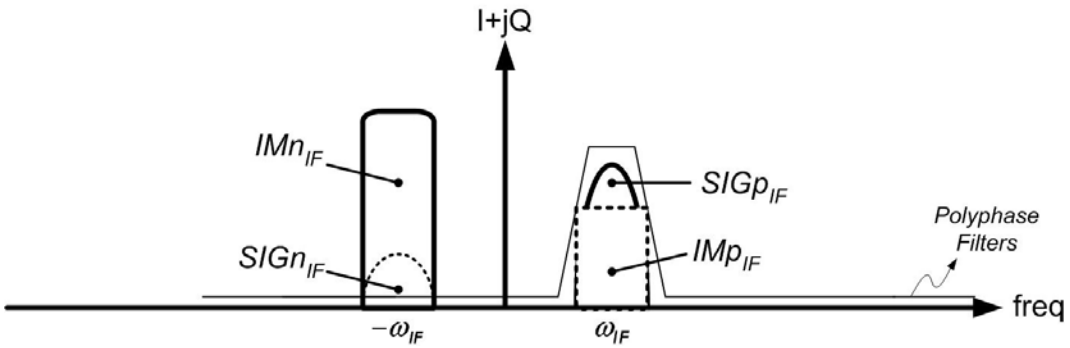


Fig. 1.8 Spectral flow of the low-IF receiver.