CHAPTER 2

THE DESIGN OF ACTIVE POLYPHASE FILTER

2.1 INTRODUCTION

The fast growth of wireless applications in recent years has driven intense efforts to design highly integrated, high-performance, low-cost RFICs. Both low-IF [33]-[37] and double-quadrature [38]-[40] architectures have been adopted as promising receiver topologies to realize these design goals because they combine the advantages of heterodyne and direct-conversion architectures. In the low-IF receiver, the RF signal is amplified and downconverted to a low IF signal in a single step through the quadrature demodulator. After downconversion, polyphase filters [41][42] must be used to filter image signals at the intermediate frequency for both I and Q channels.

To avoid the signal-to-noise ratio (*SNR*) degradation by image interferences, a polyphase filter should provide high selectivity between the desired and image signals. Moreover, the power consumption must be low to prolong the lifetime of the batteries for use in portable wireless communications systems. Polyphase filters in some current standard applications require wide bandwidths. For example, a 20MHz channel bandwidth is required for IEEE 802.11a wireless LAN [7] and HIPERLAN2 [8]. Accordingly, the design of high-performance, wideband, and low-power on-chip polyphase filters for these applications are critically needed.

So far, many polyphase filters have been proposed [43]-[47]; they can be divided into two types, namely passive RC polyphase filters and active polyphase filters. Passive RC polyphase networks are used in passive RC polyphase filters[43][44]. The voltage transfer function of the RC polyphase networks depends on the phase order of the input sequence; it can distinguish between signals with positive frequencies and those with negative frequencies. The passive RC polyphase filter can exhibit a high image rejection ratio (*IRR*), but has a limited range of operating frequencies. The desirable filtering function can only be obtained in the narrow band around the pole frequency, which depends on the RC time constant. To increase the bandwidth, a multi-stage network is proposed to achieve the broadband response [48].

The expense of the multi-stage passive polyphase filter is that it is lossy, so its output signal decays. Additional buffers should be inserted among the stages to compensate the loss. However, these buffers significantly increase the power consumption because the input impedance of each one-stage passive RC polyphase filter is low. More power is consumed as more stages are used to increase the bandwidth. Furthermore, the variation of resistances and capacitances should be kept within a desired small range to achieve a high *IRR*. This means large chip area is required because the variations of adjacent on-chip resistances and capacitances are inversely proportional to their surface area [49]. As the area of resistors increases, it also increases the parasitic capacitance and lowers the cut-off frequencies of resistors. Thus, a critical trade-off must be made among *IRR*, chip area and maximum operational frequency of passive RC polyphase filters.

Active polyphase filters have the general advantages of low power dissipation, small chip area and high signal gain. All the active polyphase filters proposed so far

[45]-[47] have operating frequencies in the range of several hundreds of KHz to several of MHz. The polyphase filter in [45] provides a good image rejection ratio at 250kHz by using op-amp circuits. In [46], the active gm-c polyphase filter provides a -53dB of image rejection ratio at 3MHz without tuning circuits by using a well-controlled special analog process. In [47], the gm-c polyphase filter with *CMFB* (common-mode feedback) and *CMFF* (common-mode feed forward) circuits and frequency-tuning circuits, can achieve more than -45dB of *IRR* in a bandwidth of 1MHz with a central frequency of 2MHz.

In this chapter, a new broadband CMOS active polyphase filter with a wide range of operating frequencies is proposed and designed by using the basic polyphase filter architecture, which is used to implement passive RC polyphase filter. A constant-gm bias circuit [50] is used to decrease the sensitivities of the filter gain and the bandwidth to temperature and process variations. Additionally, the multi-stage approach is also applied to achieve the wide bandwidth. Due to the high input impedance in each stage, the proposed active polyphase filter can avoid the degradation of gain between pairs of stages when connected in cascade. Thus, power-consuming buffers are not required. Using 0.25μm CMOS 1P5M technology, the proposed four-stage active polyphase phase filter can achieve an IRR of -48dB in the 6.1MHz ~ 30MHz band. The filter consumes 11mW (5.5mW) with a power supply of 2.5V (1V). A higher IRR can be achieved by increasing the number of cascaded stages although the achievable IRR is limited by matching.

The model for the new active polyphase filter is presented in Section 2.2. Section 2.3 describes the circuit design methodology. HSPICE simulation results verify the functions of the circuits. Section 2.4 presents experimental results. Finally, Section 2.5

draws conclusions.

2.2 MODEL FOR THE ACTIVE POLYPHASE FILTER

The polyphase filter is a complex filter because its frequency response is not symmetrical around dc. The transfer function *H(s)* of a complex filter can be represented as

$$H(s) = H_1(s) + jH_2(s) \tag{2.1}$$

where $H_1(s)$ and $H_2(s)$ are the real and imaginary parts of the complex transfer function. If a complex signal $C_i(s)=I_i(s)+jQ_i(s)$ is applied to this complex filter, the output signal $C_o(s)$ can be written as

$$C_o(s) = C_i(s)H(s) = I_o(s) + jQ_o(s) \tag{2.2}$$

$$I_o(s) = I_i(s)H_1(s) - Q_i(s)H_2(s) \tag{2.3}$$

$$Q_o(s) = I_i(s)H_2(s) + Q_i(s)H_1(s) \tag{2.4}$$

where $I_o(s)$ and $Q_o(s)$ are the real and imaginary parts of $C_o(s)$, respectively. If $C_o(s)$ can be generated by a circuit from the input complex signal $C_i(s)$ according to (2.3) and (2.4), then the complex transfer function *H(s)* can be realized by this circuit. Fig. 2.1 shows the signal flowgraph for the realization of *H(s)* by using (2.3) and (2.4). In this way, any complex filter can be realized by a combination of the real and imaginary parts of its transfer functions.

The transfer function *H(s)* of the one-stage RC network can be used to implement a polyphase filter, according to the approach presented above. The resultant transfer function *H(s)* is represented as

$$H(s) = H_1(s) + jH_2(s) = \frac{A\omega_P}{s+\omega_P} + j\frac{As}{s+\omega_P} \tag{2.5}$$

where A and ω_P are the gain and pole frequency, respectively, of the first-order low-pass filter $H_1(s)$ and the high-pass filter $H_2(s)$. The combination of $H_1(s)$ and $H_2(s)$ forms a block denoted as the Low-High-Pass filter (*LHF*) in Fig. 2.1. According to (2.5), the transfer curves of $|H(j\omega)|$ and $|H(-j\omega)|$ versus frequency for A=1 and ω_P=10MHz are shown in Fig. 2.2 in solid lines. Notably, the desired signal with negative frequency falls in the filter's passband while the image signal at positive frequency is attenuated. $|H(j\omega)|$ is lowest at $\omega=\omega_P$ where ω_P is also called the rejected frequency. Using the equation in (2.5), the image rejection ratio IRR_{PPF} of the polyphase filter defined as the ratio of the magnitude in the attenuation band to that in the passband, can be derived as

$$IRR_{PPF}(\omega) = \frac{|H(s=j\omega)|}{|H(s=-j\omega)|} = \left|\frac{\omega_p - \omega}{\omega_p + \omega}\right| \tag{2.6}$$

As may be seen from (2.6), the IRR_{PPF} can be zero at frequency ω_P if the gains and pole frequencies of $H_1(s)$ and $H_2(s)$ are perfectly matched.

Considering the gains and pole frequencies mismatches between $H_1(s)$ and $H_2(s)$, the transfer function (2.5) can be rewritten as

$$H(s) = \frac{A\omega_P(1-\Delta A/2A)(1-\Delta\omega_P/2\omega_P)}{s+\omega_P(1-\Delta\omega_P/2\omega_P)} + j\frac{A(1+\Delta A/2A)s}{s+\omega_P(1+\Delta\omega_P/2\omega_P)} \tag{2.7}$$

where ΔA and $\Delta\omega_P$ are the mismatch quantities of A and ω_P, respectively. The simulated $|H(j\omega)|$ and $|H(-j\omega)|$ versus frequency with 20% variations are shown by the dashed lines in Fig. 2.2. It is shown that the transfer curves of $H(s=j\omega)$ and $H(s=-j\omega)$ are shifted to the opposite directions and the resulting IRR_{PPF} at $\omega=\omega_P$ is degraded. Using (2.7) and neglecting high-order terms, the image rejection ratio IRR_{PPF} with

mismatch effects can be derived as

$$IRR_{PPF}(\omega) \cong$$

$$\{[64A^2(\omega^4-\omega_P{}^4)\frac{\Delta A}{A}+64A^2\omega\omega_P(\omega-\omega_P)^2\frac{\Delta\omega_P}{\omega_P}+64A^2(\omega^2+\omega_P{}^2)(\omega-\omega_P)^2$$

$$+16A^2(\omega^2+\omega_P{}^2)(\omega+\omega_P)^2(\frac{\Delta A}{A})^2+32A^2\omega_P{}^2(\omega^2-\omega_P{}^2+\omega\omega_P)(\frac{\Delta\omega_P}{\omega_P})^2]$$

$$/[64A^2(\omega^4-\omega_P{}^4)\frac{\Delta A}{A}-64A^2\omega\omega_P(\omega+\omega_P)^2\frac{\Delta\omega_P}{\omega_P}+64A^2(\omega^2+\omega_P{}^2)(\omega+\omega_P)^2]\}^{\frac{1}{2}} \quad (2.8)$$

Fig. 2.3 depicts the exact $IRR_{PPF}(\omega=\omega_p)$ with the corresponding mismatches $\Delta\omega_P/\omega_P$ and $\Delta A/A$, where the numbers on the curves denote the IRR_{PPF} values in dB. The figure demonstrates that if $|\Delta A/A|>12\%$ or $|\Delta\omega/\omega_P|>5\%$, then the IRR_{PPF} at $\omega=\omega_P$ is degraded to -30dB. Therefore, the gains and locations of the pole frequencies in $H_1(s)$ and $H_2(s)$ should be kept highly consistent to achieve the desired image rejection performance.

A broadband polyphase filter can be realized by cascading several stages of one-stage polyphase filter. The resultant image rejection ratio IRR_{PPFN} of the N-stage polyphase filter can be derived by multiplying all IRR_{PPF} values of the constituent one-stage polyphase filters as

$$IRR_{PPFN}(\omega)=\prod_{n=1}^{N} IRR_{PPF,n}(\omega) \quad (2.9)$$

where $IRR_{PPF,n}$ is the IRR_{PPF} of the nth-stage polyphase filter. Ideally, the image rejection ratio can be improved with a cascaded multistage structure, as indicated by (2.9). Note that the range of operating frequencies can also be expanded by assigning a different value of ω_P to each one-stage polyphase filter. To provide the sufficient IRR_{PPF}, the adequate number of stages should be determined. According to [48], the required stage can be shown in Fig. 2.4, where the ω_{max} and ω_{min} means the upper and

lower bounds of the rejection band, respectively. As seen from Fig. 2.4, at least four stages are required to achieve –50dB of IRR_{PPF} within the band of 5MHz~25MHz.

2.3 CIRCUIT DESIGNS

2.3.1 The Circuit Design of Wideband Active Polyphase Filter

The proposed polyphase filter structure in Fig. 2.1 consists of a low-pass filter $H_1(s)$ and a high-pass filter $H_2(s)$ in each of the two *LHF* blocks. The CMOS realization of a *LHF* block is shown in Fig. 2.5(a) where the functions of $H_1(s)$ and $H_2(s)$ are combined. In Fig. 2.5(a), the NMOS device M_1 converts the input voltage V_I to current i_1 and then the current is mirrored to i_3 and i_4 by the PMOS current mirrors M_2, M_3, and M_4. The diode-connected transistor M_L and the capacitor C_H then divide the mirrored current i_3 into i_L and i_H, respectively. The currents i_L and i_H can be derived as

$$i_L = V_I \frac{gm_1(gm_L/C_H)}{s+(gm_L/C_H)} \tag{2.10}$$

$$i_H = V_I \frac{gm_1 s}{s+(gm_L/C_H)} \tag{2.11}$$

where gm_1 and gm_L are transconductances of M_1 and M_L, respectively. Using the mirrored currents i_L and i_H, the required low-pass and high-pass transfer functions $H_1(s)$ and $H_2(s)$ can be realized as

$$H_1(s) = \frac{V_{OL}}{V_I} = \frac{1}{gm_7} i_{OL} = \frac{1}{gm_7} K_L i_L = K_L \frac{(1/gm_7)gm_1(gm_L/C_H)}{s+(gm_L/C_H)} \tag{2.12}$$

$$H_2(s)=\frac{V_{OH}}{V_I}=\frac{1}{gm_8}(i_{OH})=-\frac{1}{gm_8}(i_4-i_5)=-\frac{1}{gm_8}(K_H i_3-K_H i_L)$$
$$=-\frac{1}{gm_8}K_H i_H=-K_H\frac{(1/gm_8)gm_1 s}{s+(gm_L/C_H)} \quad (2.13)$$

where K_L is the current ratio of M_6 and M_L, K_H is the current ratio of M_4 (M_5) and M_3 (M_L), and gm_7 (gm_8) is the transconductance of M_7 (M_8). The capacitor C_C connected between node A and V_{OH} is used to pass the ac current i_{OH} = i_4-i_5, but block the dc voltage. The rejected frequency ω_P can be adjusted by changing C_H since the poles of both transfer functions $H_1(s)$ and $H_2(s)$ are determined by $\omega_P = gm_L/C_H$.

The parasitic effects of the *LHF* circuit in Fig. 2.5(a) are analyzed. The parasitic capacitance C_P at node A has the largest value as compared to those at other nodes, because C_P consists of the parasitic capacitance of C_C and the device capacitance of M_4 and M_5. With C_P at node A, the transfer function of $H_2(s)$ can be derived as

$$H_2(s)=-K_H\left[\frac{(1/gm_8)gm_1 s}{s+(gm_L/C_H)}\right]\left[\frac{gm_8/C_P}{s+\frac{gm_8(C_C+C_P)}{C_C C_P}}\right] \quad (2.14)$$

As (2.14) shows, the second pole at $\omega_{P2} = gm_8(C_C+C_P)/C_C C_P$ is generated. Since ω_{P2} may affect the magnitude and phase of $H_2(s)$ and thus degrade the *IRR* of the polyphase filter, ω_{P2} should be kept at least ten times larger than ω_P to minimize the degradation of *IRR*.

Based on the structure illustrated in Fig. 2.1, a one-stage polyphase filter $H(s)$ with a differential structure can be realized by the combination of *LHF* circuits. In general, the mixers used in the receiver are designed in differential circuits to cancel the LO-to-IF feedthrough [51]-[56]. Thus the proposed polyphase filter is designed in differential type to process the differential output signals from the mixers. Fig. 2.5(b)

shows the differential *LHF*, *LHFD*. The *LHFD* consists of two *LHFs* with a common current source device M_b, which is used to provide the bias current of *LHF* and reject the input common mode signal. Fig. 2.5(c) shows the complete circuit of one-stage polyphase filter, based on the structure in Fig. 2.1. The output node L ($\overline{L}$) of $LHFD_I$ is connected to the output node $\overline{H}$ (H) of $LHFD_Q$ to realize the subtraction function in Fig. 2.1, whereas the summation function in Fig. 2.1 is realized by connecting the output node H ($\overline{H}$) of $LHFD_I$ to the output node L ($\overline{L}$) of $LHFD_Q$. Finally, the output currents are converted to voltages by connecting them to diode-connected transistors M_7, $\overline{M_7}$, M_8 and $\overline{M_8}$. Fig. 2.5(c) realizes the signal flowgraph of Fig. 2.1 in differential structure.

According to (2.12) and (2.13), both the gains and the poles of the transfer functions $H_1(s)$ and $H_2(s)$ are dependant on transconductances of transistors. Therefore, transconductances are important parameters and must be stabilized. The stability of gm is achieved by using a constant-gm bias circuit, as shown in Fig. 2.6. In the bias circuit, M_{B1}~M_{B6} are bias transistors and M_{B7}~M_{B9} works to start-up. The transconductance of M_{B1} is

$$gm_{B1} = 2\left[1-\sqrt{(W/L)_{B1}/(W/L)_{B2}}\right]\Big/R_B \tag{2.15}$$

where $(W/L)_{B1}$ and $(W/L)_{B2}$ are geometric ratios of M_{B1} and M_{B2}, respectively. The transconductance of M_{B1} is determined by geometric ratios, independent of process parameters and temperature. Besides, not only is gm_{B1} stabilized, but all other transconductances are also stabilized since all transistor currents are derived from the same biasing network. Therefore, the transconductances of other transistors are mainly dependent on geometry.

As seen from (2.7) and (2.8), the $IRR_{PPF}(\omega=\omega_P)$ is degraded if the gain and pole frequencies of $H_1(s)$ and $H_2(s)$ are not identical. Since the pole frequencies of $H_1(s)$ and $H_2(s)$ shown in (2.12) and (2.13) are identically determined by gm_L and C_H, the pole frequencies mismatch can be avoided. The gain mismatch between $|H_1(s=\omega_P)|$ and $|H_2(s=\omega_P)|$ can be reduced to the balance between K_L/gm_7 and K_H/gm_8. K_L and K_H are current ratios and the mismatch can be kept small. To reduce the mismatch of gm_7 and gm_8, the layout of M_7 and M_8 can be put in common centroid. Moreover, minimum channel length is not used in this design to further reduce the gain mismatch. In the passive RC polyphase filter, the gain mismatch depends on not only the matching in RC values and transconductances of buffers in I/Q paths, but also parasitic capacitors of resisters. In comparison with the mismatch effects of current ratio and tansconductance in the proposed active polyphase filter, the IRR_{PPF} won't be worse than the one in passive RC polyphase filter.

A broadband multi-stage polyphase filter can be realized by cascading several stages of one-stage polyphase filters. Unlike the passive RC polyphase filter, cascading the proposed active polyphase filters can avoid the degradation of gain among stages because the input impedance in each stage is high. In each stage, C_H should be adjusted to obtain different reject frequencies. All other circuits in Fig. 2.5(c) remain unchanged, greatly reducing the complexity of the design of a multi-stage polyphase filter.

The proposed wide bandwidth polyphase filter, which targets at an image rejection ratio of -50dB within 5MHz~25MHz is realized in 0.25-um 1P5M CMOS technology with a power supply of 2.5V. According to the result shown in Fig. 2.4, four one-stage polyphase filters are cascaded in this design. Four poles are placed

equally on the logarithmic frequency axis and fine-tuned by simulations to achieve the equal ripple [48]. The equal ripple characteristic can achieve not only the highest IRR_{PPF4} but relax the IRR_{PPF4} degradation caused by mismatches between stages. The capacitors C_H in the four one-stage polyphase filters are 3.5pF, 5.5pF, 10pF and 16pF, respectively. The resultant rejected frequencies are 24.5MHz, 15.5MHz, 8.5MHz and 5.4MHz, respectively.

2.3.2 The Simulation Results of Active Polyphase Filter

With the parameters shown in Table 2.1 (C_H=3.5pF), the simulated transfer curve at positive and negative frequencies and the image rejection ratio IRR_{PPF} of the one-stage CMOS polyphase filter (ω_P=24.5MHz) are shown in Fig. 2.7. As seen from Fig. 2.7, the IRR_{PPF} of –51dB at the rejected frequency and 2dB voltage gain can be achieved.

The effects of process and temperature variations in the one-stage CMOS polyphase filter that incorporates the constant-gm bias circuit are verified, HSPICE simulation shows that the transconductance variations of M_1 in Fig. 2.6 can be kept within 2.3% and 2% with the four corners (FF, FS, SF, and SS) of device model parameters and variations in the temperature between 0^o and 80^o, respectively. Fig. 2.8 and Fig. 2.9 show the simulated transfer curve and IRR_{PPF} with process and temperature variations. As seen from Fig. 2.8 and Fig. 2.9, the variations of rejected frequency can be kept within 8% and 5%, respectively. Accordingly, the desired IRR_{PPF} can be achieved under process and temperature variations.

With the random variations among components, the one-stage polyphase filter (ω_P=25MHz) biased with a constant-gm circuit is verified by 30-times of Monte Carlo

simulations. All device dimensions are the same as the values listed in Table 2.1. The variations of transistor parameters ΔW (channel width), ΔL (channel length) and $\Delta V_{th(p,n)}$ (threshold voltage) are randomly distributed according to the values provided by the corner parameters of the MOS device model, such that ΔW=±0.03um, ΔL=±0.02um, ΔV_{thp}= ±0.06V, and ΔV_{thn}=±0.05V. The relative variations of capacitance resistance are 10%. The results of the simulation show that the worst IRR_{PPF} at 24.5MHz still exceeds -32dB and the variations of rejected frequency can be kept within 5.3%.

A wide bandwidth polyphase filter with four cascaded one-stage polyphase filters is realized. Fig. 2.10 plots the simulated transfer curves at positive and negative frequencies and the image rejection ratio IRR_{PPF4} of the designed four-stage polyphase filter. It is shown that the IRR_{PPF4} can exceed -50dB by the four-stage polyphase filter over the bandwidth 4.5MHz~27.5MHz. The voltage gain at 20MHz is 7dB. The total power consumption is 11mW at a power supply of 2.5V.

HSPICE simulations are performed to verify the effects of process and temperature variations. The results in Fig. 2.11 show that the IRR_{PPF4} exceeds -50dB over the range of 5MHz~26.5MHz under the four corners of the MOS device models. As the temperature varies from 0^o to 80^o, Fig. 2.12 shows that an IRR_{PPF4} of -50dB can also be achieved within 4.75MHz to 27MHz. Thus, the performance of the proposed wide bandwidth polyphase filter can be well controlled as the process and temperature are varied.

In the multistage polyphase filter, the gain divided between stages will lead to different noise and linearity performances. Table 2.2 lists the simulated noise figure

(*NF*) and *IIP3* characteristics of the four-stage polyphase filter where the 8dB total gain are divided between four stages in different conditions. As seen in Table 2.2, a larger gain assigned in the preceding stage results in a better noise figure and a worse *IIP3*. On the contrary, a larger gain assigned in the back stage leads to a better *IIP3* but worse noise figure. Thus, the gain can be assigned flexible between stages for different noise and linearity requirements.

The proposed active polyphase filter can be modified for Bluetooth applications. The Bluetooth standard specifies the operation channel bandwidth is 1MHz and group delay smaller than 6μs is required [47]. Since the channel bandwidth is narrow compared to the requirement in IEEE 802.11a, the intermediated frequency can be chosen as low as several MHz to relax the design complexity in IF stages. In the modified polyphase filter, the operational frequency is chosen from 3 to 4 MHz and two stages are needed by the relation shown in Fig. 2.4. The simulation shows if the poles of the two-stage polyphase filter are 3.1 and 3.8 MHz, 50dB of *IRR* and 55ns of the group delay can be achieved within the passband.

2.3.3 Layout Consideration

Layout is an important step in designing the polyphase filter. Since the gains and pole frequencies in $H_1(s)$ and $H_2(s)$ should be kept highly consistent to achieve a high IRR_{PPF}, layout of corresponding components should be kept symmetrical carefully. Fig. 2.13 shows the floor planning of the one-stage polyphase filter. The solid-line and dashed-line blocks represent the transistors in positive and negative paths, respectively. The transistors in I (Q) path are separated to two parts I1, I2 (Q1, Q2). As seen from Fig. 2.13, the transistors are placed symmetry for not only differential

paths but also I/Q paths. To reduce the process variation, dummy gates and dummy capacitors are added beside the edge-transistors and edge-capacitors. Besides, a piece of ground metal is inserted between the I and Q routing metals for shielding off the mutual interference.

2.3.4 The Circuit Design of 1-V Wideband Active Polyphase Filter

With the advantage of currents operation, the proposed active polyphase filters can be modified to operate at a low supplied voltage. Fig. 2.14 shows the low-voltage version of *LHF* where the transistor M_2 is connected in a folded structure. Therefore, the required power supply can be as low as the threshold voltage V_{th2} of M_2 plus the drain-source voltage V_{DSb2} of M_{b2}. M_{b2} works as a current source, which provides a constant dc current to M_1. Because the high impedance at the drain of M_{b2}, the current i_1, which is generated from the input voltage signal V_I by M_1, flows to M_2 and then mirrored to i_3. The functions of other transistors are similar to those of the corresponding transistors in Fig. 2.5(a). With a supplied voltage of 1V and 0.25um 1P5M CMOS technology, the transfer curves and the IRR_{PPF4} of a low-voltage four-stage polyphase filter are shown in Fig. 2.15. Fig. 2.15 shows that an IRR_{PPF4} of -50dB can be achieved within the frequency range 4.9MHz ~ 27MHz. The simulated CMRR within this bandwidth is 40dB. The 1V polyphase filter consumes 5.5mW, which is only about 50% of the power consumption in the 2.5V version.

2.4 EXPERIMENTAL RESULTS

Fig. 2.16 shows the die micrograph of a four-stage polyphase filter, which is designed and fabricated in 0.25-um 1P5M CMOS technology. The four-stage polyphase filter consumes 11mW at a supplied voltage of 2.5V and occupies a die

area of 1162×813μm^2. All of the capacitors are implemented by metal-insulator-metal (MIM) capacitors.

For measurement purposes, on-chip test buffers are placed after the polyphase filter to analyze the output signals. In the measurement set-up, a splitter converts a single-ended signal into differential signals, which are then sent to a six-stage off-chip RC polyphase filter to generate the required input quadrature signals. The off-chip RC network can provide an *IRR* of more than -55dB in the frequency range 4MHz~35MHz. After the gain loss of the off-chip RC network has been compensated for, the measured voltage gain of the fabricated four-stage polyphase filter at 20MHz is 6.6dB. The measured IRR_{PPF4} is shown in Fig. 2.17, an image rejection ratio of -48dB can be achieved in the frequency range 6.1MHz~30MHz. Fig. 2.18 shows the measured quadrature output signals when 20-MHz differential signals are applied. A two-tone test is performed to measure *SFDR* [57]. As shown in Fig. 2.19, when the input signals are at 19.5MHz and 20.5MHz, the differences between noise floor to fundamental and third-order intermodulation signals are 72.2dB and 21.5dB, respectively. Thus, a 65dB in-band *SFDR* can be achieved by the polyphase filter. Fig. 2.20 shows that the measured input third intercept point (*IIP3*) is 8dBm.

The simulation and measured results of the CMOS four-stage polyphase filter are listed in Table 2.3. The performance comparisons between the recently proposed polyphase filters are given in Table 2.4. In comparison to the passive RC polyphase filter [43], the proposed four-stage active polyphase filter has much lower average power dissipation per stage for the same power supply and higher passband gain while maintaining the same image rejection ratio per stage. In addition, the proposed polyphase filter can achieve a wider band than other active polyphase filter

[45][46][47].

2.5 SUMMARY

A wideband and low-power active polyphase filter has been proposed and analyzed. The wideband performance is achieved by simple CMOS single-stage filter circuit and directly cascaded multistage structure. Without inter-stage buffer, the power dissipation is kept low. The simulations have shown that by biasing with a constant-gm circuit, the variations in process and temperature are effectively reduced. Due to the advantage of current-mode operation, the proposed active polyphase filter has been successfully modified to fit the operation of 1V power supply. The performances of the filter have been verified through measurement on the fabricated chip in 0.25-um 1P5M CMOS technology. The measured image rejection ratio of four-stage polyphase filter is higher than -48dB over the frequency range of 6.1MHz~30MHz. The power consumption is 11mW with 2.5V power supply. It has been shown from measurement results that the proposed active polyphase filter is suitable in wireless communication applications.

Table 2.1

Dimensions of Devices in Constant-Gm Bias Circuit and Polyphase Filter.

Constant-gm bias circuit	
M_1	(4um/1um)
M_2	(4um/1um) • 4
M_3	(1um/1um)
M_4	(1um/2um)
M_5	(8um/1um)
M_6	(8um/1um)
M_7	(4um/1um)
M_8	(0.5um/20um)
M_9	(1um/1um)
R_b	6kΩ
Active Polyphase filter	
M_1	(0.5um/0.5um) • 4
M_2	(2.5um/0.5um) • 4
M_3	(2.5um/0.5um) • 8
M_4	(2.5um/0.5um) • 4
M_5	(0.5um/0.5um) • 4
M_6	(0.5um/0.5um) • 4
M_7, M_8	(2.5um/0.6um) • 4
M_b	(5um/1um) • 4
M_L	(2.5um/0.5um) • 8
C_H	4 stages: 3.5pF, 5.5pF, 10pF, 16pF
C_C	C_H/2

Table 2.2

Simulated *NF* and *IIP3* Characteristics of Different Gain Distributions in the Four-Stage Active Polyphase Filter.

	Av (dB) Stage 1	Av (dB) Stage 2	Av (dB) Stage 3	Av (dB) Stage 4	NF (dB) @ 20MHz	IIP3 (dBm)
A	4	2	2	0	37.5	5
B	2	2	2	2	38.8	9.4
C	0	2	2	4	40.2	11.6

Table 2.3

Measured Characteristics of the Active Polyphase Filter.

Parameter	Simulation Result	Measured Result
Fabrication process	0.25-um 1P5M CMOS technology	
Power supply	2.5V	
Power Dissipation	10.72mW	11mW
Bandwidth	5~25MHz	6.1~30MHz
IRR	-50dB	-48dB
Gain @ 20MHz	7dB	6.6dB
Linearity	8.7dBm	8dBm
SFDR	-	65dB
CMRR	40dB	41dB
Area	1162×813μm^2	

Table 2.4

Comparison Between the Recently Proposed Polyphase Filter.

	This Work	[43]	[45]	[46]	[47]
Type	Active	Passive	Active RC	Gm-C	Gm-C
Number of stage	4	5	5 order Butterworth	5 order Butterworth	6 order Butterworth
Power supply	2.5V	3.3V	5V	2.3V	2.7V
Center Frequency	18MHz	12.5MHz	250KHz	3MHz	2MHz
Bandwidth	23.9MHz	16.5MHz	220KHz	1MHz	1MHz
Total power dissipation	11mW	62.7mW	90mW	7.36mW	12.69mW
Average power dissipation per stage for 2.5V	2.75mW	9.5mW	9mW	1.6mW	3.92mW
Total *IRR*	-48dB	-60dB	-64dB	-53dB	-45dB
Average image rejection ratio per stage	-12dB	-12dB	-12.8dB	-10.6dB	-7.5dB
Passband gain	6.6dB	-1dB	12dB	0dB	15dB
SFDR	65dB	-	-	52dB	45.2dB
Technology	0.25μm	0.6μm	1.2μm	0.35μm	0.35μm

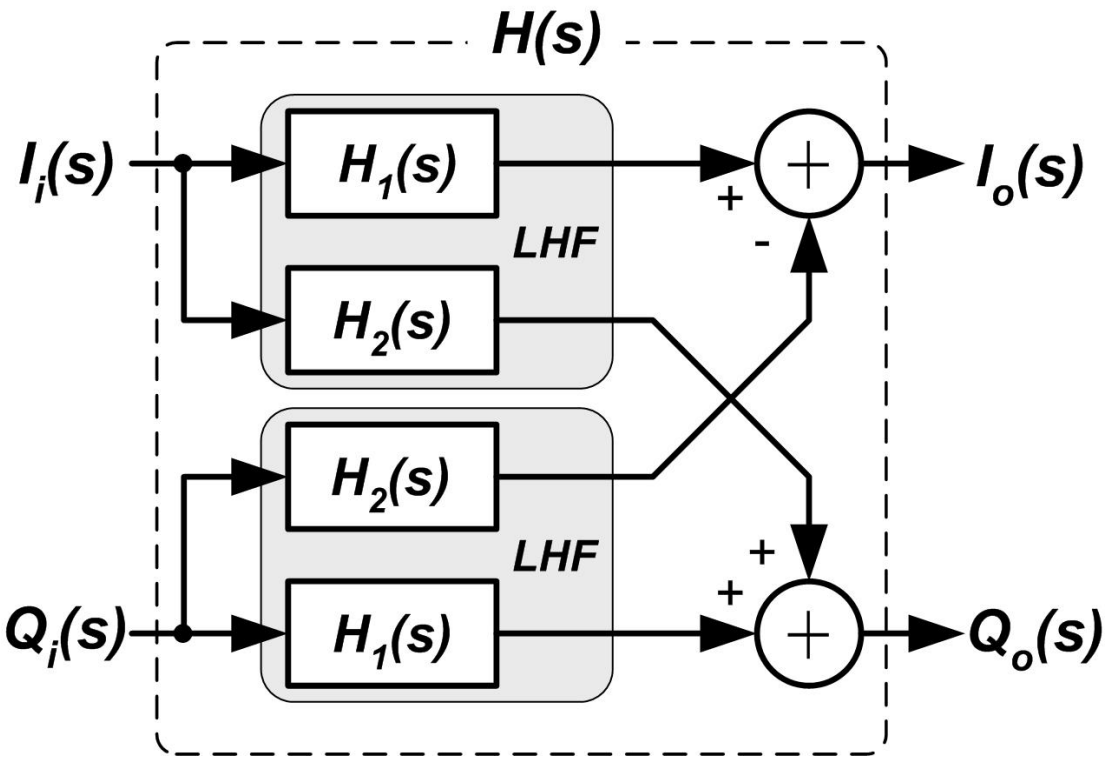


Fig. 2.1 Signal flowgraph for realizing a single-stage complex filter.

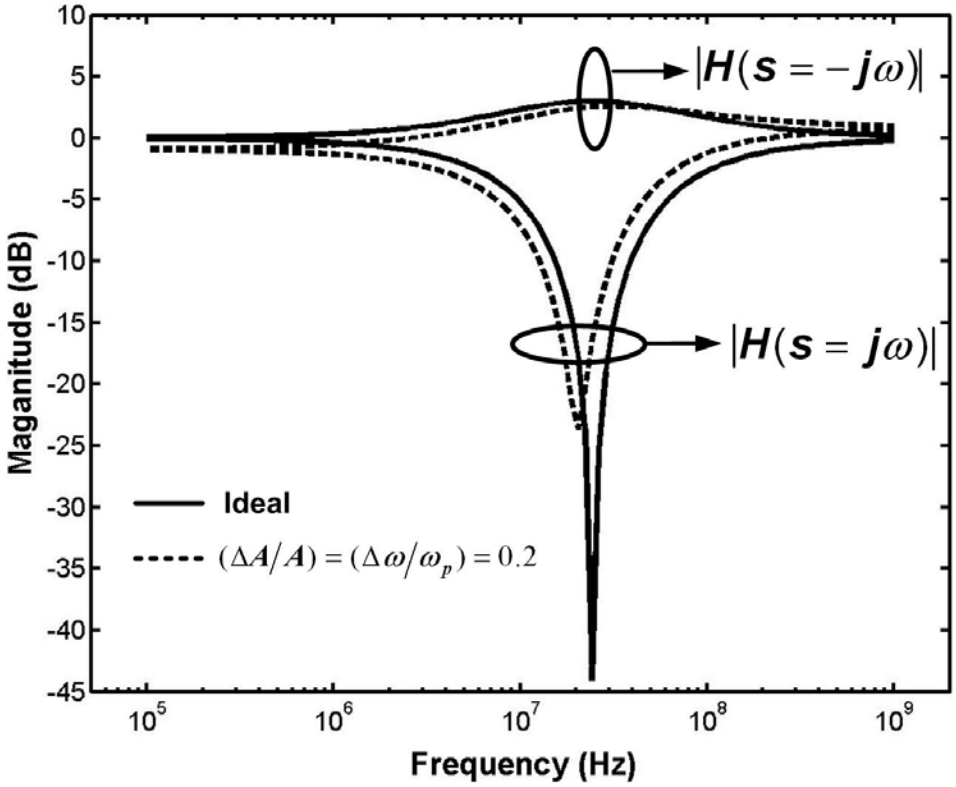


Fig. 2.2 Transfer curves of |*H(s)*| versus frequency.

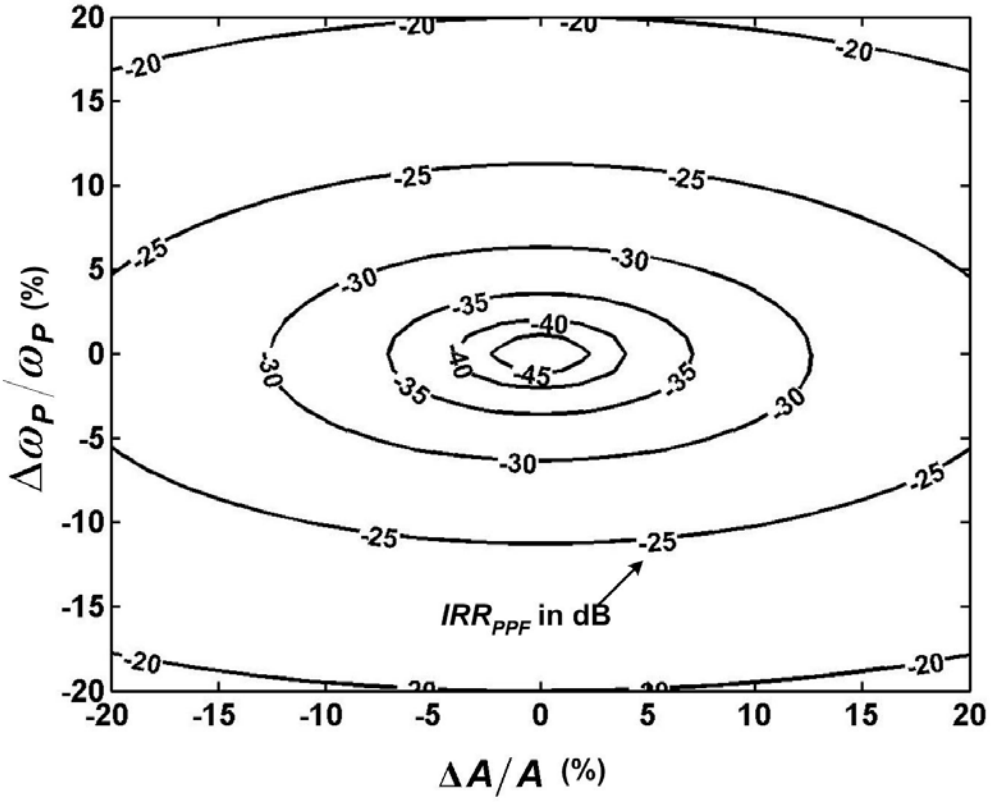


Fig. 2.3 Simulated IRR_{PPF} values (indicated on the curves) of one-stage polyphase filter at $\omega=\omega_p$ with gain and pole frequency variations.

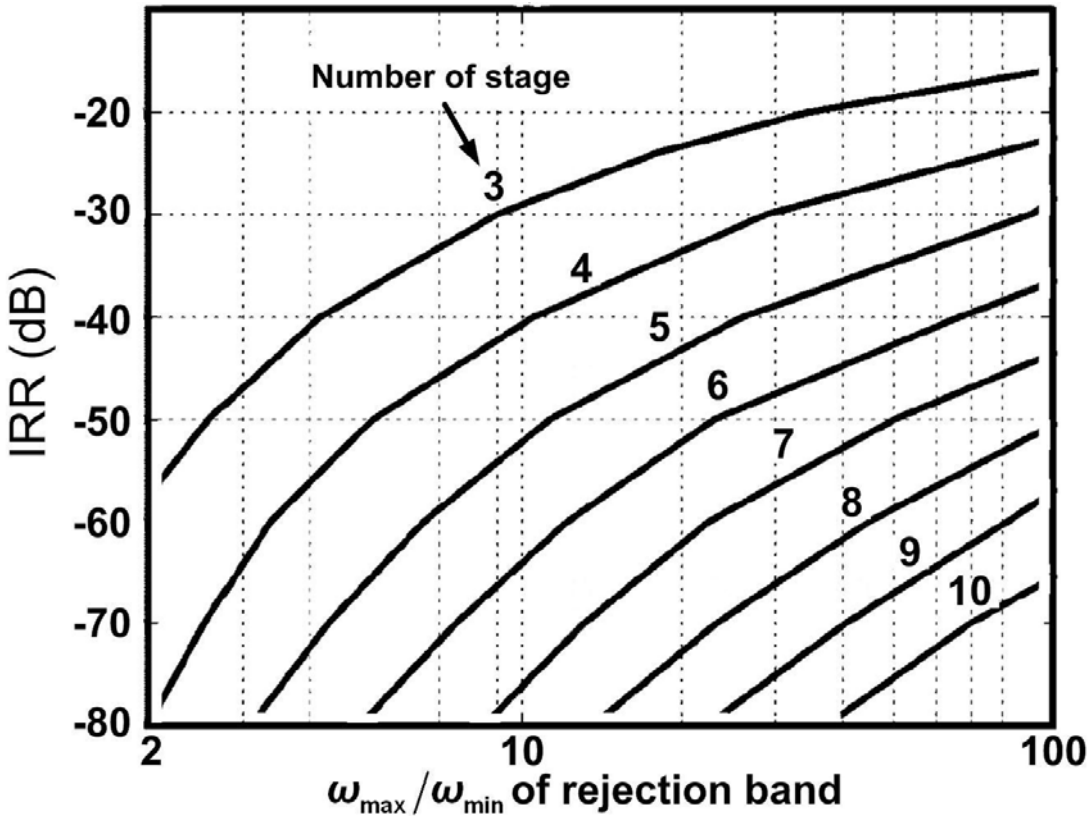
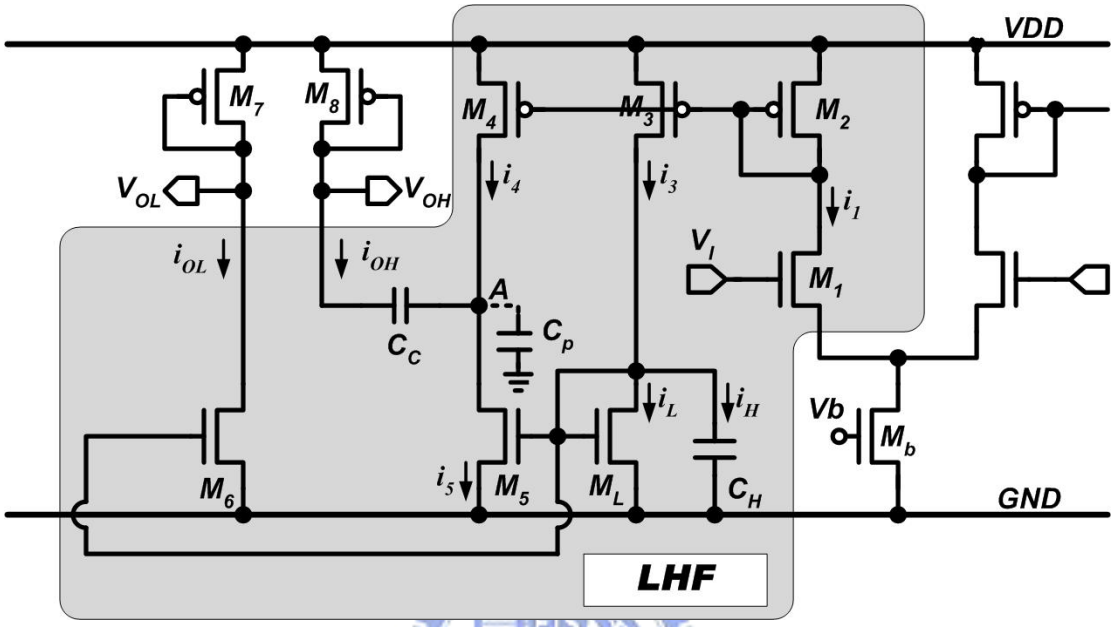
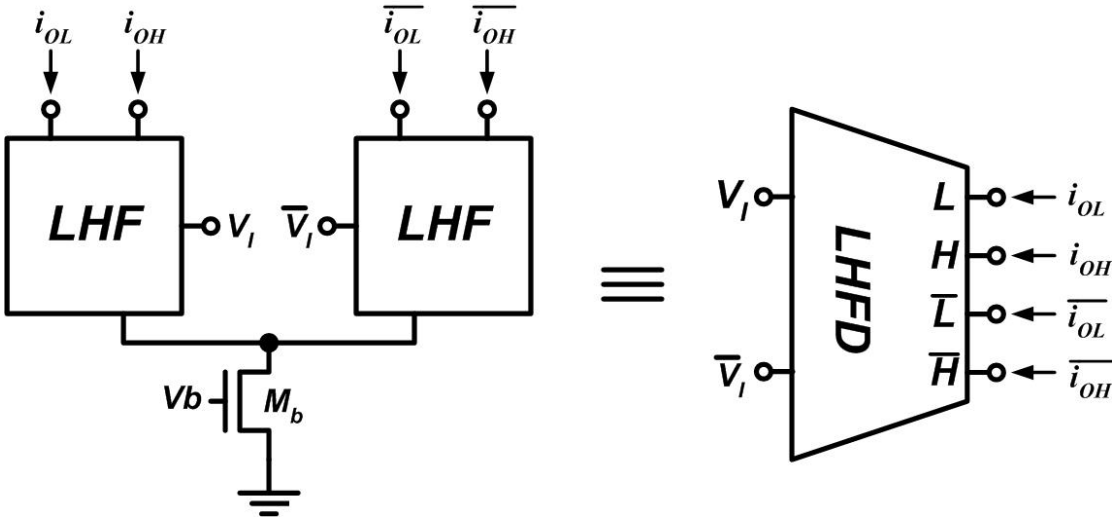


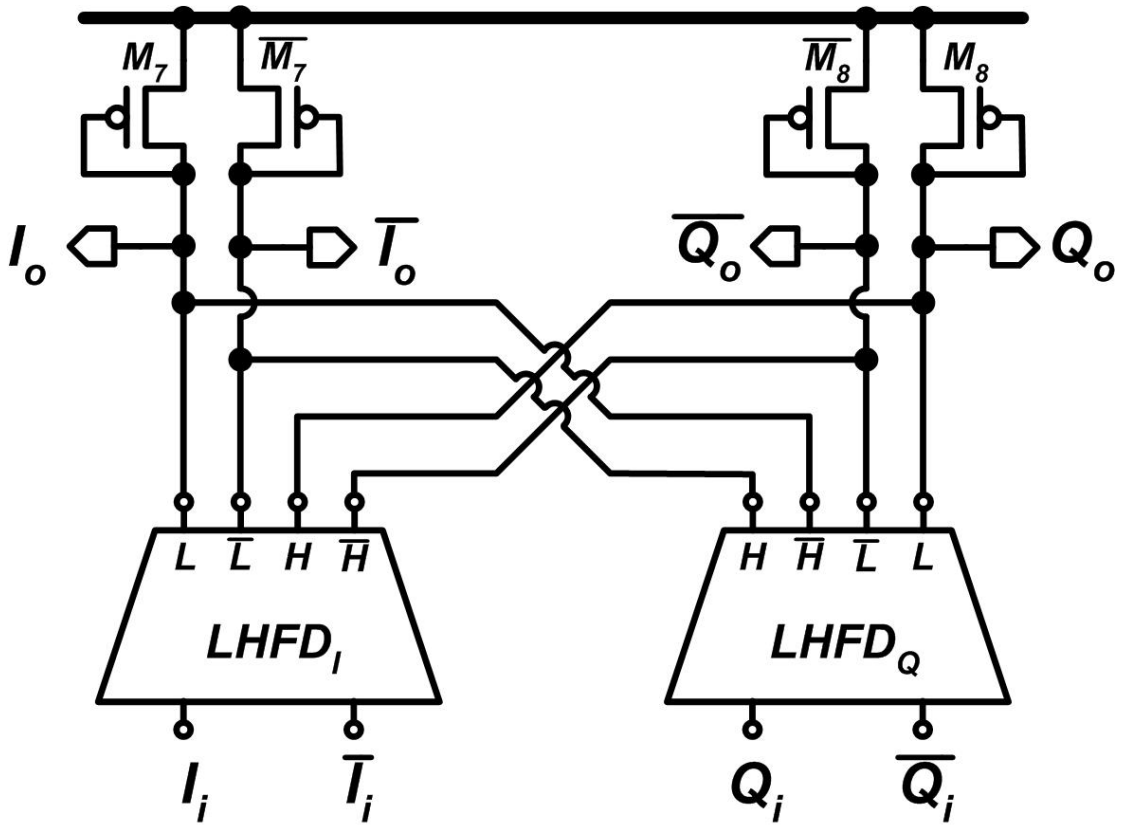
Fig. 2.4 Required stage versus achievable IRR_{PPFN} within the rejection band.


VDD
M7
M8
M4
M3
M2
VOL
VOH
i4
i3
i1
iOL
iOH
VI
M1
A
CC
Cp
iL
iH
Vb
Mb
M6
i5
M5
ML
CH
GND
LHF

(a)


iOL
iOH
LHF
VI
LHF
Vb
Mb
LHFD
L
H
iOL
iOH

(b)



(c)

Fig. 2.5 (a) Circuit of *LHF*. (b) Differential type of *LHF* and its equivalent functionality block *LHFD*. (c) Block diagram of *H(s)*.

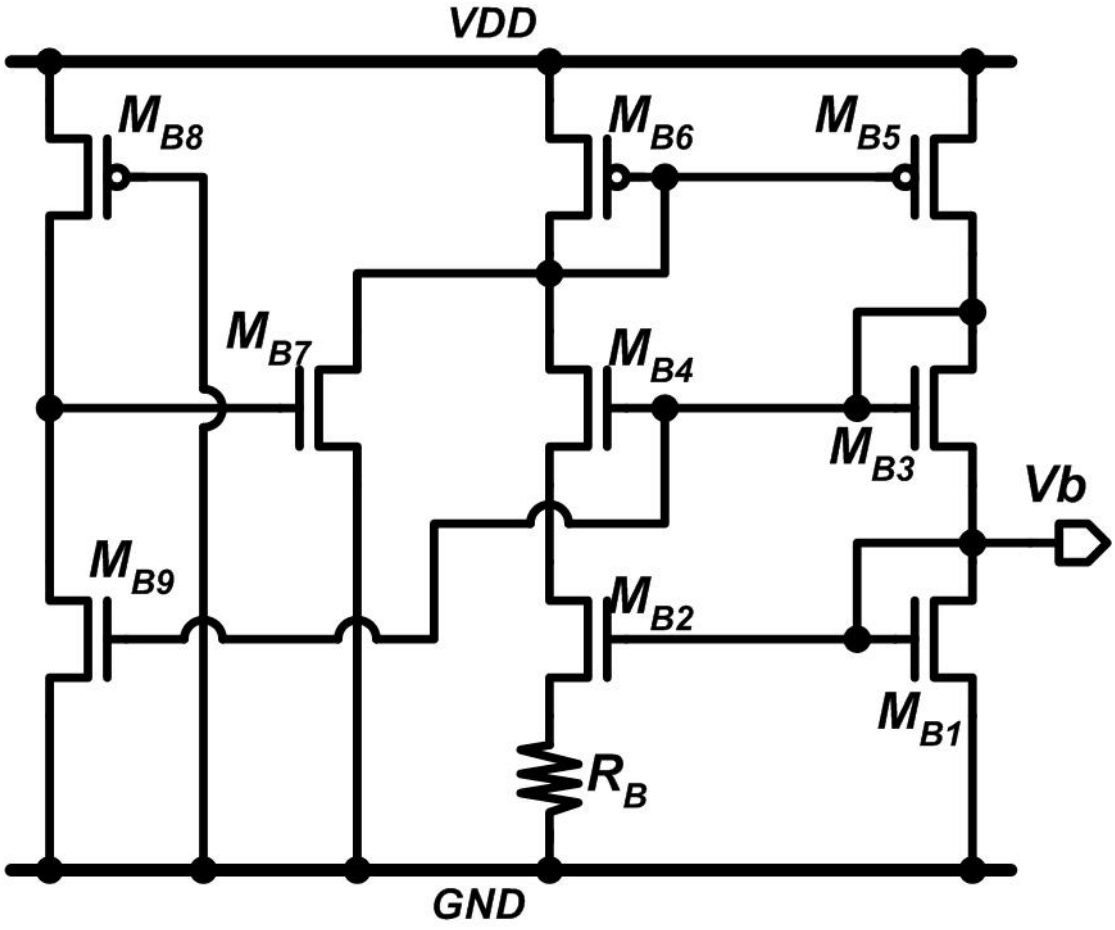


Fig. 2.6 Circuit of constant-gm bias.

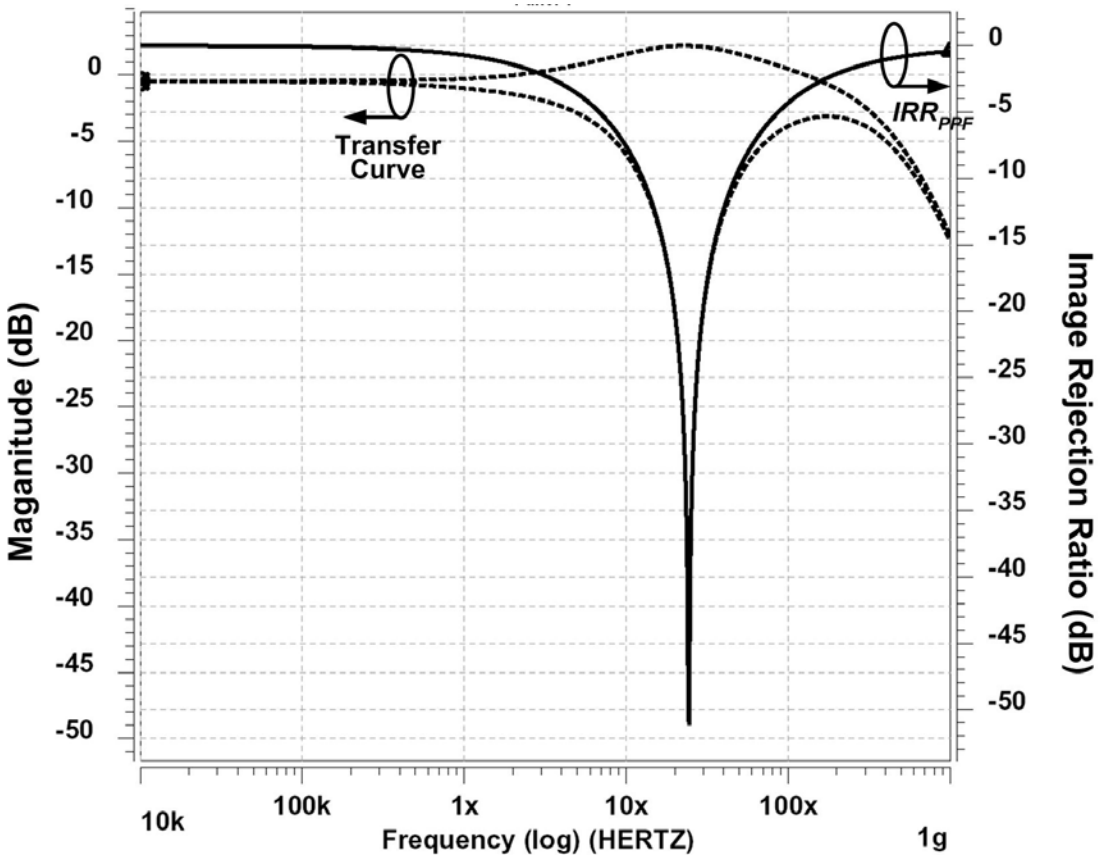


Fig. 2.7 HSPICE simulated transfer curve and IRR_{PPF} of the one-stage CMOS polyphase filter (ω_P=24.5MHz).

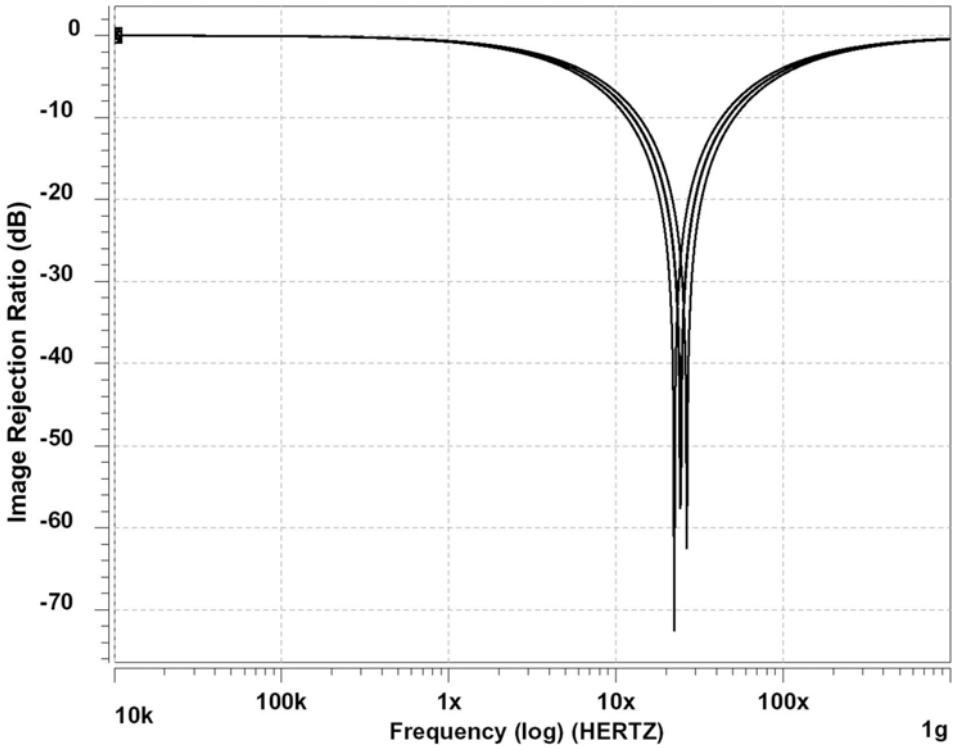


Fig. 2.8 HSPICE simulated *IRR* variations of the one-stage CMOS polyphase filter with four corners (FF, FS, SF, and SS) of MOS device models.

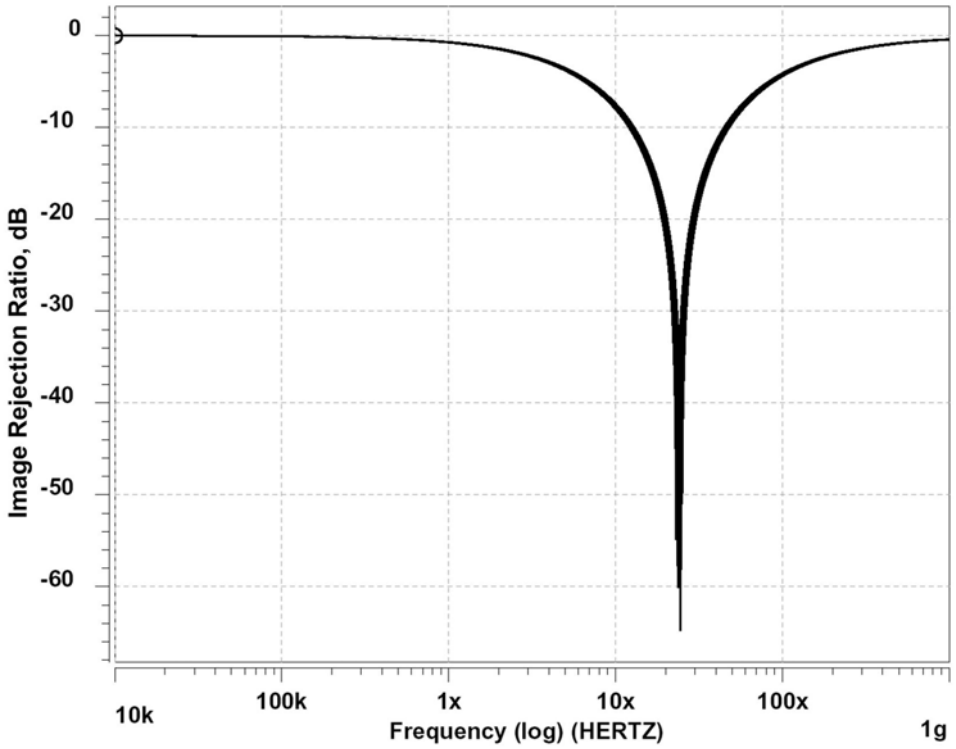


Fig. 2.9 HSPICE simulated *IRR* variations of the one-stage CMOS polyphase filter in the temperature between 0^{o} and 80^{o}.

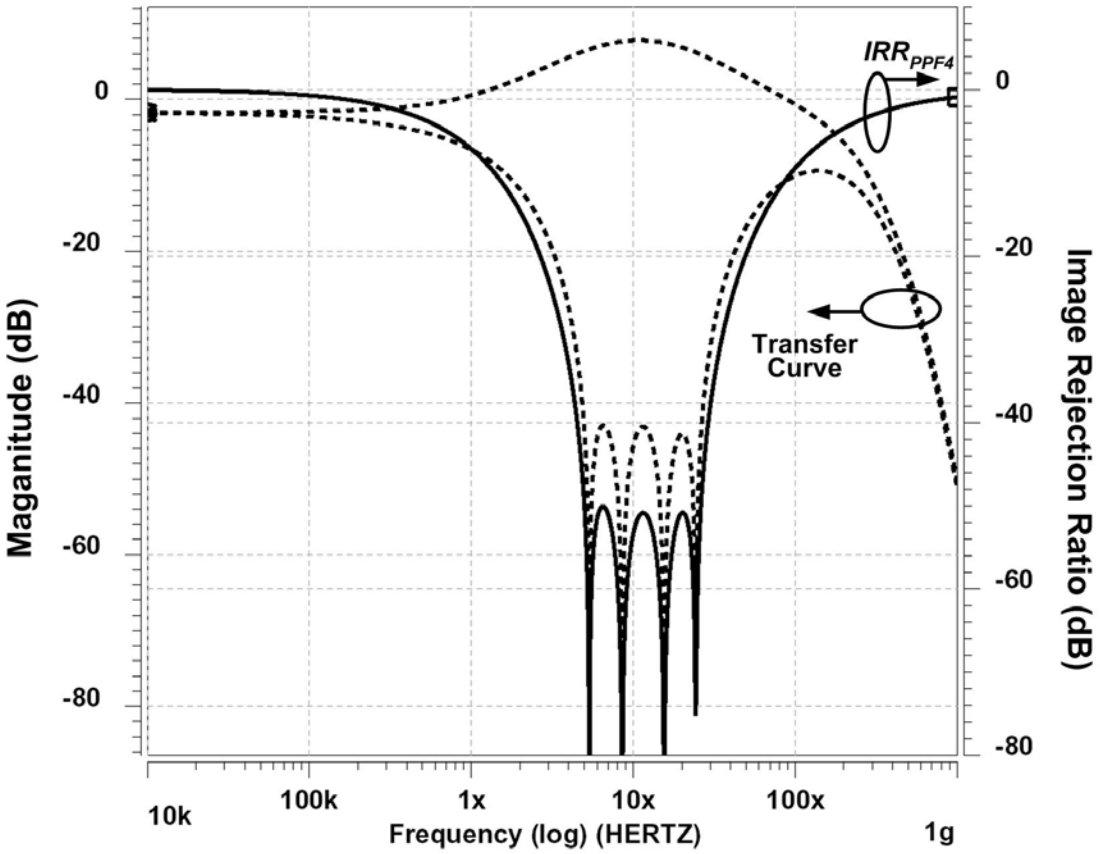


Fig. 2.10 HSPICE simulated transfer curve and IRR_{PPF4} of the four-stage CMOS polyphase filter.

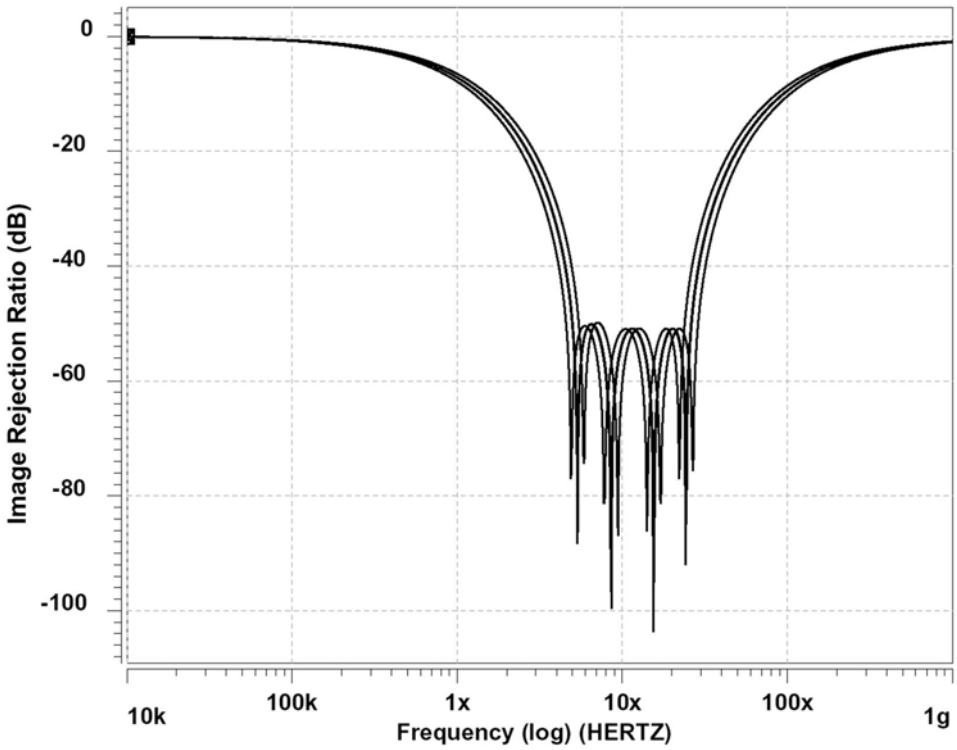


Fig. 2.11 HSPICE simulated *IRR* variations of the four-stage CMOS polyphase filter with four corners (FF, FS, SF, and SS) of MOS device models.

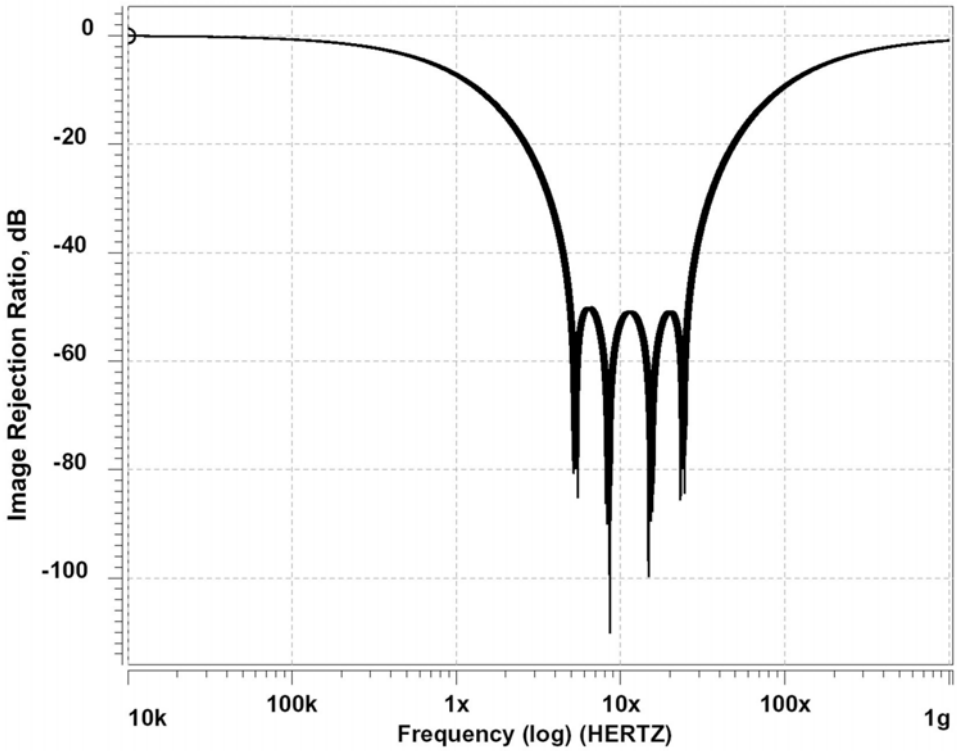


Fig. 2.12 HSPICE simulated *IRR* variations of the four-stage CMOS polyphase filter in the temperature between 0^{o} and 80^{o}.

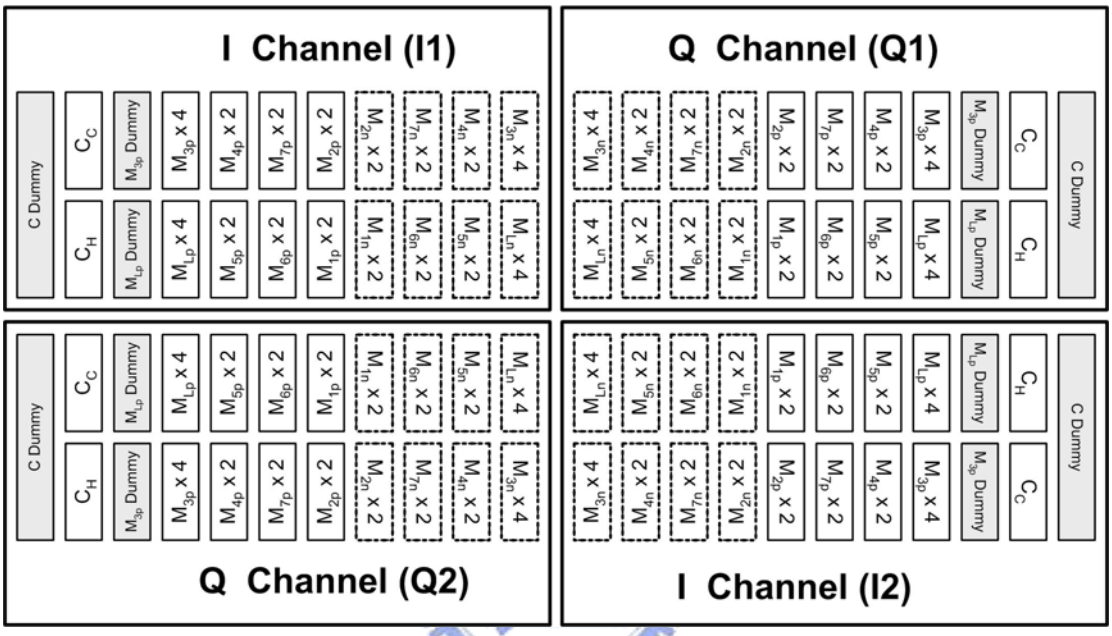


Fig. 2.13 Floor planning of the one-stage polyphase filter.

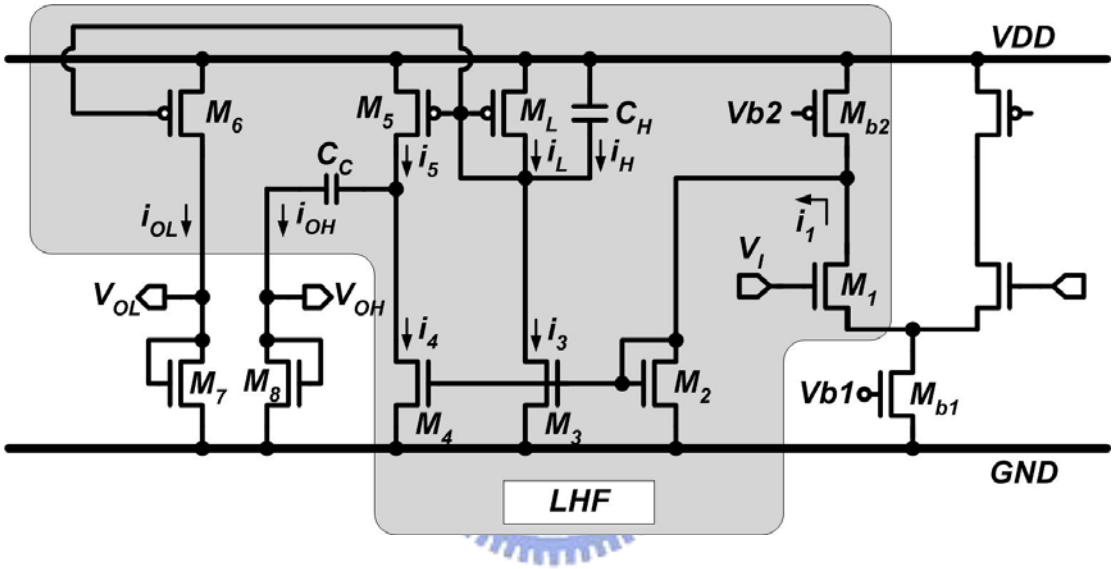


Fig. 2.14 Low-voltage version of *LHF*.

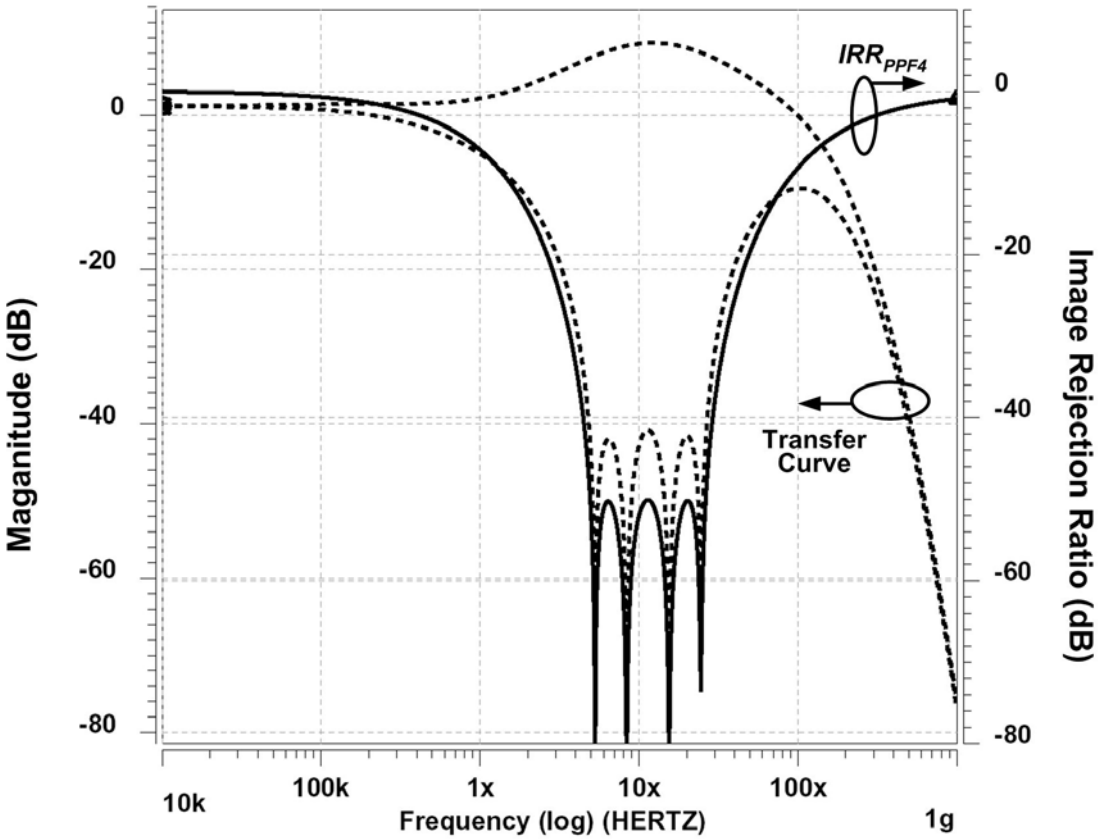


Fig. 2.15 HSPICE simulated transfer curve and IRR_{PPF4} of the low-voltage four-stage CMOS polyphase filter.

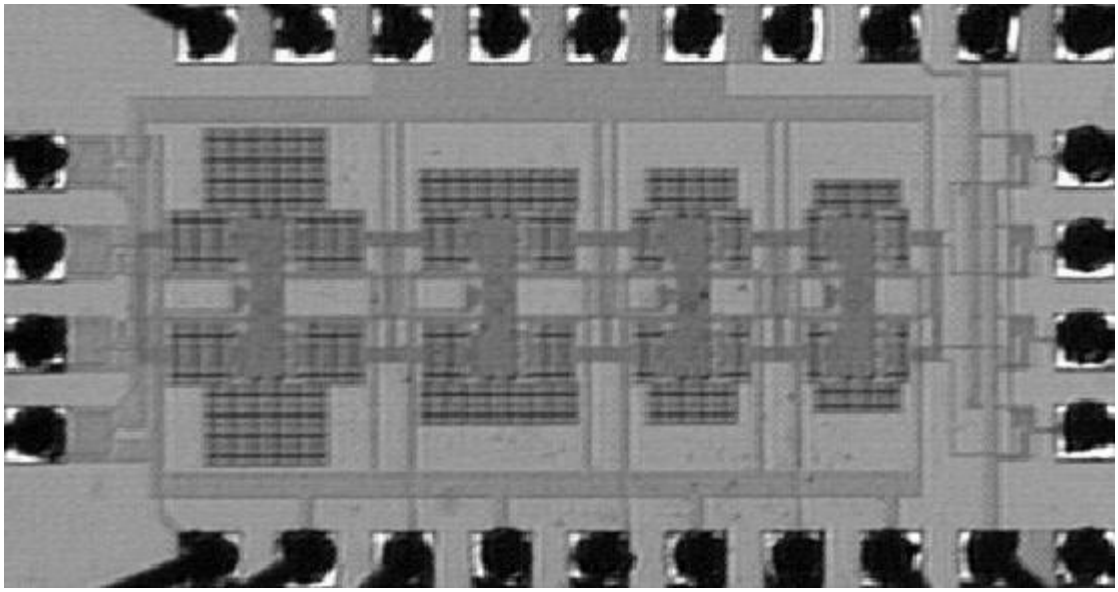


Fig. 2.16 Die micrograph of fabricated four-stage polyphase filter in 0.25-μm CMOS technology.

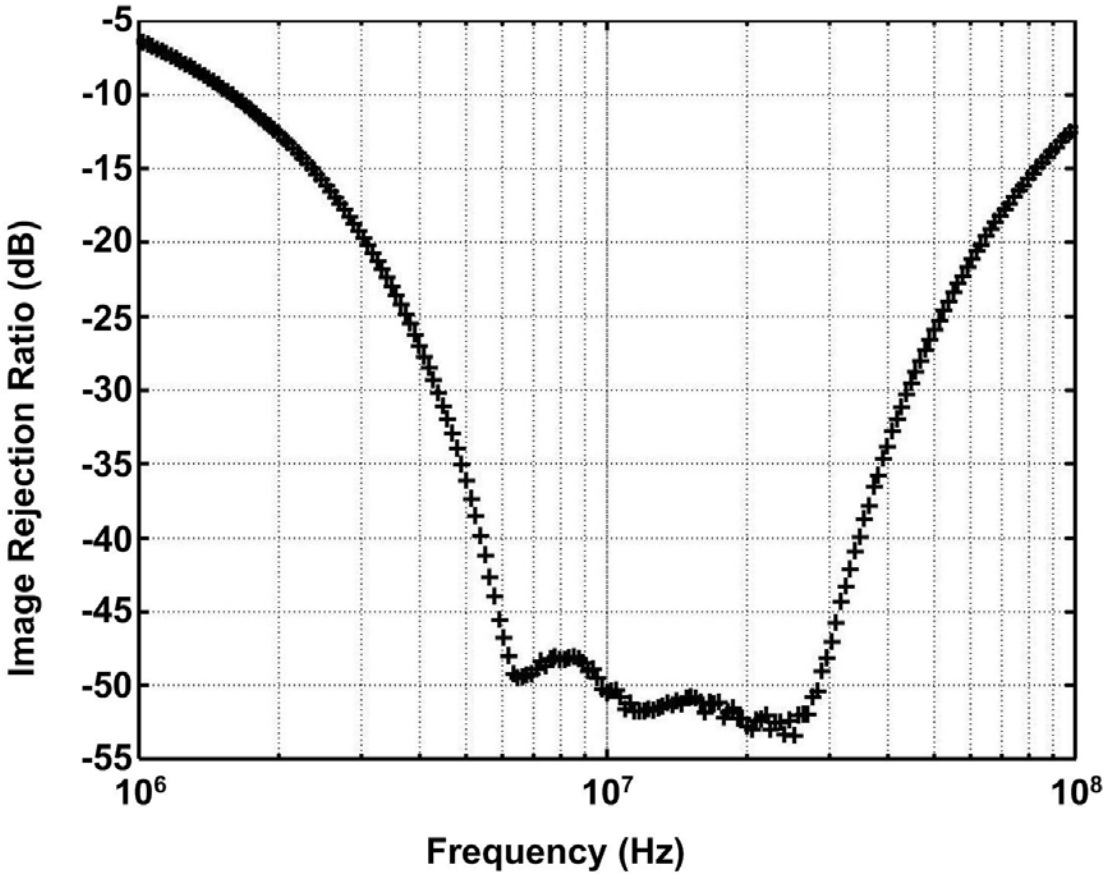


Fig. 2.17 Measured IRR_{PPF4} of fabricated four-stage polyphase filter in 0.25-μm CMOS technology.

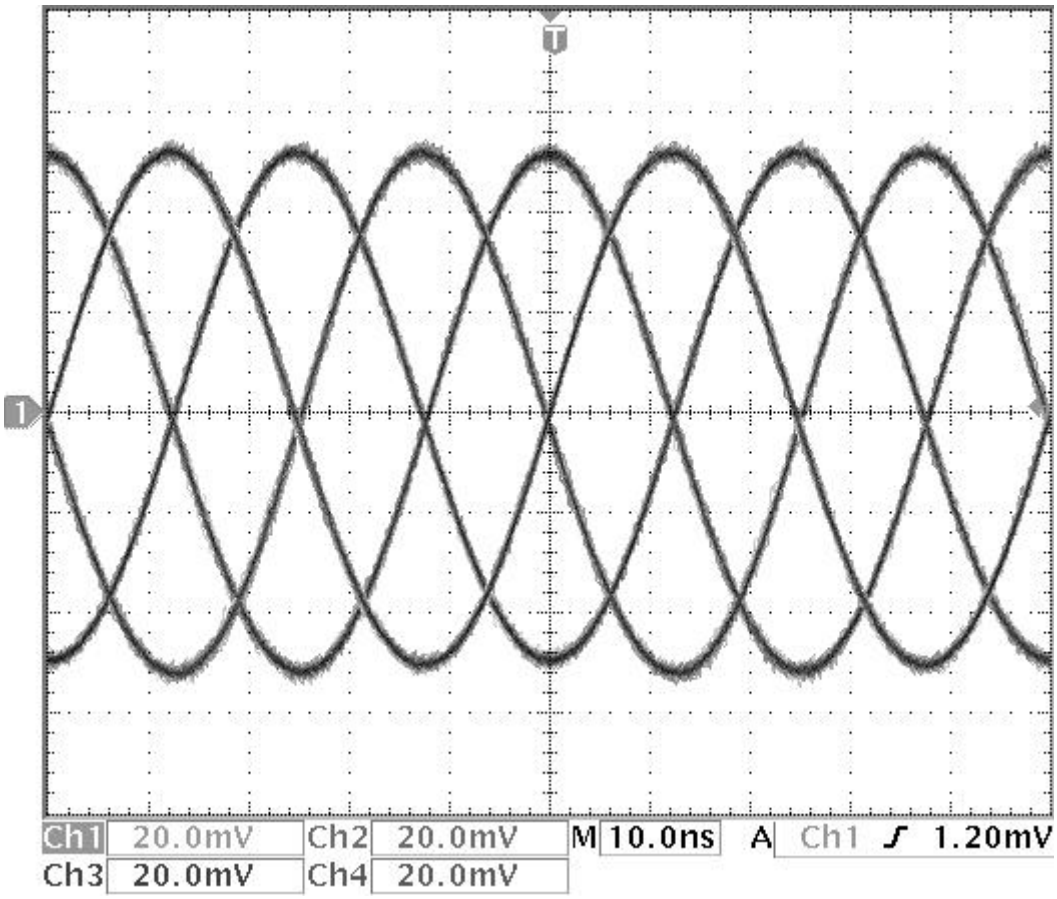


Fig. 2.18 Measured quadrature output signals when 20-MHz differential signals are applied.

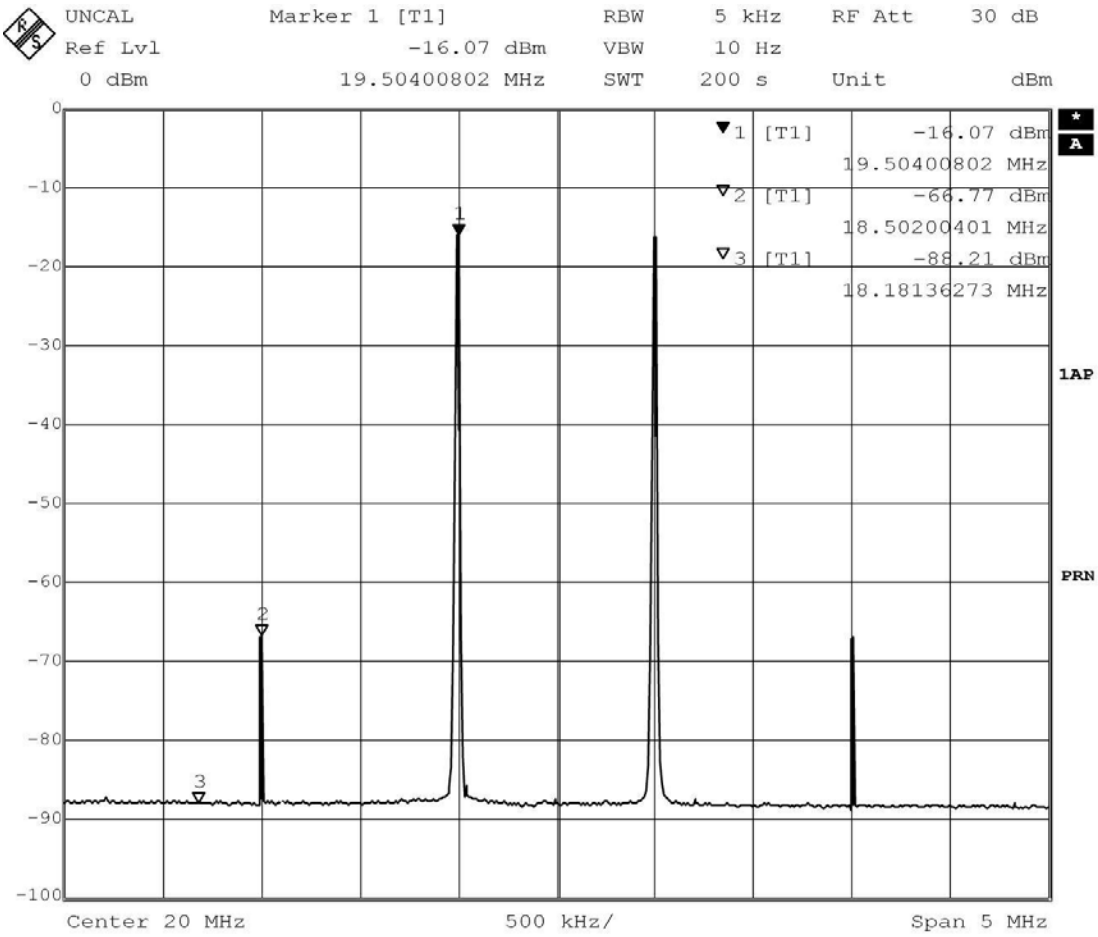


Fig. 2.19 Two-tone test for f_1 = 19.5MHz and f_2 = 20.5MHz.

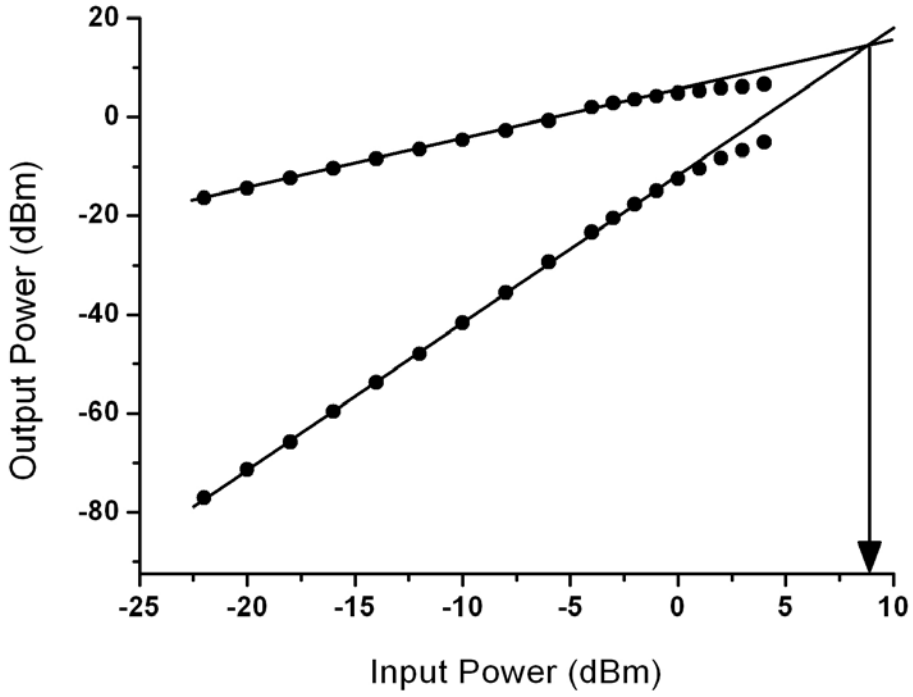


Fig. 2.20 Measured *IIP3* of fabricated four-stage polyphase filter in 0.25-μm CMOS technology.