CHAPTER 3

A 5-GHZ DOUBLE-QUADRATURE RECEIVER FRONT-END FOR IEEE 802.11A WIRELESS LOCAL-AREA NETWORK APPLICATIONS

3.1 INTRODUCTION

Wireless LANs provide wideband wireless connectivity between PCs and other consumer electronic devices, allowing access to core networks and other equipment in corporate, public and home environments. Currently, wireless LANs technology that operates in the 2.4 GHz ISM band is widely used [58]-[67]. However, because of the demand for higher bit rates and the need for a dedicated spectrum, the IEEE 802.11a standard [7], which refers to the 5-GHz, was defined in 1999. Theoretically, the maximum data rate can be achieved up to 54 Mb/s with 64 quadrature amplitude modulation (64-QAM).

The cost of increasing the spectral efficiency according to the IEEE 802.11a standard is a strict requirement on the signal-to-noise ratio (*SNR*). A higher *SNR* results in more stringent demands on image rejection. With reference to reject the image, several skills were used in the recently proposed 5-GHz CMOS wireless LAN transmitter/receiver [68]-[69]. In [68], a tracking notch filter is merged with the *LNA*

to generate low impedance at the frequency of the image. The notch filter improves the image rejection by 16dB. In the receiver structure of [69], the *LNA* rejects the image signal and a higher IF of 1.31GHz is chosen to increase the selectivity.

This chapter proposes a 5-GHz CMOS front-end receiver. Double-quadrature receiver (*DQR*) architecture is used to improve the image rejection performance. The *DQR* comprises a low-noise amplifier (*LNA*), an RF quadrature generator (*RF-QG*), double-quadrature mixers (*DQ-Mixers*), a quadrature voltage-controlled oscillator (*QVCO*) and a polyphase filter. Better image rejection can be achieved because the RF and LO signals are both put into quadrature phases.

In the circuit realization of the *DQR*, a new single-stage frequency-adjustable RLC phase shifter circuit is used to realize *RF-QG*. The single-stage quadrature generator can generate accurate quadrature signals without high power consumption and noise figure degradation. In the *DQ-Mixers* design, low power consumption is an important consideration because a *DQR* comprises four downconversion mixers. A similar current reuse technique [70] is used herein. The power consumption can be reduced significantly by merging the *DQ-Mixers* with *QVCO*. The new circuit proposed in Chapter 2 is used to realize the polyphase filter. The multi-stage structure is also used to increase the frequency bandwidth. For the high gate-impedance property of MOSFETs, the new active polyphase filter prevents the loss of signals and provides the advantages of low power dissipation, a small chip area, and low parasitic sensitivity.

The system requirements for IEEE 802.11a receiver are presented in Section 3.2. Section 0 describes the model for the *DQR* and analyze the image rejection

performance of the *DQR*. Section 3.4 explains the design concepts and the circuit implementations. Section 3.5 presents experimental results concerning the proposed CMOS *DQR*. Finally, conclusions are drawn in Section 3.6.

3.2 SYSTEM DESCRIPTION AND CALCULATIONS

3.2.1 System Description

IEEE 802.11a is a 5-GHz wireless-networking standard, which operates in the 5-GHz band. The physical layer of IEEE 802.11a is based on an Orthogonal Frequency Division Multiplexing (*OFDM*) modulation scheme. The allocated frequency in IEEE 802.11a standard is shown in Fig. 3.1. As seen from Fig. 3.1, the IEEE 802.11a standard specifies operation spectrum over an unlicensed band of 300MHz. In the 300MHz, a contiguous 200MHz portion extends from 5.15GHz to 5.35GHz and a separate 100MHz segment from 5.725GHz to 5.825GHz. The bottom 100MHz domain is limited to a maximum output power of 40mW, the next 100MHz to 200mW, and the top 100MHz to 800mW. Each carrier is 20MHz wide and is subdivided into 52 subcarriers, 48 of these subcarriers are used for data and the remaining 4 subcarriers are reserved for pilot to estimate residual phase error. The spacing of each subcarrier (Δf) is 312.5KHz.

In the operation of IEEE 802.11a wireless LAN, convolution code with one of three code rates (1/2, 2/3, 3/4) is used to reduce the *BER*. Code rate is the ratio of input bits to the output bits of the encoder. After coding, the coded bits are interleaved to prevent error bursts. Then the interleaved coded bits are grouped and modulated with one of four methods, BPSK, QPSK, 16QAM, and 64QAM to generate

modulation symbols. After modulation, the modulated symbols are mapped to the subcarrier of the 64-point *IDFT* to create the *OFDM* symbol. In the 64-point *IDFT* operation, 48 subcarriers are used for modulation symbols and four subcarriers are reserved for pilots. The remaining 12 subcarriers are not used. The output of the *IDFT* is converted to a serial sequence and a guard interval or cyclic prefix is added. Thus, total duration of the single *OFDM* symbol is the sum of the cyclic prefix or guard duration plus the useful symbol duration. After the cyclic prefix has been added, the entire *OFDM* symbol is transmitted across the channel. In the receiver, the data are recovered by performing the inverse operations of the transmitter in reverse order.

The duration of the single *OFDM* symbol defined in the IEEE 802.11a standard is 4μs, i.e. 48 modulation symbols can be transfer in 4μs. Different data rates can be achieved by using the combination of different modulations and code rates. For a *M*-ary modulation, the data rate can be calculated as

$$\left[48CR \cdot \log_2 M\right] / (4\mu) \tag{3.1}$$

where *CR* is the code rate and $\log_2 M$ means the coded bits per subcarrier. Table 3.1 shows the rate-dependant parameters of the IEEE 802.11a standard. As seen from Table 3.1, IEEE 802.11a offers eight different data rates from 6Mbits/s to 54Mbits/s. The selection of the transmission rate is based on channel condition.

3.2.2 System Calculations

3.2.2.A Noise Figure

The noise figure (NF) is an important parameter in designing a wireless receiver. It determines the RF sensitivity of the receiver and can be defined as

$$F = \frac{(S/N)_{IN}}{(S/N)_{OUT}} = \frac{N_{OUT}}{G_A N_{IN}} \tag{3.2}$$

where $(S/N)_{IN}$ and $(S/N)_{OUT}$ are the *SNR* at the input and output of a system, respectively. G_A is the available gain. N_{IN} and N_{OUT} are the received input noise and the total output noise, respectively. The noise facture is a parameter to measure how much the *SNR* degrades as the signal pass through a system. Usually, the noise factor is expressed in decibels and called the noise figure (*NF*). In a wireless communication system, the minimum detectable signal level is defined as sensitivity. Therefore, the maximum tolerated NF of a RF receiver can be calculated by the sensitivity P_{SEN}, bandwidth *BW*, required *SNR* at the output, and the input noise power P_{NOISE}.

$$NF = P_{SEN} - (P_{NOISE} + 10\log_{10} BW) - SNR \tag{3.3}$$

The quantities of P_{SEN}, *BW*, *SNR*, and P_{NOISE} are expressed in dBm, hertz, dB, and dBm/hertz, respectively.

Usually, the required quality of a complete digital communication system is not defined in *SNR* but is defined in the bit error rate (*BER*). *BER* is the percentage of bits that have errors relative to the total number of bits received in a transmission. According to the modulation method used in the communication, the *BER* can be calculated by a function of E_b/N_0. E_b/N_0 means the energy per bit to noise ratio. Then the required E_b/N_0 can be directly translated into a corresponding *SNR* by (3.4)

$$\frac{E_b}{N_0} = \frac{ST}{N_0} = \frac{S}{RN_0} = \frac{S \cdot BW}{RN_0 \cdot BW} = \frac{S}{N}\left(\frac{BW}{R}\right) \tag{3.4}$$

where *T*, *R*, and *BW* are bit time duration, bit rate, and signal bandwidth, respectively.

In the receiver specification of IEEE 802.11a standard, the packet error rate (PER) should be less than 10% at a PSDU length of 1000 bytes for the rate-dependent sensitivities. Therefore, according to the relation $PER=1-(1-BER)^{number\text{-}of\text{-}bits}$, a bit error

rate (*BER*) of 1.3×10^{-5} should be achieved for all specific sensitivities. As described above, an *OFDM* symbol may be formed with different modulation and code rate so the required *SNRs* to achieve the 1.3×10^{-5} *BER* for different modulation and code rate will be unequal. From the relation shown in (3.3), the required noise figure becomes a function of data rate. Table 3.1 lists the required *SNRs* and noise figures in different schemes. Since the required noise figure for each possible data rate is different, a noise figure of 15dB (10dB and 5dB implementation margin) is recommended by IEEE 802.11a standard to accommodate the worst-case situation.

3.2.2.B CP1dB and IIP3

Linearity is the criterion that defines the upper limit for detectable RF input power level of the receiver. The linearity performance of a RF system is usually determined by 1dB compression point (*CP*1*dB*) and input third intercept point (*IIP3*). The *CP*1*dB* is defined as the input level at which the gain has decreased 1dB. The *IIP3* is defined as the input power where the output powers of the fundamental and the third order intermodulation are equal. In many circuits the *IIP3* is beyond the allowed input range, thus the practical method to obtain the *IIP3* is linear extrapolation on measured behavior for small input amplitude. The experiential rule shows that the IIP3 is about 10dBm larger than *CP*1*dB*.

Usually, the required *IIP3* of a communication system can be calculated by the specified intermodulation characteristics in the standard. The intermodulation characteristics will specify a required performance in a two-tone test, i.e. a *BER* shall be met if a wanted signal with power P_S and two interferers with equal power P_{INT} are applied. To achieve the *BER*, a corresponding *SNR* is required and the required *IIP3*

can be calculated by the characteristic shown in Fig. 3.2. In Fig. 3.2, the slops of the fundamental and the third order intermodulation signal *IM3* are one and three, respectively. The difference power between the output wanted signal and the third order intermodulation product shall meet the required *SNR*. ΔP is the difference power between the input wanted signal and the input interferer. The variable X is set as the difference between the required *IIP3* and P_{INT}. Since the slop of the fundamental is one, the variable X in the gray triangle can be calculated by (3.5) and the required *IIP3* is obtained from (3.6).

$$X + \Delta P = 3X - SNR \tag{3.5}$$

$$IIP3 = P_{INT} + X = \frac{SNR}{2} - \frac{P_S}{2} + \frac{3}{2}P_{INT} \tag{3.6}$$

The IEEE 802.11a standard doesn't specify the intermodulation characteristics but specifies that the receiver must be able to achieve 10% *PER* when signals with a maximum input power –30dBm are received. Since the intermodulation characteristics are not specified, the required *IIP3* cannot be calculated directly by (3.6). To determine the required linearity ability of the designed *DQR* receiver, an experiential rule that the 1dB compression point ($CP1dB$) should be 4 dB above the maximum input signal power is used. Based on this approximation, a $CP1dB$ of -26dBm is targeted.

3.2.2.C Image Rejection Ratio

The required image rejection ratio (*IRR*) of the receiver should be calculated by the specified interference performance in the standard. Unfortunately, the interference performance of IEEE 802.11a has not been defined so far. Because the physical layer of HIPERLAN2 and IEEE 802.11a is almost fully compatible, the input blocking

defined in HIPERLAN2 is used to substitute the interference herein. Table 3.2 shows the blocking level defined in HIPERLAN2. Because the intermediate frequency in the designed *DQR* will lower than 500MHz, the image will locate at the frequency range of 4GHz ~ 5.47GHz and the power of image is defined as –30dBm herein. As shown in Fig. 3.3, the required require noise factor that includes the effect of image interferer can be denoted as

$$F_{REQUIRE} = \frac{S_{IN}/N_{IN}}{S_{OUT}/\left(N_{OUT} + IM_{OUT}\right)} \tag{3.7}$$

where $F_{REQUIRE}$ is the required noise factor of the receiver. N_{OUT}, IM_{OUT} denotes powers of noise and image interferer at the output of the receiver, respectively. N_{OUT}, IM_{OUT} can be expressed as (3.8) and (3.9) by definitions of noise factor and image rejection ratio,

$$N_{OUT} = S_{OUT}\frac{F_{CIR}}{S_{IN}/N_{IN}} \tag{3.8}$$

$$IM_{OUT} = S_{OUT}\frac{S_{IN}/IM_{IN}}{IRR} \tag{3.9}$$

where F_{CIR} denotes the noise factor of the receiver where the effect of image is not included. By substituting (3.8) and (3.9) for (3.7), the required *IRR* can be derived as

$$IRR = \left(F_{REQUIRE} - F_{CIR}\right)\frac{S_{IN}/IM_{IN}}{S_{IN}/N_{IN}} \tag{3.10}$$

To achieve a data rate of 54Mbits/s, Fig. 3.4 shows the required *IRR* in different NF_{CIR} (F_{CIR} in decibel). The parameters $F_{REQUIRE}$, S_{IN}, IM_{IN}, and N_{IN} are replaced by 15dB, -65dBm, -30dBm, and -101.89dBm, respectively. As seen from Fig. 3.4, -58.5dB of *IRR* is needed when the NF_{CIR} is 10dB.

3.2.2.D Phase Noise

In practice the LO signal exhibits a phase noise skirt which will down-converts the blockers and adjacent channel signals to the wanted signal. The down-converted blockers and adjacent channel signals degrade the signal's SNR and hence the LO signal needs to perform a low phase noise.

The requirement on adjacent and non-adjacent channel rejections in IEEE 802.11a can be used to calculate the required phase noise performance. As specified from the IEEE 802.11a standard, a wanted signal 3dB above the sensitivity level P_{SEN} must be detectable with a required *SNR* in the presence of an adjacent channel signal P_{ADJ} or a non-adjacent channel signal P_{NONADJ}. Therefore, the phase noise to conform the required -66dBm P_{ADJ} and -50dBm P_{NONADJ} in the 54Mbits/s transmitting rate can be calculated as

$$\begin{aligned} L\{10M\} &\le P_{SEN} + 3dB + P_{ADJ} - SNR - 10\log(BW) \\ &= -65dBm + 3dB + 66dBm - 19dB - 10\log(20MHz) = -88\,dBc/Hz \end{aligned} \quad (3.11)$$

$$\begin{aligned} L\{30M\} &\le P_{SEN} + 3dB + P_{NONADJ} - SNR - 10\log(BW) \\ &= -65dBm + 3dB + 50dBm - 19dB - 10\log(20MHz) = -104\,dBc/Hz \end{aligned} \quad (3.12)$$

The maganitue of blocking signal is another factor in determining the phase noise requirement. The required phase noise to accommodate the blocking signal P_{BLK} can be calculated the same as (3.11) and (3.12). As the out-of-band blockers are strongly attenuated by the antenna and *LNA*, the largest remaining blocking signals are the in-band blockers. As seen from Table 3.2, the in-band blocking signal is -30dBm at an offset frequency of 50MHz. Therefore, the phase noise must be lower than

$$L\{50M\} \le P_{SEN} + 3dB + P_{BLK} - SNR - 10\log(BW)$$
$$= -65dBm + 3dB + 30dBm - 19dB - 10\log(20MHz) = -124\,dBc/Hz \quad (3.13)$$

As seen from (3.11), (3.12), and (3.13), the required phase noise at offset frequencies of 10, 30, and 50 MHz are –88, -104, and –124 dBc/Hz, respectively. It is more relaxed compared to the *IRR* requirement in IEEE 802.11a receiver. Therefore, double quadrature architecture is chosen in the thesis to achieve a better *IRR* for wireless LAN applications.

3.3 MODEL FOR THE DOUBLE-QUADRATURE RECEIVER

Fig. 3.5 shows the structure of the double-quadrature receiver, in which polyphase filters are used in I/Q paths. The difference between the *DQR* and the conventional low-IF receiver is that, after the *LNA* has amplified the RF input signal, the *RF-QG* transforms this into the in-phase and quadrature-phase signals RF_I and RF_Q. Both RF_I and RF_Q signals are sent to the *DQ-Mixers*, along with the input quadrature signals LO_I and LO_Q from the *QVCO*, to realize the complex multiplication function $IF_I + jIF_Q = (RF_I - jRF_Q)\cdot(LO_I + jLO_Q)$ and generate the intermediate frequency signals IF_I and IF_Q. The polyphase filters are used to filter the image signals at the intermediate frequency to prevent interference with the desired signals.

Using the complex signal representation [35], I/Q signals can be represented as a single complex signal $S(\omega)$:

$$S(\omega) = I + j\cdot Q = A\cos(\omega t) + j\cdot A\sin(\omega t) = A\cdot e^{j\omega t} \quad (3.14)$$

where A and ω represent the amplitude and frequency of I/Q signals, respectively. The spectrum of $S(\omega)$ results in a single tone in the positive frequency ω. If the phases are

not exact quadrature or the amplitudes are not identical in I/Q paths, (3.14) can be represented as

$$S(\omega) = A\cdot[\cos(\frac{\Delta\phi}{2}) + j\frac{\Delta A}{2A}\cdot\sin(\frac{\Delta\phi}{2})]\cdot e^{j\omega t} + A\cdot[\frac{\Delta A}{2A}\cdot\cos(\frac{\Delta\phi}{2}) - j\sin(\frac{\Delta\phi}{2})]\cdot e^{j(-\omega)t} \quad (3.15)$$

where ΔA and $\Delta\phi$ are the amplitude unbalance and the phase error of the I/Q signals, respectively. As shown in (3.15), the signal amplitude at ω will be change and a crosstalk image signal at $-\omega$ will be induced. The image signal caused by mismatches in I/Q paths will interfere the desired signal after frequency translation and thus decrease the *SNR*.

Fig. 3.6(a) and (b) display the signal spectra in the *DQR* before and after downconversion, respectively. $SIGn_{RF}$ and IMn_{RF} in Fig. 3.6(a) refer to the spectra of the desired signals and the image signals at the output of the quadrature generator, respectively. *LOp* refers to the spectrum of the quadrature local oscillation signals. $SIGp_{RF}$, IMp_{RF} and *LOn* represent the crosstalk image signals of $SIGn_{RF}$, IMn_{RF} and *LOp*, respectively. The image-to-signal ratio (*ISR*) of the quadrature generator $SIGp_{RF}/SIGn_{RF}$ (or IMp_{RF}/IMn_{RF}) and *ISR* of the quadrature local oscillator *LOn*/*LOp* can be calculated by the corresponding phase and amplitude mismatches [35]. After the frequency translation, as shown in Fig. 3.6(b), the $SIGp_{RF}$, $SIGn_{RF}$, IMp_{RF} and IMn_{RF} are downconverted to $SIGn_{IF}$, $SIGp_{IF}$, IMp_{IF} and IMn_{IF}, respectively. The image IMp_{IF} mixes with $SIGp_{IF}$ at ω_{IF} and cannot be removed by the following polyphase filters. The value of IMp_{IF} can be represented as

$$IMp_{IF} = IMn_{RF}LOp\left(ISR_{QG}ISR_{LO} + ISR_{Mixers}\right) \quad (3.16)$$

where ISR_{QG}, ISR_{LO} and ISR_{Mixers} denote the *ISR* of the quadrature generator, the local oscillator and mixers, respectively. For ISR_{QG}, ISR_{LO} and ISR_{Mixers} << 1, the $ISR_{QG}ISR_{LO}$ term in (3.16) is negligible relative to ISR_{Mixers}. Therefore, IMp_{IF} is

determined by the gain/phase errors of the mixers and $IMn_{RF}Lop$. The *DQR* exhibits better image rejection performance than the conventional low-IF receiver, because IMp_{IF} is smaller and almost unaffected by ISR_{LO}.

The image IMn_{IF}, which is downconverted from IMn_{RF}, is located at $-\omega_{IF}$ whereas the desired signal $SIGp_{IF}$ is at ω_{IF}. The polyphase filters should reject IMn_{IF} at $-\omega_{IF}$ to prevent interference with the $SIGp_{IF}$. If the multistage polyphase filter can provide an image rejection ratio IRR_{PPFN}, then the total image rejection ratio IRR_{DQR} of the *DQR* can be derived by using (3.16), and the relations $IMn_{IF}=IMn_{RF}LOp$, $SIGp_{IF}=SIGn_{RF}Lop$ and $SIGn_{IF}=SIGn_{RF}LOp(ISR_{QG}ISR_{LO}+ISR_{Mixers})$. Neglecting the high-order terms yields,

$$\begin{aligned} IRR_{DQR} &\equiv \frac{(IMp_{IF} + IMn_{IF}IRR_{PPFN})/(SIGp_{IF} + SIGn_{IF}IRR_{PPFN})}{IMn_{RF}/SIGn_{RF}} \\ &= \frac{ISR_{QG}ISR_{LO} + ISR_{Mixers} + IRR_{PPFN}}{1+(ISR_{QG}ISR_{LO} + ISR_{Mixers})IRR_{PPFN}} \\ &\cong ISR_{QG}ISR_{LO} + ISR_{Mixers} + IRR_{PPFN} \end{aligned} \tag{3.17}$$

As may be seen from (3.17), the overall image rejection ratio of the *DQR* is determined mainly by the image-to-signal ratio of the mixers and the image rejection ratio of the polyphase filter because the $ISR_{QG}ISR_{LO}$ is relatively small. To achieve high IRR_{DQR}, the symmetry of the layout in mixers between I/Q paths should be regarded as reducing the amplitude of crosstalk image signals. Additionally, the polyphase filter must have a high capacity for rejecting images at intermediate frequencies.

3.4 CIRCUIT DESIGNS

3.4.1 Low-Noise Amplifier (*LNA*)

LNA is the first circuit in the receiver front-end. The functions of *LNA* not only amplify RF signals but also contribute as minimal noise as possible to enlarge the power difference between the received signal and noise. Considering the noise contributions in *LNA* design, channel thermal noise and induced gate current noise are the main sources of noise in the MOS device [72]-[75]. The thermal noise occurs because of channel resistance, the gate current noise results from the fluctuating channel charge and then induces a physical current towards the gate by capacitive coupling.

The inductive source degeneration architecture is used in the *LNA* design. By the comparison in [75], the architecture offers the possibility to achieve the best noise performance. In the inductive source degeneration architecture, two inductors connected at the gate and source of the input transistor. The *LNA* generates real term input impedance and can be used for 50Ω input matching. Choosing a suitable dimension of the input transistor can optimize the noise figure. Targeting at the power dissipation of 3mW and using process parameters in TSMC 018-μm CMOS technology, the simulated gate-width versus noise figure is shown in Fig. 3.7. As seen from Fig. 3.7, a better noise figure can be achieved by using the gate-width of 60μm~90μm. In this design, 65μm/0.18μm is determined as the dimension of input transistor.

In the design of LNA, the transconductance of the input transistor and the load

impedance dominate the voltage gain. Since the transconductance of input transistor is determined for noise optimization, sufficient load impedance should be provided by the LC-tank to achieve the gain. Besides, to avoid the miller effect in the input transistor and enhance reverse isolation, cascoded structure is chosen in the *LNA* design.

The *LNA* circuit of the proposed 5-GHz *DQR* is shown in Fig. 3.8. A fully differential scheme is used for rejecting noises from the power supply and ground. As seen from Fig. 3.8, M_1 and M_2 are the input transistors, which dimensions are optimized for minimum noise figure. L_{g1}, L_{g2}, L_{s1}, L_{s2}, and capacitors at the gates of M_1 and M_2 match the 50Ω input impedance for maximum power transfer. Cascoded transistors M_3 and M_4 are used for reverse isolation. Parasitic capacitors at *RF*, $\overline{RF}$ and L_{d1}, L_{d2} realize the LC-tanks whose resonate frequencies are tuned to 5.2GHz. A capacitor C_{bp} is connected from gates of M_3 and M_4 to ground to improve common mode noise rejection. L_{d1}, L_{d2}, L_{s1} and L_{s2} are realized by on-chip spiral inductors and L_{g1} and L_{g2} are realized by bounding wires. The device parameters of the *LNA* are listed in Table 3.3.

3.4.2 RF Quadrature Generator (*RF-QG*)

In the *DQR*, the RF signal is transformed into in-phase and quadrature-phase signals by the *RF-QG*. In this design, a single-stage frequency-adjustable RLC phase shifter is used to implement the *RF-QG*.

The conceptual circuit of proposed RLC phase shifter is shown in Fig. 3.9. The relationship between the input and output of RLC phase shifter can be derived as

$$RF_Q = RF_I \cdot \left[Z_C / \left(Z_R + Z_L + Z_C \right) \right] = RF_I \cdot K_{EQ} \cdot \exp\left(j\theta_{EQ} \right) \tag{3.18}$$

$$K_{EQ} = 1 \Big/ \sqrt{\left(\omega^2 LC - 1 \right)^2 + \left(\omega RC \right)^2} \tag{3.19}$$

$$\theta_{EQ} = -\left(\pi / 2 \right) - \tan^{-1} \left\{ \left[\omega L - \left(\omega C \right)^{-1} \right] \Big/ R \right\} \tag{3.20}$$

where RF_I and RF_Q are the input and output signals of the RLC circuit, respectively. Z_R, Z_L, and Z_C are the impedances of components R, L, and C, respectively. K_{EQ} represents the amplitude ratio at nodes RF_I and RF_Q. θ_{EQ} represents the shifted phase at node RF_Q. As seen from (3.19) and (3.20), θ_{EQ} equals to -(π/2) when $|Z_L| = |Z_C|$ and K_{EQ} equals to 1 when $|Z_L| = |Z_C| = |Z_R|$. Therefore, an ideal quadrature signal RF_Q can be generated when (3.21) is satisfied.

$$\omega L = \frac{1}{\omega C} = R \quad \Rightarrow \quad \omega = \frac{1}{\sqrt{LC}}, R = \sqrt{\frac{L}{C}} \tag{3.21}$$

Since the impedance Z_L, and Z_C vary with the frequency, an adjustable capacitor is needed to generate the quadrature phase at different frequency. In this design, a varactor is used to realize the capacitor. The capacitance of the varactor can be adjusted to compensate for the varying impedance of the inductor at different frequency. Compared with the passive RC network, a single-stage RLC phase shifter is satisfactory and it can avoid high power consumption and noise figure degradation.

Fig. 3.10 shows the circuit of the proposed *RF-QG*. M_1 and M_2 are used to isolate the effect of the impedance loading from the phase shifter to prevent the gain degradation of the *LNA*. L_{PS} is realized by the spiral inductor. The P+/N-well junction capacitor is used to implement the varactor C_{PS} and its capacitance can be adjusted by changing the voltage *VC*. In the required band of IEEE 802.11a, i.e. 300MHz, the spiral model can be represented as an inductor L_{PS} in series with a parasitic resistor R_P.

The sum of resistances R_P and R_{PS} realizes the required resistance. In this design, the simulated gain of the quadrature generator is 0dB. The simulation also verifies that the single-stage circuit can avoid the heavy noise figure degradation because this circuit only increases the noise figure by 0.5dB. The device parameters of the *RF-QG* are listed in Table 3.3.

Fig. 3.11 shows the simulated amplitude errors and *ISR* at the outputs of the quadrature generator. By adjusting the control voltage *VC* in Fig. 3.10 from 0.9V to 1.8V, the exact quadrature phase can be obtained. As seen from Fig. 3.11, the amplitude error varies from 0.17dB to –0.14dB in the frequency range from 5.14GHz to 5.39GHz. The amplitude error increases near the edge of the band because the resistance of R_{PS} is fixed but the impedance of inductor varies with frequency. To avoid a large *ISR* degradation caused at one of the band edges, the best *ISR* is achieved when the *VC* is set at the center of the tuning voltage. The simulation result shows the *ISR* of the *RF-QG* can exceed -40dB within 5.14GHz~5.39 GHz.

The effects of component mismatch is verified by 30-times of Monte Carlo simulations. The variations of transistor parameters ΔW (channel width), ΔL (channel length) and $\Delta V_{th(p,n)}$ (threshold voltage) are randomly distributed according to the values provided by the corner parameters of the MOS device model. The relative variations of capacitance and resistances are ±10%. The simulation results in an *ISR* distribution from -65dB to -40dB at 5.25GHz.

3.4.3 Double-Quadrature Mixers (*DQ-Mixers*) and Quadrature Voltage-Controlled Oscillator (*QVCO*)

Fig. 3.12 shows a circuit diagram, which combines the functions of *Mixer1* and *Mixer3* in Fig. 3.5. As seen from Fig. 3.12, the IF_I and $\overline{IF_I}$ represent the differential IF signal in I path. The gates and sources of transistors are connected to quadrature RF and LO signals, respectively. By using the ideal square-law, the function of the circuit can be derived as

$$\begin{aligned} IF_I - \overline{IF_I} &= R\cdot\left(I_1+I_2+I_3+I_4-I_5-I_6-I_7-I_8\right) \\ &= R\cdot K\cdot\begin{bmatrix} \left(RF_I-\overline{LO_I}+\Delta V_{dc}\right)^2+\left(\overline{RF_I}-LO_I+\Delta V_{dc}\right)^2 \\ +\left(RF_Q-\overline{LO_Q}+\Delta V_{dc}\right)^2+\left(\overline{RF_Q}-LO_Q+\Delta V_{dc}\right)^2 \\ -\left(\overline{RF_I}-\overline{LO_I}+\Delta V_{dc}\right)^2-\left(RF_I-LO_I+\Delta V_{dc}\right)^2 \\ -\left(\overline{RF_Q}-\overline{LO_Q}+\Delta V_{dc}\right)^2-\left(RF_Q-LO_Q+\Delta V_{dc}\right)^2 \end{bmatrix} \\ &= 8R\cdot K\cdot\left(RF_I LO_I+RF_Q LO_Q\right) \end{aligned} \tag{3.22}$$

where $K=0.5\cdot\mu_0 C_{ox}(W/L)$ and $\Delta V_{dc}=VDC_G-VDC_S-V_{th}$. VDC_G and VDC_S denote the dc voltage at the gate and source of the transistors, respectively. However, because short-channel transistors are usually used in RF design for high unit-gain frequency, (3.22) must be reexamined and revised by considering short-channel effects. Considering the mobility degradation and velocity saturation, the drain current I_D in MOSFETs is expressed as,

$$I_D = WC_{ox}v_{sat}\frac{\left(V_{GS}-V_{Th}\right)^2}{V_{GS}-V_{Th}+2\left(v_{sat}L/u_{eff}\right)} \tag{3.23}$$

$$u_{eff}=\frac{u_0}{1+\gamma\left(V_{GS}-V_{Th}\right)} \tag{3.24}$$

where v_{sat} is the saturated velocity; u_0 represents the "low-field" mobility, and γ is a fitting parameter that is approximately $(10^{-7}/t_{ox})$ V^{-1} [70]. If the overdrive voltage

V_{GS}-V_{Th} is sufficiently small, (3.23) can be rewritten as (3.25) by substituting (3.24) into (3.23).

$$I_D = \frac{1}{2}u_0 C_{ox}\frac{W}{L}\cdot\frac{(V_{GS}-V_{Th})^2}{1+\left(\frac{u_0}{2v_{sat}L}+\gamma\right)(V_{GS}-V_{Th})}$$
$$\approx \frac{1}{2}u_0 C_{ox}\frac{W}{L}\cdot\left[1-\left(\frac{u_0}{2v_{sat}L}+\gamma\right)(V_{GS}-V_{Th})\right](V_{GS}-V_{Th})^2 \quad (3.25)$$

Using (3.25), (3.22) can be revised as

$$IF_I - \overline{IF_I} = 8R(K-3K'\Delta V_{dc})(RF_I LO_I + RF_Q LO_Q) \quad (3.26)$$

where $K'=K\cdot[(\mu_0/2v_{sat}L)+\gamma]$. The result verifies that the circuit can realize the mixing function even when short-channel devices are used. The IF_Q in Fig. 3.5 can be generated by replacing RF_I, RF_Q, LO_I and LO_Q in Fig. 3.12 with RF_I, $-RF_Q$, LO_Q and LO_I, respectively.

In the frequency translation, all transistors in the *DQ-Mixers* are operated in saturation region. The input *LO* and *RF* signal are both sinusoidal waves and the outputs of *DQ-Mixers* will be the product of two sinusoidal signals. The multiplying operation achieves a more linear and low distortion output signals compared to the switching operation in the Gilbert mixer. The linear *DQ-Mixers* relax the filtering requirement of the following stages. Besides, the small voltage drop will make it suitable in the low voltage design.

In Fig. 3.13, a circuit structure based on the even-stage ring oscillator is used to implement the integrated *QVCO*. The inductors L_1 and L_2 are realized by on-chip spiral inductors and the varactors C_1~C_4 are realized by P+/N-well junction capacitors. The cross-coupled transistors M_9~M_{12} generate negative transconductances to cancel the resistances at the outputs and guarantee oscillation. The varactors, which are tuned

by the control voltage *VC*, are used to obtain the desired oscillation frequency. The fully differential inverters are used to maintain quadrature outputs. The symmetry of layout topologies must be considered carefully to ensure accurate output phases. Using Monte Carlo simulations on *QVCO* circuit and repeating it 30 times, the effects of the tank mismatch are verified. The variation in the quality factor of inductor is set as ±3. The simulation result shows that the variations of gain and phase error are 0.086 ~ 0.5 dB and –0.9 ~ 0.6 degree, i.e. the worst *ISR* of the *QVCO* is 30dB.

This design uses a current reuse structure, which is shown in Fig. 3.14. The *QVCO* is cascoded with the *DQ-Mixers* to reuse current and hence reduce the power dissipation. The simulated phase noises of the *LO* signal are –124.8, -134, and -137 dBc at offset frequencies of 10, 30, and 50 MHz, respectively. The device parameters of the *DQ-Mixers* and *QVCO* are listed in Table 3.3.

3.4.4 Active Polyphase Filter

The method proposed in Chapter 2 is used to realize the required broadband active polyphase filter, excepting a resister R_L is paralleled with M_7 (M_8) for adjusting the DC voltage to bias the next stage. According to Fig. 2.4, four stages are required to achieve –60dB IRR_{PPF4} within the band from 15MHz~45MHz. Therefore, four one-stage active polyphase filters shown in Fig. 3.15 are cascaded in this design and their rejected frequencies are 16MHz, 22MHz, 34MHz, and 45MHz, respectively. Power-consuming buffers are not required between pairs of stages because the high input impedance in each stage. For measurement purpose, two buffers are connected at the output of I/Q paths to drive the 50Ω equipment input impedance.

HSPICE are performed to verify the performance of four-stage active polyphase

filter. Fig. 3.17 shows the simulated transfer curve at positive and negative frequencies and the image rejection ratio IRR_{PPF4} of the polyphase filter. It is shown that the IRR_{PPF4} can exceed -60dB by the four-stage polyphase filter over the bandwidth 15.3MHz~47.7MHz. The voltage gain at 20MHz is 2.7dB.

The simulation results for verifying the effects of process and temperature variations are shown in Fig. 3.17 and Fig. 3.18, respectively. As seen from Fig. 3.17, the IRR_{PPF4} can exceed -60dB over the range of 15.9MHz~45.2MHz under the four corners of the MOS device models. As the temperature varies from 0^o to 80^o, Fig. 3.18 shows that an IRR_{PPF4} of -60dB can also be achieved within 15.9MHz to 44.9MHz. The simulation results show that the performance of the four-stage polyphase filter can be well controlled as the process and temperature are varied. The device parameters of the active polyphase filter are listed in Table 3.3.

3.4.5 Overall Circuit

The complete circuit of the proposed 5-GHz double-quadrature receiver is shown in Fig. 3.19. As may be seen from Fig. 3.19, the RF differential signals RF_{in} and $\overline{RF}_{in}$ are applied to the input nodes of the *LNA*. The *LNA* amplifies the differential RF signals and its outputs are connected to the *RF-QG* through dc-blocking capacitors. By adjusting the control voltage *VC* in the *RF-QG*, the required quadrature signals RF_I, $\overline{RF}_I$, RF_Q and $\overline{RF}_Q$ can be generated by the RLC phase shifter and then ac-coupled to *DQ-Mixers*. The *DQ-Mixers* in I/Q channels cascode with *QVCO* for sharing the dc current. Functions of $RF_ILO_I+RF_QLO_Q$ and $RF_ILO_Q-RF_QLO_I$ are performed in *DQ-Mixers* for I and Q channels, respectively. After frequency translating, the RF signals are down-converted to the IF frequency of 20 ~ 40 MHz.

The four-stage active polyphase filter which provides –60dB of *IRR* is connected after the *DQ-Mixers* to reject image signals. In the four-stage polyphase filter, a constant-gm bias circuit is used to reduce the effect of process and temperature variations. For measurement purposes, four output buffers with source-follower structure are connected after the polyphase filter to drive the load of equipments.

Since the double-quadrature architecture is insensitive to I/Q mismatches, regardless of the mismatch in *DQ-Mixers*, the image-reject ability of the polyphase filter will determine the *IRR* of the *DQR*. Thus, ideally, –60dB of *IRR* within channel bandwidth can be achieved by the designed 5-GHz *DQR*.

3.5 EXPERIMENTAL RESULTS

The 5-GHz *DQR* was designed and fabricated in 0.18-um CMOS technology. Fig. 3.20 shows the die micrograph. The chip consumes 22.4mW at a power supply of 1.8V, and occupies a die area of $2\times1.5mm^2$. Eight 2.5-turn, on-chip spiral inductors with an inductance of 2.63nH are used. All the resistors are implemented by n+ ploysilicon to provide more stable resistance; all linear capacitors are metal-insulator-metal capacitors.

In the measurement set-up, a single-ended RF signal from a signal generator is converted into a differential signal by a 5-GHz balun. The off-chip matching of the *LNA* is implemented by two parallel 50Ω transmission lines and a 0.2pF off-chip floating capacitor. The transmission lines are 1.65mm wide on the 0.8mm FR-4 board. An off-chip transformer is used to transform the differential output signal into a single-ended one. The overall loss caused by the cables, baluns, and transformers are

10.7dB, which will be compensated in the measurement results. Agilent E3615A, which can achieve a resolution of 10mV, is used to provide the required voltage. Besides, all external bias voltages are stabilized by regulators and the magnitudes are adjusted by variable resistors. The regulators can reject noise from the power supply and the variable resistors will provide accurate biases by dividing the supplied voltage.

The measured S_{11}, shown in Fig. 3.21, is –30.1dB at 5.11GHz, and remains lower than -10dB from 4.83GHz to 5.4GHz. The measured overall noise figure is 8.5dB at 5.2GHz. Fig. 3.22 plots the tuning characteristic of the *QVCO*. A tuning range of 240MHz can be achieved by the *QVCO* and it can cover the specified range of 5.17~5.37 GHz.

Fig. 3.23 shows the measured spectrum at the output of the *DQR*. Markers 1~3 in Fig. 3.23 denote the IF signal, LO leakage and the RF feedthrough, respectively. The -72dBm of RF feedthrough and -55dBm of LO leakage are caused by substrate couple. Fig. 3.24 shows the result of linearity measurement. The measured input-referred IP3 (*IIP3*) is –13dBm, and the measured input-referred 1-dB compression point (*CP*1*dB*) of the receiver is –24dBm. The result meets the requirement because *CP*1*dB* is 6dB higher than the maximum input power level.

Fig. 3.25 shows the measured frequency response of the overall receiver. An input signal of –45dBm is applied to keep the desired output signal and image signal in the dynamic range. The maximum gain of the desired signal is 16.5dB and a 16dB gain can be achieved in the frequency range from 20MHz to 40MHz. Small gain degradation is observed at lower and higher frequencies away from the poles of the

polyphase filter. The maximum gain of the image signal within the bandwidth is –34.6 dB. Therefore, a minimum image rejection ratio of -50.6dB is achieved in the fabricated double-quadrature receiver. According to the characteristic shown in Fig. 3.11, the maximum ISR_{QG} degradation within the band is 26dB. Since the mismatch in *RF-QG* becomes insensitivity, a minimum image rejection ratio of -50.55dB that calculated by using (3.17) can still be achieved within the operation band.

A discussion for the measured IRR_{DQR} is performed herein. Since the frequency translation in the *DQR* is achieved by mixing two quadrature signals, the effects of errors on quadrature RF and LO signals can be neglected. According to (3.17), the overall image rejection ratio of the *DQR* is determined mainly by the image-to-signal ratio of the *DQ-Mixers* ($ISR_{DQ\text{-}Mixers}$) and the image rejection ratio of the four-stage polyphase filter (IRR_{PPF4}). As seen from the measurement results in the previous chapter, the actual IRR_{PPF4} is close to the simulation result, i.e. –60dB. Therefore, the reason why the measured IRR_{DQR} cannot reach to -60dB may be the mismatch of *DQ-Mixers*. Fig. 3.26 shows the result of 30-times Monte-Carlo simulations for *DQ-Mixers*. The parameters ΔW (channel width), ΔL (channel length), ΔV_{th} (threshold voltage), and ΔR (resistance) are randomly distributed according to the values provided by device mismatching characterization reports and corner parameters of the MOS device model, such that ΔW=±0.022um, ΔL=±0.0133um, ΔV_{th}=±0.01V, and ΔR=±24Ω (resistor width=2um). The simulated results show that the $ISR_{DQ\text{-}Mixers}$ may vary from –45.6dB to –74.9dB. Therefore, $ISR_{DQ\text{-}Mixers}$ become a dominator of IRR_{DQR}.

Since the mismatching performance depends on the geometry dimension of the devices, better resistor mismatching can be obtained with the larger resistor width.

The mismatching report shows that the ΔR can less than ±6Ω when the resistor width is increased to 10um. Fig. 3.27 shows the results of Monte-Carlo simulations with ΔR=±6Ω. The result shows that the $ISR_{DQ\text{-}Mixers}$ vary from –52.5dB to –72.6dB and most $ISR_{DQ\text{-}Mixers}$ can distribute around –60dB.

Table 3.4 summarizes the measured results of the fabricated double-quadrature receiver and the IEEE 802.11a requirements. Table 3.5 includes the performance summaries of recently proposed CMOS double-quadrature receiver and 5GHz receivers. These receivers demonstrate overall good quality and are suitable for wireless applications. The double-quadrature architecture is originated from [38]. In [38], the noise figure is high because the author uses passive RC structure to generate the quadrature RF signals. In [68], a notch filter is merged with the *LNA* to achieve high image rejection. To control the zero frequency of the notch filter, an image-reject PLL is added and hence the power dissipation is increased. In the receiver structure of [69], the image rejection performance will be dominated by the second-stage frequency translation. Although an accuracy quadrature LO with 0.05dB amplitude unbalance and 0.3^{o} phase unbalance is used in the IF mixers, the image rejection ratio remains be limited to –44.5dB. In this thesis, the double-quadrature architecture is adopted to tolerate LO mismatches. Besides, new circuit structures are designed to reduce the power dissipation and noise degradation.

3.6 SUMMARY

A 1.8-V low-power 5-GHz CMOS front-end receiver for wireless LAN system was proposed. Double-quadrature architecture in the proposed receiver is adopted and analyzed. A single-stage frequency-adjustable RLC phase shifter is used to generate

RF quadrature signals. The current reuse technique is employed by merging downconversion mixers with quadrature VCO to take advantage of low power consumption. The four-stage polyphase filter is integrated in the receiver to reject image signals. The 5-GHz receiver is fabricated using 0.18-um 1P6M CMOS technology. The measured results have shown that the proposed receiver is suitable for wireless LAN applications.

Table 3.1

Rate-dependent Parameters in IEEE 802.11a

Data Rate (Mbits/s)	Modulation (Code Rate)	Coded Bits per Subcarrier	Sensitivity (dBm)	Theoretical SNR (dB) [71]	Required NF (dB)
6	BPSK (1/2)	1	-82	1.0	18.7
9	BPSK (3/4)	1	-81	3.5	17.2
12	QPSK (1/2)	2	-79	3.8	18.9
18	QPSK (3/4)	2	-77	6.5	18.2
24	16QAM (1/2)	4	-74	8.8	18.9
36	16QAM (3/4)	4	-70	12.3	19.4
48	64QAM (2/3)	6	-66	16.8	18.9
54	64QAM (3/4)	6	-65	19.0	17.7

Table 3.2

The Input Blocking Defined in HIPERLAN2 (f_C : carrier frequency)

Frequency of the interference	Blocking level (dBm)
100KHz ~ 2.5GHz	0
2.5GHz ~ 4.0GHz	-10
4.0GHz ~5.15GHz	-30
5.15GHz ~ f_C – 50MHz	-30
f_C + 50MHz ~ 5.35GHz	-30
5.35GHz ~ 5.47GHz	-30
5.47GHz ~ f_C – 50MHz	-30
f_C + 50MHz ~ 5.725GHz	-30
5.725GHz ~ 7GHz	-30
7GHz ~ 13GHz	-20

Table 3.3

Device Parameters of the 5-GHz DQR

LNA		**RF-QG**	
M_1, M_2	65μm/0.18μm	M_1, M_2	210μm/0.18μm
M_3, M_4	32.5μm/0.18μm	M_3, M_4	20μm/0.18μm
M_5	160μm/0.9μm	M_5	625μm/0.8μm
L_{d1}, L_{d2}, L_{s1}, L_{s2}	2.3nH	C_{PS}	117.6μm/0.18μm
L_{g1}, L_{g2}	3.5nH	R_{PS}	70Ω
C_{bp}	10pF	L_{PS}	2.3nH
R_{bp}	10kΩ	VB1	0.8V
VB1	0.79V	VB2	1V
DQ-Mixers		VB3	0.75V
M_1 ~ M_8	10μm/0.5μm	**Active Polyphase Filter**	
R	800Ω	M_1	1.5μm/0.3μm
QVCO			M_2
M_1, M_4	120μm/1μm	M_3, M_4	4.5μm/0.54μm
M_2, M_3	20μm/1μm	M_5, M_6, M_L	1.5μm/1.8μm
M_5 ~ M_8	60μm/0.18μm	M_7, M_8	10μm/0.54μm
M_9 ~ M_{12}	45μm/0.18μm	M_b	10.5μm/0.9μm
C_1 ~ C_4	60μm/1μm	C_H	0.33p, 0.45p, 0.72p, 1p
L_1, L_2	2.3nH	C_C	C_H /2
VB	0.7V	R_L	30KΩ

Table 3.4

Measured Results of the 5-GHz Double-Quadrature Receiver.

Parameter	Measured Result	802.11a Requirement
S_{11} within Band	< -10 dB	-
NF	8.5 dB	10dB+5dB(margin)
Gain	16 dB	-
*CP*1*dB*	-24 dBm	-26 dBm
IIP3	-13 dBm	-
Tuning range of VCO	240 MHz	200 MHz
IRR	-50.6 dB	-58 dB
Power dissipation	22.4 mW	-
Die area	2×1.5 mm^2	-
Technology	0.18-um 1P6M CMOS	-

Table 3.5

Performance Summaries of the Recently Proposed CMOS Double-Quadrature receiver and 5GHz Receivers.

	This Work	[38]	[68]	[69]
Architecture	Double-Quadrature	Double-Quadrature	Weaver (Notch filter with PLL)	Wideband-IF (Accurate QVCO)
Frequency	5 GHz	900 MHz	5 GHz	5 GHz
Supply voltage	1.8 V	5 V	1.8 V	1.8 V
NF	8.5 dB	24 dB	7.2 dB	5.6 dB
Gain	16 dB	9.2 dB	26 dB	83/9 dB
*CP*1*dB*	-24 dBm	-	-18 dBm	-
IIP3	-13 dBm	27.9 dBm	-7 dBm	-1/-23 dBm
IRR	-50.6 dB	-46 dB	-53 dB	-44.5dB*
Power	22.4 mW	500 mW	58.8 mW	212.4 mW
Technology (CMOS)	0.18-um	0.7-um	0.18-um	0.18-um

* Theoretical calculated result.

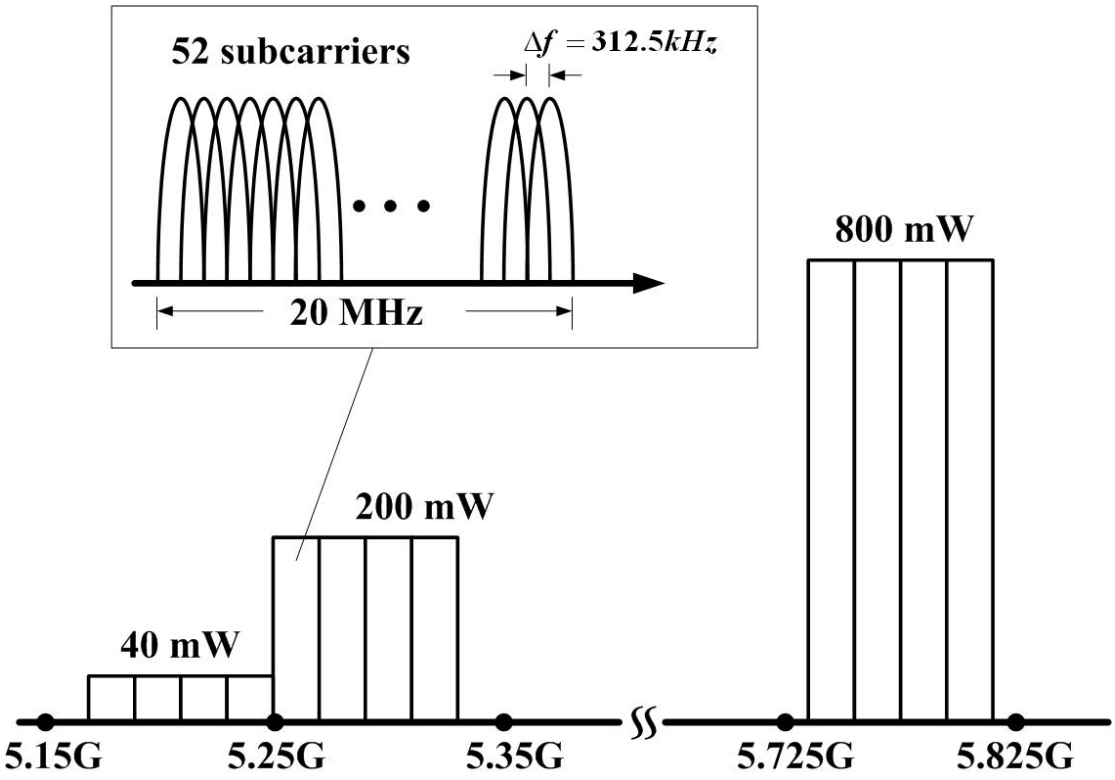


Fig. 3.1 Allocated frequency of wireless LAN IEEE 802.11a.

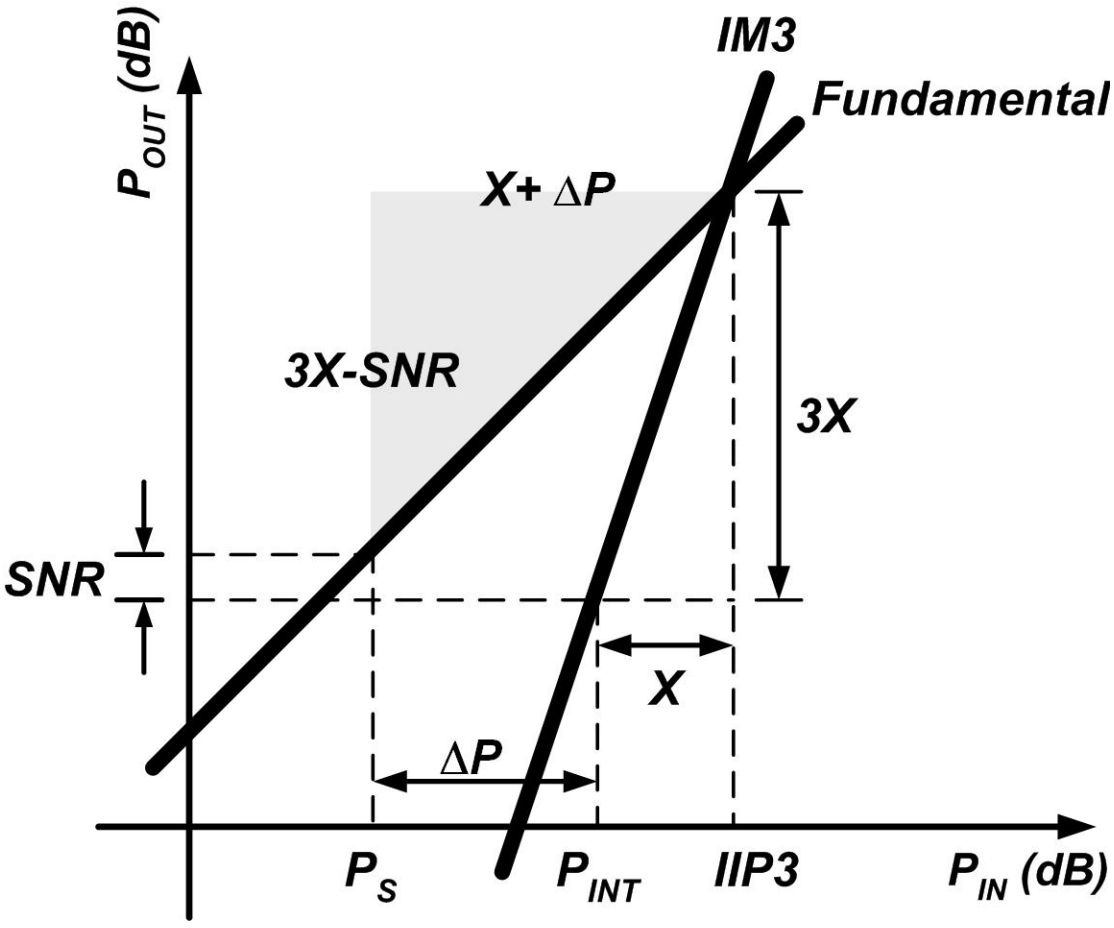


Fig. 3.2 Determination of *IIP3* in a communication system.

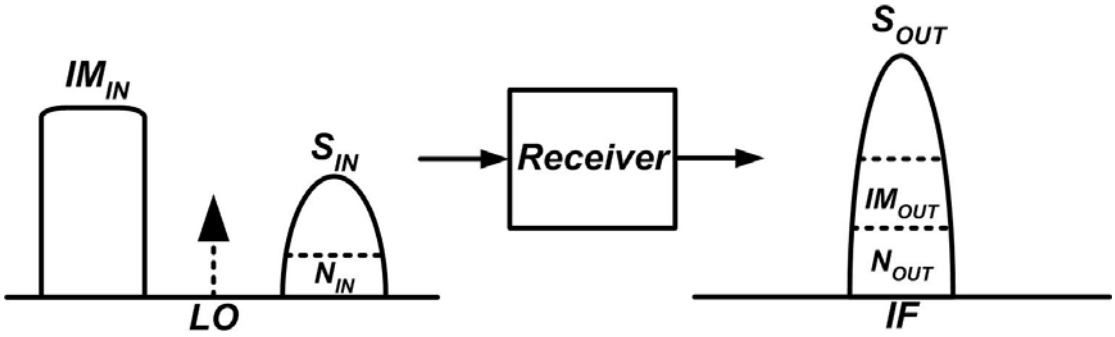


Fig. 3.3 Noises and image interferers at the input and output of the receiver.

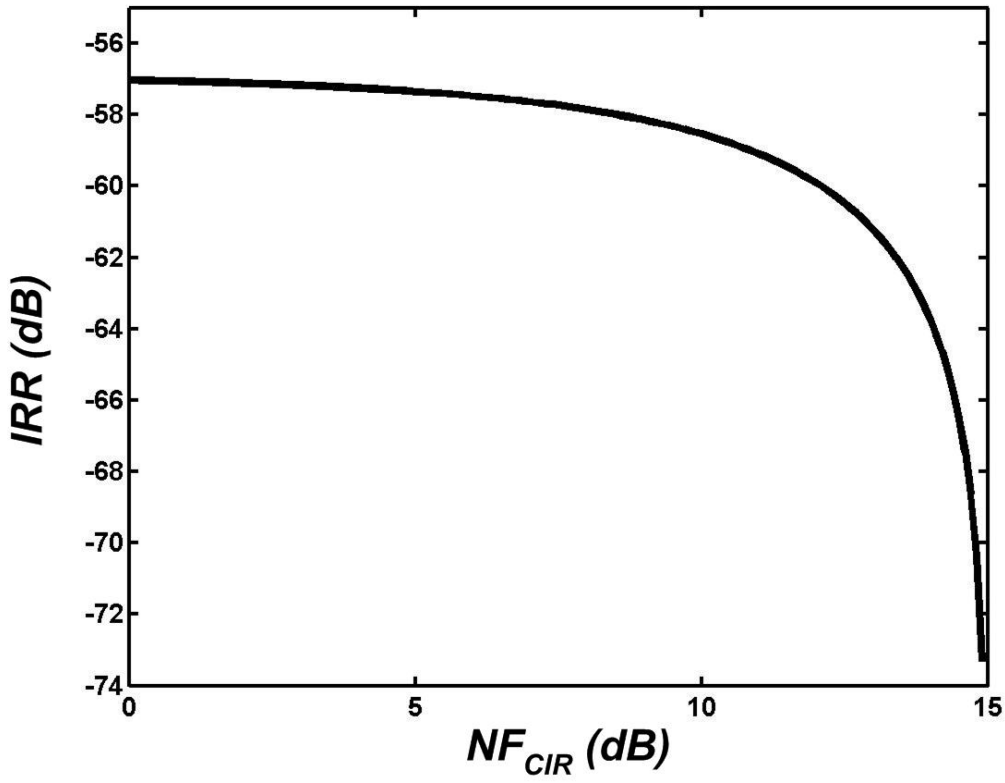


Fig. 3.4 The Required IRR_{DQR} in different NF_{CIR} to achieve the data rate of 54Mbits/s.

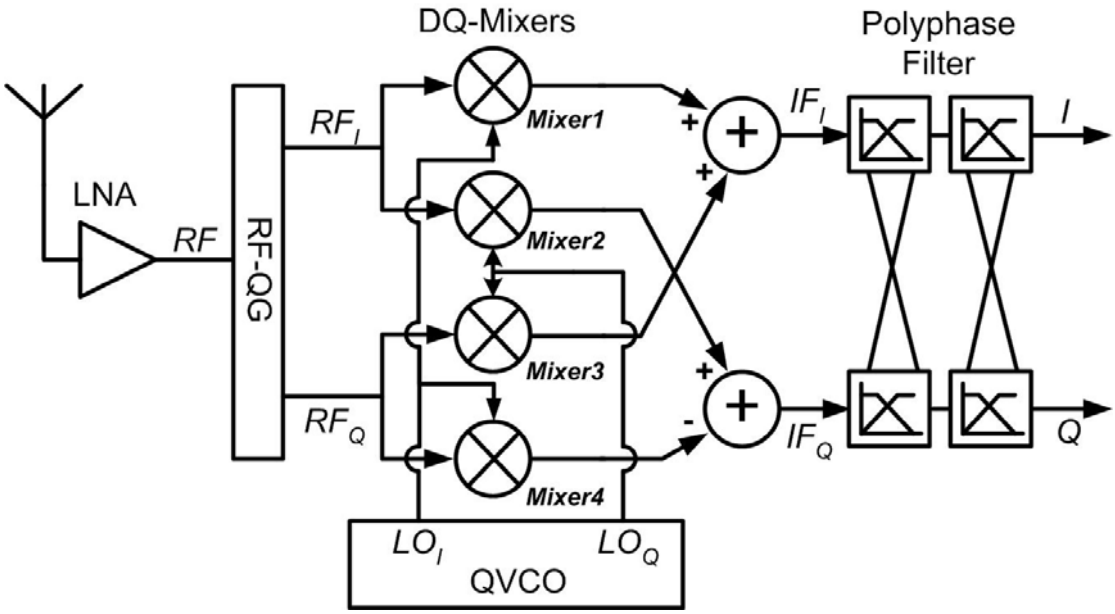
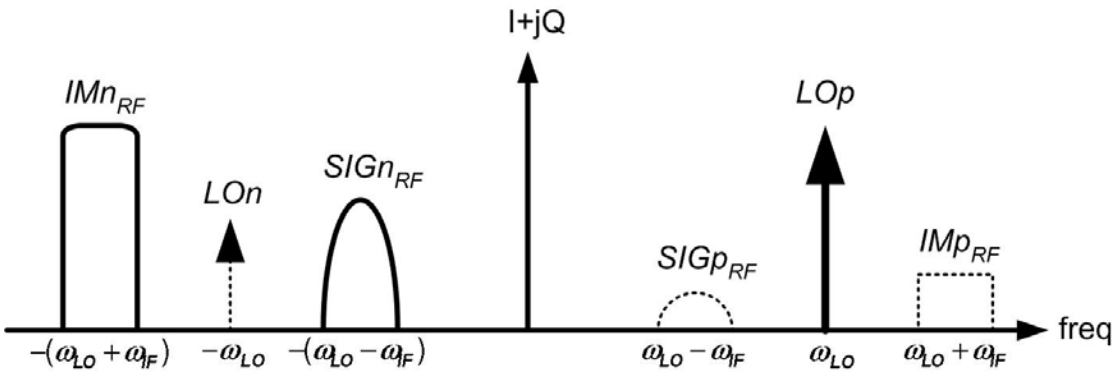
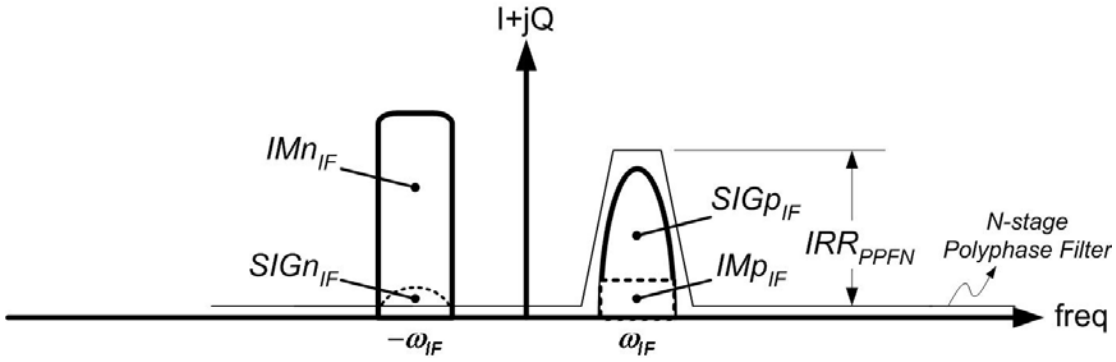


Fig. 3.5 Block diagram of double-quadrature receiver (*DQR*).



(a)

$$LOp\otimes(SIGn_{RF}+IMn_{RF})+LOn\otimes(SIGp_{RF}+IMp_{RF})$$



(b)

Fig. 3.6 Signal spectra in the *DQR* (a) before the downconversion and (b) after the downconversion.

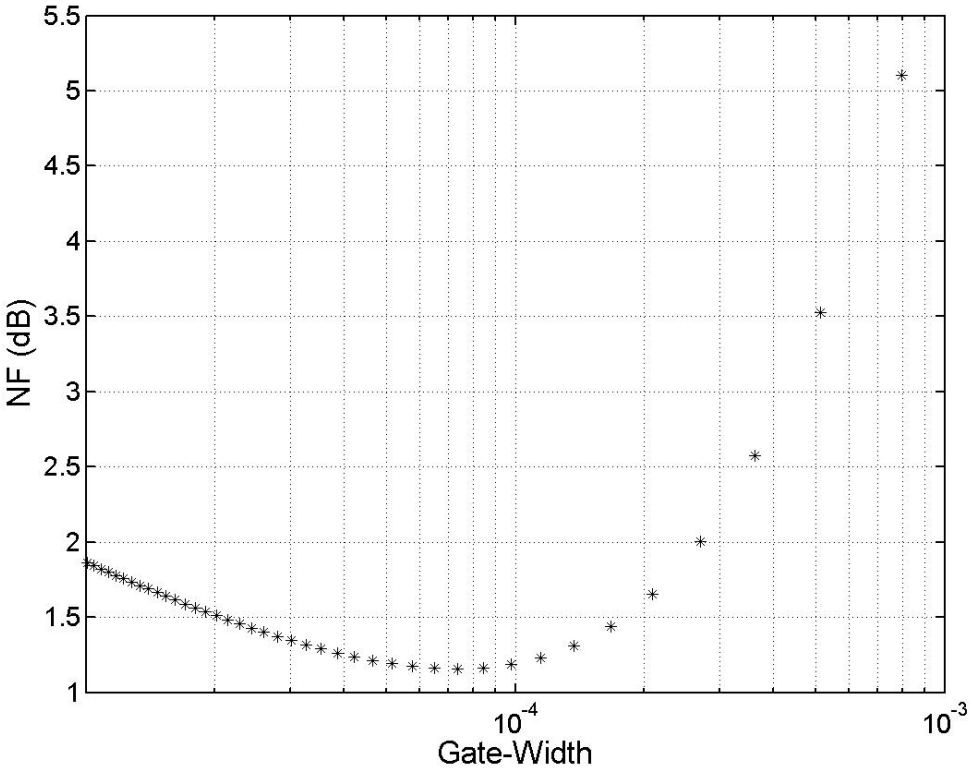


Fig. 3.7 Simulated noise figure versus gate-width of the input transistor of the *LNA*.

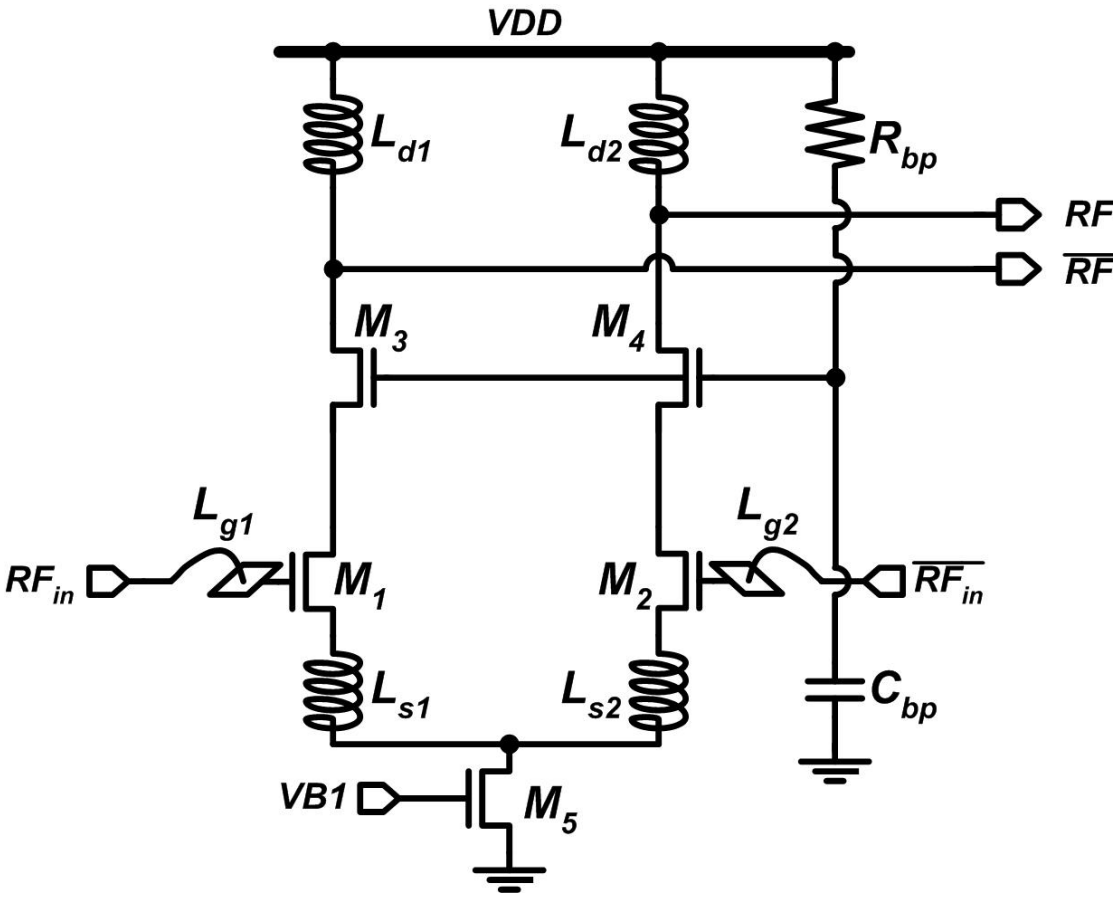


Fig. 3.8 Circuit diagram of the low-noise amplifier (*LNA*).

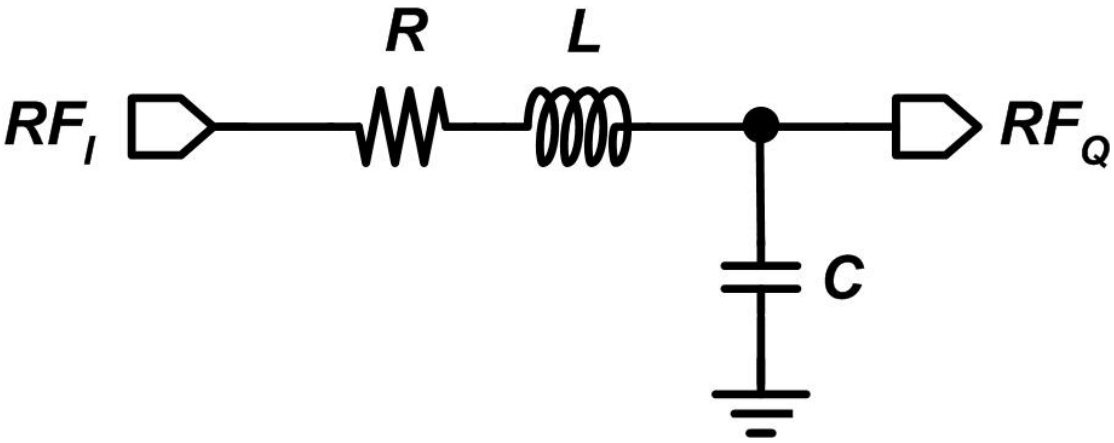


Fig. 3.9 RLC phase shifter.

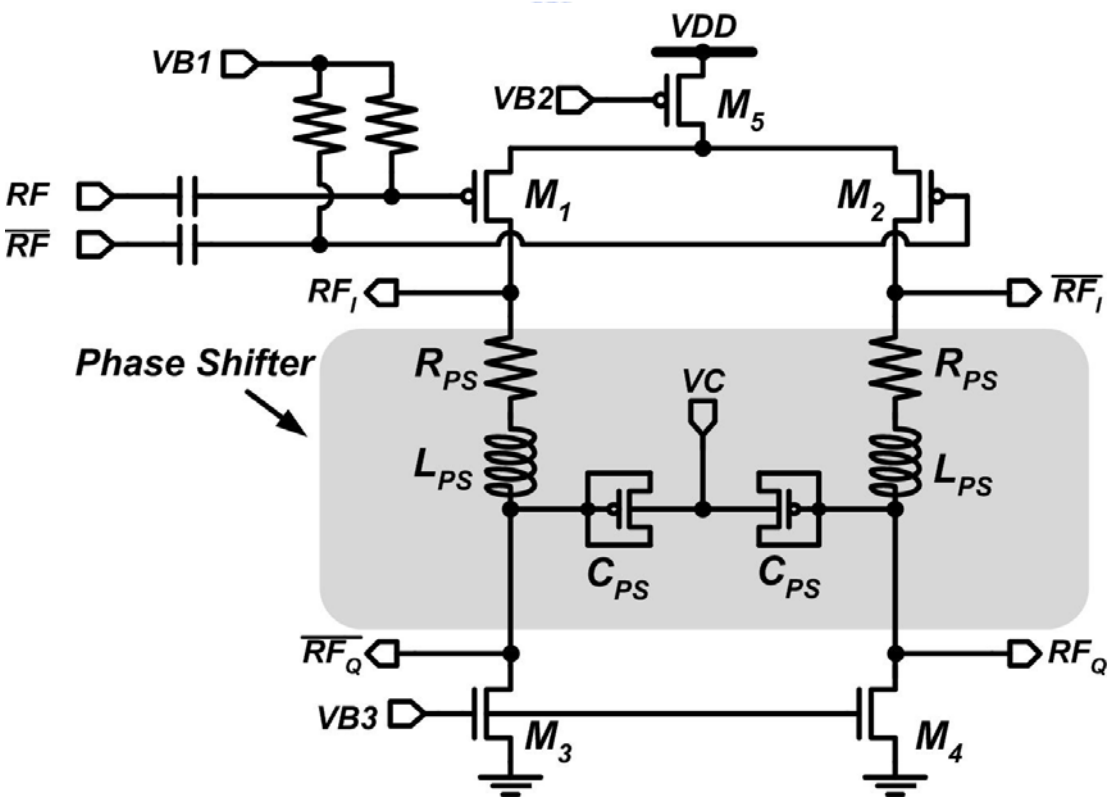


Fig. 3.10 Circuit diagram of the RF quadrature generator (*RF-QG*).

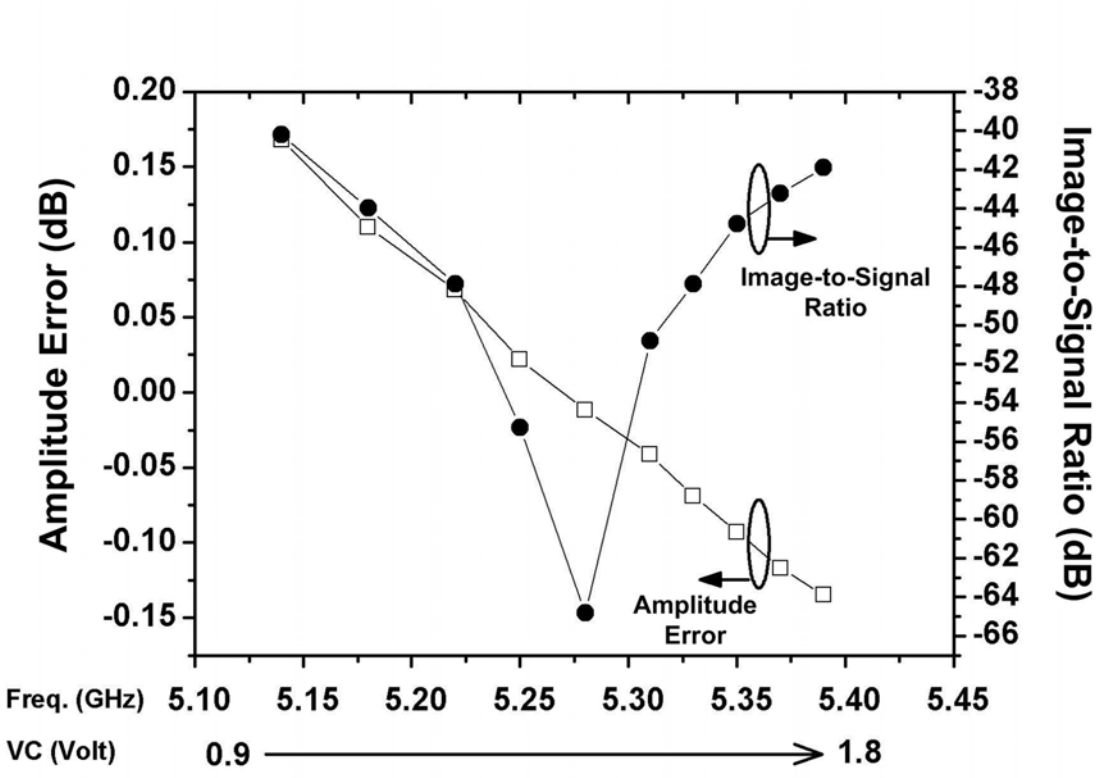


Fig. 3.11 Simulated amplitude errors and *ISR* at the outputs of the *RF-QG*.

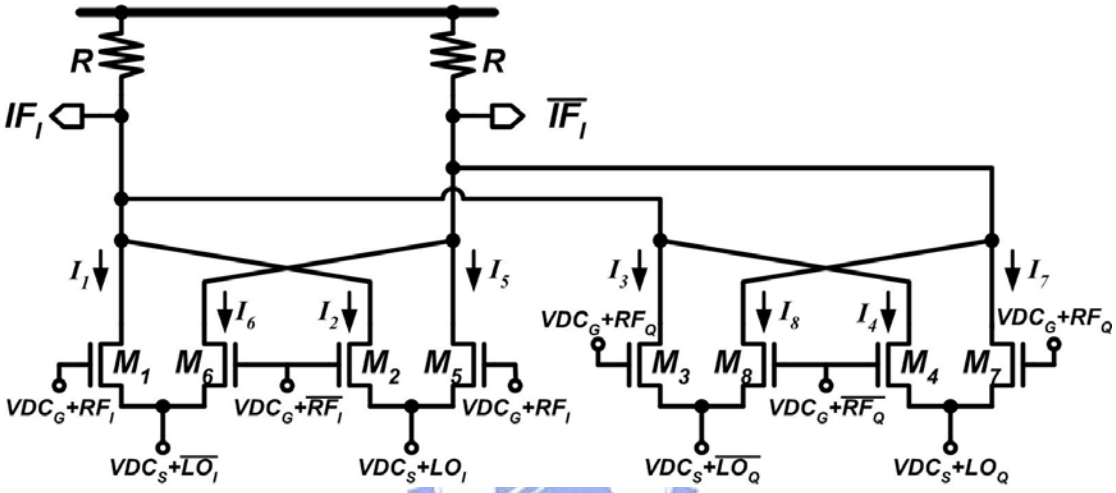


Fig. 3.12 Circuit diagram, which combines the functions of *Mixer1* and *Mixer3* in Fig. 3.5.

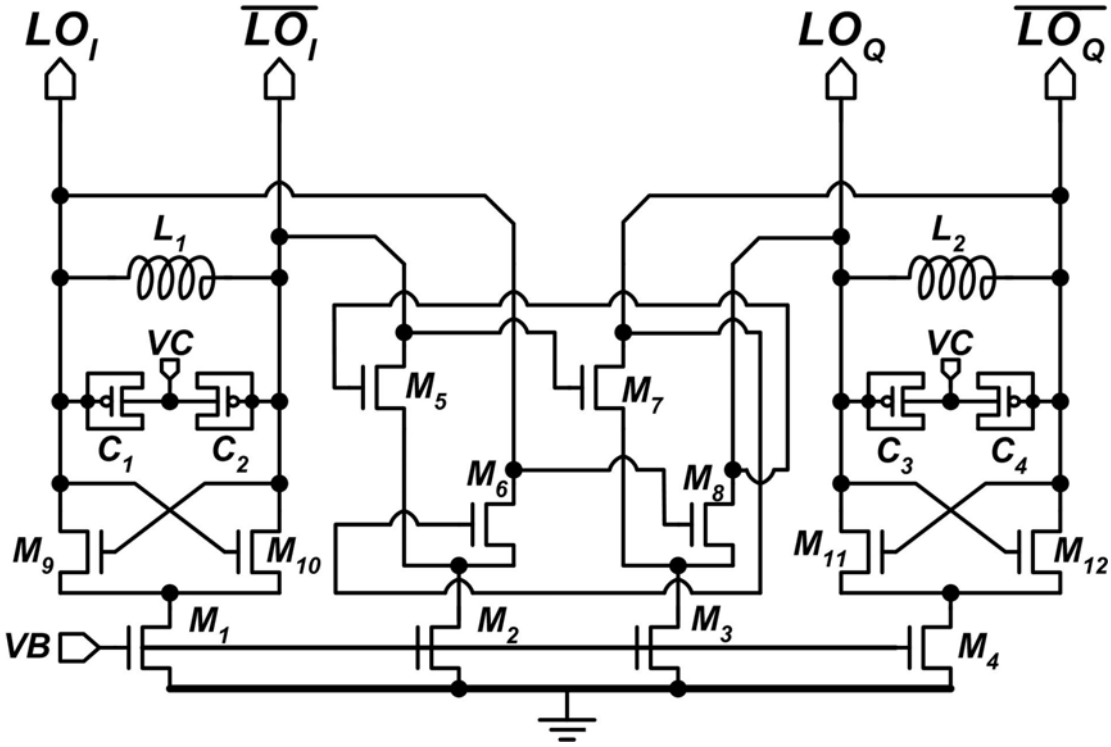


Fig. 3.13 Circuit diagram of quadrature voltage-controlled oscillator (*QVCO*).

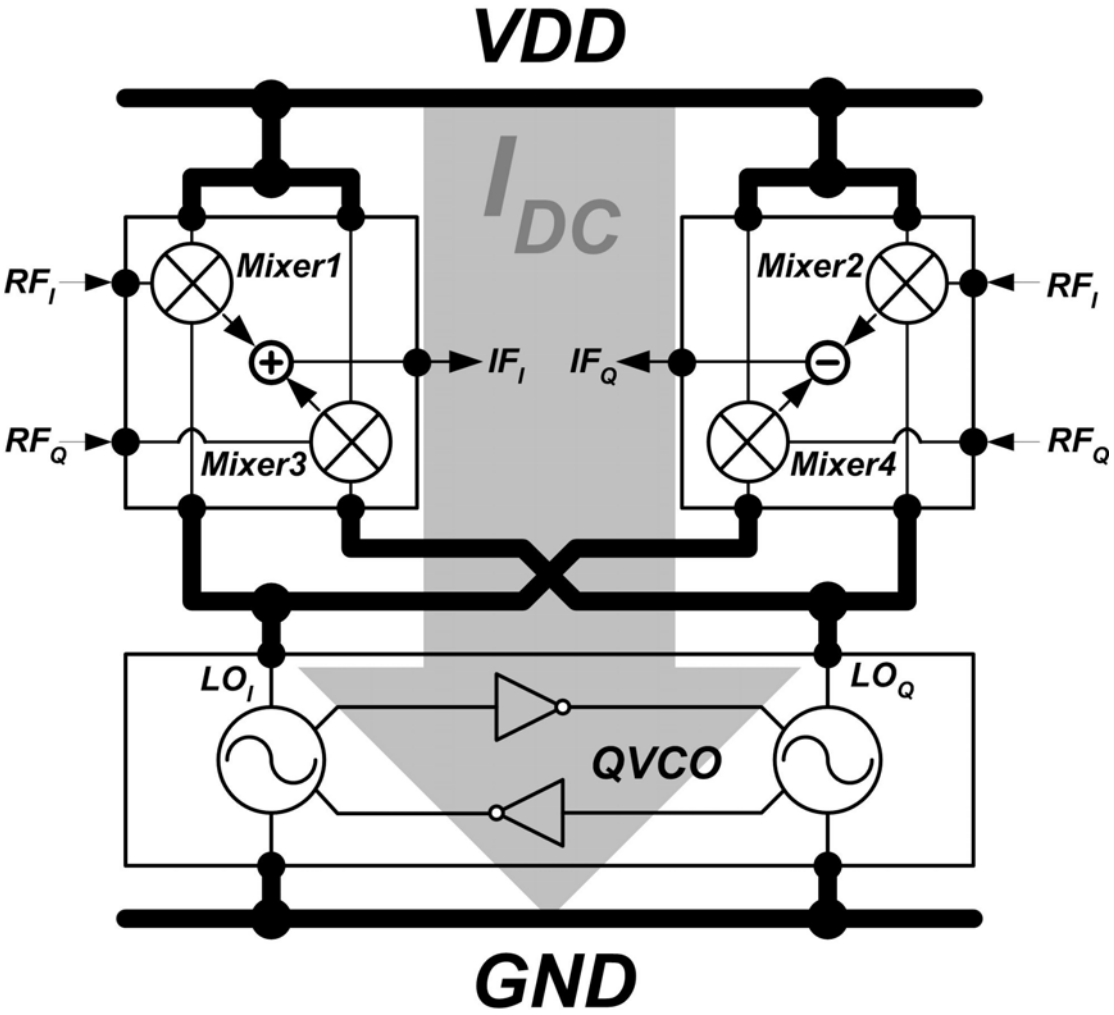


Fig. 3.14 Block diagram of current reuse structure.

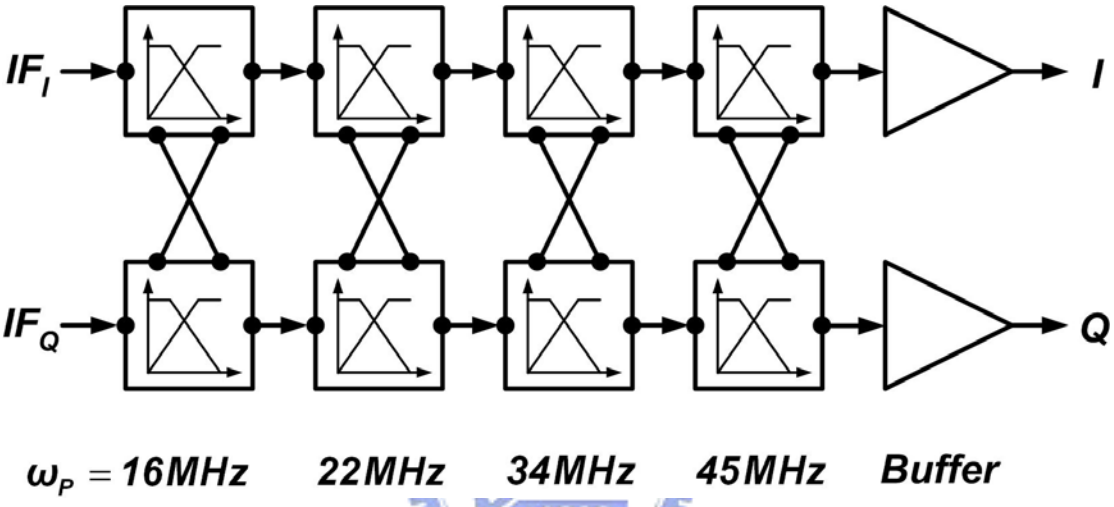


Fig. 3.15 Block diagram of the four-stage active polyphase filter.

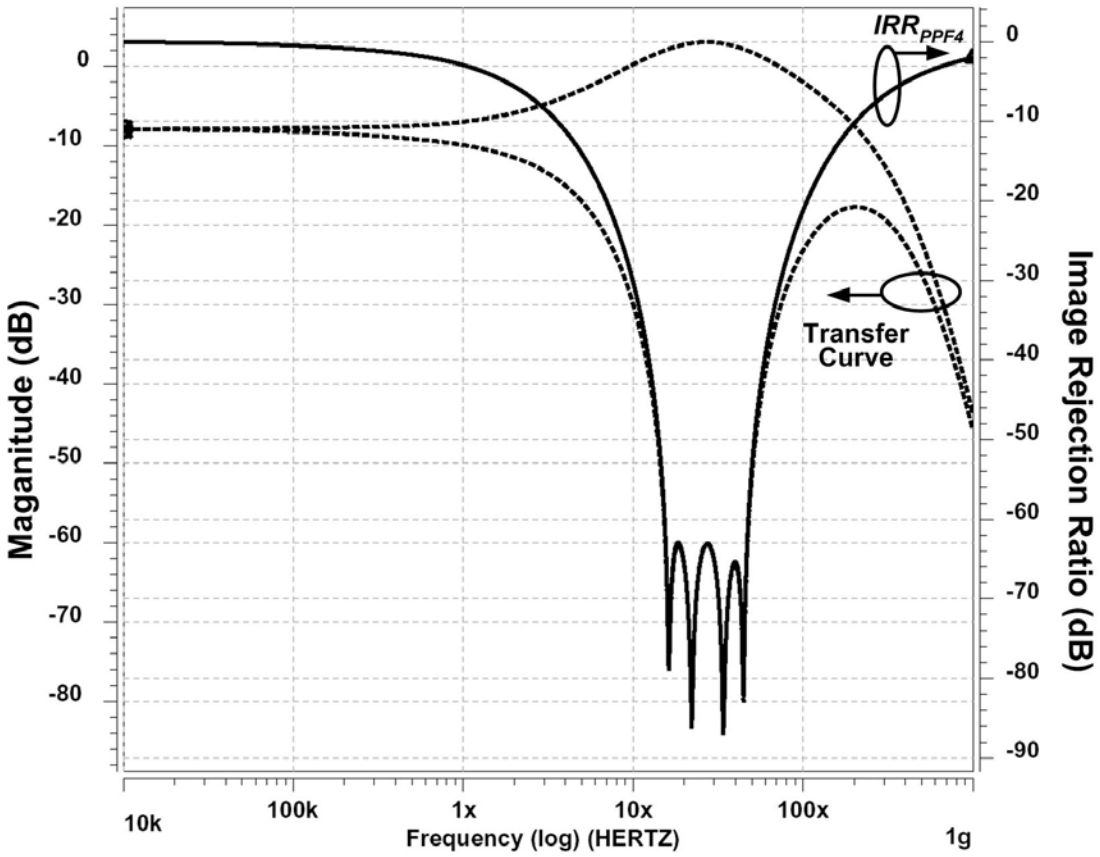


Fig. 3.16 HSPICE simulated transfer curve and IRR_{PPF4} of the four-stage active polyphase filter.

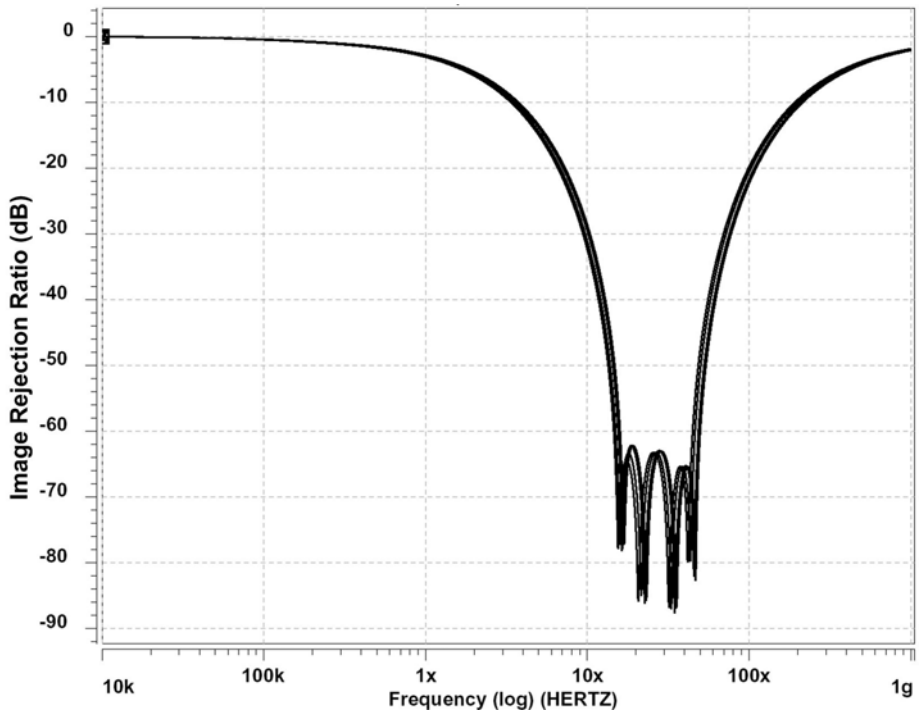


Fig. 3.17 HSPICE simulated *IRR* variations of the four-stage active polyphase filter with four corners (FF, FS, SF, and SS) of MOS device models.

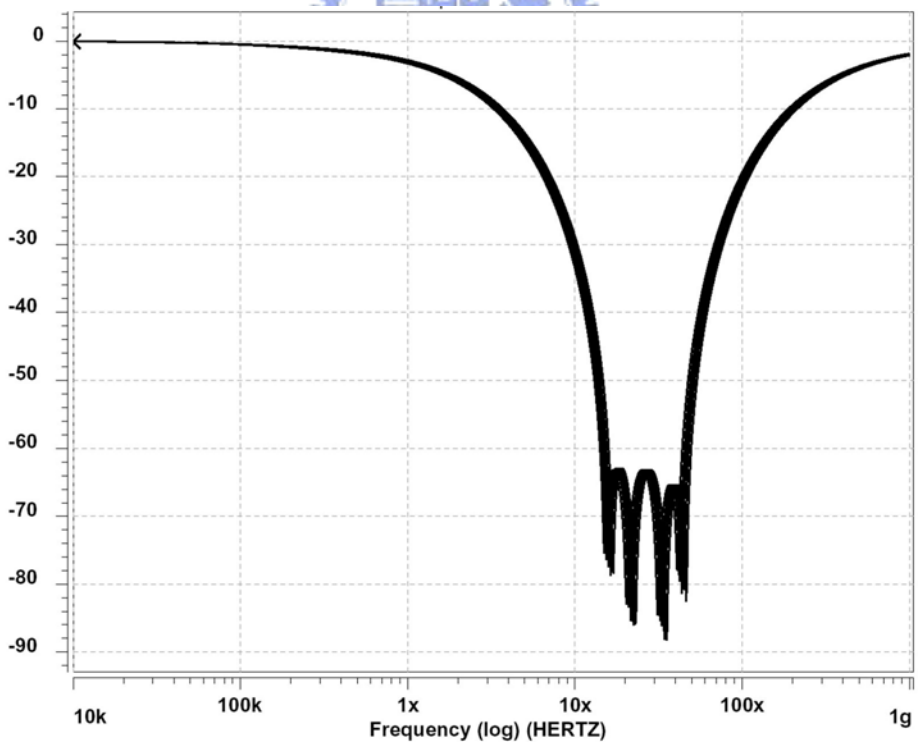


Fig. 3.18 HSPICE simulated *IRR* variations of the four-stage CMOS polyphase filter in the temperature between 0^{o} and 80^{o}.

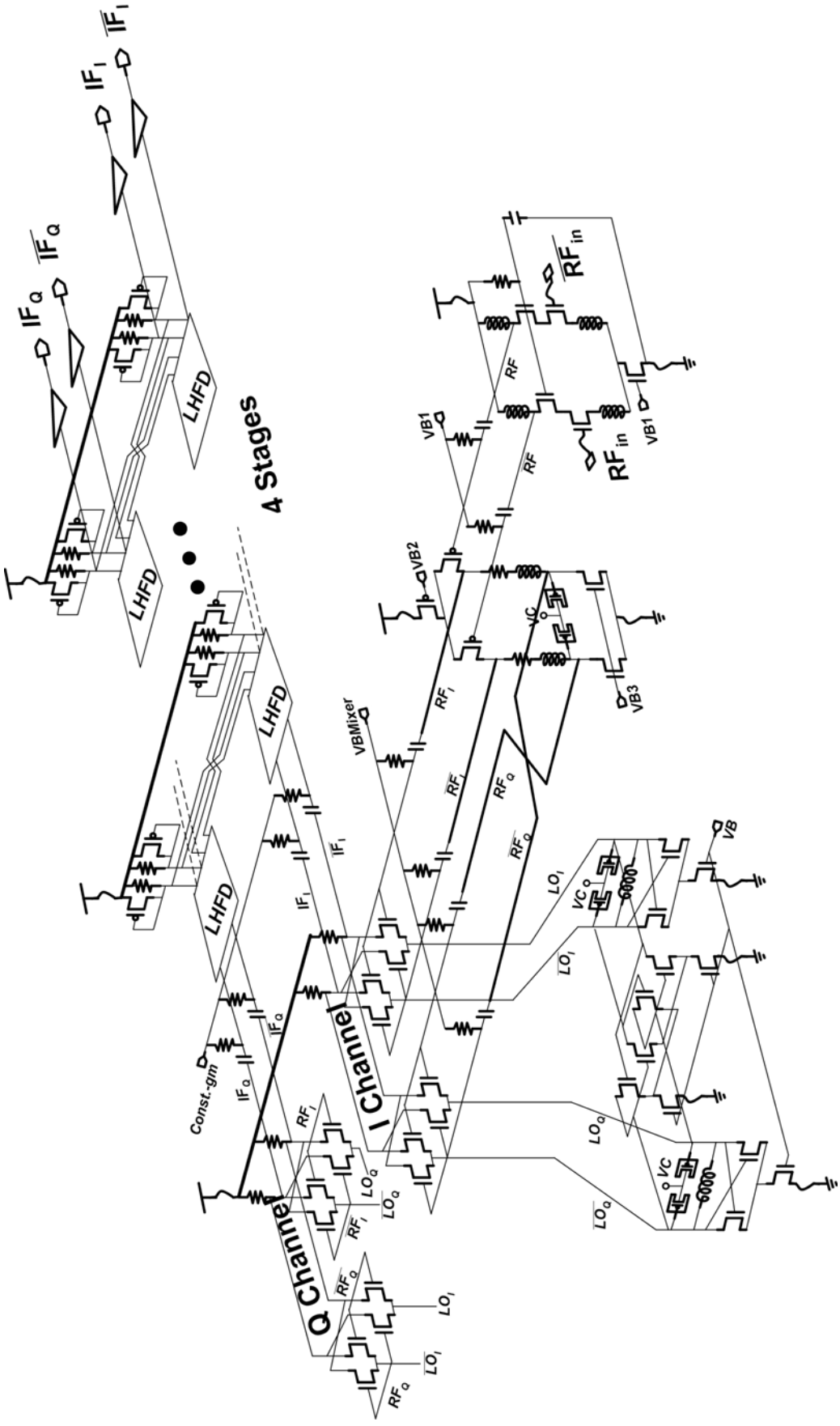


Fig. 3.19 Complete circuit diagram of the 5-GHz double-quadrature receiver

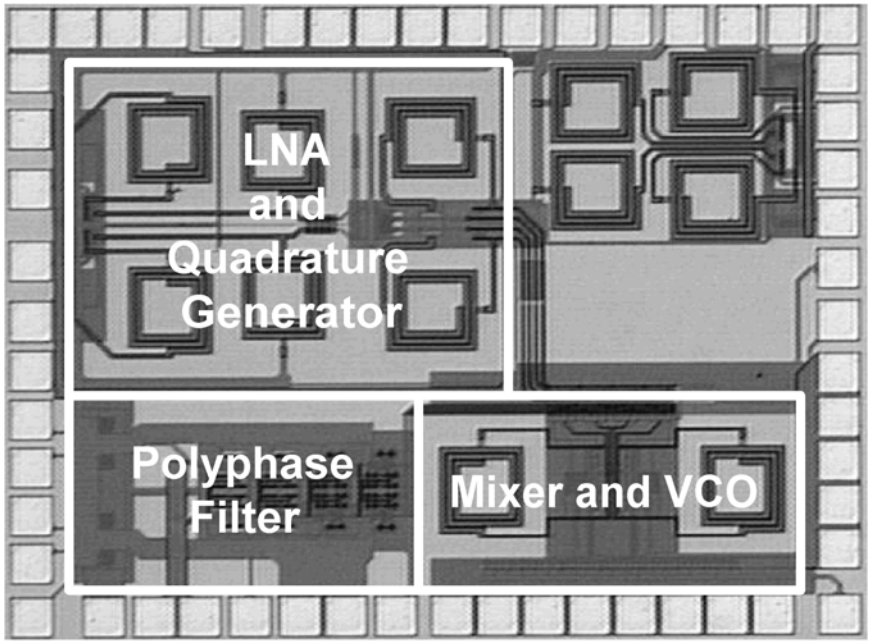


Fig. 3.20 Die micrograph of the fabricated CMOS double-quadrature receiver.

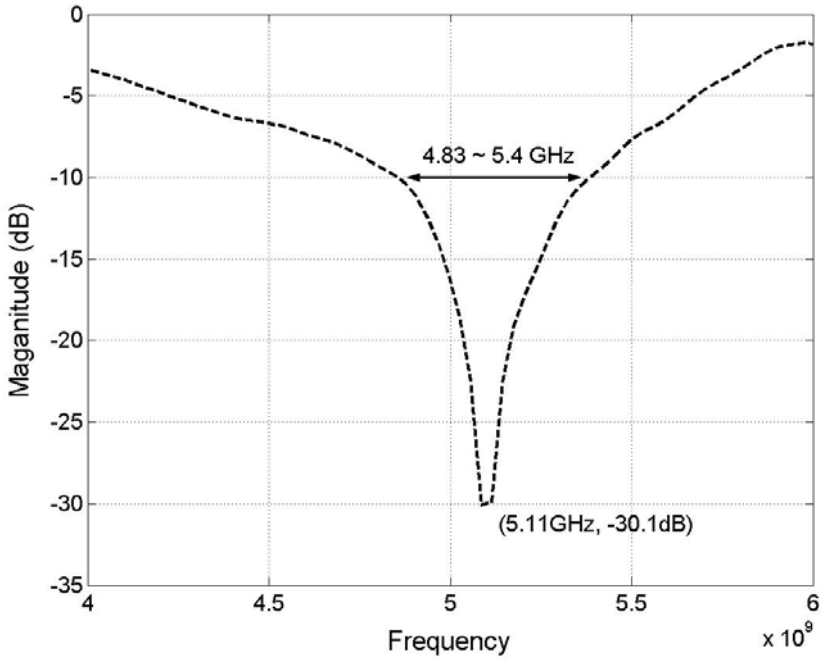


Fig. 3.21 Measured S_{11}.

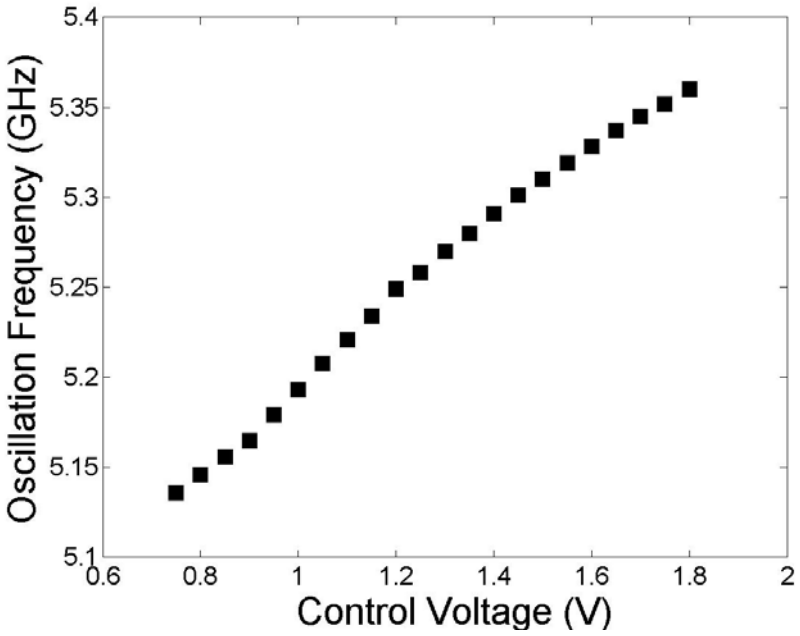


Fig. 3.22 Measured tuning range of quadrature VCO.

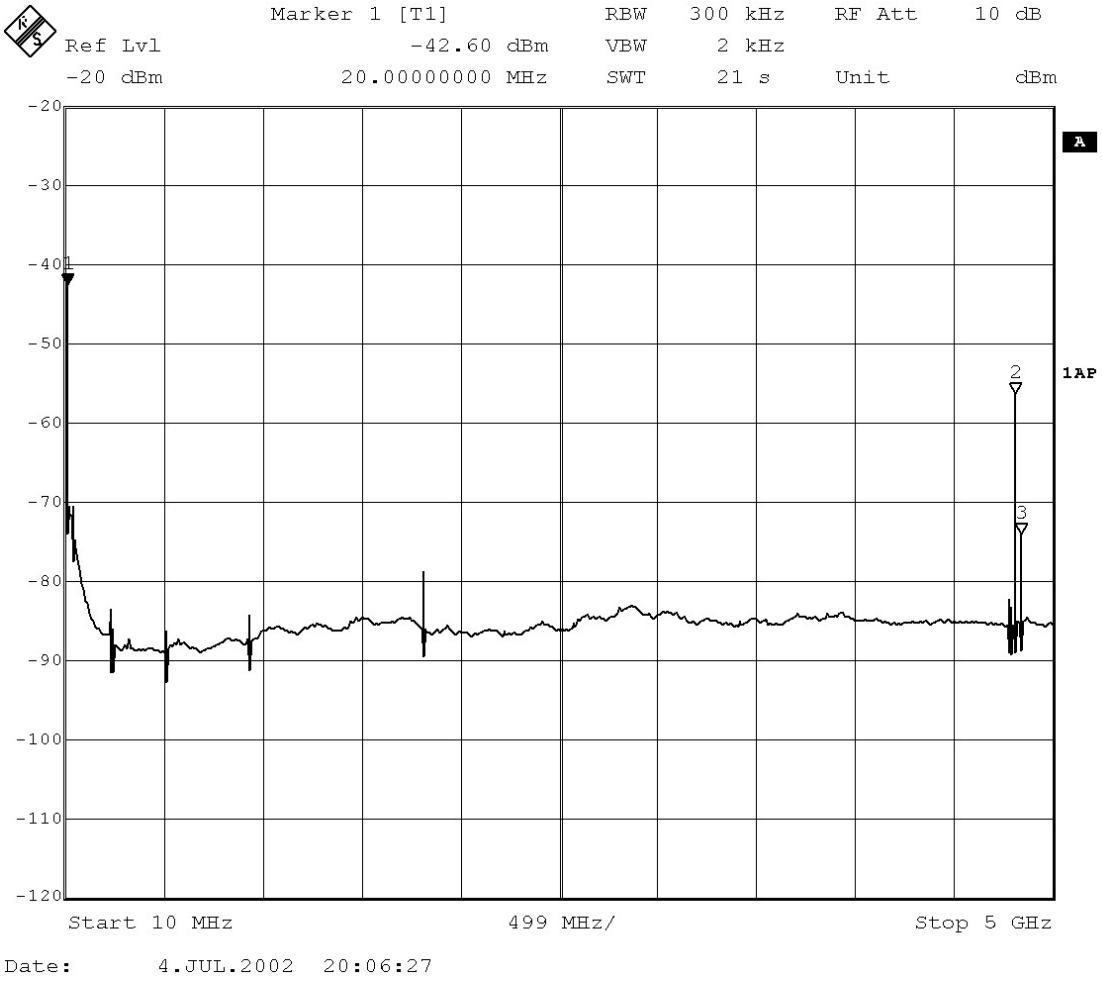


Fig. 3.23 Output spectrum of the *DQR*

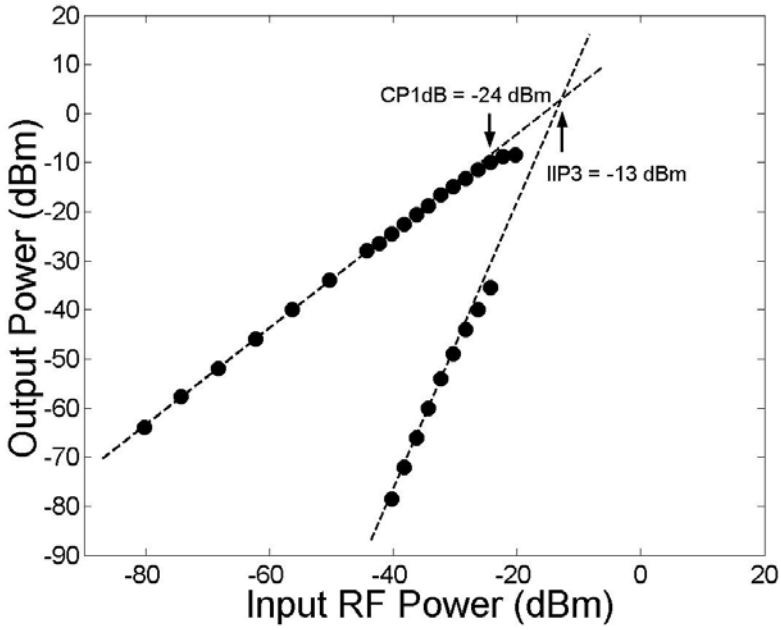


Fig. 3.24 Measured results concerning *CP*1*dB* and *IIP3*.

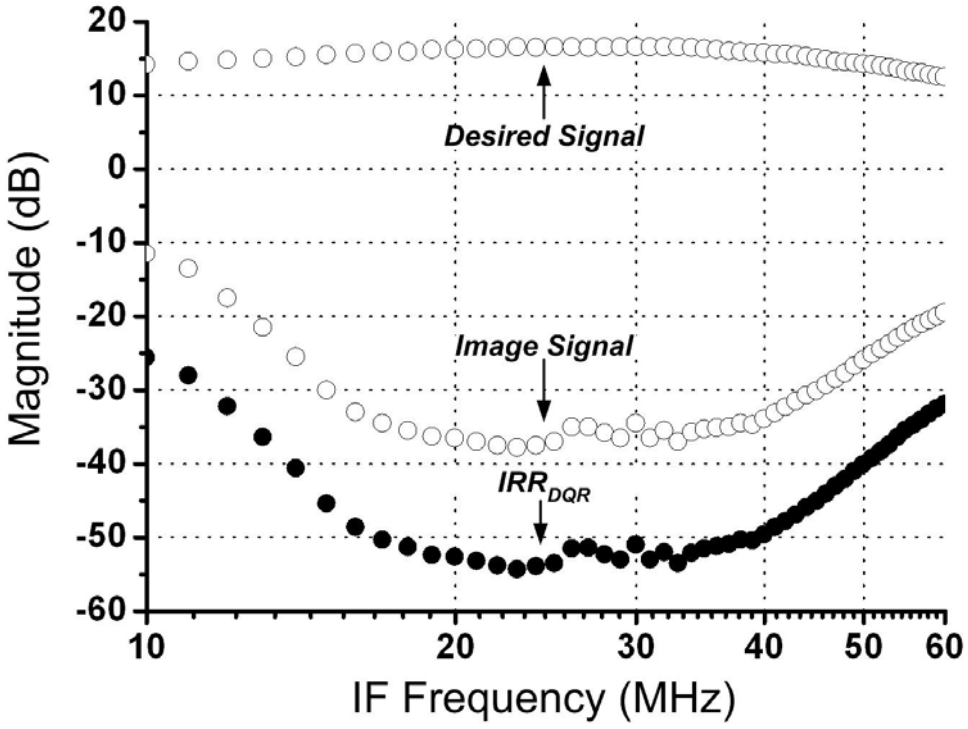


Fig. 3.25 Measured frequency response and IRR_{DQR} of fabricated 5-GHz CMOS *DQR*.

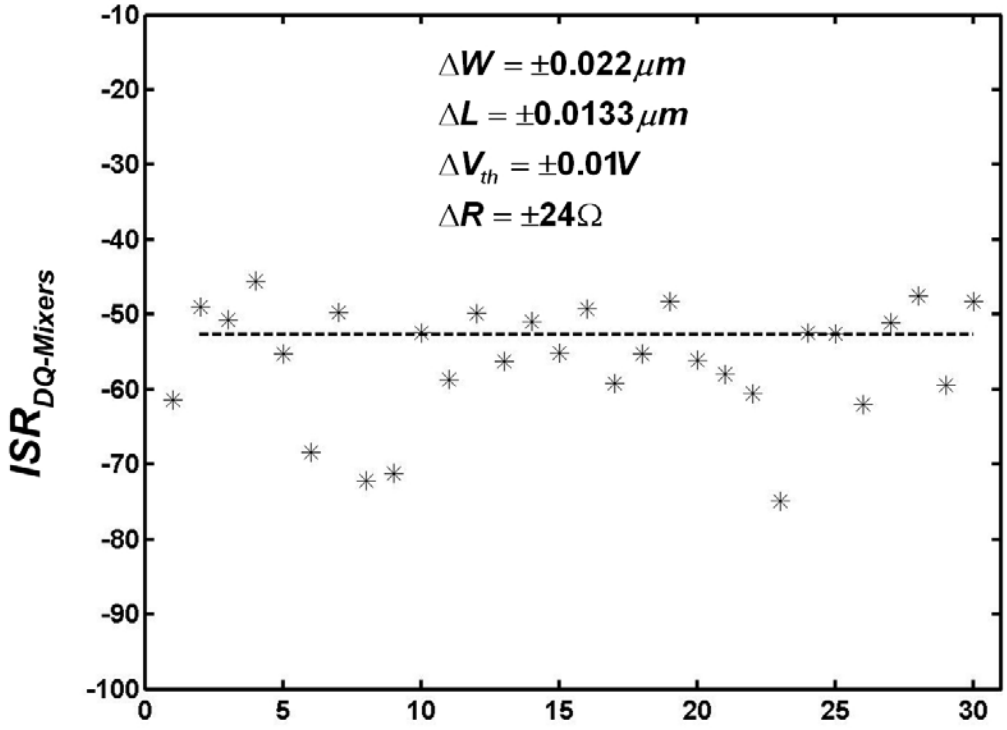


Fig. 3.26 Results of 30-times Monte-Carlo simulations for *DQ-Mixers* (resistor width=2um)

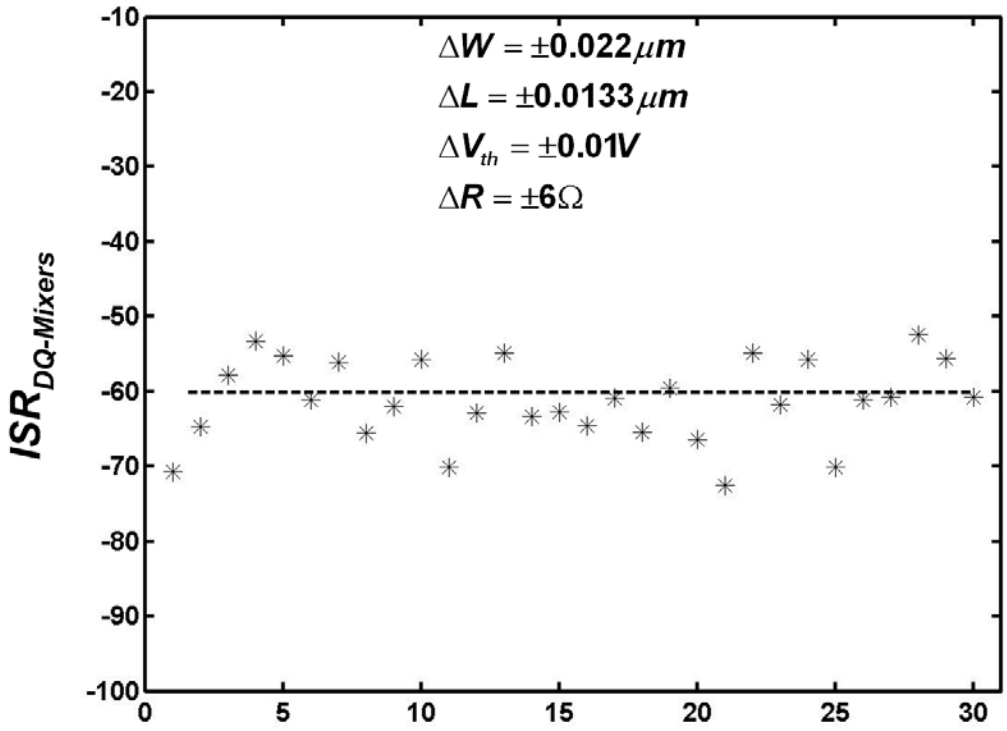


Fig. 3.27 Results of 30-times Monte-Carlo simulations for *DQ-Mixers* (resistor width=10um)