CHAPTER 4

A 1-V 2.4-GHZ DOUBLE-QUADRATURE RECEIVER FRONT-END FOR LOW-VOLTAGE APPLICATIONS

4.1 INTRODUCTION

Recently, battery-operated wireless communication systems with low power consumption and high sustainability on operating time for batteries have wide applications. In these systems, low-power CMOS RF ICs are the key components for achieving system performance goals. One effective means of reducing power dissipation is to decrease supply voltage. Moreover, as CMOS technology moves below 100 nm, supply voltage scaling is also required.

Regarding the design of CMOS low-voltage RF front-end circuits, 1-V power supply is a challenge for 0.25-um or 0.18-um CMOS technology. Generally, the number of cascoded MOS devices in all CMOS circuits should be kept below three. Thus all MOS devices can be operated normally and sufficient voltage swing can be obtained. So far, separate components of CMOS RF *VCO* and *LNA* have been successfully designed and operated at 1-V supply voltage for receiver front-end applications [76]-[78].

In this chapter, a *DQR* that operates at 1-V supply voltage is designed and

analyzed in 0.25-um CMOS technology. The proposed *DQR* integrates a new *LNA*, a new *RF-QG*, *DQ-Mixers*, and a *QVCO* together.

The circuit realizations use a differential structure in the *LNA* design to reduce the power supply and ground noise effects. Considering common-mode interferences, an LC-tank working as a source degenerator is used to suppress common-mode signals. The LC-tank has the advantage of providing high impedance for common-mode signals in the desired RF range with a negligible dc voltage-drop. Hence the LC-tank is suitable for low-voltage differential RF amplifier which will improve the common-mode rejection ability. The experimental results yield a differential gain of 17 dB and a –12 dB of common-mode gain, i.e. the fabricated *LNA* is capable of achieving a total of 29 dB of common-mode rejection ratio (*CMRR*).

A single-stage frequency-adjustable RLC phase shifter circuit is used to realize the new RF quadrature generator. In comparison to the *RF-QG* in Chapter 3, the cross-couple transistors are used to increase the load impedance enhancing the gain and resulting in a reduction of the power consumption. In the *DQ-Mixers*, the NMOS operating in the triode region serve as the load. Adjustment of the bias voltage at the gates of NMOS transistors can control the conversion gain. To increase the voltage headroom in *DQ-Mixers* and *QVCO*, the proposed circuit does not utilize the cascoded structure used in Chapter 3.

The fabricated *DQR* consumes 34.6mW at a supplied voltage of 1V and occupies a chip area of 2.88mm^2. A 2.4GHz of RF signal is received by *DQR* which is then down-converted to 80MHz.

Section 4.2 presents the design considerations and circuit implementations of the

proposed 1-V *DQR*. Section 4.3 then presents the experimental results. Finally, Section 4.4 draws conclusions.

4.2 CIRCUIT DESIGNS

4.2.1 Low-Noise Amplifier (*LNA*)

The *LNA* circuit of the proposed 2.4-GHz *DQR* is shown in Fig. 4.1. The *LNA* is designed using 0.25μm CMOS 1P5M technology and operated at a supplied voltage of 1V. As seen in Fig. 4.1, M_1 and M_2 are the input transistors. To minimize noise at a target power consumption of 4mW, the dimensions of M_1 and M_2 are chosen as 180μm/0.24μm [7]. L_{g1}, L_{g2}, L_{s1}, L_{s2}, and capacitors at the gates of M_1 and M_2 match the input impedance of 50Ω. M_3 and M_4 are used for reverse isolation. Parasitic capacitors at *RF*, $\overline{RF}$ and L_{d1}, L_{d2} realize the LC tanks in which the resonant frequency is tuned to 2.4GHz. L_{d1}, L_{d2}, L_{s1} and L_{s2} are realized by on-chip spiral inductors and L_{g1} and L_{g2} are realized by bounding wires.

Since the power of the received signal can be very weak, RF receiver front-end is sensitive to noise from the power supply and ground. Thus a fully differential scheme is chosen in this design to reject noise from these sources. However, a common-mode issue exists in the differential amplifier. If one end of a differential pair does not perfectly match the other a differential *LNA* will receive an RF signal with a common-mode fraction. The large common-mode signal will corrupt the desired signal and may saturate the amplifier. Therefore, a common-mode signal suppression capability is required in the design of the differential *LNA*.

A MOS device is generally used as the current source in an analog

integrated-circuit design. For a common-mode signal, the gain is suppressed because the high drain-impedance of current source works as a source degenerator. However, the drain-impedance decreases to a very low value if the circuit operates at GHz. In this design, the proposed *LNA* uses a LC-tank as a source degenerator. Fig. 4.2 shows the simulated impedances at the coupled-source node of differential LNAs with MOS current source and LC-tank operating between 2 to 3 GHz. From Fig. 4.2, it can be seen that impedances generated by the MOS current source and the LC-tank at 2.4 GHz are 70Ω and 300Ω, respectively. Hence the LC-tank provided a much higher impedance than a MOS device in the desired RF range. Additionally, the voltage-drop to near zero makes the LC-tank a suitable choice for the low voltage circuit design. The total DC-drop for the sufficient drain-source voltages in this *LNA* is merely 0.4V. Therefore, the function of a *LNA* can be achieved at a supply voltage of less than 1V.

If the transistors M_1 and M_2 are not matched ideally, the node *A* in Fig. 4.1 is no longer ideally short and open for differential and common mode signals, respectively. Using Monte Carlo simulations on 1-V *LNA* circuit and repeating it 30 times, the effects of the component mismatch are verified. The variations in the ΔW (channel width), ΔL (channel length), ΔV_{th} (threshold voltage) are set as ±0.03um, ±0.02um, and ±0.06V, respectively. The simulation result shows that at 2.43GHz the S_{21} variations for differential and common mode signals are 1.1 and 2.2 dB, respectively.

In this design, an individual *LNA* is fabricated and measured. Thus an output buffer is essential for measurement purposes. Two source-followers, which work as buffers, are connected to the differential output terminals of the *LNA*. The buffers cause signal attenuation, and this loss needs to be compensated for when measuring the gain of the *LNA*. Furthermore, the input impedance of the buffer is kept positive in

this design. Although the negative resistance can increase the equivalent Q value of the load of the *LNA*, increase to an excessive value may cause oscillation of the *LNA*. The device parameters of *LNA* are listed in Table 4.1.

4.2.2 RF Quadrature Generator (*RF-QG*)

In this design, a circuit comprising a phase shifter and a gain stage circuit is proposed to realize the *RF-QG*. The conceptual circuit of the phase shifter is illustrated in Fig. 4.3. The phase shifter consists of an inductor, a resistor and a capacitor. When the I-channel RF signal RF_I is applied to the input terminal, the output RF_Q of the phase shifter is

$$RF_Q = RF_I \cdot \left\{ \left(Z_R \parallel Z_C \right) \Big/ \left[\left(Z_R \parallel Z_C \right) + Z_L \right] \right\} = RF_I \cdot K_{EQ} \cdot \exp\left(j\theta_{EQ} \right) \tag{4.1}$$

$$K_{EQ} = 1 \Big/ \sqrt{\left(\omega^2 LC - 1 \right)^2 + \left(\omega L / R \right)^2} \tag{4.2}$$

$$\theta_{EQ} = \tan^{-1} \left\{ 1 \Big/ R \left[\left(\omega L \right)^{-1} - \omega C \right] \right\} \tag{4.3}$$

where Z_R, Z_L, and Z_C represent the values of the resistor, inductor and capacitor, respectively. K_{EQ} represents the amplitude ratio at nodes RF_I and RF_Q. θ_{EQ} represents the shifted phase at node RF_Q. Similar to the result in (3.18), the identical magnitude and 90^o phase shift can be realized between RF_I and RF_Q when (4.4) are satisfied.

$$\omega L = \frac{1}{\omega C} = R \quad \Rightarrow \quad \omega = \frac{1}{\sqrt{LC}}, \; R = \sqrt{\frac{L}{C}} \tag{4.4}$$

Except for the phase shifter, active circuits are used in the designed *RF-QG* to prevent the gain loss. Fig. 4.4 shows the circuit diagram of the proposed *RF-QG*. L_{PS}, R_{PS}, and C_{PS} represent the differential-type phase shifters and they are realized by a spiral-inductor, poly-resistor and PMOS, respectively. Additionally, C_{PS} functions as a varactor and its capacitance can be adjusted manually by varying the external voltage

VC.

Fig. 4.5 shows the simulated amplitude errors and the corresponding image rejection of the designed *RF-QG*. By varying the voltage *VC* between 0 and 0.64 V, the exact quadrature phase can be obtained and the amplitude error varies between -0.08dB and 0.06dB in the frequency range of approximately 2.4 to 2.48 GHz. The simulation result shows that a –45dB of image rejection can be achieved by the designed RF-QG.

The M_1~M_5 construct the gain stage of the RF-QG. If the phase shifter operates at the resonant frequency of $1/\sqrt{L_{PS}C_{PS}}$, the LC impedance vanishes and the load impedance is the summation of R_{PS} and the parasitic resistors of the inductors. Since the magnitude of the load impedance is critical to the gains of M_1 and M_2, two cross-coupled transistors M_3 and M_4 are added to enhance the impedance. The addition of the cross-coupled transistors generates a negative gm which boosts the equivalent load impedance at the drains of M_3 and M_4. In addition, M_3 and M_4 can increase the *CMRR* ability. For the common-mode signal, the equivalent load impedance is 1/gm and hence the gain of the common-mode signal can be reduced. A current source is not used at the source nodes of *M3* and *M4* because it will increase the equivalent impedance at the outputs for common mode signal and decrease *CMRR*. To avoid the oscillation of *RF-QG*, the value of negative gm is determined by compensating for the loss of the phase shifter only. The gain of the RF signal is largely contributed by the *LNA*. The *RF-QG* with no attenuation is adequate in the proposed design.

The Monte Carlo simulation on *RF-QG* circuit is performed thirty times to verify

the effects of component mismatch. The variations in the quality factor of inductors, resistors, and capacitors are set at ± 2, $\pm 10\%$, and $\pm 10\%$, respectively. The simulation result shows that at 2.48GHz, the image rejection value distributes from -38dB to -23dB. The information of device parameters is listed in Table 4.1.

4.2.3 Quadrature Voltage-Controlled Oscillator (*QVCO*)

The circuit of the quadrature voltage controlled oscillator (*QVCO*) is shown in the schematic diagram of Fig. 4.6. The 2.4-GHz *QVCO* comprises resonators, cross-couple transistors and inverters.

To maintain a low-voltage circuit, the LC-tanks L_1~L_4, C_1~C_4, and C_{V1}~C_{V2} function as both resonator components and loads. The inductors L_1~L_4 are realized by on-chip spiral inductors, while the varactors C_1~C_4 are realized by P+/N-well junction capacitors. The varactors are tuned via the controlled voltage *VC* to achieve the desired oscillation frequency. M_1~M_4 function as inverters to align four output signals to quadrature phases. Moreover, the cross-coupled transistors M_5~M_8 generate negative gm to cancel the parasitic resistances at outputs so as to ensure oscillation. Because the sources of the mixer transistors load the *VCO* tanks, larger negative transconductances are needed to overcome the decay of LO amplitude and a decrease in the phase noise performance. In this design, the simulated LO amplitude is 1.05V and the phase noise of the QVCO is -107dBc/Hz at an offset of 1MHz.

Using Monte Carlo simulations on *QVCO* circuit and repeating it 30 times, the effects of the component mismatch are verified. The variations in the quality factor of inductors and resistors are set at ± 2, and $\pm 10\%$, respectively. The simulation result shows that the gain error varies between 0.02% and 1.72% and phase error distributes

from 0.001^{o} to 3.18^{o}, i.e. the image rejection varies between –57dB to –25dB. Table 4.1 lists the device parameters of *QVCO*.

4.2.4 Double-Quadrature Mixers (*DQ-Mixers*)

The proposed *QVCO* has equal DC levels that are close to those of the VDD. In order to connect to the output terminals of the *QVCO* without re-biasing, the *DQ-Mixers* use p-type transistors to realize the mixing function. Fig. 4.7 shows the circuit diagram, which combines the functions of *Mixer1* and *Mixer3* in Fig. 3.5. The output voltage $IF_I - \overline{IF_I}$ in Fig. 4.7 is similar to the derived result shown in (3.26) except the *R* in (3.26) should be replaced by the equivalent impedance at node IF_I ($\overline{IF_I}$).

As seen from (3.17), the *IRR* of the receiver depends on not only the accuracy of quadrature RF and LO signals but also on the degree of matching between the transistors of *DQ-Mixers* in I/Q paths. Actually, the device-mismatch of *DQ-Mixers* dominates the *IRR* of the *DQR*. Therefore, the channel-lengths of M_1~M_8 are the key points for mismatch consideration because larger devices exhibit smaller mismatches. Although designing the PMOS devices with longer channels can reduce the variation, the conversion gain of the *DQ-Mixers* is simultaneously decreased. Additional power is needed to avoid the gain attenuation. Thus, a trade-off must be made among IRR_{DQR}, conversion gain, and power consumption. The effects of component mismatch are verified by the thirty Monte Carlo simulations performed on DQ-Mixers circuit. With the channel-length variation set as $\pm 5\%$, the simulation result shows that the image rejection varies between –55dB to –25dB.

Two NMOS transistors M_9~M_{10} are chosen as the DQ-Mixer load. The NMOS devices operating in the linear region provide sufficient load impedances and low drain-source voltage drop. Table 4.1 lists the device parameters of the *DQ-Mixers*.

4.3 EXPERIMENTAL RESULTS

This section shows the experimental results of an individual *LNA* and a *DQR* chips. The *DQR* chip integrates an *LNA*, an *RF-QG*, a *QVCO*, and *DQ-Mixers*. Both *LNA* and *DQR* chips are designed and fabricated in 0.25-μm CMOS technology.

In the chip measurement set-up, baluns and transformers are used for RF and IF terminal measurements. Signal attenuation caused by the baluns and transformers is measured and compensated for in the experimental results. For the inductance variation of bond-wires, series discrete inductors are employed to compensate for the input matching.

4.3.1 1-V 2.4-GHz Low-Noise Amplifier

Fig. 4.8 shows the die micrograph of the fabricated individual *LNA*. The *LNA* consumes 4mW at a supplied voltage of 1V. At 2.42GHz and with 4.7nH external matching inductors, the S11 and S22 of *LNA* are below –19 dB and –17 dB, respectively. Fig. 4.9 and Fig. 4.10 show the measured S21 and common-mode gain of the *LNA*. When the attenuation loss caused by the output buffers and two baluns are compensated for, the core *LNA* achieves the desired signal gain of 17 dB and the common-mode signal gain of –12 dB. This means the *LNA* can achieve 29dB of common-mode rejection ratio (*CMRR*). Fig. 4.11 shows the measured noise figure of the fabricated *LNA* where 5.5 dB can be achieved at 2.44GHz. Fig. 4.12 shows the

results of the two-tone test, where the loss of external components has been compensated. The measured *IIP3* of *LNA* is –9 dBm. Table 4.2 lists the overall measurement results of the fabricated individual *LNA*.

4.3.2 1-V 2.4-GHz Double-Quadrature Receiver

The chip with the integration of a *LNA*, a *RF-QG*, a *QVCO* and *DQ-Mixers* is measured. Fig. 4.13 shows the die micrograph of the fabricated *DQR*. The *DQR* consumes 34.6mW at a supplied voltage of 1V. The measured S11 at 2.44 GHz is –21 dB. Fig. 4.14 shows the measured spectrum at the output of *DQR*. Markers 1~3 in Fig. 4.14 denote the RF feedthrough, LO leakage and the desired IF signal, respectively. The –61.51dBm of RF feedthrough and –55.71dBm of LO leakage are caused by the mismatch of mixers and substrate couple. The measured gain of the fabricated *DQR* is 12dB. The measured *IIP3* is shown in Fig. 4.15, where –12 dBm of *IIP3* reveals that the *DQR* can perform sufficient linearity. Fig. 4.16 shows the *IRR* of the two samples of the *DQR* chip, where 31.3 and 27.5 dB of *IRR* are measured at 2.4GHz. The maximum variation of *IRR* from 2.4 to 2.48 GHz is 4.7dB. If a polyphase filter with 40dB of image rejection ratio is connected after the designed *DQR*, the image rejection ratio of the overall receiver can be calculated to be 30.8 and 27.3 dB, respectively.

In the experimental chip, the measured dc current of the fabricated DQR is found to be smaller than that in the simulation. This would mean that the transistor parameters in the fabricated DQR chip may have shifted to the slow corner. The smaller dc current reduces the amplitude of negative gm in *QVCO* and hence lowers the LO amplitude. The small LO amplitude not only decreases the conversion gain of

DQ-Mixers but it also increases the switching noise. This caused an increase in the measured noise figure to 21dB and a reduction in the gain by the *DQR* to 12dB. A modified design on *DQR* is performed. The simulation shows that when the dimensions of M_5~M_8 in Fig. 4.6 are increased to 90/0.24um in order to achieve a larger negative gm amplitude, the noise figure can be reduced to 11.5dB. Furthermore, as the dimensions of M_9~M_{10} in Fig. 4.7 are increased to 240/0.48um, the effect of flicker noise is reduced and resulting in a further decrease in the noise figure to 10 dB. The gain of the modified *DQR* is increased to 17dB. Since the dimensions of M_9~M_{10} are increased, the output bandwidth should be verified because larger parasitic capacitors at the output nodes may lower the pole frequency. HSPICE simulation shows the output bandwidth of the modified *DQ-Mixers* is 720MHz, which is still larger than the IF frequency 80MHz. Table 4.2 lists the overall measurement results of the fabricated *DQR*, the simulated results of the modified *DQR*, and the requirements of Bluetooth. As seen from Table 4.2, the results of the modified design are suitable for Bluetooth applications.

4.4 SUMMARY

A 1-V 2.4-GHz double-quadrature receiver, which includes a *LNA*, a RF quadrature generator, double-quadrature mixers, and a quadrature *VCO* has been designed, fabricated and measured. In the *LNA* design, common-source configuration is used to optimize the performance and a LC-tank is used as the common-mode source degenerator. The tank achieves high impedance at the desired frequency band and causes no DC drop to achieve the 1-V operation while enhancing common-mode rejection. A one-stage RLC phase shifter with cross-couple transistors is employed to realize the RF quadrature generator. The phase shifter generates the required

quadrature signals while the cross-couple transistors are used to increase the load impedances so as to reduce the power consumption. The performances of the individual *LNA* and *DQR* are verified through measurements of the fabricated chips in 0.25um 1P5M CMOS technology. The measurements in the *LNA* show a 5.5dB of noise figure and a common-mode rejection ratio of 29 dB can be achieved. The *LNA* consumes only 4.0mW at a supplied voltage of 1V. The fabricated *DQR* achieves a 31.3dB of image rejection ratio at 2.4GHz. Furthermore, at 2.42GHz the measured voltage gain is 12dB and the IIP3 is -12dBm. The power dissipation is 34.6mW at a supplied voltage of 1V and the active chip area is $1.8\times1.6mm^2$. Measurement results have shown that the proposed low-voltage double-quadrature receiver is suitable for low-power wireless communication applications.

Table 4.1

Device Parameters of the 1-V Double-Quadrature Receiver.

Low-Noise Amplifier	
M_1、M_2	180 um / 0.24 um
M_3、M_4	90 um / 0.24 um
L_{S1}、L_{S2}	3.7 nH
L_{d1}、L_{d2}	3.7 nH
L_S	2.2 nH
C_d	0.32 pF
C_S	0.50 pF
R_b	2 kΩ
RF Quadrature Generator	
M_1、M_2	420 um / 0.24 um
M_3、M_4	90 um / 0.24 um
M_5	660 um / 0.35 um
L_{PS}	2.2 nH
R_{PS}	41 Ω
VB1	0.89V
VB2	0.75V
Quadrature VCO	
M_1~M_4	20 um / 0.24 um
M_5~M_8	50 um / 0.24 um
C_{v1}、C_{v2}	0.27 pF
L_1~L_4	2.2 nH
Double-Quadrature Mixers	
M_1~M_8	20 um / 0.30 um
M_9~M_{10}	90 um / 0.24 um
VB	0.62V

Table 4.2

Experimental Results of *LNA* and 1-V Double-Quadrature Receiver

Low-Noise Amplifier			
Technology	0.25 um 1P5M		
Chip area	1.2×1.0 mm^2		
Power supply	1.0 V		
Frequency	2.4 GHz		
S11	-19 dB		
Gain	17 dB		
Common-mode gain	-12 dB		
Noise figure	5.5 dB		
S22	-17 dB		
IIP3	-8 dBm		
Power consumption	4.0 mW		
Double-Quadrature Receiver			
	Measured	Modified	Bluetooth Spec.
Technology	0.25 um 1P5M		-
Power supply	1.0 V		-
RF frequency	2.4 GHz		2.4 ~ 2.48 GHz
IF frequency	80 MHz		-
S11	-20 dB	-20	-
Gain	12 dB	17dB	-
Noise figure	21 dB	10dB	32dB
IRR	31.3 dB	-	-
IIP3	-12 dBm	-15dBm	-20dB
Power consumption	34.6 mW	46.3 mW	-
Chip area	1.8×1.6 mm^2	-	-

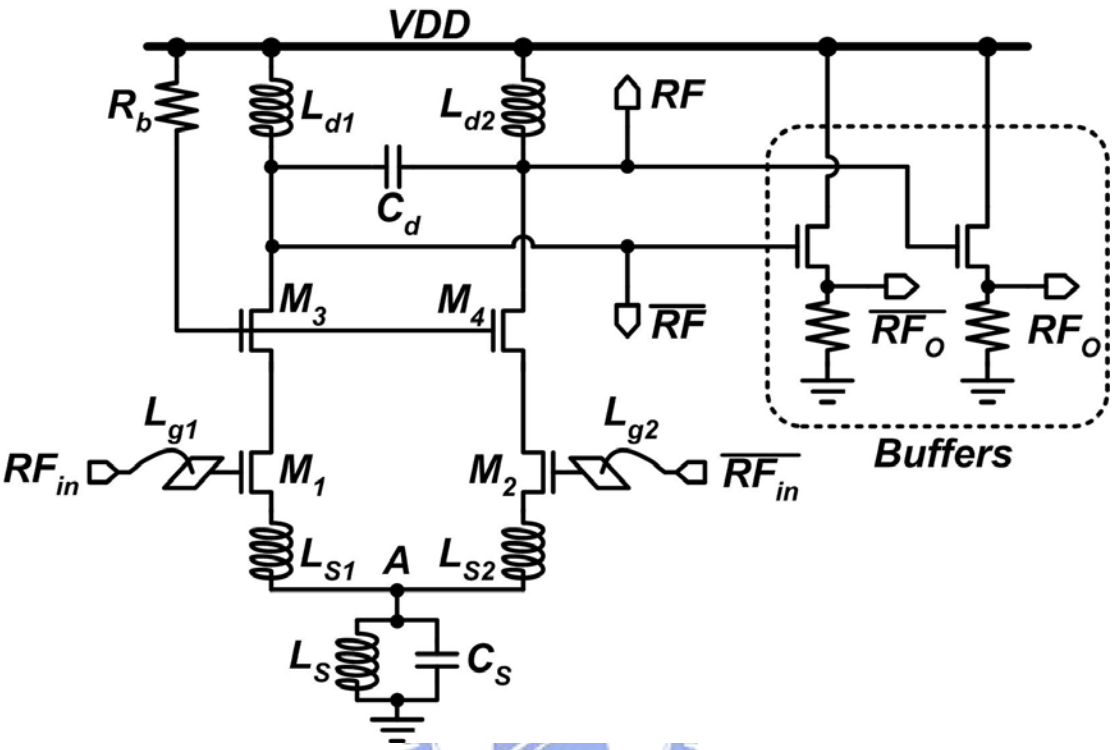
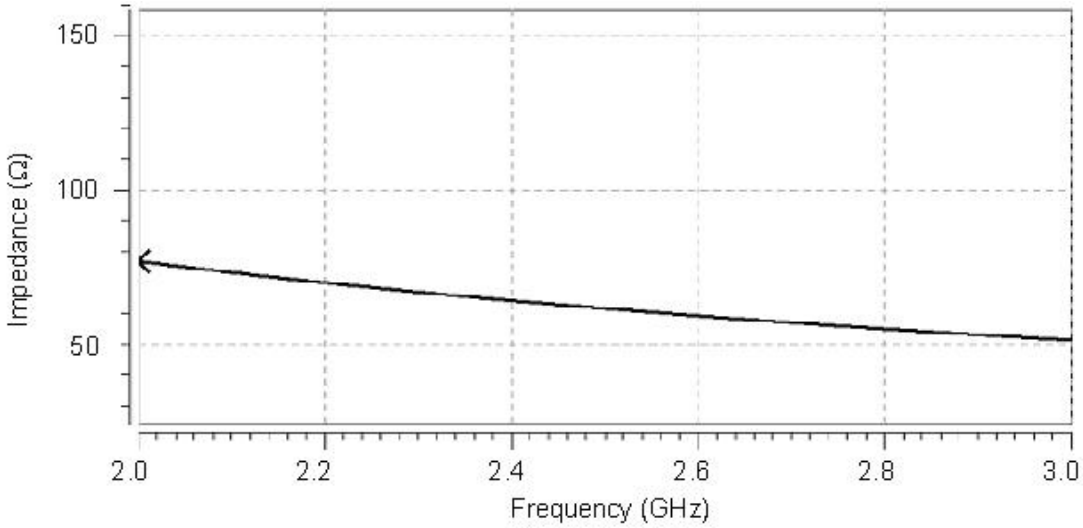
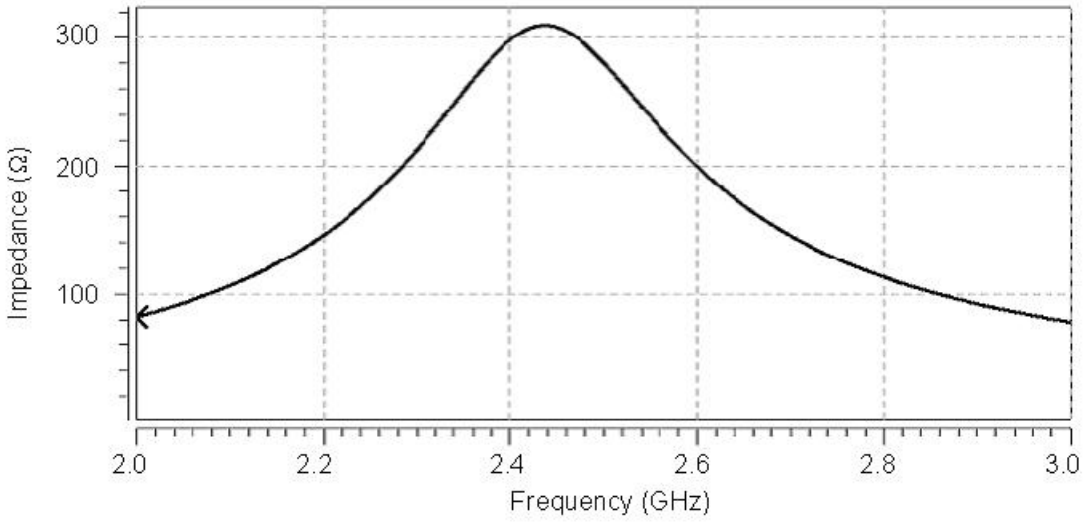


Fig. 4.1 Circuit diagram of the designed individual low-noise amplifier (*LNA*).



(a)



(b)

Fig. 4.2 Simulated impedance at the coupled-source node of differential low-noise amplifiers (*LNAs*) with (a) MOS current source and (b) LC-tank.

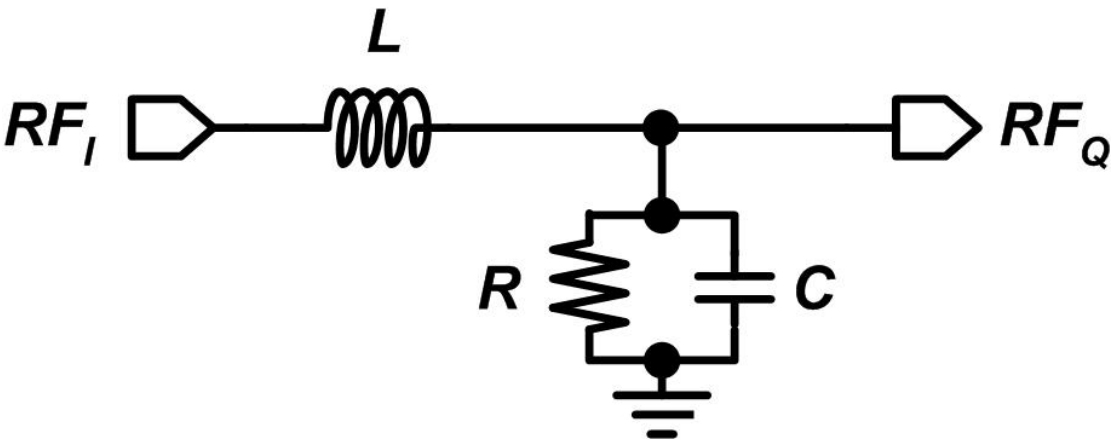


Fig. 4.3 RLC phase shifter.

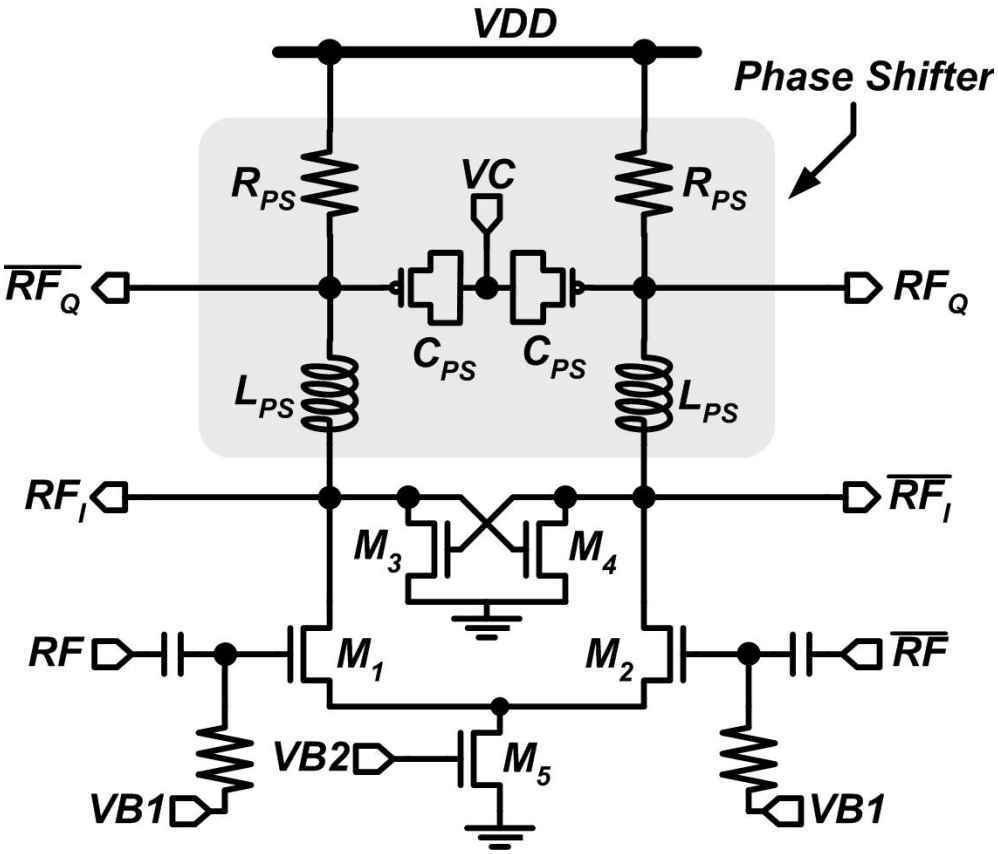


Fig. 4.4 Circuit diagram of the RF quadrature generator (*RF-QG*).

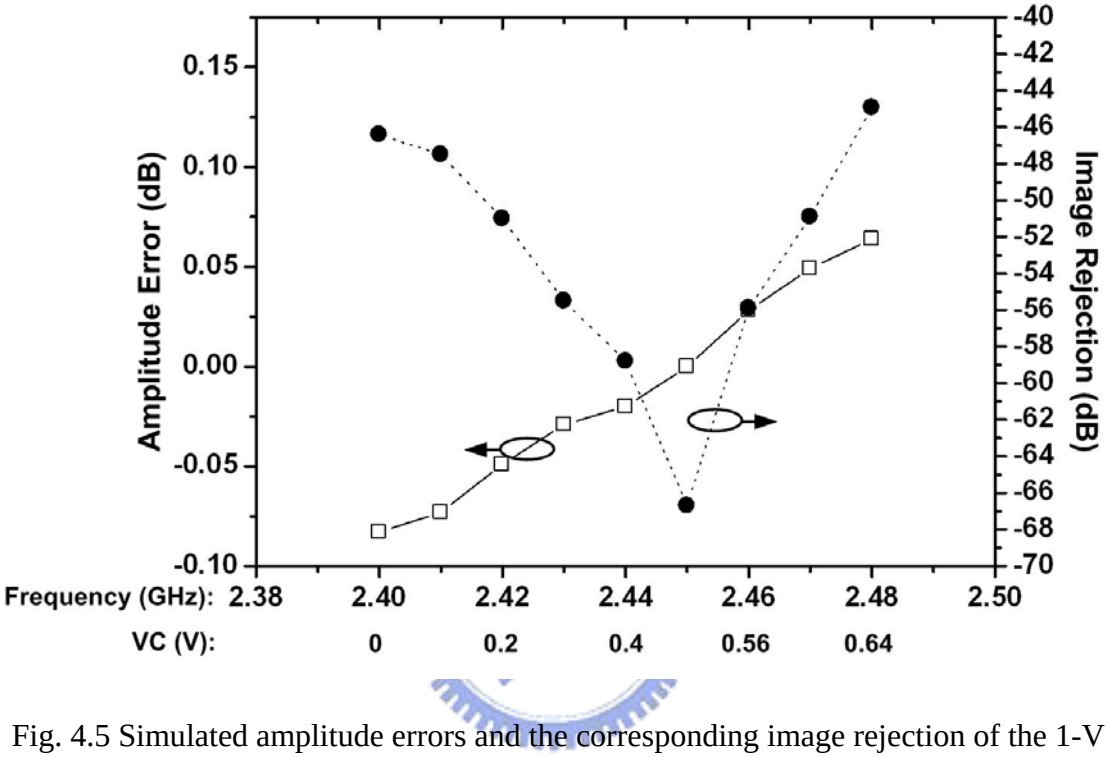


Fig. 4.5 Simulated amplitude errors and the corresponding image rejection of the 1-V RF-QG

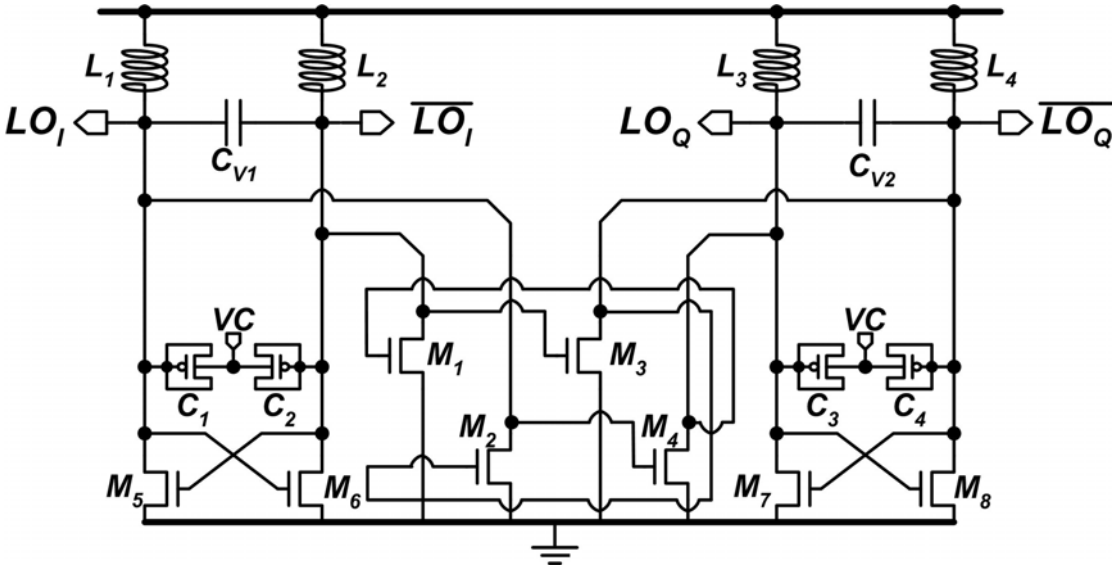


Fig. 4.6 Circuit diagram of the quadrature voltage-controlled oscillator (*QVCO*).

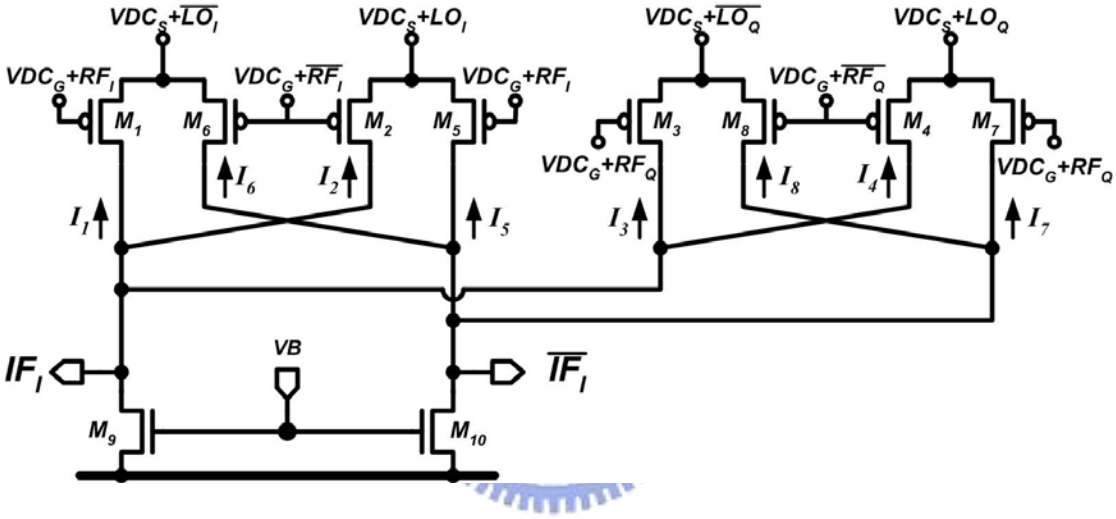


Fig. 4.7 Circuit diagram, which combines the functions of *Mixer1* and *Mixer3* in Fig. 3.5.

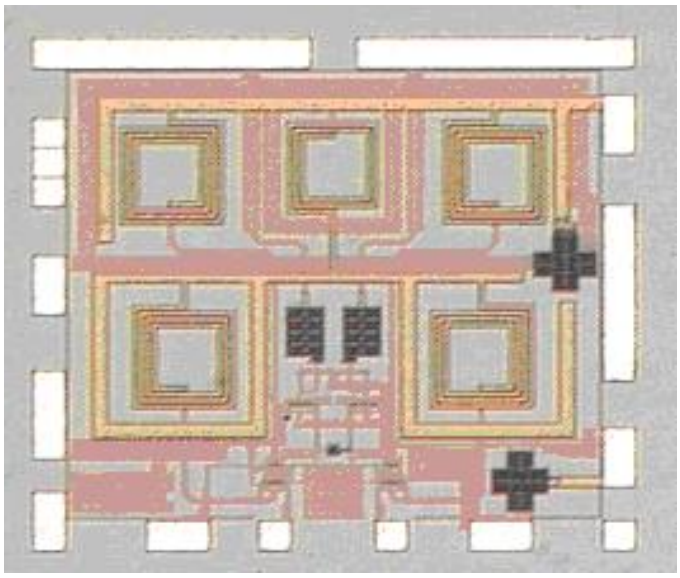


Fig. 4.8 Die micrograph of the fabricated *LNA* in 0.25-μm CMOS technology.

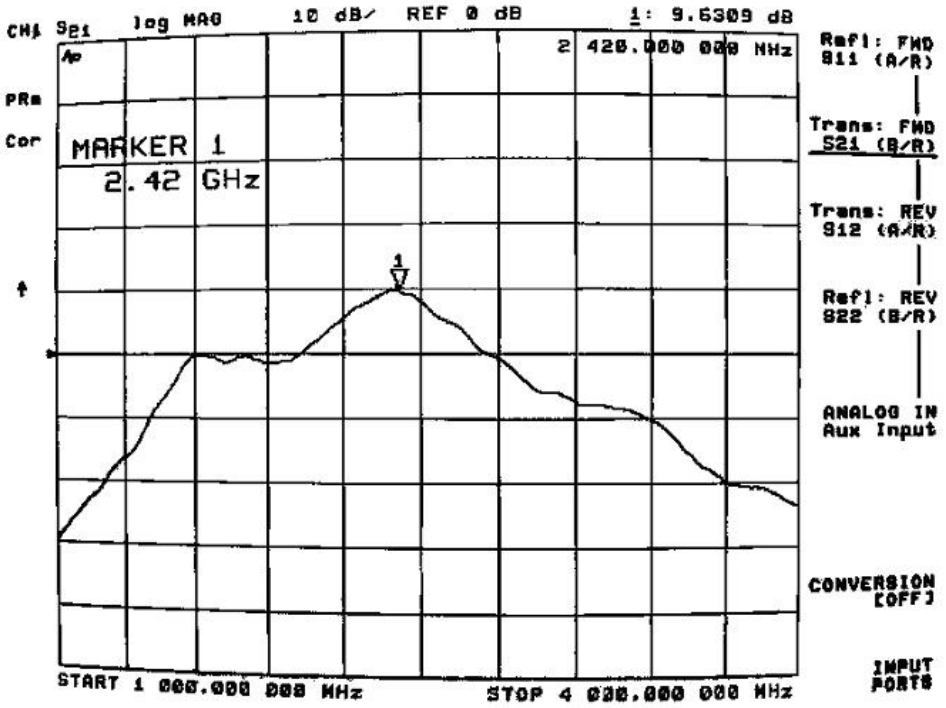


Fig. 4.9 Measured S21 of 1-V 2.4-GHz low-noise amplifier

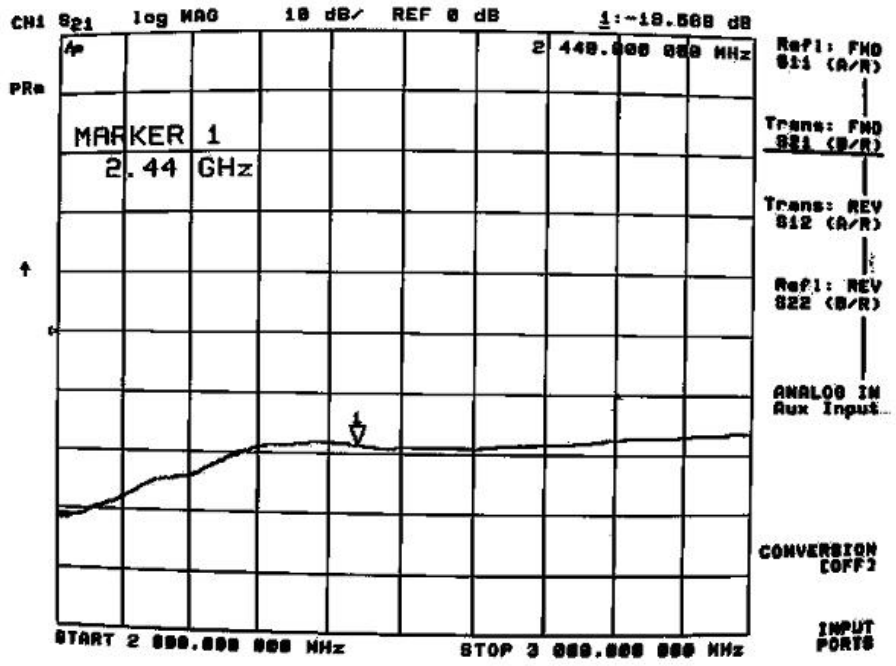


Fig. 4.10 Measured common-mode gain of 1-V 2.4-GHz low-noise amplifier

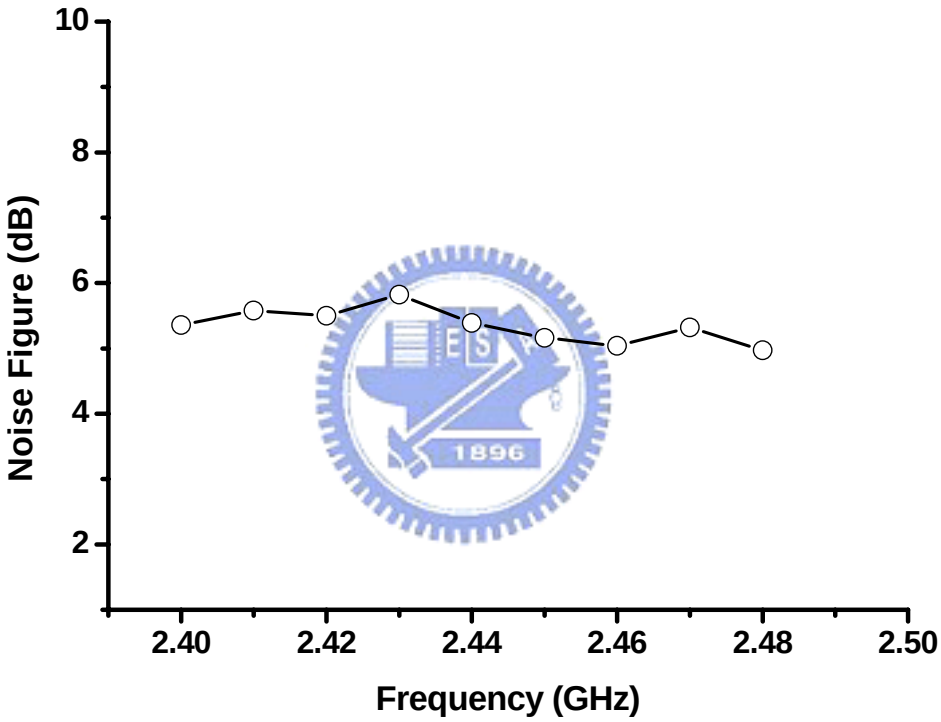


Fig. 4.11 Measured noise figure of 1-V 2.4-GHz low-noise amplifier

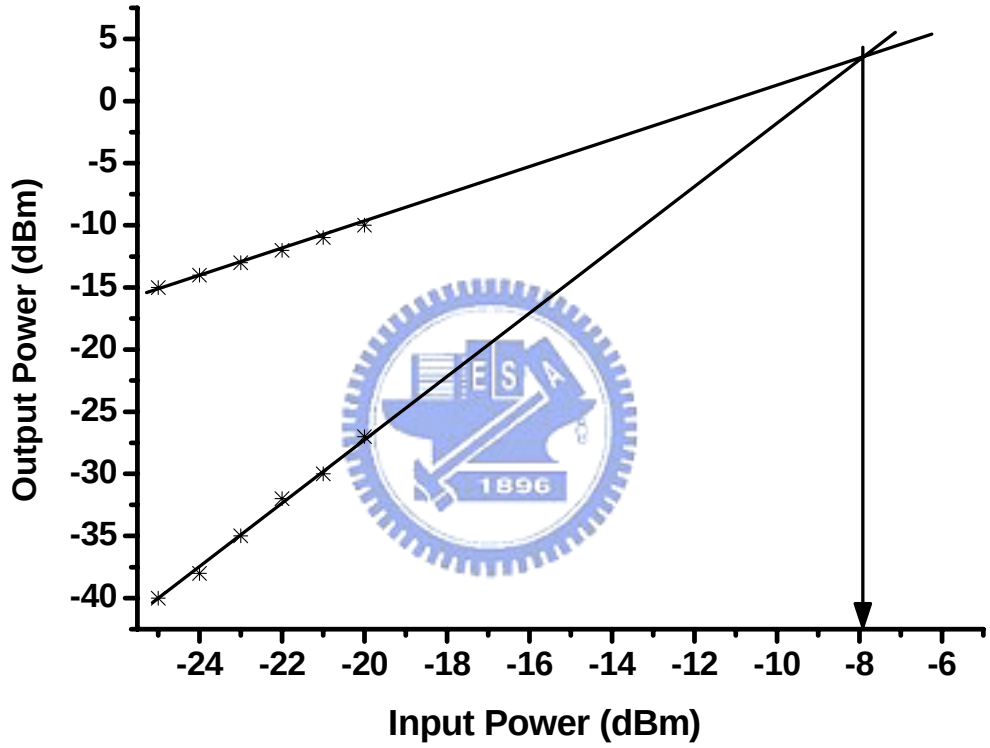


Fig. 4.12 Measured *IIP3* of 1-V 2.4-GHz low-noise amplifier

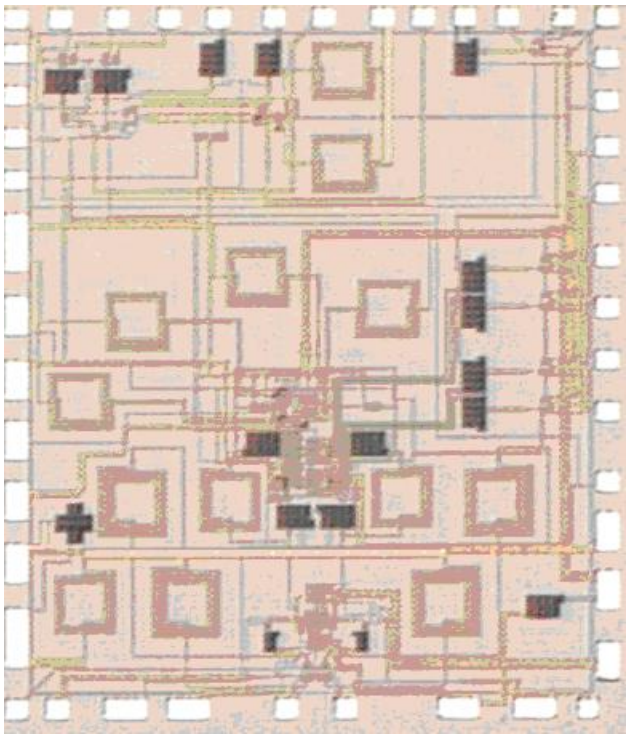


Fig. 4.13 Die micrograph of the fabricated *DQR* in 0.25-μm CMOS technology

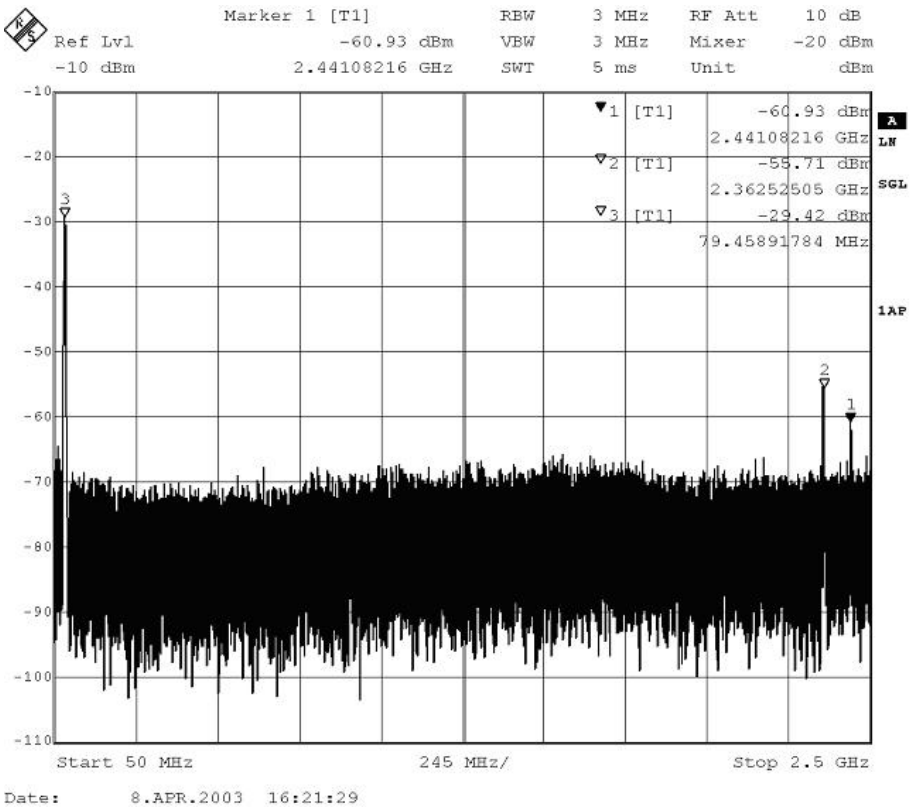


Fig. 4.14 Output spectrum of the *DQR*

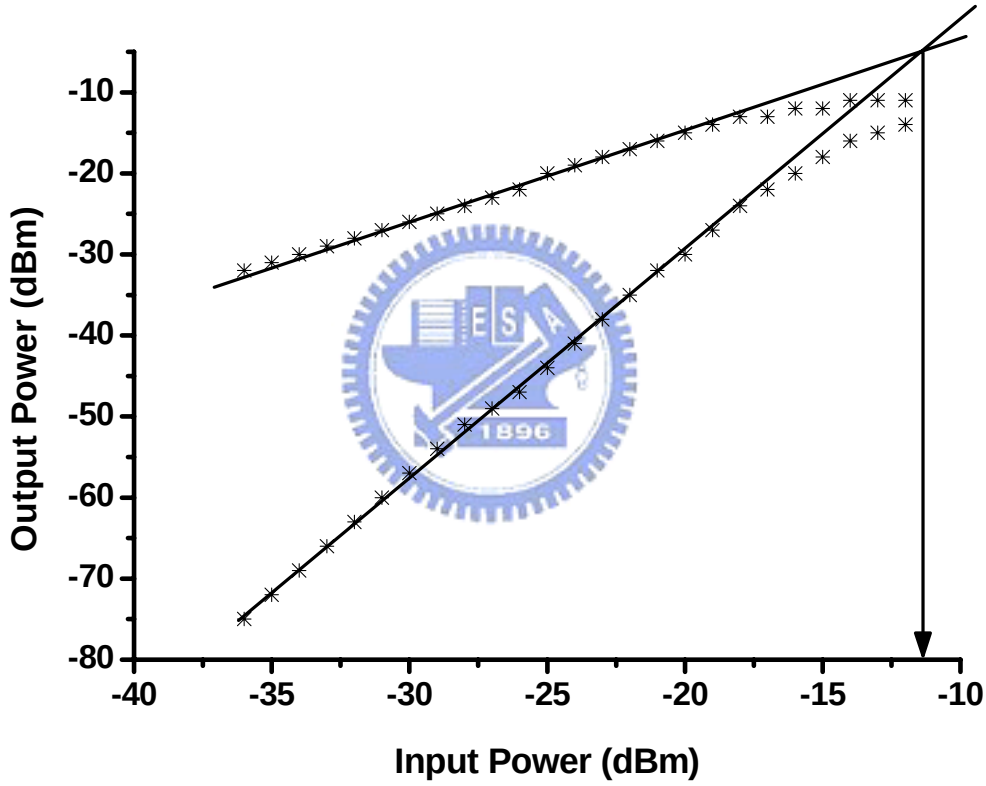


Fig. 4.15 Measured *IIP3* of the *DQR*

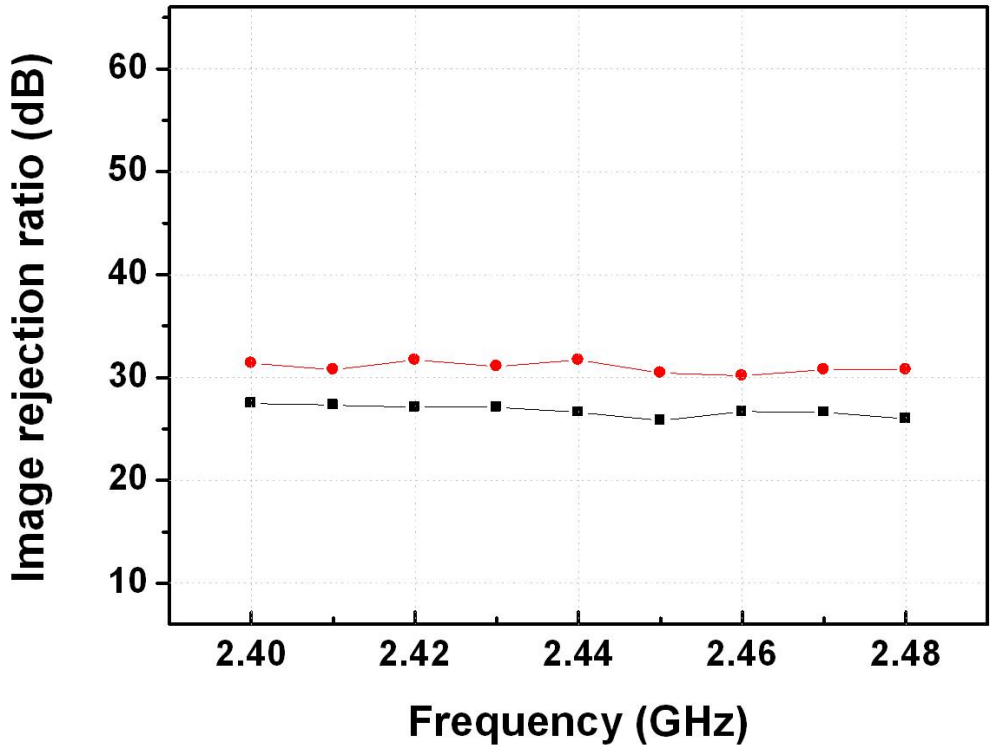


Fig. 4.16 Measured image rejection ratio of the *DQR*