CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 MAIN RESULTS OF THIS THESIS

In this thesis, the design methodologies and implementation techniques of two double quadrature receiver front-ends are presented.

First, a wideband and low-power active polyphase filter has been proposed and analyzed. In the proposed polyphase filter structure, the currents mirrored from capacitors and the transistors in a single-stage are used to realize high-pass and low-pass functions, respectively. Simple single-stage filter circuit and directly cascaded multi-stage structure achieve the wideband performance. Without inter-stage buffer, the power dissipation is kept low. Furthermore, a constant-gm bias circuit is employed to decrease the sensitivity of image rejection to temperature and process variations. Due to the advantage of current-mode operation, the proposed active polyphase filter has been successfully modified to fit the operation of 1V power supply. The performances of the filter have been verified through measurement on the fabricated chip in 0.25-um 1P5M CMOS technology. It has been shown from measurement results that the proposed active polyphase filter is suitable in wireless communication applications.

Secondly, a 1.8-V low-power 5-GHz CMOS receiver front-end for IEEE 802.11a wireless LAN system is proposed. Double-quadrature architecture in the proposed receiver is adopted and analyzed. The receiver consists of a low-noise amplifier, an

RF quadrature generator, double-quadrature mixers, a quadrature VCO, and an active four-stage polyphase filter. A new one-stage RLC phase shifter is employed to generate quadrature RF signals. Using the current reuse technique, double-quadrature mixers are merged with quadrature VCO. The power consumption is thus reduced obviously in the current reuse structure. The four-stage polyphase filter is integrated in the receiver to reject image signals. The receiver provides the advantages of low power dissipation, a small chip area, and a low sensitivity to parasitic components. The measured results have shown that the proposed receiver is suitable for IEEE 802.11a wireless LAN applications.

Finally, a 1-V 2.4-GHz CMOS double-quadrature receiver is proposed and analyzed. The double-quadrature receiver comprises a new low-noise amplifier, a new RF quadrature generator, a quadrature voltage-controlled oscillator, and double-quadrature mixers. In the *LNA* design, common-source configuration is used to optimize the performance and a LC-tank is used as the common-mode source degenerator. The LC-tank achieves high impedance at the desired frequency band and causes no DC drop to achieve 1-V operation while enhancing common-mode rejection. These characteristics make it suitable for high frequency and low-voltage design. A one-stage RLC phase shifter with cross-couple transistors is employed to realize the 2.4-GHz RF quadrature generator. The gain of the RF quadrature generator can be enhanced by negative transconductance and the power consumption can be reduced. The double-quadrature receiver is fabricated with 0.25-μm CMOS 1P5M technology. Measurement results have shown that the proposed low-voltage double-quadrature receiver is suitable for low-power portable wireless communication applications.

In summary, the double-quadrature architecture is capable of achieving high image rejection. Since image signals are rejected at low IF frequency, the cost can be reduced because the external high-Q RF filters are not required. Using the proposed new circuits to realize the double-quadrature receiver, the power consumption can be reduced and performance can still be maintained. Since the advance in scaling CMOS technology has reduced the threshold voltage of MOSFETs and increased its unit-gain frequency, it is quite feasible to design high-performance high-frequency low-voltage high-integration double-quadrature receiver front-ends by using the advanced CMOS technology and integrate them with the baseband signal processing VLSI.

5.2 FUTURE WORKS

The simulation and measurement results have shown that the active polyphase filter can achieve high image rejection. However, the wireless receiver deals with not only image interferers but also adjacent-channel interferers and harmonics caused by previous circuits. Therefore, the channel selectivity is required at the IF stage. To select the desired signal from interferers, a channel-select filter will be added to the double-quadrature architecture after the polyphase filters in the future. Although the constant-gm bias can stabilize the variations to some degree, a tolerance on the rejection bandwidth is still required in designing the polyphase filter. To achieve a more precise rejection bandwidth, auto-tuning circuits can be incorporated to adjust the pole frequency in each stage of the polyphase filter.

In the 5-GHz double-quadrature receiver, the unbalances between I/Q LO signals are of little significance and the image rejection is mainly determined by mismatches in mixers. Even the achieved image rejection in the proposed receiver is excellent in

comparison with other proposed receivers, it still doesn't meet the image rejection requirement of IEEE 802.11a. To achieve a more image rejection ability, the calibration technique for phases and gains of mixers can be adopted. In the calibration circuits, currents of mixers can be adjusted by feedback signals measured from outputs of mixers or from baseband processing. The mixers are calibrated during preamble time and therefore the mismatches will be reduced when signals are processing.

In the implementation of 1-V 2.4-GHz double-quadrature receiver, gain control technique can be incorporated to improve the linearity. Linearity is the most difficult specification to achieve in designing a low-voltage receiver. To decode the minimum sensitivity signal, a sufficient gain should be provided by the receiver. Since headroom is strictly limited in low-voltage circuits, high gain may saturate later circuits when a maximum signal or high-power blockings received. To handle the large signals, sufficient linearity is necessary. The expense to maintain linearity is usually the increasing of currents. To solve the problem, the gain control scheme is a suitable technique in low-voltage design. The gain can be distributed to multi-stage *LNAs* or by adjusting currents of mixers. Thus the circuits are operated at high gain when weak signals are received but operated at low gain for strong signals. This technique can be implemented in the future.