

用於雙頻帶 802.11a-802.11b 無線網路系統 之可程式增益放大器電路設計

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摘 要

本篇論文主旨在藉由電路的設計及模擬，實現一個適用於雙頻帶 802.11a-802.11b 無線網路系統之可程式增益放大器，具有高頻寬，低雜訊，直流誤差補償，易於控制增益大小的優點。此設計是採用四級差動放大器的架構來達到系統要求，增益範圍設計在 0dB 到 60dB，最低增益步階為 1dB。在高增益的情況下等效輸入雜訊電壓 V_n 僅 6.5nV/sqrtHZ，頻寬仍可達 125MHz。

本論本中所提出的可程式增益放大器，是以安捷倫 ADS 軟體模擬，並以聯華電子 0.18 微米金氧半製程實現，此製程具有一層複晶矽和六層金屬。當操作在 1.8 伏特電源電壓時，整個晶片僅消耗 3.73mW (含四級可程式增益放大器，相關偏壓電路及直流誤差消除電路等，不含 3.3 伏特的輸出驅動電路)，在除能的狀態下消耗 3.6uW，晶片面積僅為 0.01mm²。

本論文實現了一個低雜訊，高頻寬的可程式增益放大器。其可實現於一個低成本，低消耗功率及易於整合的相關應用。

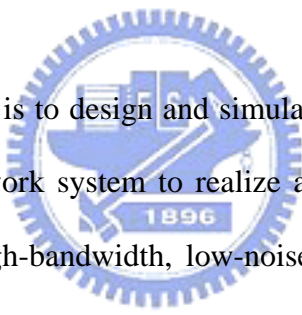
CMOS Programmable Gain Amplifier Design for Dual Band 802.11a-802.11b Wireless Network System

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ABSTRACT



The purpose of this thesis is to design and simulate a reliable circuit suit for Dual-Band 802.11a-802.11b wireless network system to realize a programmable gain amplifier, which includes the advantages of high-bandwidth, low-noise, DC-Offset-Cancellation feature and easy to control the gain setting. Using four Gain-Amplifier cascade architecture on circuit achieves the system requirement that the gain range is 0~60dB, with 1dB gain step. Input referred noise at high-gain mode is only 6.5nV/sqrtHZ, and bandwidth up to 125MHz.

The proposed circuit simulates with Agilent ADS tool, and the circuit is implemented with UMC 01.8um 1P6M CMOS process. The verification values approaches to the simulation results. It consumes only 3.73mW from a 1.8V supply voltage (includes 4-stage Gain-Amplifier, related bias circuit and DC-Offset-Cancellation circuit; the 3.3V output drive circuit is not include). The consumption of power-down mode is 3.6uW and die occupies 0.01mm².

In sum, this work presents a low-noise and high-bandwidth PGA circuit for a low cost, low power, and high-integration solutions.

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Contents

Abstract (Chinese)	I
Abstract (English)	II
Acknowledgments	III
Contents	IV
Table Captions	VI
Figure Captions	VII
Chapter 1 Introduction.....	1
1.1 Motivation.....	1
1.2 Thesis Organization.....	3
Chapter 2 Fundamentals of Gain Amplifier.....	4
2.1 Architecture of the Programmable Gain Amplifier.....	4
2.2 Related Requirement.....	8
2.3 Specification of PGA.....	12
Chapter 3 The Design of the Programmable Gain Amplifier.....	15
3.1 Design Consideration.....	15
3.2 Gain-Amplifier Design.....	17
3.3 Programmable Degeneration-Resistor Design.....	27
3.4 Common Mode Feedback Design.....	30



3.5 High-Pass Filter and DC-Offset-Cancellation Design.....	34
3.6 Digital Control Design.....	45
3.7 Output Buffer Design.....	49
3.8 Advantages of the Proposed PGA.....	50
Chapter 4 Implementation.....	51
4.1 Integrated Circuit Layout.....	52
4.2 ESD Protection.....	57
4.3 Package Issue.....	59
4.4 PCB Layout.....	60
Chapter 5 Measurement Results.....	62
5.1 Measurement Setup.....	62
5.2 Measurement Results.....	64
5.3 Summary.....	67
5.4 Debugs.....	68
Chapter 6 Conclusions and Future Works.....	70
6.1 Conclusions.....	70
6.2 Future Works.....	71
References.....	72



Table Captions

Table. 2.1	Target specifications for PGA.....	13
Table. 3.1	Temperature effect.....	26
Table. 3.2	Resistor process deviation effect.....	26
Table. 3.3	MOS process deviation effect.....	26
Table. 3.4	Noise voltage of the PGA in different gain setting.....	44
Table. 3.5	6-bits digital controlled gain setting table.....	48
Table. 4.1	Pin description of the PGA package.....	56
Table. 5.1	Measurement gain value versus gain setting.....	63
Table. 5.2	Performance summary of the PGA.....	67
Table. 5.3	Performance compare.....	67

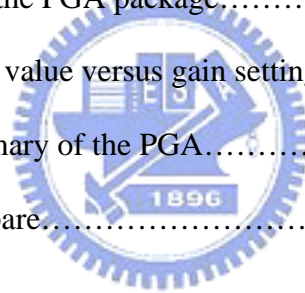


Figure Captions

Fig. 1.1	Dual-band system architecture.....	2
Fig. 2.1(a)	Analog controlled AGC loop.....	5
Fig. 2.1(b)	Digitally controlled AGC loop.....	5
Fig. 2.2	1-B compression curve.....	9
Fig. 2.3	Growth of output components IP3 test.....	10
Fig. 3.1	Basic degeneration differential pair.....	17
Fig. 3.2	Gain-amplifier of the PGA circuit.....	18
Fig. 3.3	Representation of output voltage limit.....	20
Fig. 3.4	The gain, phase and group delay of gain-amplifier.....	22
Fig. 3.5	1-dB compression of gain-amplifier at 0dB gain.....	23
Fig. 3.6	1-dB compression of gain-amplifier at 15dB gain.....	23
Fig. 3.7	Transient of gain-amplifier at 0dB gain.....	24
Fig. 3.8	Transient of gain-amplifier at 15dB gain.....	24
Fig. 3.9	IIP3 of gain-amplifier at 0dB gain.....	25
Fig. 3.10	OIP3 of gain-amplifier at 15dB gain.....	25
Fig. 3.11	Programmable degeneration resistor.....	28
Fig. 3.12	The degeneration resistor R_d value in different gain setting.....	29
Fig. 3.13	The amplifier of common-mode feedback with modified Miller compensation.....	31
Fig. 3.14	Bode plots of closed-loop gain-amplifier.....	32
Fig. 3.15	Simulation result of the close-loop gain amplifier.....	32

Fig. 3.16	PGA circuit with DC-offset cancellation.....	35
Fig. 3.17	The gain, phase and group delay of PGA.....	38
Fig. 3.18	1-dB compression of PGA at 0dB gain.....	39
Fig. 3.19	1-dB compression of PGA at 60dB gain.....	39
Fig. 3.20	1-dB compression of PGA at 3dB gain.....	40
Fig. 3.21	IIP3 of PGA at 0dB gain.....	41
Fig. 3.22	OIP3 of PGA at 60dB gain.....	41
Fig. 3.23	Gain curve of non-DC-offset-cancellation PGA when R3 has 1% mismatch	42
Fig. 3.24	Gain curve of DC-offset-cancellation PGA when R3 has 50% mismatch	42
Fig. 3.25	Gain curve of DC-offset-cancellation PGA when remove HPF with 1mV DC offset.....	43
Fig. 3.26	Gain curve of DC-offset-cancellation PGA when remove HPF with 1mV DC offset.....	43
Fig. 3.27	PGA settling time performance.....	44
Fig. 3.28	Ideal gain stage partition but not workable.....	45
Fig. 3.29	Recommend gain stage partition.....	45
Fig. 3.30	Another recommends gain stage partition.....	45
Fig. 3.31	The 6-bits to 16-bits decoder circuit.....	46
Fig. 3.32	6-bits input AND gate.....	47
Fig. 3.33	The PGA output buffer circuit.....	49
Fig. 4.1	Programmable-Gain-Amplifier Full Layout.....	54
Fig. 4.2	Single-stage Gain-Amplifier Layout.....	54
Fig. 4.3	6-bits to 16-bits Decoder Layout.....	55
Fig. 4.4	Output Driver Layout.....	55
Fig. 4.5	Fully Chip Layout and Pin Assignment Define.....	56

Fig. 4.6	ESD Protection Circuit.....	57
Fig. 4.7	Effective model of package pins.....	59
Fig. 4.8	PCB design for PGA package use.....	61
Fig. 5.1	Environment setup for testing.....	62
Fig. 5.2	Device under test PCB.....	63
Fig. 5.3	Measurement gain curve versus gain setting.....	65
Fig. 5.4	Measurement 1-dB compression of PGA at 0dB gain.....	65
Fig. 5.5	Measurement 1-dB compression of PGA at 60dB gain.....	66
Fig. 5.6	Resonate oscillation spectrum.....	68
Fig. 5.7	DC-offset-cancellation loop gain curve and phase curve, the cancellation capacitor is not connected.....	69
Fig. 5.8	DC-offset-cancellation loop gain curve and phase curve, the cancellation capacitor is connected.....	69

