Chapter 1
Introduction

1.1 Motivation

In modern communication receiver, the received signal is quantized by an analog to digital (ADC) so that complex signal processing can be performed in the digital domain. As shown in Fig.1.1, a programmable gain amplifier (PGA) is placed in front of the ADC, adapting the loss variation of the transmission channel in order to ease the dynamic range requirement for the ADC. Due to the low cost of digital signal processing in the deep-submicron technology, the gain of the PGA is digitally controlled by an automatic gain control (AGC) loop. The clock timing for the sampled-and-hold amplifier and ADC is extracted by the clock-recovery circuit, which is controlled by digital signal processing.

The linear-in-dB gain control for the PGA is usually required to achieve short settling time of the AGC loop [1]. Also the PGA needs to maintain its high linearity and low noise over the entire signal bandwidth as well as gain range. For solving these problems, the later chapters will have the discussion about these issues and the optimizations for the design of the programmable gain amplifier (PGA).

The purpose of this thesis is to design and simulate a high-speed high-linearity PGA circuit to meet the requirements of the dual-band 802.11a-802.11b wireless network system, which includes the advantages of high-bandwidth, low-noise, DC-offset-cancellation feature and easy to control the gain setting. In sum, this work presents a low-noise and high-bandwidth PGA circuit for a low cost, low power, and high-integration solutions.

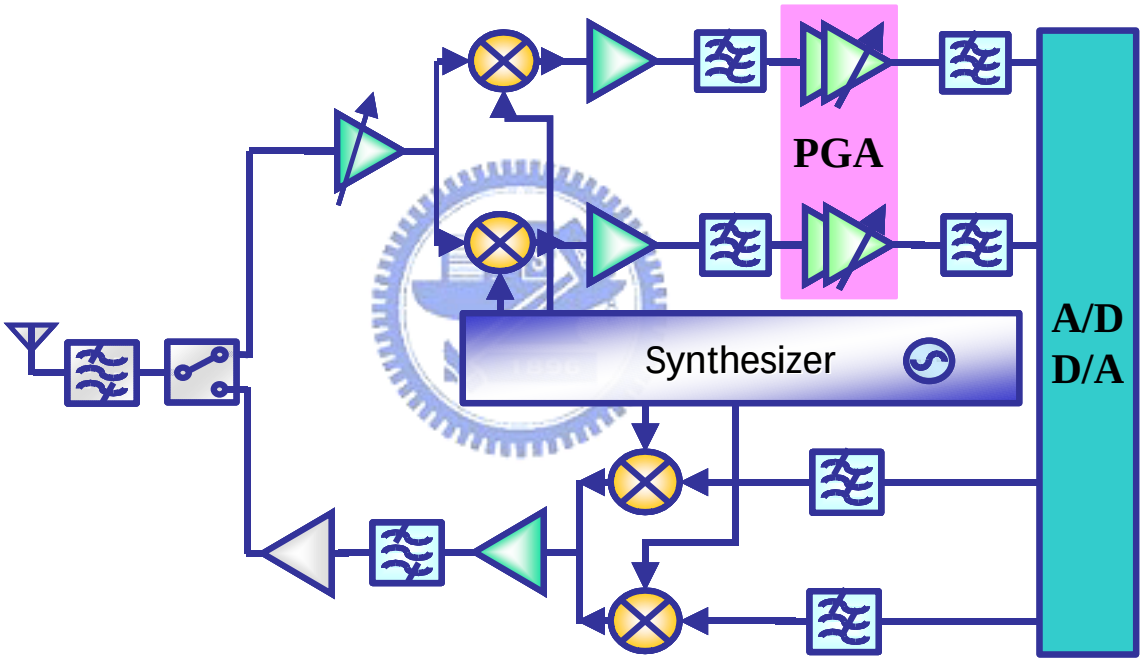


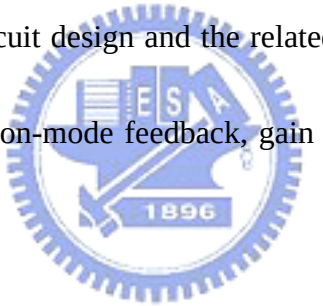
Fig.1.1 Dual-band system architecture

1.2 Thesis Organization

The content of this thesis is focused on design and implementation of CMOS PGA that applied for dual-band wireless network system. This thesis is organized in a sequence as listed in the following.

Chapter 2 discusses two type models of variable gain amplifier. It gives explanations to the advantage and feasibility of using digital controlled gain amplifier PGA. This chapter will also describe some basic concepts and the design specification.

Chapter 3 presents the circuit design and the related simulation results. Some topics are included in this chapter, common-mode feedback, gain partition, DC-offset-cancellation and high-pass filter feature.



Chapter 4 shows the implementation of the PGA. It includes detail chip layout, ESD protection, package model and PCB layout.

Chapter 5 shows the testing plan for measurement work, the measurement results, and the analysis of discussion toward the verified results.

Chapter 6 gives the conclusions and future works of the proposed PGA.

Chapter 2
Fundamentals of Gain Amplifier

Variable gain amplifier is one of the most popular building blocks used in a variety of circuits. It is employed in many applications in order to maximize the dynamic range of the overall system. The programmable gain amplifier (PGA) plays an important role in communication systems. It is an essential part of wireless transceivers as well. It has been discussed two type models of variable gain amplifier at beginning of this Chapter. The second, some basic concepts about PGA will be presented. The last, the design specification for PGA will be proposed.

2.1 Architecture of Programmable Gain Amplifier

The variable gain amplifier is typically employed in a feedback loop to realize automatic gain control (AGC), where the amplitude of an incoming signal can vary over a wide dynamic range. The role of the AGC circuit is to provide a relatively constant output amplitude so that circuits following the AGC circuit require less dynamic range.

A straightforward block diagram of an AGC loop in a mixed digital/analog chip is shown

in Fig.2.1(a). [5] The gain control of the AGC circuit is provided by baseband or digital circuit. The output signal of the baseband or digital circuit is converted to an analog voltage by the DAC. The exponential characteristic is obtained using special exponential conversion circuit. The output of this circuit is used as a gain control signal. One possibility is applied to a linear multiplier to multiply this gain control signal with the input. An additional base-band or digital circuit is needed for offset control, where it converts the digital offset word generated by the baseband or digital circuit to an analog value. The offset is subtracted from the input signal at the input terminal.

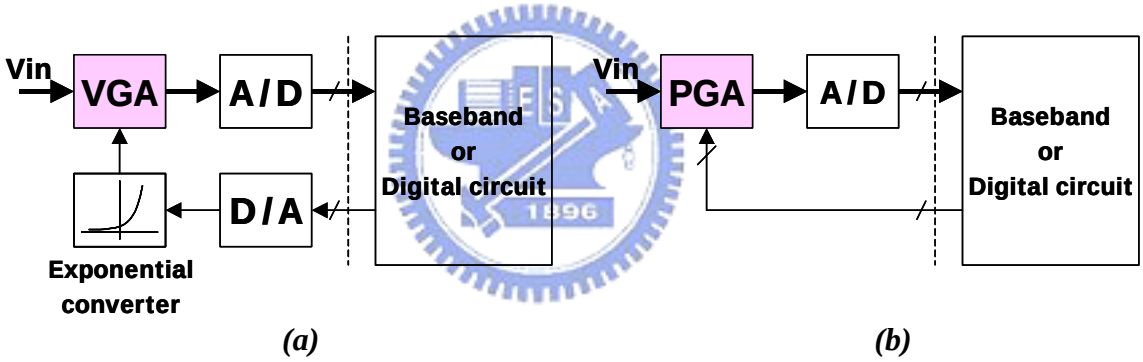


Fig.2.1 (a) Analog controlled AGC loop. (b) Digitally controlled AGP loop.

The approach developed in this article is shown in Fig.2.1 (b), where a single digitally controlled PGA block is required to provide a gain which is exponentially controlled by the digital word form the baseband or digital circuit. The PGA circuit is cascadable to achieve wider gain control range. A digitally controllable gain amplifier is desirable since the gain can be varied simply with switched devices according to the adjustment codes. Therefore, PGA, i.e. digitally controlled structure, has been used in many circuit implementations, which

are included and discussed in this chapter. VGA, which has an analog control signal, is not within the scope of this thesis and is not discussed here.

There are many ways to design a Gain Amplifier. However for different applications, many kinds of PGA have been developed [1] [2] [3] [4]. Among them, the design proposed by Mohamed A. I. Mostafa, Sherif H. K. Embabi, and Mostafa Elmala [3], has the highest operation frequency; however typically the bandwidth is limited to a small bandwidth, thus it is not suitable for design of PGA. The design proposed by Ahmed Emira [4] provides a large gain setting range but a lower bandwidth, also the input referred noise is too high. The bandwidth of the design proposed by J. J. F. Rijns [1] is too low. The design proposed by K. Philips and E. C. Dijkmans [2] has the best performance because of the bandwidth is much higher, but the gain range is not enough. Therefore, this thesis tries to implement a PGA with wider bandwidth and larger gain setting range. It will be discussed in detail in following chapters.

In this work, the PGA has been done based on the architecture that proposed by Mohamed A. I. Mostafa, Sherif H. K. Embabi, and Mostafa Elmala [3]. However, for wider operation bandwidth, smaller chip size, reduces circuit complicacy and also avoids senseless power consumption, the architecture is changed and the new architecture is shown in chapter3.

Another concept of exponential gain control is revealed recently to approximate the

logarithmic function:

$$gain = \left(\frac{1+x}{1-x}\right)^n \tag{2.1}$$

refer to the architecture that proposed by Po-Chiun Huang, Li-Yu Chiou and Chorng-Kuang Wang [6]. This technique is suit for analog control system since it can provide an approximate exponential gain curve, this is important in dB-linear application. Also the proposed circuit is not complex and easy to control. But it is not accurate since it is an "approximate" function and it may not suit for digital control system. In digital control system, an accurate gain-step is required in a closed AGC loop.

For application of wireless communication system, the large gain setting range is required. And because of the requirements of the system design, the auto gain control (AGC) will be generated by baseband. The amount of programmable gain depends on the receiver input signal range, and the accuracy and sampling rate in the analog-to-digital conversion. Most of the programmable gain must be implemented in the analog baseband circuit if an ADC with low or medium resolution is used, like 6 – 8 bits in receiver. Besides, there are some design issues for making the system. The DC-offset-cancellation feature is used for the suppression of the mismatches problems. The high-pass filter with a reasonable corner frequency to filter out DC offset from mixer output. These features will also be discussed in chapter3.

2.2 Related Requirement

The major consideration of the design parameter includes 1dB-Compression and third intercept point IP3, describe as bellowing.

1dB-Compression

While many analog and RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena. For simplicity, we limit our analysis to memoryless, time-variant systems and assume

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.1}$$

where *x(t)* is input and *y(t)* is the nonlinear system output.

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. In Eq. 2.1, if $x(t)=A\cos\omega t$, then

$$\begin{aligned} y(t) &= \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \\ &= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \end{aligned} \tag{2.2}$$

In Eq.2.2, the term with the input frequency is called the “fundamental” and the higher-order terms the “harmonics”. From the above expansion, we can make two

observations. First, even-order harmonics result from α_j with even *j* and vanish if the system has odd symmetry, i.e., if it is fully differential. In reality, however, mismatches corrupt the symmetry, yielding finite even-order harmonics. Second, the amplitude of the *n*-th harmonic grows approximately in proportion to A^n.

The small-signal gain of a circuit is usually obtained with the assumption that harmonics are negligible. For example, if $\alpha_1 A$ is much greater than all the other factors that contain *A*, then the small-signal gain is equal α_1. However, as the signal amplitude increases, the gain begins to vary. In fact, nonlinearity can be view as variation of the small-signal gain with the input level. This is evident from the term $3\alpha_1 A^3/4$ added to $\alpha_1 A$. In most circuits of interest, the output is a "compressive" function of the output; that is, the gain approaches zero for sufficiently high input level if α_3 <0. Written as $\alpha_1+3\alpha_1 A^2/4$, the gain is therefore a decreasing function of *A*. This effect is quantified by the "1-dB compression point", defined as the input signal level that causes the small-signal gain to drop by 1dB. If plotted on a log-log scale as a function of the input level, the output level falls below its ideal value by 1dB at the 1-dB compression point in Fig.2.2.

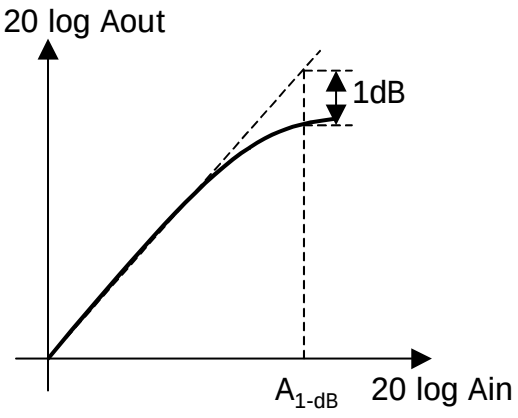


Fig.2.2 1-dB compression curve

To calculate the 1-dB compression point, we can write from Eq.(2.2)

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A^2{}_{1-dB}\right| = 20\log|\alpha_1| - 1dB \tag{2.3}$$

that is,

$$A_{1-dB} = \sqrt{0.145 \cdot \left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.4}$$

IP3, third intercept point

The corruption of signals due to third-order inter-modulation of two nearby interferers is so common and so critical that a performance metric has been defined to characterize this behavior. Called the "third interception point" IP3, this parameter is measured by a two-tone test in which A is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant and equal to α_1. As A increases, the fundamentals increase in proportion to A, whereas the third-order inter-modulation products increase in proportion to A^3 as shown if Fig.2.3(a). Plotted on a logarithmic scale is shown in Fig.2.3(b), the magnitude of the inter-modulation products grows at three times the rate at which the main components increase. The third-order intercept point is defined to be at the intersection of the two lines. The horizontal coordinate of this point is called the input IP3 (IIP3), and the vertical coordinate is called the output IP3 (OIP3).

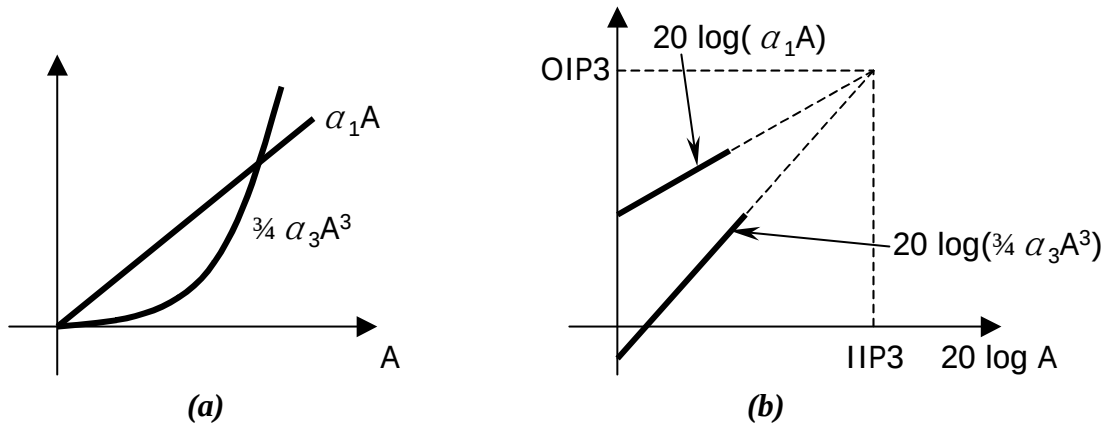


Fig.2.3 Growth of output components IP3 test

It is important to appreciate the advantage of IP3 over a simple inter-modulation measurement. If the magnitude of inter-modulation products (normalized to that of the carrier) is used as a measure of linearity, then the input amplitude with which the test is performed must be specified. The third intercept point, on the other hand, is a unique quantity that by itself can serve as a means of comparing the linearity of different circuits.

From the input-output characteristic of Eq.2.1, we can derive a simple expression for IP3. Let $x(t) = A\cos\omega_1 t + A\cos\omega_2 t$. Then,

$$y(t) = \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right)A\cos\omega_1 t + \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right)A\cos\omega_2 t + \frac{3}{4}\alpha_3 A^3\cos(2\omega_1 - \omega_2)t + \frac{3}{4}\alpha_3 A^3\cos(2\omega_2 - \omega_1)t + \cdots\cdots \tag{2.5}$$

If $\alpha_1 >> 9\alpha_3 A^2/4$, the input level for which the output components at ω_1 and ω_2 have the same amplitude as those at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 is given by

$$|\alpha_1| \cdot IIP3 = \frac{3}{4}|\alpha_3| \cdot IIP3^3 \tag{2.6}$$

Thus, the IIP3 is

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \qquad (2.7)$$
$$OIP3 = \alpha_1 \cdot IIP3$$

2.3 Specification for PGA

The proposed PGA is applied in dual-band 802.11a-802.11b wireless network system. Refer to the specification of dual-band system, the minimum receiver power is –82dBm. As the front-end band-pass filter (BPF) and transmitter/receiver switch insertion about 4dB loss, the receiver power of low-noise amplifier (LNA) is –86dBm. From the formula,

$$-86dBm = 10\log\frac{Pi\min}{1mW} \qquad (2.8)$$
$$\Rightarrow \quad Pi\min = 2.512\,pW$$

since the input impedance of LNA is 50ohm,

$$Pi\min = \frac{Vi'^{\,2}_{rms}}{50} \qquad (2.9)$$
$$\Rightarrow \quad Vi'_{rms} = 11.297uV$$

the LNA with 20dB gain and the following mixer provide 10dB gain, the amplitude of mixer output voltage is

$$Vo' = \sqrt{2}\cdot Vi'_{rms}\cdot 10^{\frac{30dB}{20dB}} \qquad (2.10)$$
$$\Rightarrow Vo' = 501.187uV$$

From our system architecture, the target output amplitude of PGA is 0.5V.

$$Gain,\max = 20\log\frac{0.5V}{501.187uV}$$
$$\Rightarrow \quad Gain,\max = 59.979dB \tag{2.11}$$

Also refer to the specification of dual-band system, the maximum receiver power is –10dBm. As the front-end band-pass filter (BPF) and transmitter/receiver switch insertion about 4dB loss, the receiver power of low-noise amplifier (LNA) is –14dBm. From the formula,

$$-14dBm = 10\log\frac{Pi\max}{1mW}$$
$$\Rightarrow \quad Pi\max = 39.811uW \tag{2.12}$$

since the input impedance of LNA is 50ohm,

$$Pi\max = \frac{Vi''_{rms}{}^2}{50}$$
$$\Rightarrow \quad Vi''_{rms} = 44.615mV \tag{2.13}$$

the LNA with 5dB gain and the following mixer provide 10dB gain, the amplitude of mixer output voltage is

$$Vo'' = \sqrt{2}\cdot Vi''_{rms}\cdot 10^{\frac{15dB}{20dB}}$$
$$\Rightarrow Vo'' = 0.35V \tag{2.14}$$

From our system architecture, the target output amplitude of PGA is 0.5V.

$$Gain,\min = 20\log\frac{0.5V}{0.35V}$$
$$\Rightarrow \quad Gain,\min = 3.098dB \tag{2.15}$$

so the require of minimum gain is 3dB, and the input 1-dB compression is 0.35V.

Following is the target specification on design phase.

Table 2.1 Target specifications for PGA

Item	Specification
Bandwidth	>12MHz
Gain Range	0~60 dB
Gain Step	1dB
Input Referred Noise	10 nV/√Hz
1dB-Compression	0.35V
Technology	0.18 μm CMOS
Supply Voltage	1.8V

Chapter 3
The Design of the Programmable Gain Amplifier

This chapter describes the design of the programmable gain amplifier (PGA). It has been organized as follows. Section 3.1 describes the design consideration of PGA. Section 3.2 analyzes single-stage gain-amplifier architecture. Section 3.3 describes the digital controlled degeneration-resistor structure. Section 3.4 analyzes the common-mode feedback feature. Section 3.5 contains the DC-offset-cancellation and high-pass filter features. Section 3.6 discusses the gain partition of each stage. Section 3.7 shows the output buffer design. The last, the advantages of the proposed PGA are given in Section 3.8.

3.1 Design Consideration

An important requirement for the PGA is a decibel-linear gain control characteristic, where the gain of the amplifier changes exponentially with the control signal. Another consideration in many PGA systems is the DC offset compensation. A small DC offset can be amplified by the PGA to a level that saturates the following stages or may cause the output

signal to be clipped. Thus, active compensation of the DC offset is an important part of PGA circuit design.

Some design features have to be concerned for PGA design include programmable gain range, gain step, frequency range, power consumption and chip size should be under consideration at one time. Besides, process variations, noise, mismatch and circuit nonlinearity and influence of layout should also be considered. Therefore, understandings of the CMOS circuit design and the characteristic of device are very important. The skill of circuit design and analysis will be discussed in this chapter. The PGA is implemented with 0.18um 1P6M mixed-mode CMOS process and operated in 1.8V supply voltage.

3.2 Gain-Amplifier Design

Gain-amplifier is the core module of the PGA system because the PGA system is generated by it, and the overall gain range and frequency bandwidth are typically dominated by it. Therefore, a good design of gain-amplifier will result in a better performance of PGA.

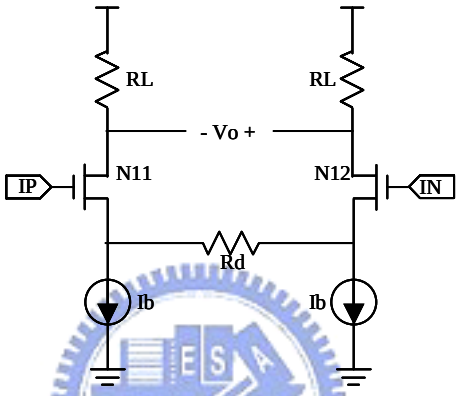


Fig.3.1 Basic degeneration differential pair

In order to get high precision gain steps and good linearity, fully differential degeneration differential amplifier is required. A standard topology for a differential gain amplifier is a degenerated differential pair with a resistive load as shown in Fig.3.1. The input stage N11 creating a linear voltage copy of the input signal form gate to source. The differential input voltage signal is converted to a differential current through the trans-conductance of the degenerated differential pair, which is given by

$$\frac{1}{gm_{diff}} = \frac{1}{gm_{11}} + \frac{Rd}{2}$$
$$\Rightarrow gm_{diff} = \frac{gm_{11}}{1 + gm_{11} \cdot \frac{Rd}{2}} \qquad (3.1)$$

therefore, the gain of this stage is

$$Gain = \frac{R_L}{\frac{R_d}{2} + \frac{1}{gm_{11}}} \tag{3.2}$$

By changing the ratio of the load and degeneration resistors, this circuit can provide both amplification and attenuation. The gain-amplifier schematic is shown in Fig.3.2. The linearized differential signal current can easily be copied to output stage with a matched device N51. The output current of the gm boosting circuit is mirrored from N21 to N51 and is converted to voltage through the load resistor RL1. The degeneration resistor (Rd) is connected between the two sources of N11 and N12 of the differential pairs. By the way, the substrate of N11 is connected to its source to avoid body-effect and increase the input common mode range.

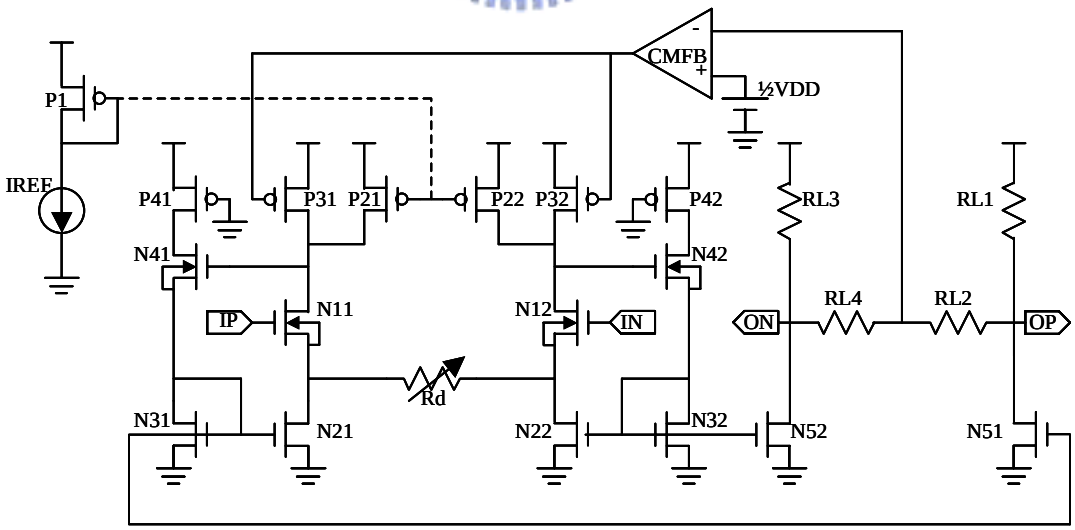


Fig.3.2 Gain-amplifier of the PGA circuit

The gain is accurately set by the ratio of the load resistor (RL1 // RL2) to the degeneration resistor ($Rd/2 + 1/gm_{11}$) of the input stage, and the gain is given by

$$Gain = N \cdot \frac{RL1 // RL2}{\frac{Rd}{2} + \frac{1}{gm_{11}}} \approx N \cdot \frac{RL1 // RL2}{\frac{Rd}{2}} \tag{3.3}$$

where N is the current mirror gain from N31 to N51.

A major advantage of this gain amplifier architecture is that the amplifier can be designed to produce both gain and attenuation by means of the ratio of load and degeneration resistors. For high-frequency applications, wide-band noise specifications limit the value of the degeneration and load resistors to the kOhm range. Practical values for the trans-conductance of the differential pair are limited to the mA/V range for modern CMOS processes. As the first consequence of the limited range for these resistors values, the degeneration gain will be relatively low, e.g., 1-10 times, resulting in a moderate gain accuracy and linearity of the voltage-to-current (VI) conversion.

The amplifier gain can be selected either by using a variable degeneration or load resistor. In order to realize an amplifier bandwidth independent of the programmable amplifier gain, the poles at the output nodes have to be kept constant. A variable degeneration resistor is therefore mostly preferred as programmable impedance in the gain amplifier. A variable degeneration resistor can be created using a resistor bank with CMOS switches to obtain selectable taps. A consequence of the limited range for the degeneration resistor's values relates to the practical implementation of these selector switches, which have nonlinear

on-resistances and will therefore have a non-negligible influence on the conversion impedance. This effect also results in a moderate gain accuracy and linearity, it should be taken into account in design phase.

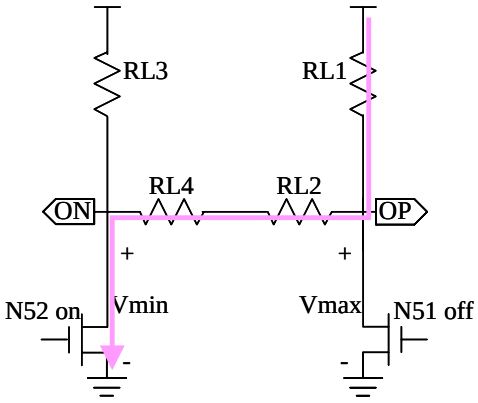


Fig.3.3 Representation of output voltage limit

The output stage of gain-amplifier is drawn in Fig.3.3; it shows the limit of the output swing. The maximum and minimum output voltage is happened when N52 is off and N51 is on.

$$\begin{aligned} Vo_{\min} &= V_{DS,sat} \\ &\approx 0 \end{aligned} \tag{3.4}$$

$$\begin{aligned} Vo_{\max} &= (V_{DD} - V_{DS,sat}) \cdot \frac{RL2 + RL4}{RL1 + RL2 + RL4} + V_{DS,sat} \\ &\approx \frac{RL2 + RL4}{RL1 + RL2 + RL4} \end{aligned} \tag{3.5}$$

Fig.3.4 to Fig.3.10 shows the simulation results. The AC response of the amplifier at room temperature is shown in Fig.3.4. The 3dB bandwidth of the gain-amplifier is up to 298MHz at 15dB gain. A large margin on bandwidth in our design would bring more confidence in the future using. The phase is linear and the group delay is less than 800ps.

Fig.3.5 and Fig.3.6 shows the 1dB-compression V1-dB,in=0.369V, V1-dB,out=0.674V. Fig3.7 and Fig 3.8 show the maximum input and output swing waveforms. Fig.3.9 and Fig.3.10 show IIP3=16.610dBm, OIP3=12.406dBm. Table 3.1 to Table 3.3 shows the temperature-shift and process-deviation effects.

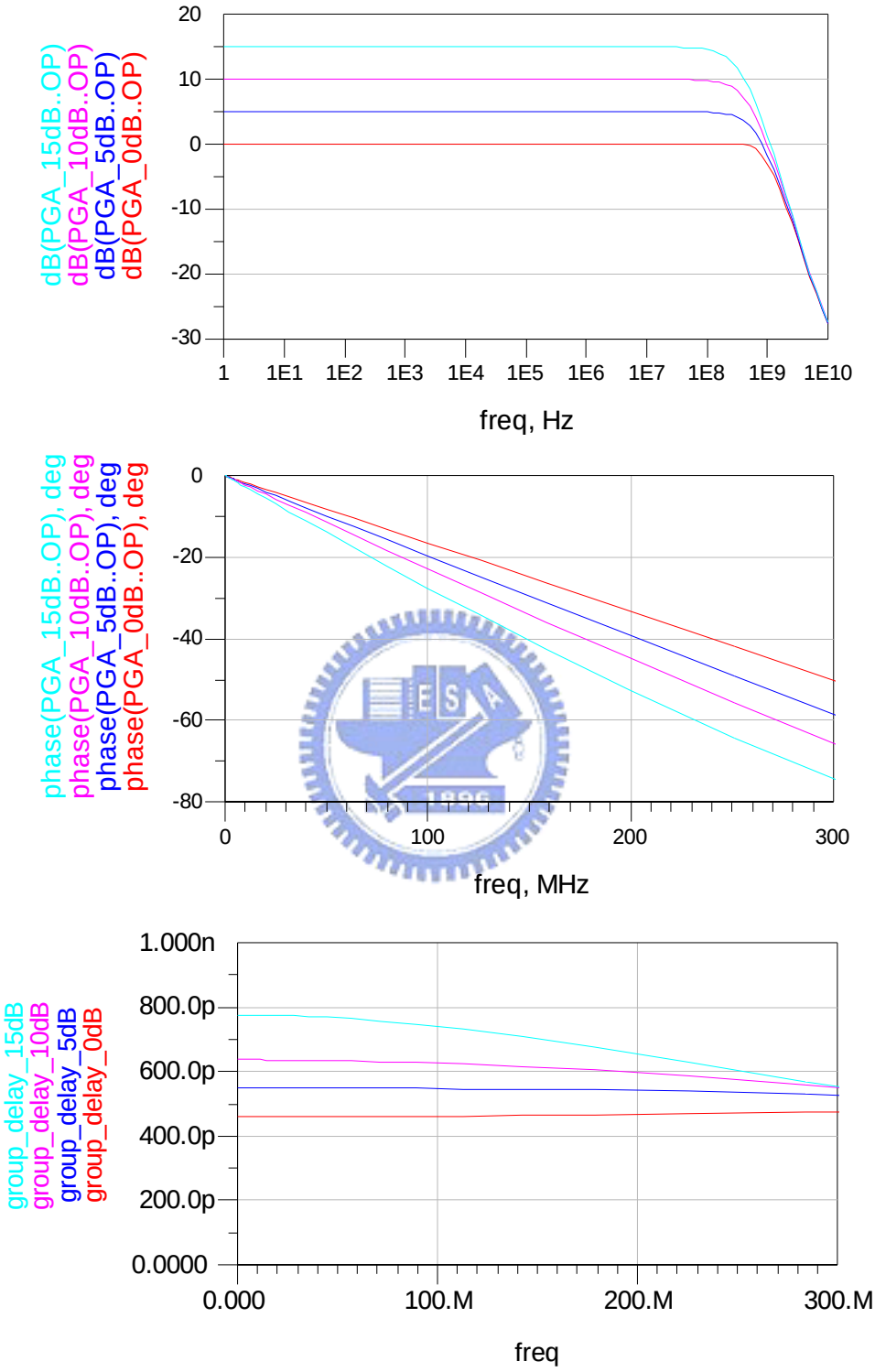
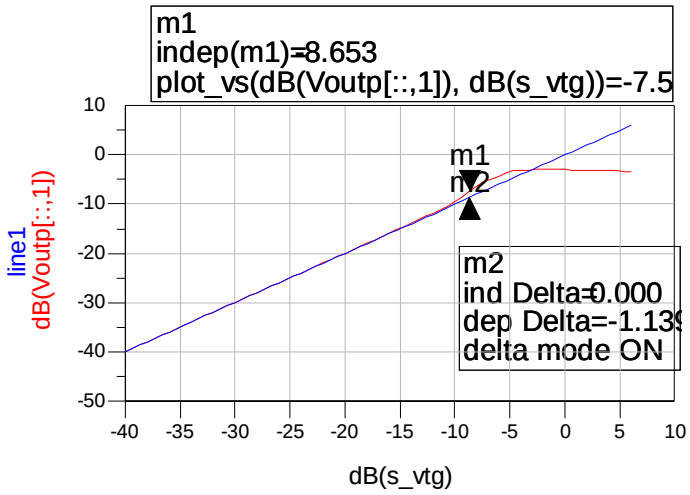


Fig.3.4 the gain, phase and group delay of gain-amplifier



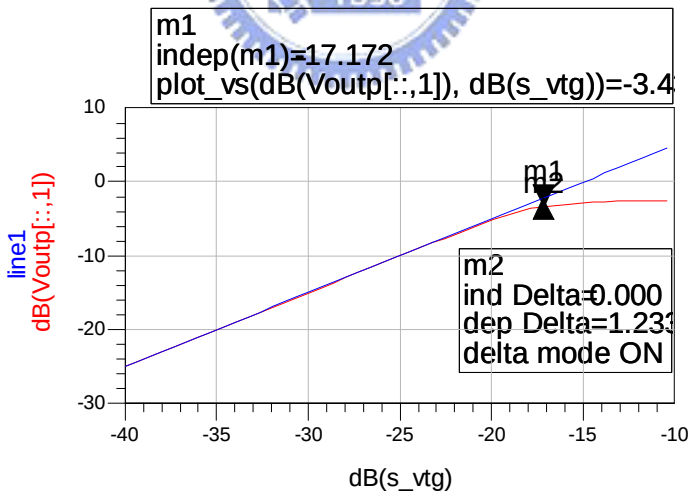
Eqn oV_1dB=10**(m1/20)

Eqn iV_1dB=10**(indep(m1)/20)

indep(oV_1dB)	oV_1dB	iV_1dB
-8.653	0.421	0.369

Fig.3.5 1-dB compression of gain-amplifier at 0dB gain

V1-dB,in = 0.369V



Eqn oV_1dB=10**(m1/20)

Eqn iV_1dB=10**(indep(m1)/20)

indep(oV_1dB)	oV_1dB	iV_1dB
-17.172	0.674	0.138

Fig.3.6 1-dB compression of gain-amplifier at 15dB gain

V1-dB,out = 0.674V

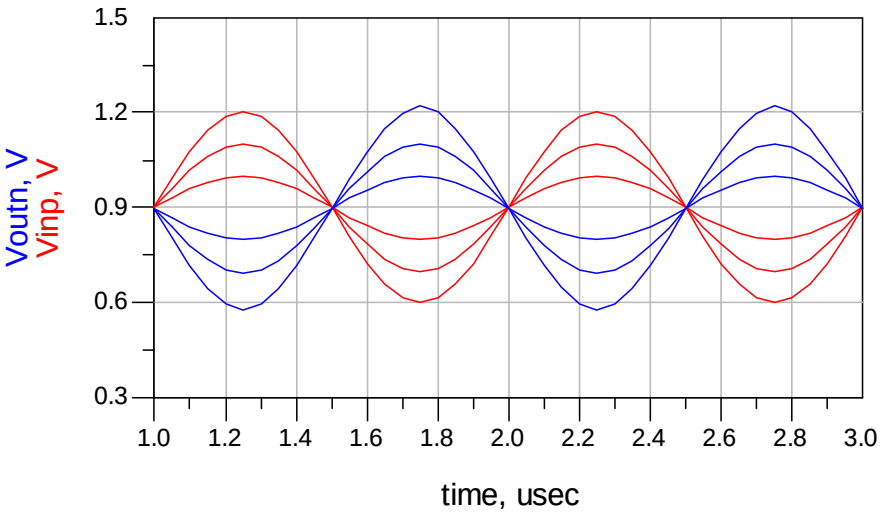


Fig.3.7 Transient of gain-amplifier at 0dB gain
Maximum input swing is 0.6V

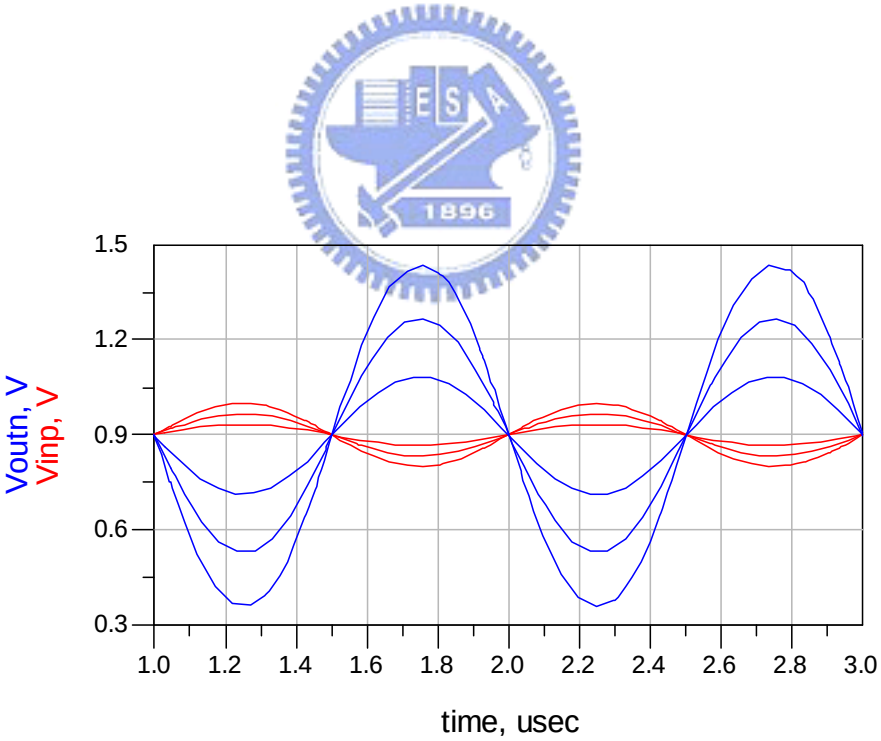


Fig.3.8 Transient of gain-amplifier at 15dB gain
Maximum output swing is 1.1V

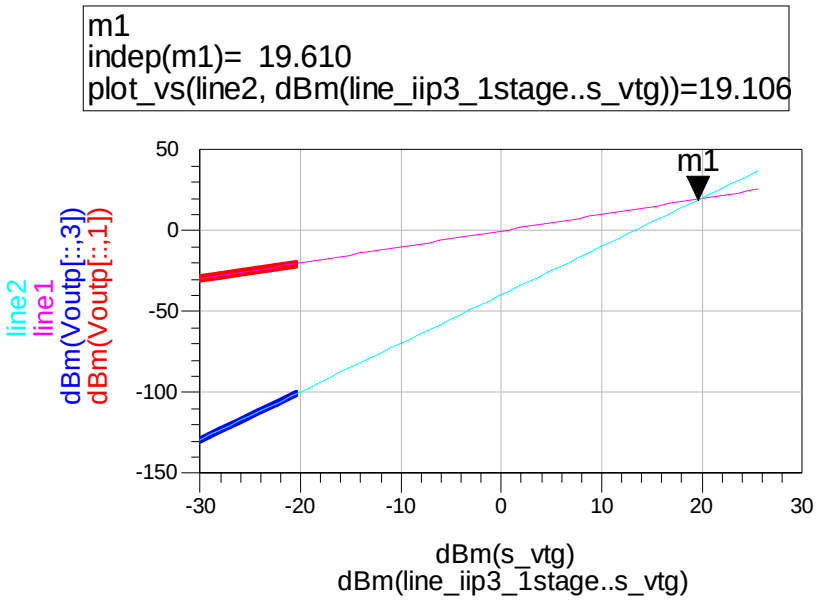


Fig.3.9 IIP3 of gain-amplifier at 0dB gain

IIP3 = 19.610 dBm

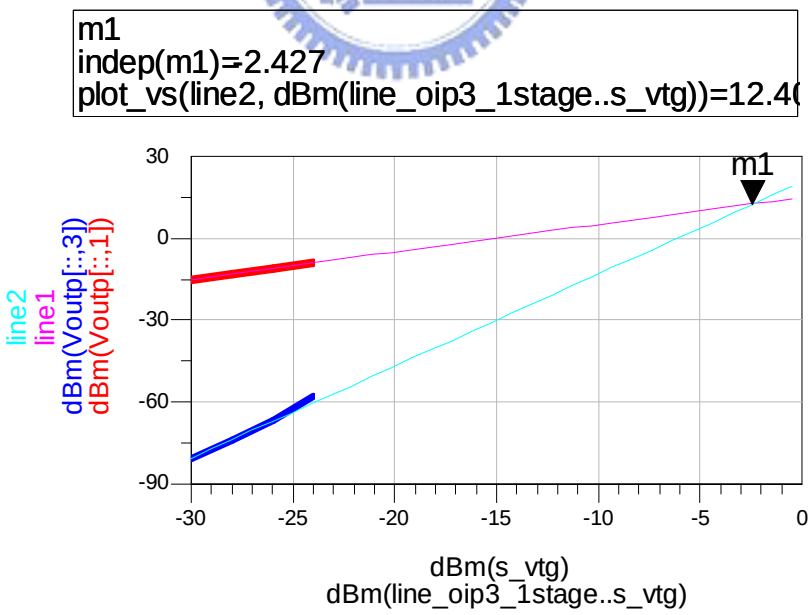


Fig.3.10 OIP3 of gain-amplifier at 15dB gain

OIP3 = 12.406 dBm

Table 3.1 Temperature effect

	0?C	25?C	70?C
Gain (0dB)	0.135dB	0dB	-0.221dB
Gain (15dB)	15.228dB	15dB	14.440dB
I_{DC}	225uA	259uA	263uA

Table 3.2 Resistor process deviation effect

	Rmax	Rtyp	Rmin
Gain (0dB)	-0.036dB	0dB	0.078dB
Gain (15dB)	15.432dB	15dB	14.307dB
I_{DC}	176uA	259uA	399uA

Table 3.3 MOS process deviation effect

	N:slow P:slow	N:slow P:fast	N:typ. P:typ.	N:fast P:slow	N:fast P:fast
Gain (0dB)	0.073dB	0.015dB	0dB	-0.024dB	-0.112dB
Gain (15dB)	14.797dB	14.888dB	15dB	15.059dB	15.037dB
I_{DC}	261uA	261uA	259uA	257uA	257uA

3.3 Programmable Degeneration-Resistor Design

According to the previous discussions, changing the degeneration resistor can change the gain ratio of the gain-amplifier. The trans-conductance of the source-coupled pair is varied by changing the resistance of the degeneration resistor Rd. When the input signal is weak, small Rd is used to obtain high gain and low noise. When the input signal is large, large Rd is used to obtain low gain and high linearity. Thus, this topology can achieve constant signal-to-noise-and-distortion ratio for the fixed output level regardless of the gain settings.

Fig.11 shows a digitally controlled degeneration resistor circuit. The programmable resistor Rd between the nodes RP and RN is given by

$$\begin{aligned} &Rd1 = R1 + R_{switch}, \quad where\ R1 = R1a + R1b \\ &Rd2 = R1 + R2 + R_{switch}, \quad where\ R2 = R2a + R2b \\ &\vdots \\ &Rd15 = R1 + R2 + \ldots + R15 + R_{switch}, \quad where\ R15 = R15a + R15b \\ &Rd16 = R1 + R2 + \cdots + R15 + R16 \end{aligned} \tag{3.6}$$

where the R_{switch} is the finite resistance of the MOS switch.

A large width MOS switch can be used to provide a smaller R_{switch}, however, the large capacitance of the switch will limit the bandwidth. To minimum the parasitical capacitor effect, a smaller size of switch is used and includes the turn-on resistor of the switch to a part of the degeneration resistor. The advantage of this circuit uses only a switch to program the gain-amplifier.

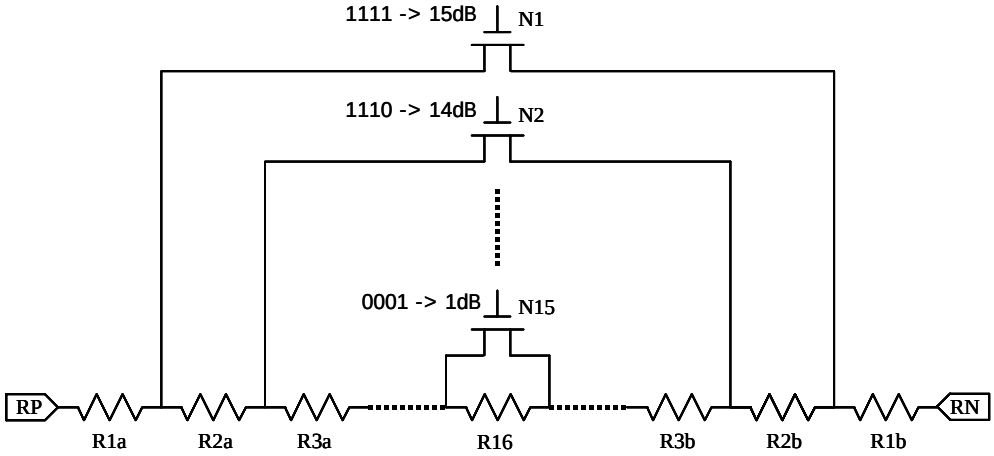


Fig.3.11 Programmable degeneration resistor

It is worth noting that using the degeneration resistance of the input stage for gain selection does not affect the operation of the common mode feedback, as it does not change the biasing of the circuit because the load resistor does not change. In addition, the second, third and fourth stages of the PGA could be directly coupled without coupling capacitor nor DC biasing circuit. It will save the needed current and bandwidth. Another method to change the gain is to change the current ratio to the output; however, this was found to dramatically degrade the bandwidth of the PGA due to the large capacitance from the array of the current mirrors.

Poly-resistance has been utilized for the degeneration resistor and load resistor; it has a less capacitance to the substrate than n^+ or p^+ resistors. Although the process of the poly-resistance has a large variation range, it will not affect the gain of gain-amplifier since the gain depends on the ratio of output-resistor to degeneration-resistor. Fig.3.12 shows the

relationship of the degeneration resistor changes exponentially with the gain setting. The high-gain (15dB) mode resistance of degeneration resistor Rd is 4Kohm, and the low-gain mode resistance is about 32Kohm.

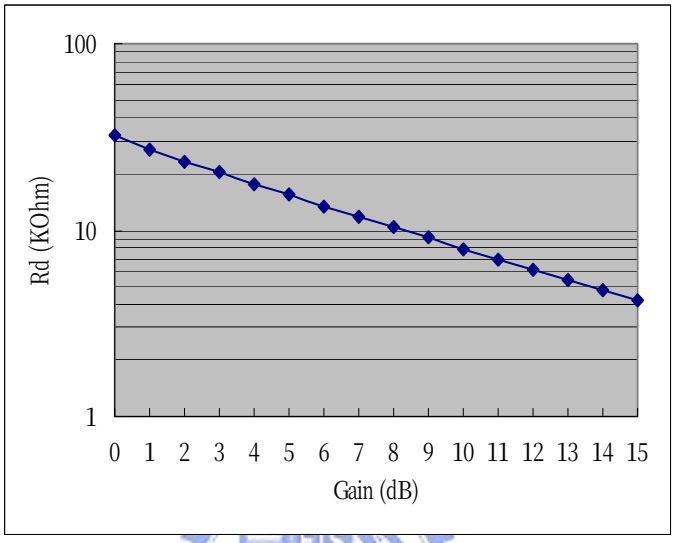


Fig.3.12 The degeneration resistor Rd value in different gain setting

3.4 Common-Mode Feedback Design

Common-mode feedback circuit that is frequency appeared at fully differential circuit is applied here to set the amplifier output common-mode voltage level. A common-mode feedback circuit set the voltage at which the output nodes of the fully differential amplifier biased themselves. For a high-gain differential amplifier, the output common-mode level is quite sensitive to device properties. When the process, temperature or input signal variation, the bias current may shift and affect the output DC level. A common-mode feedback network must be added to sense the common-mode level and adjust the bias current in the amplifier in addition to greater output swings.

In order to sense the output common-mode level, refer to Fig.3.2, the point where RL2 and RL4 are connected is used to sense the common-mode feedback voltage. This voltage is feedback through a differential operation amplifier and compared to the middle voltage 1/2 VDD to give maximum output swing. The output of the feedback operation amplifier is used to adjust the biasing current through the two transistors, P31 and P32.

The common-mode feedback is a two-stage amplifier, which has two amplifying stages and can have a voltage-mode output. The common-mood feedback using modified Miller compensation is shown in Fig.3.13. In Miller compensation, the compensation capacitor C_C makes one of the poles a low-frequency dominant pole. The other pole is moved to higher

frequencies. The ω_{GBW} can be further enhanced by adding a resistor R_Z in series with C_C. The poles and zeros in the modified Miller compensation can be approximated to be [7]

$$p_1 \approx -\frac{1}{g_{mN5} R_L R_{DS} C_C}, \quad p_2 \approx -\frac{g_{mN5}}{C_L}, \quad p_3 \approx -\frac{1}{R_Z C_P}, \quad z \approx \frac{1}{C_C\left(\frac{1}{g_{mN5}} - R_Z\right)} \qquad (3.7)$$

where g_{mP3}, g_{mN5}, R_L, and R_{DS} are the g_m of transistors *P3* and *N5*, load resistance at the output, and the resistance at the output of the first stage, respectively. C_L and C_P are the output capacitance and the capacitance at the output of the first stage, respectively. With R_Z, the zero can be moved to the left-half-plan and placed on top of the second pole. Therefore, only p_1 and p_3 remain and ω_{GBW} becomes g_{mP3}/C_C. Since both stages contribute to DC gain, the DC gain can be 60dB or higher, even with resistor loads at the output.

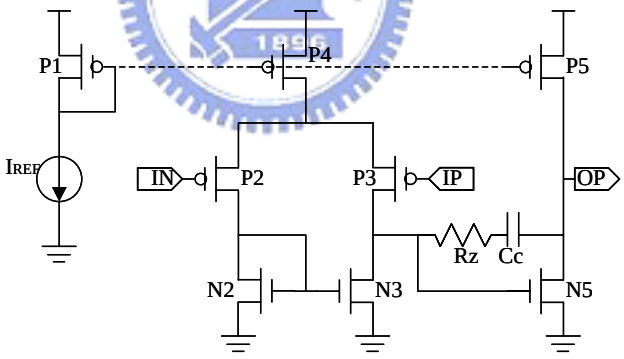


Fig.3.13 The amplifier of common-mode feedback with modified Miller compensation

It can be shown that a 60deg phase margin suggesting a negligible frequency peaking for a stable feedback system. This typically means that the step response of the feedback system exhibits little ringing, providing a fast settling. For greater phase margins, the system is more stable but the time response slows down. The close-loop of the common-mode feedback form a negative-feedback structure, larger phase margin is necessary to avoid

oscillate issue. From the simulation result in Fig.3.15, the feedback operation amplifier has 73dB gain and 66deg phase margin.

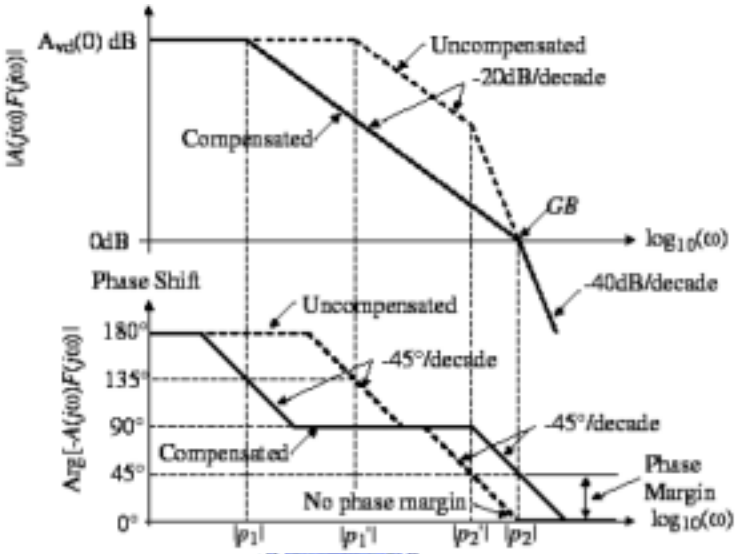


Fig.3.14 Bode plots of close-loop gain-amplifier

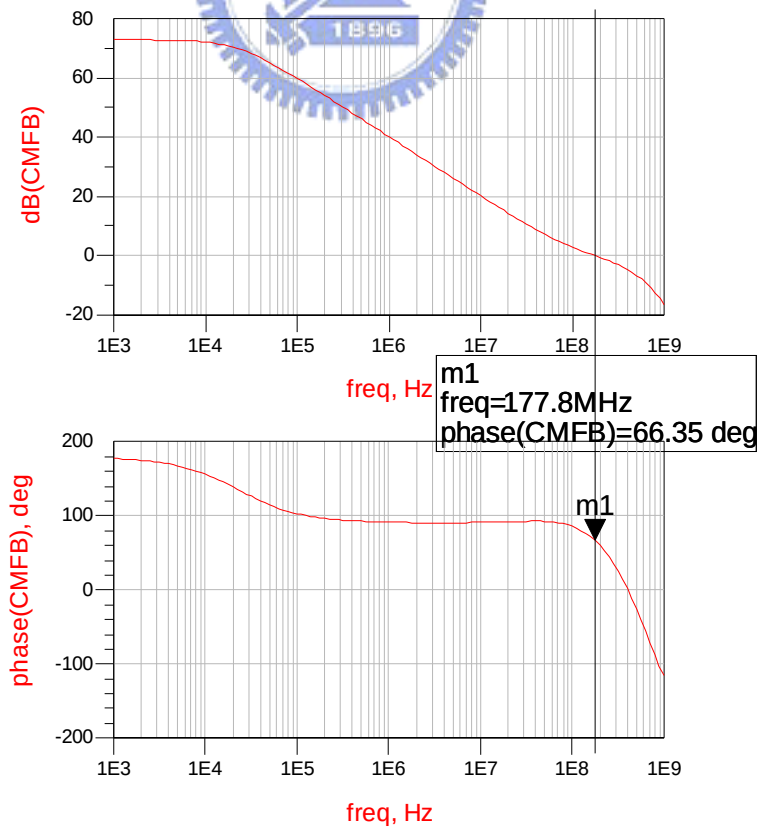


Fig.3.15 Simulation result of the bode plots of close-loop gain-amplifier

Since the absolute value of interlayer capacitances is poorly controlled in process, the capacitor Cc of Fig3.13. may experience process variations as high as 20%. By contrast, the gate oxide capacitance is typically controlled with less than 5% error. Also the gate oxide capacitance has a small layout area, the simplest capacitor structure in CMOS technology is implemented by a MOSFET to save substantial area.

3.5 High-Pass Filter and DC-Offset-Cancellation Design

The PGA is designed as a four-stage cascaded gain-amplifier to achieve large dynamic range and large bandwidth. Each stage has 0 to 15dB gain range. Since the PGA is a high gain device, even a slight DC offset may smear small input signal coming from RF front-end. The PGA incorporates a DC-offset-cancellation circuit, also called auto-zero circuit, used to cancel the inherent offset voltage in the signal path.

DC offset is a series problem in gain amplifier circuit; offset suppression is necessary otherwise it will degrade the receiver dynamic range. AC coupling of each stage is the easier way to remove the offset. However this approach requires large capacitor values that are not realizable on-chip.

The other method is detected and removed by digital time-averaging or by using more complex digital algorithm. This sort of digital cancellation requires the analog base-band circuits to have enough spurious-free dynamic range to overcome the DC offset [8]. The third approach is using circuit technique to depress the low frequency offset, either by feedback or fed forward methods. In this paper, a programmable gain amplifier with this approach is presented.

The DC feedback loop shown in Fig.16 with one off-chip capacitor and four on-chip

resistors. The circuit provides an offset correction function that effectively reduces the offset voltage to negligible levels. Input offset is partially removed by the offset correction function. An external capacitor C3 is required to compensate the DC offset correction loop determining the lower 3dB point and also block AC feedback loop. The suggested value of the correction capacitor C3 should be 1uF for optimized performance.

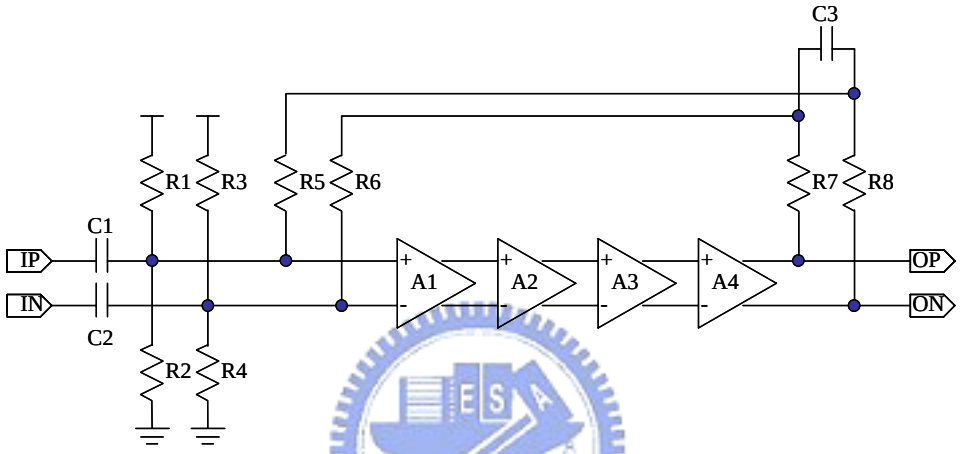


Fig.3.16 PGA circuit with DC-offset-cancellation

If the input-referred DC offset voltage is not zero, the four-stage cascade gain-amplifier will amplify the difference and the output is practically non-zero. Because of the negative-feedback loop of DC-offset-cancellation circuit, it will compensate the input DC offsets of the circuit approaches zero. The PGA is based on this topology and has an excellent performance. From the simulation results, if is regardless of the DC offsets and the process mismatches in the signal path of the PGA.

It is worth noting that using the DC-offset-cancellation structure will affect the loading of fourth-stage gain-amplifier. The output loading changes form (RL1//RL2) to

(RL1//RL2//R7), and it will affect the gain of the fourth-stage gain-amplifier. Set ($RL2_{4th}$//R7) of the fourth-stage equal to RL2 of other stage is a good choice, and the gain ranges of the four stages will the same.

The PGA input must be AC coupled to block DC signal and allow proper operation of the offset correction function. Two external AC-couple capacitors for input signal are necessary. The AC coupled input is possible to use a high-pass filter with a reasonable corner frequency to filter out DC offsets. At the maximum channel gain the –3dB frequency of the high-pass filter is less than 1KHz. The corner frequency moves to lower frequencies when the channel gain is decreased.

The lower –3dB point of the circuit is determined by the input coupling capacitors C1 and C2, and the capacitors should be large enough to not affect the signal quality. Refer to the Fig.3.16, C1 and R1,R2,R5 construct a high-pass filter. The lower –3dB frequency is

$$f_{L3dB} = \frac{1}{2\pi(R_1 // R_2 // R_5)\cdot C_1} \tag{3.8}$$

Fig.3.17 to Fig.3.23 shows the simulation results. The AC response of the amplifier at room temperature is shown in Fig.3.17, and the peak response of low frequency is cause of the DC-offset-cancellation circuit. When the operation frequency is low enough, the C3 in Fig.3.16 is not short and the output AC signal will feedback to input terminal to effect the loop gain. The 3dB bandwidth of the PGA is up to 125MHz at 60dB gain. The phase is linear and a fairly flat group delay of 4ns. Fig.3.18 and Fig.3.19 show the 1dB-compression

V1-dB,in=0.252V, V1-dB,out=0.531V. Fig.3.20 shows the 1dB-compression at 3dB gain setting is 0.331V, this value is approach to the target specification 0.35V. Fig3.21 and Fig 3.22 show IIP3=22.858dBm, OIP3=61.490dBm. Fig.3.23 shows the PGA gain curve without DC-offset-cancellation feature when R3 has 1% mismatch, the output AC curve is not an amplifier performance and cannot operation properly. Fig.3.24 shows the gain curve of DC-offset-cancellation PGA when R3 has even 50% mismatch, the AC output performs a good performance. Fig.3.25 and Fig.3.26 show the gain curve when remove the high-pass filter in Fig.3.16 with 1mV and 2mV input DC-offset respectively. When the high-pass filter is removed, he input DC level is forced by the input signal and cannot be fixed by DC-offset-cancellation feature. Fig.3.26 shows that when input DC offset is larger than 1mV, the PGA cannot work properly. Fig.3.27 shows the settling time performance of PGA when gain setting is changed, and the output signal is stable in a short time. A short settling time in a wireless receiver system is very important. Table 3.4 shows the output noise spectral density is about 6.553nV/squtHz at 10MHz.

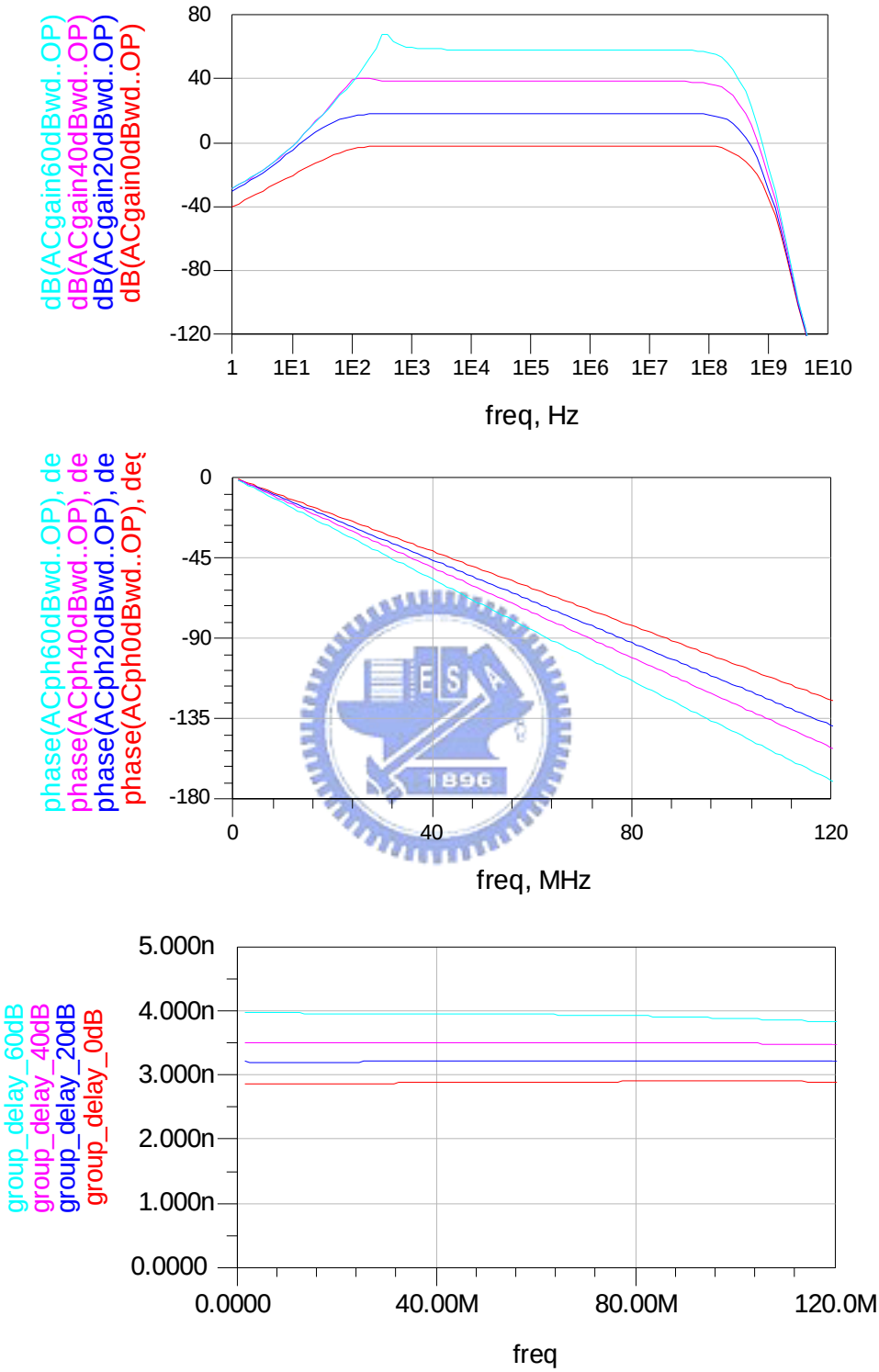
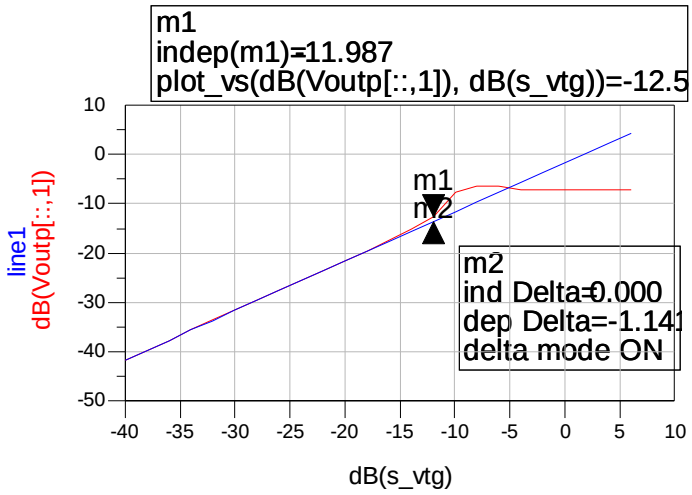


Fig.3.17 The gain, phase and group delay of PGA



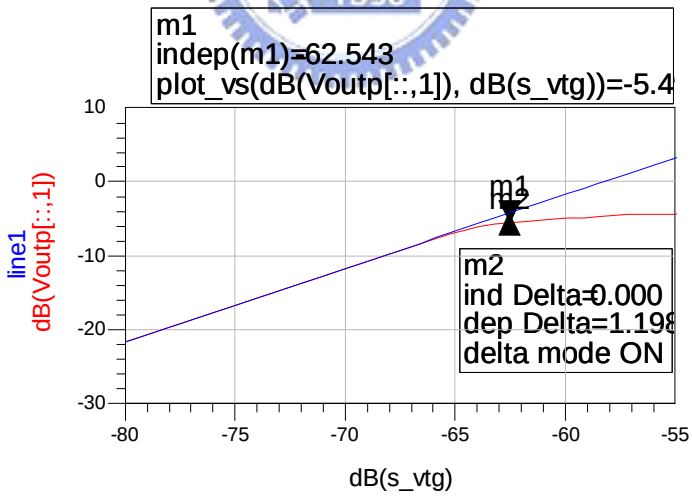
Eqn oV_1dB=10**(m1/20)

Eqn iV_1dB=10**(indep(m1)/20)

indep(oV_1dB)	oV_1dB	iV_1dB
-11.987	0.236	0.252

Fig.3.18 1-dB compression of PGA at 0dB gain

V1-dB,in = 0.252V



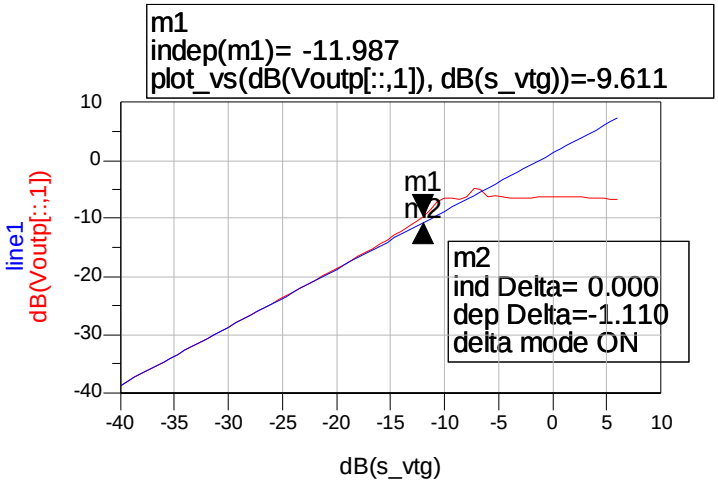
Eqn oV_1dB=10**(m1/20)

Eqn iV_1dB=10**(indep(m1)/20)

indep(oV_1dB)	oV_1dB	iV_1dB
-62.543	0.531	7.462E-4

Fig.3.19 1-dB compression of PGA at 60dB gain

V1-dB,out = 0.531V



Eqn oV_1dB=10**(m1/20)

Eqn iV_1dB=10**(indep(m1)/20)

indep(oV_1dB)	oV_1dB	iV_1dB
-11.987	0.331	0.252

Fig.20 1-dB compression of PGA at 3dB gain

V1-dB,in = 0.331V

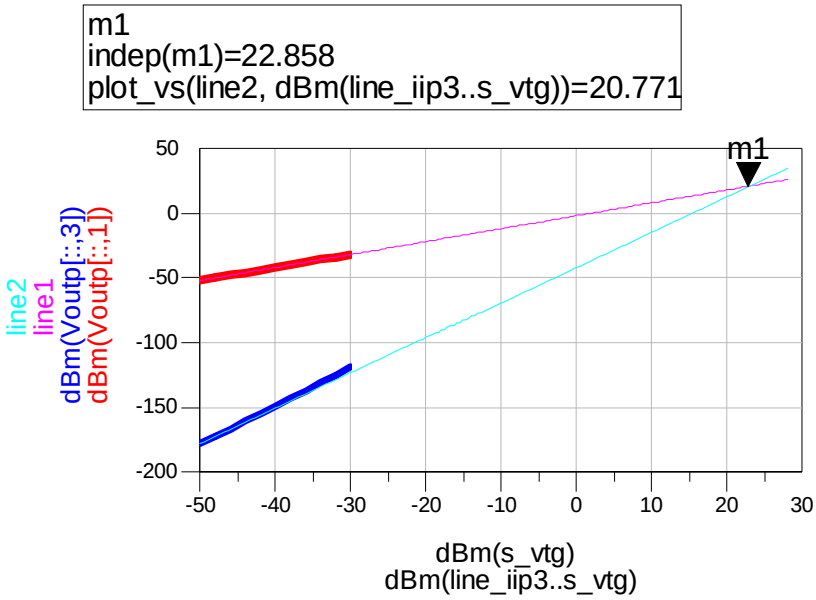


Fig.3.21 IIP3 of PGA at 0dB gain

IIP3 = 22.858 dBm

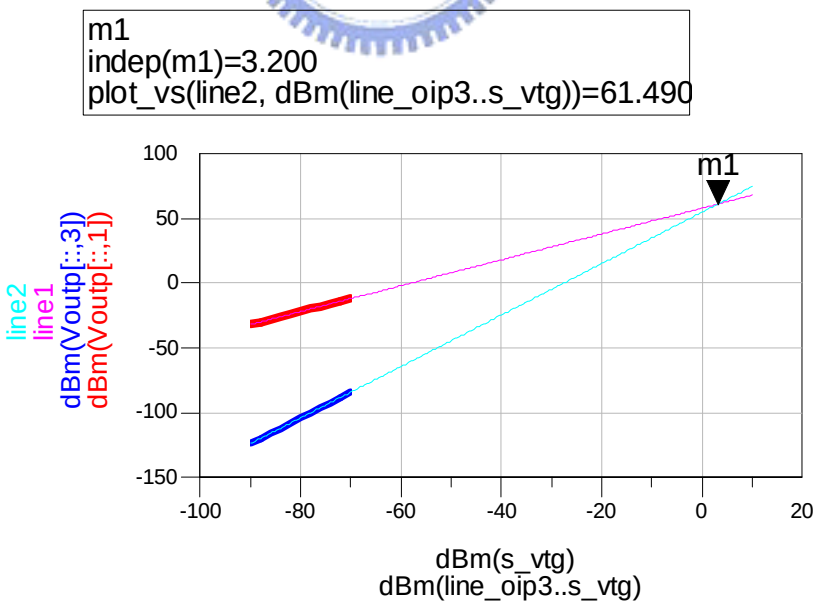


Fig.3.22 OIP3 of PGA at 60dB gain

OIP3 = 61.490 dBm

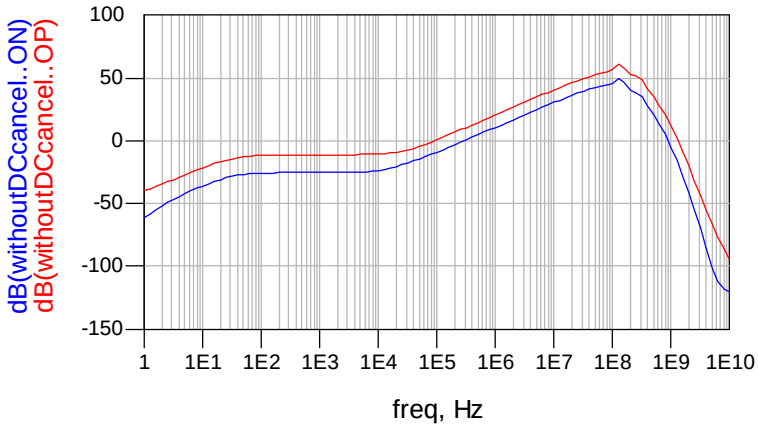


Fig.3.23 Gain curve of non-DC-offset-cancellation PGA when R3 has 1% mismatch

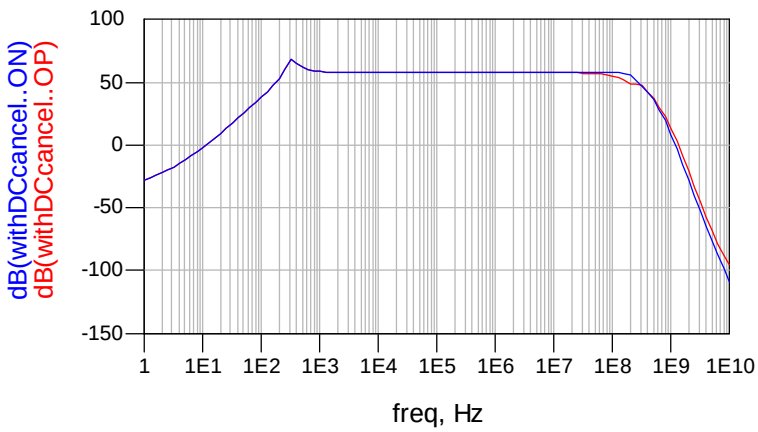


Fig.3.24 gain curve of DC-offset-cancellation PGA when R3 has 50% mismatch

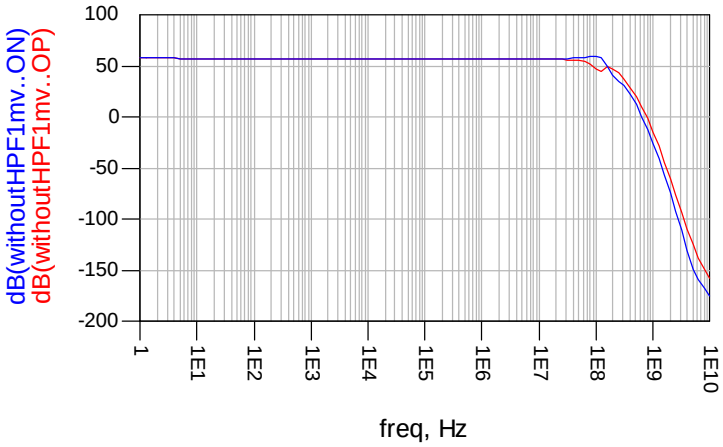


Fig.3.25 gain curve of DC-offset-cancellation PGA when remove HPF with 1mV DC offset

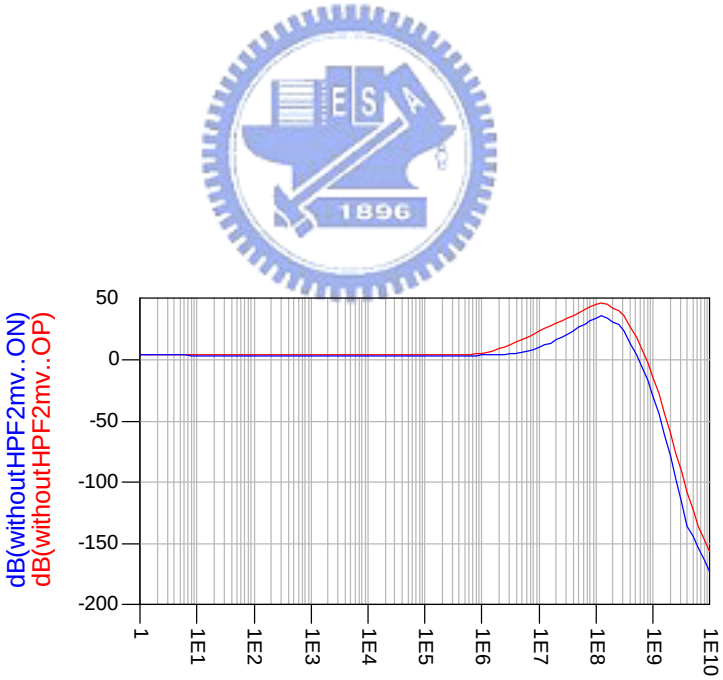


Fig.3.26 gain curve of DC-offset-cancellation PGA when remove HPF with 2mV DC offset

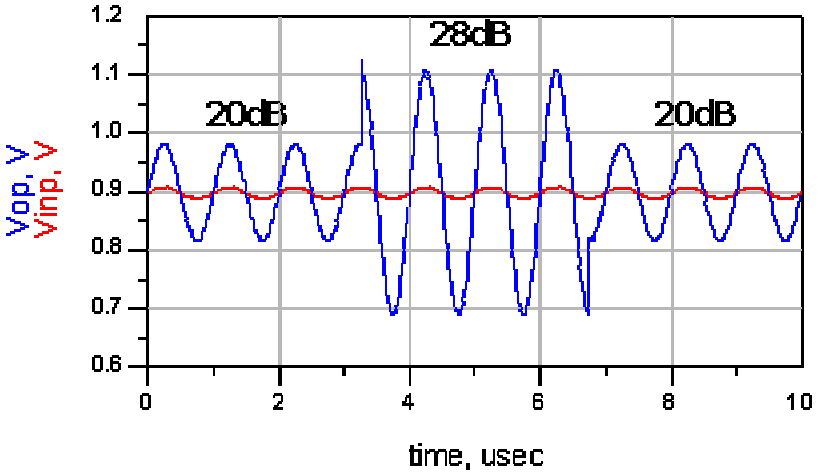


Fig.3.27 PGA settling time performance

Table.3.4 Noise voltage of the PGA in different gain setting

Gain	0dB	20dB	40dB	60dB
Vn,in (nV/sqrtHz)	64.22	20.65	10.72	6.553

3.6 Digital Control Design

The PGA is constructed of 4-stage gain-amplifier, each stage provide 0 to 15dB gain. How to partition each stage gain is a problem. Form the following formula

$$NF_{Total} = NF_1 + \frac{NF_2 - 1}{A_1} + \frac{NF_3 - 1}{A_1 \cdot A_2} + \frac{NF_4 - 1}{A_1 \cdot A_2 \cdot A_3} \tag{3.9}$$

where NF_I and A_I are the noise figure and the gain of stage I, respectively.

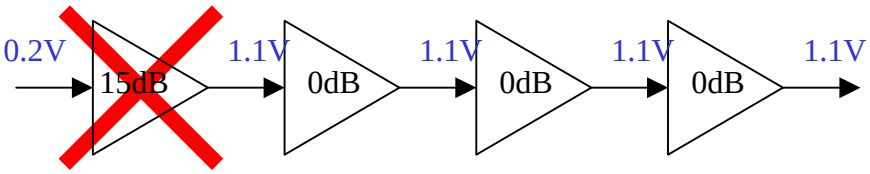


Fig.3.28 Ideal gain stage partition but not workable

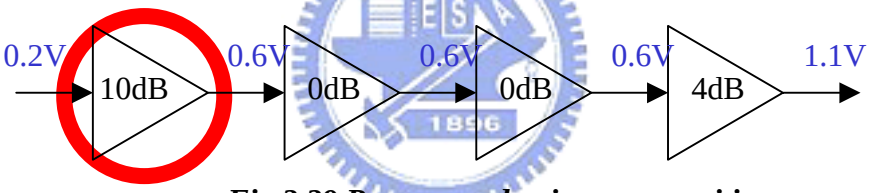


Fig.3.29 Recommend gain stage partition

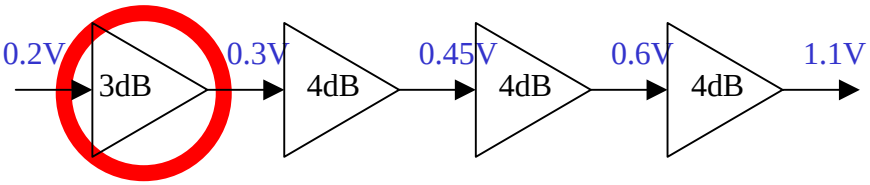


Fig.3.30 Another recommends gain stage partition

It is clear from this equation that a large gain in the first stage will reduce the noise figure of the whole PGA. The maximum output amplitude of our gain amplifier is 1.1V, but the maximum input amplitude is only 0.6V. If a 15dB gain is required with a 0.2V signal input and we set first stage to 15dB, as shown in Fig.3.28, the output amplitude of first stage

is 1.1V and the second stage cannot operate normally since it excess maximum input amplitude 0.6V. The best policy is shown in Fig.3.29, set first stage to 10dB gain and the output amplitude is 0.6V and set 4^{th} stage to 5dB. Fig.3.30 is another method to partition each stage gain, it averagely separate the required gain. By the way, from the simulation results, the 1-dB compression is better when partition more gain to rear stage.

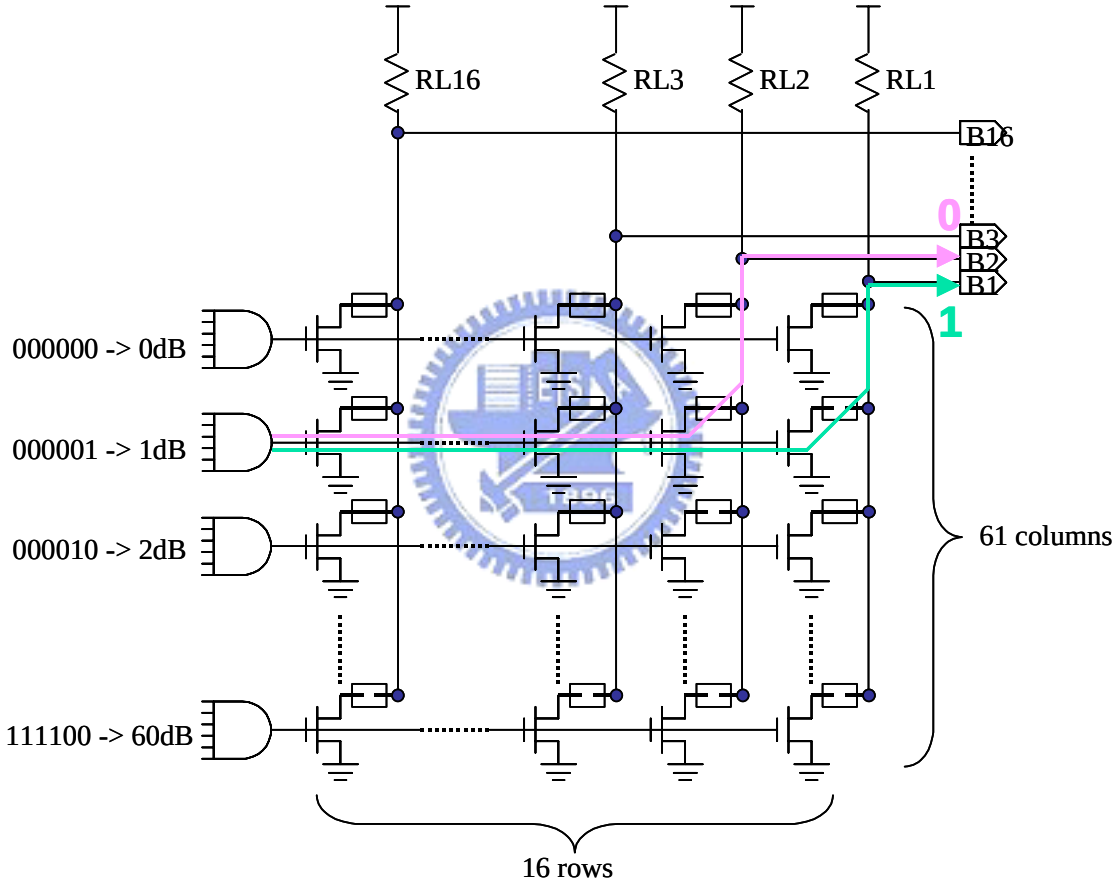


Fig.3.31 The 6-bits to 16-bits decoder circuit

Each stage has four programmable bits; four stages have 16 bits. Programmable logic array (PLA) structure provides a high-integrated decoder. The PLA shows in Fig.3.31 is a 6-bits to 16-bits decoder; 6-bits input AND-gate select which column is available, and the

jumper decide the output level. If jumper is short, NMOS short to ground and output is low; if jumper is open, resistor pull-up to VDD and output is high. To have 0dB to 60dB gain range, 61 columns AND-gate and NMOS is needed; and to have 16 bits output, 16 NMOS is required. There are 61 X 16 = 976 NMOS, use layout technique can shrink the chip size effective. Also choose long-channel PMOS transistor as a resistor to replace RL1~RL16 can also reduce the layout size.

Fig.3.32 is 6-bits AND-gate circuit. Using minimum W/L size and minimum layout rule can reduce its layout size since there is no frequency concern.

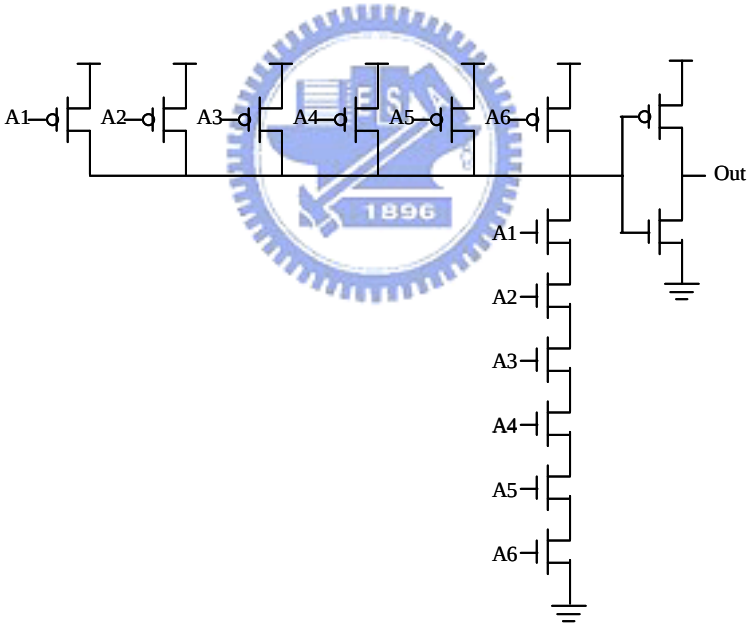


Fig.3.32 6-bits input AND gate

Table 3.5 shows the 6-bits digital controlled gain setting table. The gain setting increasing is according to the increasing binary input bits B[5:0].

Table 3.5 6-bits digital controlled gain setting table

B[5:0]	Gain	B[5:0]	Gain	B[5:0]	Gain	B[5:0]	Gain
000000	0 dB	010000	16 dB	100000	32 dB	110000	48 dB
000001	1 dB	010001	17 dB	100001	33 dB	110001	49 dB
000010	2 dB	010010	18 dB	100010	34 dB	110010	50 dB
000011	3 dB	010011	19 dB	100011	35 dB	110011	51 dB
000100	4 dB	010100	20 dB	100100	36 dB	110100	52 dB
000101	5 dB	010101	21 dB	100101	37 dB	110101	53 dB
000110	6 dB	010110	22 dB	100110	38 dB	110110	54 dB
000111	7 dB	010111	23 dB	100111	39 dB	110111	55 dB
001000	8 dB	011000	24 dB	101000	40 dB	111000	56 dB
001001	9 dB	011001	25 dB	101001	41 dB	111001	57 dB
001010	10 dB	011010	26 dB	101010	42 dB	111010	58 dB
001011	11 dB	011011	27 dB	101011	43 dB	111011	59 dB
001100	12 dB	011100	28 dB	101100	44 dB	111100	60 dB
001101	13 dB	011101	29 dB	101101	45 dB	111101	
001110	14 dB	011110	30 dB	101110	46 dB	111110	
001111	15 dB	011111	31 dB	101111	47 dB	111111	

3.7 Output Buffer Design

The operational amplifier, which has become one of the most versatile and important building blocks in analog-circuit design. It provides high output resistance and low output resistance. More over, it enables the output to be tested off-chip with low impedance loading thus reducing the number of off-chip components, which is a nice feature for system design.

The buffer stage with low output impedance is required at PGA output. The NMOS source couple pair with unit gain feedback is used, as shown in Fig.3.33. The output buffer is designed in 3.3V supply voltage rule to provide a larger driving capacity.

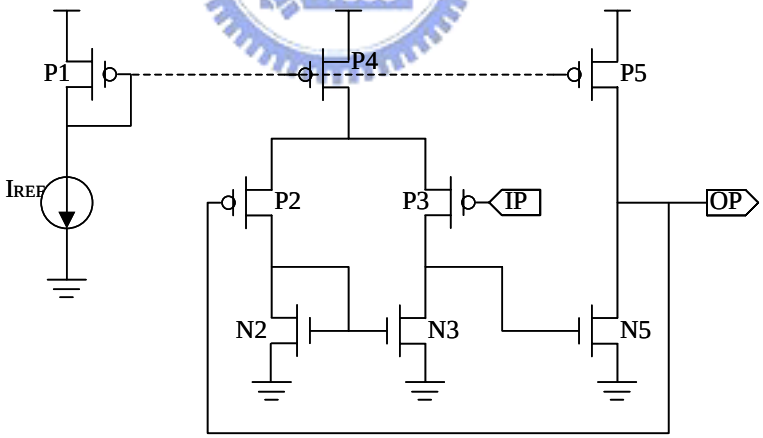


Fig.3.33 The PGA output buffer circuit

3.8 Advantages of the Proposed PGA

This thesis proposed the PGA circuit that can adjust the gain by the degeneration resistors. It can reduce the output resistors layout size, reduce switching transistors and increase operation bandwidth. Also the bias current is fixed to simplify the circuit operation.

As the circuit is operating in only 1.8V supply voltage, remove the output switching transistors can also increase the output amplitude. By the way, construct N11 and N12 on substrate will induce body-effect and increase the threshold voltage. To get a larger input range, construct N11 and N12 shown in Fig.3.2 on triple-well can avoid body-effect and reduce threshold voltage Vt about 0.2 to 0.3V.

The common-mode feedback feature set the output DC voltage fix on 1/2 VDD. The four-stage of the gain-amplifier could be directly coupled without coupling capacitor nor DC biasing circuit, saving needed current and bandwidth.

Finally, the high-pass filter can cancel the DC element that comes form direct-conversion mixer, and the DC-offset-cancellation can cancel the DC offset that causes by process mismatch.

Chapter 4
Implementation

The analog CMOS circuits has evolved from low-speed, low-complexity, small-signal, high-voltage topologies to high-speed, high-complexity, low-voltage “mixed-signal” systems containing a great deal of digital circuitry. While device scaling has enhanced the raw speed of transistors, unwanted interaction between different sections of integrated circuits as well as non-idealities in the layout and packaging increasingly limit both the speed and the precision of such systems. Today’s analog circuit design is very heavily influenced by layout and packaging.

This chapter describes the implementation of the programmable gain amplifier. This chapter is organized as follow. Section 4.1 contains the chip layout of PGA. Section 4.2 analyzes ESD protection architecture. Section 4.3 describes the package model. The last , the PCB layout is given in Section 4.4.

4.1 Integrated Circuit Layout

The layout of an integrated circuit defines the geometries that appear on the masks used in fabrication. The geometries include n-well, gate oxide, ploysilicon, source/drain areas, n^- and p^+ implants, interlayer contact windows, and metal layers.

For the analog or RF circuit design, even with the same schematic design, different layouts will make entirely difference performance of the circuit. Therefore, the design of the layout is an important topic, especially for high frequency design. The most important things of the layout are parasitic and mismatches. For parasitic, the metal line will cause the parasitic capacitor and resistor thus decrease the bandwidth and gain loss of the circuit.

Improper layout could result in large difference of performance between simulated and measurement result, or even result in non-working circuits. The layout is following the rule that no signal returns close to its origin in order to avoid coupling back to the input. The matching and symmetry should be arranged very carefully for the differential circuit. The common-centroid layout is employed to alleviate device mismatch due to process variation.

The supply power is drawn in form of power ring within the pads. The die of packaged version is to fit the standard form of the QFN-20 pin package. The pads of packaged version are ESD protected which will be introduced in the later sections. Finally, all the line widths are drawn according to following criterions, minimizing parasitic capacitance and series

resistance. The DC current paths should be wide enough to prevent electro-migration. The line length of signal path should be kept as short as possible.

The PGA circuit layout is shown in Fig.4.1, where 4-stage gain-amplifier, DC-offset-cancellation, 6-bits to 16-bits decoder and output driver circuit can be found. Also the detail layout circuit is shown in Fig.4.2 to Fig.4.4. The main considerations regarding layout design are to minimize the local metal routing length to reduce the parasitic capacitance. Each metals width of VDD and GND has been calculated to support enough current flow; large metal width is not necessary and will cause the waste of chip area.

To optimum the operation performance, a good placement of floor plan is very important. It can reduce the trace interleave issue and routing distance. Refer to Fig.4.2, the input port and the output port of 1-stage gain-amplifier are at the same vertical axis. It will be very easy to connect to Gain-Amplifier without any other routing trace.

Fig.4.5 is the chip layout of the PGA circuit. It also defines the pin-out assignment. Table 4.1 shows the pin description of the PGA package.

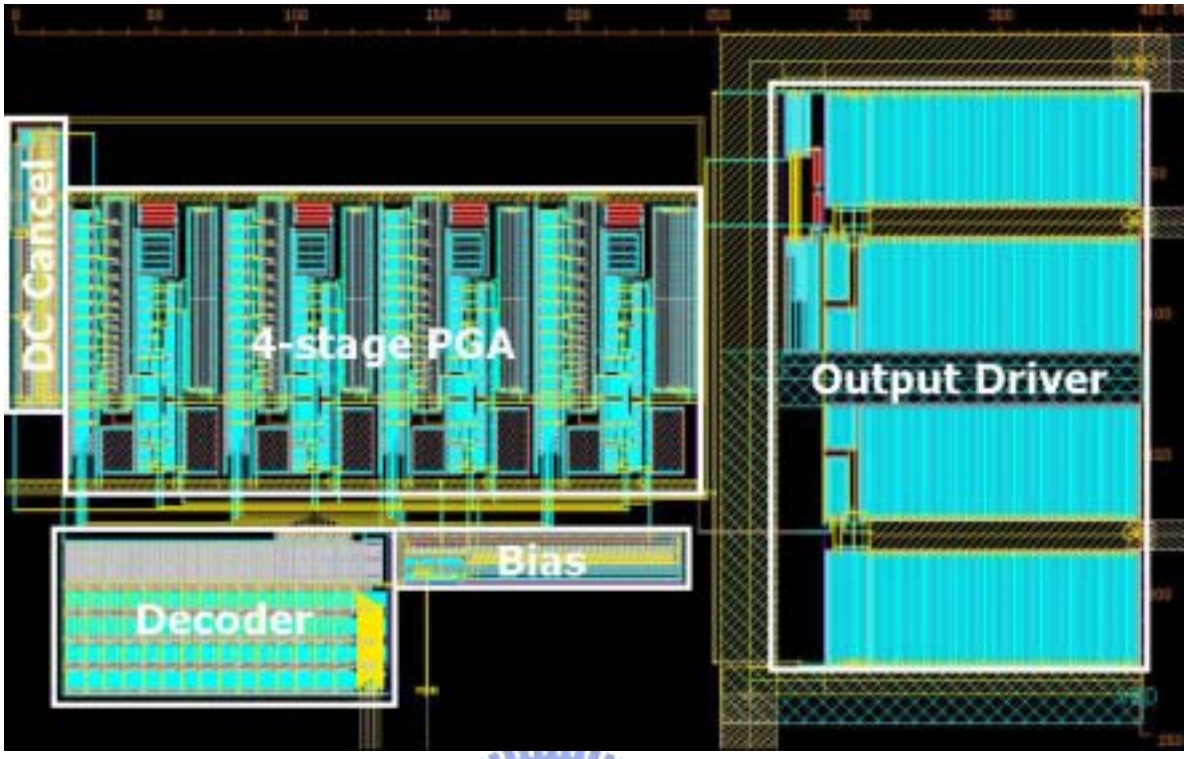


Fig.4.1 Programmable-Gain-Amplifier Fully Layout

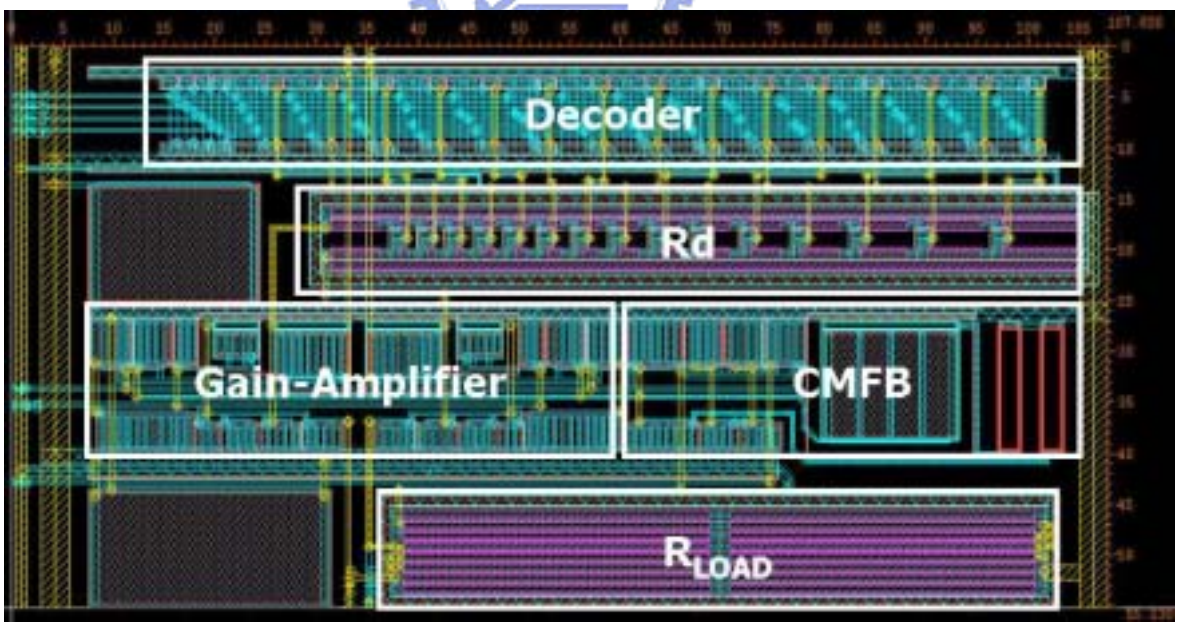


Fig.4.2 single-stage Gain-Amplifier Layout

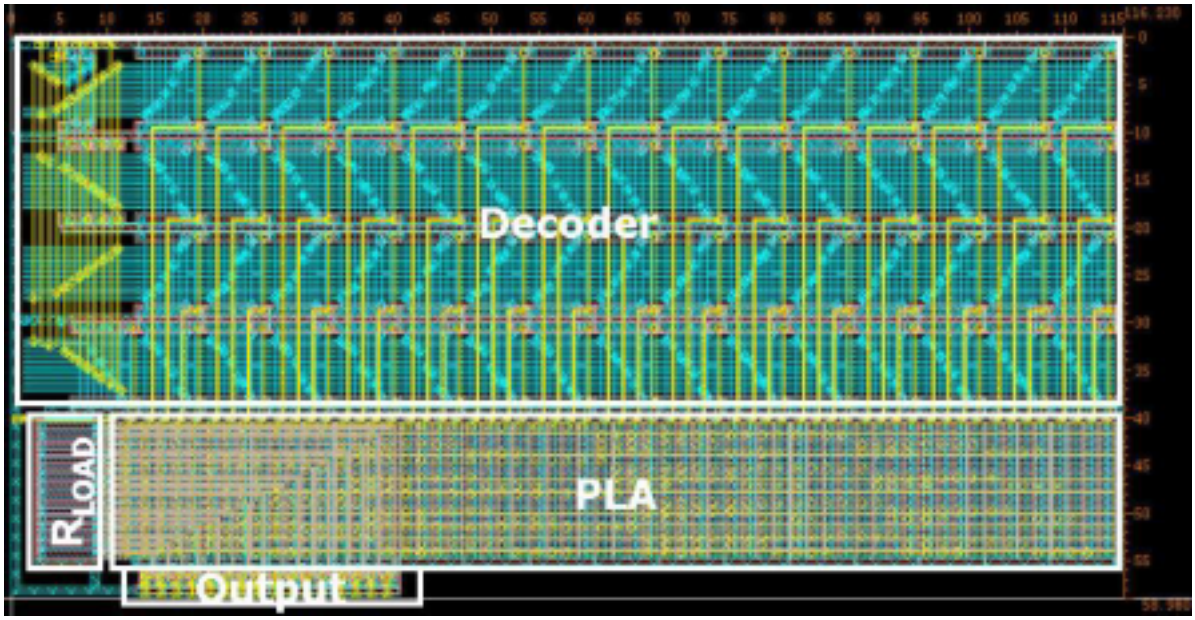


Fig.4.3 6-bits to 16-bits Decoder Layout

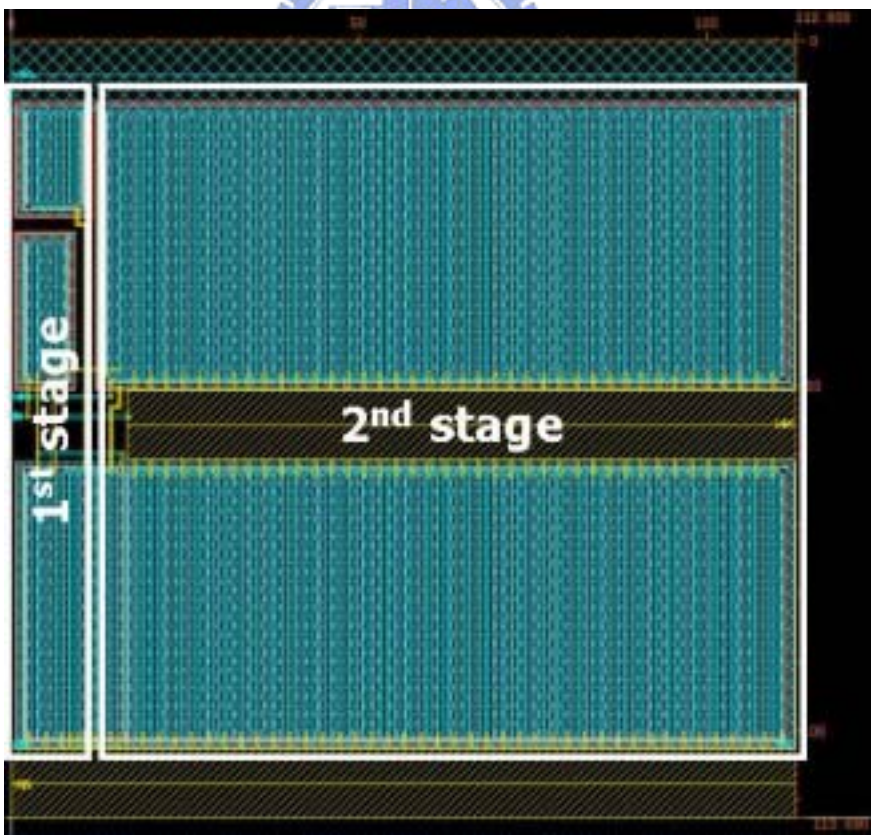


Fig.4.4 Output Driver Layout

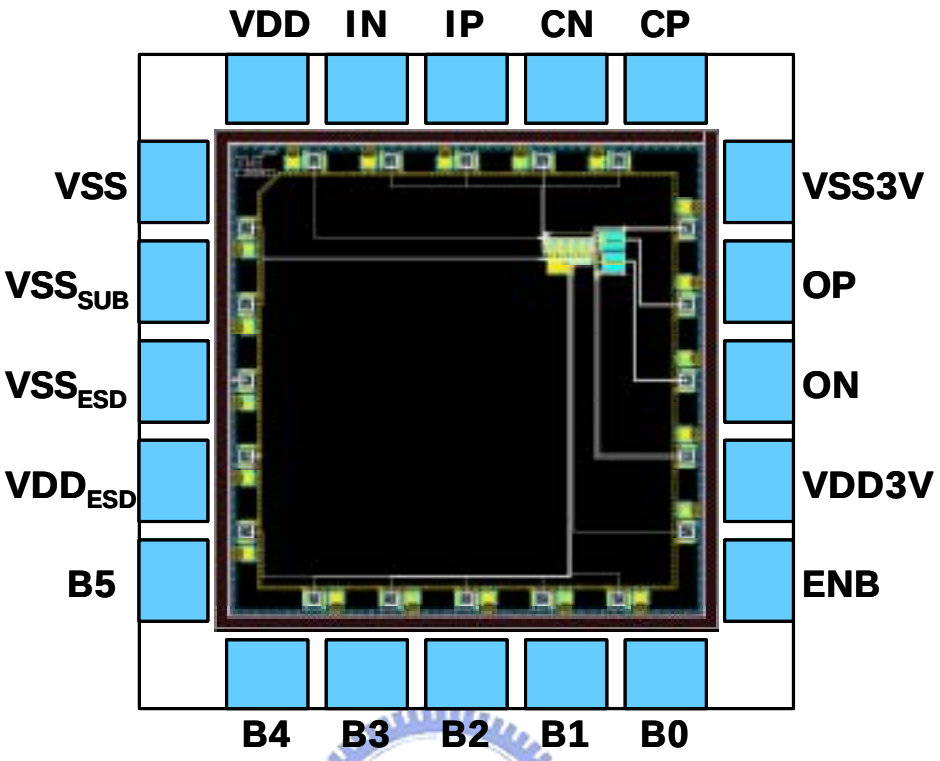


Fig.4.5 Fully Chip Layout and Pin Assignment Define

Table 4.1 Pin description of the PGA package

Pin Name	Description
VDD	Core chip power pin. Connect to 1.8V supply voltage.
VDD3V	Output section power pin. Connect to 3.3V supply voltage.
VDDESD	ESD protection power pin. Connect to 1.8V supply voltage.
VSS	Core chip ground pin. Connect to most negative supply voltage.
VSS3V	Output section ground pin. Connect to most negative supply voltage.
VSSESD	ESD protection ground pin. Connect to most negative supply voltage.
VSSSUB	Substrate ground pin. Connect to most negative supply voltage.
IP	Differential input signal pin. Complementary to pin IN.
IN	Inverse differential input signal pin. Complementary to pin IP.
OP	Differential output signal pin. Complementary to pin ON.
ON	Inverse differential output signal pin. Complementary to pin OP.
CP	Offset correction capacitor pin. Connect a capacitor between CP and CN.
CN	Offset correction capacitor pin. Connect a capacitor between CP and CN.
ENB	PGA enable pin. Connect this pin to VDD to disable the PGA operation.
B[5:0]	Gain setting pins. [000000] for 0dB and [111111] for 60dB gain setting.

4.2 ESD Protection

For deep submicron device, the thin oxide is weak and the static electricity will make the device damage because of the very large current go through the thin oxide and make the damage on the device. The electrostatic discharge (ESD) protection is added to each I/O pin to prevent the chip from being damaged by ESD. For the ESD protection, the diode protection is most common and has shown in Fig 4.6.

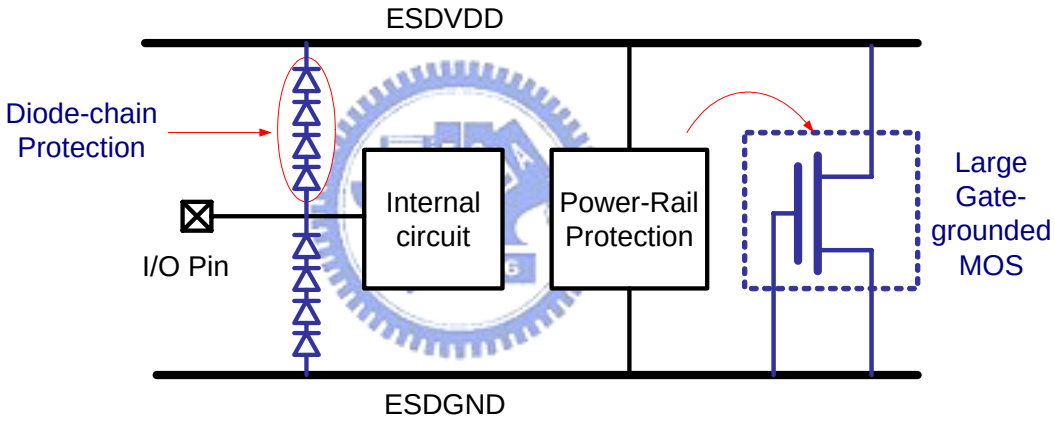


Fig.4.6 ESD Protection Circuit

The input diode-chain together with large gate-grounded MOSFET serves as protection against pin-to-pin ESD stress. In addition, large gate-grounded MOSFET can resist the rail-to-rail ESD stress as well. The diode chain is equivalent to a parasitic capacitance as small as 40fF, which has only a negligible influence on the input and output matching. The small parasitic capacitance of the diode from the ESD protection is about 40fF, the loading

effect is small and the overall performance is almost the same with the system without ESD protection. The large gate-grounded MOSFET is to be fabricated without LDD and salicide to reach the required high ESD protection level. The ESD protection circuit can provide 3.6-kV HBM protection.

The interface between an IC and the external world entails the problem of electrostatic discharge (ESD). This effect occurs when an external object having a high potential touches one of the connections to the circuit. Since the capacitance seen at each input or output is quite small, the ESD produces a large voltage, possibly damaging the devices fabricated on the chip.

MOS devices sustain two types of permanent damage as a result of ESD. First, the gate oxide may break down if the electric field exceeds roughly 10^7V/cm (e.g., 10V for an oxide thickness of 100Å), typically leading to a very low resistance between the gate and the channel. Second, the source/drain junction diodes may melt if they carry a large current in forward or reverse bias, creating a short to the bulk. For today's short-channel devices, both of these phenomena are likely to occur.

4.3 Package Issue

Package effect grows more and more important for modern circuit design because of the operation frequency becomes higher and higher. For the package we used, the serial inductance is about 1nH.

The 20-pin QFN package provided by SPIL is employed in our design and illustrated in Fig. 4.7. The package shows primarily inductive parasitic effect. Hence the parasitic effect of the package should be taken into account with cautious in order to precisely predict the circuit's performance. The major characteristic is the equivalent serial bond-wire inductance, which is about 1-nH for each pin. By shunting more pins for GND and VDD in layout, the effect of serial inductance can be reduced. The design of the PGA is operate in a small current consumption, the effect of the equivalent serial bond-wire inductance will be very small.

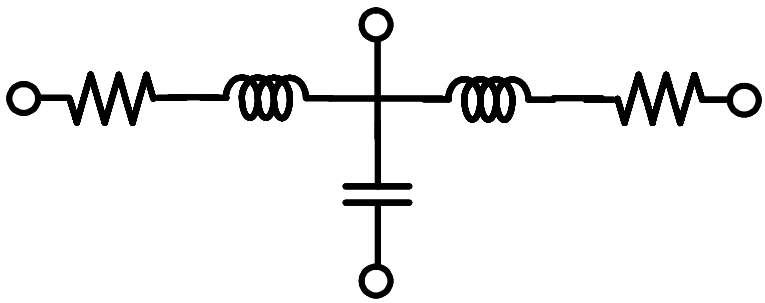


Fig.4.7 Effective model of package pins

4.4 PCB Layout

The printed circuit board (PCB) is designed for measurement the design chip. A circuit's performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via the power supply. The device has several round pins and a substrate connection. All of these should be connected to the circuit board's ground. Use multiple PCB vias close to the part to connect the grounds. Avoid long, inductive runs, which can degrade PGA performance. The PGA VDD supply pins should be decoupled separately.

Good high-frequency operation requires all of the de-coupling capacitors to be placed as close as possible to the power supply pins in order to insure a proper high-frequency low-impedance bypass. Adequate ground plane and low-inductive power returns are also required of the layout. Minimizing the parasitic capacitances will assure best high frequency performance.

The PCB layout should be done carefully, the width of the metal line from IC to SMA connector is not the same, thus the insertion loss will have problem. Therefore, the width of metal line from IC to SMA connector should be enlarged little by little. Besides, for the external passive devices, the self resonate frequency (SRF) should be chosen as one which is large than the desire frequency.

Fig.4.8 shows the PCB layout for the PGA package use. The PCB layout is designed using Protel. Part of the design guideline is the same with chip layout. The length of the differential inputs and outputs signal should be equal and symmetric to prevent phase mismatch.

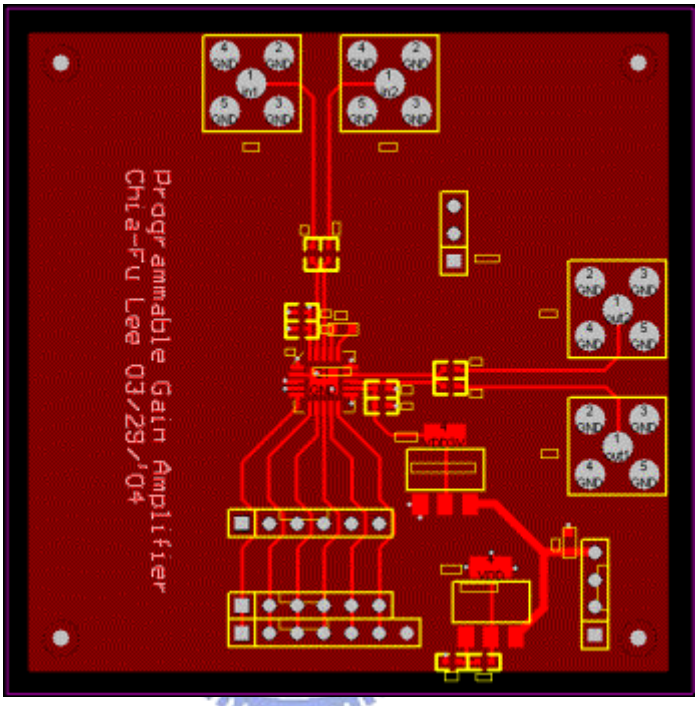


Fig.4.8 PCB design for PGA package use

An FR4 substrate was chosen for the PCB design because it was the thinnest substrate with readily available side-mounted connectors. The signal traces are coplanar waveguide with ground for improved grounding and ease of modification during evaluation. The top layer contains all mounted components, power and signal traces. The bottom layer is solid ground plane. Particular attention was paid to isolation and supply bypassing. Because excess signal is shunted to the VDD pin when the gain is not at maximum, bypassing on this pin is important to keep the excess signal from influencing the bias circuits.

Chapter 5
Measurement Results

5.1 Measurement Setup

The testing setup for PGA measurement is illustrated in Fig.5.1, which requires several instruments such as ESG signal generator and Spectrum Analyzer. The output of ESG is single-ended output, two ESG instruments can provide differential output signal by connection synchronization. The 1.8V and 3.3V supply voltages are generated by two regulators with a 5V power supply. The Spectrum Analyzer can measure gain curve, frequency response and 1-dB compression.

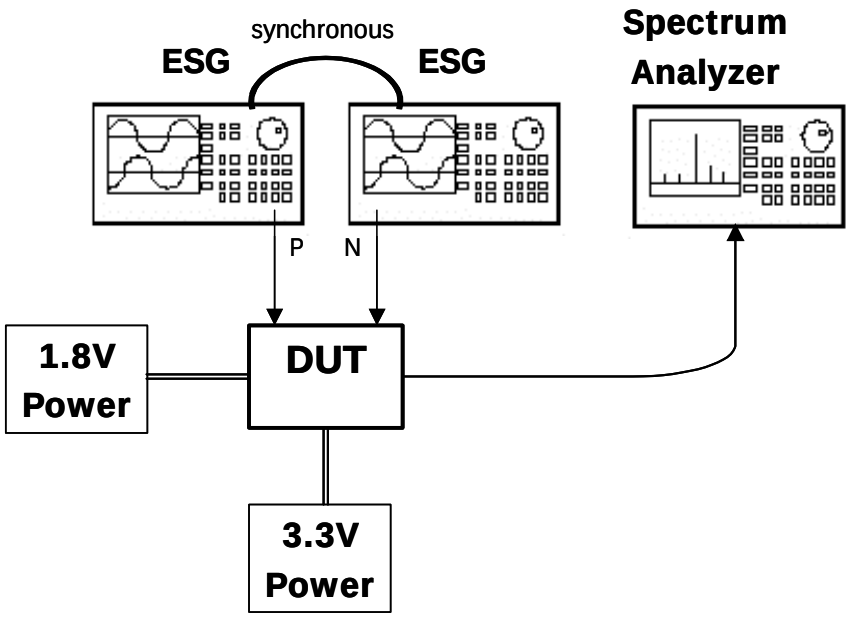


Fig.5.1 Environment setup for testing

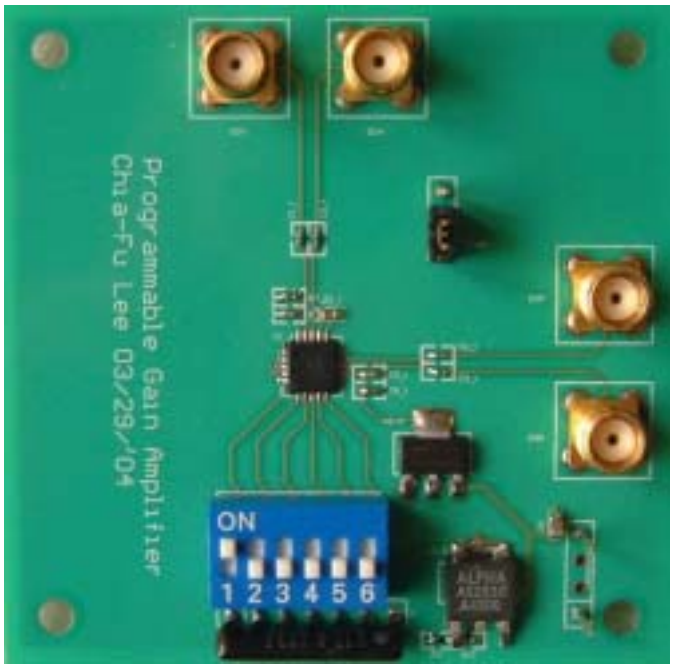


Fig.5.2 Device under test PCB

5.2 Measurement Results

The gain value and gain curve is shown in Table 5.1 and Fig.5.3. It shows that the measurement gain value is close to the target setting. Also the gain curve is monotonic increasing function.

Table 5.1 Measurement gain value versus gain setting

Setting	Gain(dB)	Setting	Gain(dB)	Setting	Gain(dB)	Setting	Gain(dB)
0 dB	1.30	16 dB	17.68	32 dB	33.88	48 dB	49.29
1 dB	2.66	17 dB	18.82	33 dB	34.89	49 dB	50.15
2 dB	3.63	18 dB	19.85	34 dB	35.87	50 dB	51.02
3 dB	4.84	19 dB	20.94	35 dB	36.83	51 dB	51.80
4 dB	5.63	20 dB	21.97	36 dB	37.75	52 dB	52.72
5 dB	6.80	21 dB	22.99	37 dB	38.74	53 dB	53.71
6 dB	7.82	22 dB	23.98	38 dB	39.61	54 dB	54.59
7 dB	8.88	23 dB	25.01	39 dB	40.57	55 dB	55.58
8 dB	9.67	24 dB	25.98	40 dB	41.57	56 dB	56.57
9 dB	10.86	25 dB	26.99	41 dB	42.52	57 dB	57.44
10 dB	11.84	26 dB	27.98	42 dB	43.56	58 dB	58.47
11 dB	12.90	27 dB	29.03	43 dB	44.59	59 dB	59.42
12 dB	13.85	28 dB	30.04	44 dB	45.65	60dB	60.31
13 dB	14.86	29 dB	31.10	45 dB	46.55		
14 dB	15.87	30 dB	31.99	46 dB	47.40		
15 dB	16.88	31 dB	32.98	47 dB	48.36		

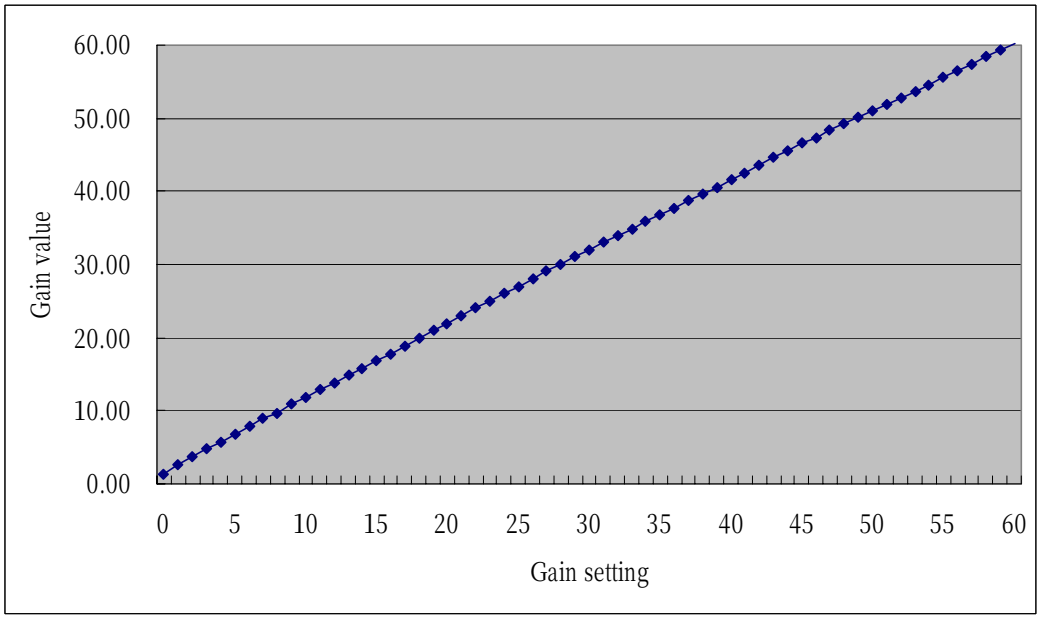


Fig.5.3 Measurement gain curve versus gain setting

Fig.5.4 shows the input 1-dB compression of PGA at 0dB gain setting.

$$P,in = 10^{\frac{-2dBm}{10}} = 0.631mW$$
$$V1-dB,in = \sqrt{2} \times \sqrt{50ohm \times P,in} = 0.251V \quad (5.1)$$

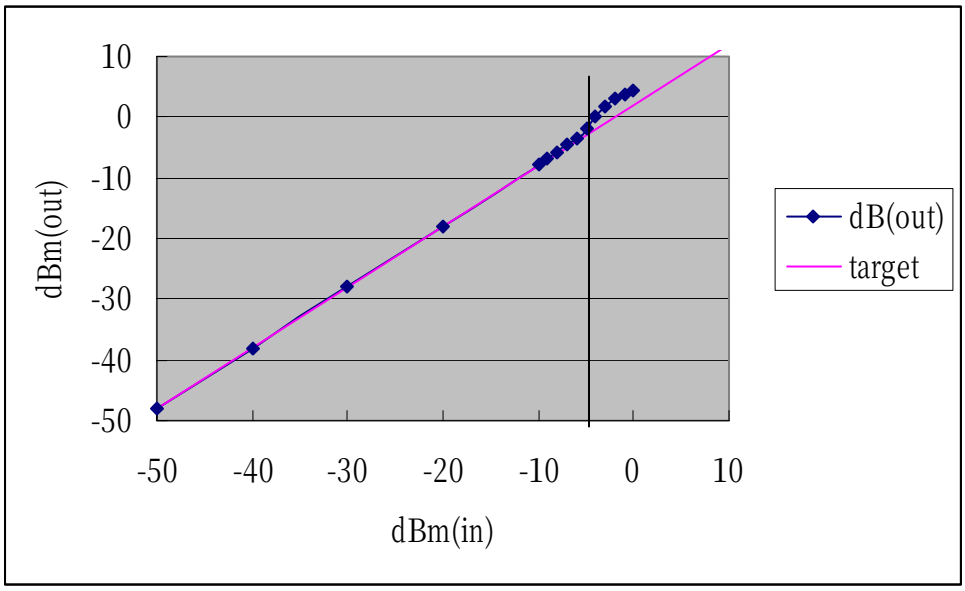


Fig.5.4 Measurement 1-dB compression of PGA at 0dB gain

Fig.5.5 shows the output 1-dB compression of PGA at 60dB gain setting.

$$P,out = 10^{\frac{2.5dBm}{10}} = 1.778mW$$
$$V1-dB,out = \sqrt{2} \times \sqrt{50ohm \times P,out} = 0.422V \quad (5.2)$$

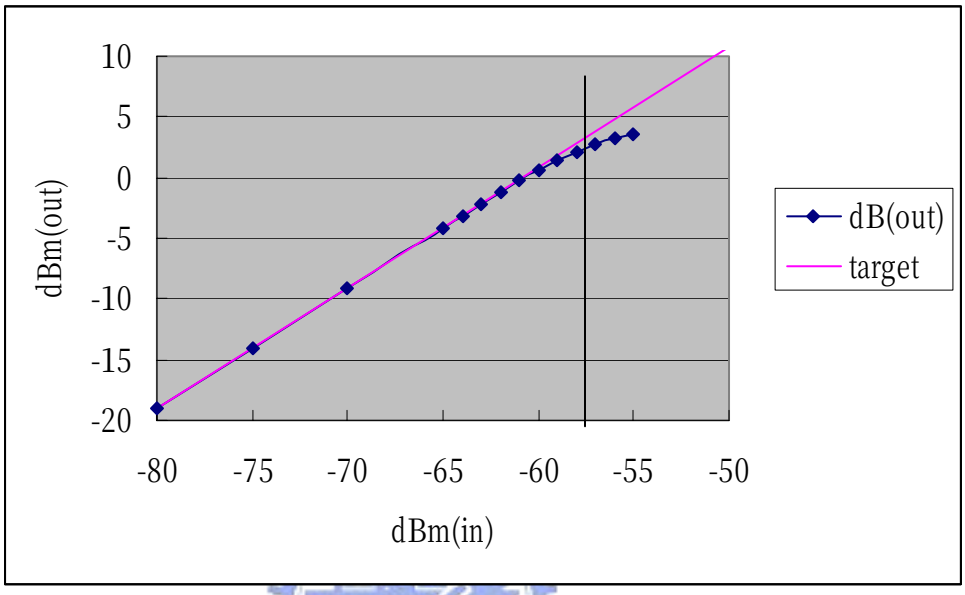


Fig.5.5 Measurement 1-dB compression of PGA at 60dB gain

5.3 Summary

Table 5.2 summarizes the measured performance of the PGA chip. The bandwidth cannot be measured since there is a resonate frequency near 3dB frequency. The gain range is 0 to 60dB with 1dB gain step as shown in Fig.5.1. The input 1-dB compression is 0.251V and output 1-dB compression is 0.422V as shown in Fig.5.3 and Fig.5.4. When process shift, the DC-offset-cancellation feature will shift the output DC-level and reduce the output 1-dB compression value. Finally, the operation current is 2.14mA and so the power consumption is 3.85mW. Table 5.3 shows the performance compare to other design.

Table 5.2 Performance summary of the PGA

Item	Specification	Simulation	Measurement
Bandwidth	>12MHz	125MHz	~125MHz
Gain Range	0~60 dB	0~60 dB	0~60 dB
Gain Step	1dB	1dB	1dB
Input Referred Noise	10 nV/√Hz	6.553 nV/√Hz	
1-dB Compression,in	0.35V	0.252V	0.251V
1-dB Compression,out	-	0.531V	0.422V*
Power consumption	-	3.73mW	3.85mW

* : due to process deviation

Table 5.3 Performance compare

Design	[1]	[2]	[3]	[4]	This work
Bandwidth	15 MHz	100 MHz	x (oper.246MHz)	36MHz	125MHz
Gain Range	-2~12 dB	5.6~17 dB	-15~45 dB	-4~64 dB	0~60 dB
Gain Step	-	-	2dB	2dB	1dB
Input Referred Noise	16.75 nV/√Hz	12 nV/√Hz	-	26 nV/√Hz	6.553 nV/√Hz
Technology	0.5 μm CMOS	0.25 μm CMOS	0.35 μm CMOS	0.25 μm CMOS	0.18 μm CMOS
Total Current	5 mA	2.7 mA	9mA	1.5mA	2.14mA
Supply Voltage	5 V	2.5V	3V	2.5V	1.8V

5.4 Debugs

Fig.5.6 shows the PGA output spectrum has a 146MHz resonate oscillation frequency.

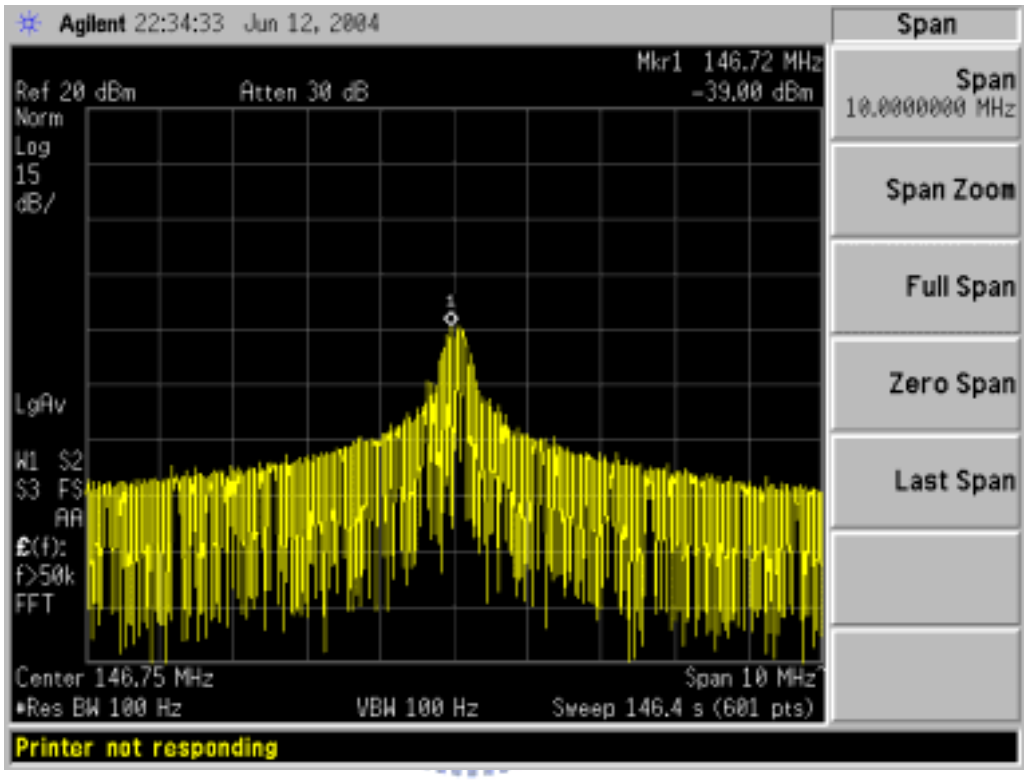


Fig.5.6 Resonate oscillation spectrum

The resonate frequency source may caused of the DC-offset-cancellation closed-loop. Fig.5.7 is the DC-offset-cancellation loop gain and phase curve, which does not connect the cancellation capacitor C3 as shown in Fig.3.16. It's clear that the resonate frequency is 150MHz. Fig.5.8 is the DC-offset-cancellation loop gain and phase curve, which the cancellation capacitor is connected. Since the close-loop gain is less than 0dB, it should have not oscillation issue.

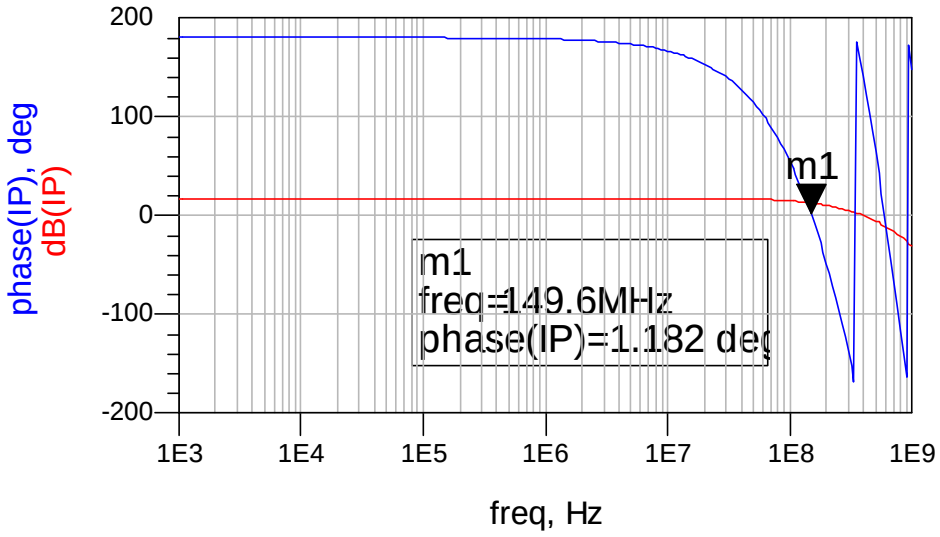


Fig.5.7 DC-offset-cancellation loop gain curve and phase curve, the cancellation capacitor is not connected.

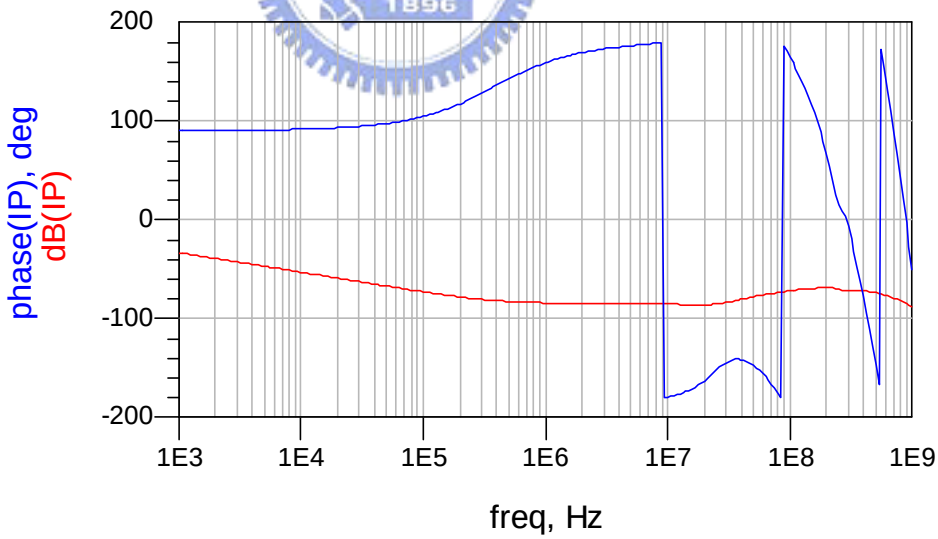


Fig.5.8 DC-offset-cancellation loop gain curve and phase curve, the cancellation capacitor is connected.

Chapter 6
Conclusions and Future Works

6.1 Conclusions

In this thesis, the PGA suit for dual-band wireless system is designed, implemented, and measured. The chip is fabricated using UMC 0.18um 1P6M CMOS technology. The chip area is 0.01 mm^2 and the power consumption is only 3.73mW from a 1.8V supply voltage. The 20-pin QFN package provided by SPIL is used in this design, and the FR-4 PCB is used for measurement and verification. The measurement results show that the chip of PGA is closed to simulation.

Although the resonate frequency cannot be removed in current state, the PGA circuit will include an 8MHz/12MHz low-pass filter in the application of dual-band wireless system. It will efficiently remove the 146MHz resonate frequency. Exclude the resonate issue, the design of PGA can serve a trusty programmable gain amplifier.

6.2 Future Works

First, the resonate issue should be improved. One of the solutions is included the low-pass filter as describe in section 6.1. Also there is many other DC-offset-cancellation technique can be replaced to fix the process deviation issue.

Second, the degeneration resistor of 4^{th} stage gain-amplifier has been better re-calculated. The gain value of the proposed PGA is depending on the load resistor to degeneration resistor ratio. The load resistor of 4^{th} stage is changed by the DC-offset-cancellation circuit, so the gain step has a little difference to the front gain stages. To obtain a more accurate gain step, the degeneration resistor of 4^{th} stage gain-amplifier should be re-calculated.

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