My-box representation for faulty CMOS circuits

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Abstract: A new logic element, My-box, is proposed to model the line faults (stuck-at-1 and stuck-at-0) and the transistor faults (stuck-on and stuck-open) of CMOS circuits, which consist of fully CMOS logic, pseudo *n*MOS logic, dynamic CMOS logic, clocked CMOS (C^2MOS) logic, CMOS domino logic and NORA CMOS logic. It can also be used to model the faults and the functions of a transmission gate logic. A procedure is described to transform a transistor level CMOS circuit to a gate-level equivalent circuit which is composed of AND, OR and the My-box logic element. A fault collapsing procedure is also derived to determine the representative set of prime faults (RSPF) for the transformed gate-level circuit. By applying this procedure to ten benchmark circuits, the number of faults can be reduced to approximately 15% of the original total faults, if the ten benchmark circuits are implemented in the fully CMOS logic.

1 Introduction

In combinational CMOS circuits, the transistor stuck-open faults introduce 'memory' behaviour. To detect this type of fault, a special test procedure is required [1, 2]. For transistor stuck-on faults, the faults may or may not be detectable, depending on the resistance of the stuck-on devices. Hence, CMOS technology poses a special challenge to testing [3].

Most conventional testing procedures treat the problem at gate level. There have been proposed fault models which cover line faults (stuck-at-1 and stuck-at-0) as well as transistor faults (stuck-on and stuck-open). For example, 'gate-latch' [4], 'B-block' [5] and 'D-latch' [6] have been introduced to represent the 'memory' behaviour of CMOS circuits. In this paper, a new logic element, My-box is proposed to model faults in CMOS circuits. It has the following advantages over the previously proposed models:

(*a*) it can model all types of CMOS circuits which include fully CMOS, pseudo *n*MOS, dynamic CMOS [7], clocked CMOS [8], domino CMOS [9] and NORA CMOS [10] circuits. It can also model faults and the function of the transmission gate logic

(*b*) the same logic diagrams are used to represent both the *p* and *n* transistor circuits of the fully CMOS circuit

(*c*) all the line faults and transistor faults have the corresponding faults in the transformed gate-level equivalent circuit

(*d*) fault-collapsing procedure can be applied to the transformed circuit to reduce the number of faults

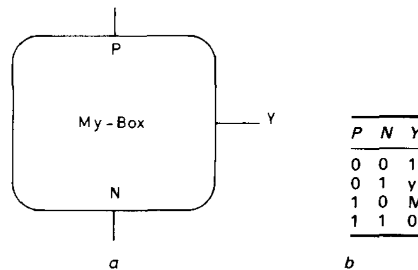
(*e*) the classical test pattern generation algorithms such as PODEM [11], FAN [12] and SLOPE [13] can be applied to the transformed circuit to generate tests.

In the paper, a transformation procedure is proposed to transform a CMOS transistor-level circuit to the gate-level equivalent circuit with My-box logic elements. A fault-collapsing procedure is also presented to collapse faults based on the equivalence and the dominance relationships [14]. This fault-collapsing procedure is a further improvement over that of Reddy *et al.* [15], who derived the 'checkpoint' faults in their equivalent gate-level circuits. Ten benchmark circuits [16] have been applied with this fault-collapsing procedure to derive the representative sets of prime faults (RSPF). On average, the fault number can be reduced to 15% of the original total faults.

2 Gate-level equivalent circuits

2.1 My-box logic representation

The logic diagram and the truth table of the My-box logic element are shown in Fig. 1, where 'M' represents the high-impedance (memory) state and 'y' may be 0 or 1, depending on whether the represented circuit is *GND*-dominant or V_{DD}-dominant. (The circuit can be designed in such a way that, once the stuck-on fault occurs, the circuit always goes to '0' (*GND*-dominant) or '1' (V_{DD}-dominant)). The fully CMOS circuit of Fig. 2*a* can be represented with the My-box logic element at Fig. 2*b*, where both *p* and *n* gate blocks have the same logic diagram. In the transformed equivalent circuit, the *p* and *n* gate blocks are converted directly from the *p*MOS and *n*MOS transistor circuits, respectively. Every *p*(*n*)MOS



P	N	Y
0	0	1
0	1	y
1	0	M
1	1	0

Fig. 1 *Logic diagram and truth table of My-box representation*
M = memory
y = '1' or '0'

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transistor has a corresponding input in the $p(n)$ gate blocks of the equivalent circuit, and there exist corresponding faults between the transistor diagram and the equivalent logic circuit. In the transformed equivalent circuit, except for the My-box logic element, only AND and OR logic gates are used. This makes the conventional test generation algorithms directly applicable to the circuit.

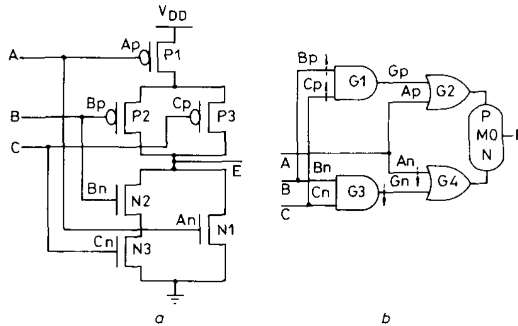


Fig. 2
a Fully CMOS example circuit
$E = \neg(A + BC)$
b My-box representation for circuit of Fig. 2a

2.2 Procedure to convert transistor-level circuits to gate-level equivalent circuits

Any planar nonbridge (series-parallel) network of a fully CMOS circuit can be converted to a gate-level equivalent circuit incorporating My-box logic elements. The procedure to construct the equivalent gate level circuit consists of two main steps.

Step 1: For each CMOS gate in the circuit, replace it by a network consisting of My-box logic element driven by two logic blocks, i.e. the p and n gate blocks which are constructed by step 2.

Step 2: Iteratively replace the series connections of pMOS (nMOS) transistors with OR (AND) gates and the parallel connections of pMOS (nMOS) transistors with AND (OR) gates according to Table 1.

For the transformed gate-level equivalent circuit, converted with the above procedure, some properties can be found as follows:

Property 1: There is a one-to-one correspondence between input nodes of the planar nonbridge transistor-level circuit and the transformed gate-level equivalent circuit.

Proof: Since the structure of the transistor diagram is series parallel, the input nodes corresponding to the gate inputs of transistors will not be missed and reduplicated during the transformation procedure.

Property 2: For any planar nonbridge transistor-level circuit, the transformed equivalent circuit contains, in addition to My-box logic elements, only AND and OR gates.

Proof: Since the transistor-level circuit is series parallel, it is equivalent to the combination of AND and OR gates.

Property 3: For the transistor-level circuit, if there exists a connection graph [17] G for the pMOS network, and its dual graph G^D for the nMOS network, the same logic

Table 1: Transformation rules for CMOS transistor circuits to LOGIC gates

MOS ——→	LOGIC
single pMOS transistor	single input AND/OR gate or a wire
single nMOS transistor	single input AND/OR gate or a wire
series pMOS transistors	OR gate
parallel pMOS transistors	AND gate
series nMOS transistors	AND gate
parallel nMOS transistors	OR gate

diagram will be obtained to represent both the P and N gate blocks in the transformed equivalent circuit.

Proof: From the principle of duality, the proof is trivial.

2.3 Application to other CMOS logic circuits

The above transformation procedure cannot only be applied to fully CMOS logic, but can also be applied to other CMOS circuits such as pseudo nMOS logic, dynamic CMOS logic, C^2MOS logic, CMOS domino logic and NORA CMOS logic.

Fig. 3 shows an example, which is a dynamic CMOS AOI logic gate, where $E = \neg(A + BC)$ and Φ is the clock signal. When $\Phi = 0$, $E = 1$ and when $\Phi = 1$, $E = \neg(A + BC)$. The procedure of the above Section is applied as follows to derive the n gate block:

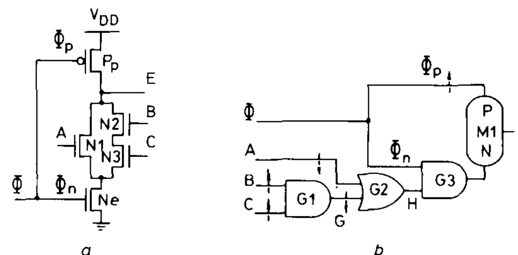


Fig. 3 *Gate-level representation of dynamic CMOS circuit using My-box representation*
a Transistor circuit
Φ_p and Φ_n are clocking lines for precharge transistor Pp and evaluation transistor Ne, respectively
b My-box representation

Step 1: Replace the gate output E with a My-box logic element.

Step 2: (*a*) Replace the serially connected $N2$ and $N3$ transistors with an AND gate with gate inputs B and C and gate output G, and collapse these transistors to a new transistor $N4$.

(*b*) Replace the parallel-connected $N1$ and $N4$ transistors with an OR gate with gate inputs A and G and gate output H, and collapse these transistors to a new transistor $N5$.

(*c*) Replace the serially connected Ne and $N5$ transistors with an AND gate with gate inputs Φ_n and H and its output connected to input n of My-box.

For the p gate block, only one transistor needs to be transformed. It can be modelled by either a single input AND gate or a single input OR gate or just a connection of wire. Fig. 3*b* is the converted gate-level equivalent circuit, where the My-box logic element is an 'M1-box'. For this equivalent circuit, there is no p gate block, but properties 1 and 2 still hold.

3 Fault correspondence and fault-collapsing procedure

In this Section, the fault correspondence between the transistor-level circuit and the transformed gate-level equivalent circuit is discussed. A fault-collapsing procedure is also derived to apply to the transformed gate-level equivalent circuits to reduce faults.

3.1 Fault correspondence

As discussed in the preceding Section, p and n gate blocks are converted directly from the respective pMOS and nMOS transistor circuits, and all gates of p and nMOS transistors have corresponding inputs in the p and n gate blocks of the equivalent circuit, respectively. There exist corresponding faults between the transistor diagram and the transformed equivalent circuit. The following lemmas hold:

Lemma 1: The stuck-at-0/1 faults at the inputs of a gate in the p gate block of the transformed equivalent circuit are equivalent to the stuck-open/on faults of the corresponding transistors in the pMOS network of the transistor circuit.

Lemma 2: The stuck-at-0/1 faults at the inputs of a gate in the n gate block of the transformed equivalent circuit are equivalent to the stuck-open/on faults of the corresponding transistors in the nMOS network of the transistor circuit.

Lemma 3: The line stuck-at-0/1 faults at the inputs and the output of a gate of the transistor circuit and its corresponding gate in the transformed equivalent circuit are equivalent.

From the above lemmas, the following property can be obtained.

Property 4: There is a one-to-one correspondence between faults in the transistor-level circuit and the transformed gate-level equivalent circuit.

For example, Tables 2*a* and *b* list the corresponding faults between the transistor-level circuits of Fig. 2*a* and the transformed gate-level equivalent circuit of Fig. 2*b*. It can be seen that all the line faults and transistor faults in the transistor-level circuit can be represented by the stuck at faults in the gate-level equivalent circuit.

Another example is shown in Tables 3*a* and *b*, which list the corresponding faults between the transistor diagram of Fig. 3*a* and the transformed equivalent circuit of Fig. 3*b*. It is also seen that the faults in the transistor-level circuit are fully represented by the faults in the gate-level equivalent circuit.

3.2 Fault-collapsing analysis

Faults in the transformed gate-level equivalent circuit can be collapsed according to the equivalence and dominance

Table 2: Fault tables for circuits of Fig. 2

				Line faults						Transistor faults											
A	*B*	*C*	*E*	*A* sa1	*B* sa1	*C* sa1	*A* sa0	*B* sa0	*C* sa0	*N*1 son	*N*2 son	*N*3 son	*P*1 son	*P*2 son	*P*3 son	*N*1 sop	*N*2 sop	*N*3 sop	*P*1 sop	*P*2 sop	*P*3 sop
0	0	0	1	0						0									M		
0	0	1	1	0	0					0	0								M	M	
0	1	0	1	0		0				0		0							M		M
0	1	1	0					1	1					0	0		M	M			
1	0	0	0				1						0			M					
1	0	1	0				1						0			M					
1	1	0	0				1						0			M					
1	1	1	0																		

a

A	*B*	*C*	*E*	*A* sa1	*B* sa1	*C* sa1	*A* sa0	*B* sa0	*C* sa0	*An* sa1	*Bn* sa1	*Cn* sa1	*Ap* sa0	*Bp* sa0	*Cp* sa0	*An* sa0	*Bn* sa0	*Cn* sa0	*Ap* sa1	*Bp* sa1	*Cp* sa1
0	0	0	1	0						0									M		
0	0	1	1	0	0					0	0								M	M	
0	1	0	1	0		0				0		0							M		M
0	1	1	0					1	1					0	0		M	M			
1	0	0	0				1						0			M					
1	0	1	0				1						0			M					
1	1	0	0				1						0			M					
1	1	1	0																		

b

The circuit is assumed to be *GND* dominant

a List of line faults and transistor faults for the circuit of Fig. 2*a*

b List of stuck-at faults for the circuit of Fig. 2*b*

Table 3: Fault tables for circuits of Fig. 3

				Line faults								Transistor faults									
A	*B*	*C*	*E*	*A* sa1	*B* sa1	*C* sa1	Φ sa1	*A* sa0	*B* sa0	*C* sa0	Φ sa0	*N*1 son	*N*2 son	*N*3 son	*Ne* son	*Pp* son	*N*1 sop	*N*2 sop	*N*3 sop	*Ne* sop	*Pp* sop
0	0	0	1	0								0									M
0	0	1	1	0	0							0	0								M
0	1	0	1	0		0						0		0							M
0	1	1	0						1	1	1					1		1	1	1	
1	0	0	0					1			1					1	1			1	
1	0	1	0					1			1					1	1			1	
1	1	0	0					1			1					1	1			1	
1	1	1	0								1					1				1	

a

A	*B*	*C*	*E*	*A* sa1	*B* sa1	*C* sa1	Φ sa1	*A* sa0	*B* sa0	*C* sa0	Φ sa0	*A* sa1	*B* sa1	*C* sa1	Φ_n sa1	Φ_p sa0	*A* sa0	*B* sa0	*C* sa0	Φ_n sa0	Φ_p sa1
0	0	0	1	0								0									M
0	0	1	1	0	0							0	0								M
0	1	0	1	0		0						0		0							M
0	1	1	0						1	1	1					1		1	1	1	
1	0	0	0					1			1					1	1			1	
1	0	1	0					1			1					1	1			1	
1	1	0	0					1			1					1	1			1	
1	1	1	0								1					1				1	

b

The circuit is assumed to be V_{DD} dominant
a List of line faults and transistor faults for the circuit of Fig. 3*a*
b List of stuck-at faults for the circuit of Fig. 3*b*

relationships [14]. In this Section, a fault-collapsing procedure is presented. First, some theorems and related corollaries are stated.

3.2.1 Intergate fault collapsing

Lemma 4: In CMOS circuits, the stuck-at-1 (or 0) fault at the output of a gate dominates the single stuck-at-0 (or 1) fault at the input of *n*(or *p*) gate block.

Proof: To test the stuck-at-0 fault at an input *i* of the *n* gate block, it is sufficient to apply a '1' to the input *i*, after an initialising pattern. This will cause the output to '0', thus the stuck-at-1 fault at the output is also detected. Similarly, the test to detect the stuck-at-1 fault at the input of *p* gate block will also detect the stuck-at-0 fault at the output.

Theorem 1: Given a CMOS fanout-free combinational circuit *C*, we can test the entire circuit for single stuck-at or stuck-on/open faults by testing only the single stuck-on and stuck-open faults of transistors associated with the primary inputs, provided that the initialisation part of the test sequence can propagate to the primary output.

Proof: From property 4, every fault in the transistor circuit has a one-to-one corresponding stuck-at fault in the transformed equivalent circuit. Hence, the stuck-at faults in the equivalent circuit only are considered.

Assume a set of tests *T* detects all stuck-at faults on the primary inputs of *C* but does not detect some internal faults. Then there must be some gate *G* in *C* such that *T* detects all faults on the inputs of *G* but does not detect some output fault. However, from lemma 4, the output faults must also be detected since the output faults dominate the input faults of any gate. Therefore, the test *T* will detect all the stuck-at faults. From lemmas 1, 2 and 3, the test *T* which detects the single stuck-on and stuck-open faults associated with the primary inputs will detect all single stuck-at, stuck-on and stuck-open faults of the entire circuit *C*.

Theorem 2: Given a CMOS irredundant combinational circuit, we can test the entire single stuck-at or stuck-on/open faults by testing only the single stuck-at faults of the fanout stems of primary inputs, and the single stuck-on and stuck-open faults of transistors associated with the primary inputs and fanout branches, provided that the initialisation part of the test sequence for each line can propagate to primary outputs.

Proof: Theorem 1 covers the case of fanout-free circuits. However, for reconvergent fanout circuits, they can be decomposed into many fanout-free subcircuits and fanout stems of primary inputs. From theorem 1, all faults in a fanout-free subcircuit are tested by testing the transistors associated with the primary inputs. The primary inputs in this case can be primary inputs or fanout branches originating from the primary inputs or from the output of a subcircuit. Hence, by combining with the stuck-at faults of the fanout stems of primary inputs and the transistor faults associated with the primary inputs and fanout branches, the set of tests for these faults must test the entire circuit.

3.2.2 Intragate fault collapsing

Theorem 3: For the equivalent circuit of a CMOS circuit

(i) the stuck-at-0(or 1) faults at the inputs and the output of an AND(or OR) gate are equivalent

(ii) the stuck-at-1(or 0) fault at the output of an AND(or OR) gate dominates the stuck-at-1(or 0) faults at the inputs of the gate.

Proof: The proof is the same as that for a conventional gate-level circuit [17], except that the test may follow an initialising pattern.

Corollary 1: If transistors are connected in parallel, then the stuck-on faults of these transistors are equivalent.

Proof: Assume that these parallel transistors are *p*MOS transistors. They will be converted to an AND gate in the gate-level equivalent circuit. From lemma 1, stuck-at-0 faults in the equivalent circuit correspond to stuck-on faults in the transistor circuit. From theorem 3i, for an AND gate, all input stuck-at-0 faults are equivalent. Similarly, for the parallel *n*MOS transistors, the stuck-on faults of these transistors are equivalent.

Corollary 2: If transistors are connected in series, then the stuck-open faults of these transistors are equivalent.

Proof: The proof is similar to that of the above corollary except that an initialising pattern is applied before the test pattern.

Similarly, the stuck-on fault in *p*MOS network dominates the corresponding stuck-open fault in the *n*MOS network.

These corollaries agree with those of Chiang [2] and Shih [19], who dealt with the problem at the transistor level.

3.2.3 Fault-collapsing procedure

With the above theorems and corollaries, the fault-collapsing procedure for the transformed gate-level equivalent circuit is given as follows:

Step 1: Determine all the primary inputs and fanout nets and label each primary input and fanout net as a *C*-net.

Step 2: Determine all the dual inputs for *p* gate blocks and *n* gate blocks in the logic gate equivalent circuit and label each dual input as a dual node.

Step 3: Flag both S-A-1 and S-A-0 on the fanout stem of each primary input.

Step 4: FOR each logic gate *G* of the *p*(*n*) logic gate block:
IF all the inputs of *G* are *C*-net,
THEN, IF all the inputs of *G* are dual node,
THEN flag (1) an S-A-1(0) on the output of *G*, if *G* is an OR(AND) gate;
(2) an S-A-1(0) on each input of *G*, if *G* is an AND(OR) gate;
ELSE flag (1′) an S-A-1(0) on the output of *G* and an S-A-0(1) on each nondual node input of *G*, if *G* is an OR(AND) gate;
(2′) an S-A-0(1) on the output of *G* and an S-A-1(0) on each input of *G*, if *G* is an AND(OR) gate;
(END IF)
ELSE flag (1″) an S-A-0(1) on each *C*-net and nondual node input of *G*, if *G* is an OR(AND) gate;
(2″) an S-A-1(0) on each *C*-net input of *G*, if *G* is an AND(OR) gate.
(END IF)

Step 5: The flagged faults constitute an RSPF.

An example is used to demonstrate the above procedure. Consider the logic-level equivalent circuit shown in Fig. 2*b*.

Step 1: Nodes *A*, *B*, and *C* are determined and labelled to be *C*-nets.

Step 2: Nodes *A*, *B* and *C* are determined and labelled to be dual nodes.

Step 3: No fault is flagged.

Step 4: For gate *G*1, an S-A-1 on each input is flagged;
for gate *G*2, no fault is flagged;
for gate *G*3, an S-A-0 on the output is flagged;
for gate *G*4, an S-A-0 on the input *An* is flagged.

Step 5: The RSPF of the circuit consists of the stuck-at-1 fault at *Bp*, the stuck-at-1 fault at *Cp*, the stuck-at-0 fault at *An*, and the stuck-at-0 fault at *Gn*.

Theorem 4: If the same logic diagrams exist for the *p* and *n* gate blocks of the gate-level equivalent circuit, the stuck-at-1 faults at inputs of a gate in the *n* gate block dominate the stuck-at-1 faults of the inputs of the corresponding gate in the *p* gate block.

Proof: Since *p* and *n* gate blocks have the same logic diagram, a test with an initialising pattern which can detect the stuck-at-1 faults in the *p* gate block must detect the corresponding stuck-at-1 faults in the *n* gate block.

Theorem 5: If the same logic diagrams exist for the *p* and *n* gate blocks of the gate-level equivalent circuit, the stuck-at-0 faults at inputs of a gate in the *p* gate block dominate the stuck-at-0 faults of the inputs of the corresponding gate in the *n* gate block.

Proof: The proof is the same as that of theorem 4.

Corollary 3: If the same logic diagrams exist for the *p* and *n* gate blocks of the gate-level equivalent circuit, the stuck-on faults of the transistors in the *p*MOS(or *n*MOS) network of the transistor network dominate the stuck-open faults of the corresponding transistors in the *n*MOS(or *p*MOS) network.

Proof: From lemmas 1 and 2, a stuck-at-1 fault in the *p*(or *n*) gate block represents a stuck-open (or stuck-on) fault in the *p*MOS(or *n*MOS) network. From theorem 4, a stuck-at-1 fault in *n* gate block dominates the corresponding stuck-at-1 fault in the *p* gate block. Therefore, the stuck-on fault in the *n*MOS network dominates the corresponding stuck-open fault in the *p*MOS network.

Table 4*a* lists the reduced RSPF fault table for this circuit and the reduced prime faults are marked in the equivalent circuit of Fig. 2*b*. The same step-by-step procedure can be applied to the gate-level equivalent circuit of Fig. 3*b* to reduce faults to obtain the RSPF as shown in Table 4*b*. The reduced prime faults are marked in the circuit of Fig. 3*b*.

Figs. 4 and 5 are another two examples, one of which is a pseudo *n*MOS logic circuit and the other is C^2MOS logic circuit. The reduced RSPF faults for each circuit are marked on the respective transformed gate-level equivalent circuits of Figs. 4 and 5*b*.

This fault-collapsing procedure has been applied to ten benchmark circuits [15] to reduce faults by assuming that these circuits are implemented in the fully CMOS

Table 4: Reduced RSPF fault tables for circuits of Fig. 2b and Fig. 3b

A	B	C	E	An sa0	Gn sa0	Bp sa1	Cp sa1
0	0	0	1				
0	0	1	1			M	
0	1	0	1				M
0	1	1	0		M		
1	0	0	0	M			
1	0	1	0	M			
1	1	0	0	M			
1	1	1	0				

a

A	B	C	E	A sa0	B sa1	C sa1	G sa0	Φ_p sa1
0	0	0	1					M
0	0	1	1		0			M
0	1	0	1			0		M
0	1	1	0				1	
1	0	0	0	1				
1	0	1	0	1				
1	1	0	0	1				
1	1	1	0					

b

a List of RSPF faults for the circuit of Fig. 2b
b List of RSPF faults for the circuit of Fig. 3b

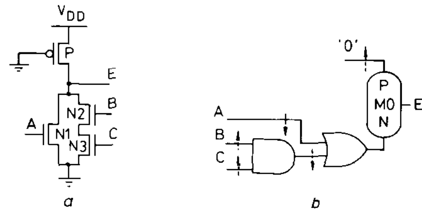


Fig. 4 *Gate-level representation of pseudonMOS circuit using the My-box representation*
a Transistor circuit
Gate input of transistor *P* is connected to ground
b My-box representation
Input *P* of M0-box is connected to logic '0'

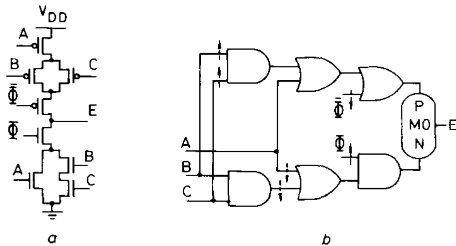


Fig. 5 *Gate-level representation of clocked CMOS circuit using the My-box representation*
a Transistor circuit
Φ and ¬Φ are clocking lines
b My-box representation

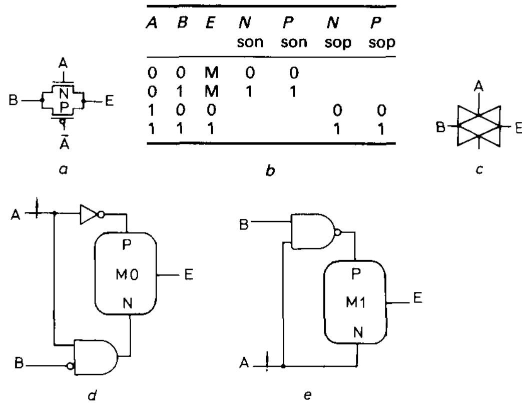
logic circuit. Table 5 is a compilation of the results after the fault reduction. The number of faults can be reduced to approximately 15% of the original total faults.

4 Representation for transmission gates

A transmission gate functions as a switch with a charge retention (memory) capability in its OFF state. Although it is a bidirectional device, it is often used as a unidirectional element whose normal and faulty functions are represented in the truth table as shown in Fig. 6, along with its transistor circuit diagram. Functionally, the My-box logic element can also model its logic behaviour. In this Section, the gate-level equivalent circuit using My-box elements for the transmission gate logic circuit is demonstrated. However, the proposed procedure to construct the logic-level equivalent circuit and the fault-collapsing procedure to obtain the RSPF can not be applied to a transmission gate circuit. The RSPF can be derived from the fault table of the circuit.

Table 5: Results of applying fault-collapsing procedure to ten benchmark circuits if they are implemented in fully CMOS circuit

Circuit	Total gate	Total tx and line fault	Reduced prime fault	%
*C*432	160	2408	442	18.4
*C*499	202	2934	690	23.5
*C*880	383	5254	737	14.0
*C*1355	546	7560	1194	15.8
*C*1908	880	10806	1349	12·5
*C*2670	1193	15308	1964	12.8
*C*3540	1669	21066	2459	11.7
*C*5315	2307	34966	4072	11.6
*C*6288	2406	33648	5824	17.3
*C*7552	3512	44310	5402	12.2



A	B	E	N son	P son	N sop	P sop
0	0	M	0	0		
0	1	M	1	1		
1	0	0			0	0
1	1	1			1	1

Fig. 6 *Transmission gate as unidirectional logic element and its My-box representations*
a Transistor diagram
b Fault table
c Simplified symbol
d M0-box representation
e M1-box representation

For a single transmission gate, any single transistor stuck-open fault is not detectable since the faulty value is not distinguishable from the fault-free value. Only stuck-on faults need to be modelled. The gate level representation is shown in Fig. 6d and e. Either an 'M0-box' or an 'M1-box', depending on the technology, can be used to model the circuit. The stuck-on fault is represented with a stuck-at-1 fault in the equivalent circuit.

For the parallel transmission gates shown in Fig. 7a, the output of the circuit can be either a wire-AND or a wire-OR, depending on the technology. For the wire-AND case, the 'M0-box' can be used to construct the gate-level equivalent circuit as shown in Fig. 7b, and for the wire-OR case, the M1-box' can be used to construct

the equivalent circuit as shown in Fig. 7*c*. For both of the representing circuits, only the stuck-at-1 faults at nodes *A* and *C* are adequate to model the stuck-on faults of the original circuit.

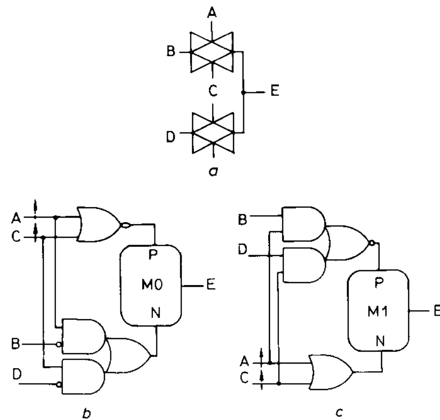


Fig. 7 *Transmission gates connected in parallel and their My-box representations*

a Logic diagram
b M0-box representation for the wire-AND operation
c M1-box representation for the wire-OR operation

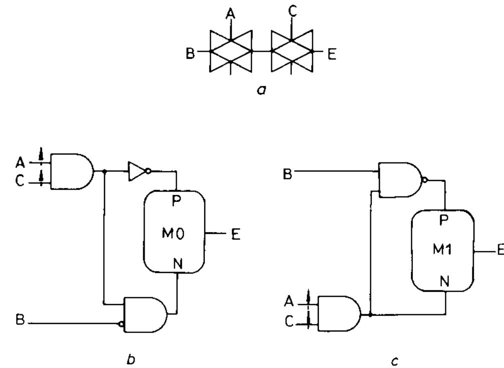


Fig. 8 *Transmission gates connected in series and their My-box representations*

a Logic diagram
b M0-box representation
c M1-box representation

Fig. 8*a* is a circuit of transmission gates connected in series. Similarly to a single transmission gate, either an 'M0-box' or an 'M1-box' can be used to construct the equivalent circuit as shown in Figs. 8*b* and *c*, except that two stuck-at-1 faults at nodes *A* and *C* represent the original stuck-on faults.

For a general circuit connected with transmission gates as shown in Fig. 9*a*, which is a four input multiplexer, the gate-level equivalent circuits of Figs. 9*b* or *c*, depending on whether an 'M0-box' or 'M1-box' is used, can be used to represent the circuit.

It is to be mentioned that, in all the above representing circuits, additional NOT gates were used.

5 Conclusions

A logic model, My-box, which can represent the line faults as well as transistor faults of CMOS circuit has been proposed. It has been shown that nonbridge types of CMOS logic circuits can be transformed into the gate-level equivalent circuits using this logic model incorporating the conventional AND, OR and NOT gates. A procedure has also been described to transform the CMOS transistor circuit to the gate-level equivalent circuit. All the faults in the transistor-level circuits have been shown to be transformable into the stuck-at-1 and stuck-at-0 faults in the gate-level equivalent circuits. This makes the test generation very simple since conventional test generation algorithms can be directly applied to transformed circuits with only minor modification. A fault-collapsing procedure has also been described to obtain the RSPF for transformed circuits and this significantly reduces the number of faults which testing is needed. Besides, My-box has been shown to represent the function and faulty behaviour of transmission gate circuits.

6 References

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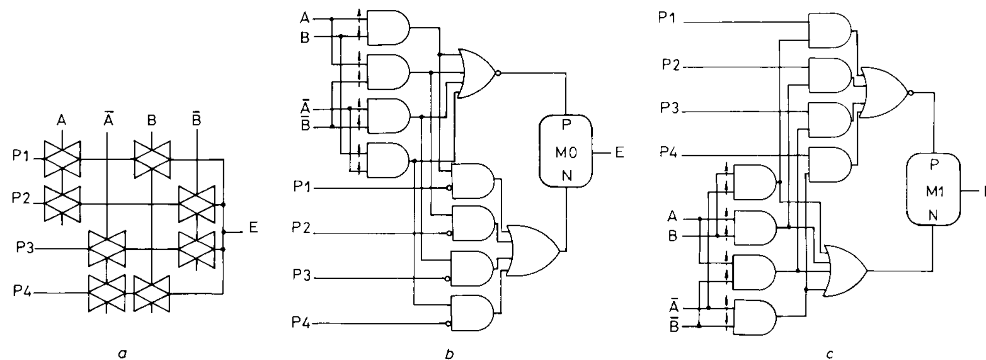

Fig. 9 *Logic diagram and My-box representation for a four-input multiplexer*
a Logic diagram *b* M0-box representation for the wire-AND operation *c* M1-box representation for the wire-OR operation

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Erratum

ADIBI, A., and ESHRAGHIAN, K.: 'Generalised model for MESFET photodetectors', *IEE Proc. G, Circuits, Devices and Systems*, 1989, **136**, (6), pp. 337–343

In the above paper, the following correction should be made:

Section 5 should read:

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