國立交通大學

電機學院　電子與光電學程

碩士論文

應用於液晶顯示器背光之發光二極體驅動器具有動態參考電壓追蹤

LED Driver with an Adaptive Reference Tracking Voltage Technique for the Backlight of LCD Display

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中 華 民 國 九 十 九 年 三 月

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摘　要

由於發光二極體廣泛的被應用於各種產品，最近幾年 PDA、行動電話、數位相機、NB 等可攜式電子產品的液晶顯示器大多改用彩色面板。液晶顯示器本身屬於非主動性發光元件，必需利用背光照明模組照明才能夠讀取面板的影像。

從目前趨勢看來，LED 有充分的理由取代現有冷陰極燈管（CCFL）的地位，由於 LED 背光源符合環保、輕薄、省電與色彩飽和度佳等優勢，特別是在 NB 面板方面，與傳統的 CCFL 背光源比較，LED 背光源 NB 面板厚度約為 CCFL 背光源 NB 面板厚度的 1/2，節能方面，LED 背光源 NB 面板更可較 CCFL 背光源 NB 面板節省約 20%～30%之電力.

本篇論文中提出應用於發光二極體驅動電路之電流控制式直流-直流升壓電源轉換電路設計，其輸入電壓為 5V，而輸出電壓為 35V。其中回授控制電路以脈波寬度調變之方式實現，並根據發光二極體順向電壓改變的回授機制。本論文之設計使用 TSMC 0.25um BCD 5V/40V 2P3M CMOS 製程技術進行模擬與製作。

LED Driver with an Adaptive Reference Tracking Voltage Technique for the Backlight of LCD Display

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ABSTRACT

In recent year, LED is extensive and is applied to various products, such as PDA, mobile phone, several cameras, NB, etc. Modern display can mostly use the colored panel instead of type liquid crystal display of electronic product, since liquid crystal display is non-self-luminous component. It must utilize backlight module of lighting to read image of the panel.

By the look of trend at present, LED has had sufficient reasons to replace the status of the existing cold cathode fluorescent lamp (CCFL). Since LED backlight source has some advantages, it accords environmental protection, light and thin, energy saving and high color saturation. Especially in NB panel, compared with traditional CCFL backlight source, the thickness of LED backlight source of NB panel is about 1/2 of CCFL backlight source in NB panels. In an aspect of energy saving, it can save about 20%- 30% of power consumption.

This thesis presents a current mode DC-DC boost converter for LED applications with 5V input voltage and 35V output voltage. The boost voltage regulator uses a pulse width modulation (PWM) with a dynamic resistor and a reference tracking circuit according to the variation of forward voltage of LEDs. The LED driver circuit was simulated and fabricated by TSMC 0.25um BCD 40V process.

誌　謝

經過多年的訓練學習，終於完成學生的碩士論文，這段期間，要感謝許多人的教導與指引，讓學生在專業技術領域與個人工作發展上皆有所成長。首先要向我的指導教授 陳科宏博士致上萬分的謝意，也感謝全體實驗室同學給予的關懷照應與幫助。

最後，我特別要感謝我美麗女友禮雲，在這段時間的包容及付出，感謝他所給予的關懷，還有一直支持我的家人以及我所有的好朋友，讓我能順利的完成學業。

魏永昇

Contents

Figure Captions

Table Captions

Chapter 1
Introduction

1.1 Background

In the past, cold cathode fluorescent lamp (CCFL) was the most common backlight module for liquid crystal displays (LCDs). However, the drawbacks of CCFL include a low color gamut and high power consumption. Due to recent improvements in the light emitting diode (LED) process, LEDs are now common in backlight modules. This is because the LED backlight module has a better color gamut and longer lifetime than a CCFL backlight module [1] [2].

Light illumination is generally related to the amount of driving current. Thus, the method of using forward voltage to control the driving current is unreliable when environment temperature and usage time change. Furthermore, LED forward voltage often fluctuates due to the different process variations and I-V curves of LEDs from different manufactures. An LED backlight module can manually select a similar LED forward voltage, but the cost is too high. Therefore, using an equal forward voltage to change LED brightness is not effective for ensuring high quality images for LCD TVs. On the other hand, the constant driving current technique is a suitable method to drive LEDs strings and uniformly control the brightness of an LED lighting system. Using a current sink regulator to maintain LED's luminous intensity and chromaticity (color) is a better controlling method.

White or RGB LEDs have the benefit of being energy-efficient. They are cost-effective choices for the next generation of LCD backlight. The system scheme is shown in Fig. 1. There are four blocks: LED driver, RGB LEDs backlight module, color controller and color sensor.

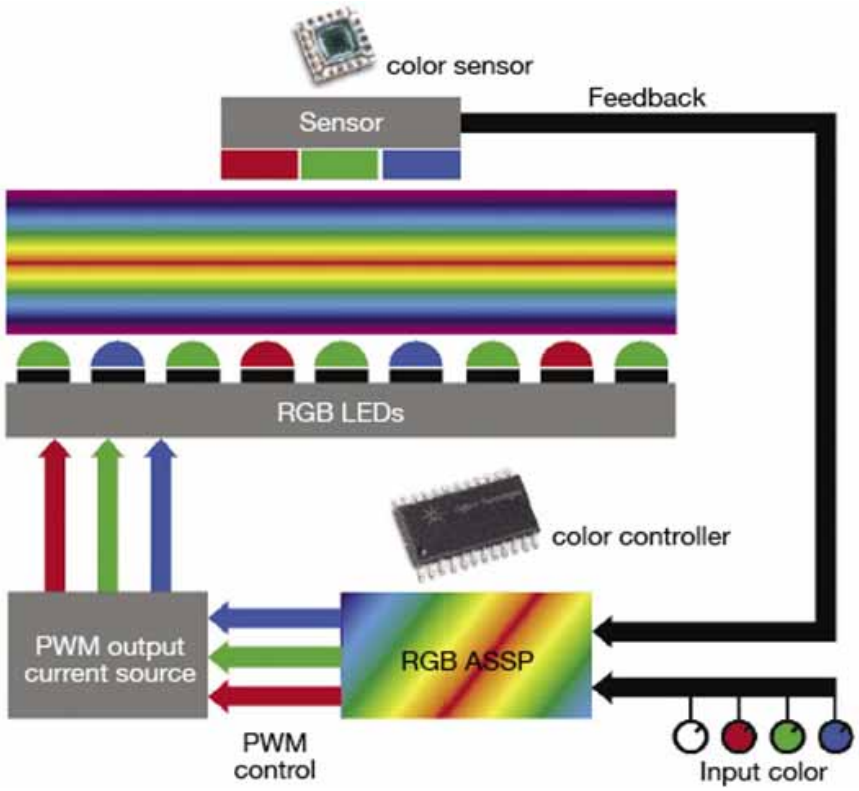


Fig. 1. LED backlight driver block diagram in LCD display

1.2 The Basic Concepts of Current Regulators

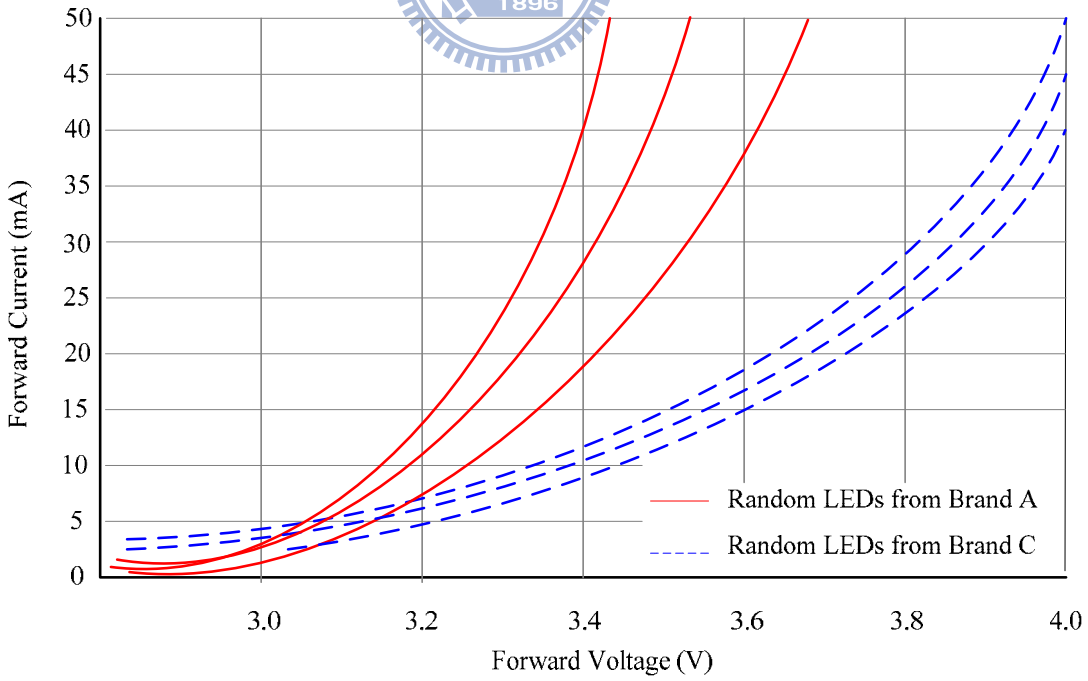


Fig. 2. Forward Current Versus Forward Voltage

LED forward voltage fluctuates due to the process variation and the I-V curves of LEDs from different manufactures are shown in Fig. 2 [3]. LEDs can be manufactured with smaller mismatch, but only at an increased cost. However, the forward voltage also varies according to temperature and time. To obtain high-quality images for LCD TVs, it is impossible to drive forward voltage by dimming the LEDs to change the backlight brightness. The brightness of LEDs is directly related to their current. A higher driving current produces greater brightness. The relative luminous intensity versus forward current of LED is shown in Fig. 3. As a result, using the current to dim LEDs can prevent the forward voltage variation and increase the brightness uniformity of LED backlighting to obtain high-quality images on an LCD TV.

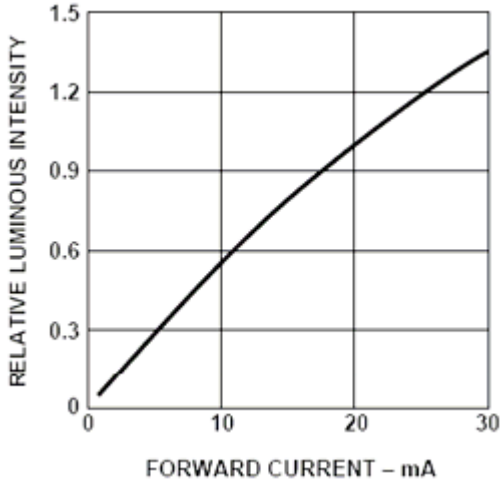


Fig. 3. Relative luminous intensity versus forward current of LED

When using white LEDs for display backlighting applications, why do we drive them use constant current [4]?

1. To avoid violating the Absolute Maximum Current Rating and compromising their liability.
2. To produce matched brightness intensity and chromaticity from each LED.

The most common method for driving LED current is to use the constant-current source to regulate LEDs.

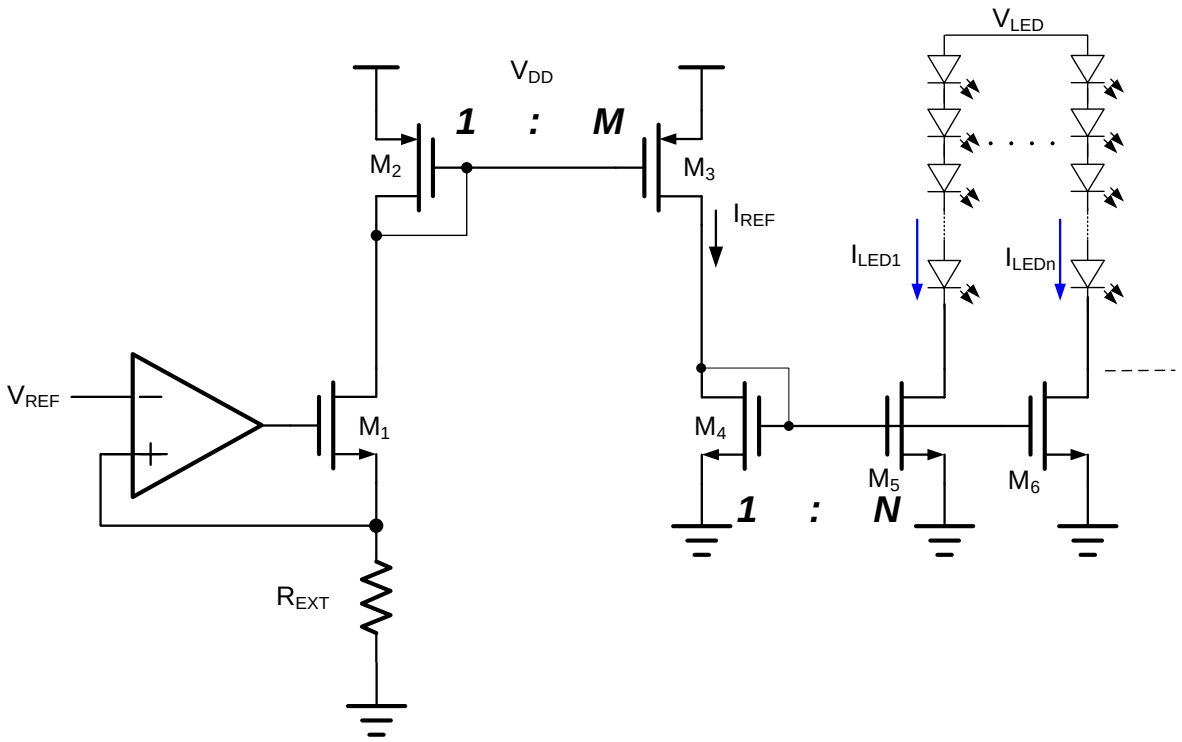


Fig. 4. A simplified diagram for LED driver.

Fig. 4 shows a simple current regulator design for LED strings. This circuit includes an operational amplifier, a reference voltage, V_{REF}, and the external resistor, R_{EXT}. The voltage-to-current converter generates the reference current I_{REF} by an external resistance R_{EXT} and a precise internal reference voltage V_{REF} through the current mirror pair (M_2 and M_3). X uses the constant-current source to regulate LED strings [5] [6]. The constant-current source eliminates the LED current changes caused by variations in forward voltage. The constant-current source produces constant LED brightness and uniform strings. This configuration makes it possible to connect LEDs in series and parallel to ensure an identical current in each LED. As a result, the LED current can be expressed as Eq. (1).

$$I_{LEDn} = \frac{V_{REF}}{R_{-EXT}} \times M \times N \tag{1}$$

1.3 Classifications of LED Driver

The basic power supply circuits of an LED driver can be classified into three kinds of regulator: switch regulators, charge pumps, and linear regulators. We will make a comparison for why we choose boost dc-dc converter as the LED driver voltage regulator. Factors to consider when choosing a voltage regulator include low quiescent current consumption, low noise, high conversion efficiency, low cost, and more.

1.3.1 Linear Regulator

The basic architecture of a linear regulator includes a power switch, which is an NMOSFET transistor to supply the load current; a voltage reference set to produce 1.25V and an operational amplifier (op-amp) to control the power switch, as shown in Fig. 5. The op-amp tries to keep the voltage at the output equal to the voltage at the adjust (ADJ) pin minus the reference voltage.

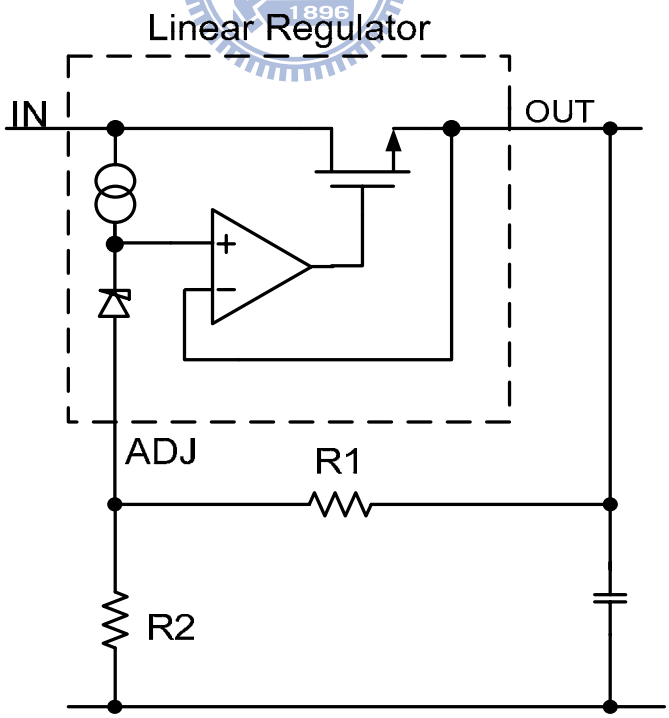


Fig. 5. Linear Regulator

Because the control circuit of a linear regulator is compact and simple, it allows a smaller chip than other regulators. Moreover, an application circuit that does not use an inductor to transfer the energy not only reduces the PCB space, but also reduces costs. However, a linear regulator only can perform buck regulation because it lacks a storage element. A capacitor on the output terminal helps with stability. Equation (2) shows the output voltage:

$$V_{OUT} = 1.25 \times \frac{1 + R_2}{R_1} + I_{ADJ} \times R_2 \tag{2}$$

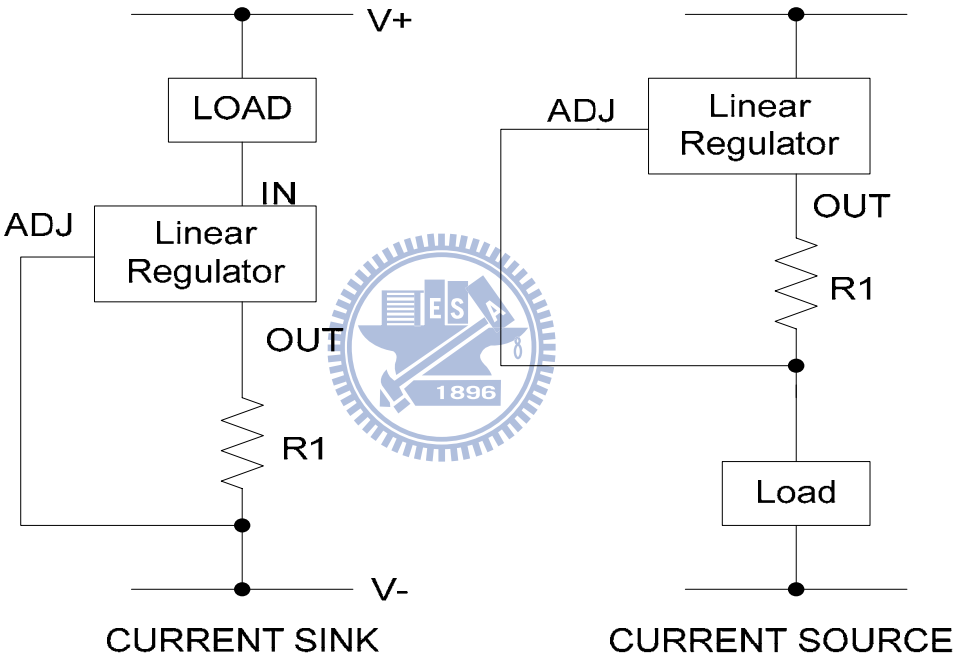


Fig. 6. Voltage Regulator as a Current Source and Current sink

The voltage regulator as a current source and the other as a current sink is shown in Fig. 6. The linear regulator begins to regulate the current when there is +1.25V difference between the OUT and ADJ pins. A current flowing through R_1 produces a voltage drop. When the voltage drop across R_1 reaches 1.25V, the linear regulator begins to regulate the current, which could be expressed as Eq. (3)

$$I = \frac{1.25}{R_1} \tag{3}$$

1.3.2 Charge Pump

The basic structure of a two-phase charge pump regulator is shown in Fig. 7 [8] [9]. This design consists of capacitors (C_1 C_2) and switches (SW_1 SW_2 SW_3 SW_4). During the first interval of switching period, clock *CK1* is high and *CK2* is low. The *SW1* and *SW2* switches turn on and the *SW3* and *SW4* switches turn off. The capacitor, *C1* is being charged to the supply voltage *VIN*. In the second interval of switching period, clock *CK1* is low and *CK2* is high. The *SW1* and *SW2* switches turn off and the *SW3* and *SW4* switches turn on. The capacitor, *C1* is being charged to twice the supply voltage *VIN*.

The most common method of regulating the output voltage is to use a control circuit and an error amplifier. The error amplifier senses variations in output voltage, and the control circuit controls switches *SW1~SW4* based on the error amplifier signal, stabilizing the output voltage.

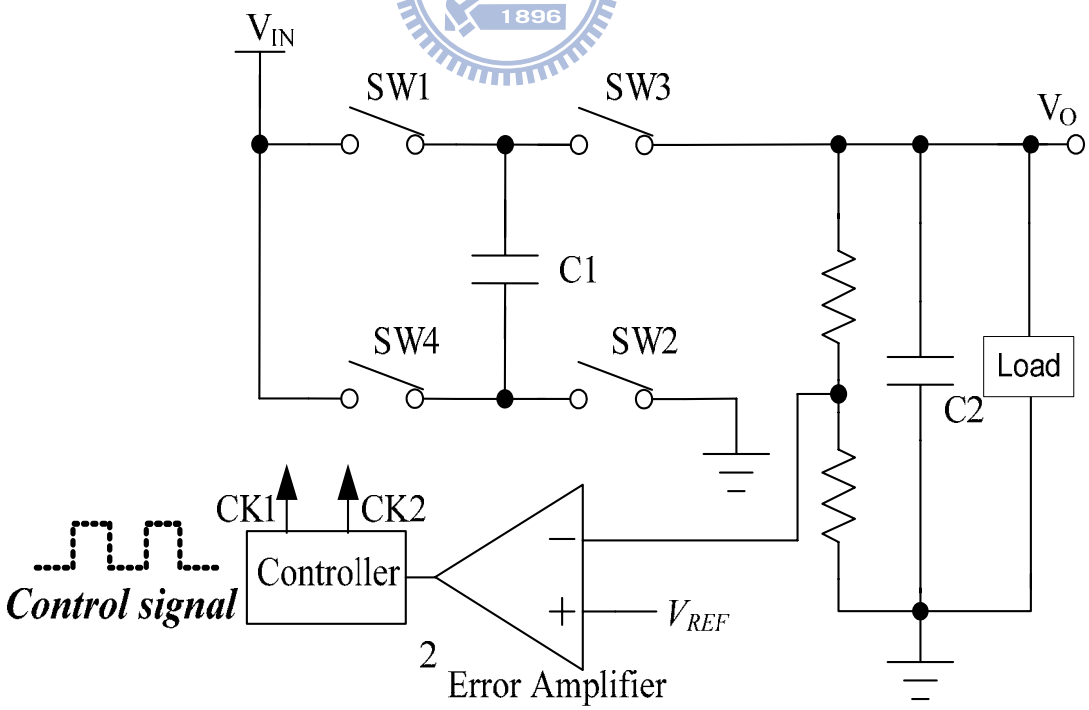


Fig. 7. The basic structure of charge pump

The complex of charge pump is between linear regulator and switching regulator. The load capacity is weakest at this point because the load ability depends on the output capacitor

C_2. As a result, a larger output capacitor leads to greater load ability. This design achieves an efficiency exceeding 90%, but only when output voltage is a multiple of the input voltage.

1.3.3 Switching Regulator

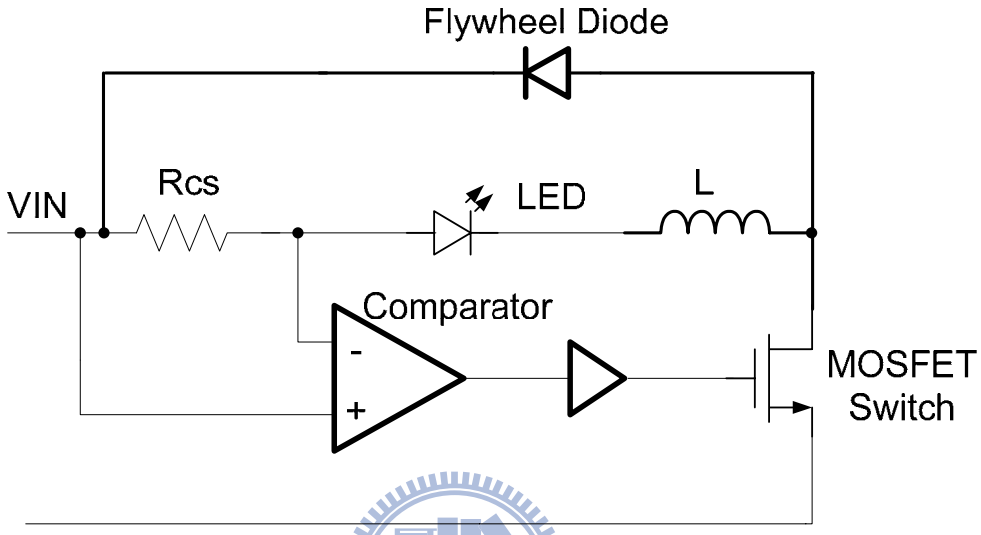


Fig. 8. The Simple Buck LED driver

As shown in Fig. 8 [7] [10], the simple buck LED driver. It includes a power MOSFET that switches the supply voltage across an inductor and LED load connected in series. The inductor stores energy when the power MOSFET is on. This energy then provides current for the LED when the MOSFET is off. A diode across the LED and inductor circuit provides a return path for the current during the MOSFET off time.

The hysteretic buck control circuit as shown in Fig. 9. This design uses a comparator to drive the MOSFET switch. The comparator input is a high side current sense circuit that monitors the voltage across a resistor in the positive power feed to the LED load. The MOSFET turns on when the current level falls below a minimum reference voltage. The MOSFET turns off when the current exceeds a maximum reference voltage. This is shown in Fig. 10. By this method, the average LED current remains constant, regardless of changes in

the supply voltage or LED forward voltage. The range of hysteretic voltage exhibits a tradeoff current accurate and noise margin, with typical values ranging from 50mv to 250mv.

A suitable resistor value determines the current level. This resistor value is given by:

$$R_{sensee} = \frac{1}{2}\frac{V_{CS(high)} + V_{CS(LOW)}}{I_{LED}} \quad (4)$$

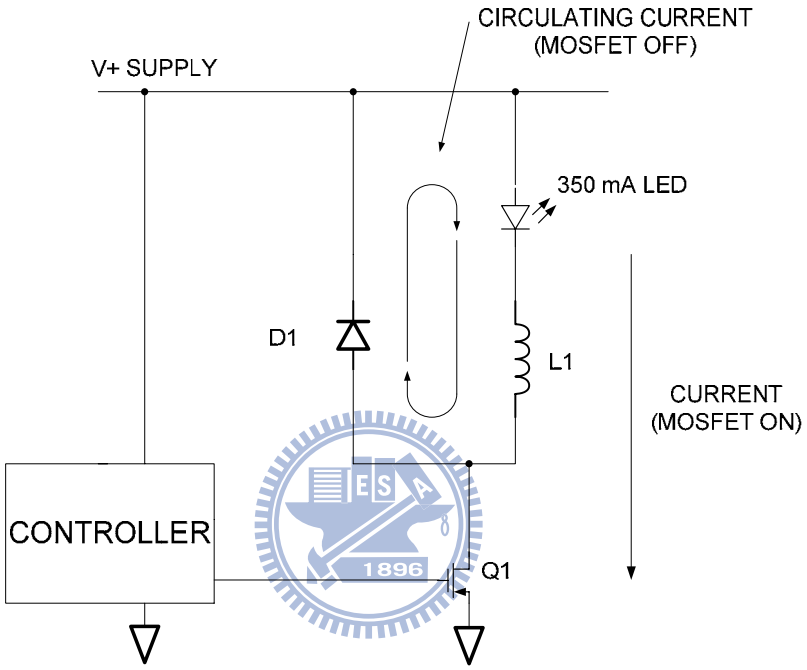


Fig. 9. Hysteretic Buck Control LED driver

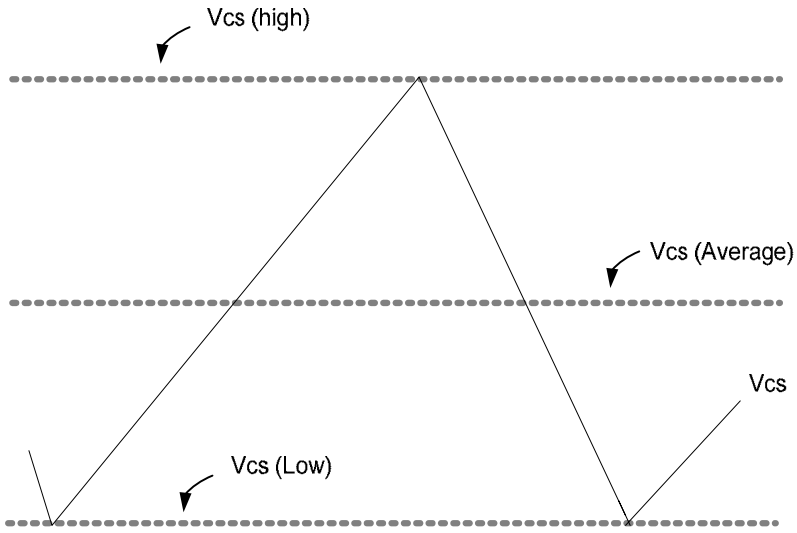


Fig.10. Current Sense Voltage

1.3.4 Comparison

The three kinds of voltage regulators described above have their own advantages and disadvantages. Selecting the best voltage regulator for the power supply of an LED driver depends on the electronic characteristics and specifications. The comparison of different type voltage regulator is listed in TABLE I [11]. An LED driver needs a wider output range for more LEDs in series and a stronger loading capacity for more strings connect in parallel. Therefore, the proposed design chooses the boost type switching regulator as the voltage regulator to enable high brightness LED backlight applications.

Table Ⅰ. Comparisons of Different Type Regulators.

Characteristics	**Linear Regulator**	**Charge Pump**	**Switching Regulator**
Regulation Type	Buck	Buck/boost	Buck/boost/buck-boost
Chip Area	Minimum	Medium	Maximum
Efficiency	Minimum	Medium	Maximum
EMI/Noise	Minimum	Medium	Maximum
Load ability	Medium	Minimum	Maximum
Complexity	Simplest	Medium	Complicated
Cost	Low	Medium	High

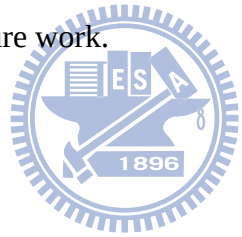
1.4 Motivation

Since the growing LED backlight application, the research topics is focus on the voltage regulator. Fig. 1 show the high brightness LED driver proposed in this thesis. The LED backlighting in LCD TV applications requires a boost type switching regulator to drive the LEDs in series and parallel. The constant current-driven LED backlight module is composed

of two parts as shown in Fig. 1. The boost DC/DC converter offers a sufficiently high voltage to overcome the LED forward voltage, and offers a constant voltage level whether the digital PWM dimming is turned on or off. On the other hand, a current sink circuit can ensure a constant current flow through each LED string without being affected by variations in the LED's forward voltage.

1.5 Thesis Organization

This thesis is organized as follows. Chapter 2 introduces the basic current mode DC-DC converter. Chapter 3 describes the design and implementation for proposed LED driver. Chapter 4 provides the overall circuit structure and simulation results based on the proposed technique, along with simulation results simulated by Hspice. Finally, Chapter 5 presents conclusions and directions for future work.

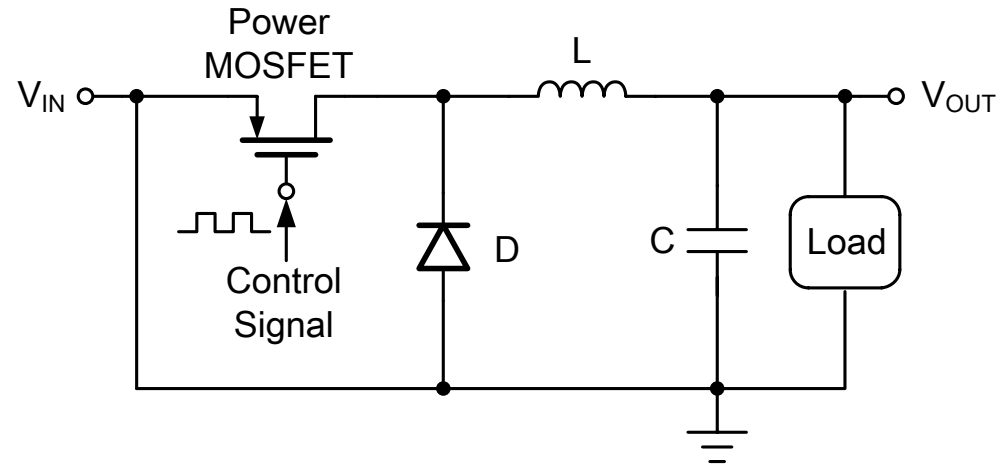


Chapter 2
Basic Concepts of DC-DC Converter

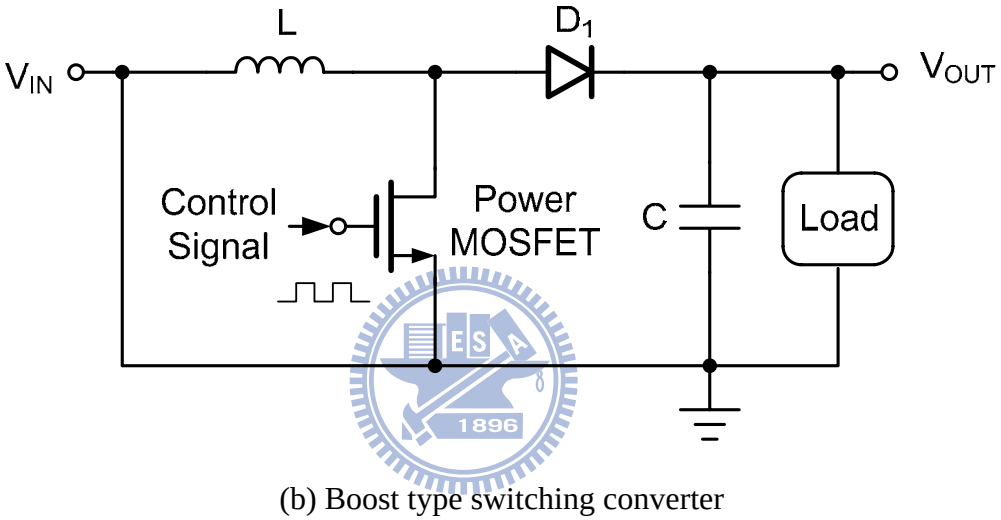
This chapter presents the basic concepts of dc-dc regulators. Section 2.1 introduces the three kinds of DC-DC converter topologies, including the conversion ratio. Section 2.2 compares current-mode control and voltage-mode control. Section 2.3 analyzes the current mode boost converter. Finally, Section 2.4 presents the characteristics and performance specifications of the dc-dc converter.

2.1 Topologies of Basic Converter

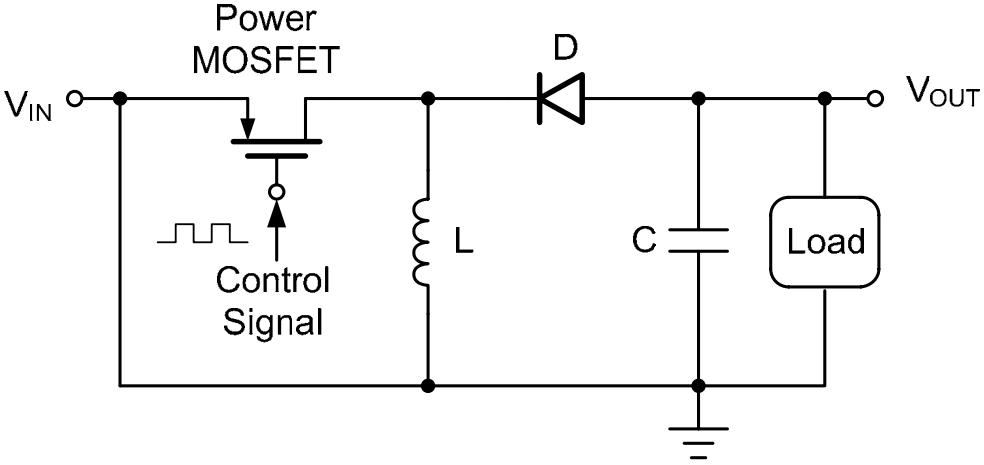
This section introduces three converter topologies of switching regulators, including the buck, boost, and buck-boost converters shown in Fig. 5 [12]. The fundamental operations of three switching regulators are described as following expressions. Fig. 11(a) shows the basic structure of a buck switching converter. When the power MOS is turned on, the diode D is turned off and the power supply supplies the load current. When the power MOS is turned off, the diode D is turned on and the inductor current supplies the load current. The boost switching converter is shown in Fig. 11(b). When the power MOS is turned on, the diode D is reverse biased and output capacitor C supplies the load current. When the power MOS is turned off, the diode D is forward biased. Then the inductor current supplies the load current and recharges the capacitor. Buck-Boost switching converter is illustrated in Fig. 11(c). When the power MOS is turned on, the reverse biased diode disconnects the power supply and output voltage and the output capacitor supplies the load current. When the switch is turned off, the diode is forward biased and the inductor current supplies the load current. Table Ⅱ summarizes the characteristic of these converter topologies of switching converter, where the duty ratio is the power MOSFET on time of one switching cycle.



(a) Buck type switching converter



(b) Boost type switching converter



(c) Buck-Boost type switching converter

Fig. 11. The basic structure of Switching Converter

Table Ⅱ. Comparisons of converter topologies

Topology	Buck converter	Boost converter	Buck-Boost converter
Conversion Ratio	$\frac{V_{OUT}}{V_{IN}} = D$	$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$	$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D}$
Conversion Type	Only Buck	Only Boost	D>0.5 doing Boost D<0.5 doing Buck

2.2 Comparison between Current-Mode and Voltage-Mode Control

The voltage-mode switching converter has only one voltage feedback path. The clock signal is used to constant switching frequency. The pulse-width modulation is performed by comparing the output signal of the error amplifier with the constant sawtooth waveform.

The voltage-mode control offers some advantages [13]:

- It is easier to design and analyze a single feedback loop.
- The large amplitude of the sawtooth waveform provides a good noise margin.

However, the voltage-mode control also has some disadvantages:

- Any change in line voltage or load current must have an affects on the output voltage. Then it is sensed and corrected by feedback loop. The response is become slowly.
- The inductor and capacitor of the output filter form two poles. Therefore, it is necessary to add one dominant pole or zero to compensate this system.
- The loop gain is varies with the line voltage. This makes further complicated compensation.

In the current-mode control, there is an inner current feedback path and an outer voltage feedback path. The sawtooth waveform is replaced with a signal derived from output inductor current.

The current-mode control offers some advantages::

- The current-mode system is faster response for change of line voltage. Since the rising slope of inductor current is proportional to V_i-V_o, the waveform is responded directly to line voltage changes.
- The inductor and capacitor of the power stage offer only one low frequency pole. Compensation is easier using a type II compensator than the voltage-mode.
- Current sensing is already done by the inner current feedback loop. The current limiting protection could be done by restricting the output voltage of compensator pulse by pulse.
- Current sharing of multi-output DC-DC converter is easier to be controlled.

However, current-mode control also has some disadvantages:

- It is more difficult to design and analyze two feedback paths.
- Sub harmonic oscillation occurs when duty is above 50%, necessitating a slope compensation function.
- The signal from current feedback path may be affected by the noise of power stage.

2.3 Analysis of Current-Mode Boost Converter

2.3.1 Continuous condition Mode (CCM)

The boost converter is capable of providing an output voltage that is greater than the input voltage. In Fig. 12 [12], shows the circuit of a boost converter. During the continuous conduction mode (CCM) the inductor current conducts continuously and the minimum current is always larger than zero. In Fig. 13, shows the waveforms of a boost converter in CCM operation. Therefore, there are only two subintervals for switching converter in CCM operation. The two equivalent circuits of the first and second subintervals are as shown in Fig. 14.

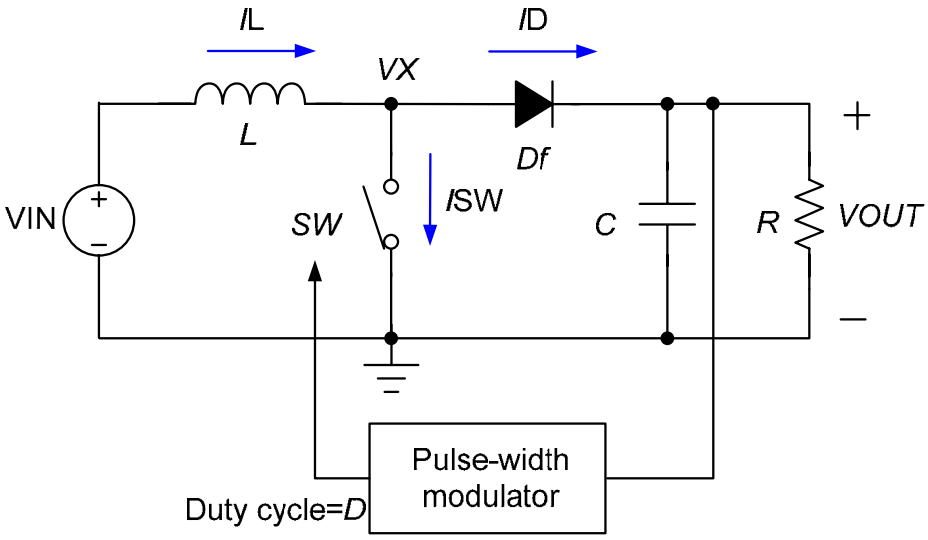


Fig. 12. The boost converter with pulse width modulator

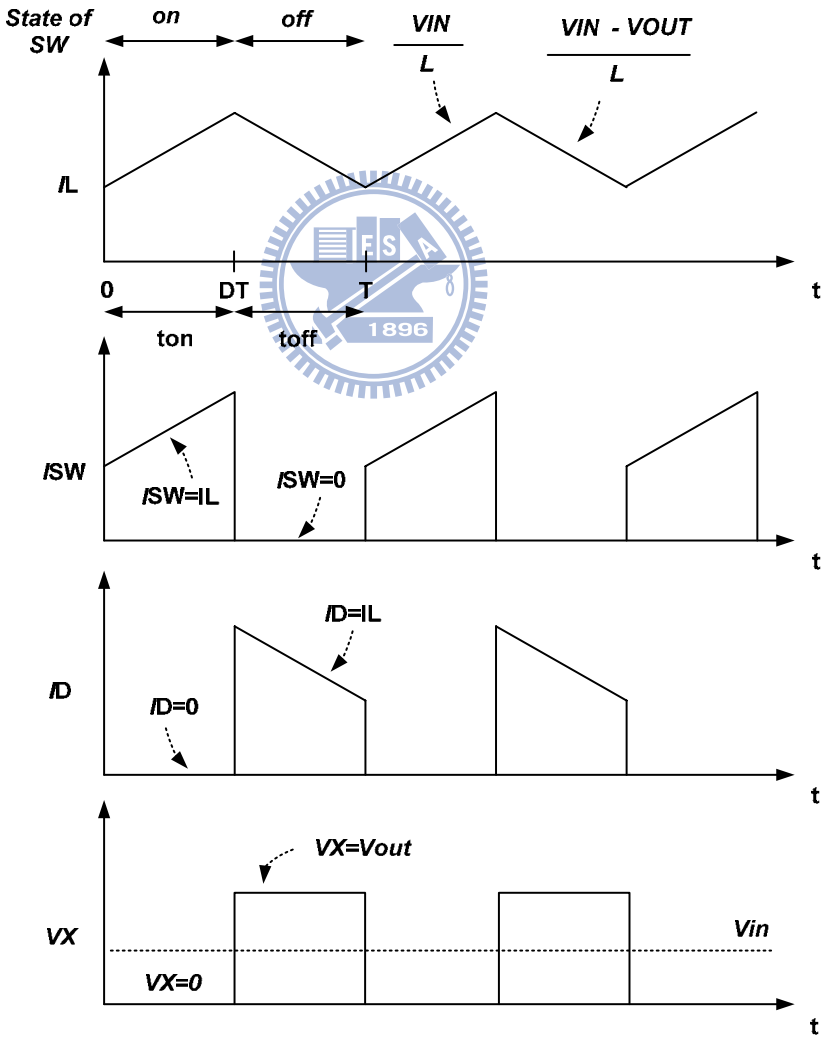


Fig. 13. Waveforms of a Boost Converter in CCM operation

Fig. 14(a) shows the first subinterval operation in CCM. When converter operating in first subinterval the low side NMOS turned on and the inductor current increased. During this subinterval the inductor voltage and capacitor current can be derived as Eq. (5) and (6).

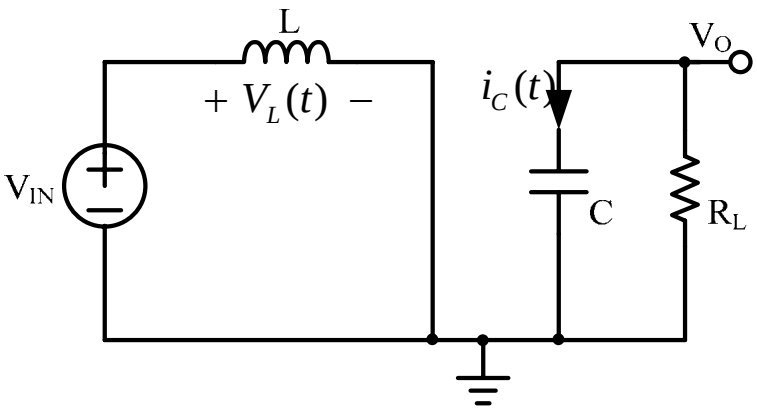
$$v_L(t) = L\frac{di_L}{dt} = V_{in} \tag{5}$$

$$i_C(t) = C\frac{dv_C}{dt} = \frac{-V_{out}}{R} \tag{6}$$

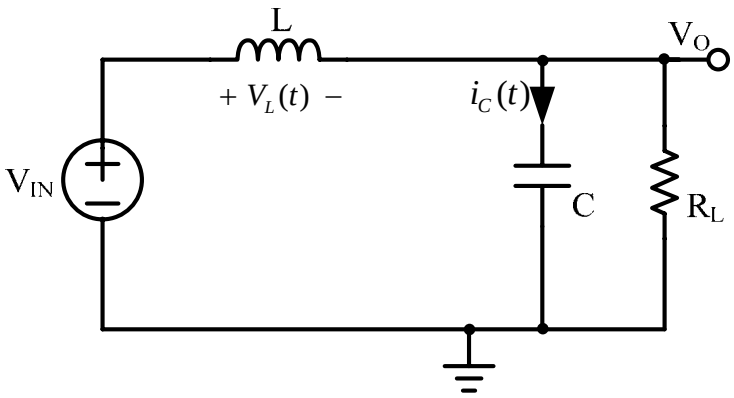
Fig. 14(b) illustrates the second subinterval operation in CCM. When the converter operates in the second subinterval the high side PMOS turned on and inductor current delivering to output. During this subinterval the inductor voltage and capacitor current can be derived as Eq. (7) and (8).

$$v_L(t) = L\frac{di_L}{dt} = V_{in} - V_{out} \tag{7}$$

$$i_C(t) = C\frac{dv_C}{dt} = i_L - \frac{V_{out}}{R} \tag{8}$$



(a)



(b)

Fig. 14. (a) Equivalent circuit of the first subinterval in CCM. (b) Equivalent circuit of the second subinterval in CCM

Equation (9) is based on the inductor voltage second balance. The output voltage increases when D rises. In the ideal case, the conversion ratio tends to infinity when D is toward to 1.

$$V_{in}\cdot DT_s+\left(V_{in}-V_{out}\right)\cdot D'T_s=0,\quad \frac{V_{out}}{V_{in}}=\frac{1}{D'}=\frac{1}{1-D} \tag{9}$$

The steady-state current in the switching converter is based on the capacitor charge balance, as Eq. (10) shows.

$$\left(\frac{-V_{out}}{R}\right)\cdot DT_S+\left(i_L-\frac{V_{out}}{R}\right)\left(1-D\right)\cdot T_S=0\ ,\quad i_L=\frac{V_{out}}{D'R}=\frac{V_{in}}{D'^2R} \tag{10}$$

The inductor current in Eq. (10) is equal to the input current of converter, and its magnitude is greater than the load current. Combining Eq. (5) and (6) shows that the inductor current ripple and output voltage ripple can be calculated as Eq. (11) and (12), respectively:

$$\Delta i_L=\frac{V_{in}}{2L}\cdot DT_S \tag{11}$$

$$\Delta v=\frac{V}{2RC}\cdot DT_S \tag{12}$$

2.3.2 Discontinuous Condition Mode (DCM)

When the output average current is smaller than the half of the inductor peak-to-peak ripple current, the voltage regulator is operated in DCM as shown in Fig. 15 [12]. Because the inductor current conducts discontinuously and the minimum current equals zero during this mode, this situation usually occurs under light load condition. This is why the boost converter has three subintervals. The first and the second subinterval structures are the same as depicted in Fig. 14 (a) and the Fig. 14 (b) respectively. The third subinterval for the boost converter in DCM is shown in Fig. 16.

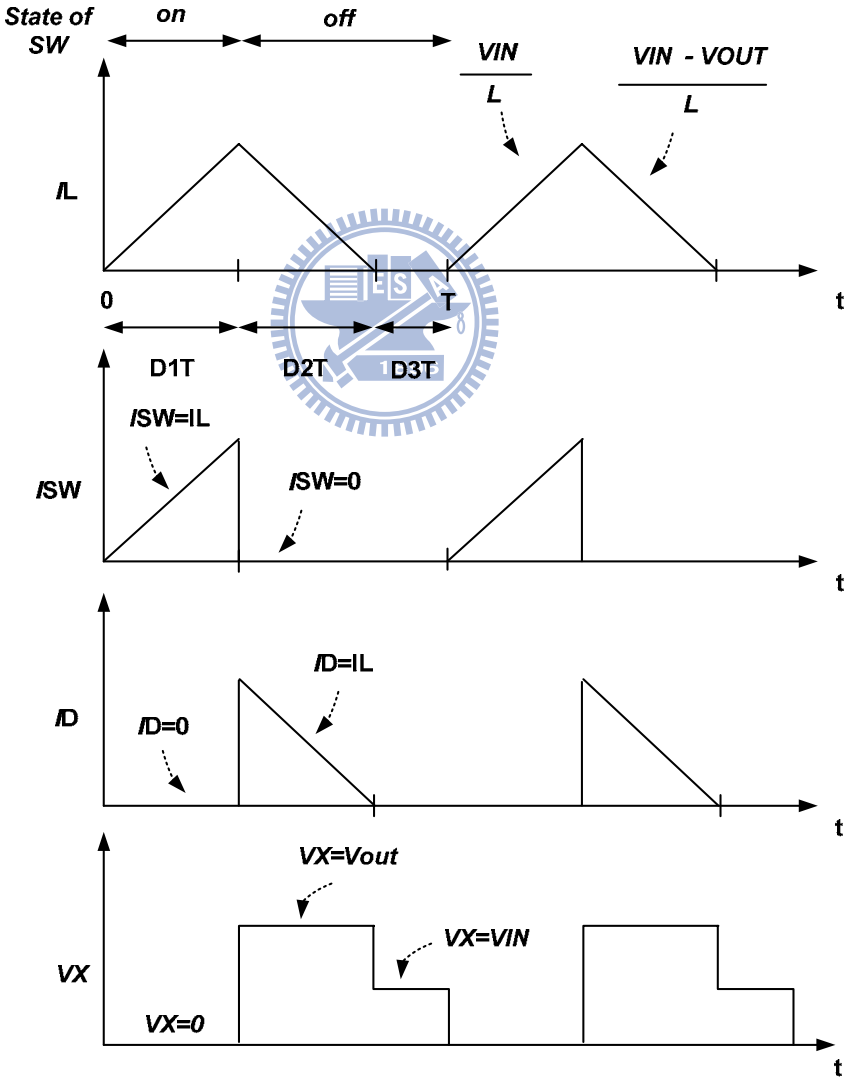


Fig. 15. Waveforms of a Boost Converter in DCM operation

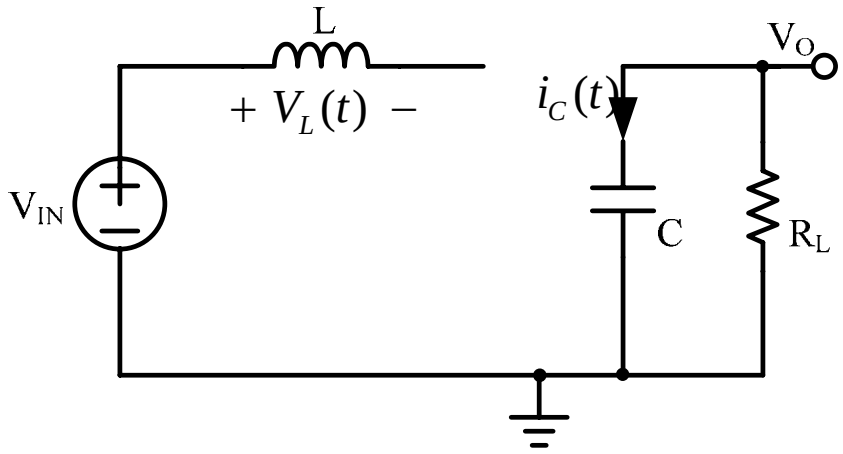


Fig. 16. Equivalent circuit of the third subinterval in DCM

The inductor voltage and capacitor current during the first subinterval are given by:

$$v_L(t) = L\frac{di_L}{dt} = V_{in} \tag{13}$$

$$i_C(t) = C\frac{dv_C}{dt} = \frac{-V_{out}}{R} \tag{14}$$

The inductor voltage and capacitor current during the second subinterval are given by

$$v_L(t) = L\frac{di_L}{dt} = V_{in} - V_{out} \tag{15}$$

$$i_C(t) = C\frac{dv_C}{dt} = i_L - \frac{V_{out}}{R} \tag{16}$$

The inductor voltage and capacitor current during the third subinterval are given by

$$v_L = 0 \tag{17}$$

$$i_C = -\frac{V_{out}}{R},\ i_L = 0 \tag{18}$$

In the steady-state, Eq. (13) to (18) can be written by the volt second theorem:

$$V_{in}\cdot D_1T_s + (V_{in} - V_{out})\cdot D_2T_s + 0\cdot D_3T_S = 0\ ,\ \frac{V_{out}}{V_{in}} = \frac{D_1 + D_2}{D_2} \tag{19}$$

The output current can be derived as follows:

$$I_{out} = \frac{V}{R} = \frac{1}{T_S} \cdot \left[\frac{1}{2} \left(\frac{V_{in}}{L} D_1 T_S \right) \cdot D_2 T_S \right] = \frac{V_{in} D_1 D_2 T_S}{2L} \quad (20)$$

Let Eq. (19) is equal to Eq. (20), it is possible to derive the expression of output voltage as follows:

$$\frac{V_{out}}{V_{in}} = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2} \text{ , } where\ K = \frac{2 \cdot L}{RT_S} \quad (21)$$

Analyzing Eq. (21) and (9) reveals major differences between CCM and DCM operation. In DCM operation, the voltage conversion ratio depends on the input voltage, duty cycle, power stage inductance, switching frequency, and output load resistance. In CCM operation, however, the voltage conversion ratio depends only on the input voltage and duty cycle.

2.3.3 Operation Theorem of Current Mode Control

The block diagram of the current mode boost converter is shown in Fig. 17 [12]. In this case, the switching converter has two control modes: one is the voltage mode controller, and the other is the current mode controller.

Voltage mode control uses a single voltage feedback loop to regulate the output voltage. The duty cycle of pulse width modulation is produced by comparator output signal of error amplifier compares with a ramp signal of fixed frequency.

The current mode control method uses two control loops, an inner current control loop and an outer loop for voltage control. The block diagram of the current mode boost converter is shown in Fig. 17 [12]. The small duty ratio of the clock signal generates the PWM signal at the start of each switching period. In this state, the power MOSFET MN is turned on and the diode D is tuned off. The inductor current increases follow a raised slope which depends on the input voltage and the value of inductor. An artificial ramp prevents unstable oscillation

when the duty ratio is larger than 0.5. The output signal from the error amplifier is compared with the sum of ramp and sensed inductor current signal. When the sum of the ramp and sensed inductor current signal exceed than the control signal, the output of comparator produce high to reset the SR latch and turn off the power MOSFET MN and connect the diode D as shown in Fig. 18 [12].

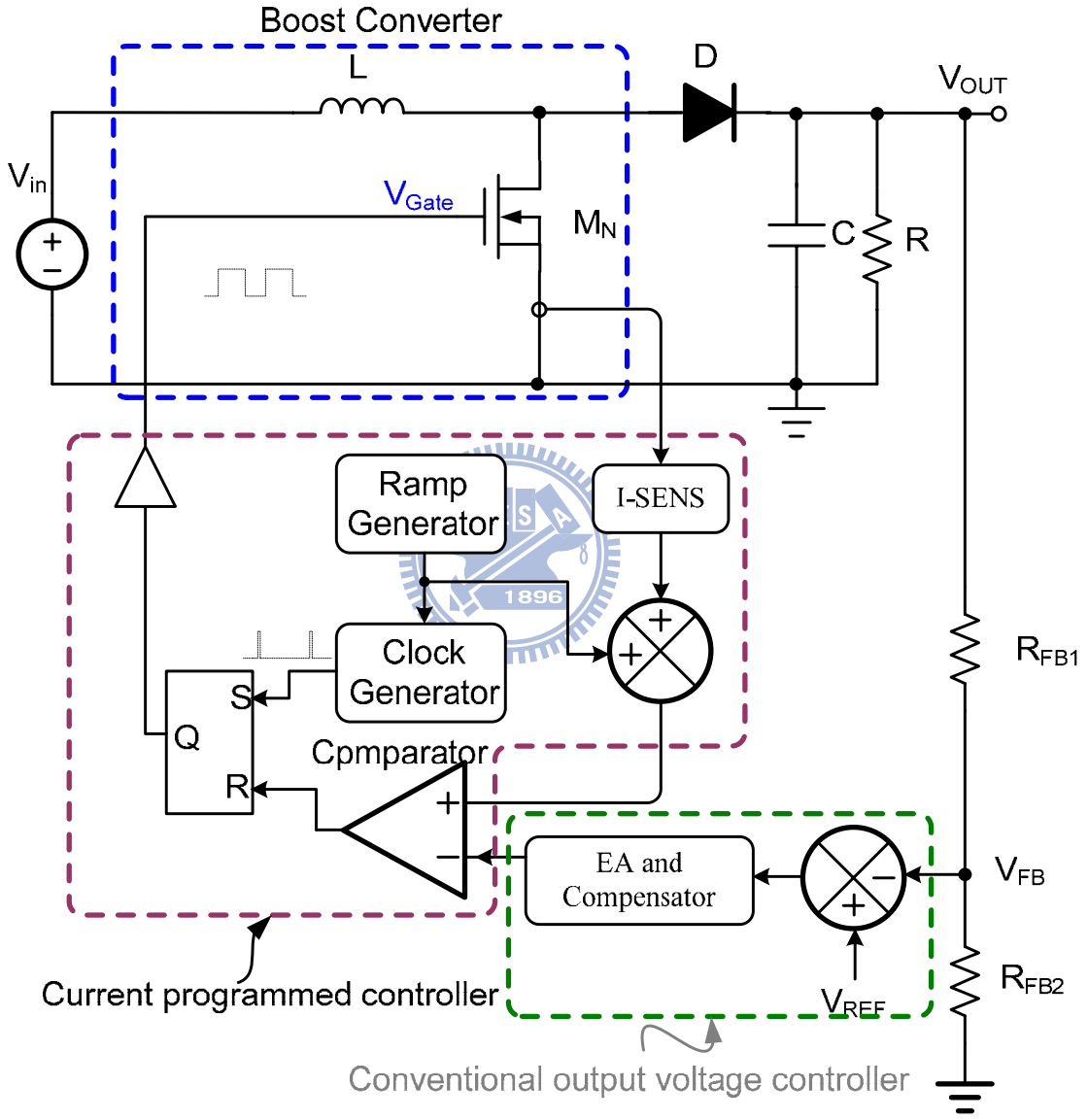


Fig. 17. Block Diagram of current mode boost switching converter

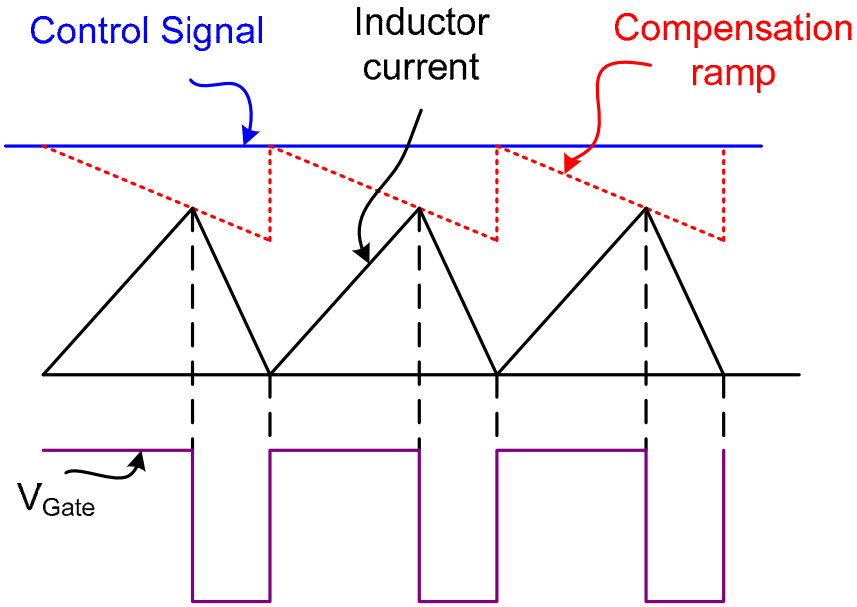


Fig. 18. Inductor current waveform with compensation ramp.

2.3.4 Oscillation when Duty > 50% and Slope Compensation

The current mode controller encounters major instability problems when the duty ratio D is larger than 50%. Fig. 19 depicts the inductor current waveform; a small perturbation in the inductor current down slope is greater than the upslope. These perturbations could be due to noise or other changes in the operating environment.

In the current mode control, the inductor current changes with the rising and falling slopes for boost converter are as:

$$m_1 = \frac{V_{in}}{L}, -m_2 = \frac{V_{in} - V_{out}}{L} \tag{22}$$

Assume that the inductor current is perturbed by an amount ΔI_1 at the beginning of the switching period; the perturbation ΔI_2 for the following period is greater if the duty cycle is greater than 50%. If the duty cycle is smaller than 50%, the successive periods attenuate the perturbation until it disappears. Mathematically, this can be stated as

$$\Delta I_2 = -\Delta I_1\left(\frac{m_2}{m_1}\right) \quad ; \quad \text{For stable condition} \quad \frac{m_2}{m_1} < 1 \qquad (23)$$

Equation (23) shows the stable condition. To maintain a stable operation, the duty cycle of the converter must remain below 0.5.

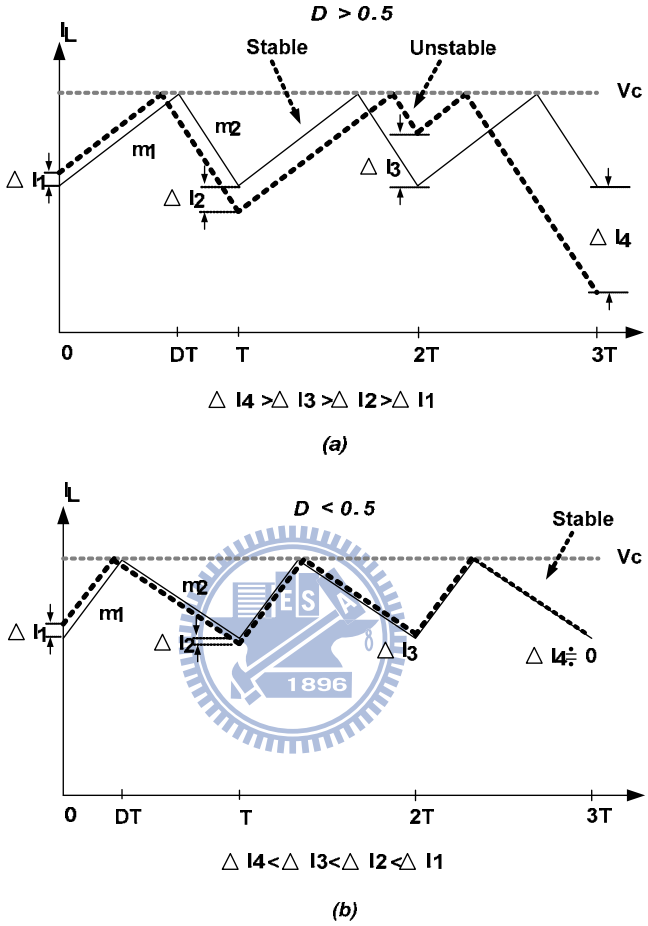


Fig. 19. (a) Waveform of I_L with perturbation ΔI_1 for $D > 0.5$

(b) Waveform of I_L with perturbation ΔI_1 for $D < 0.5$

The artificial ramp generator which prevents unstable oscillation is applied to the switching current sensing loop, as illustrated in Fig. 20 [12][14]. The relation of inductor current and perturbation $\hat{i}_L(0)$ is derived as Eq. (24) and (25).

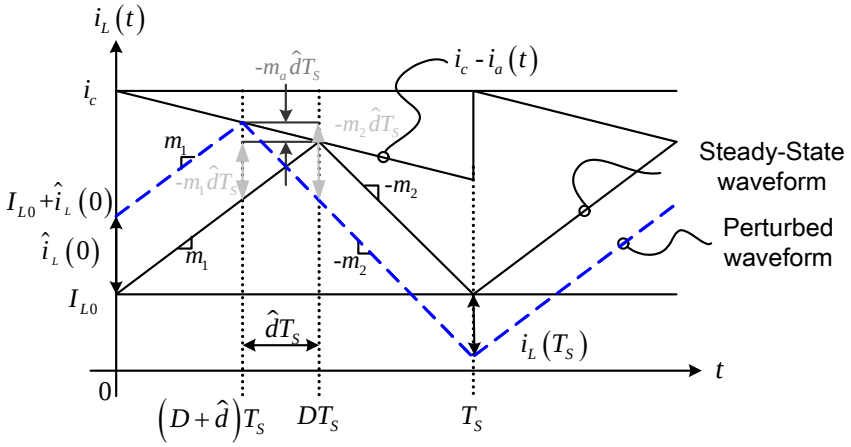


Fig. 20. Inductor Current Waveform with Slope Compensation

$$\hat{i}_L(0) = -m_1\hat{d}T_S - m_a\hat{d}T_S \tag{24}$$

$$\hat{i}_L(T_S) = -m_2\hat{d}T_S + m_a\hat{d}T_S \tag{25}$$

Equation (24) and Eq. (25) then lead to

$$\hat{i}_L(T_S) = -\hat{i}_L(0)\cdot\frac{m_2 - m_a}{m_1 + m_a},\ \hat{i}_L(nT_S) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n \tag{26}$$

Therefore, the slope of the artificial ramp should be larger than the slope of the second subinterval period, as Eq. (23) indicates. This make sure current-mode controlled DC-DC boost converter stable for all possible duty cycle.

$$m_a = \frac{1}{2}m_2 \tag{27}$$

$$m_a \geq \frac{1}{2}m_2 \tag{28}$$

2.4 Performance Specification

Because more and more electronics applications require switching converters, switching converter performance must be considered. The most important specifications include the high conversion efficiency of switching converter, excellent regulation of load and line regulation, and fast transient response. This section describes some terms and definitions that will make it easier to design or evaluate a switching converter.

2.4.1 Efficiency

Although a switching converter has high conversion efficiency, it wastes power at different load conditions, reducing efficiency. There are many sources of power loss, including switching loss, power MOSFET conduction loss, diode conduction loss, ESRL and ESRC conduction loss, control circuit power consumption, etc. Because the pass of power MOSFET can equal that of a resistor (R_{ON}), it will result in a power loss. This power consumption is also called conduction loss (P_{cond}), and expressed as follows:

$$P_{cond} = I_{rms}^{2} R_{DS(ON)} \tag{29}$$

When the power MOSFET switches on and off, the gate parasitic large capacitor of power MOSFET alternately charges and discharges. This produces a large conversion loss, called switching loss (P_{SW}), which can be expressed as follows:

$$P_{SW} = (C_{GP} + C_{GN}) V_{IN}^{2} F_{SW} \tag{30}$$

The terms C_{GP} and C_{GN} represent the gate parasitic capacitors of the power PMOSFET and power NMOSFET respectively. V_{IN} is represented the input voltage and F_{SW} is represented the switching frequency. The final part is the idle mode, which is the condition in which the converter has no loading. Although there is no load at output, the converter can still regulate the output voltage. This current consumption in the internal controller is called the quiescent current. The system power loss (P_{SYS}) is the product of the quiescent current and input voltage. The ratio of the output power and input power, including the power loss, represents the efficiency of a DC-DC converter, and can be expressed as follows:

$$Efficiency = \frac{P_{out}}{P_{in}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{P_{OUT}}{P_{OUT} + P_{SW} + P_{cond} + P_{SYS}} \times 100\% \tag{31}$$

2.4.2 Load and Line Regulation

Variations in the supply voltage or output load current can affect the operation of the circuit. To keep the regulated voltage and decrease the steady state error when increasing, the supply voltage and load condition of DC-DC converter is very important.

The load regulation is the percentage change of output voltage when the load current changes. Load regulation is

$$\textbf{\textit{Load Regulation}} = \frac{\Delta V_{OUT}}{\Delta I_{LAOD}} \times 100\% \tag{32}$$

Line regulation is a measure of the ability of changes in input power supply to maintain the output voltage. Line regulation is the percentage of change in the output voltage relative to the change in the input line voltage. Line regulation is defined as:

$$\textbf{\textit{Line Regulation}} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 100\% \tag{33}$$

2.4.3 Transient Response

The transient response is one of the most important specifications of switching regulator for the system applications. It is measured by the magnitude of output voltage drop and output voltage settling time when applying the step load is applied to the switching converter. Due to limits in switching regulator bandwidth, the feedback control cannot provide sufficient current in time. Therefore, the output capacitor discharges the energy to support the load current and make an output voltage drop. The switching converter is the concern of key parameter for transient response that is affected by output capacitor, equal series resister of the switching and passive component.

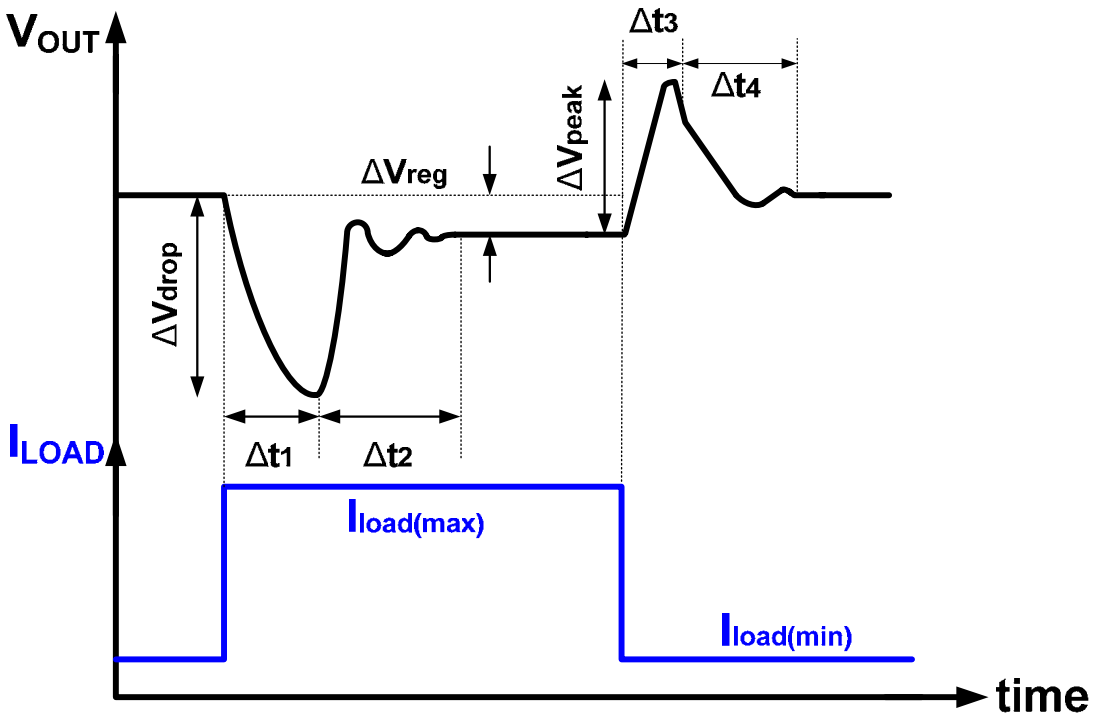


Fig. 21. The output waveform when a dynamic load is applied

Fig. 21 [15] shows the time characteristic of the transient response. At time period Δt_1, the large current flow to the output load forms a switching regulator This is due to limitation in the system bandwidth, which prevent the switching regulator from providing current for the output in time. Therefore the output capacitor discharges the energy to support the load current and make an output voltage drop. As a result, the voltage ΔV_{drop} can be calculated as:

$$\Delta V_{drop} = \frac{I_{LOAD(\max)}}{C_{OUT}} \Delta t_1 + \Delta V_{ESR} \quad ; \quad \Delta V_{ESR} = I_{LOAD(\max)} \times R_{C\_ESR} \tag{34}$$

Δt_1 depends on the bandwidth of the switching converter. Besides, a large output capacitor continues to provide charges to the output load and holds the output voltage steady without a drop.

The timing of Δt_2 depends on the feedback system to turn on the power MOSFET to support the load energy. The output voltage finally settles to its final value in period Δt_2. The

sum of Δt_1 and Δt_2 is called "Recovery Time." The static error, ΔV_{reg} represents the voltage difference between no-load and full load affected by the load regulation. The system loop gain and closed-loop output resistance both affect ΔV_{reg} .

Suddenly removing the load from the output causes the output voltage to increase until the switching regulator turns off the pass element completely. Δt_3 is the system response time. Before the pass element turns off, the excessive current charges the output capacitor. Therefore, the voltage ΔV_{peak} can be calculated as:

$$\Delta V_{peak} = \frac{I_{LOAD(\max)}}{C_{OUT}} \Delta t_3 + \Delta V_{ESR} \quad ; \quad \Delta V_{ESR} = I_{LOAD(\max)} \times R_{C\_ESR} \qquad (35)$$

During the time period of Δt_4, the output capacitor is discharged by feedback resistor. The value of the feedback resistors determines the timing of Δt_4: when the value of the feedback resistors is smaller, the settling time of Δt_4 is shorter. On the other hand, when the value of feedback resistors is larger, the settling time of Δt_4 is longer.

As a result, the transient response is related to the bandwidth of the switching regulator, output capacitor, ESR of output voltage, and the load current.

Chapter 3
LED Driver with DC-DC Converter

3.1 The Conventional LED Driver with Current-Mode Converter

The constant current-driven LED backlight module is composed of two parts as shown in Fig. 22 (a). The boost DC/DC converter offers a sufficiently high voltage to overcome the LED forward voltage. On the other hand, the current sink circuit ensures constant current flow through each LED string without being affected by variations in the LED's forward voltage.

The ratio of two external resistors, R_1 and R_2, determines the boost output voltage. V_{OUT} is given by

$$V_{OUT} = V_{REF} \times \frac{R_1 + R_2}{R_1} \tag{36}$$

The output voltage must be satisfied for maximum forward voltage drop of LED in series to ensure that the voltage headroom of the current sink circuit is larger enough to guarantee that each LED string has the same constant current [16] [17] [18]. To overcome the maximum forward voltage drop in all the LED strings, the boost converter usually provides a higher V_{OUT}. Unfortunately, there is a redundant voltage drop, V_{ext}, across the current sink regulator as Fig. 23 shows. However, the power dissipation of the constant current generator is proportional to the LED current and the voltage headroom. Thus, this structure generates relatively large power dissipation.

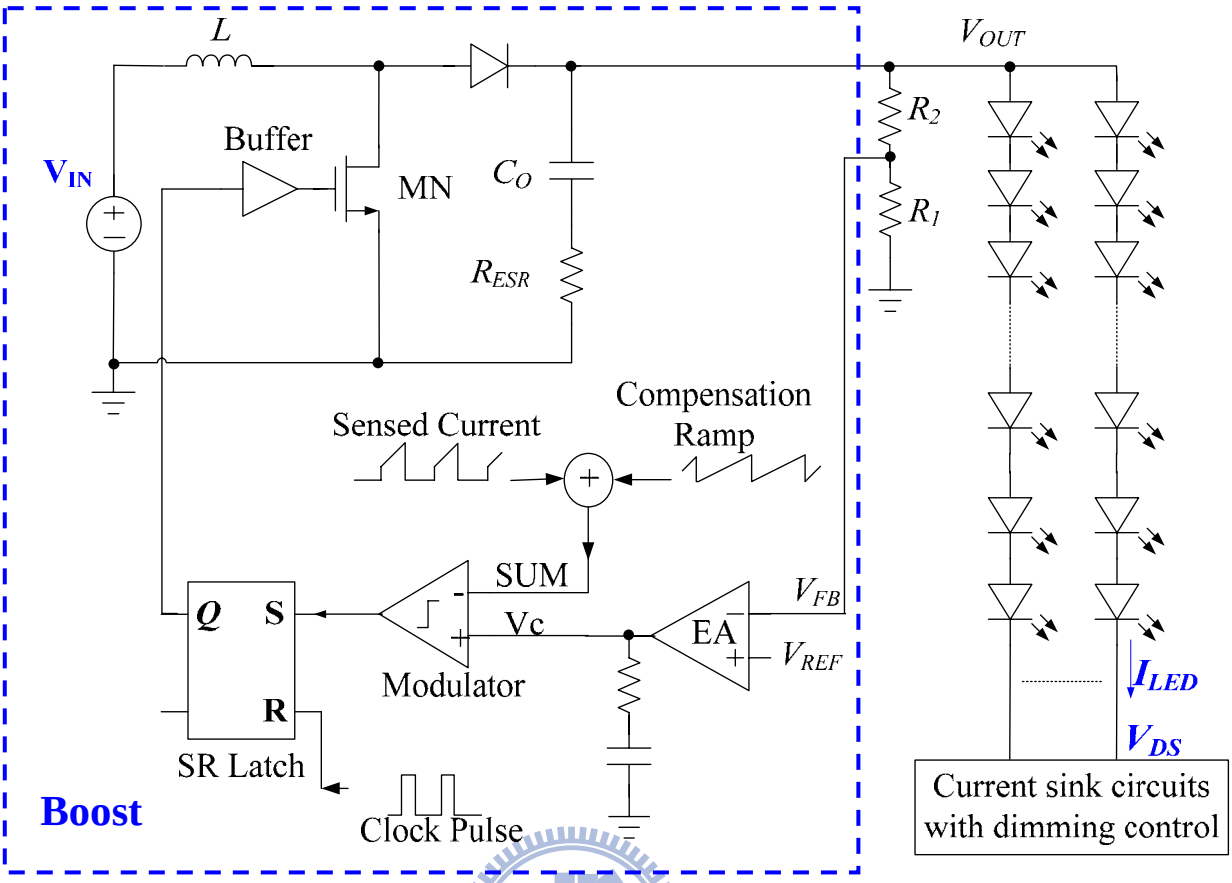


Fig. 22. The LED driver with a fixed output voltage of the boost converter.

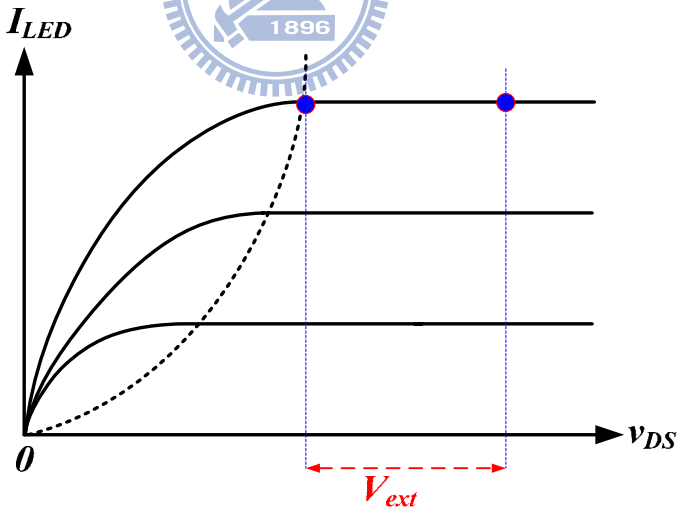


Fig. 23. The redundant drop voltage V_{ext} consumes more power on the current sink circuit

In order to improve efficiency of the LED driver, the minimum voltage [19] detection is utilized to dynamically adjust the boost output voltage to drive the LED strings as shown in Fig. 24. Since the digital pulse width modulation (PWM) dimming control method is used to tune the brightness of the LED strings, the feedback voltage, V_{FB}, must be one of the two

voltages, V_{FB2} and V_{min}. When the digital PWM dimming signal is high, the value of V_{min} determines the On the other hand, the fixed ratio must decide the closed-loop as shown in Fig. 24. The minimum voltage of the LED strings can not be decided when the digital PWM dimming signal is low. There is a large voltage difference between V_{FB2} and V_{min}. As a result, the boost output voltage has an oscillation when the digital dimming starts to control the brightness of the LED strings. The oscillation phenomenon is depicted in Fig. 25 and the simulation result shown in Fig. 26. Unfortunately, the LED backlight driver consumes more power due to the variation of output voltage.

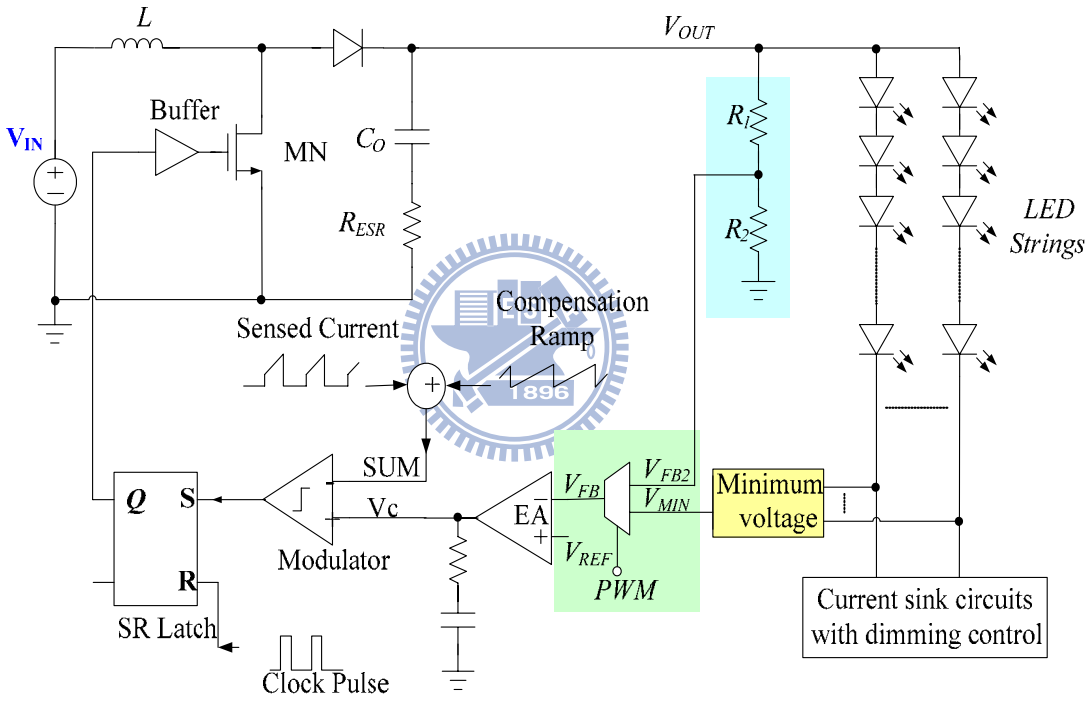


Fig. 24. The LED driver with a minimum voltage drop detector for the current sink regulator

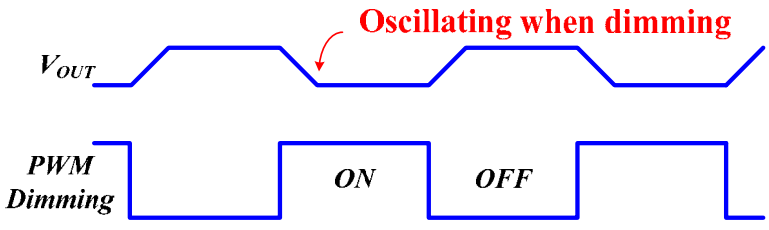


Fig. 25. The output voltage oscillates when the LED strings are controlled by the digital PWM dimming signal

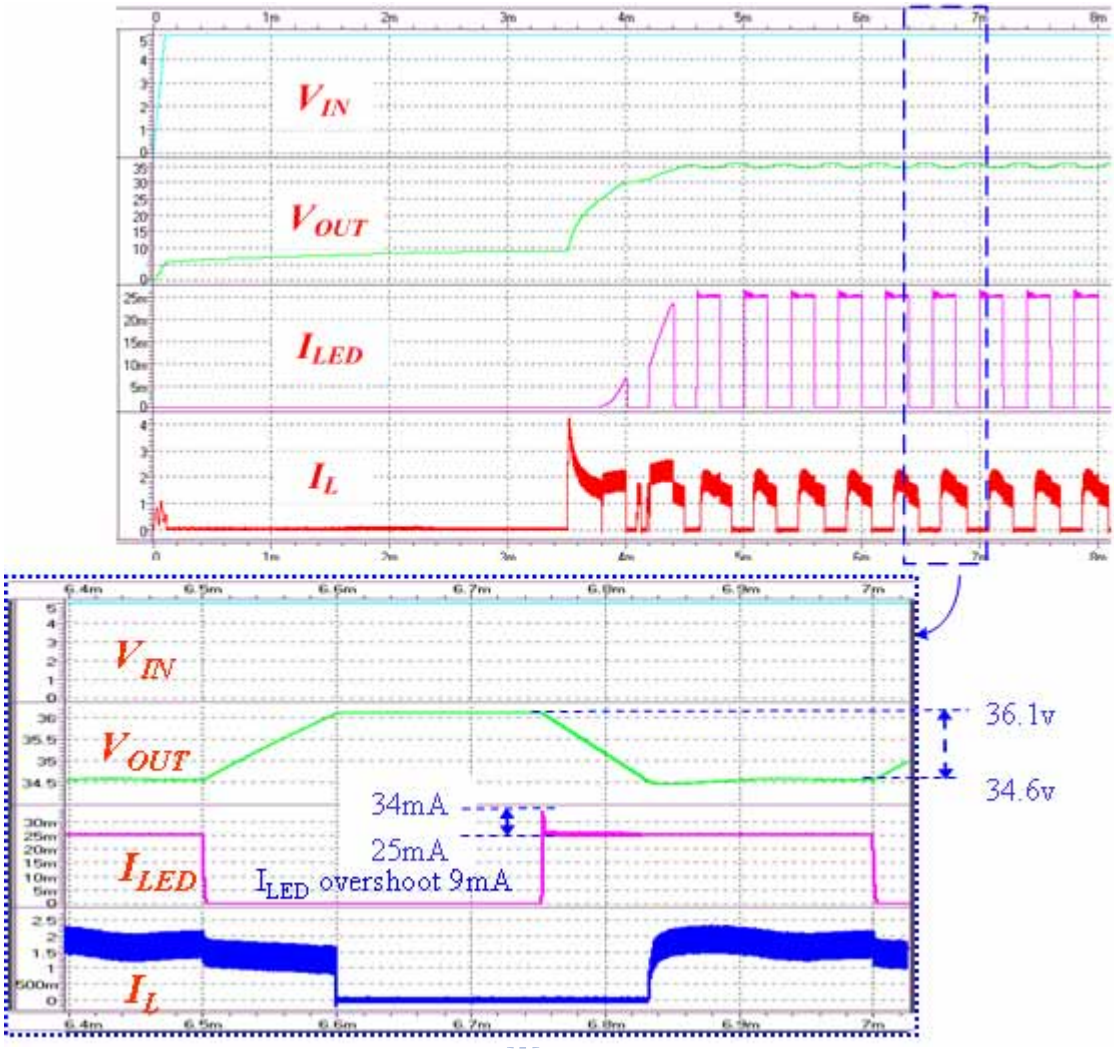


Fig. 26. Simulation results of the LED driver with a minimum voltage drop detector for the current sink regulator.

3.2 The Proposed LED Driver with Current-Mode Boost Converter

As shown in Fig. 27, the proposed LED driver with a reference tracking technique consists of a dc-dc boost converter and multiple parallel current sink regulators. The boost converter makes the signal V_{FB}, which is the ratio of the output voltage, equal to the reference voltage V_{REF}. Two control methods can determine the brightness of the LED array. One is the digital PWM dimming control method and the other one is the analog dimming control method.

The DPWM dimming signal, generated by the timing control system, has a low switching frequency and can thus determine the average LED current. This makes it possible to accurately adjust the brightness of the LED array without being affected by noise.

On the other hand, the analog dimming control method can determine the average LED current by adjusting V_{REF}. Thus, the output voltage of the boost converter is regulated to a predefined value. However, the predefined output voltage consumes much power on the current sink circuits. In order to improve the analog dimming efficiency, the value of V_{FB} must to be determined by the signal V_{ref_track} or the signal V_{min}. The minimum voltage selector can determine V_{min} among the voltages $V_{cs(1)}$~$V_{cs(n)}$ in the LED array. Therefore, the lowest voltage V_{min} is set equal to V_{ref} to ensure the output voltage V_{OUT} is regulated to high enough to overcome the forward voltage of all LEDs in series when the digital PWM dimming signal turns on. As a result, the power efficiency can be improved. Interestingly, the closed-loop is decided by the reference tracking state machine circuit when the digital PWM dimming signal turns off. To improve efficiency, the reference tracking state machine ensures that the voltage drop across the current sink circuit remains low. The boost output voltage is determined by V_{ref_track} not by a fixed ratio as depicted in Fig. 27.

The V_{ref_track} controlled by the dynamic resistor (DR) R_{DY} can minimize the output voltage ripple as shown in Fig. 28, when the LEDs in series are turned on and off. When the LED strings turn off, V_{OUT} is expressed as (37). The value of R_{DY} is defined as (38).

$$V_{OUT} = V_{REF} \times \frac{R_1 + R_{DY}}{R_{DY}} \tag{37}$$

$$R_{DY} = R_2 \times S_3 + R_3 \times S_2 + R_4 \times S_1 + R_5 \times S_0 + R_6 \tag{38}$$

The value of R_{DY} can be dynamically adjusted by the digital codes $S_{[0\text{-}3]}$. Therefore, the reference tracking technique can ensure that the value of V_{ref_track} follows the minimum

voltage of current sink voltage V_{min} when the LED strings turn on. As a result, the output voltage maintains a constant level regardless of whether the digital PWM dimming is on or off. The operation principle of the voltage reference tracking technique is described as follows.

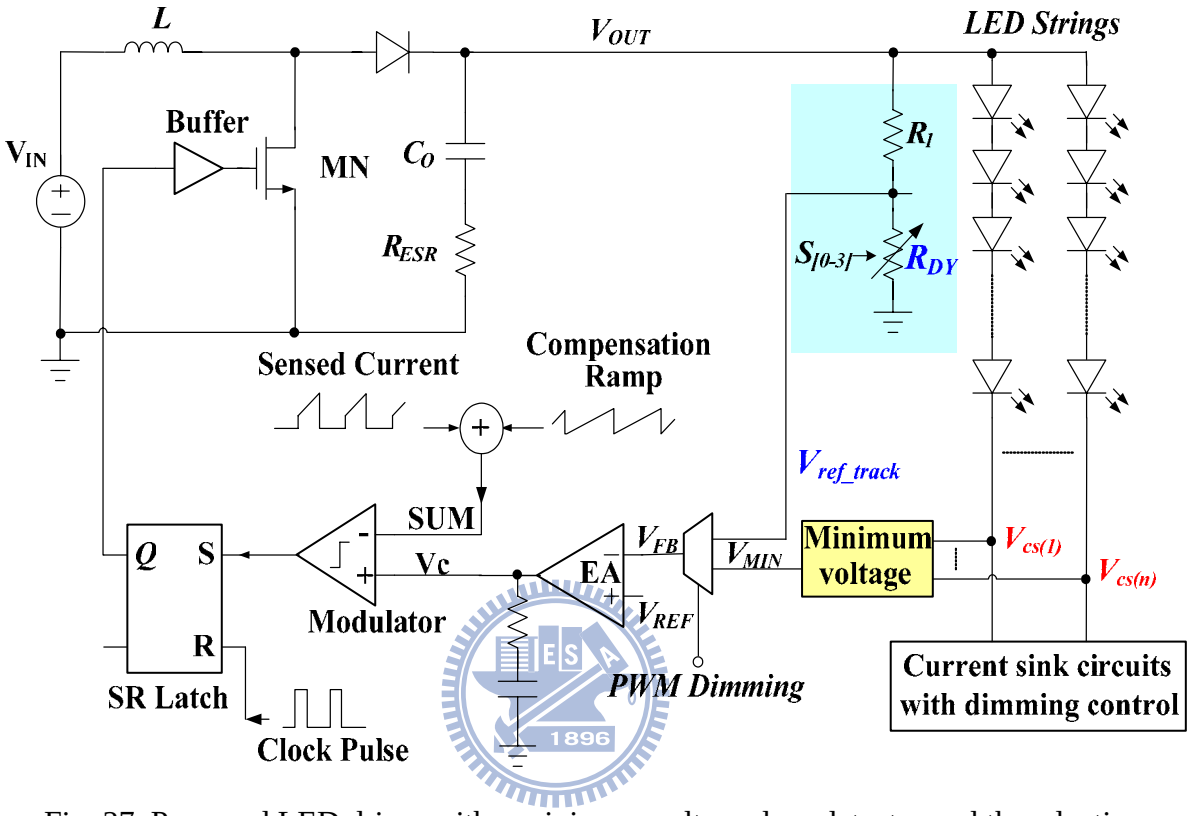


Fig. 27. Proposed LED driver with a minimum voltage drop detector and the adaptive reference tracking technique

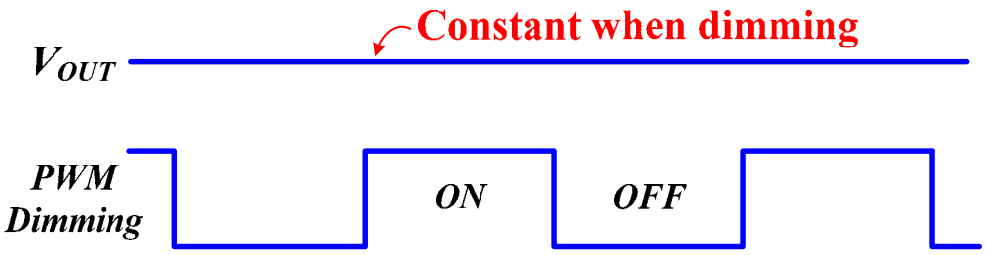


Fig. 28. The output voltage V_{OUT} can maintain a constant level whether the LED strings turn on or off.

3.3 Operation Principle of Voltage Reference Tracking Technique

The entire signal state machine is shown in Fig. 29. The signal *VS* is the current sensing signal from current sink circuit. The signal D_C is utilized to detect the LED current. The

control signal D_C confirms that the LED current already reaches to set up. V_{ref_track} compares with V_{min} to generate the signal D_V to decide the value of V_{ref_track} needs to increase or decrease. The reference tracking technique uses the two signals D_C and D_V to generate the 4-bit control signal $S_{[0-3]}$ through the use of the reference tracking state machine when the digital PWM dimming is enable. $S_{[0-3]}$ is utilized to adjust the dynamic resistor R_{DY}. When the LED strings turn on, D_V stays in a low level or a high level would decide the up tracking the down tracking compared to V_{min}. Table Ⅲ shows the truth table of the tracking state machine. When the digital PWM dimming is low, the reference tracking procedure is turned off. The dynamic resistor R_{DY} can be used to regulate the boost output voltage level. Besides, when the digital PWM dimming is high and the signal D_C is low, it means the output voltage is not in the correct level to ensure a correct LED current. Therefore, the reference tracking state is set to the idle status. The timing diagram of the voltage reference tracking is shown in Fig. 30.

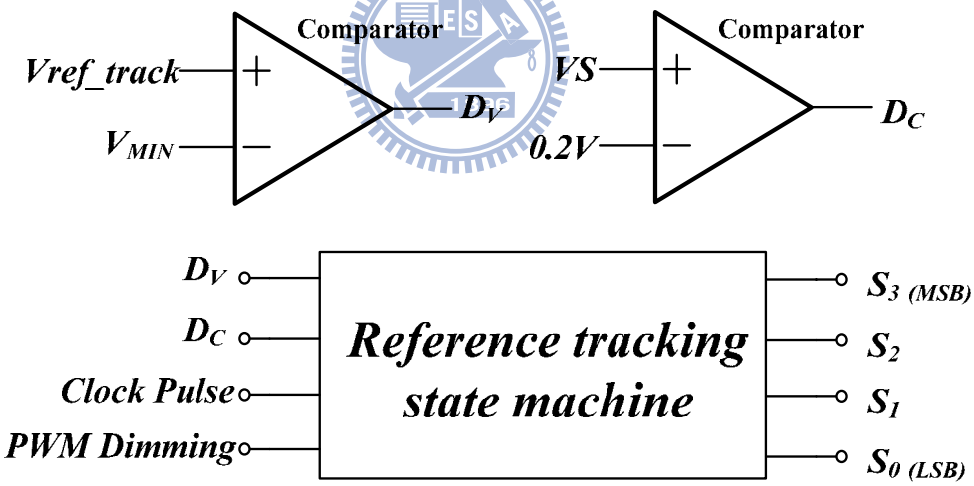


Fig. 29. State machine of Voltage reference tracking.

D_C	D_V	PWM Dimming	Tracking state
1	0	1	up tracking
1	1	1	Down tracking
0	x	1	idle
x	x	0	idle

Table Ⅲ. The relationship between of input and output control signals.

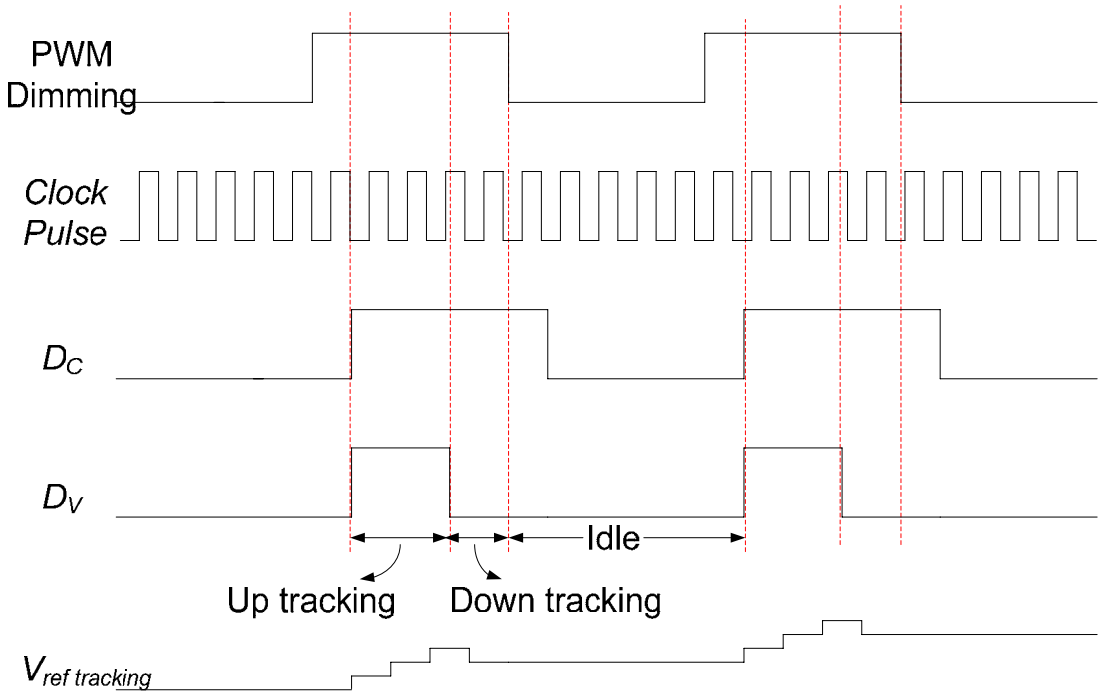


Fig. 30. The timing diagram of the proposed LED driver circuit with the adaptive reference tracking technique.

3.4 Constant Current Sink

The current sink circuit is necessary for the LED driver to achieve a constant and uniform luminous. The structure of the precise constant current sink circuit is depicted in Fig. 31 [20] [21]. This circuit only uses one external resistor R_{EXT} to provide the precise current and thereby reducing the PCB area and chip area. The voltage-to-current converter is used to generate the reference current I_{REF} by an external resistance R_{EXT} and a precise internal reference voltage 0.6 V. The current mirror pair (M_5 and M_6) amplifies the current I_{SET} , and the voltage V_{SET} can be written as Eq. (39):

$$V_{SET} = I_{SET} \times R_{SET} = \frac{0.6 \times M}{R_{\_EXT}} \times R_{SET} \text{ where } I_{SET} = M \times I_{REF} = \frac{0.6 \times M}{R_{\_EXT}} \quad (39)$$

The operational amplifier OP_1 is employed to ensure an equal drain-source voltage (V_{DS}) of the two P-type MOSFETs, M_5 and $M_{.}$ This design prevents the channel length modulation effect and obtains a precise mirror current. For good matching, the M_5 and M_6 should inter-

digitize each other. In addition, the resistor R_{SET} is larger than the resistors R_1 - R_8 to reduce the power consumption sue to the current I_{SET}. Moreover, the resistors R_{SET} and R_1~R_8 must be the same type of resistor and carefully matched in the layout. Therefore, the LED current can be expressed as Eq. (40):

$$I_{OUT1} = \frac{V_{SET}}{R_1} = \frac{0.6}{R_{\_EXT}} \times M \times N \text{ where } R_1 = \frac{R_{SET}}{N} \tag{40}$$

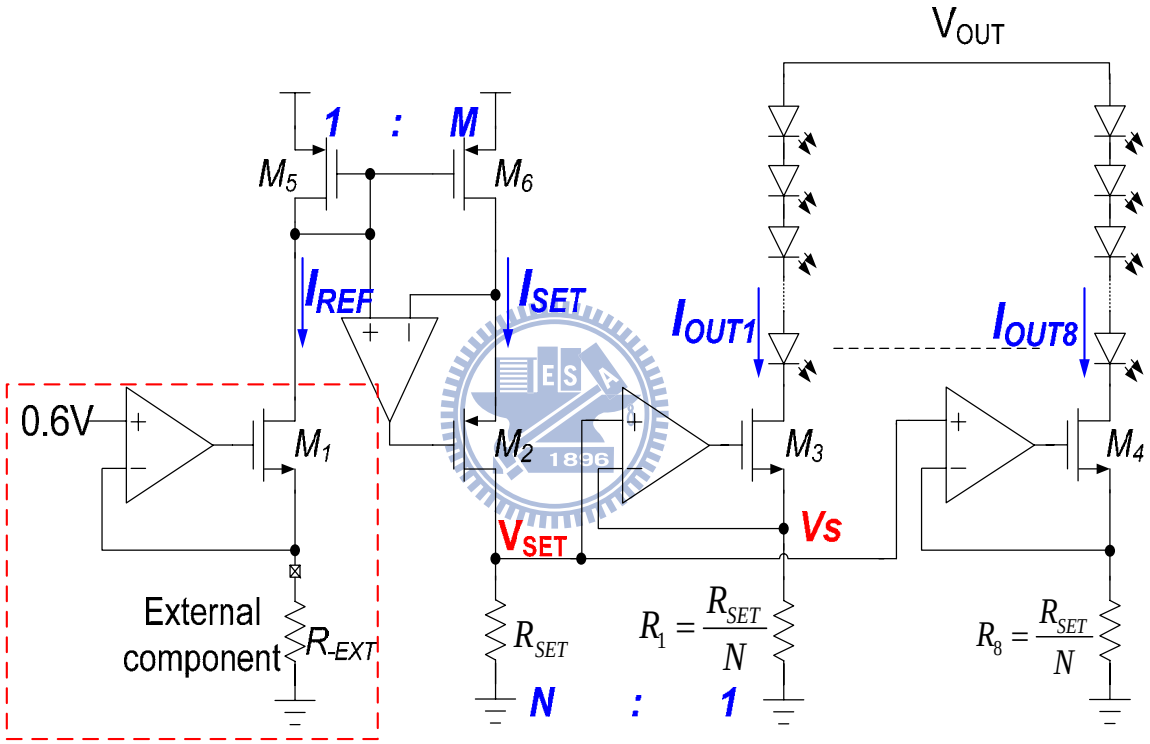


Fig. 31. Structure of the precise constant current sink circuit

Chapter 4
Circuits Implementations and Simulation Results

This chapter discusses the design analyses and simulation results of each sub-circuit. Table IV shows simulation conditions.

Table. Ⅳ. Simulation Condition

Power supply of control circuit				
4.5 V		5V		5.5V
Temperature Range				
-25 ~ 125				
Process Corner				
TT	FF	SF	SS	FS

4.1 Bandgap Reference and Bias Circuit

The bandgap reference circuit is used to generate a fixed voltage level, V_{REF}, that is independent of power supply V_{DD}, temperature and process variations [22] [23]. Furthermore, the reference voltage produced by the bandgap reference voltage must be compared with the feedback voltage V_{FB} in PWM control. Hence, the accurate bandgap voltage reference is important for voltage regulator.

The bandgap voltage reference involves the bandgap core circuit, bias circuit, trimming circuit and startup circuit, which are shown in Fig. 32. The bandgap reference voltage is formed using CTAT and PTAT reference. With the proper design, the temperature coefficient of the bandgap reference voltage can be very small. The reference voltage is the sum of PTAT and CTAT voltage drop, which can be expressed as Eq. (41). The base-emitter voltage of the bipolar transistor is a negative temperature coefficient (TC) and V_T is the positive TC. Therefore by adjusting the coefficient of resistor R_1-R_3 and the ratio of bipolar Q_1-Q_2 can obtain zero TC for voltage reference V_{REF}, which can be written as (42)

$$V_{REF} = V_{BE2} + \frac{V_T \ln n}{R_3}(R_3 + R_2) = V_{BE2} + (V_T \ln n)\left(1 + \frac{R_2}{R_3}\right) \quad (41)$$

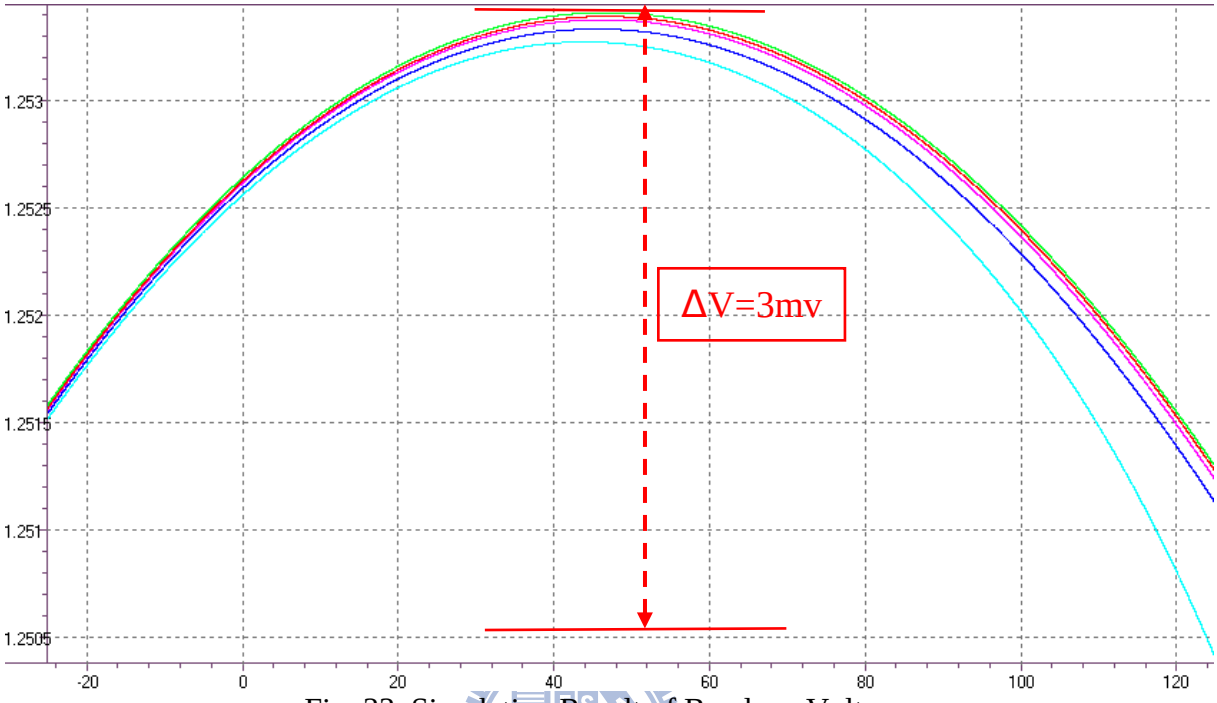


Fig. 33. Simulation Result of Bandgap Voltage.

$$TC = \frac{\frac{\partial V_{REF}}{V_{REF}}}{\partial T} \times 10^6 = \frac{\frac{3mV}{1.25V}}{150°} \times 10^6 = 15.9\,ppm/°C \quad (42)$$

The bandgap voltage variation is about 3.0mV when the temperature varies from -25℃ to 125℃ in over corner condition simulation.

4.2 Voltage to Current Converter

A current mode DC-DC converter must add a compensation ramp to prevent the sub-harmonic oscillation. Therefore, a voltage to current converter can be used to convert the voltage signal to the current signal. The structure of the V-I converter is shown in Fig. 34. This converter includes the resistor R1, two PMOS transistors, an operational amplifier OP1, and the NMOS MN1. The OP1 and M_{N1} constitute a negative feedback system. The

operational amplifier can force the same voltage at the inverting input Vs of OP1 and the node VFB. The I_1 current can be expressed as (43).

$$I_1 = I_R = \frac{Vs}{R_1} \tag{43}$$

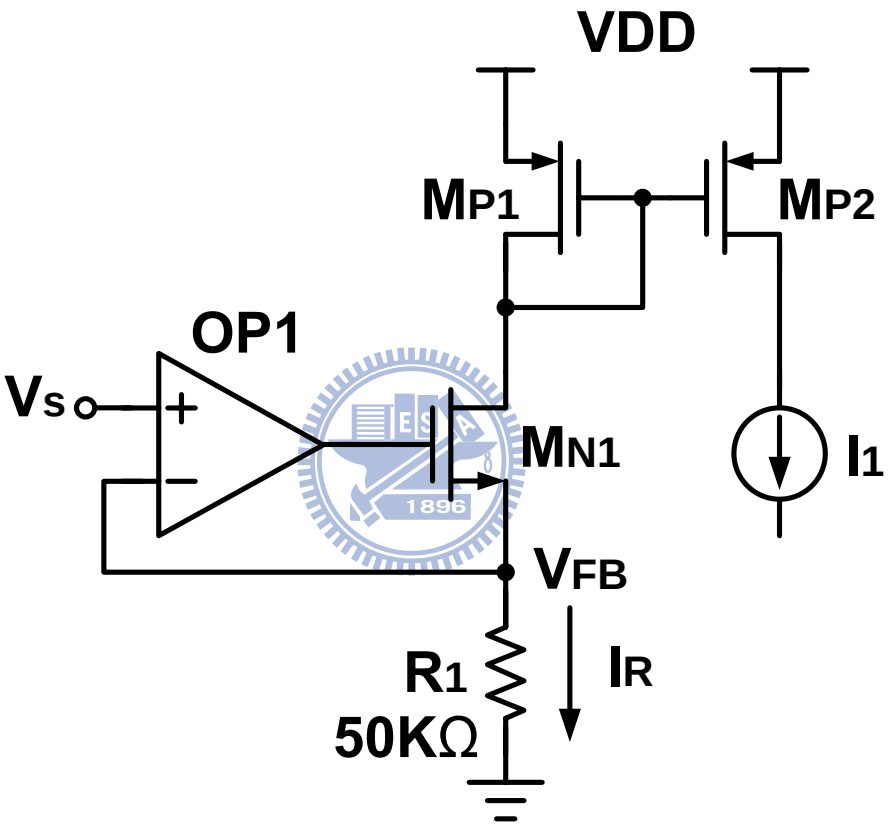


Fig. 34. Voltage to Current Converter

Table. V shows the converting accuracy of simulation result and the converting accuracy is 99.3%.

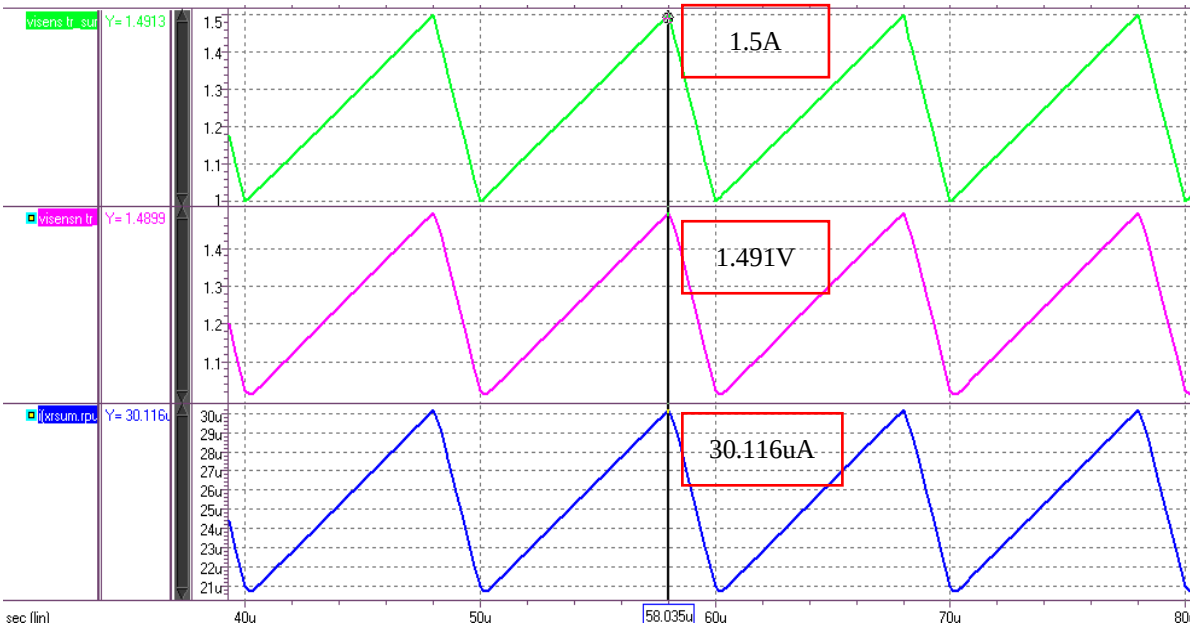


Fig. 35. Simulation Results of the Voltage to Current Converter.

Table. Ⅴ. Conversing accuracy of V-I Converter				
V_S	**I_{MP2_IDEAL}**	**V_{FB_ACTUAL}**	**I_{MP2_ACTUAL}**	**Converting Accuracy**
1.491v	29.82uA	1.489v	30.116uA	99.3%

4.3 Sum

When operating in the current-mode control, the proposed design experiences an instability problem for duty ratios greater than 50%. A ramp signal as acting as a slope compensator must be added to the sensed current signal to prevent sub-harmonic oscillation. Both the current sensing output and the compensation ramp can convert the current information. Adding these two currents together sums the voltage through a single resistor. The structure of sum circuit is shown in Fig.36.

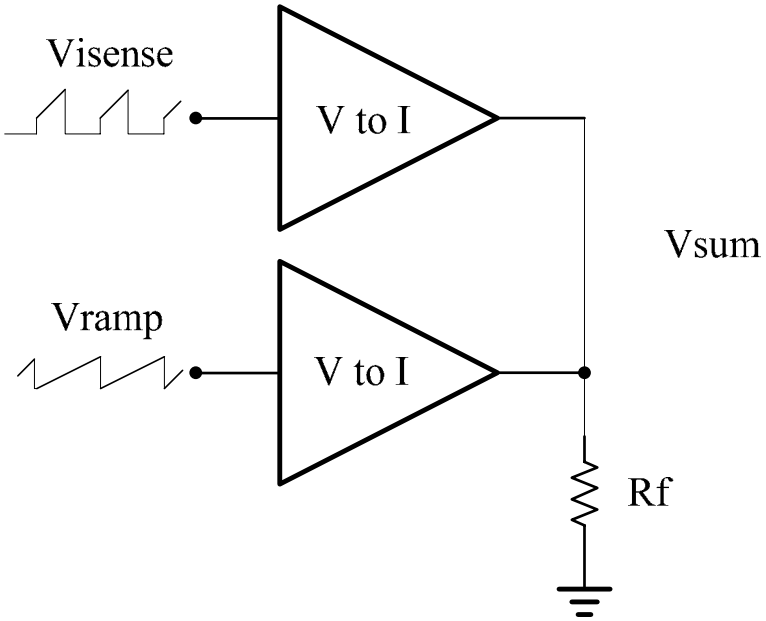


Fig. 36. Sum circuit

4.4 Clock and Ramp Generator

The Structure of the clock and ramp generator is shown in Fig. 37. The oscillator and ramp generator is used to generate the clock and ramp signals for the PWM control and the compensation slope for the current-mode converter, respectively. As shown in Fig. 37, [24] it consists of a V-I converter and a resistor R_{FEST} to generate the constant current I_{FSET} as expressed in Eq. (44).

$$I_{FSET} = \frac{0.6v}{R_{FEST}} \tag{44}$$

I_{M3} is multiplied by the aspect ratio of transistor M_2. It is used to charge the capacitor C_F. When the ramp signal V_{RAMP} reaches VH, the upper comparator changes its state. At this moment clock signal CLK turns on transistor M_4 to discharge capacitor C_F. When the ramp signal V_{RAMP} reaches VL, the lower comparator changes its state. At this moment, transistor M_4 is turned off to recharge capacitor C_F. Therefore, the clock frequency and the slope of the compensation ramp are generated. The transient response of the ramp signal V_{RAMP} and the clock signal CLK is shown in Fig. 38.

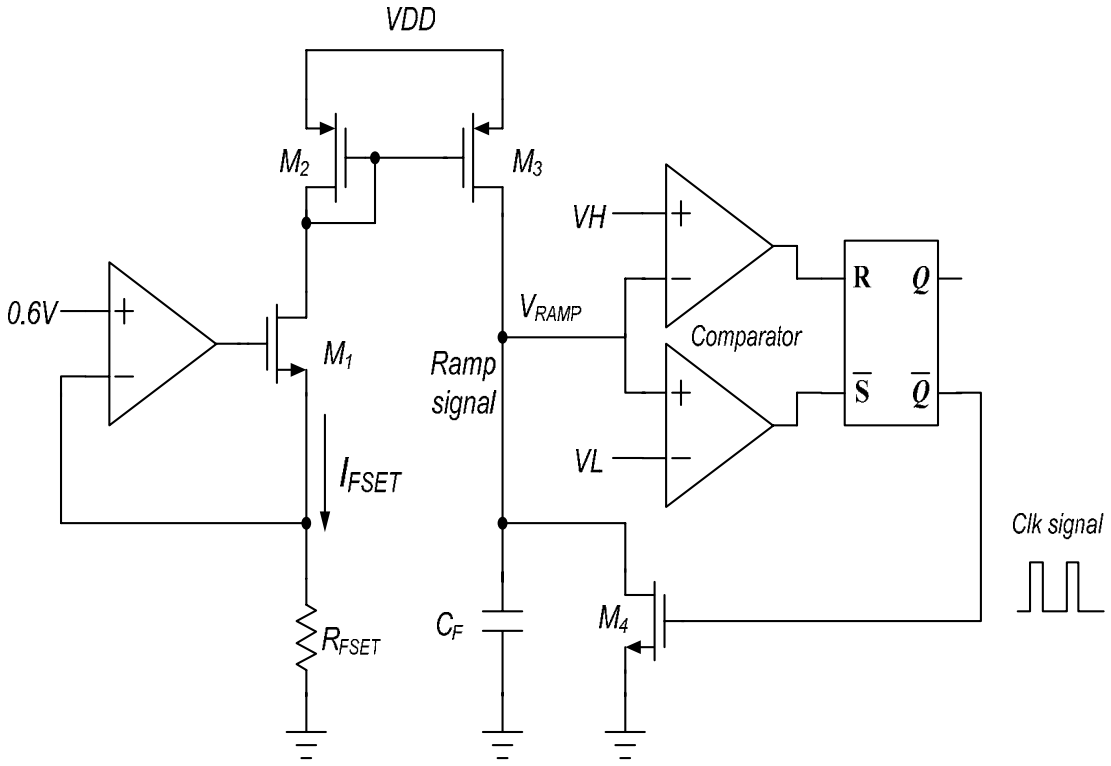


Fig. 37. Structure of the clock and ramp generator.

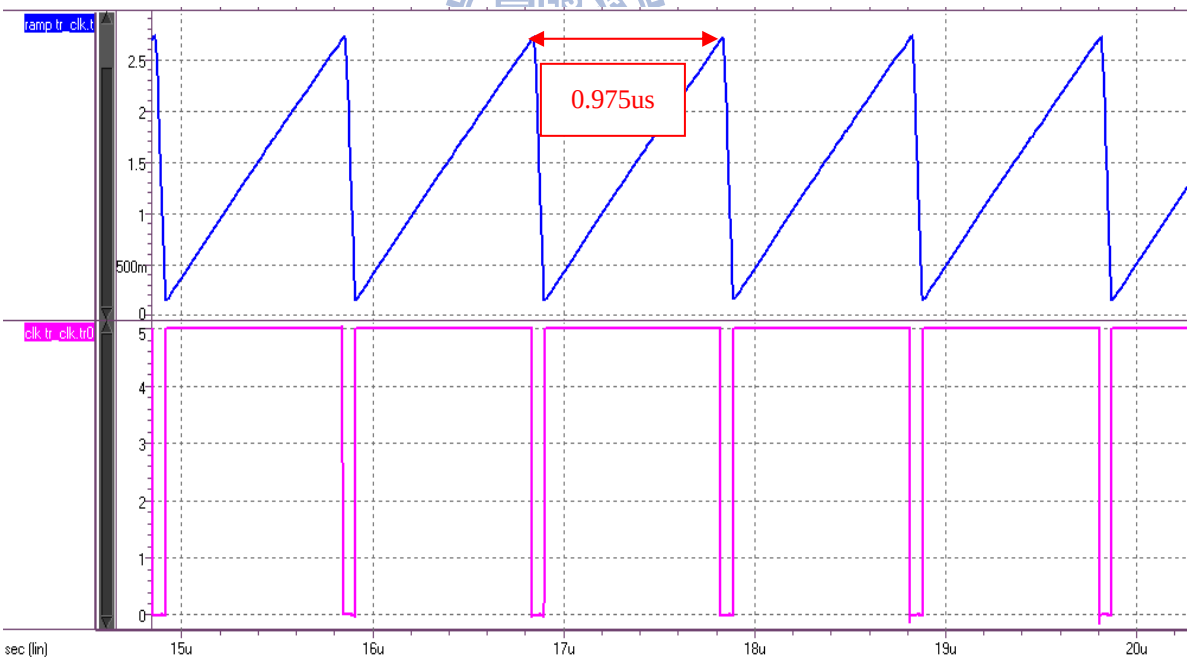


Fig. 38. Waveform of the clock and ramp signal.

The resistor R_{FSET} and the capacitor C_F can adjust the switching frequency. This design sets the frequency at 1MHz.

$$f = \frac{1}{T} = \frac{1}{0.975us} = 1.026MHz \qquad (45)$$

4.5 Non-Overlap Gate Driver

Fig. 39 shows the non-overlap gate-driver circuit. The power losses are mainly due to the conduction loss, switching loss, and shoot-through current loss. The shoot-through current loss is related to the design of the buffer stage driving the Power MOS. If the buffer stage is poorly designed with a simple inverter chain, a shoot-through current will occur and a large current will pass through the transistor. Therefore, a non-overlap gate driver buffer stage circuit is necessary to avoid shoot-through current and eliminate the extra power loss in dc-dc converters. The MP and MN are non-overlapping switches.

To implement the delay1 and delay2 of inverter chain generate delay time signal. The delay time signal and NOR gates operate to generate a dead time control. The simulation result is as shown in Fig. 40.

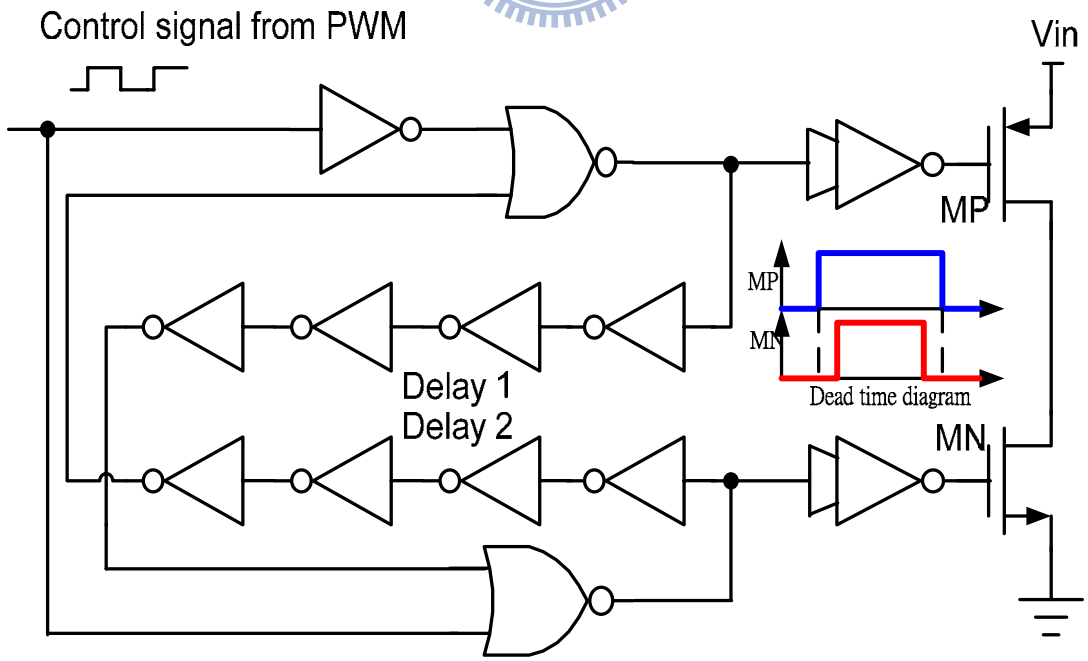


Fig. 39. Non-Overlap Gate Drive

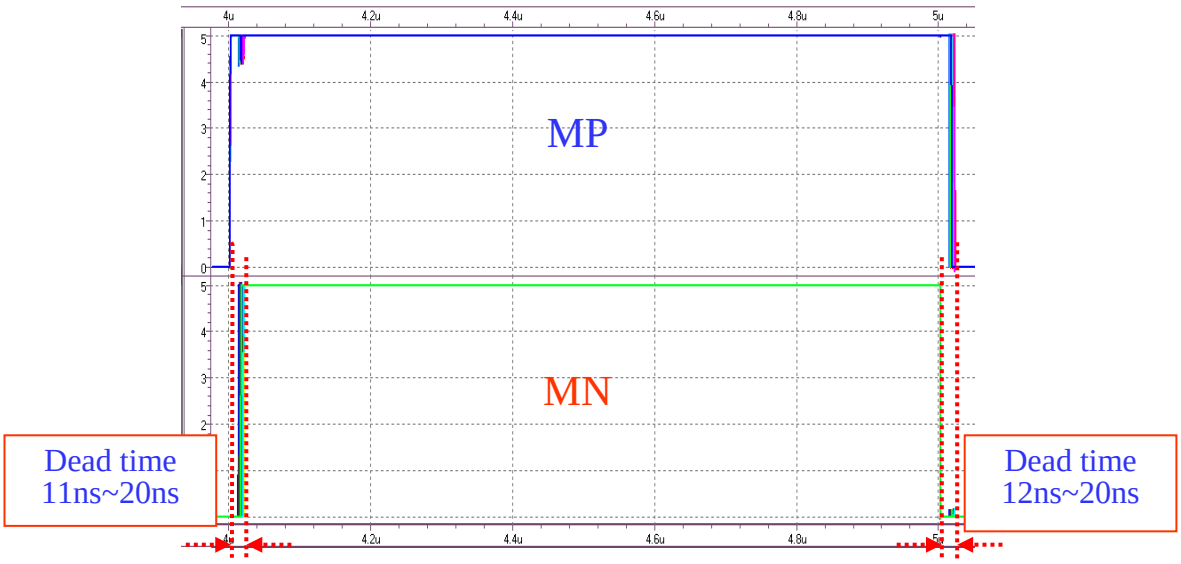


Fig. 40. Dead time diagram

4.6 Current Sensing

The structure of the current sense is shown in Fig.41. [24] The inductor current sensing circuit is based on an error-amplifier voltage mirror. The MN1 is a power transistor and the MN2 is a sensing transistor. The size ratio of MN1 to MN2 is K=3600 in this design, and thus their drain-current ratio is 3600 when their drain-source voltage match. The inductor current and Power MOS current are shown in Fig. 42, have two different slopes at ON and OFF periods. Both slopes contain V_{IN} information, while the falling slope includes additional information about Vo. the feedback network to the error amplifier has already measured Vo. Therefore, only the rising slope of the inductor current is necessary, and sensed by measuring the drain current of MN1.

Because the error amplifier produces a virtual short circuit during the on period, the drain–source voltages of MN1 and MN2 are equal. The current mirror MPR1 and MPR2 produce the sensed current of MN2 ISEN, which can be derived as Eq. (46):

$$I_{SENS} = \frac{I_L}{K} = \frac{I_L}{3600} \tag{46}$$

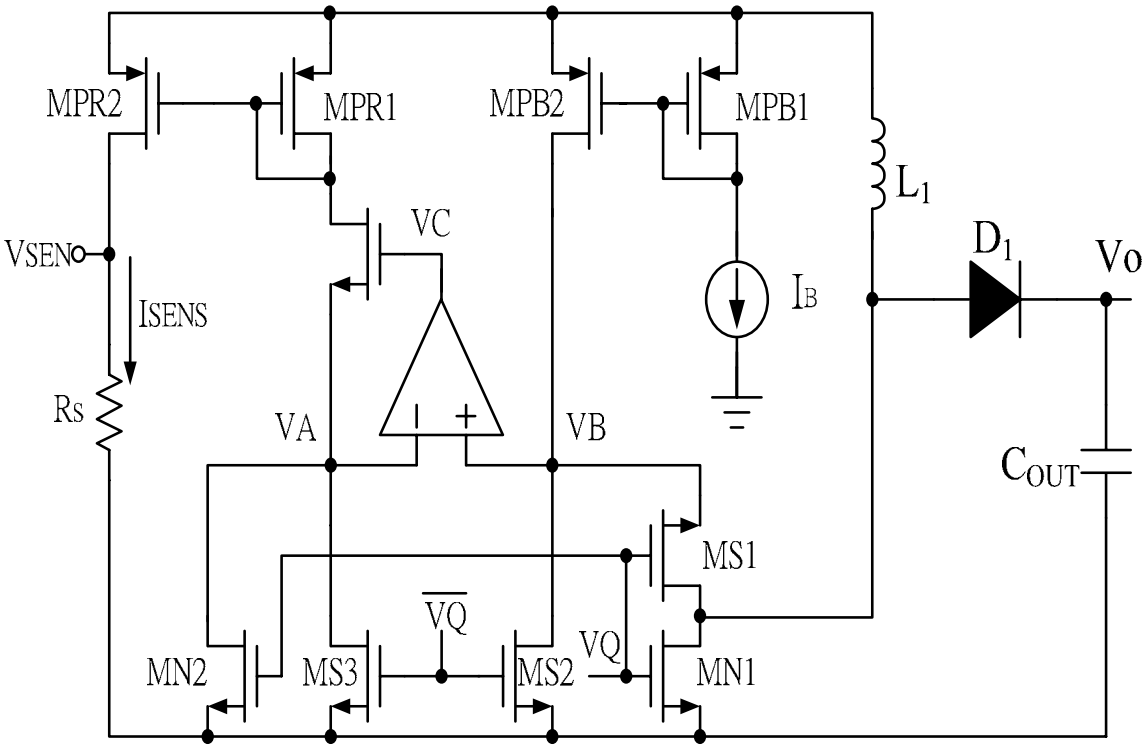
The sensed current is reproduced by the current mirror formed by MR1 and MR2. As a result, the generated voltage canbe expressed as (47).

$$V_{SENS} = I_{SENS} \times R_S \tag{47}$$

The design of the error amplifier for the current-sensing circuit requires a high voltage gain to reduce finite-gain error and a low offset voltage to ensure $VA \approx VB$, a low input common-mode range ($VA \approx VB \approx 0$ as MN1, MN2, and MS1–MS3 are switches), and a wide output swing so that different sensed currents can be generated by different VC. The structure of amplifier is used by low voltage operational amplifier.

The stability problem of the current-sensing, both nodes at VA and VB have low impedance in both ON and OFF periods due to the low on-resistances of MN1and MN2. It is only one high-impedance node at VC. This design makes it easier to achieve frequency compensation.

The Fig. 43 and Fig.44 show the waveforms of the current sensing circuit when the peak current of inductor I_{L_PEAK} is 1.5A and 2.5A, respectively. The I_{SEN_ACTUAL} and V_{SEN_ACTUAL} are simulated values of sensed current and sensing voltage. Table Ⅵ shows that sensing accuracy the lowest sensing accuracy of the current sensing circuit is 98.0%.



Element:

(a) Power NMOS: MN1

(b) Sensing MOS:MN2

(c) Switch: MS1 ~ MS3

(d) Current mirror MOS: MPR1 ~ MPR2

Fig. 41. Current Sense

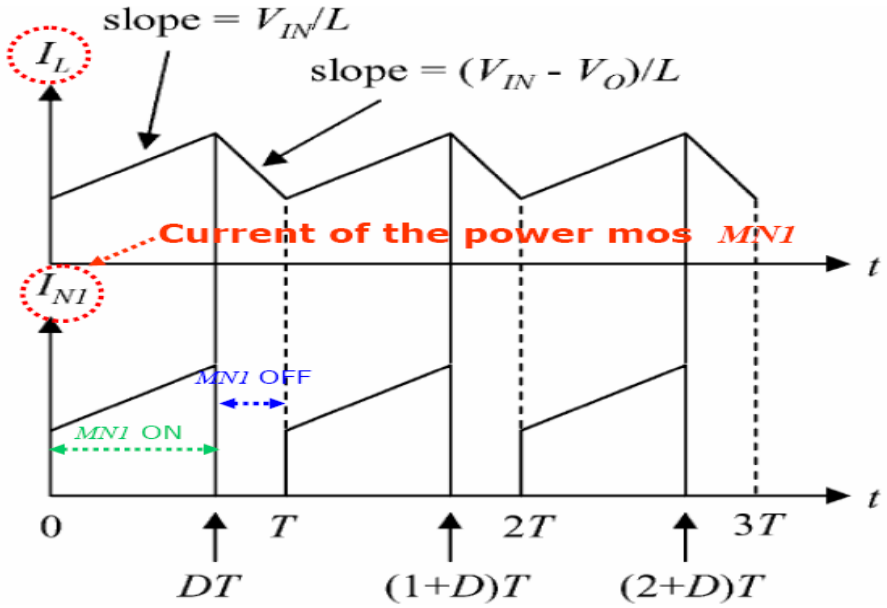


Fig. 42. Inductor Current and PowerMOS Current of Boost converter

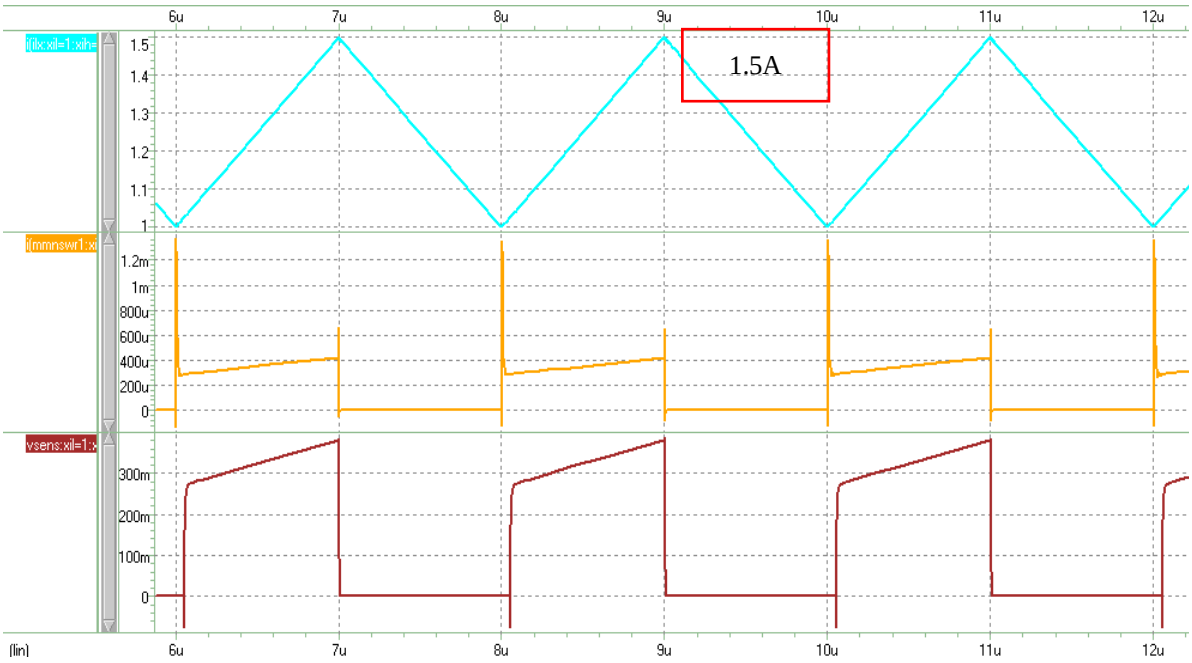


Fig. 43. Waveforms of current sensing circuit when I_{L_PEAK} is equal to 1.5A

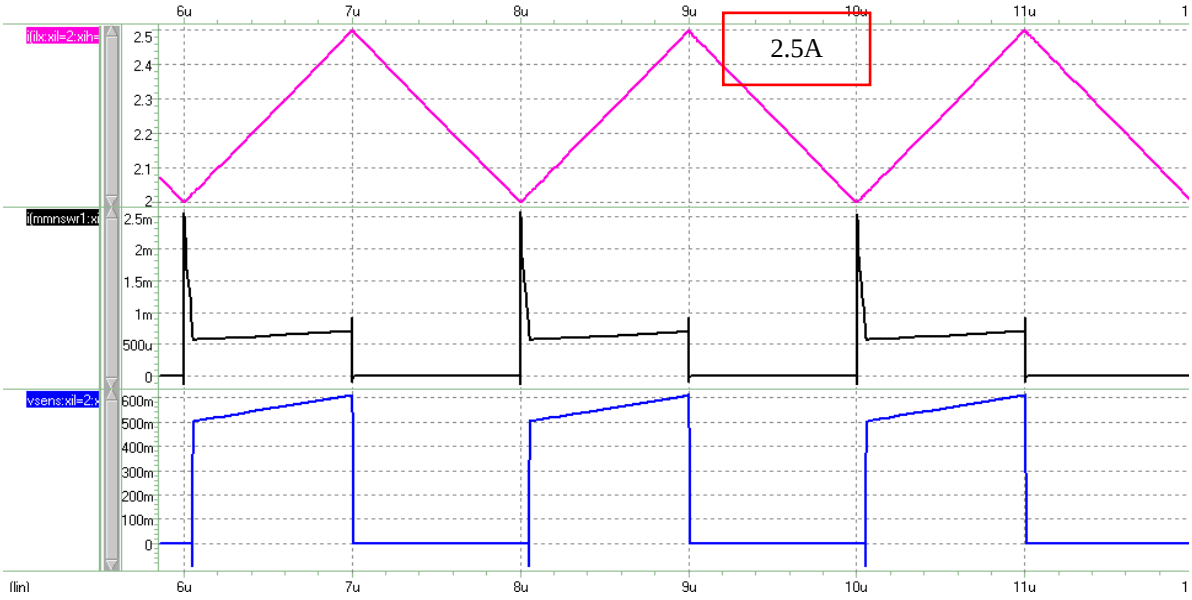


Fig. 44. Waveforms of current sensing circuit when I_{L_PEAK} is equal to 2.5A

Table. Ⅵ. Sensing Accuracy of Low Voltage Current Sensing Circuit			
Simulation condition: Temp: -25 ~ 125, 5 corner			
I_{L_PEAK}	**I_{SEN_IDEAL}**	**I_{SEN_ACTUAL}**	**Current Sensing Accuracy**
2.5A	57.9uA	61.0 ~ 63.3uA	91.5% ~ 94.9%
1.5A	34.7uA	37.6 ~ 40.1uA	86.9% ~ 92.3 %

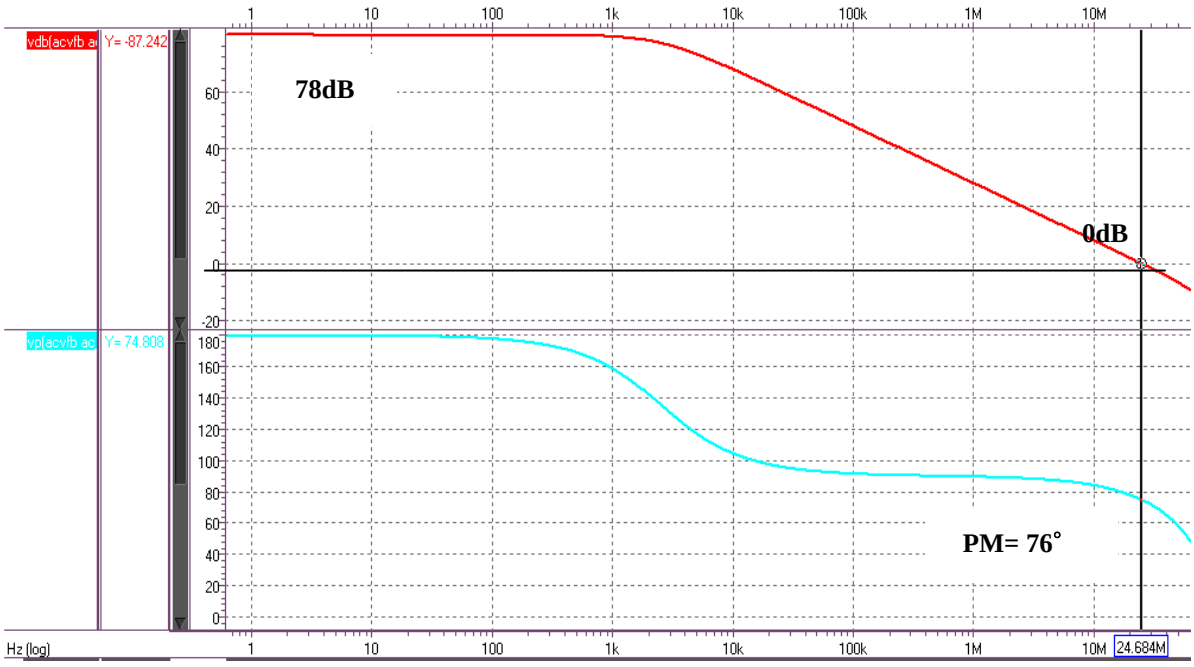


Fig. 45. Simulation result of Frequency Response

The simulation result of the frequency response is shown in Fig. 45. The dc gain of the error amplifier is about 78dB for all corners. The unity gain frequency is 24.6MHz and the phase margin is 76° under the condition inductor current is 1.5A.

4.7 Lead Edge Blanking

Fig. 46 shows that the current waveform is the leading-edge spike caused by parasitic capacitance in the dc-dc converter, and recovery current from the output rectifiers. It is easy to see that this spike needs to be isolated from any fault sensing circuit.

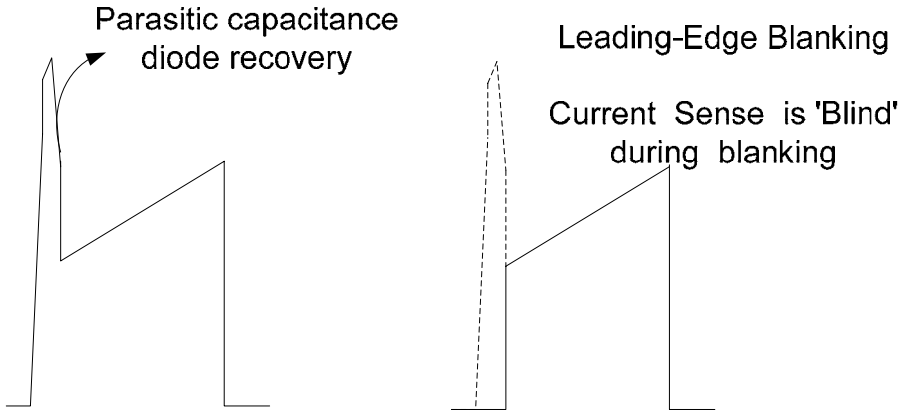


Fig. 46. A typical current waveform and current sense is ‘Blind’ during blanking

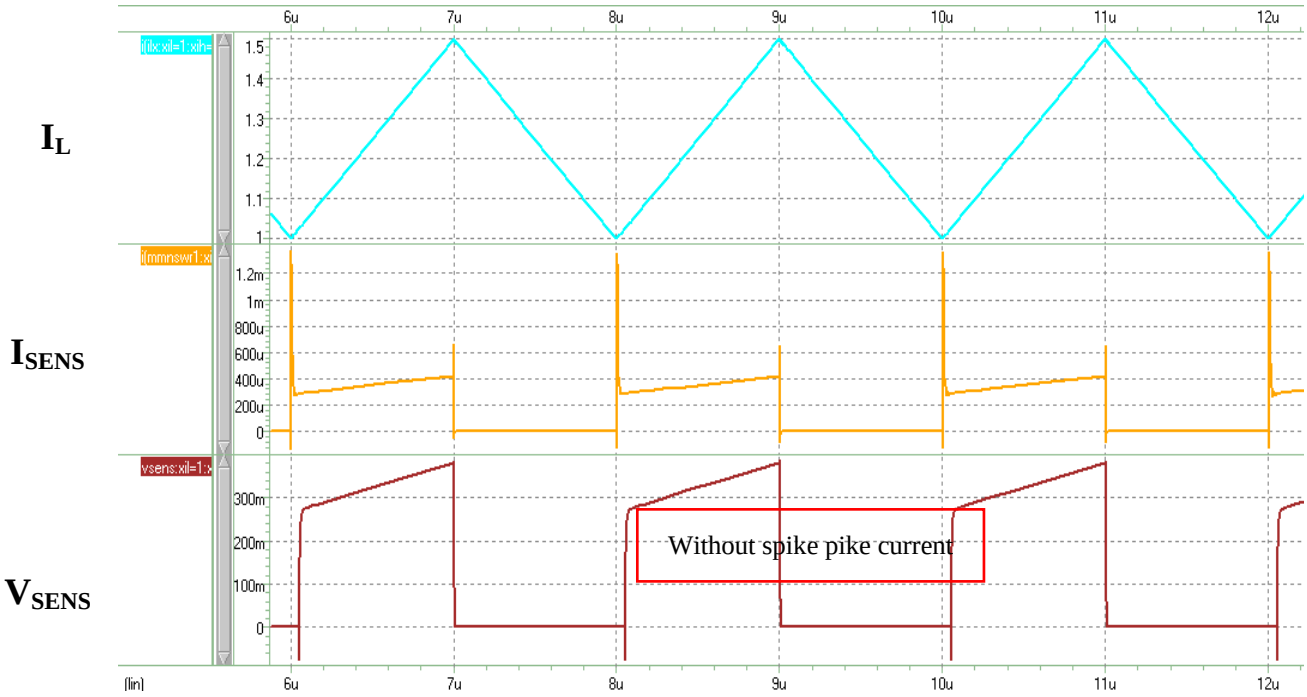


Fig. 47. V_{SENS} waveform of with Leading-edge blanking

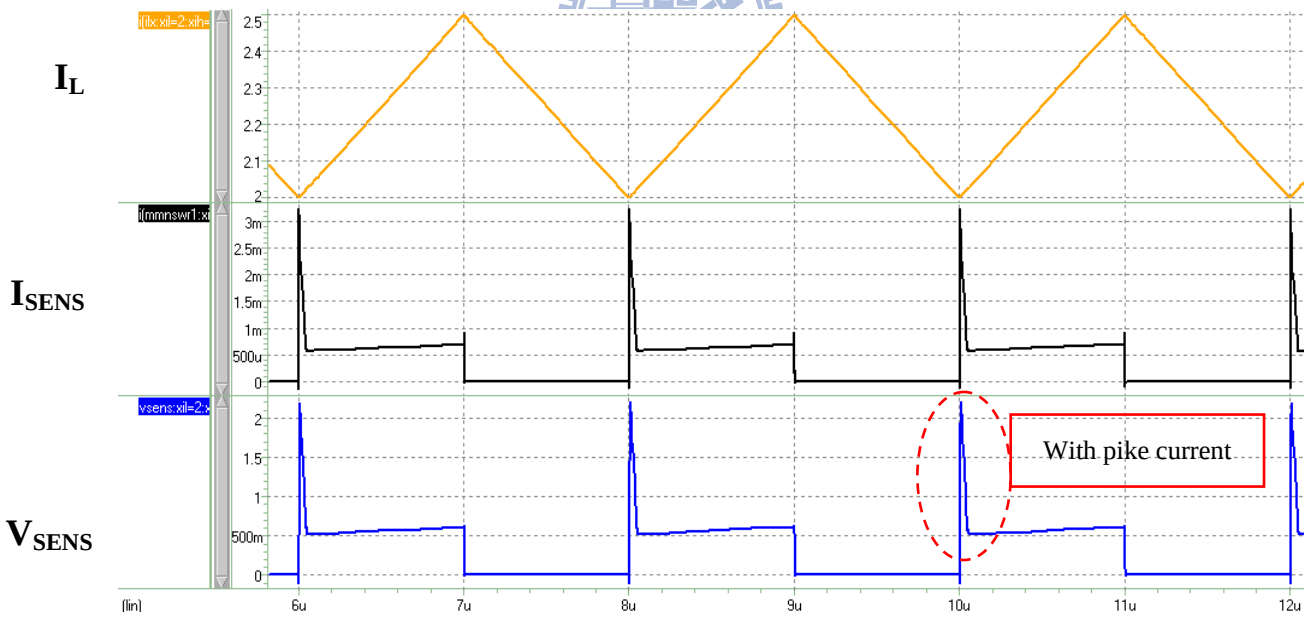


Fig. 48. V_{SENS} waveform of without Leading-edge blanking

4.8 Error Amplifier

The error amplifier is utilized to amplify the error of feedback and reference voltage. The structure of the error amplifier is that of a cascode operational transconductance amplifier

(OTA). The OTA is with characteristic of high current driver capability, and therefore, the OTA is suitable for the boost converter with a large compensation capacitor. The structure of the cascode operational transconductance amplifier is shown in Fig. 49. Transistors MB1 to MB10 constitute the biasing circuit. This design uses a cascode OTA because it is a single-stage amplifier that has a high gain and only one dominant pole.

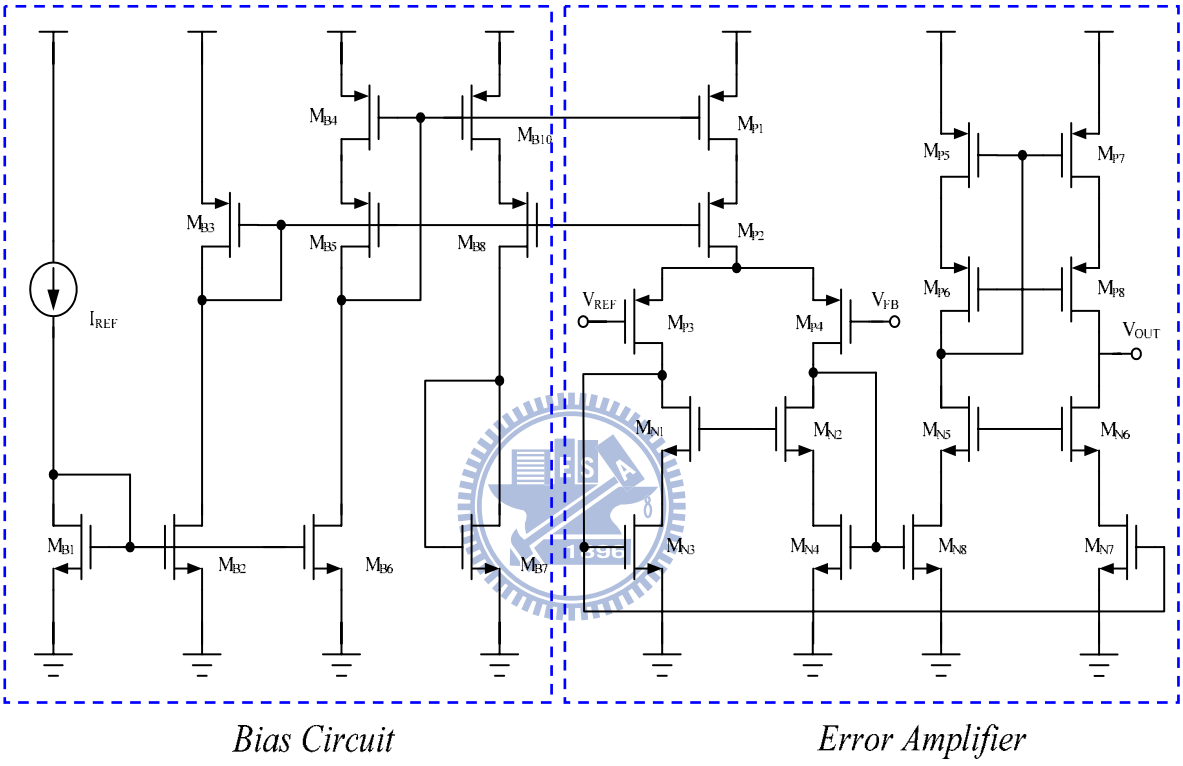


Fig. 49. The structure of Error Amplifier.

The simulation result of the operational transconductance amplifier is shown in Fig. 50. The dc gain of the error amplifier exceeds 86dB for all corners. The unity gain frequency is about 1.5MHz and the phase margin is 78° with a capacitive load of 10pF.

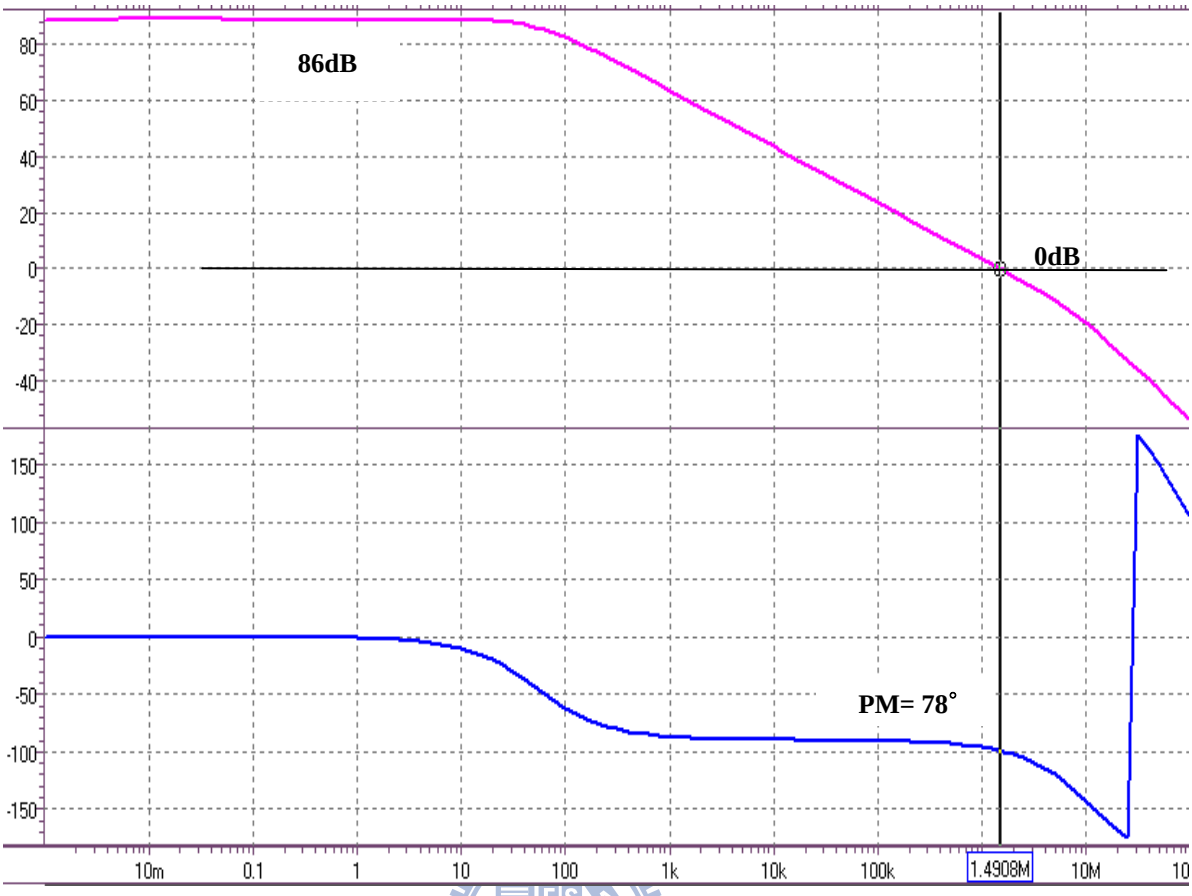


Fig. 50. Simulation result of Frequency Response

Using pole-zero cancellation is preferable for dominant pole compensation because it speeds up response time by extending the bandwidth with pole-zero cancellation. Figure 2.20 shows that the compensator consists of an operational transconductance amplifier [5], a resistor R_1, and a capacitor C_1. The zero and pole provided by this compensator with OTA consist of passive elements at the output node of OTA and output impedance of OTA. The transfer function of this compensator is given by Eq. (48). The frequency compensation components R_1 and C_1 can be calculated directly using the zero and pole:

$$T(S) \approx g_m R_o \frac{1+\frac{S}{1/C_1 R_1}}{1+\frac{S}{1/C_1 R_o}} \quad for\ R_o >> R_1 \qquad (48)$$

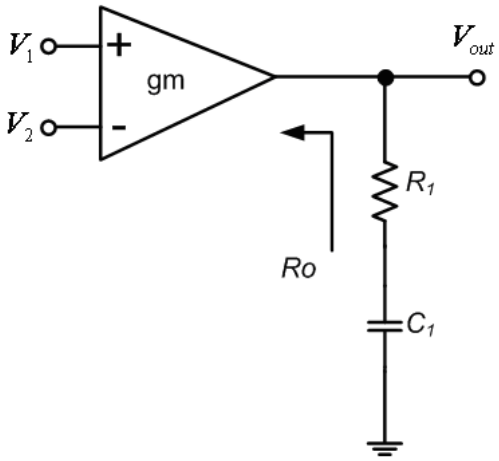


Fig. 51. Compensator organized with an OTA.

4.9 Minimum Voltage Detector Circuit

The LED string can have the same type of LEDs in each string, or have different types of LEDs. The output voltage must be satisfied for the maximum forward voltage drop of LED in series to ensure that the voltage headroom of the current sink circuit is large enough to guarantee that each LED string has the same constant current. To improve efficiency of the LED driver, the minimum voltage detection dynamically adjusts the boost output voltage to drive the LED strings.

Using V_{OUT0} and V_{OUT1} as inputs, the comparator CMP shows that V_{MIN} is V_{OUT1} if $V_{OUT0} > V_{OUT1}$ or V_{OUT0} if $V_{OUT1} > V_{OUT0}$, which is accomplished by the multiplexer MUX0. The minimum voltage Vmin03 is produced from V_{OUT0} to V_{OUT3}; the Vmin47 is produced from V_{OUT4} to V_{OUT7}. Therefore, the V_{MIN} is produced by V_{OUT0} to V_{OUT7}. As a result, seven basic cells are necessary to get the minimum voltage of eight channels. The structure of minimum voltage detector is shown in Fig.52.

The control loop of the dc-dc converter compares the minimum voltage V_{MIN} to the V_{REF} of the dc-dc converter, showing that the minimum voltage V_{MIN} is V_{REF}.

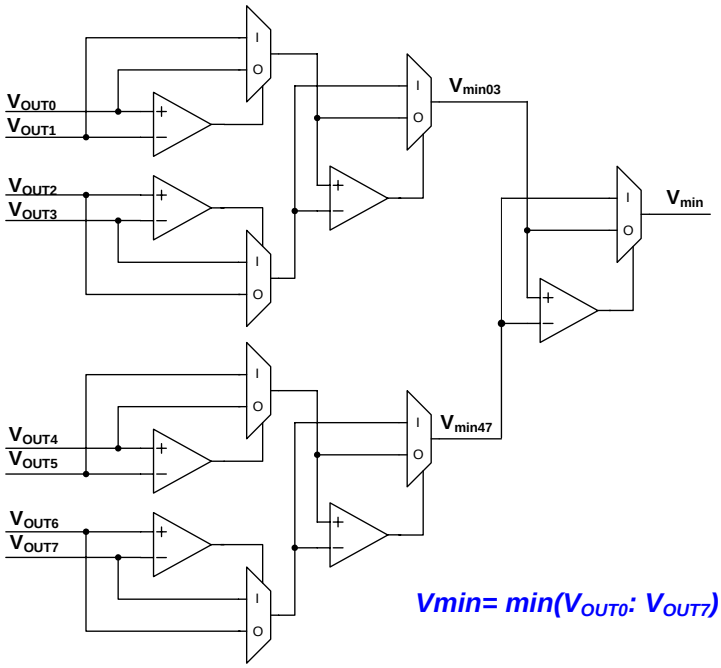


Fig. 52. Structure of Minimum Voltage Detector.

4.10 Whole Chip Simulation Results

The simulation condition of whole chip system is as shown in Fig. 53.

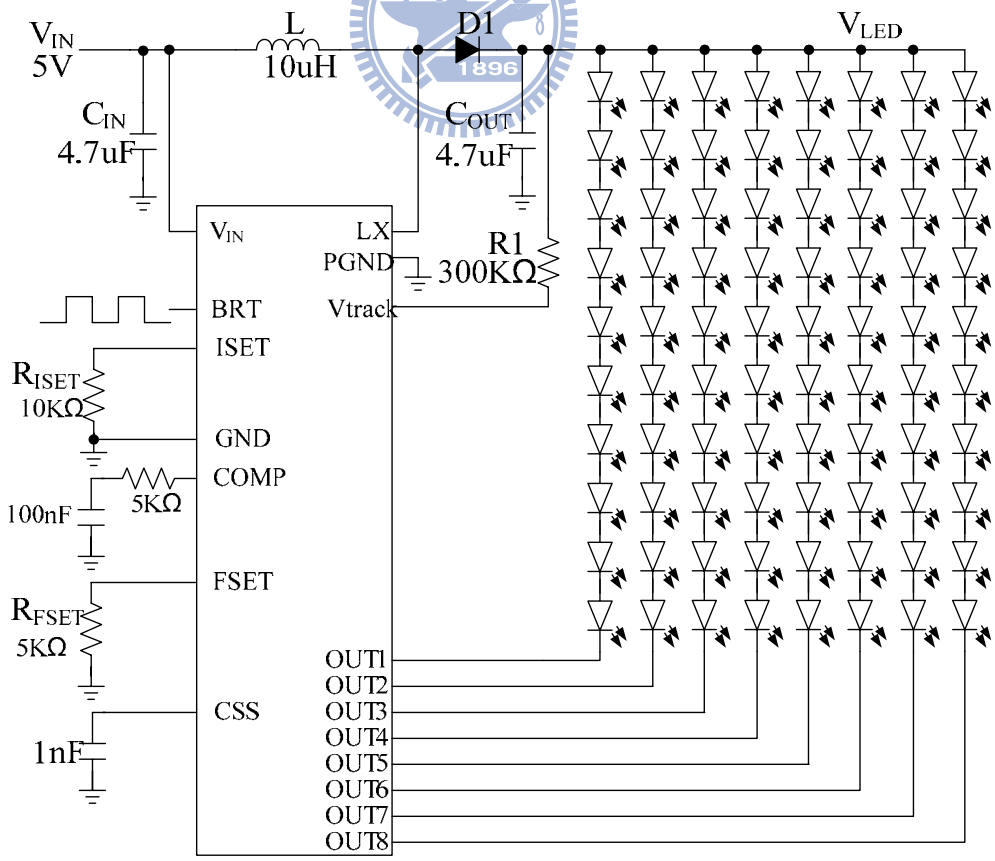


Fig. 53. Whole Chip System Diagram

The simulation result is shown in Fig. 54. The voltage of VOUT at the LED string in turn off, it can similar to regulated VOUT at the LED strings turn on at the LED strings turn on receive steady voltage. In Fig. 54, the load current changes from 0mA to 210mA. The load regulation is 0.47mV/mA with transient recovery time about 100μs. In Fig. 56, the input voltage changes from 5v to 5.5v. The line regulation is 200mV/V and transient response time 0.8ms.

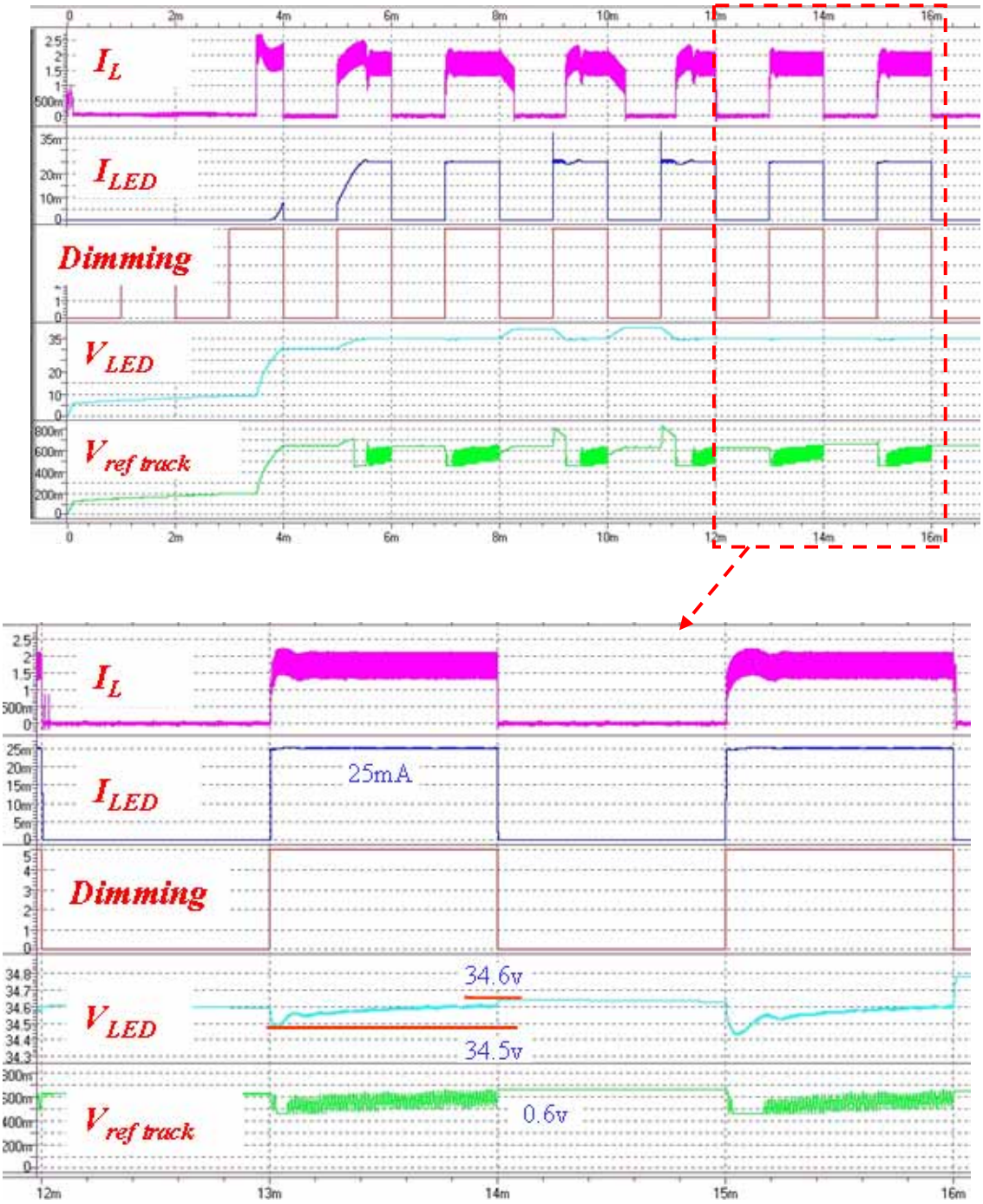


Fig. 54. The simulation results of proposed driving circuit with PWM Dimming.

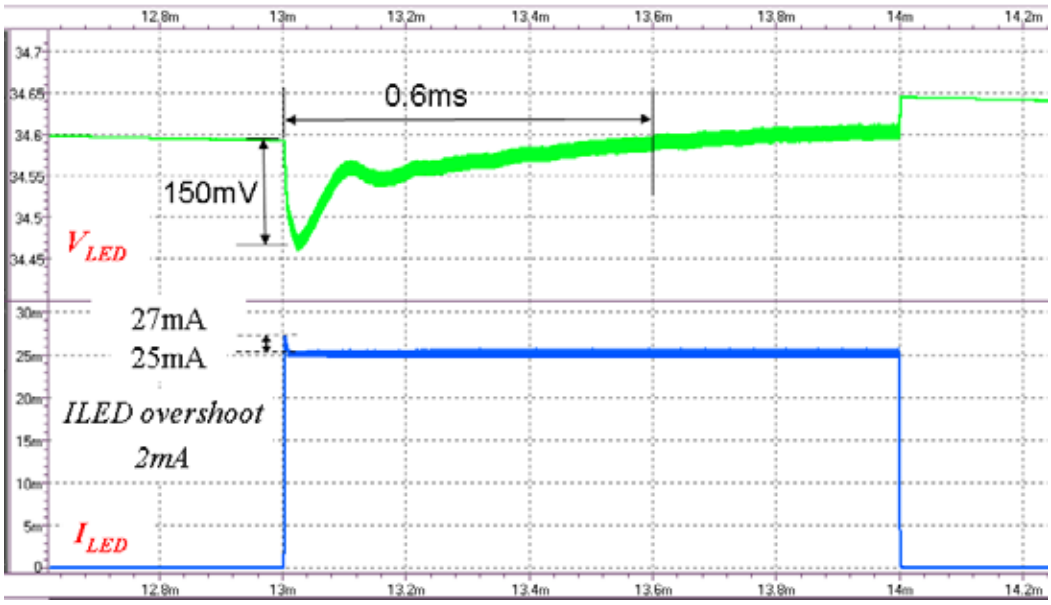


Fig. 55. Load Transient Response.

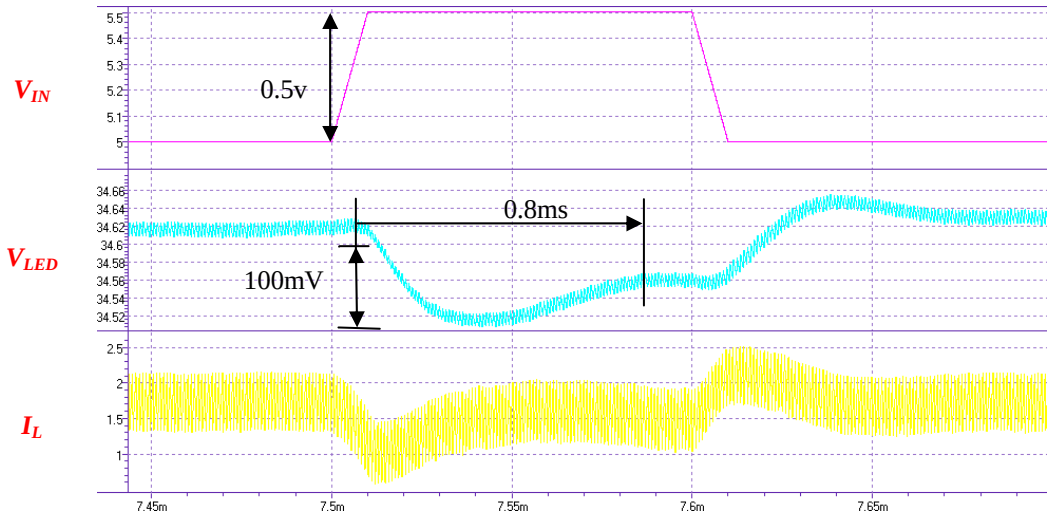


Fig. 56. Line Transient Response.

Specification	**Conventional LED Driver**	**Proposed LED Driver**
Input voltage	4.5V ~ 5.5V	
Output voltage	20V ~ 40V	
Switching frequency	1MHz	
Maximum output current	240mA	
Inductor	4.7μH	
Capacitor	4.7μF	
Load regulation	-	0.4mV/mA @V_{IN}=5V and V_{OUT}=35V
Line regulation	-	200mV/V @V_{OUT}=35V and I_{OUT}=200mA
Ripple of V_{OUT}	1.5V	0.1V
Power loss $P=V*I*8$	300mW	20mW
I_{LED} *overshoot*	9mA	2mA

Table.Ⅶ. PERFORMANCE SUMMARY

Chapter 5
Conclusions and Future Work

5.1 Conclusions

This thesis presents an adaptive reference tracking driving technique that minimizes boost output voltage oscillation and improves the power efficiency when the digital pulse width modulation dimming is enabled. An asynchronous 1MHz DC/DC converter with a dynamic resistor implements the minimum voltage reference tracking technique. This approach guarantees high efficiency and a stable boost output voltage regardless of whether the LED strings are on or off. Therefore, the output voltage has almost similar voltage level whether the LED strings are turned on or off. Therefore, the output voltage maintains a similar voltage level at all times, allowing the V_{OUT} to maintain a constant voltage. In addition, the LED current could be more accurate to guarantee the uniform luminosity. The output voltage is equal to 34.6V whether the LED strings are on or off. The low-feedback voltage of 600mV at each LED string helps to reduce power loss and improve efficiency.

The test chip was simulated by TSMC 0.25um BCD 40V to demonstrate high efficiency and the stable boost output voltage. Simulation results show that the proposed design can minimize the oscillation output voltage from 1.4V to 0.2V, and decrease the overshoot of LED current from 9mA to 2mA. Finally, this approach reduces the power consumption of the current sink regulator from 300mW to 20mW.

5.2 Future Work

LED is extensive and applied to the backlight source of various products. To provide satisfactory for high quality and brightness for large-size LCD TV backlights, the development trend of the LED drivers require a high-current boost converter and a higher output voltage to drive LED strings Therefore, the LED driver circuit fabrication needs the development of high voltage process.

Reference

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