直流二極濺鍍銦鎵鋅氧化物薄膜電晶體技術開發研究

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摘　　要

本研究論文成功地發展出一套新式具有高載子移動率 (High mobility) 的銦鎵鋅氧化 (Indium-Gallium-Zinc-Oxide) 薄膜電晶體 (Indium-Gallium-Zinc-Oxide Thin Film Transistors)，可應用於主動式顯示面板 (Active Matrix Liquid Crystal Display) 技術及搭配有機發光二極體面板 (Organic Light Emitter Diode Panel) 作為驅動電路，以增大顯示電晶體元件的效能與顯示畫素開口率，並減緩光漏電 (Photo leakage current) 對元件造成這影響。亦可推廣應用至驅動電路，達成系統面板整合技術 (System On Panel) 的遠景。在研究中，我們利用工業技術研究院顯示中心之直流二極濺鍍機台 (DC Sputter)，使用 300 × 540 mm 銦鎵鋅氧化物 (Indium-Gallium-Zinc-Oxide) 的靶材 (Target)，改變不同的直流濺鍍功率與基板移動速率，於玻璃基板上形成最具均勻性之薄膜，並在濺鍍過程中，控制通入氧氣的流量，來形成具備半導體特性之銦鎵鋅氧化物薄膜，而於半導體層製程完成後藉由後續的退火處理，我們成

功建立一個得以在室溫環境之下，均勻沈積銦鎵鋅氧化物薄膜的沈積條件且具有最佳薄膜電晶體電性表現的半導體層 (Semiconductor layer)。在本論文中，我們也利用各種材料分析技術與儀器，如原子力顯微鏡 (AFM)、X 光薄膜繞射儀 (XRD)、掃瞄式電子顯微鏡 (SEM)、四點探針 (Four-Point Probe) 等 ... 來針對銦鎵鋅氧化薄膜之結晶性 (Crystallization)、晶格尺寸 (Grain size) 和薄膜片電阻 (sheet resistance) 等特性進行分析與研究，並將銦鎵鋅氧化物薄膜製作成電晶體元件，進行電晶體元件“電性特性的分析”與“直流劣化特性分析”。最後，因不具通道保護層的電晶體元件會與環境中的水氧產生反應，故我們使用 PECVD 於 200 °C 下沈積 SiNx 與 SiOx 於銦鎵鋅氧化薄膜電晶體上，探討當電晶體元件加上保護層時其對元件電性的影響。

Investigation of Indium-Gallium-Zinc-Oxide Layer by Direct-Current sputtering in Thin-Film Transistors

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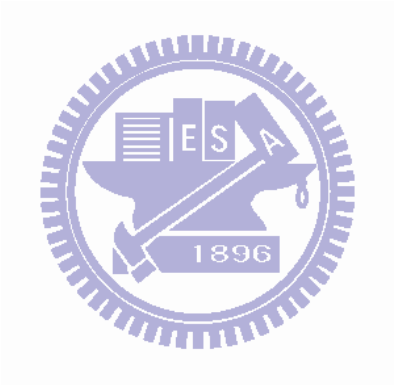
ABSTRACT

In this thesis, we have successfully developed a thin film transistors (TFT) using a novel material amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) as semiconductor layer, with high carrier mobility. The use of IGZO-based material can increases the field-effect mobility of TFT devices, the aperture of AMLCD panel and releases the issue of photo-excited leakage current. In this work the a-IGZO film was deposited on a glass substrate by sputtering Indium-Gallium-Zinc-Oxide target in DC glow discharge plasma of an argon/oxygen mixture. We changed the power of DC sputter and substrate move rate to adjust the uniformity of the a-IGZO film. Also, the conductivity and carrier concentration were controlled by adjusting the flux of the mixture oxygen during film deposition and thermal annealing temperatures. An optimal IGZO film deposition condition was finally established at room temperature for the IGZO TFTs. The benefit of using the DC sputter system possesses the feasibility and varieties to easily adjusting the optimal rate of a-IGZO for TFTs.

Several material analysis techniques, such as AFM, XRD, SEM, Four-Point Probe, and etc. were utilized to discussing the crystallization, grain size, and sheet resistance of a-IGZO films. Electrical characteristics and conduction mechanisms of a-IGZO TFT devices were also investigated by I-V characteristic analysis and DC bias stress stability. Finally, the ambient effect was discussed. The water molecule absorption dominates the a-IGZO ambient interaction in ambience. The SiNx or SiOx passivation layer was deposited by PECVD at 200 °C. Furthermore, their performance such as environmental stability is investigated.



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中華民國九十九年七月

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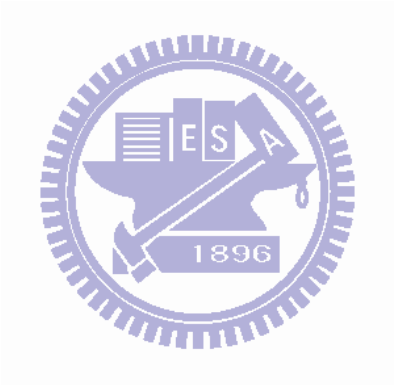

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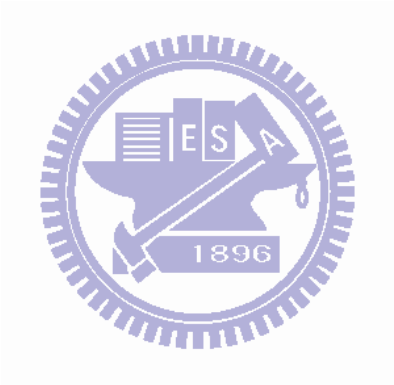

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Chapter 1 Introduction

1.1. General Background

Display technologies have become an important Hi-Tech industry in recent years. Nowadays, the a-Si:H TFT, which is used widely as drivers of Active Matrix Liquid-Crystal Display (AMLCD), has encroached on the territory of the cathode ray tubes. But the deadly issue to the material based on a-Si:H in channel layer in TFTs is low field effect mobility (~ 0.5 cm^2/Vs), photo sensitivity (low band gap about 1.7 eV) and rather high deposition temperature (~ 400 ℃). Since the band gap of a-Si is in visible regime, the photo excited carriers (photo current effect) might make the array of AMLCD out of control. For this reason, the opaque metals to keep a-Si based channel blind from visible light are integrated necessarily. This causes lower opening of AMLCD pixels and more complicated device fabrication.

In terms of power consumption, a large part of the energy of the display is cost from the backlight instruments, such as Cold Cathode Fluorescent Lamps (CCFL). We need to maximize brightness and efficiency, but the opaque TFTs based on a-Si:H restricts the amount of light that can be transmitted to the observers [1]. Then, fabricating high-performance devices is challenging of owing to a trade-off between the brightness and power consumption. For the purpose of enhancing power efficiency, display technology based on organic

light emitting diodes (OLED), including polymers light emitting diode (PLED) are demonstrated for promising for providing lightweight, power efficient, and high brightness performance at reasonable voltage and current levels.

Another advantage of using organic and polymer material is the low fabrication temperature, which can also realize the array on flexible substrate (processing temperature below 200 ℃). But the challenging facing the OLED and PLED is the need of high driving voltage and high driving current for the controlling circuit. However, the driving circuit seems difficult for us to use the a-Si based material for the low mobility limited.

1.2. Amorphous Semiconductors

An important semiconductor feature is the carrier concentration controllability over several orders of magnitude. Amorphous semiconductors are preferred over polycrystalline ones for active layers from the viewpoints of processing temperature and uniformity of device characteristics.

Research on amorphous semiconductors started in 1950s to seek appropriate materials. Fig. 1-1 summarizes the brief history of amorphous semiconductors. The largest impact on electronics is the discovery of hydrogenated amorphous silicon (a-Si:H) by Spear and LeComber in 1975. This is the first material which can control carrier concentration by impurity doping as in crystalline, and it opened a new frontier called ‘Giant Micro-

electronics' which means electronics based on circuits fabricated on a large area substrate. Nowadays, active-matrix flat-panel display (AMFPD) circuits mainly use a-Si:H thin film transistors (TFTs).

Recently, a new electronics is emerging for applications which cannot be fabricated by Si MOS technology. This frontier "flexible electronics" is characterized by electronic circuits fabricated on organic (flexible substrates) instead of inorganic (hard) glasses. The flexible electronic area was born to meet a strong demand for large-area displays because glass substrates are heavy and fragile, and are obviously inconvenient. Amorphous semiconductors are much preferable than crystalline semiconductors for flexible electronics. So far, organic molecule semiconductors have been almost exclusively examined for such applications but their performance and chemical instability are not sufficient for practical applications. Further, the field-effect mobilities of organic TFTs are too low to drive high-resolution, high speed active matrix organic light emitting diode (AMOLED) displays [2].

1.3. Amorphous In-Ga-Zn-O TFTs

Transparent Amorphous oxide semiconductors (AOSs) have attracted keen attention since the high performance thin-film transistors can by obtained by using the amorphous In-Ga-Zn-O (a-IGZO) thin films for the semiconductor layers deposited on plastic substrates by pulse-laser deposition (PLD) at room

temperature [2]. The TFT performance is also confirmed by using the sputter deposition [3], which demonstrates the possibility of the large-area applications. The dependence of the TFT characteristics on the metal composition is investigated in detail by a novel combinational approach [4], since the multi-metal AOSs can take any ratios of the composition.

The average carrier transportation paths in covalent semiconductors, such as a-Si:H, consist of strongly directive sp3 orbitals. The bond angle fluctuation significantly alters the electronic levels, causing high density of deep tail-states, as shown in Fig. 1-2.

In contrast, transparent oxides constituting of heavy post transition metal cations with the $(n-1)d^{10}ns^{0}$ electron configuration, where $n \geq 4$, are the transparent AOS (TAOS) candidates having large mobilities comparable to those of the corresponding crystals. The electron pathway in oxide semiconductor is primarily composed of spatially spread ns orbitals with an isotropic shape, as shown in Fig. 1-2.

The a-ITO、ZTO [6] 、IZO [7] and c-ZnO have high density carrier density, hence is difficult to control the device characteristics. Besides, amorphous In-Ga-Zn-O (a-IGZO) is transparent throughout the visible spectrum; the transmittance is greater than 80 % in visible light region as shown in Fig. 1-3.

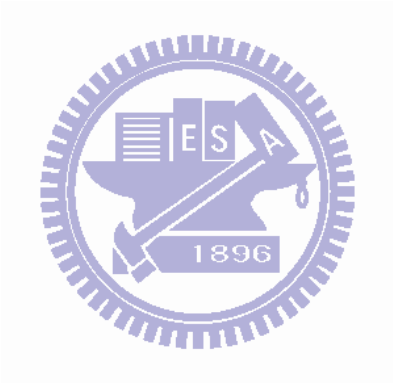
1.4. Motivations

One method to achieve the purpose of efficient power consumption, low fabrication temperature, and the recent progress in transparent oxides which are semiconducting to near-metallic materials is to develop Transparent Conducting Oxide (TCO). TCO has been studied for several years, including Indium Tin Oxide (ITO), Tin Oxide (SnO_2), Zinc Oxide (ZnO), In-Ga-Zn-O (IGZO), and etc.

We study and develop TFTs by substituting traditional amorphous silicon based from a popular TCO material－IGZO as channel layer. Un-doped IGZO film behaves as an n-type transparent semiconductor due to the defects such as oxygen vacancy. It has a wide band gap (2.8 ~ 3.0、3.3 eV) [8, 9] with optical transmission about 80 % transparency in the visible range (400 ~ 900 nm) in the visible portion of the electromagnetic spectrum [10]. The main advantage of using IGZO deals with the fact that it is possible to growth high quality amorphous IGZO films at room temperature [11]. Besides that, thin films based on a-IGZO have been studied for several years for their low cost, low photo sensitivity, no environmental concern, and especially high mobility [12].

In this paper, we report on the properties of amorphous indium gallium zinc oxide (a-IGZO) TFTs fabricated on glass substrates near room temperature using a single target. The resistivity and carrier concentration of a channel in TFTs were controlled by sputtering power of an argon and oxygen mixture

atmosphere. Studies will be undertaken to interpret the growth mechanism of a-IGZO films, crystallographic structure, and electrical properties of the films. We have explored experimentally as functions of the deposition and annealing conditions and defined an optimal deposition condition for TFT. By considering the device characteristics, the mechanisms of film growth and preserve methods will be reported and discussed later.



Chapter 2 Principles and Characterization

2.1. Operation Principle of TFTs

Conventional TFTs compose of a semiconductor layer, a gate insulator layer, and three electrode terminals including gate, source and drain. The bottom-gate-top-contact TFT structure is shown in Fig. 2-1.

Transistors can be classified into the depletion-mode and the enhancement-mode, based on whether drain current flows through TFT when no voltage is applied to gate electrode. For the depletion-mode TFT, when the device is on, drain current flows through the device when no gate voltage is applied. For the enhancement-mode TFT, when the device is off, only leakage current flows through the TFT without applying the gate voltage.

The energy band diagrams through the gate of an n-type enhancement-mode TFT is introduced to explain the three modes of TFT operation, as shown in Fig. 2-2.

When no gate voltage is applied, the semiconductor is in an equilibrium state. When a negative gate bias is applied, delocalized electrons in the channel are repelled from the semiconductor/gate interface and create a depletion region of positive charge, as indicated by the positive curvature in the conduction band and valance band near the insulator shown in Fig. 2-2 (b). When a positive gate bias is applied, delocalized electrons in the channel are attracted to the semiconductor/insulator interface, creating electron

accumulation at the interface, as indicated by the negative curvature in the conduction band and valance band near the insulator in Fig. 2-2 (c). These accumulated electrons at the semiconductor/insulator interface provide a current conduction path and form the channel.

2.2. TFTs Structure

An amorphous In-Ga-Zn-O (a-IGZO) TFT is similar to the corresponding inorganic device that is called the metal-oxide-semiconductor field-effect transistor (MOSFET) in basic structure and operation mode. The three fundamental device components of TFTs are the contact electrodes (source, drain, and gate), the active semiconductor layer, and the dielectric layers. The typical device configurations are shown as Fig. 2-3. The common configuration is the bottom-gate structure with the gate electrode is on the bottom of the dielectric layer. The source and drain electrodes are defined either on top of the semiconductor called top-contact structure or the semiconductor is deposited on top of the source-drain electrode and dielectric layer called bottom-contact structure. The other important device structure is the top-gate, where the gate electrodes are defined on the most top of TFT devices.

Top contact devices have been reported to have superior performance for semiconductors compared with their bottom contact devices. A reason has been suggested that this is a result of reduced contact resistance between the electrode

and the semiconductor layer. In opposite to bottom contact devices, there is an increase of area for charge injection because of the smaller contact resistance in top contact structure. In addition, different structure has individual advantages and disadvantages about fabrication process. They are shown as Table 2-1.

2.3. Electrical Measurement

The device electrical properties were measured by a HP 4156A analyzer in a light-isolated probe station at room temperature. In I_{DS}-V_{GS} measurement, the typical drain-to-source bias was swept from V_{GS} = -10 V to V_{GS} = 20 V. In I_{DS}-V_{DS} measurement, the typical drain-to-source bias was swept from V_{DS} = 0 V to V_{DS} = 20 V.

2.4. Parameter Extraction Method

2.4.1. Determination of the Vth

Threshold voltage (V_{th}) was defined from the gate to source voltage at which carrier conduction happens in TFT channel. V_{th} is related to the “gate insulator thickness” and “the flat band voltage”.

Plenty of methods are available to determine V_{th} which is one of the most important parameters of semiconductor devices. This thesis adopts the constant drain current method, which is, the voltage at a specific drain current NI_D is taken as V_{th}, that is, $V_{th} = V_G (NI_D)$ where V_{th} is threshold voltage and NI_D

stands for normalized drain current. Constant current method is adopted in most studies of TFTs. It provides a V_{th} close to that obtained by the complex linear extrapolation method. Generally, the threshold current $NI_D = I_D/ (W/L)$ is specified at 1 nA in linear region and at 10 nA in saturation region; W and L represent for TFT channel length and width, respectively.

2.4.2. Determination of the Subthreshold Swing

Subthreshold swing (S.S., V/dec.) is a typical parameter to describe the control ability of gate toward channel which is the speed of turning the device on and off. It is defined as the amount of gate voltage required to increase and decrease drain current by one order of magnitude. S.S. is related to the process, and is irrelevant to device dimensions. S.S. can be lessened by substrate bias since it is affected by "the total trap density including interfacial trap density and bulk density". In this study, S.S. was defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude (from 10^{-8} A to 10^{-10} A). The threshold current was specified to be the drain current when the gate voltage is equal to V_{th}.

2.4.3. Determination of the Field-Effect Mobility

Typically, the field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain bias (V_D = 0.1 V). The TFT transfer I-V

characteristics can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D{}^2] \quad (2\text{-}1)$$

Where

C_{OX} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If V_D is much smaller than $V_G - V_{TH}$ (i.e. $V_D << V_G - V_{th}$) and $V_G > V_{th}$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{th})V_D \quad (2\text{-}2)$$

The transconductance is defined as:

$$g_m = \mu_{FE} C_{ox} \frac{W}{L} V_D \quad (2\text{-}3)$$

Thus,

$$\mu_{FE} = \frac{L}{C_{OX} W V_D} g_m \quad (2\text{-}4)$$

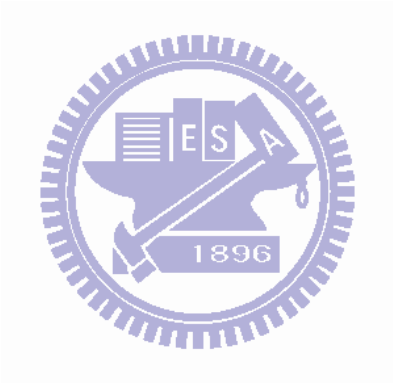
2.4.4. Determination of On/Off Current Ratio

Drain on/off current ratio is another important factor of TFTs. High on/off current ratio represents not only the large turn-on current but also the small off current (leakage current). It affects AMLCD gray levels (the bright to dark state

number) directly.

There are many methods to determine the on and off currents. The practical one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage equal to 10 V. The on/off current ratio is expressed as：

$$\frac{I_{DS\ max,on}}{I_{DS\ max,off}} \Big|_{V_D=10\ V} \qquad (2\text{-}5)$$



Chapter 3 Experimental Procedure

3.1. TFT Fabrication

Table 3-1 shows experimental flow path in my experiment. There were seldom papers about this deposition method for depositing a-IGZO film for TFTs utility. Because of the innovation of DC sputter, we got to reference lots of surveys on other deposition and treatment methods. Finally, we defined a suitable deposition condition.

3.1.1. a-IGZO TFT Device Fabrication

In my experiments, the fabrication and properties of bottom-gate-type (BG/BC) thin-film transistors using a-IGZO films as channel layer will be described. The cross-section view of a-IGZO TFTs fabricated on glass substrates is shown schematically in Fig. 2-3 (c). We follow TFT fabrication in Taiwan. And it used G2 glass that size is 370 × 470 mm. Table 3-2 shows a-IGZO TFT device fabrication flow path in my experiment. The detail descriptions are as followed：

(a) **Substrate Cleaning**

Step 1: Clean glass substrate by DI water

Step 2: Clean glass substrate by DHF solution

Step 3: Clean glass substrate by DI water.

Step 4: Dry Clean glass substrate by N^2 gas.

(b) Gate Metal formation

In Fig. 3-1, we used the sputter to deposit MoW layer of 500 Å on glass substrate. After the deposition, gate region were defined by lithography process, which is the first mask. Then the patterned gate was formed by dry etching. After metal gate forming, stripper solution in supersonic oscillator was used to eliminate passive photoresist.

(c) Gate dielectric formation.

In Fig. 3-2, as metal gate had been defined, the glass substrate was sent to chamber plasma-enhanced chemical-vapor deposition system to deposit 1000 Å SiNx as gate dielectric. After the deposition, gate dielectric was defined by photolithography process, which is the second mask. Then the patterned gate dielectric was formed by dry etching. After gate dielectric forming, stripper solution in supersonic oscillator was used to eliminate passive photoresist.

(d) **Source-drain isolation formation**

In Fig. 3-3, we used the sputter to deposit layer as ITO 1000 Å on gate dielectric. After the deposition, gate region were defined by lithography process, which is the third mask. Then the patterned gate was formed by wet etching.

After metal gate forming, stripper solution in supersonic oscillator was used to eliminate passive photoresist.

(e) **Active region defined**

In Fig. 3-4, we used the metal pad as a hard mask to defined active region. Finally, a 500 Å thick a-IGZO (In:Ga:Zn:O = 1:1:1:4) thin-film was deposited by sputter at room temperature. The DC sputtering was used for reducing the charges accumulated on the a-IGZO target. The deposition was done with a continuously gas flow of argon and oxygen without intentional substrate heating.

The cross-sectional and planed view of a-IGZO TFTs structure are shown schematically in Fig. 3-5 (a) and (b), respectively. The channel width (W) of the device were of 500 μm and the channel lengths (L) are 30, 50 and 60 μm. and the width/Length ratio of our a-IGZO TFTs was about 16.66, 10, and 8.33.

3.1.2. DC Sputtering

DC sputtering has the advantage of higher deposition rate and is less expensive than RF sputtering. A DC sputtering system is shown in Fig. 3-6, the substrate is located above the target and acts as the anode. DC sputtering is commonly applied to deposit conductive materials.

3.2. Methods of Depositing a-IGZO Films

3.2.1. The Taguchi Method

We expect to find the process parameter of excellent uniformity by using Taguchi Method. It also helped us to understand the characteristics of N-Slot ICP system. The main purpose is to apply in one set optimization parameter of the product manufacturing process physically at adjusting. The uniformity is below 10 %, and the Sheet electric resistance then needs in $10^{7\sim9}$ Ω/□. Residual plots for thickness show in Fig. 3-7. Residual plots for uniformity show in Fig. 3-8.

3.2.2. Changing of DC Power in Sputter System

a-IGZO films were prepared by reactive pre-sputtering with a direct current power in mixed argon and oxygen gas at atmosphere at a constant pressure of 3×10^{-3} Torr. As the sputtering apparatus a diode-type reactor equipped with a substrate holder, DC power supply, gas lines, vacuum gauges, and a pumping system was used. By using a machine pump, a residual pressure of the order of 2×10^{-6} Torr was achieved. A square of Indium-Gallium-Zinc-Oxide 300 × 540 mm dimension was used as a target.

We change the DC power of sputtering to adjust the optimal thickness and uniformity of our a-IGZO films. Pre-sputtering is used to clean the surface of

IGZO target. The results are listed on the Table 3-3.

The characteristics of a-IGZO film can be controlled by varying the deposition conditions. When the DC power is low, a-IGZO film is not applicable for TFT channel layer because the film Uniformity is bad. When DC power is high (over 2.3 kW), a-IGZO film becomes thickness too thick. In intermediate DC power 2.3 kW, a-IGZO film is suitable for TFT channel layer. it is one of the key parameter to control the uniformity of TFT behavior. They are shown in Fig. 3-9. So we define the optimal power condition on sputtering as 2.3 kW.

3.2.3. Changing of substrate move rate in Sputter System

We change the substrate move rate of sputtering to adjust the optimal thickness and uniformity of our a-IGZO films. The results are listed on the Table 3-4.

The characteristics of a-IGZO film can be controlled by varying the deposition conditions. When the substrate move rate is low, a-IGZO film is not applicable for TFT channel layer because the film thickness is too thick. When substrate move rate is high (over 400 mm/min), a-IGZO film becomes thickness too thin. In intermediate substrate move rate 400 mm/min, a-IGZO film is suitable for TFT channel layer. it is one of the key parameter to control the uniformity of TFT behavior. They are shown in Fig. 3-10. So we define the optimal substrate move rate condition on sputtering as 400 mm/min.

3.2.4. Adjusting the Rate of Oxygen

The carrier source of Si and metal oxide is shown in Fig. 3-11. For Si, the carriers are resulted from impurity doping as shown in Fig. 3-11 (a). Electrons dominate the carrier transport for phosphorous-doped Si. Carrier transport is dominated by holes for boron-doped Si. For metal oxide, the carrier concentration is related to the oxygen vacancy; one oxygen vacancy provides two electrons, as shown in Fig. 3-11 (b).

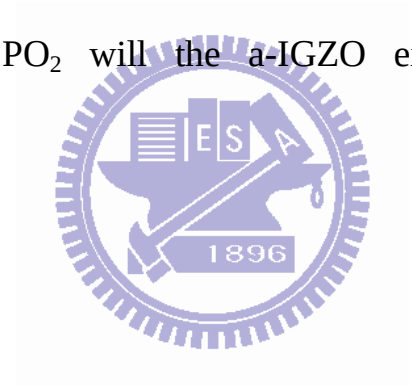
Because of the oxygen vacancies in the a-IGZO film, a-IGZO TFT characteristics are strongly associated with the a-IGZO film. The reactions on film surface dominate the threshold voltage (V_{th}) shift. The oxygen absorption changes the carrier concentration. The oxygen absorption forms depletion layer, resulting in V_{th} shift.

The oxygen absorption accompanies partial charge transfer, V_{th} varies at different oxygen flow rate implies the change in carrier concentration during the absorption and desorption processes. When the oxygen flow rate increases, the channel carrier concentration decreases because of less oxygen vacancies in a-IGZO film. Therefore, higher voltage is needed to turn on the channel.

In our experiments, several oxygen flow rates (0.1, 0.45, 0.8, 2, 3, 4, and 5 sccm) were adopted so as to prepare the a-IGZO film with various physical properties. The results are listed on Table 3-5.

The electrical characteristics of a-IGZO film can be controlled by varying

the deposition conditions (Ar flow rate and O_2 flow rate). When the oxygen flow rate is low, a-IGZO film is not applicable for TFT channel layer because the film conductivity is high. When oxygen flow rate is high (over 3 sccm), a-IGZO film becomes insulator. In intermediate oxygen flow rate (0.5 ~ 2 sccm), a-IGZO shows semiconductor characteristics and is suitable for channel layer. It is considered that the low oxygen flow rate increases the electrical conductivity of the deposited film [2, 13]. In the case of Ar gas flow, even though it is not strongly related to electrical property of a-IGZO film, it is one of the key parameter to control the uniformity of TFT behavior. Fig. 3-12 shows that only in a proper range of PO_2 will the a-IGZO exhibit the semiconductor characteristics [14].



Chapter 4 Results and Discussions

4.1. Thin film Analysis of Material

4.1.1. Four-Point Probe

Resistance measurement was practiced in this study to confirm the film qualities of our dual metal layers samples. The samples were measured 9 points on the glass of G2 size (370 × 470 mm).

In the sheet resistance measurement, several resistances need to be considered, as shown in Fig. 4-1 (a). The probe has a probe resistance Rp. It can be determined by shorting two probes and measuring their resistances. At the interface between the probe tip and the semiconductor, there is a probe contact resistance, Rcp. When the current flows from the small tip into the semiconductor and spreads out in the semiconductor, there will be a spreading resistance, Rsp.

Finally, the semiconductor itself has a sheet resistance Rs. The equivalent circuit for the measurement of semiconductor sheet resistance by using the four-point probe is shown in Fig. 4-1 (b), and (c). Two probes carry the current and the other two probes sense the voltage. Each probe has a probe resistance Rp, a probe contact resistance Rcp and a spreading resistance Rsp associated with it. However, these parasitic resistances can be neglected for the two voltage probes because the voltage is measured with a high impedance voltmeter, which

draws very little current. Thus the voltage drops across these parasitic resistances are insignificantly small. The voltage reading from the voltmeter is approximately equal to the oltage drop across the semiconductor sheet resistance. By using the four-point probe method, the semiconductor sheet resistance can be calculated:

$$R_s = F\frac{V}{I}$$

Where V is the voltage reading from the voltmeter, I is the current carried by the two currentcarrying probes, and F is a correction factor. For collinear or in-line probes with equal probe spacing, the correction factor F can be written as a product of three separate correction factors:

$$F = F1\ F2\ F3$$

F1 corrects for finite sample thickness, F2 corrects for finite lateral sample dimensions, and F3corrects for placement of the probes with finite distances from the sample edges. For very thin samples with the probes being far from the sample edge, F2 and F3 are approximately equal to one (1.0), and the expression of the semiconductor sheet resistance becomes:

$$R_s = \frac{\pi}{\ln 2}\frac{V}{I}$$

The four-point probe method can eliminate the effect introduced by the probe resistance, probe contact resistance and spreading resistance. Therefore it has more accuracy than the two point probe method [15]. The a-IGZO film sheet resistance is shown in Fig. 4-2.

4.1.2. X-ray Diffraction (XRD)

X-ray diffraction (XRD) is a rapid analytical technique primarily used for phase identification of a crystalline material and can provide information on unit cell dimensions. The analyzed material is finely ground, homogenized, and average bulk composition is determined. X-ray diffraction is based on constructive interference of monochromatic X-rays and a crystalline sample. These X-rays are generated by a cathode ray tube, filtered to produce monochromatic radiation, collimated to concentrate, and directed toward the sample. The interaction of the incident rays with the sample produces constructive interference (and a diffracted ray) when conditions satisfy Bragg's Law ($n\lambda = 2d \sin \theta$). This law relates the wavelength of electromagnetic radiation to the diffraction angle and the lattice spacing in a crystalline sample. These diffracted X-rays are then detected, processed and counted. By scanning the sample through a range of 2θ angles, all possible diffraction directions of the lattice should be attained due to the random orientation of the powdered material. Conversion of the diffraction peaks to d-spacings allows identification of the mineral because each mineral has a set of unique d-spacings. Typically, this is achieved by comparison of d-spacings with standard reference patterns [16].

Fig. 4-3 show the measurement of as-deposited a-IGZO film on a glass substrate (G2) with different oxygen flow rates (0.5, 1, and 2 sccm). This plot presents the non-crystallization characteristics of film.

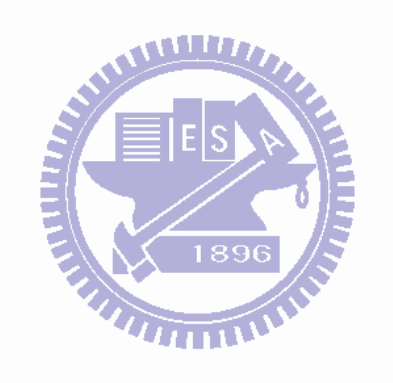
4.1.3. Atomic Force Microscope (AFM)

The Digital Instruments Dimension SPA500 atomic force microscope (AFM) was used to characterize the surface morphology of the a-IGZO thin films. The tapping-mode scanning prevents the probe from damaging the sample surface and can get more precise surface topographic information. In the tapping-mode, the probe oscillates up and down regularly. The cantilever vibrates at various frequencies depending on the magnitude of the van der Waals force between the cantilever tip and the sample surface. A laser beam reflected by the cantilever detects the tiny vibration of the cantilever, as shown in Fig. 4-4. The feedback amplitude and the phase signals of the cantilever were recorded by the computer. The amplitude signals provide the morphology information and the phase signals reveal the material information [17].

AFM provides three-dimensional surface topography at nanometer lateral and sub-angstrom vertical resolution on a-IGZO film. Fig. 4-5 and Fig. 4-6 show the atomic force topography of a-IGZO film (thickness of 500 Å) without and with annealing in 250 ℃ (1 hr), respectively. Use to scan size is 5 μm of square and scan rate is 0.8 Hz. The root-mean-square for roughness of surface on the a-IGZO film before annealing is 5.510 Å and after annealing is 8.414 Å. The roughness information of surface morphology of without annealing is better than annealing.

4.1.4. SEM

Fig. 4-7 and Fig. 4-8 show the cross-section view image of a-IGZO film after DC sputtering deposition before and after 250 °C (1 hr) thermal treatment, respectively, and reveals the grain size increases with temperature. Fig. 4-9 and Fig. 4-10 schematics the a-IGZO film before and after 250 °C (1 hr) thermal treatment respectively. It reveals that the grain size increases with temperature.



4.2. The a-IGZO TFTs Analysis of Electrical Characteristics

4.2.1. The Effects of Post-Annealing on a-IGZO TFTs

A remarkable advantage of AOSs (e.g. IGO, ZTO, ZIO) is that AOSs works as active layers in semiconductor devices even if these are formed at a low temperature including room temperature (RT) without any defect passivation treatment. However, it has also been recognized that a post-deposition thermal annealing at e.g. ≧ 300 °C improves TFT stability and performances; including better saturation current, smaller hysteresis, and V_{th} [18-20].

The post-annealing effect on device with 1KÅ SiNx gate insulator is shown in Fig. 4-11. V_{th} shifts positive after post-annealing because post-annealing leads to the lattice structure rearrangement, structural relaxation, and the improved a-IGZO bonding. Post-annealing improves the channel/dielectric interface; and the charge trapping defects are decreased. V_{th} shifts positive to be near 3.44 V after the thermal treatment. Table 4-1 shows the characteristics of devices without and with thermal annealing.

4.2.2. The Effects of DC power on a-IGZO TFTs

The a-IGZO TFTs were operated in enhancement mode. The SiNx gate insulator is 1000 Å thickness. Fig. 4-12 (a) shows the oxygen rate as 0.5 sccm I_D-V_G. Fig. 4-12 (b) shows the oxygen rate as 0.65 sccm I_D-V_G. The sample was fabricated in DC power 1, 1.5, and 2.3 KW and argon/oxygen rate as (50 / 0.5, and 0.65 sccm) by sputtering. The overall transfer characteristics exhibit almost parallel shifts with little change in other device parameters such as mobility and subthreshold swing. After DC power 2.3 kW, the shift is saturated and we can see electrical characteristics have better others. Table 4-2 show the device characteristics were measured semiconductor parameter after thermal annealing.

4.2.3. The Effects of Oxygen Flow Rate on a-IGZO TFTs

Good electrical characteristics like large on-state drain current, small threshold voltage, and low threshold voltage were obtained when the oxygen flow rate is 0.7 sccm, as shown in Fig. 4-13. The sample was fabricated in DC power 2.3 KW and argon/oxygen rate as (50 / 0.65, 0.7, 0.75, and 0.85 sccm) by sputtering. We can obviously observe the similar electrical performance they appeared. After oxygen rate 0.7 sccm, we can see mobility and subthreshold swing have better others. Table 4-3 show the device characteristics were measured semiconductor parameter after thermal annealing.

4.2.4. Summary

Post-annealing improves the bonding in a-IGZO because of the semiconductor/insulator interface modification and local atomic rearrangement and the threshold voltage can be adjusted to be near 3.4 V.

The DC power improves the film density in a-IGZO because of the semiconductor modification and local atomic rearrangement and the device electrical properties have better.

The oxygen flow rate was varied to examine oxygen absorption effect. The V_{th} changes with the oxygen flow rate. The oxygen vacancies provide electrons and increase the channel carrier concentration, leading to a bigger mobility.

4.3. The a-IGZO TFTs Reliability Analysis

4.3.1. The DC (10 V) Bias stress of different active layer thivkness (500 Å, 1 kÅ, and 2 kÅ)

To investigate the characteristics of a-IGZO TFTs having various channel thicknesses, we varied the a-IGZO channel thickness, i.e., 500 Å, 1 kÅ, and 2 kÅ, by controlling the deposition time during sputtering growth. The DC bias stress stability of a-IGZO TFT was also investigated. During the stress, a positive DC voltage was applied to the gate while the source and the drain were grounded. The a-IGZO TFT behavior under stress is shown in Fig. 4-14, which reveals that the transfer curves of the a-IGZO TFT shift generally to the same direction as the gate bias. Fig. 4-14 (a) shows the results of a-IGZO TFT under positive gate bias stress (+10 V) for 50000 seconds. The transfer curves shift to positive voltage direction for longer time. The Fig. 4-14 (b) is the extracted electrical parameter of V_{th} and SS from Fig.4-14 (a). We can see the delta V_{th} have about 1.59 V positive shift behavior and SS was similar.

The TFT behavior under stress is shown in Fig. 4-15, which reveals that the transfer curves of the a-IGZO TFT shift generally to the same direction as the gate bias. Fig. 4-15 (a) shows the results of a-IGZO TFT under positive gate bias stress (+10 V) for 50000 seconds. The transfer curves shift to the positive voltage direction as the gate bias as expected. The Fig. 4-15 (b) is the extracted electrical parameter of V_{th} and SS from Fig. 4-15 (a). We can see the delta V_{th}

have about 0.75 V positive shift behavior and S.S. was similar.

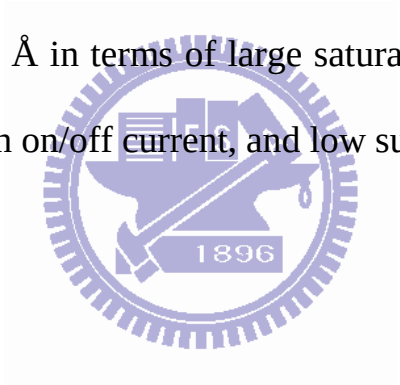
The TFT behavior under stress is shown in Fig. 4-16, which reveals that the transfer curves of the a-IGZO TFT shift generally to the same direction as the gate bias. Fig. 4-16 (a) shows the results of a-IGZO TFT under positive gate bias stress (+10 V) for 50000 seconds. The transfer curves shift to positive voltage direction for longer time. The Fig. 4-16 (b) is the extracted electrical parameter of V_{th} and SS from Fig. 4-16 (a). We can see the delta V_{th} have about 0.46 V positive shift behavior and SS was similar.

4.3.2. Summary

As shown in Fig. 4-17, increasing the thickness of the active layer leads to a higher off current. The reason for this is that the off current is proportional to the channel layer thickness, as indicated in the following equation: I_{DS} [off] = (σ Wt/L)V_{DS}, (σ : electrical conductivity, t: thickness of active layer, W: width of channel, L: length of channel). The on-current values are not significantly changed regardless of the channel thickness. The increase of off current and similar on current resulted in a decrease of the on/off current ratio with increasing the active layer thickness. The on/off current ratios for the TFTs with 50, 100, and 200 Å thick active semiconductor were 2.89E+08, 1.35E+08, and 1.34E+08, respectively. The corresponding field-effect mobilities of the TFTs with 50, 100, and 200 Å thick a-IGZO layers were 4.77, 4.75, and 4.73 cm^2/Vs,

respectively. The shape of the transfer curve and the behavior of the mobility change are similar to the results reported by Suresh et al [21, 22].

The V_{th} always shows positive values and is slightly increased with time under the experiment. This demonstrates that the a-IGZO TFT remains in enhancement-mode operation. The threshold voltage shift may be caused by the bias stress during measurement, resulting in the defect state creation in the channel [23-25]. Powell et al. suggested that deep-state defect creation is dependent on stress time and strongly affected by temperature in a-Si/H TFTs [26]. Based on the above results, we concluded that the optimum a-IGZO channel thickness was 500 Å in terms of large saturation current, low threshold voltage, high mobility, high on/off current, and low subthreshold swing.



4.4. The a-IGZO TFTs passivation Environmental stability analysis

4.4.1. The Effects SiNx 1 kÅ and SiOx 1 kÅ (rich and less H atomic) on a-IGZO TFTs

The effects of the passivation process on the a-IGZO annealed devices were investigated. We employed silicon nitride as a passivation layer. We were deposited by PECVD at 200 °C, with 160 W rf power and 0.9 Torr process pressure. For deposition of the silicon nitride layer, H_2 flow rate was varied at 700 sccm. The device characteristics were measured semiconductor parameter analyzer before and after the passivation process and measured again after additional thermal annealing in air at 250°C for 1 h.

Fig. 4-18 shows the transfer characteristics of the a-IGZO TFTs passivation with silicon nitride. The characteristics were measured before and after the post-annealing. It is observed that the drain current of the nitride-passivation a-IGZO TFT is not modulated by gate voltage and is higher than that of the oxide-passivation TFT.

We employed silicon oxide (rich H atomic) as a passivation layer. We were deposited by PECVD at 200 °C, with 700 W rf power and 1 Torr process pressure. For deposition of the silicon oxide layer, N_2O flow rate was varied at 2500 sccm for a fixed SiH_4 flow rate of 50 sccm. The device characteristics were

measured semiconductor parameter analyzer before and after the passivation process and measured again after additional thermal annealing in air at 250 °C, and 300 °C for 1 hr.

Fig. 4-19 shows the transfer characteristics of the a-IGZO TFTs passivation with silicon oxide (rich H atomic). The characteristics were measured before and after the thermal annealing. It is observed that the drain current of the unannealed a-IGZO TFT is not modulated by gate voltage and is higher than that of the post-annealed a-IGZO TFT. The annealed at 250 °C a-IGZO TFT shows poor characteristics such as a saturation mobility (μ) of 4.25 cm^2/Vs, a subthreshold voltage swing (S.S.) of 0.36 V/decade, and a threshold voltage (V_{th}) of -6.24 V. By contrast, the annealed at 300 °C TFT shows much improved characteristics such as μ of 4.56 cm^2/Vs, S.S. of 0.18 V/decade, and V_{th} of -2.58 V. Table 4-4 shows the device characteristics were measured semiconductor parameter before and after thermal annealing.

We employed silicon oxide (less H atomic) as another passivation layer. We were deposited by PECVD at 200 °C, with 700 W rf power and 1 Torr process pressure. For deposition of the silicon oxide layer, N_2O flow rate was varied at 1000 sccm for a fixed SiH_4 flow rate of 20 sccm. The device characteristics were measured semiconductor parameter analyzer before and after the passivation process and measured again after additional thermal annealing in air at 250 °C, and 300 °C for 1 hr.

Fig. 4-20 shows the transfer characteristics of the a-IGZO TFTs passivation with silicon oxide (less H atomic). The characteristics were measured before and after the thermal annealing. It is observed that the drain current of the unannealed a-IGZO TFT is not modulated by gate voltage and is higher than that of the post-annealed a-IGZO TFT. The annealed at 250 °C a-IGZO TFT shows characteristics such as a saturation mobility (μ) of 4.04 cm^2/Vs, a subthreshold voltage swing (S.S.) of 0.11 V/decade, and a threshold voltage (V_{th}) of 0.77 V. By contrast, the annealed at 300 °C TFT shows much improved characteristics such as μ of 4.42 cm^2/Vs, S.S. of 0.11 V/decade, and V_{th} of 0.07 V. Table 4-5 show the device characteristics were measured semiconductor parameter before and after thermal annealing.

Fig. 4-21 shows the environmental stability of a-IGZO TFTs. The devices were stored in humidity 40 % RH, 25 °C and measured after some time periods. Many cases show that the oxide semiconductors are sensitive to the humidity. One expect that the chemisorbed water molecules in the oxide semiconductors may donate electrons, and changing (increasing) the intrinsic conductivity [27]. Here two types of devices are compared, one none passivation layer and the other uses SiOx (less H atomic). As shown in Fig. 4-21 (a), the transfer curves of a-IGZO TFT with none passivation shifted voltage largely. Table 4-6 show the device characteristics with none passivation. This phenomenon may be due to the poor water impermeability of the a-IGZO film. The environmental

stability was improved remarkably for the devices with SiOx (less H atomic) as passivation. No significant changes were observed in the transfer curves of a-IGZO TFT using SiOx (less H atomic) as passivation layer, as shown in Fig. 4-21 (b). Table 4-7 show the device characteristics with SiOx (less H atomic) passivation.

4.4.2. Summary

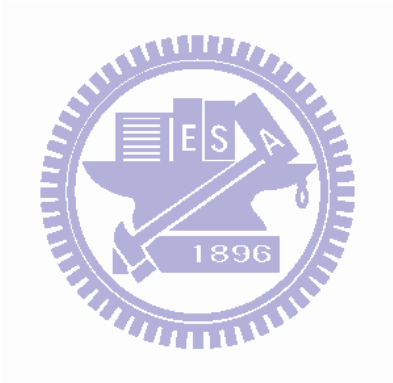
In the contrast, the oxide-passivated TFT exhibits normal transfer characteristics. This difference can be explained as follows: During the deposition of the passivation layer by PECVD, the channel surface of a-IGZO is exposed to plasma including hydrogen, nitrogen, and oxygen radicals. In case of nitride passivation, a large amount of hydrogen provided from SiH_4 and NH_3 gases is contained in the plasma and is resultantly incorporated in the deposited nitride film. It is known that the hydrogen radical easily reduces an oxide film and the reduction reaction is dependent upon the substrate temperature and the partial pressure of hydrogen [28]. Fig. 4-22 presents the SEM cross-sectional view of a-IGZO films treated by hydrogen plasma at none and at 700 sccm / 340 W, respectively. When the a-IGZO films are exposed to hydrogen plasma, reduced indium concentrates on localized area through the surface diffusion and agglomerates. Consequently, the a-IGZO film becomes more conductive by oxygen reduction during the deposition of the nitride passivation layer, even

though the bond breakage due to ion bombardment is cured by the final thermal annealing. The silicon oxide has relatively low hydrogen content and is deposited in oxygen-rich plasma. So we expected that if the physical damage by the ion bombardment could be minimized and enough oxygen was supplied to the back surface of the a-IGZO film, the channel current might decrease and the threshold voltage would shift to the positive direction.

The characteristics were measured after the thermal annealing in air at 250 °C, and 300 °C for 1 hr. From electrical characteristic, the a-IGZO TFT with SiOx (less H atomic) passivation is better than that with SiOx (rich H atomic) passivation. When hydrogen ions are implanted in a film, it is suggested that incorporation of hydrogen-related species would influence largely threshold voltages, on-to-off current ratios, and stability of TFTs [29]. Fig. 4-23 shows the SEMS depth profiles of SiOx deposited with the flow rate of SiH_4 at 50 and 20 sccm, respectively. The hydrogen atoms diffuse into the a-IGZO layer deposited with SiH_4 at 50 sccm is more than that at 20 sccm.

The a-IGZO film is sensitive to the surface absorption of oxygen and water molecules. When the oxygen molecules in atmosphere fill into the oxygen vacancies, they decrease the electrical conductivity of a-IGZO film. In other view, the oxygen vacancies can be assumed as holes and they can assist the electrical conduction of a-IGZO film. Passivation is the key factor for sustaining the a-IGZO TFT subthreshold properties and the devices reliability. The V_{th} for both devices shifted after their exposure to humidity. Furthermore, the V_{th} shift

was accompanied by the rapid increase of the on/off current ratio from 4.41E+09 to 1.94E+07. This suggests that H_2O adsorption indeed donates a partial negate charge to the a-IGZO surface with either molecular or hydroxyl forms. The similar formation of extra electron carriers has been attributed to the donation of electrons (called the “donor effect”) from the chemically adsorbed H_2O molecules to the surface of oxides such as ZnO [30-33].



Chapter 5 Conclusion

We have developed an optimized deposition condition for sputtering a-IGZO semiconductor film and succeeded to fabricate a IGZO-based transparent thin film transistor with bottom-gate structure. The optimal conditions for depositing the a-IGZO film by DC sputtering at room temperature is under the atmosphere of (argon/oxygen) mixture (50/0.7) sccm. With the definition of hard mask, a-IGZO active regions can be patterned exactly and completing TFT device fabrication.

In the first part, we have developed an optimized deposition condition for sputtering a-IGZO semiconductor film.

In the second part, Post-annealing improves the crystallinity in a-IGZO because of the semiconductor/insulator interface modification and local atomic rearrangement. As a result, the field mobility can be up to 3.07 cm^2/Vs and the threshold voltage can be adjusted to 3.44 V. The DC sputter power improves the crystallinity in a-IGZO. As a result, the field mobility can be up to 3.09 cm^2/Vs and the threshold voltage can be adjusted to 3.77 V. The oxygen flow rate was varied to examine oxygen absorption effect. V_{th} is smaller for smaller oxygen flow rate, since the depletion layer underneath the absorption layer forms due to the charge transfer between absorbed O_2 and a-IGZO forms. Our device performance is appropriate for display applications.

In the third part, to investigate the characteristics of a-IGZO TFTs having

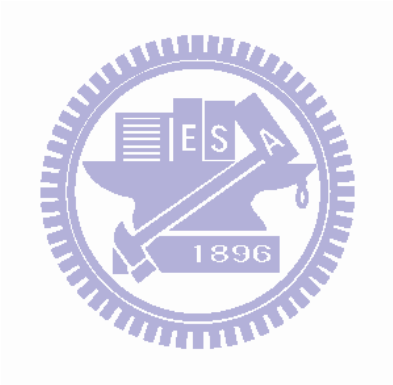
various channel thicknesses, we varied the a-IGZO channel thickness, i.e., 50, 100, and 200 nm, by controlling the deposition time during sputtering growth.

The V_{th} always shows positive values and is slightly increased with time under the experiment. This demonstrates that the a-IGZO TFT remains in enhancement-mode operation. The threshold voltage shift may be caused by the bias stress during measurement, resulting in the defect state creation in the channel. However, the Hall mobility of the a-IGZO films increases with increasing carrier concentration contrary to conventional crystal semiconductors, as reported in earlier works [34, 35]. To clarify the correlation between the field-effect mobility of InGaZnO4 films and variations of carrier concentration by manipulating the thickness of the a-IGZO channel layer, further in-depth study is required.

In the fourth part, the effects of different passivation materials on a-IGZO TFT were investigated. The adopted materials are SiNx, SiOx (rich H atomic), and SiOx (less H atomic). The direct SiNx passivation on a-IGZO TFT by the PECVD process will not be adopted since the hydrogen doped SiNx will increase the a-IGZO TFT conductivity. In our proposed TFT structure with passivation layer, an hydrogen less SiOx channel protection layer on the a-IGZO thin film can prevent a-IGZO TFT from losing the oxygen and water molecules.

The adoption of the passivation layer prevents the degradation under humidity. Passivation is the key factor for sustaining the subthreshold properties and devices reliability. Based on our previous results, we will further

study the effects of organic/inorganic passivation on a-IGZO TFTs. Passivation for a-IGZO TFT opens a potential way to fabricate high performance a-IGZO TFT with good reliability in ambience.



Figures

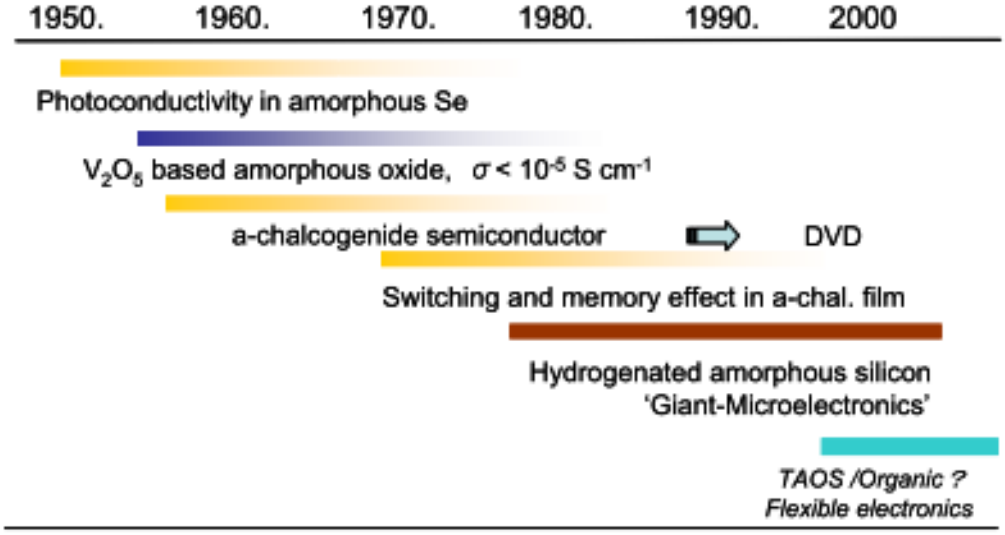


Fig. 1-1 History of amorphous semiconductors on new fields.[2]

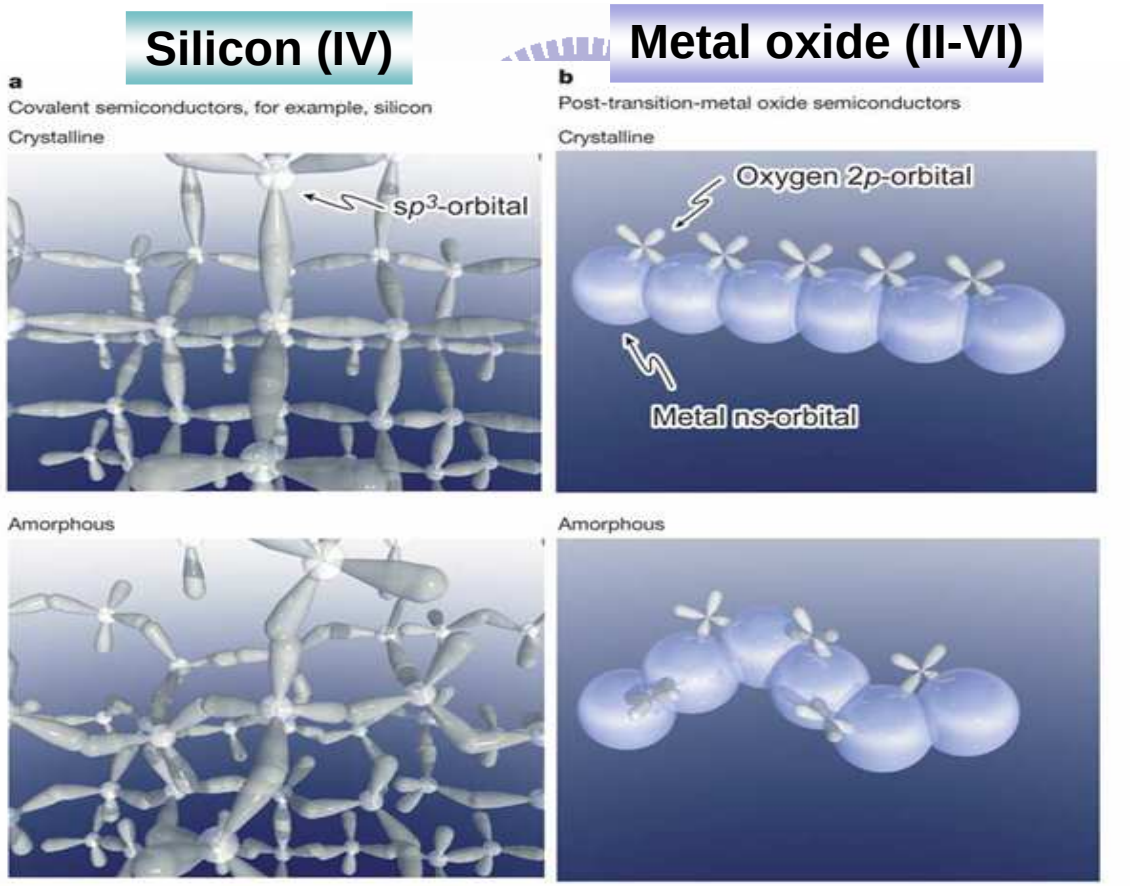


Fig. 1-2 Schematic orbital drawing of electron pathway (conduction band bottom) in conventional silicon-base semiconductor and ionic oxide semiconductor.[5]

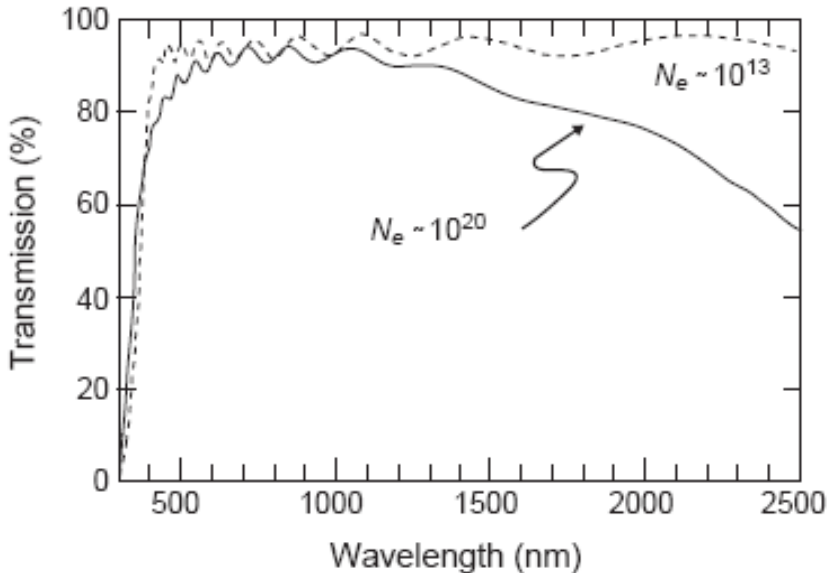


Fig. 1-3 Optical transmittance of a-IGZO film in visible light region.[10]

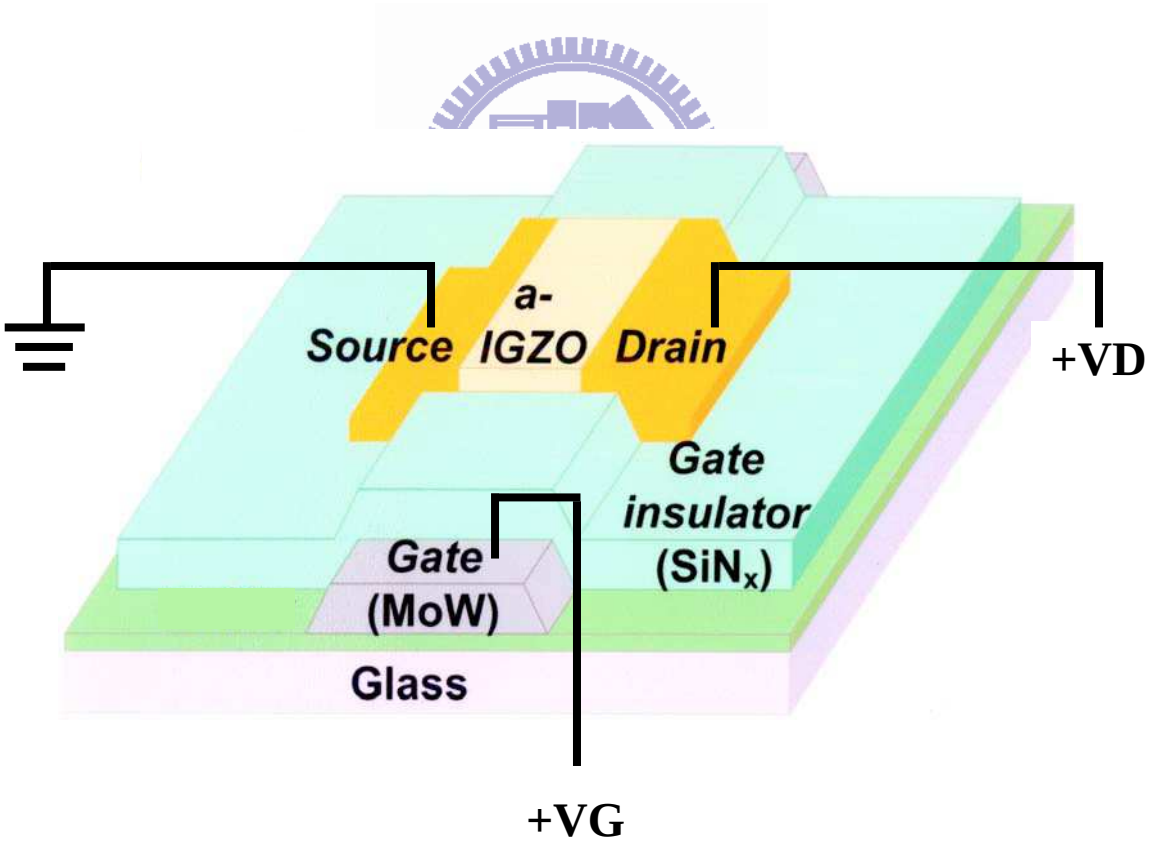


Fig. 2-1 Bottom-gate-bottom-contact TFT structure.

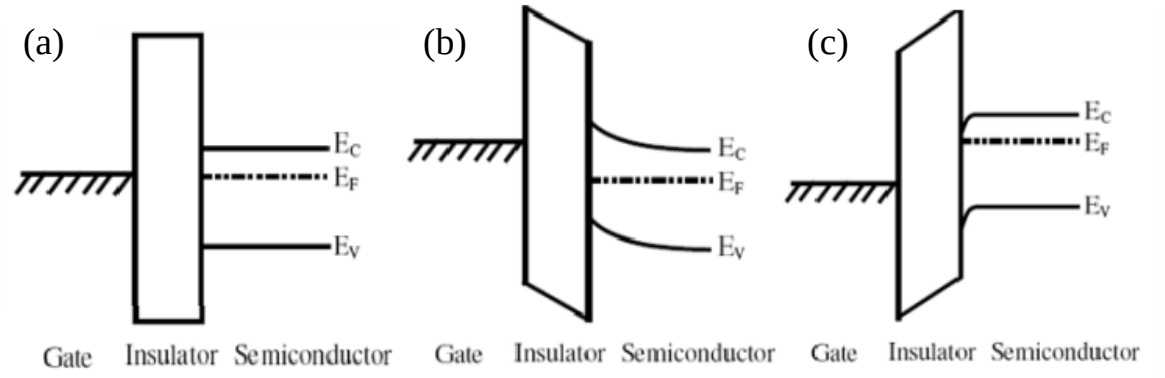


Fig. 2-2 The semiconductor energy band diagram when (a) unbiased, (b) negative gate voltage bias, and (c) positive gate voltage bias.

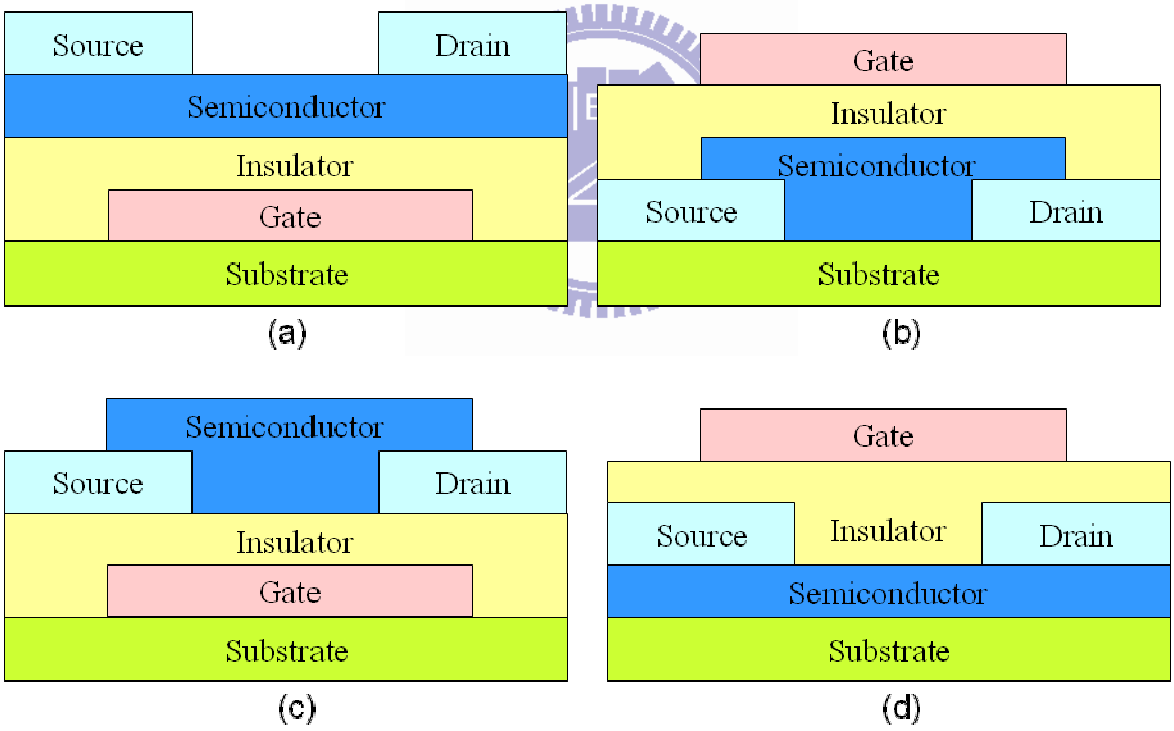


Fig. 2-3 IGZO TFT device configurations when (a) bottom gate top contact, (b) top gate bottom contact, (c) bottom gate bottom contact, and (d) top gate top contact.

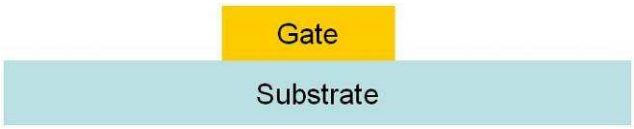


Fig. 3-1 The gate metal of MoW deposition process.

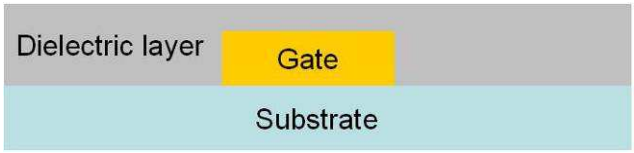


Fig. 3-2 The gate metal of SiNx deposition process.

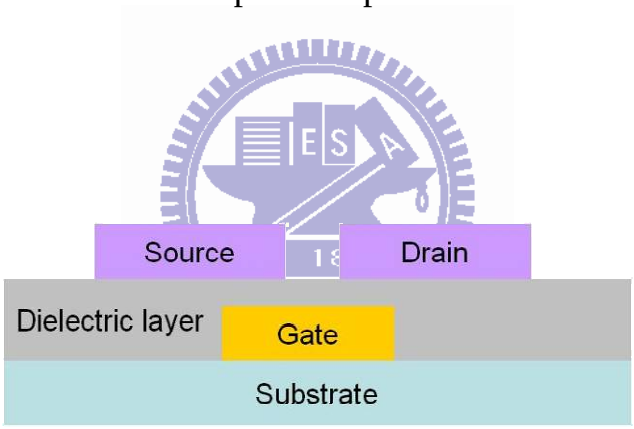


Fig. 3-3 The S/D metal of ITO deposition process.

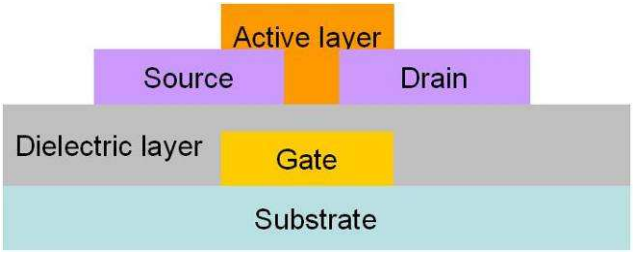
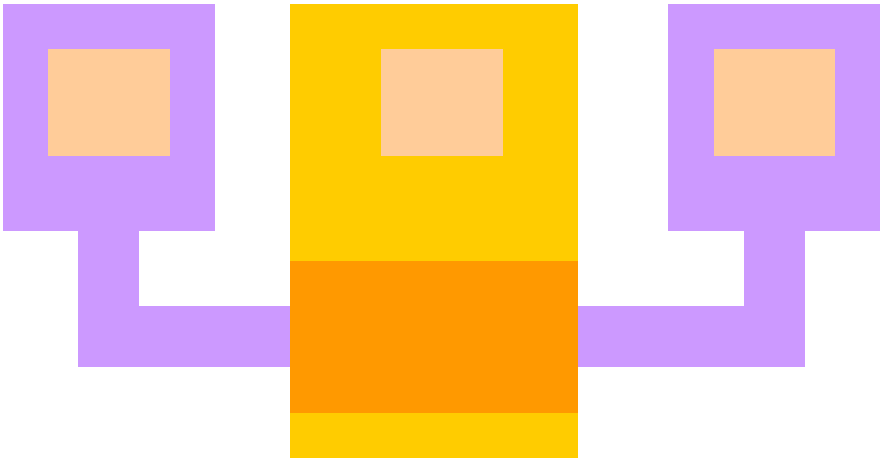
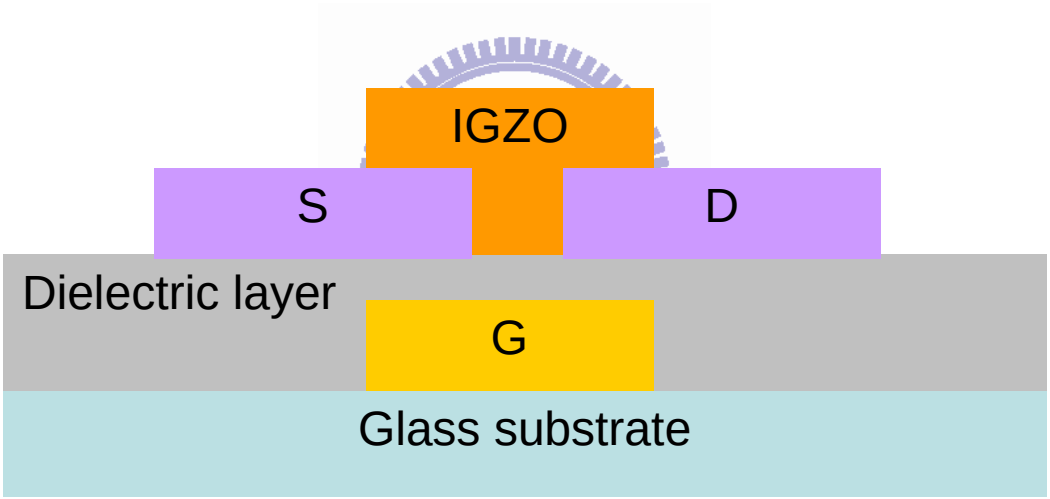


Fig. 3-4 The active region of a-IGZO deposition process.



(a)



(b)

Fig. 3-5 (a) Schematically illustrated top-view a-IGZO TFTs, (b) Schematically illustrated cross-sectional a-IGZO TFTs.

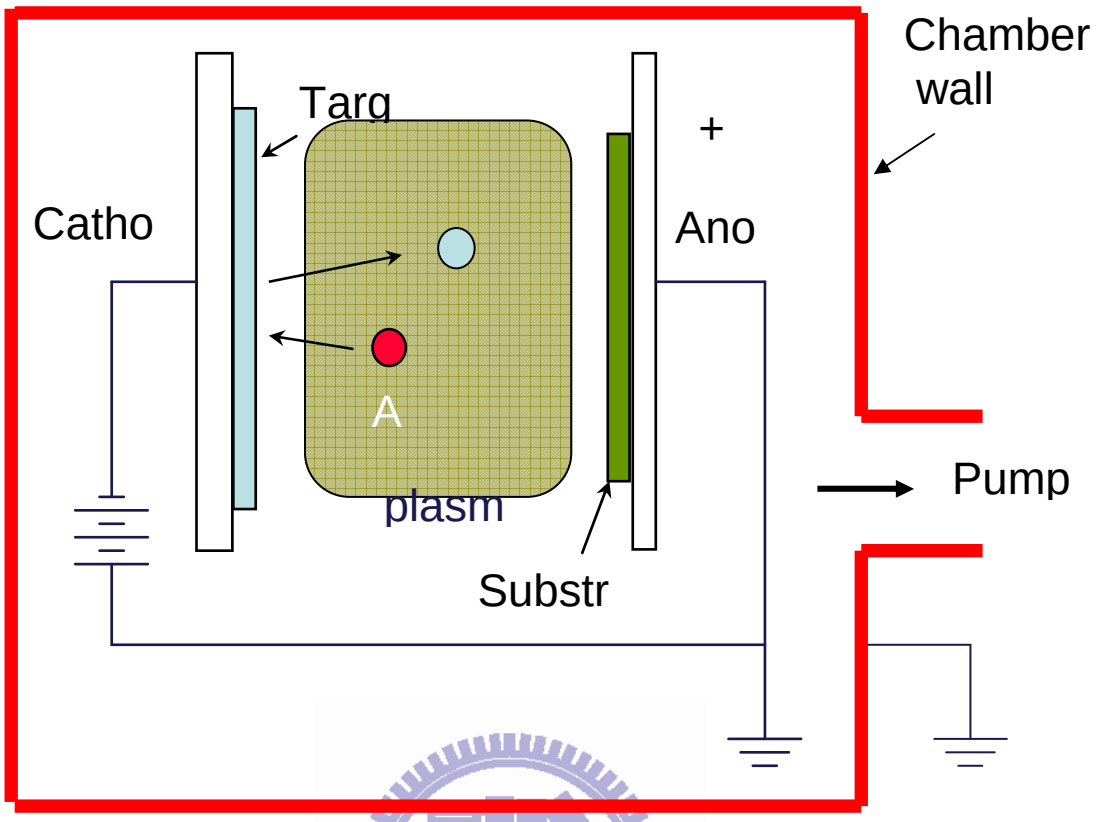


Fig. 3-6 Schematic DC sputtering system.

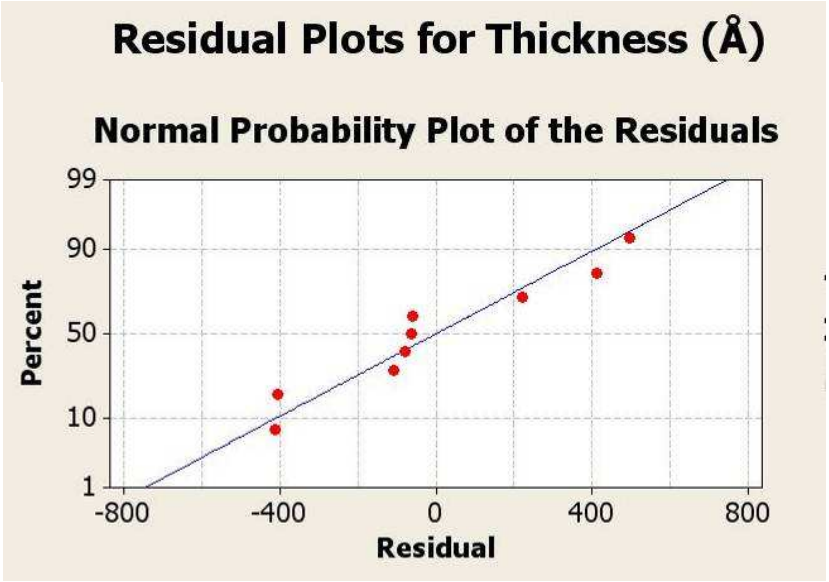


Fig. 3-7 Residual plots for thickness.

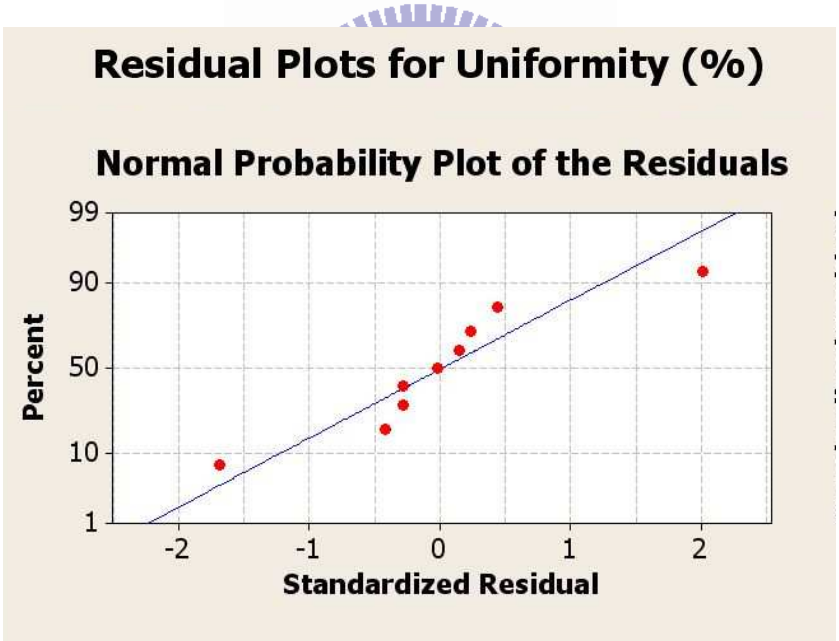


Fig. 3-8 Residual plots for uniformity.

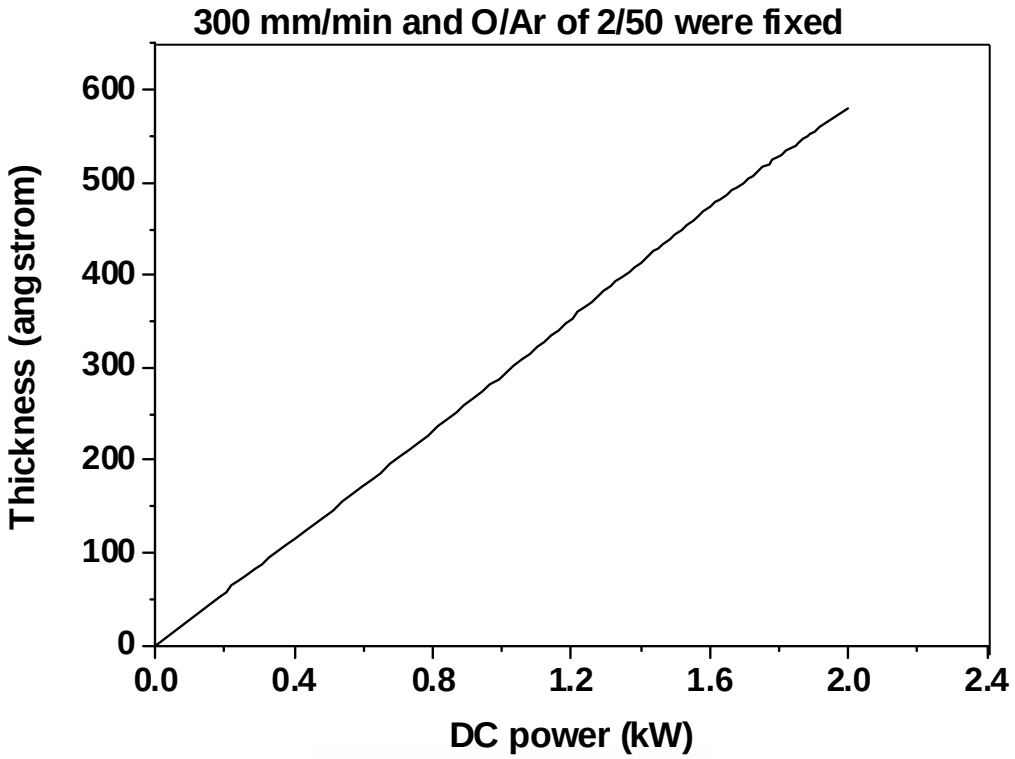
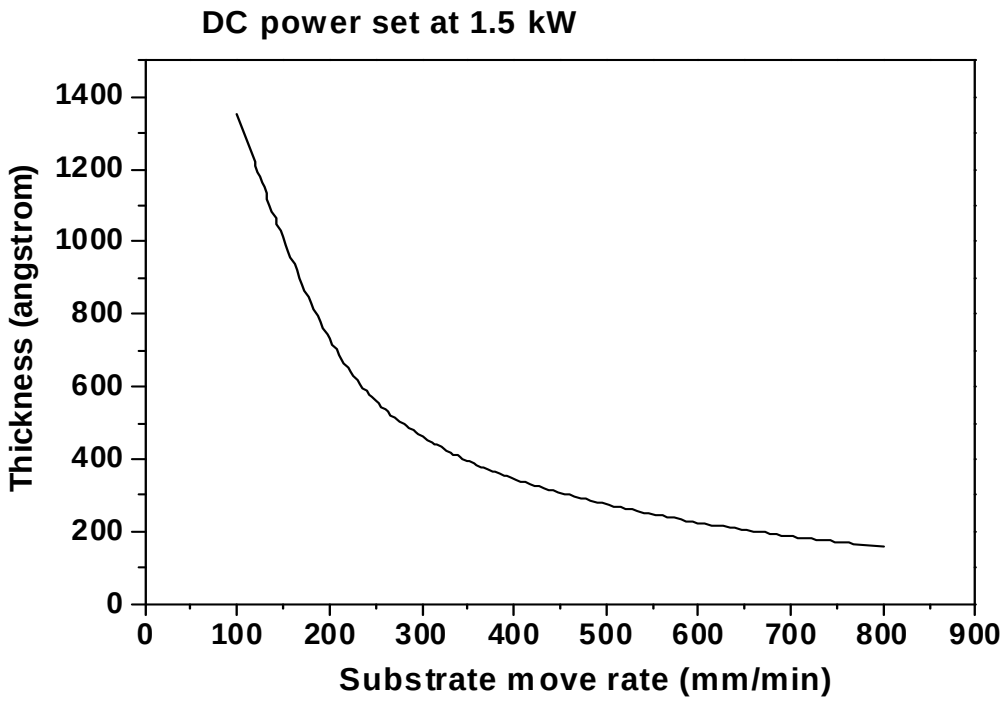
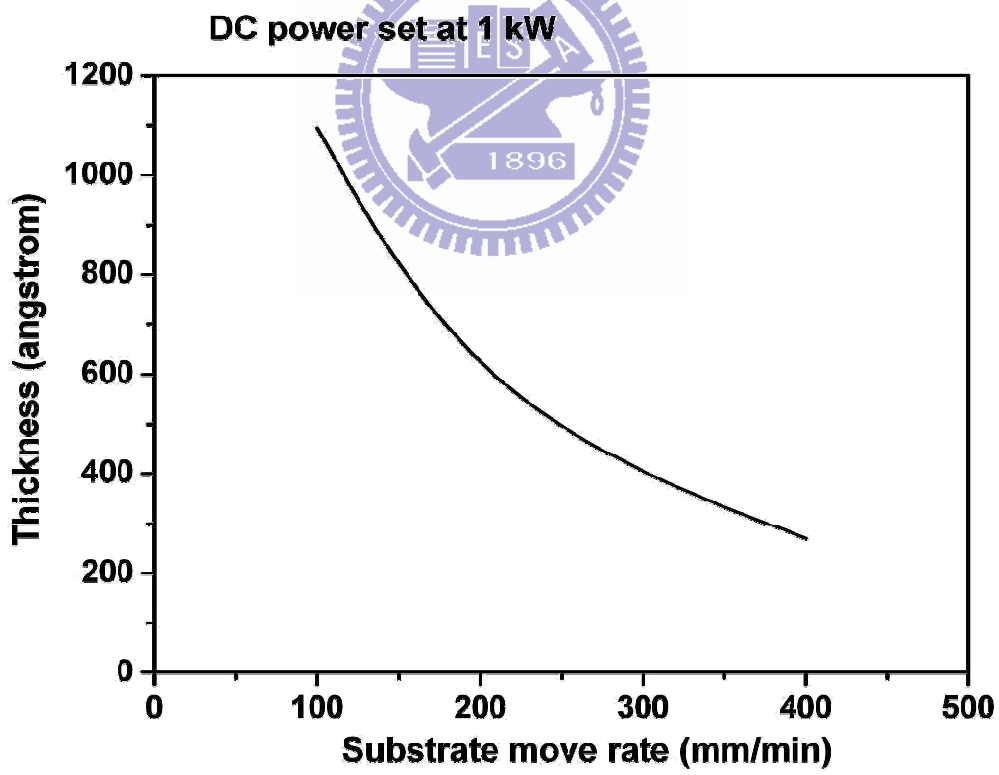


Fig. 3-9 Physical property of a-IGZO film as a function of DC power during deposition.

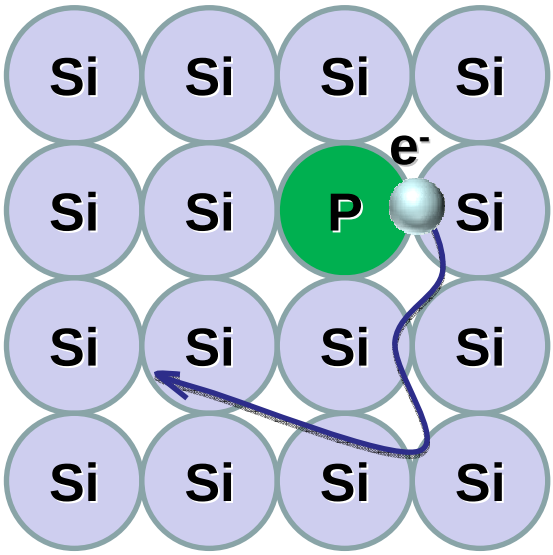


(a)

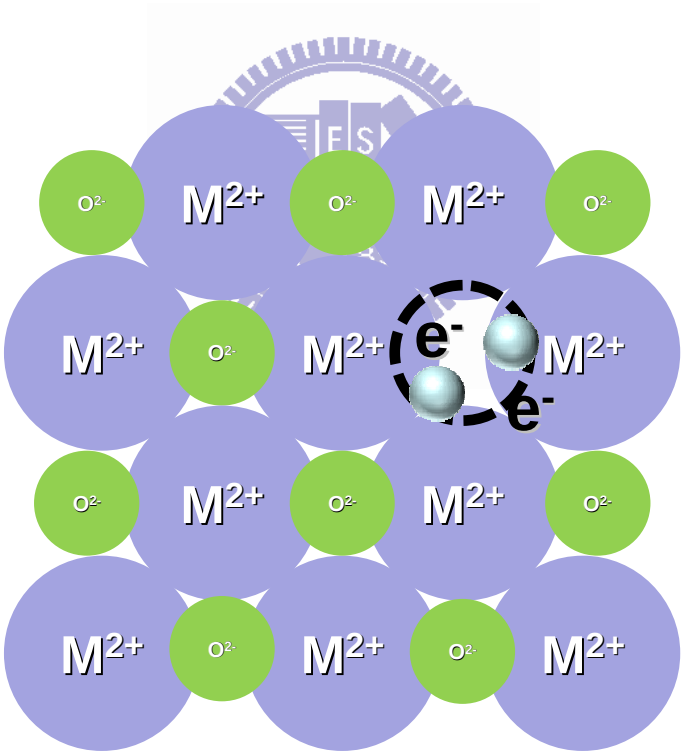


(b)

Fig. 3-10 Physical property of IGZO film as a function of substrate move rate during deposition. (a) DC power set at 1.5 kW, and (b) DC power set at 1 kW



(a)



(b)

Fig. 3-11 The carrier source of (a) Si, and (b) Metal oxide.

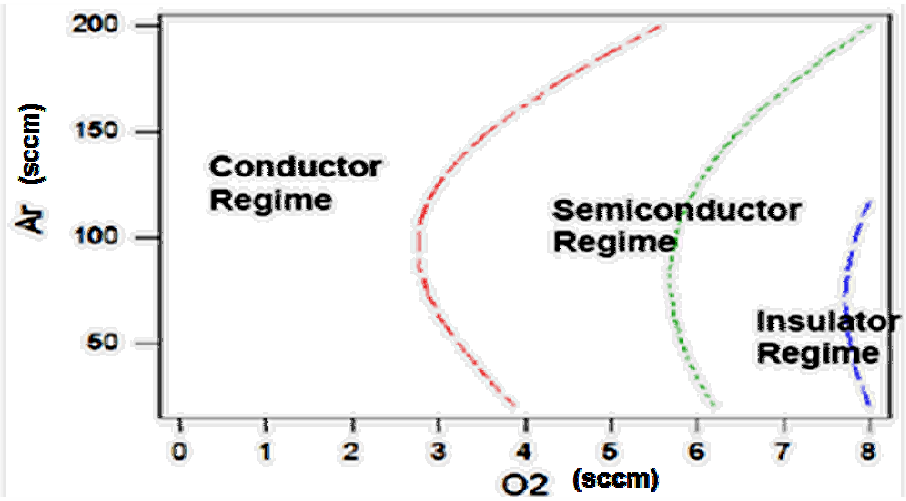


Fig. 3-12 Electrical property of IGZO TFT as a function of oxygen and argon flow rate during deposition.[14]

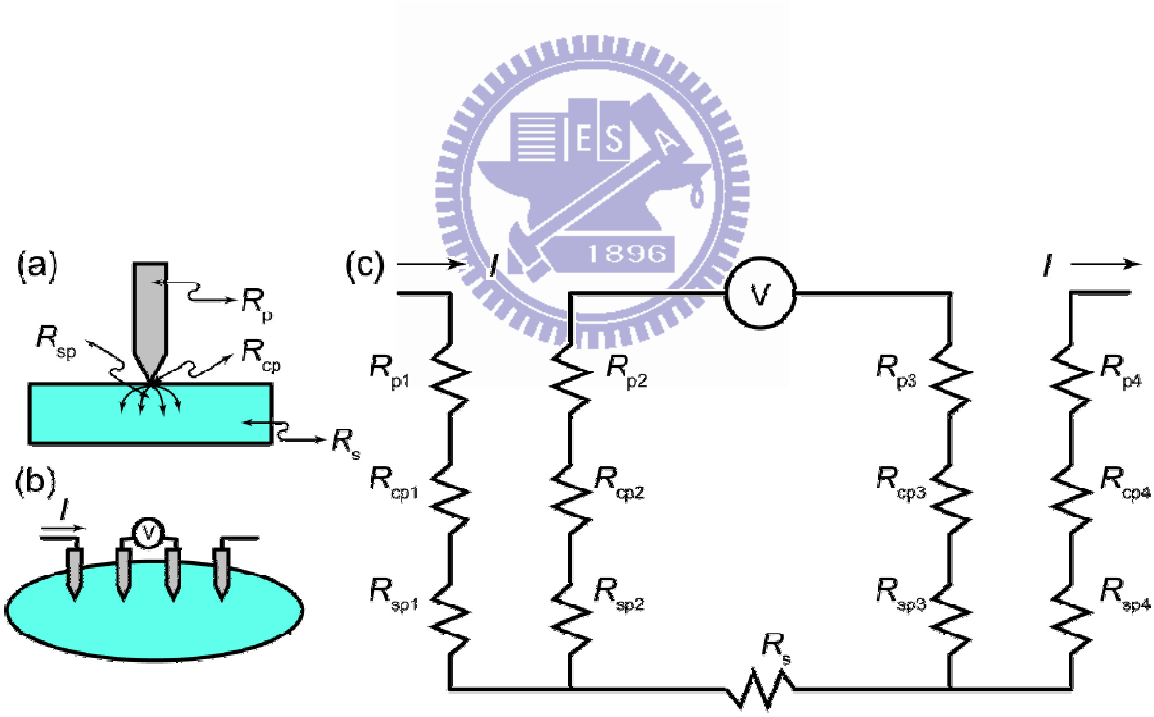


Fig. 4-1 Measurement of film sheet resistance.

$4.190e^4$	$6.524e^4$	$5.704e^4$
$3.921e^4$	$7.030e^4$	$6.347e^4$
$8.982e^4$	$1.611e^5$	$1.331e^5$

Unit: Ω/□

Fig. 4-2 The sheet resistance of a-IGZO film on 370 × 470 mm substrate.

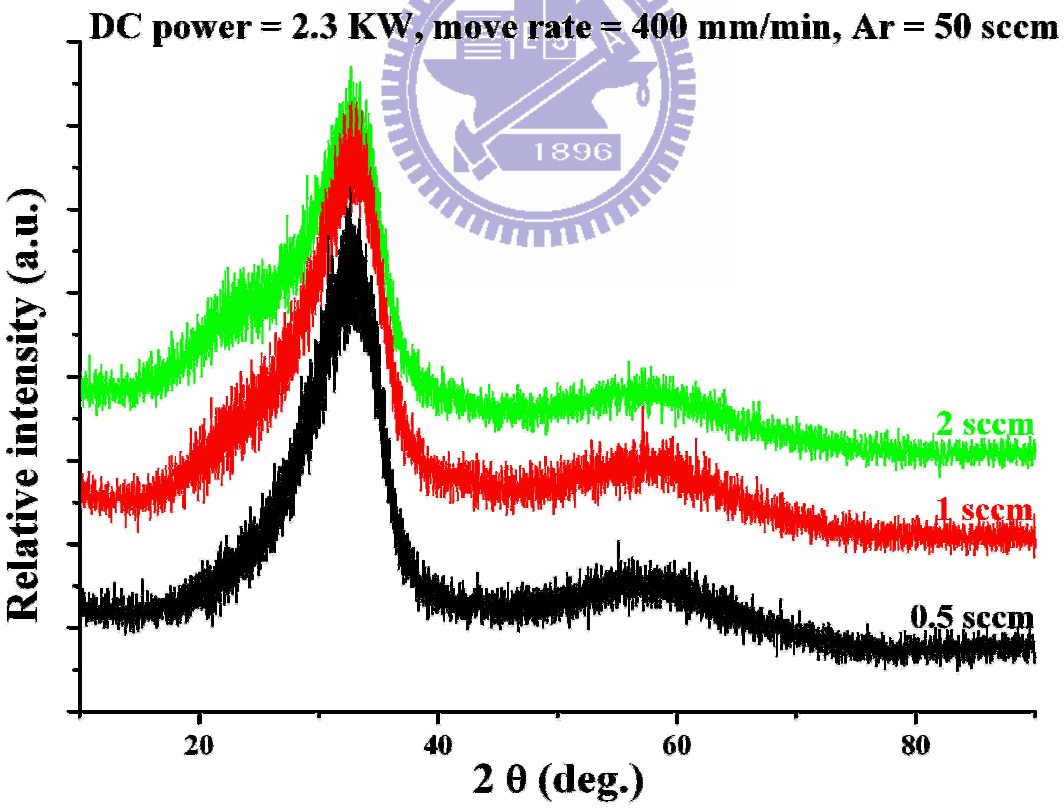


Fig. 4-3 The measurement of as-deposited IGZO films on a glass substrate (G2) with different oxygen flux.

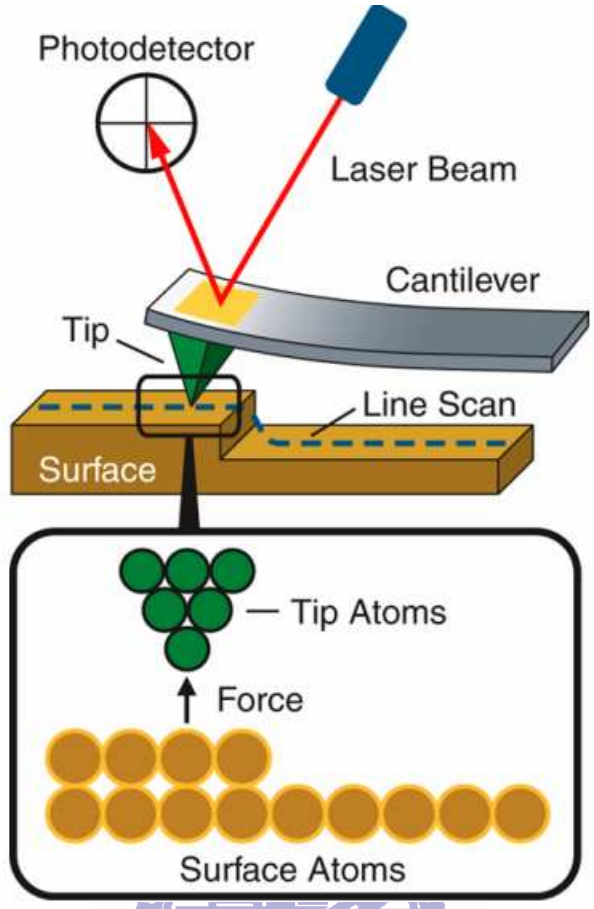
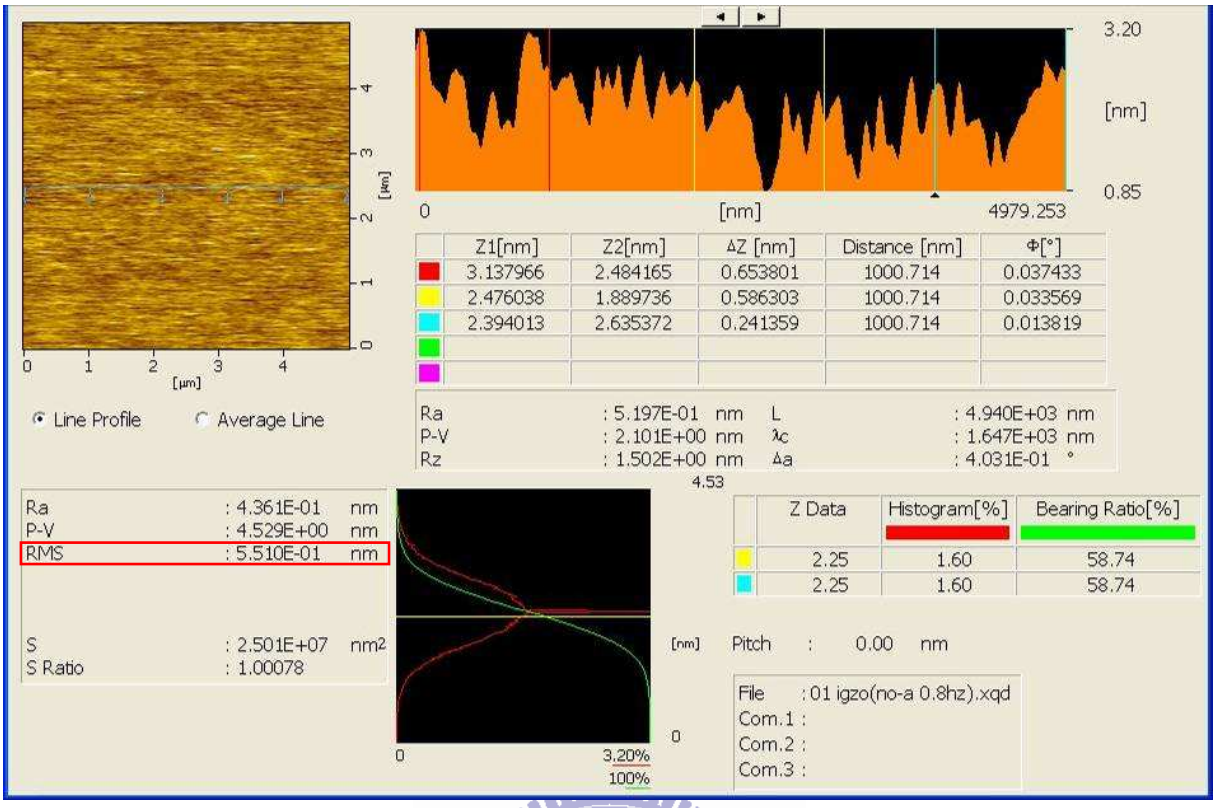
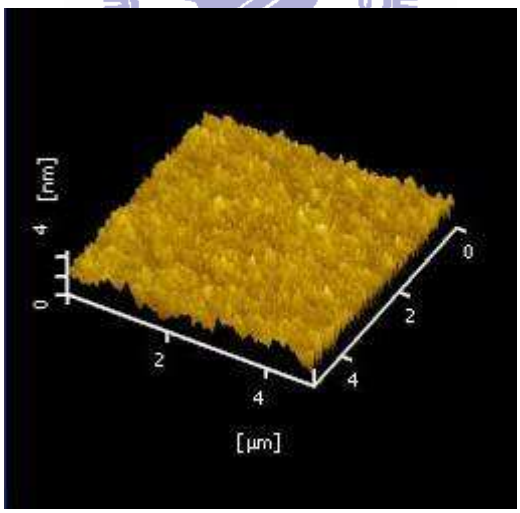


Fig. 4-4 The schematic model of AFM.

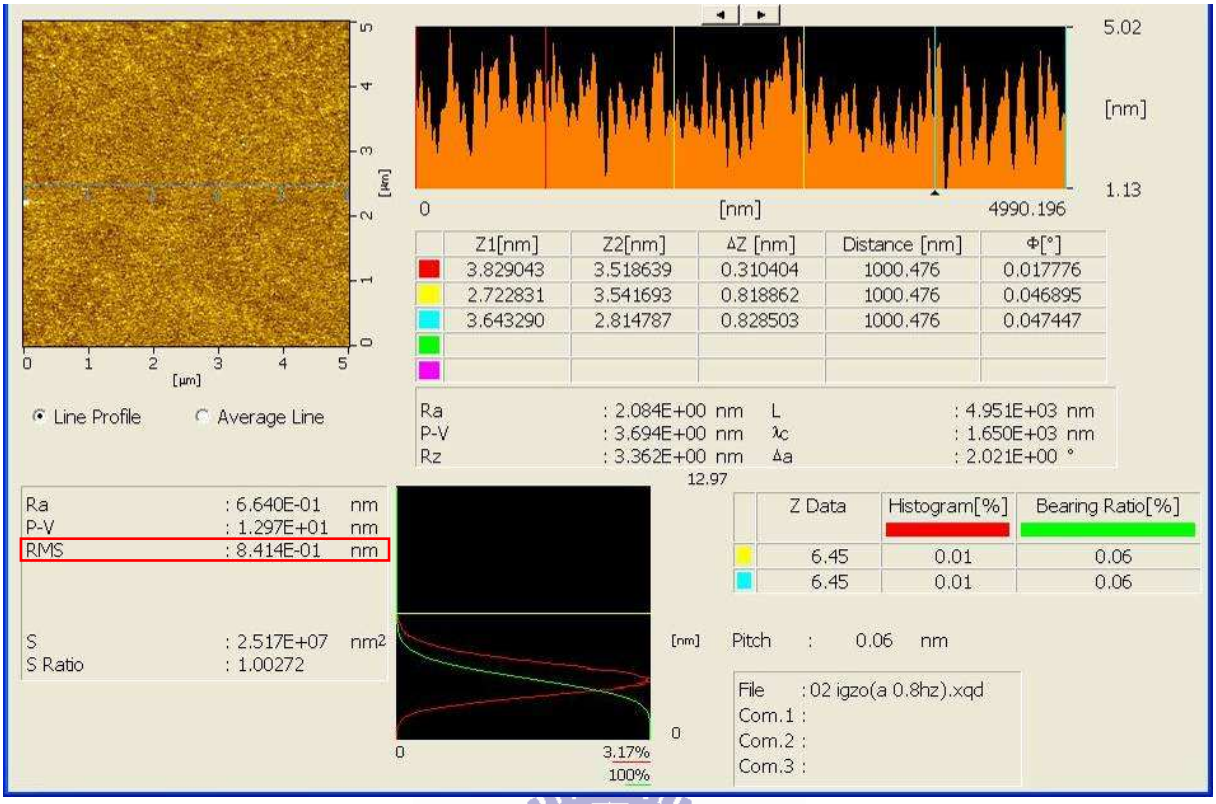


(a)

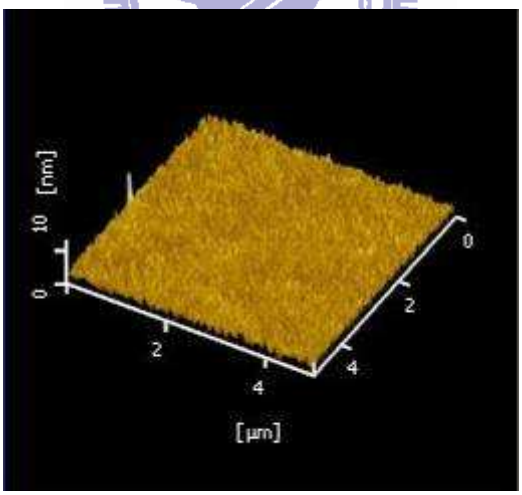


(b)

Fig. 4-5 The AFM result of a 500 Å thick a-IGZO film grown at room temperature without annealing. (a) 2D picture (RMS), and (b) 3D picture

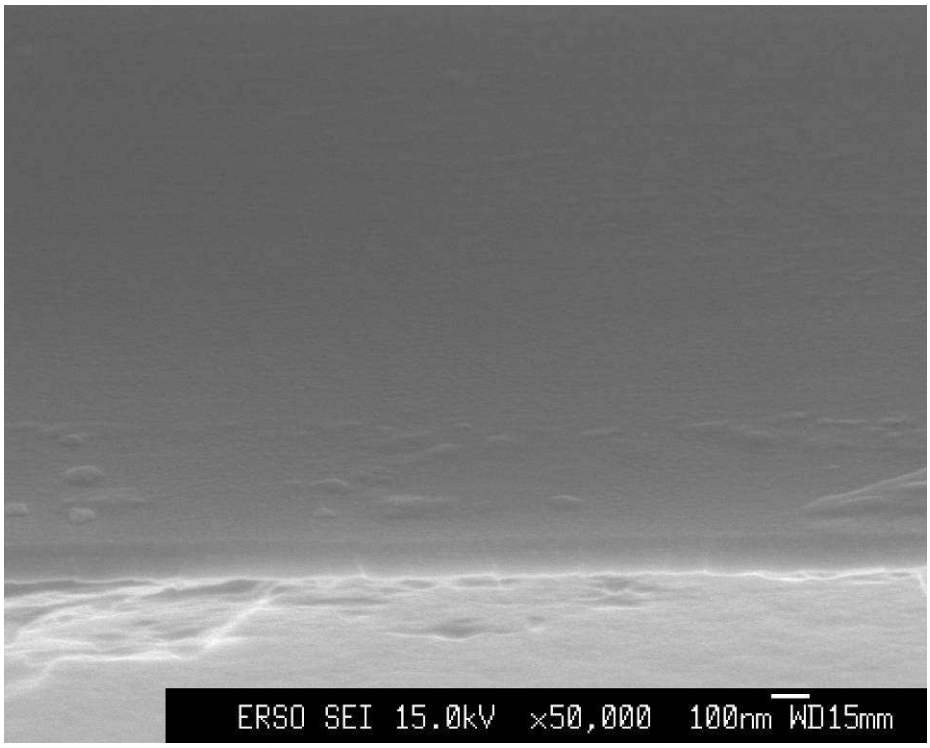


(a)

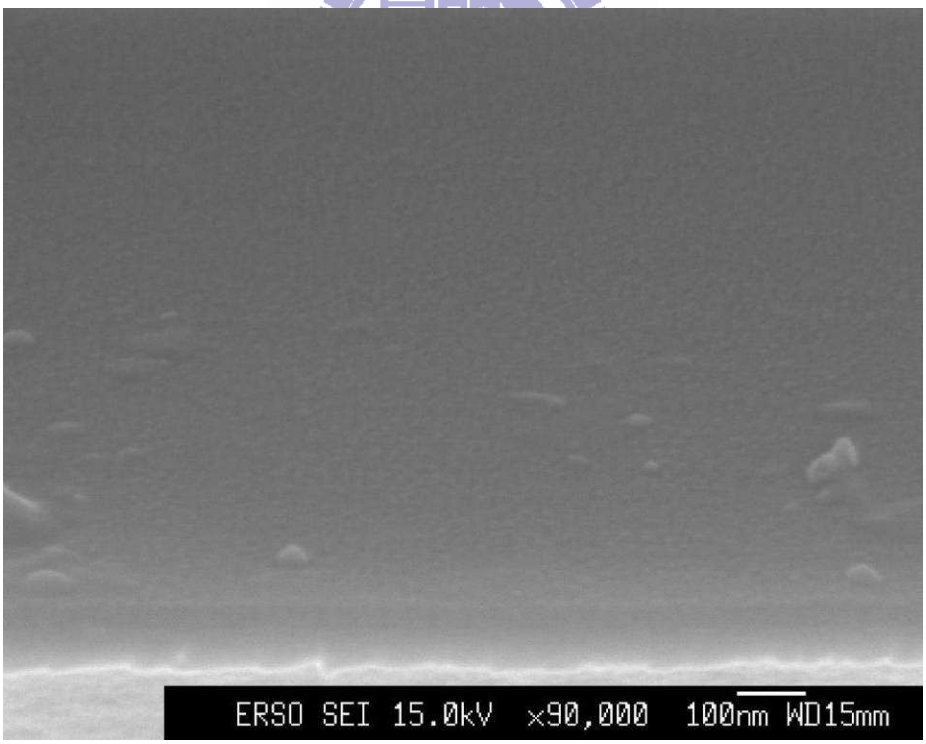


(b)

Fig. 4-6 The AFM result of a 500 Å thick a-IGZO film grown at room temperature after annealing in 250 °C (1 hr). (a) 2D picture (RMS), and (b) 3D picture

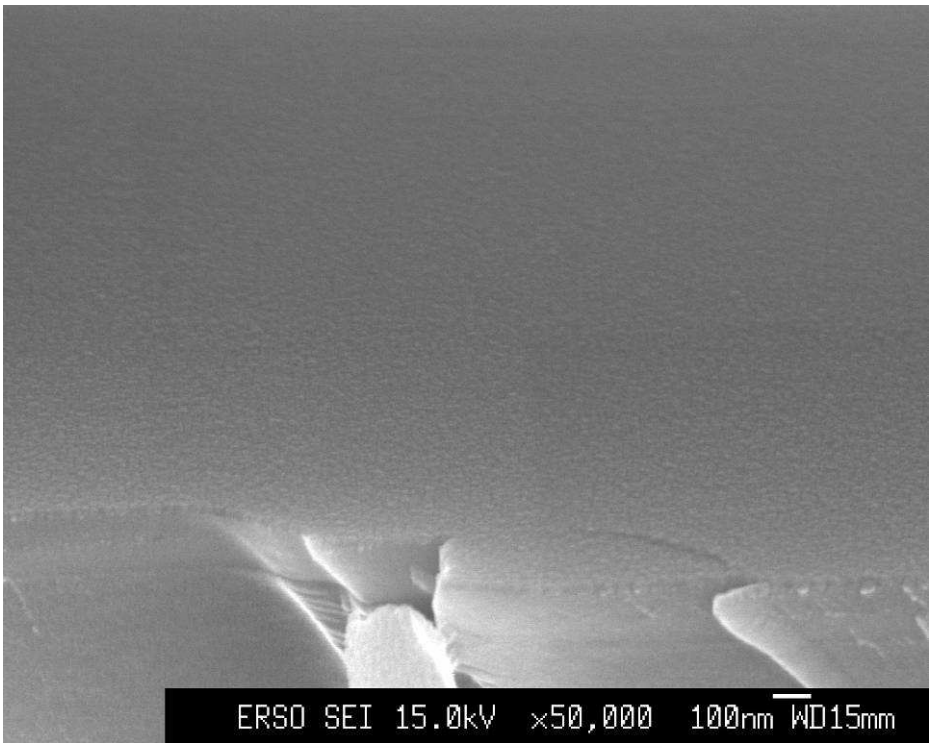


(a)

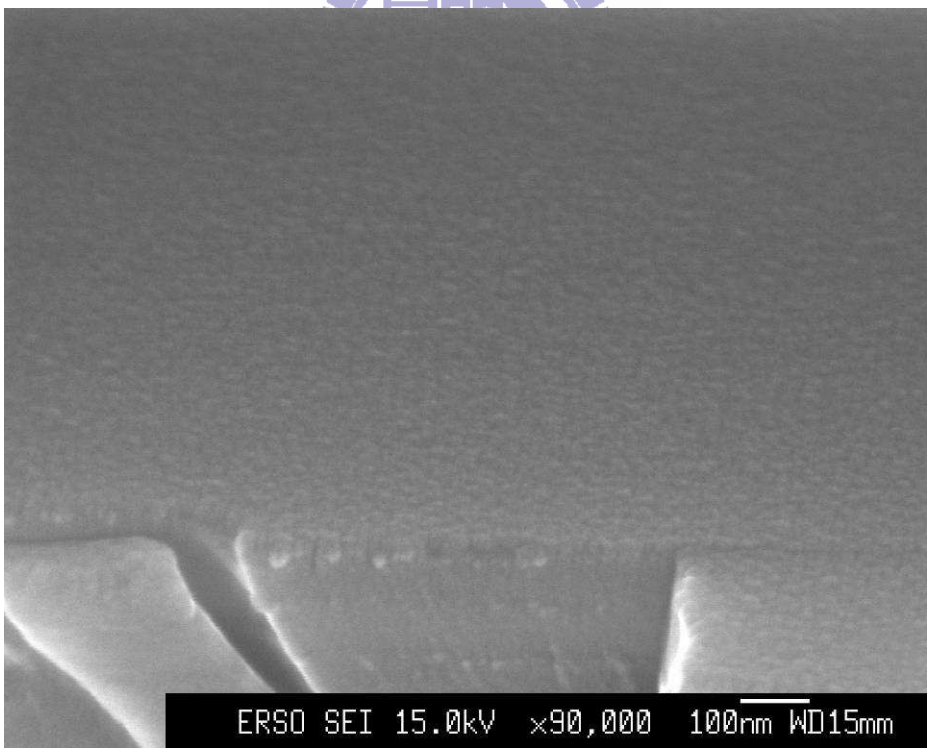


(b)

Fig. 4-7 The cross-section view of full a-IGZO film without annealing. (a) 50,000 magnification, and (b) 90,000 magnification

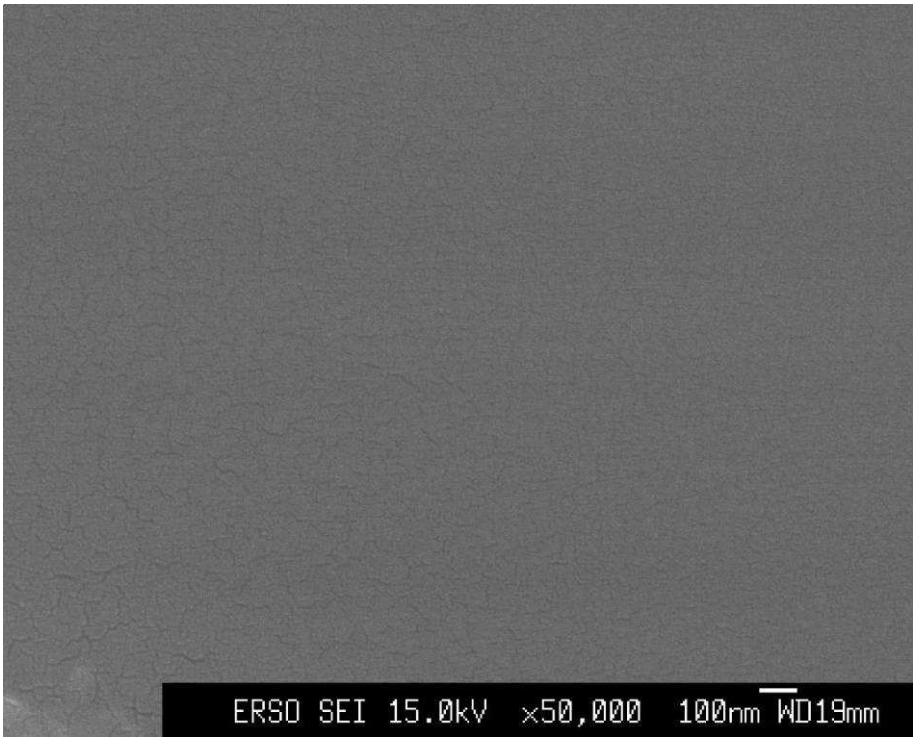


(a)

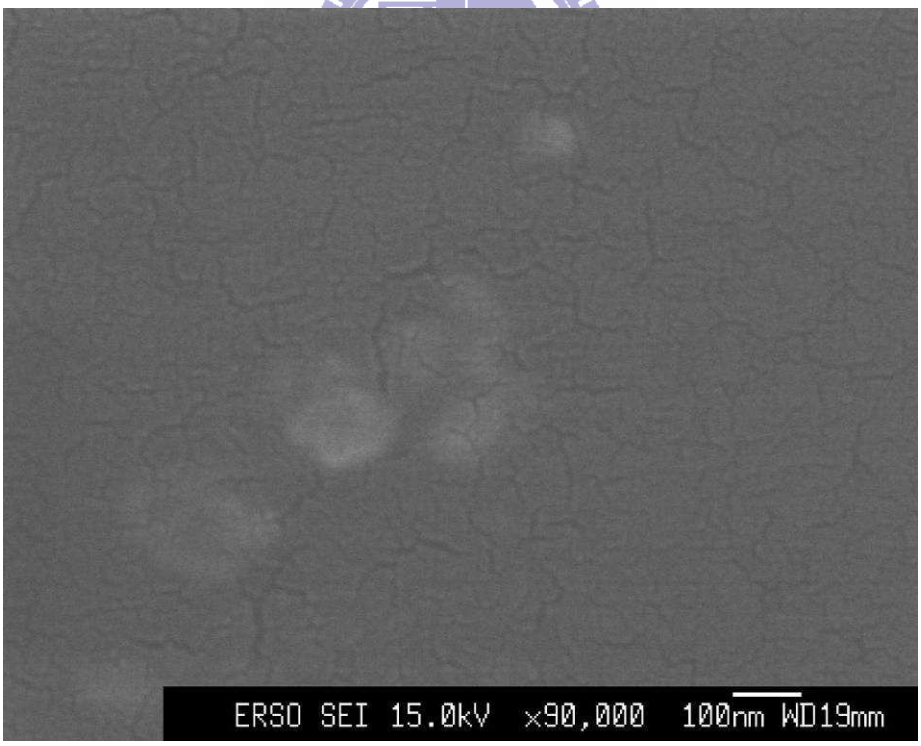


(b)

Fig. 4-8 The cross-section view of full a-IGZO film after annealing in 250 °C (1 hr). (a) 50,000 magnification, and (b) 90,000 magnification

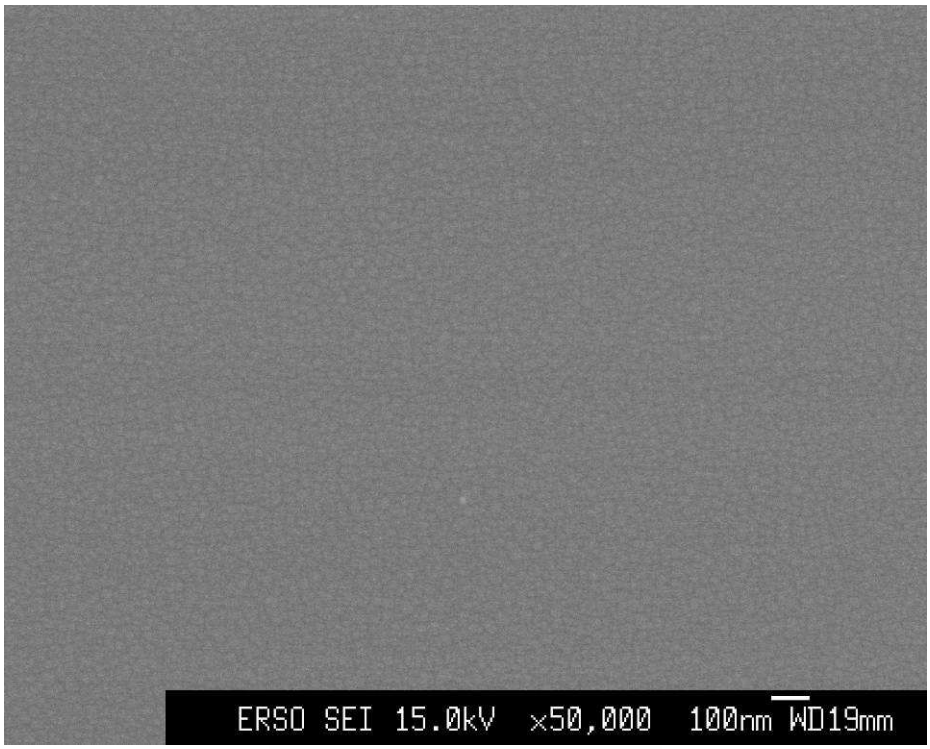


(a)

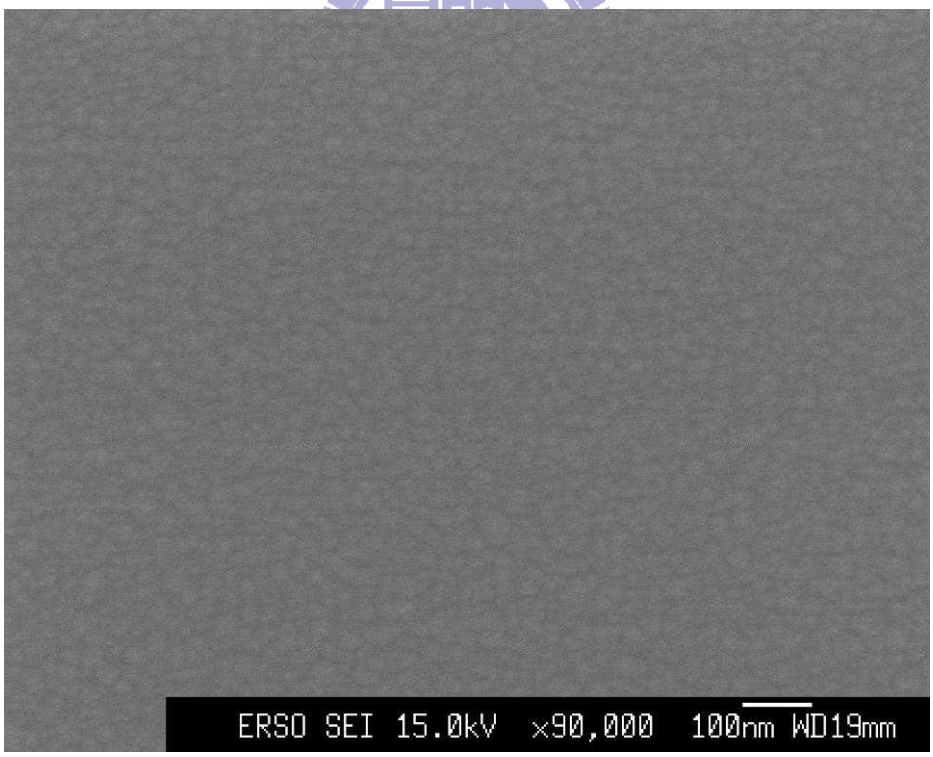


(b)

Fig. 4-9 The top-view of a-IGZO film without annealing. (a) 50,000 magnification, and (b) 90,000 magnification



(a)



(b)

Fig. 4-10 The top-view of a-IGZO film after annealing in 250 °C(1 hr). (a) 50,000 magnification, and (b) 90,000 magnification

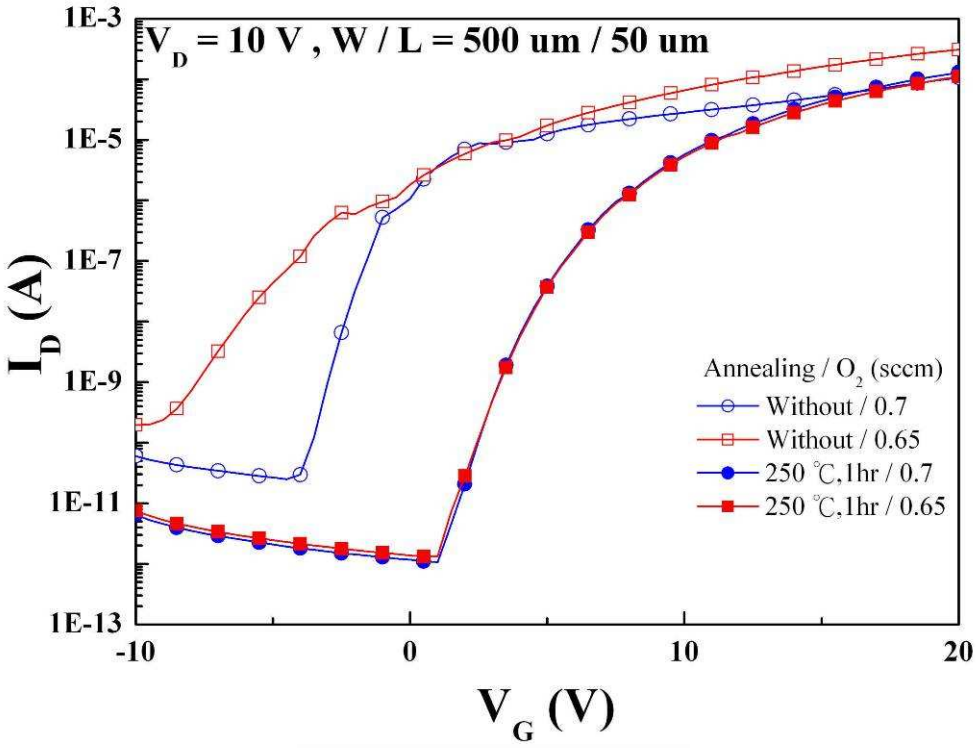
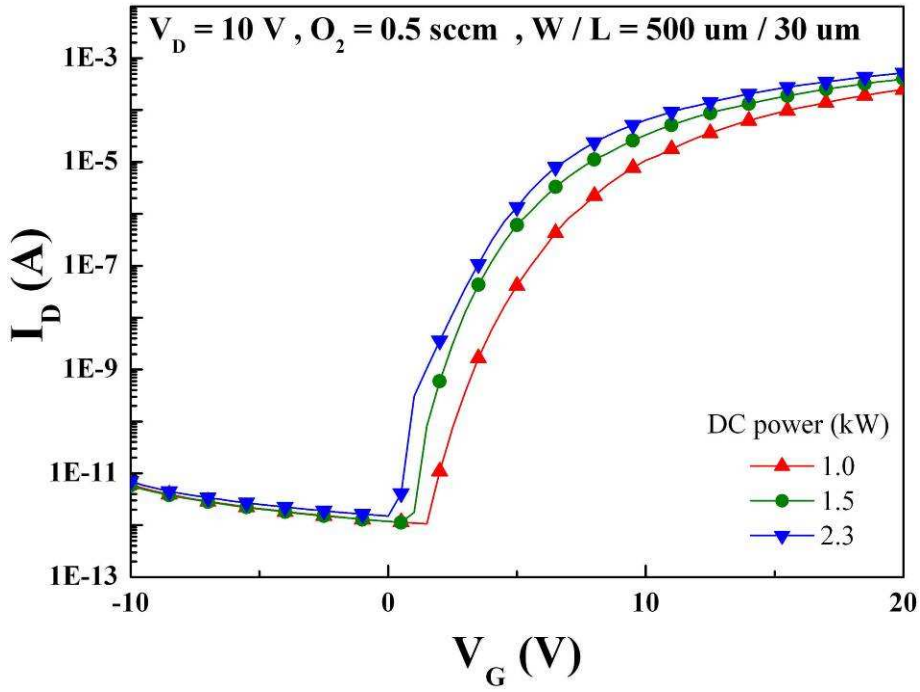
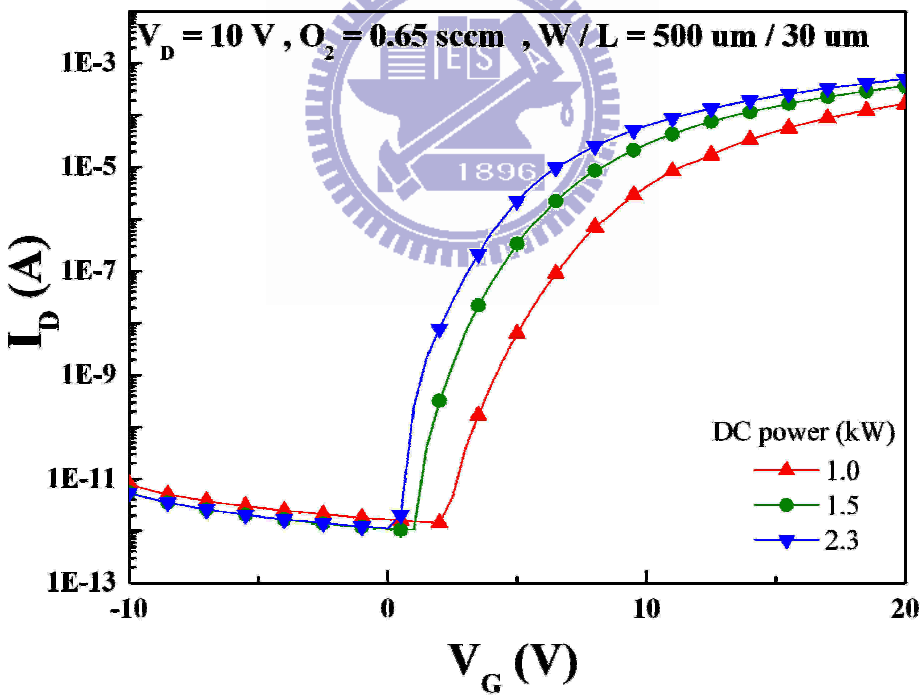


Fig. 4-11 The I_D-V_G characteristic of TFTs with different O_2 flow rate (0.65 and 0.7 sccm) before and after thermal annealing.



(a)



(b)

Fig. 4-12 The I_D-V_G characteristics of a-IGZO TFTs fabricated with DC power 1, 1.5, and 2.3 kW and argon/oxygen rate of (a) 50/0.5 sccm, and (b) 50/0.65 sccm by sputtering after annealing in 250 °C (1 hr).

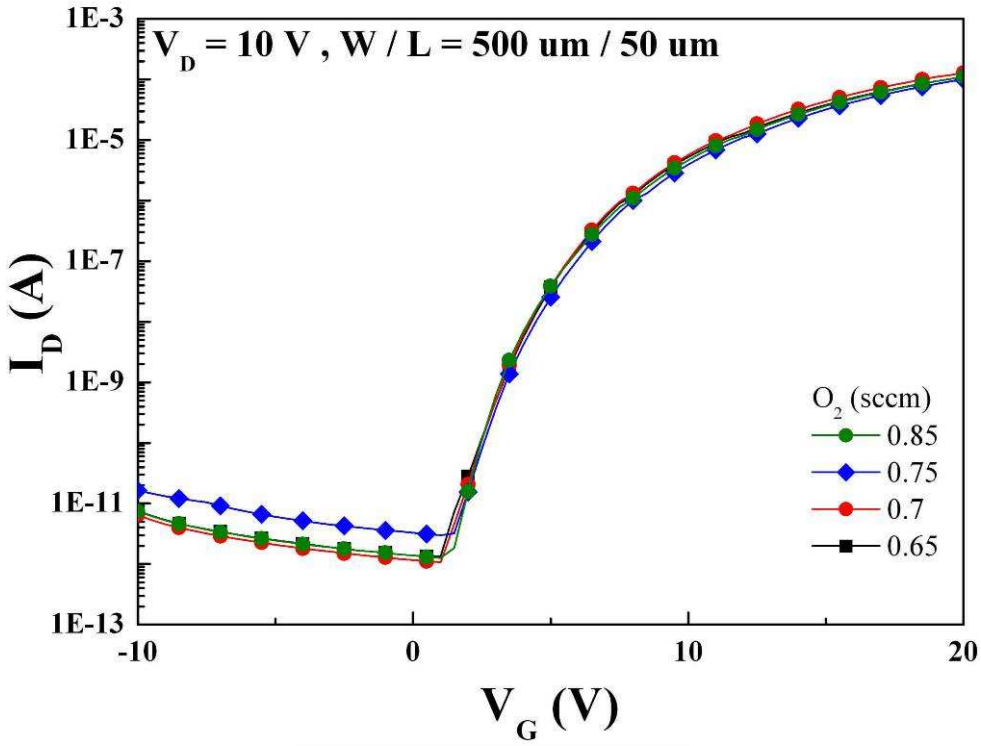
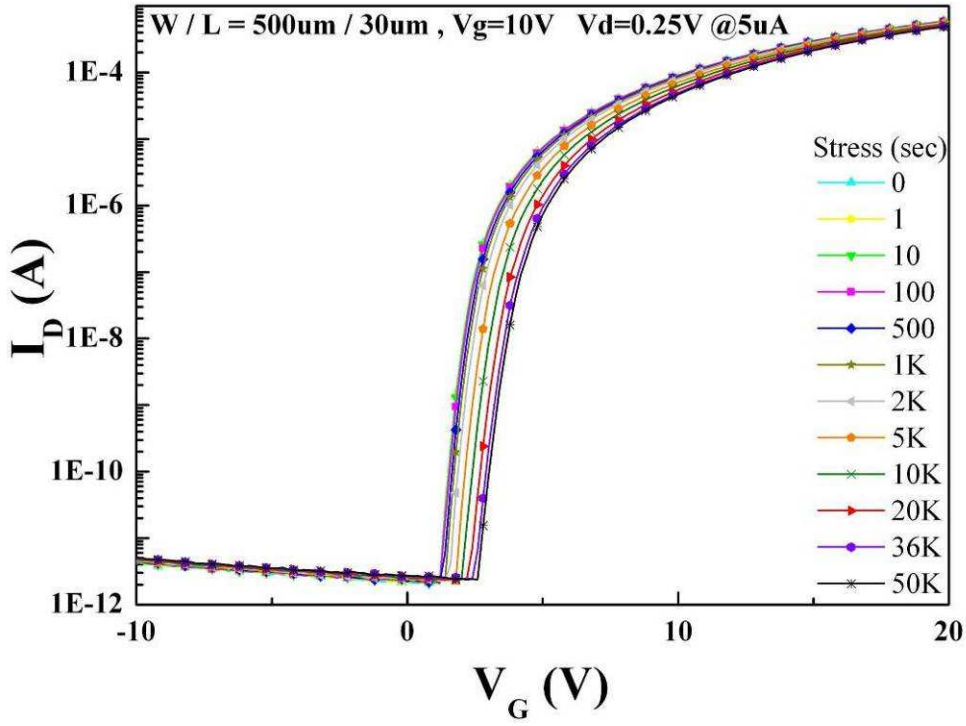
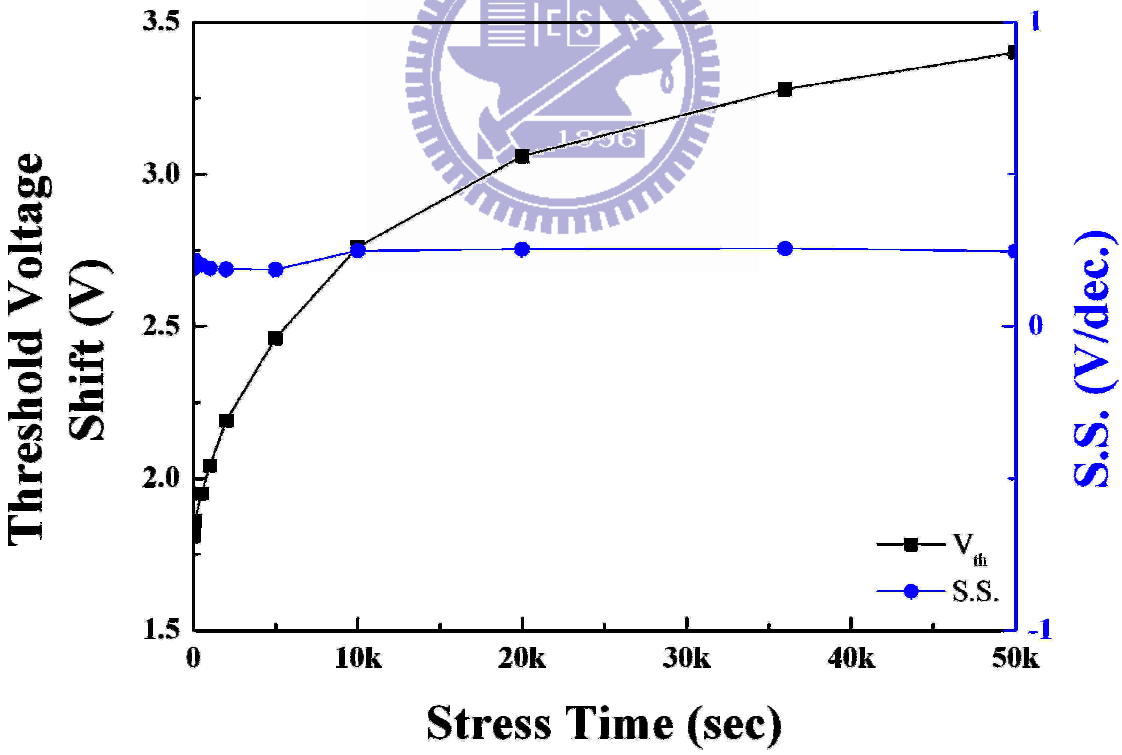


Fig. 4-13 The I_D-V_G characteristics of a-IGZO TFTs fabricated with DC power 2.3 kW and argon/oxygen rate of 50/0.65, 50/0.7, 50/0.75, and 50/0.85 sccm by sputtering after annealing in 250 °C (1 hr).

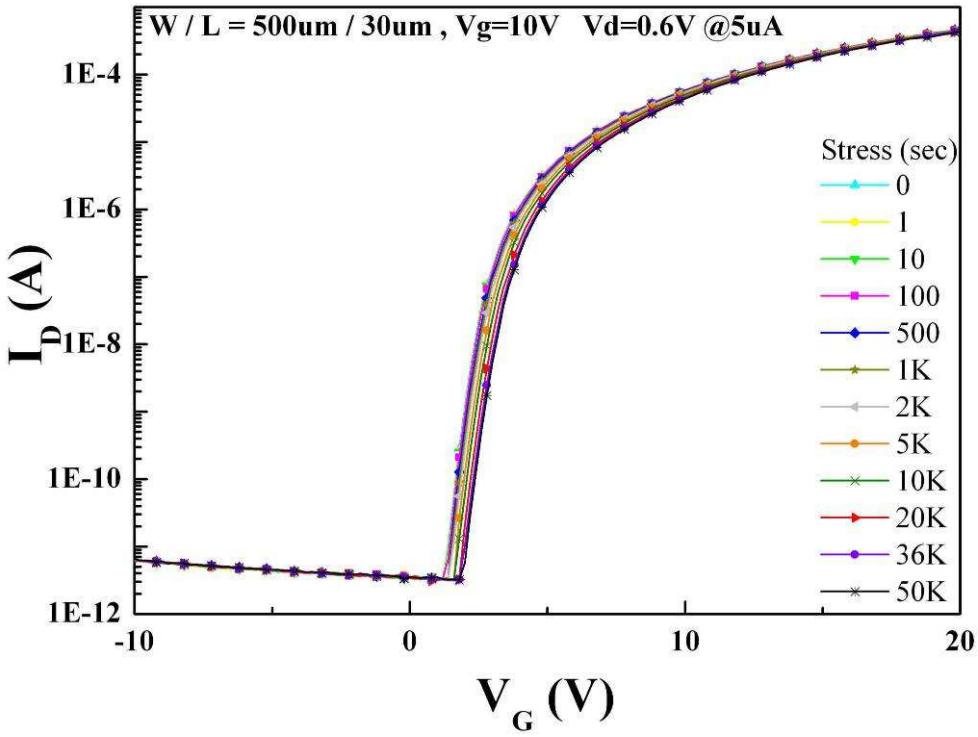


(a)

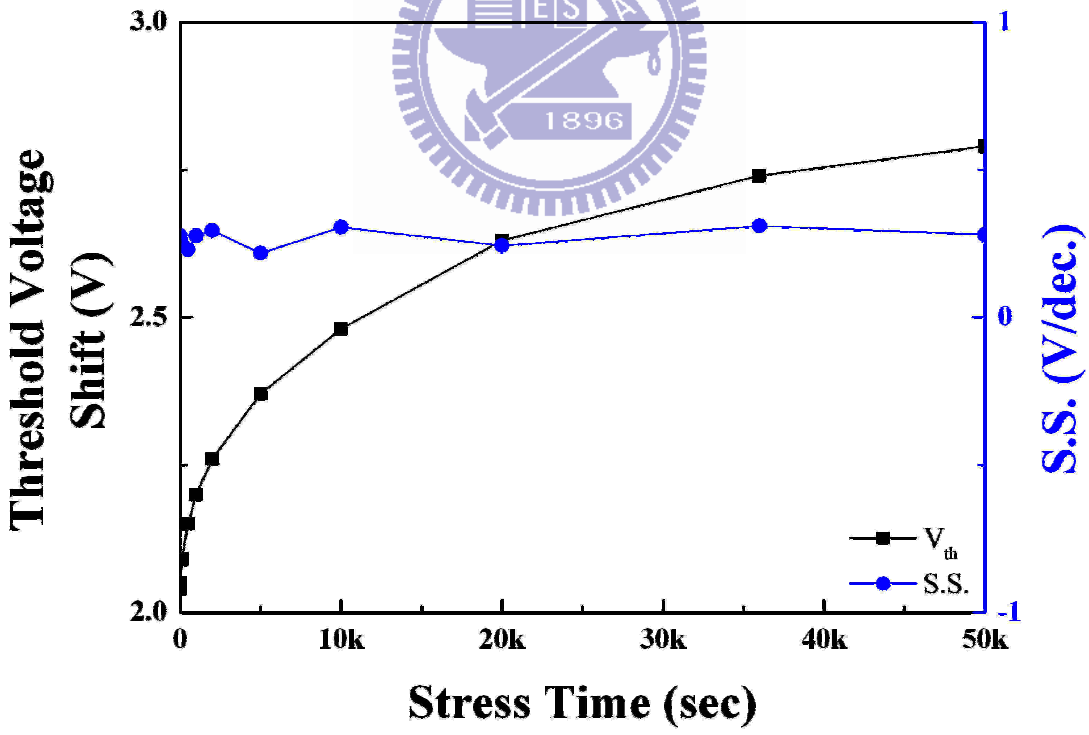


(b)

Fig. 4-14 The bias stress stability of a-IGZO 500 Å TFTs at room temperature (25 °C), (a) I_D-V_G, and (b) shows the stressing time via V_{th} shift and S.S.

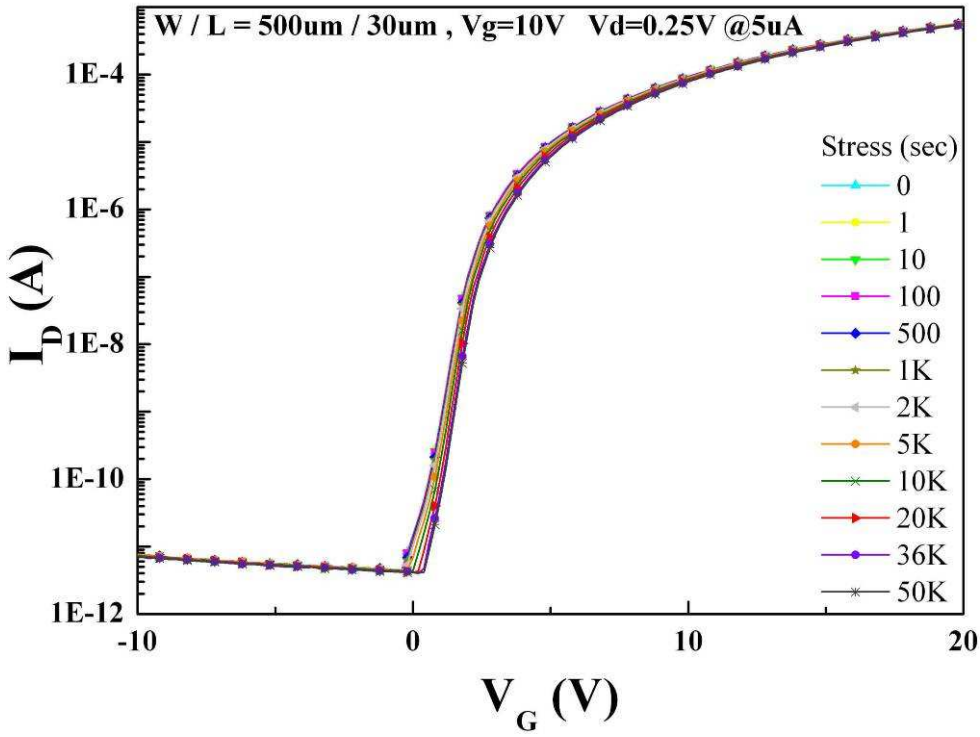


(a)

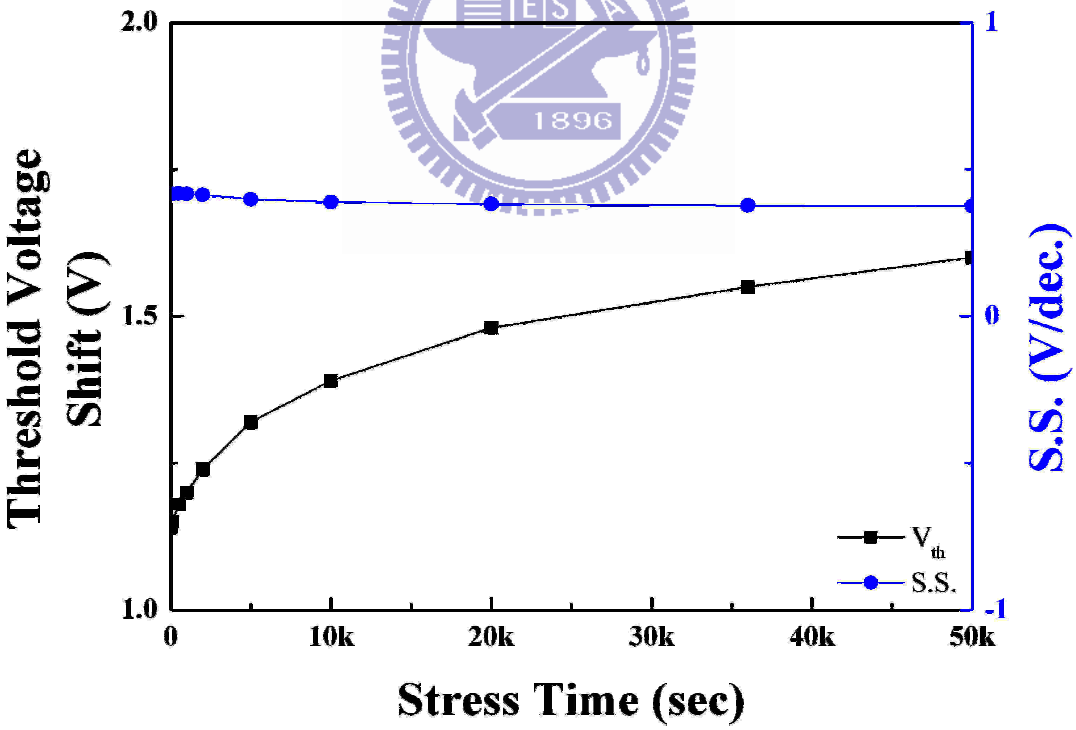


(b)

Fig. 4-15 The bias stress stability of a-IGZO 1 kÅ TFTs at room temperature (25 °C), (a) I_D-V_G, and (b) shows the stressing time via V_{th} shift and S.S.



(a)



(b)

Fig. 4-16 The bias stress stability of a-IGZO 2 kÅ TFTs at room temperature (25 °C), (a) I_D-V_G, and (b) shows the stressing time via V_{th} shift and S.S.

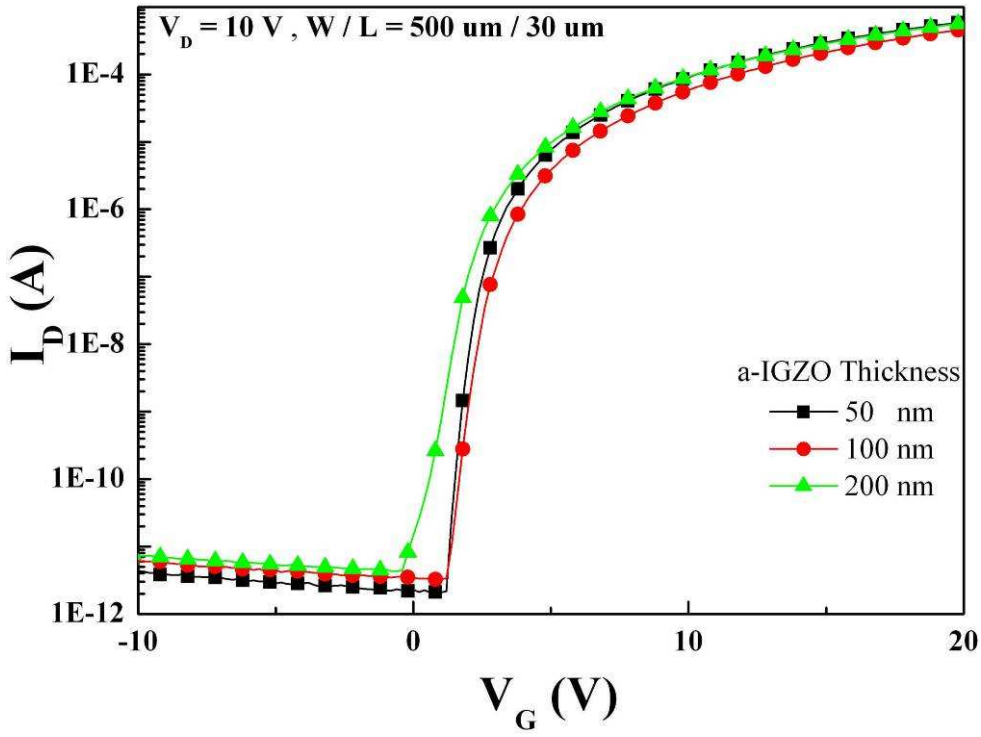


Fig. 4-17 Drain to source current (I_{DS}) vs gate to source voltage (V_{GS}) as a function of semiconductor thickness (500 Å, 1 kÅ, and 2 kÅ). V_{DS} was 10 V.

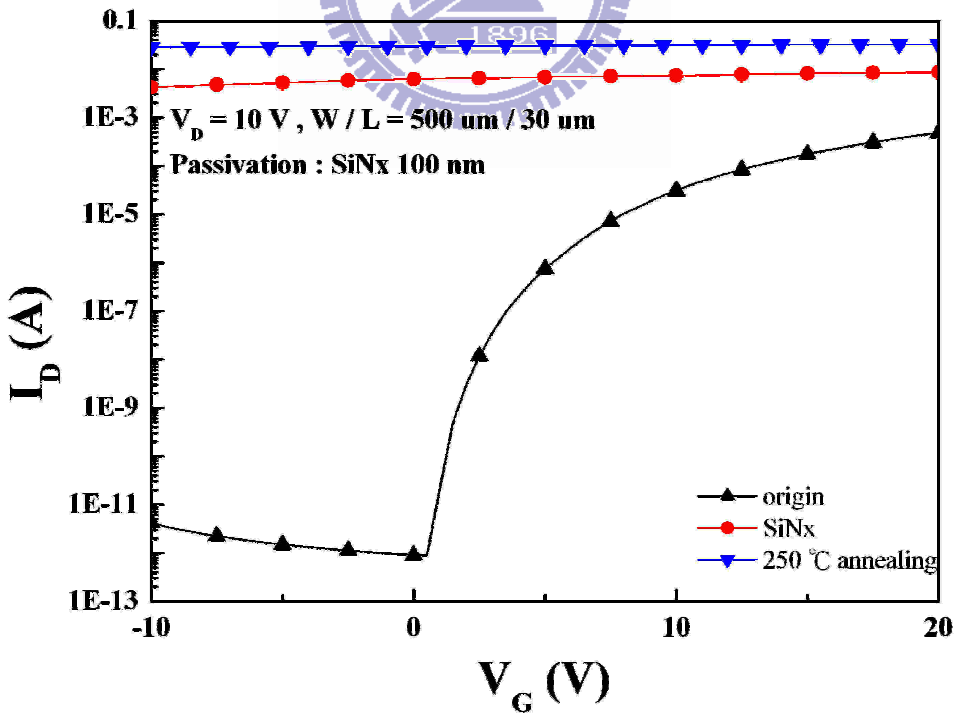


Fig. 4-18 The I_D-V_G our a-IGZO TFTs with 1 kÅ SiNx passivation. The characteristics were measured after 1 hr final annealing at 250 °C.

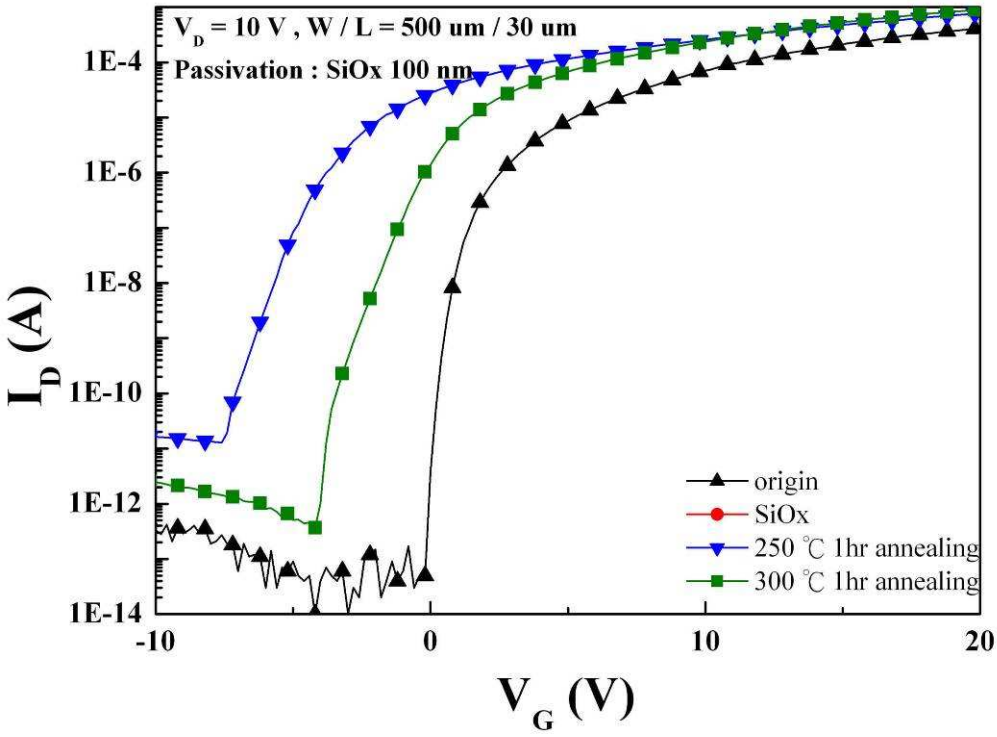


Fig. 4-19 The I_D-V_G our a-IGZO TFTs with 1 kÅ SiOx passivation (rich H atomic). The characteristics were measured after 1 hr final annealing at 250 and 300 °C.

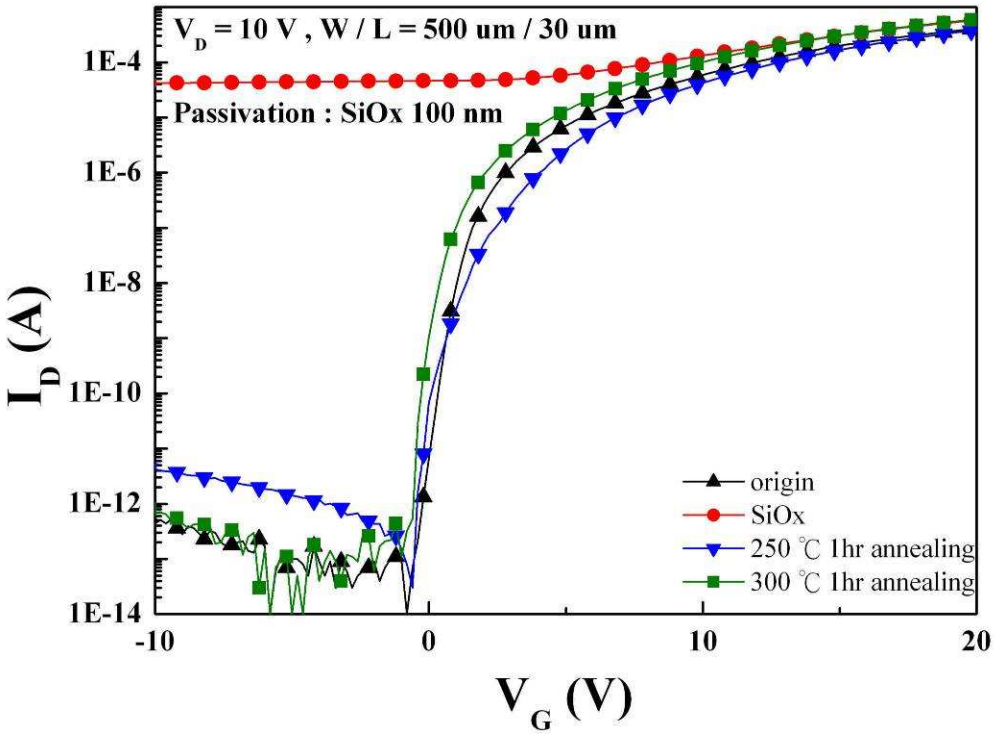
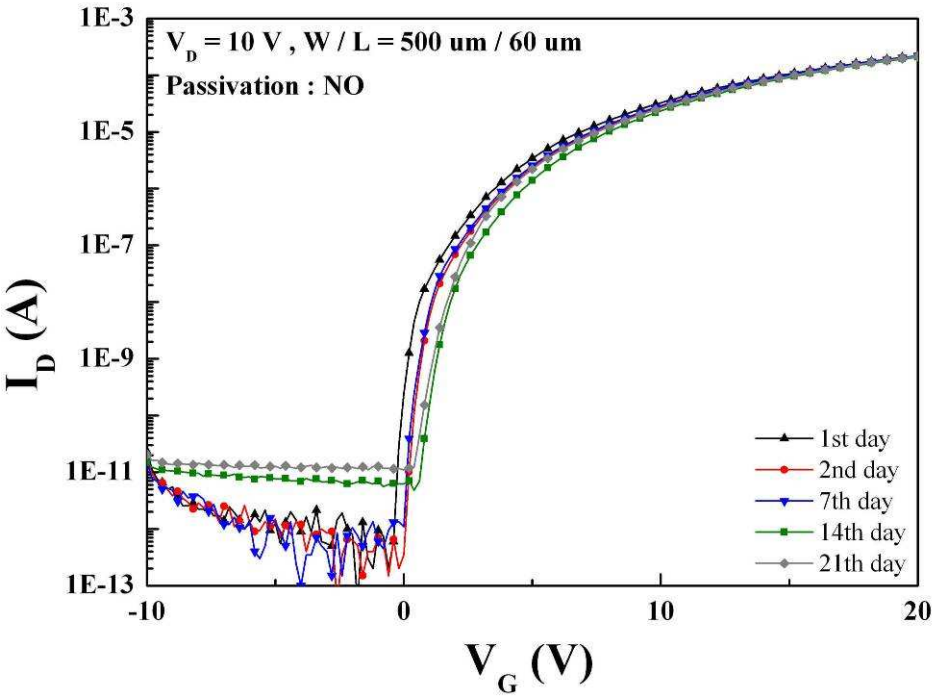
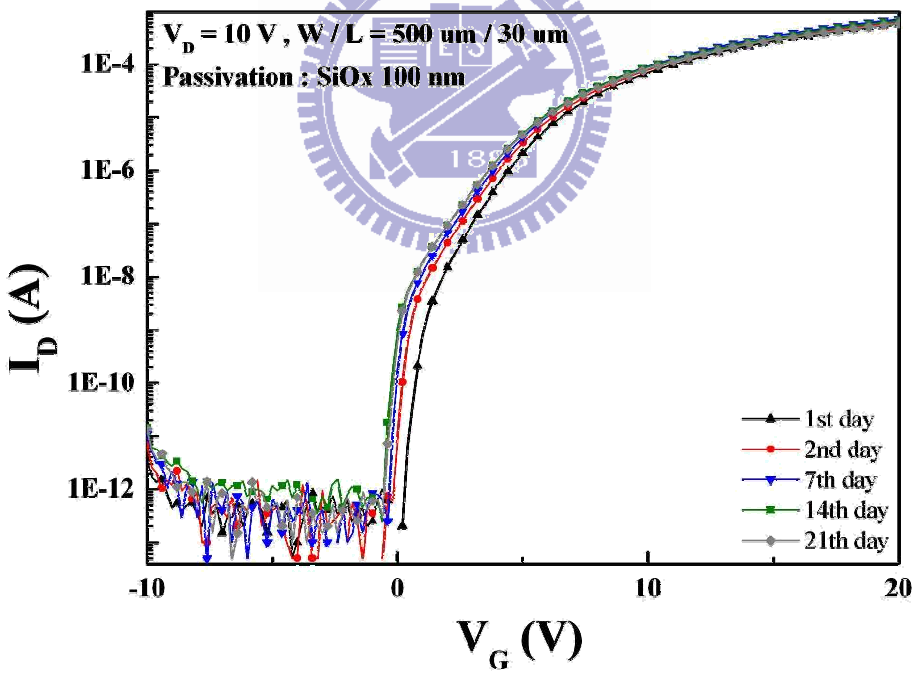


Fig. 4-20 shows the I_D-V_G our a-IGZO TFTs with 1 kÅ SiOx passivation (less H atomic). The characteristics were measured after 1 hr final annealing at 250 and 300 °C.

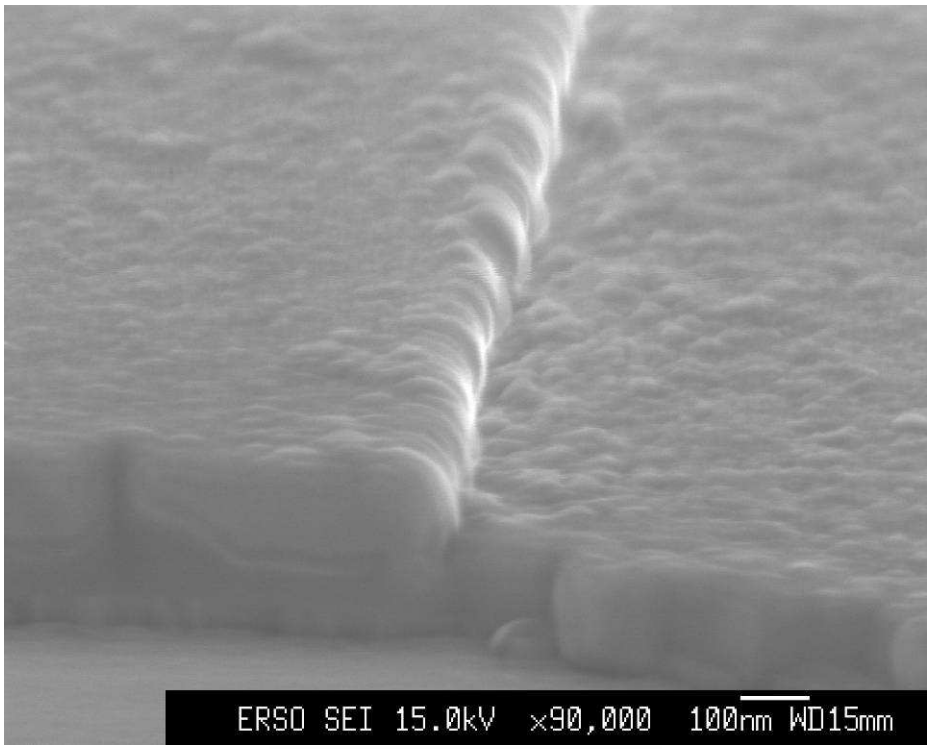


(a)

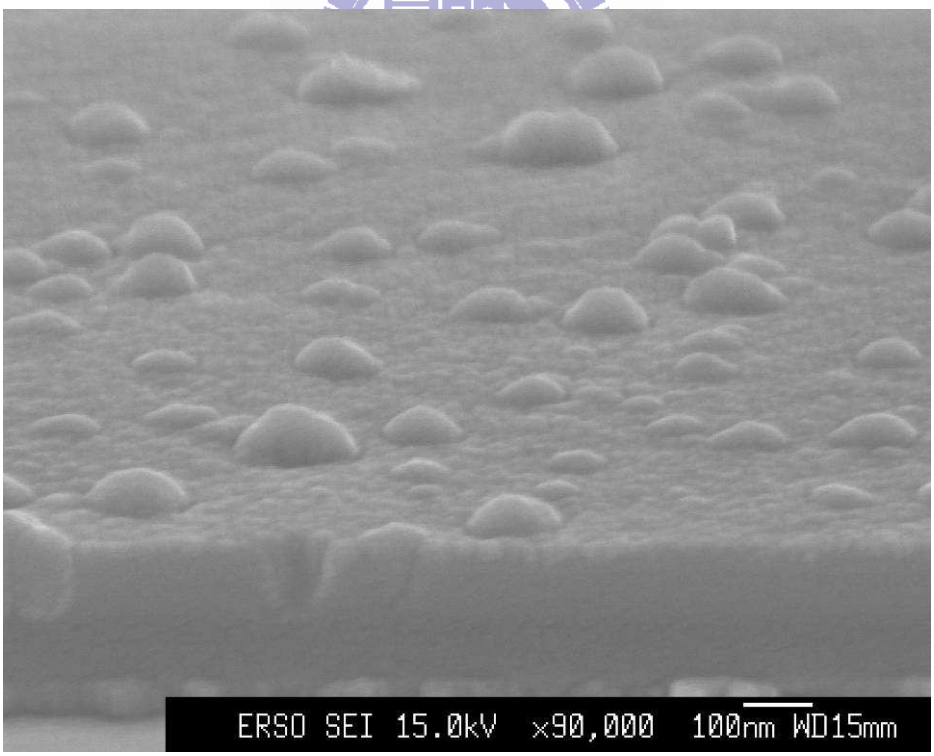


(b)

Fig. 4-21 The transfer curves of a-IGZO TFTs showing the environmental stability, (a) none passivated device, and (b) SiOx (less H atomic) passivated device.



(a)



(b)

Fig. 4-22 The cross-sectional view of SEM of a-IGZO films treated by hydrogen plasma at (a) none, and (b) 340 W / 700 sccm.

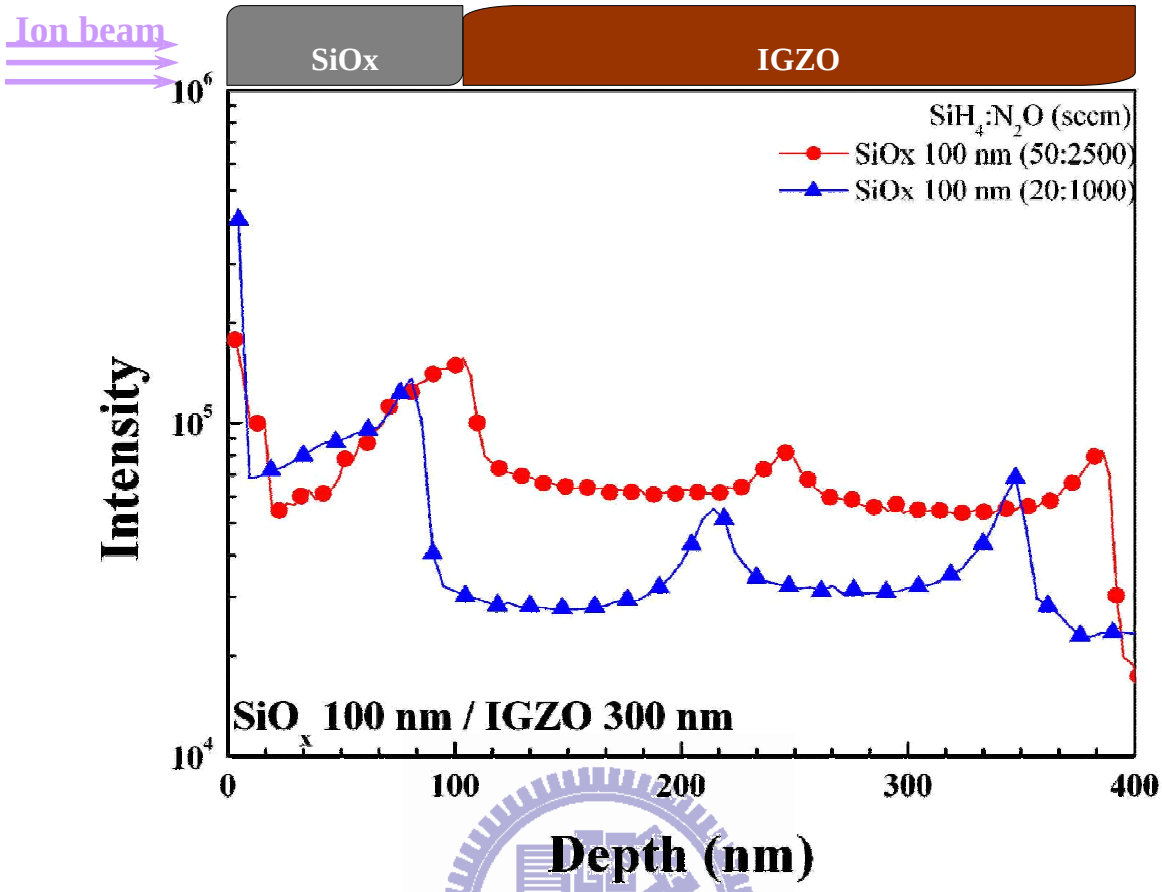


Fig. 4-23 The depth profile of SEMS of SiOx/a-IGZO deposited with SiH_4 flow rate at 50 sccm and 20 sccm. (H atomic)

Table

Table 2-1 Features of top contact and bottom contact structures.

	Top contact	Bottom contact
Advantage	better TFT performance	easy to make higher resolution
	easy to control interface	easy to make short channel
	easy to control active layer formation	
Disadvantage	shadow mask for S/D pattern	worse TFT performance
	difficult to control channel length	degradation during the process
	difficult to control alignment	
	difficult to make high resolution	
	difficult to make large TFT array	

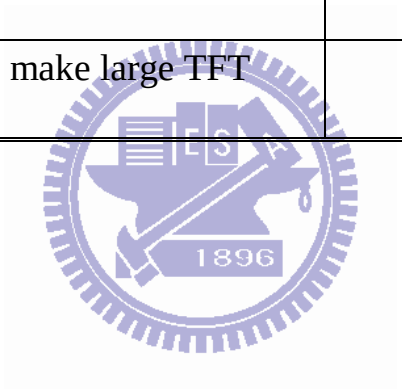


Table 3-1 Experimental Flow Path.

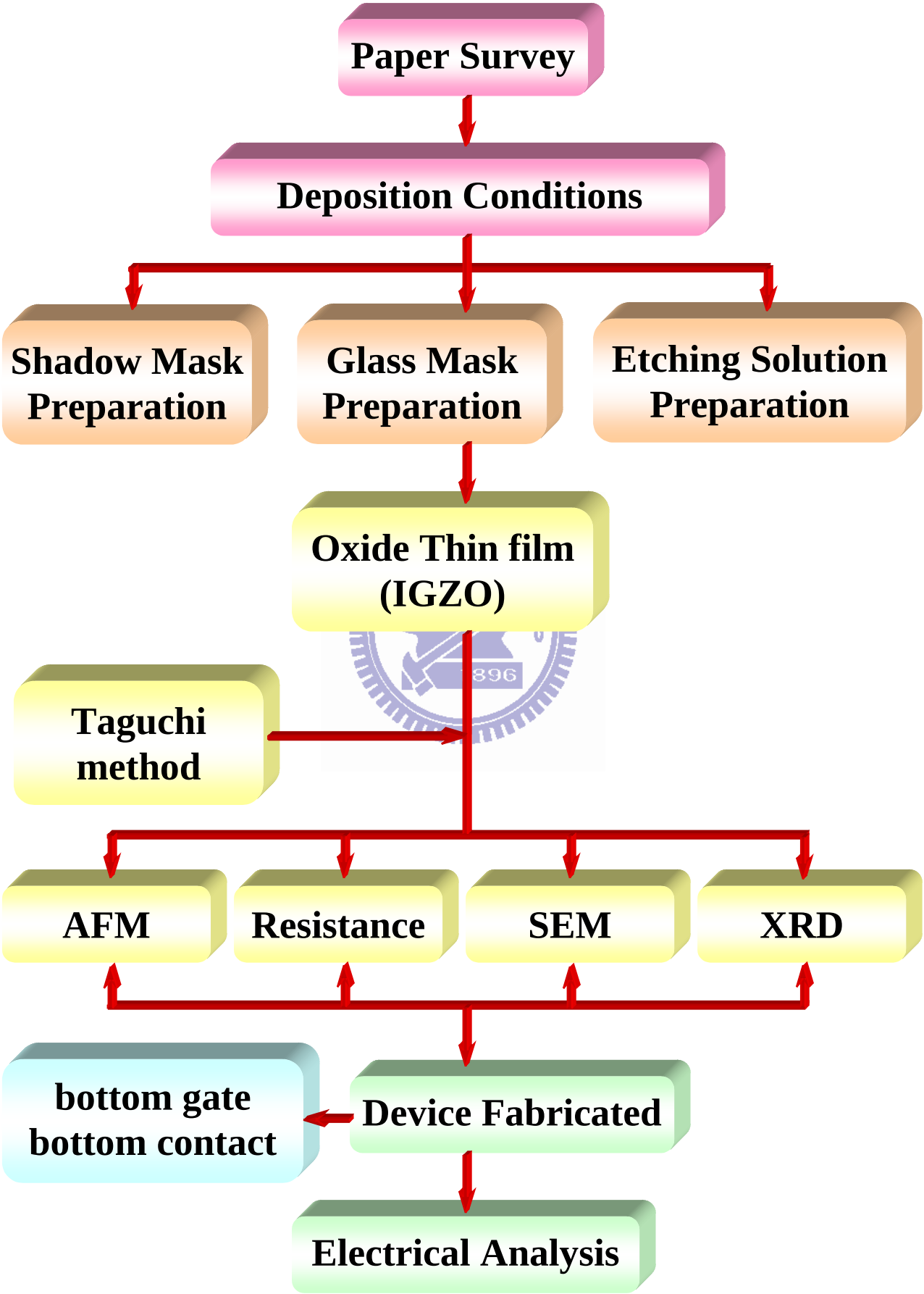


Table 3-2 a-IGZO TFT device fabrication Flow Path.

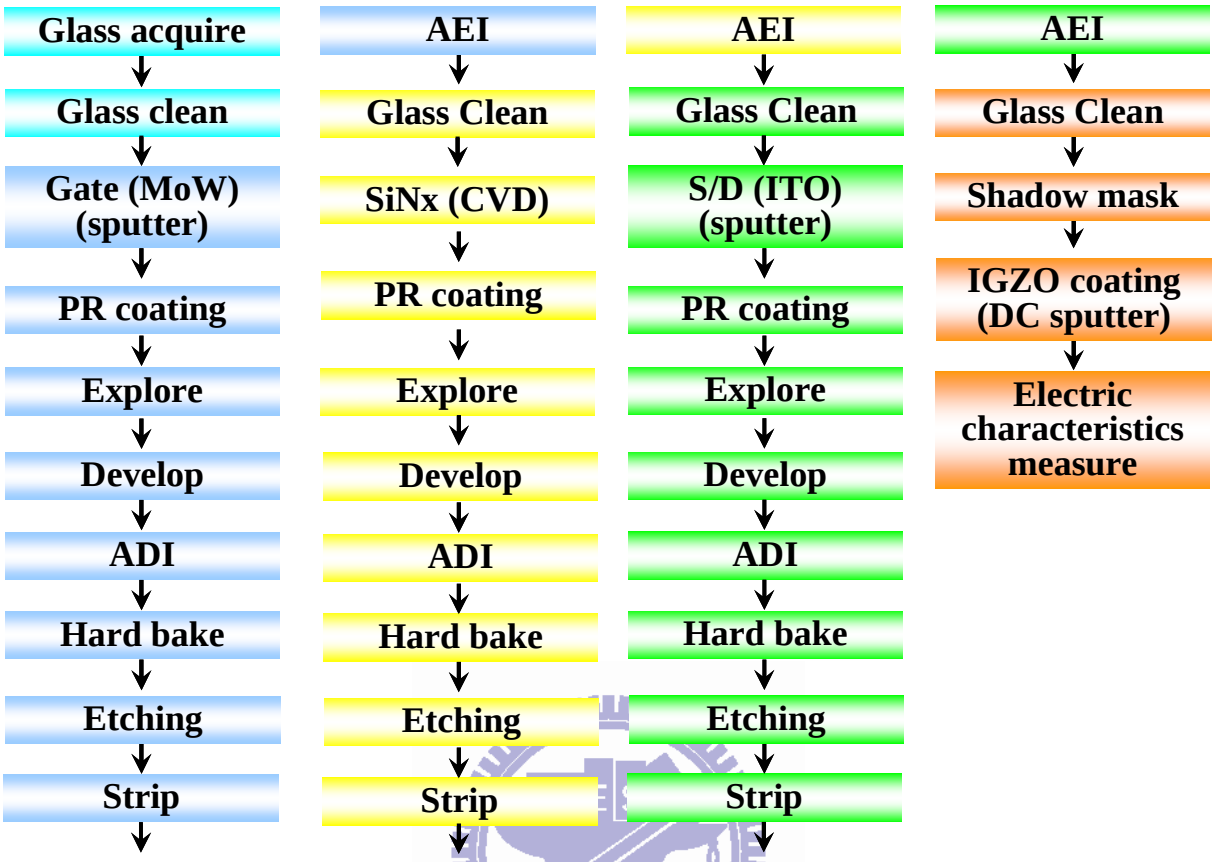


Table 3-3 Conditions of the DC power we applied.

dc power (kW)	Sub. move rate (mm/min)	O_2/Ar (sccm)	Thickness (Å)	Uniformity (%)	Sheet electric resistance	
					(Ω/□)	(Ω•cm)
1	300	2/50	≈ 287	6.3	7 – 12 E+12	2 – 3.4 E+07
1.5	300	2/50	≈ 450	4.1	8.3 – 15 E+12	3.7 – 7 E+07
2	300	2/50	≈ 581	4.5	1.06 – 1.6 E+13	6 – 9.3 E+07

Table 3-4 Conditions of the substrate move rate applied.

dc power (kW)	Sub. move rate (mm/min)	O_2/Ar (sccm)	Thickness (Å)	Uniformity (%)
1.5	100	2/50	≈ 1349	1.5
1.5	200	2/50	≈ 647	2.9
1.5	300	2/50	≈ 450	4.1
1.5	400	2/50	≈ 332	6.3
1.5	600	2/50	≈ 215	7
1.5	800	2/50	≈ 158	7.3
1	100	0.5/50	≈ 1094	2.6
1	200	0.5/50	≈ 523	3.3
1	400	0.5/50	≈ 270	7.6

Table 3-5 Conditions of the oxygen flow rate applied.

dc power (kW)	Sub. move rate (mm/min)	O_2/Ar (sccm)	Thickness (Å)	Uniformity (%)	Sheet electric resistance	
					(Ω/□)	(Ω•cm)
1	150	0.1/50	≈ 731	4.7	2.1 – 9.6 E+05	1.5 – 7
3	500	0.8/50	≈ 596	6.7	3.1 – 12 E+05	1.9 – 7.2
5	850	0.45/50	≈ 385	8.5	3.6 – 15 E+05	1.4 – 5.8
2.3	120	2/50	≈ 1748	2.7	1 E+11~12	1.7 E+06~07
2.3	200	3/50	≈ 957	4.2	3 E+11~12	2.9 E+06~07
2.3	400	4/50	≈ 448	5.5	1 E+12~13	4.5 E+06~07
2.3	600	5/50	≈ 248	7.3	3.5 – 7.3 E+13	8 – 18 E+07
2.3	800	5/50	≈ 207	8.2	2 E+13~14	4 E+07~08
2.5	100	2/50	≈ 2156	5.6	5 E+09~10	1 E+05~06

Table 4-1 The performance for a-IGZO TFTs before and after thermal annealing.

O2 (sccm)	**0.65**	**0.7**
V_{th} (V) (unannealed)	2.44 (-7.44)	2.46 (-2.87)
μ (cm^2/V-s)	2.5	3.07
s.s. (V/dec)	0.68	0.69
on/off ratio	8.34E+07	1.21E+08

Table 4-2 The performance of the a-IGZO TFTs with the DC sputter power.

DC power (KW)	1		1.5		2.3	
O_2 (sccm)	0.5	0.65	0.5	0.65	0.5	0.65
V_{th} (V)	4.5	4.8	4.08	4.14	3.82	3.77
μ (cm^2/V-s)	3	2.6	3	3.1	3.05	3.09
s.s. (V/dec)	0.5	0.54	0.3	0.31	0.26	0.24
on/off ratio	7.14E+08	4.27E+08	7.84E+08	9.17E+08	8.07E+08	1.07E+09

Table 4-3 The performance of the a-IGZO TFTs with the oxygen flow rate.

O2 (sccm)	0.65	0.7	0.75	0.85
V_{th} (V)	2.44	2.46	2.57	2.47
μ (cm^2/V-s)	2.5	3.07	2.65	2.88
s.s. (V/dec)	0.68	0.69	0.7	0.53
on/off ratio	8.34E+07	1.21E+08	3.35E+07	8.77E+07

Table 4-4 The performance of the a-IGZO TFTs with the SiOx (rich H atomic) passivation.

O2 (sccm)	origin	SiOx	250℃ 1hr Anneal	300℃ 1hr Anneal
V_{th} (V)	0.55		-6.24	-2.58
μ (cm^2/V-s)	4.86		4.25	4.56
s.s. (V/dec)	0.1		0.36	0.18
on/off ratio	4.3E+10		5.9E+07	1.4E+09

Table 4-5 The performance of the a-IGZO TFTs with the SiOx (less H atomic) passivation.

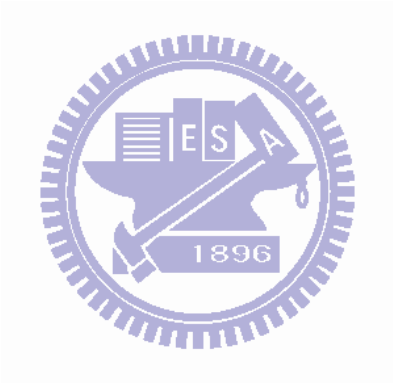
O2 (sccm)	origin	SiOx	250℃ 1hr Anneal	300℃ 1hr Anneal
V_{th} (V)	0.71		0.77	0.07
μ (cm^2/V-s)	3.6		4.04	4.42
s.s. (V/dec)	0.24		0.11	0.11
on/off ratio	4.0E+10		1.2E+10	6E+10

Table 4-6 The device characteristics of the a-IGZO TFTs with none passivation.

O2 (sccm)	1st day	2nd day	7th day	14th day	21th day
V_{th} (V)	0.15	0.66	0.58	1.25	1.09
μ (cm^2/V-s)	2.94	3.07	3.04	3.05	3.04
s.s. (V/dec)	0.21	0.29	0.35	0.33	0.39
on/off ratio	4.41E+09	4.38E+09	2.19E+09	4.33E+07	1.94E+07

Table 4-7 The device characteristics of a-IGZO TFTs with SiOx (less H atomic) passivation.

O2 (sccm)	1st day	2nd day	7th day	14th day	21th day
V_{th} (V)	1.17	0.58	0.33	0.1	0.11
μ (cm^2/V-s)	3.83	4	4.36	4.16	3.63
s.s. (V/dec)	0.32	0.22	0.31	0.20	0.28
on/off ratio	1.15E+10	1.24E+10	1.39E+10	2.61E+09	1.17E+10



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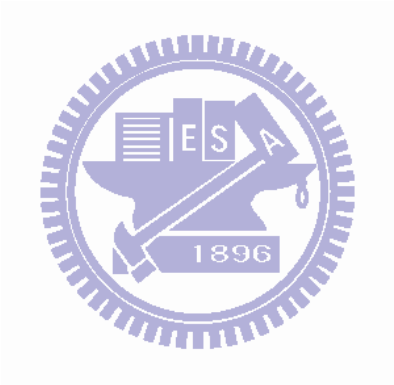

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