應用直接數位頻率合成器架構數位調變器

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摘　　要

本論文嚐試著以直接數位頻率合成器實現一個可做FSK,DFSK,BPSK及QPSK等不同形式調變之數位調變器,而此數位調變器則是架構在直接數位頻率合成器,論文中亦討論正弦相位輸入及輸出位元數對正弦輸出特性的影響,進而利用兩段直線作為正弦值的起始猜測值及 ROM 作為補償值逼近正弦值,在可接受的 SFDR 下採用分割 ROM 補償值來降低 ROM 的大小。ROM 表被分為粗細兩個表,粗表含有384位元,細表含有192位元,共用到ROM表大小為576位元, 在合成頻率中,模擬結果最差的SFDR可達61dBc,相關控制電路只用到加法器,不需減法及乘法器,與相同規格的直接數位頻率合成器比較,所用到的 ROM 表大小及所需控制電路皆比較小,只是需要稍微犧牲 SFDR 特性。本文同時利用所提出的直接數位頻率合成器實現一個可做 FSK,DFSK,BPSK 及 QPSK 等不同形式具正餘弦調變輸出之數位調變器,最後使用 Synplify Pro 合成 verilog 碼, 並以 Altera EPK100ARC240-1 作為數位調變器功能的驗證,用到 238 邏輯單元(4%)及 1152 記憶位元(2%)IC 資源。

Application Of Direct Digital Frequency Synthesizer In Digital Modulator

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Abstract

In this thesis, we propose a digital modulator with FSK, DFSK, BPSK and QPSK function by using direct digital frequency synthesizer (DDFS). For DDFS, the spur item were caused by finite output word length, phase truncation and sine/cosine mapping function (SCMF) are also presented. The initial guess and error correct ROM table are used to approximate the sine function, Initial guesses techniques using 2-segment line approximation. In order to reduce the ROM size, the ROM memory was partitioned into two ROM blocks. Coarse ROM (384 bits) and fine ROM (192 bits) were explored. The total size of ROM table is 576 bits. Only adder circuits were required in the additional circuits. No subtractor and multiplier were needed. Simulation shows that the worst case of SFDR (spurious free dynamic range) is 61dBC for various output frequency. When we compared with other same spec DDFS, Rom table size and additional circuits are smallest, but under sacrificing the performance of SFDR. The proposed DDFS is used to implement the digital modulator with FSK, DFSK, BPSK and QPSK function; the digital modulator is also with sine/cosine output. Using Synplify Pro to synthesize the verilog code and Altera device EPF10K100ARC240-1 to verify the function of digital modulator; it share the 238 logic elements (4%) and 1152 bits (2%) memory with device.

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