國立交通大學

電機學院　電子與光電學程

碩 士 論 文

應用於MP3播放器訊號處理器之鎖相迴路式頻率合成器之設計

Design of PLL-Based Frequency Synthesizer for DSP in MP3 Player

研　究　生：高明正

指導教授：溫瓌岸 博士

中　華　民　國　九　十　七　年　六　月

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摘要

MP3音樂壓縮格式具有極佳的方便性，被廣泛的應用在多媒體的播放與儲存，成爲今日非常重要的一種數位音響壓縮標準。一個MP3播放系統，可以藉由軟體或硬體設計的方式來達到不同聲音取樣頻率的效果。對於手持式裝置來說，通常採用硬體設計的方式來實現，藉由調整數位訊號處理電路的操作頻率，可以完成此設計需求。除此之外，由於數位電路的消耗功率與操作頻率成正比，經由變頻操作的方式，也可以達到降低功率消耗的效果。本論文描述一個應用於數位訊號處理器之鎖相迴路式頻率合成器之設計。此設計提供了一個可程式化的輸出時脈，可以讓數位訊號處理器有不同的操作頻率。在輸出的時脈頻率較高的情況下，操作的速度快，效能也比較高。在輸出的時脈頻率較低的情況下，則是可以

達到省電的效果。

此電路爲一完全積體化的設計，採用0.18微米的製程技術。電路所使用的基本時脈是由一個24MHz的晶體震盪器所產生。再經由一個除頻器，將此24MHz的基本時脈做除頻，藉以產生鎖相迴路所需的參考頻率。除此之外，電路中還包括了一個可程式化的除頻器，藉此來合成所需要的輸出時脈頻率。此頻率合成器之合成頻率範圍爲31.059MHz到81.882MHz。其工作電壓爲1.8伏特，並且要能容許正負十個百分比的電壓誤差。此頻率合成器經過量測後，顯示其鎖相迴路在所有的輸出情況下皆可以正常的鎖住相位。當量測輸出時脈頻率爲81.882MHz時，其時脈抖動爲85ps，最大消耗電流爲570μA。

Design of PLL-Based Frequency Synthesizer for DSP in MP3 Player

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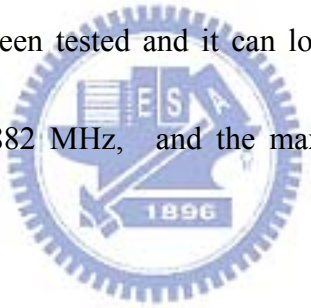
Abstract

MP3 compression format has been widely used in multimedia player and storage application for its convenient. It is an essential standard for digital audio compression nowadays. A MP3 player can implement different sampling rate in software or hardware design method. It is usually implemented in hardware design method especially for hand-held devices. It can be realized by adjusting the operating frequency of digital signal processing circuit. In addition, it will reduce the power consumption since the power consumption of digital circuit is proportional to operating frequency. In this thesis, the design of PLL-based frequency synthesizer for a digital signal processor (DSP) is described. It provides a programmable clock signal with variable frequency for DSP to operate in different condition. For higher speed and performance, a clock signal

with higher frequency is used. For power saving requirement, a lower frequency clock signal is used.

This circuit was fully integrated with a 0.18 μm 1P6M CMOS process. An 24 MHz crystal oscillator is used as a fundamental clock for this PLL. To generate the reference frequency for this PLL, a frequency divider is used to divide down the 24 MHz clock first. In addition, there includes a programmable frequency divider for frequency synthesizer. The frequency synthesizer is designed to generate a clock frequency from 31.059 MHz to 81.882 MHz. The supply voltage is 1.8 V with a ± 10% tolerance. The PLL has been tested and it can lock to all frequency range. The measured jitter is 85ps at 81.882 MHz, and the maximum current consumption is around 570uA.



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Contents

Figure Captions

Chapter 1. Introduction

1.1. Backgrounds

Phase Locked Loop (PLL) has been widely used in communications, wireless systems, digital circuits, and disk drive electronics, etc. It has played an important role in the high-technology industry. The main applications of PLL are synchronization [1], frequency synthesis [2], clock recovery [3], and so on. The PLL in CPU, for example, can be used to lock the phase between internal and external clock signals. Furthermore, it can be used to synthesize the frequency of internal clocks with multiple times of the frequency of external clock.

A PLL is a circuit synchronizing an output signal with a reference or input signal in frequency as well as in phase. It can be considered as a negative feedback control system. The basic building blocks of PLL are Phase Detector (PD), Loop Filter (LF) and Voltage Controlled Oscillator (VCO).

The PD is a circuit capable of delivering an output signal that is proportional to the phase difference between its input signal and the feedback signal. This output signal of PD consists of a dc component and a superimposed ac component. The latter is undesired, hence it is canceled by the loop filter. In most cases a first-order, low-pass filter is used. This dc control voltage from the loop filter controls the VCO output frequency. Due to the negative feedback, the loop will make sure the output signal is in phase with the reference signal. When this happens the phase error between the input and output frequencies is zero and PLL is said to be in lock.

As long as the initial difference between the input signal and the VCO is not too big, the PLL eventually locks onto the input signal. This period of frequency acquisition, is referred to as pull-in time, which depends on the bandwidth of the PLL. The

bandwidth of a PLL depends on the characteristics of the phase detector, voltage controlled oscillator and on the loop filter.

The above described architecture with a divider in the feedback is widely used as a frequency synthesizer and is shown in Figure 1.1. A PLL can be thought of as a synthesizer with output frequency equal to reference frequency. Most of the research in this field is done on optimizing individual building block to get better performance.

In this thesis, we design a PLL-based frequency synthesizer that is used for a digital signal processor (DSP) which will be used in digital audio player. To implement the effect of various sampling rate, the operating frequency of DSP should be adjustable. For different operation condition, the DSP needs a clock signal with different frequency. It can be realized by a programmable PLL frequency synthesizer. To meet the requirement, the divider in Figure 1.1 is designed to be programmable. The details about the design of this frequency synthesizer will be shown in the following chapters.

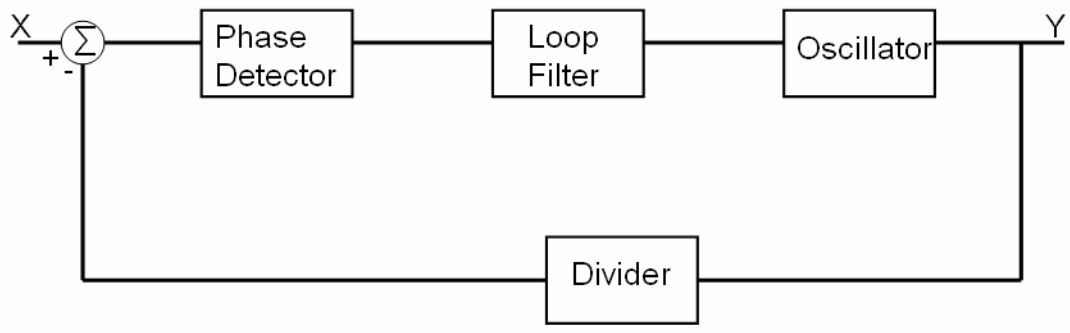


Figure 1.1 PLL-based frequency synthesizer

1.2. Organization of the Thesis

The thesis is organized into five chapters. In chapter 1, the background and organization of this thesis is introduced. In chapter 2, the review of fundamental principle and building blocks of the PLL-based frequency synthesizer is introduced. In chapter 3, the circuits of the building blocks of this frequency synthesizer are described. In chapter 4, the simulation results are illustrated. Chapter 5, the measurement results are illustrated. Chapter 6 gives the conclusion and future work of this thesis.

Chapter 2. PLL Building Blocks

2.1. Principle of Operation

A frequency synthesizer generates an output frequency which is the multiples of an accurate reference frequency (f_{ref}). Usually the synthesized frequency can be combined by two integer multiples over some range. The output frequency will be given by $f_{out} = (N \times f_{ref}) / M$, where N and M are integers.

A PLL is a feedback control system that operates on the excess phase of nominally periodic signals. As shown in Figure 2.1, a simple PLL consists of three basic blocks: Phase Detector (PD), Low-Pass Filter (LPF) and Voltage Controlled Oscillator (VCO).

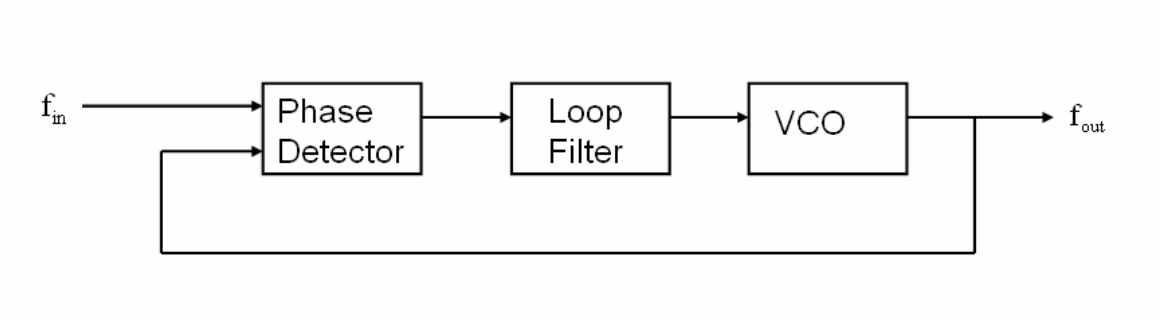


Figure 2.1 A basic phase locked loop synthesizer

A PD serves as an error amplifier in the feedback loop, thereby minimizing the phase difference ($\Delta\phi$) between f_{in} and f_{out}. The loop is considered locked if $\Delta\phi$ is constant with time, and the input and output frequencies are equal. In the locked

condition, all the signals in the loop have reached a steady state. The PD produces an output whose dc value is proportional to $\Delta\phi$. The low-pass filter suppresses the high-frequency components in the PD output, allowing the dc value to control the VCO frequency. The VCO then oscillates at a frequency equal to the input frequency and with a phase difference equal to $\Delta\phi$. Thus, the LPF generates the proper control voltage for the VCO. Before examining the overall loop operation, let us discuss the three building blocks in detail.

2.2. Phase Detector

The role of a phase detector in a PLL is to generate an error signal proportional to the phase error between the input signal and the VCO output signal. Let θ_d represents the phase difference between the input phase and the VCO phase. In response to this phase difference, the PD produces a proportional voltage (V_d). The relation between the voltage V_d and the phase difference θ_d is shown in Figure 2.2 [4]. The curve is linear and periodic, which repeats every 2π radians. This periodicity is necessary as a phase of zero is indistinguishable from a phase of 2π.

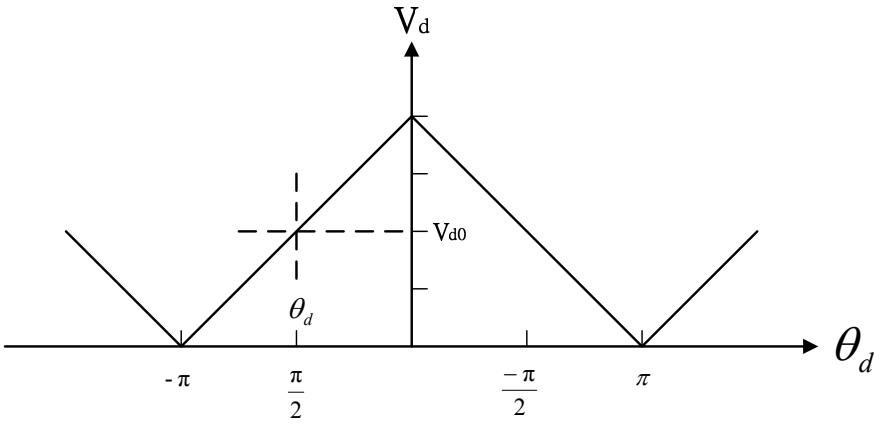


Figure 2.2 Phase detector characteristic

The slope of the curve gives the gain of PD, and is given by

$$K_d = \frac{dV_d}{d\theta_e} \tag{2.1}$$

where, $\theta_e = \theta_i - \theta_o$

A simple PD can be modeled by the following equation

$$V_d = K_d \theta_e + V_{do} \tag{2.2}$$

This is represented by the block diagram in Figure 2.3.

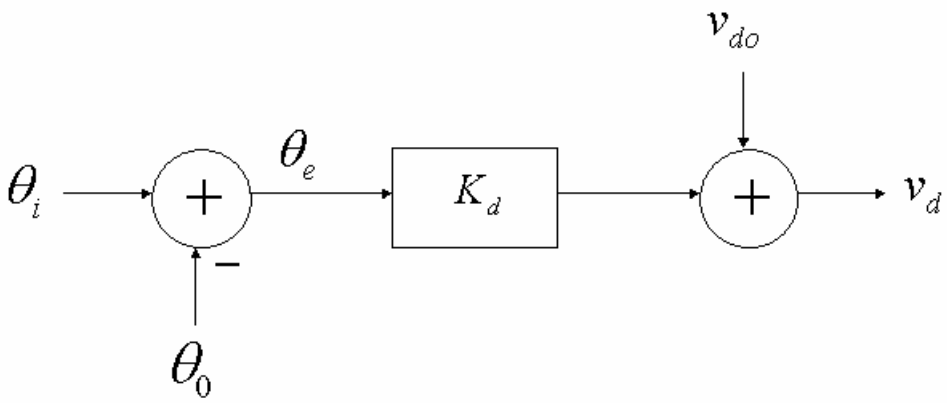


Figure 2.3 Signal flow model of phase detector

There are many ways to implement a PD circuit. Three types of phase detectors are implemented by EXOR gate, JK flip-flop and Phase Frequency Detector (PFD). EXOR and JK flip-flop output gives information about the phase difference between input signals, but do not have any information about the frequency difference. They are used anyway for the ease of implementation. More popular PD is PFD, which detects the difference in phase as well as frequency between input signals as the name implied.

2.3. Voltage Controlled Oscillator

A Voltage Controlled Oscillator (VCO) is a circuit whose output frequency ω_o is linearly proportional to the control voltage, V_c, which is generated by the phase detector. A typical VCO characteristic is shown in Figure 2.4.

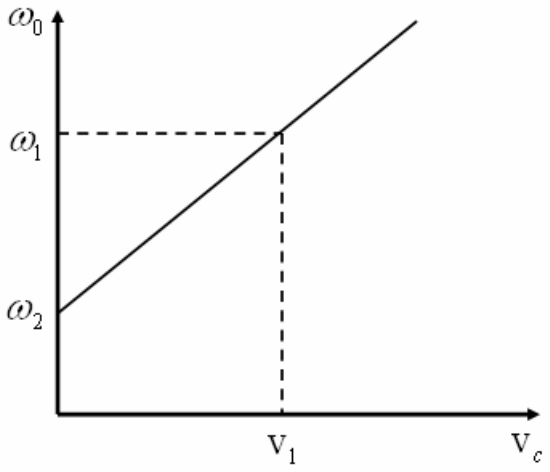


Figure 2.4 A typical VCO characteristic

Ideally the slope of the curve is constant. As the control voltage varies from 0 to V_1, the output frequency of the VCO varies from ω_2 to ω_1. Outside this range the curve may not be linear and the VCO performance becomes non-linear. Depending on the requirements of the circuit, the range can be selected such that the circuit always remains in its linear range. The slope of the curve is the VCO gain, K_o, which is given by

$$K_o = \frac{d\Delta\omega_o}{dV_c} \tag{2.3}$$

A simple VCO can be modeled by the following equation

$$\Delta\omega = K_o(V_c - V_{co}) \tag{2.4}$$

This is represented by the block diagram shown in Figure 2.5.

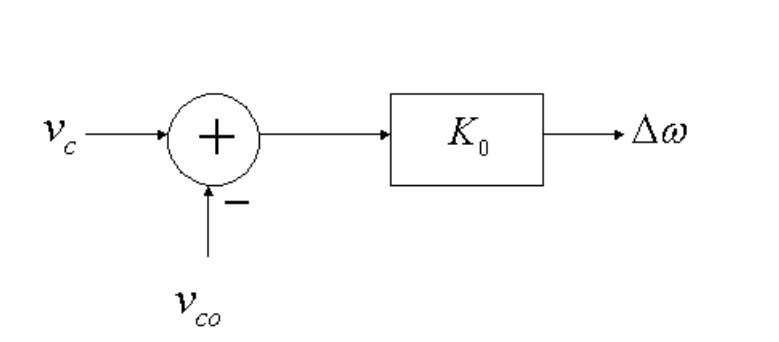


Figure 2.5 Signal flow model of VCO

2.4. Loop Filter

A loop filter lies between the VCO and CP to suppress high frequency components of data. The passive second-order loop filter is adopted in this design which is consisted of a resistor R and two capacitors C1, C2 as shown in Figure 2.6. If we focus on the serial R and C1, the transfer function of the filter can be expressed as:

$$F(S) = \frac{K(S + \omega_Z)}{S} \tag{2.5}$$

Where

$$\omega_Z = \frac{1}{R_1 C_1}, \quad K = R_1 \tag{2.6}$$

It is obviously to show that there are one pole on the original point to suppress high frequency component when open loop, and one zero to increase the phase margin. Afterward, we consider the other capacitor C2. It is used to add another pole to determine the loop bandwidth.

$$F(S) = \frac{K(S + \omega_Z)}{S \times (1 + \frac{S}{\omega_P})} \tag{2.7}$$

Where

$$K = \frac{R_1 \times C_1}{C_1 + C_2}, \quad \omega_P = \frac{C_1 + C_2}{R_1 (C_1 C_2)} \tag{2.8}$$

Thus some important constant in the PLL can be calculated based on the pole

and zero. The bandwidth will be

$$BW = \frac{I_P K_{VCO} R}{2\pi N} \frac{C_1}{C_1 + C_2} \tag{2.9}$$

And the phase margin will be

$$PM = \tan^{-1} \frac{BW}{\omega_Z} - \tan^{-1} \frac{BW}{\omega_P} \tag{2.10}$$

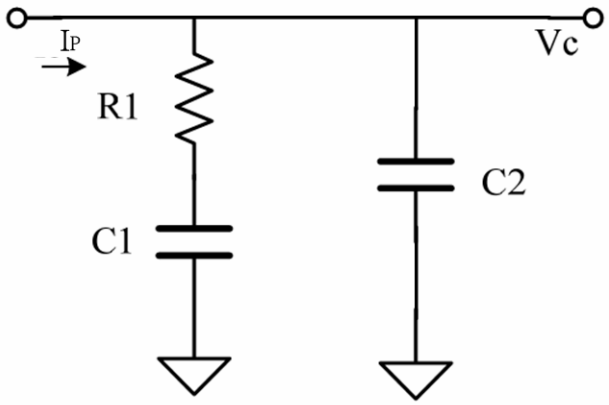


Figure 2.6 Second-order loop filter

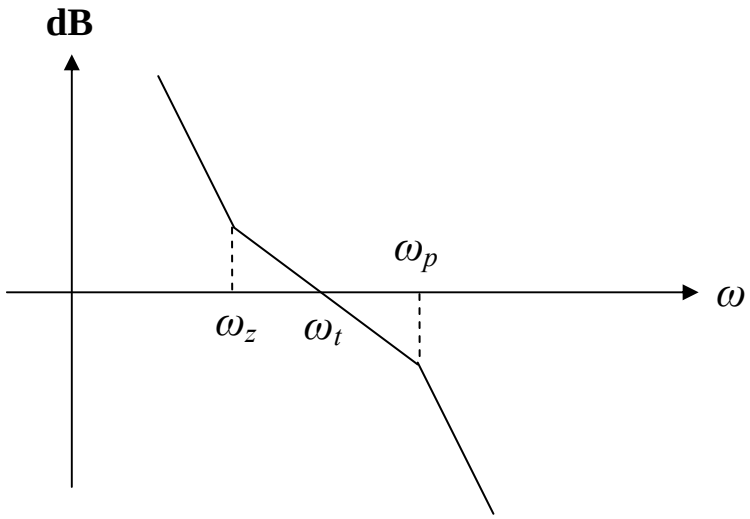


Figure 2.7 Loop response of third-order PLL

Figure 2.7 shows the frequency response of the third-order PLL, where ω_t is the unit-gain frequency. The goal of loop filter is to provide enough phase margin which is better between 30°~70°. However, it is always vied against response time and attenuation of noise. In general case, we usually let

$$\omega_P / \omega_t = \omega_t / \omega_Z = 4 \tag{2.11}$$

to have a phase margin around 60°.

2.5. Charge Pump

In the low-pass filter, the average value of the PD output is obtained by depositing or removing charge onto a capacitor during each phase comparison. In a charge pump, on the other hand, there is negligible decay of charge between phase comparison instants. Charge pump consists of two switched current sources driving a capacitor as shown in Figure 2.8 [4].

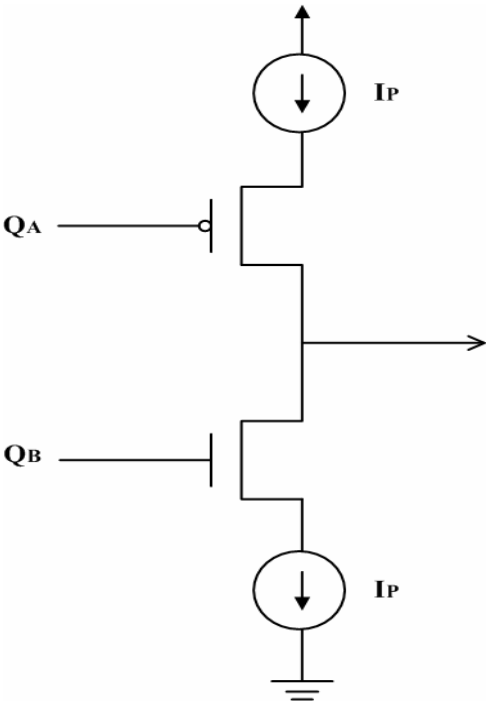


Figure 2.8 Charge pump

Charge pump is used mostly with PFD. In Figure 2.8, let Q_A and Q_B be the up and down outputs of PFD and I_P is the charge pump current. The up and down are a series of pulse width signal, which represent one input of the PFD leads or lags the other input signal.

Each field effect transistor (FET) acts as a simple switch to source or sink charge with respect to Q_A or Q_B. The output is pulled high and I_P sources charge to loop filter when Q_A goes low since the upper switch is a PMOS FET. The output is pulled low and I_P sinks charge from loop filter when Q_B goes high since the lower switch is a NMOS FET. The output current of charge pump is thus a logical function of the PFD state. When PFD is in state 1, the output current must be positive, and when PFD

is in state 2, the output current must be negative. For state 0, the output current will be zero. If we plot the average output current ($\overline{I_d}$) vs. phase error (θ_e), a sawtooth waveform will be obtained as shown in Figure 2.9.

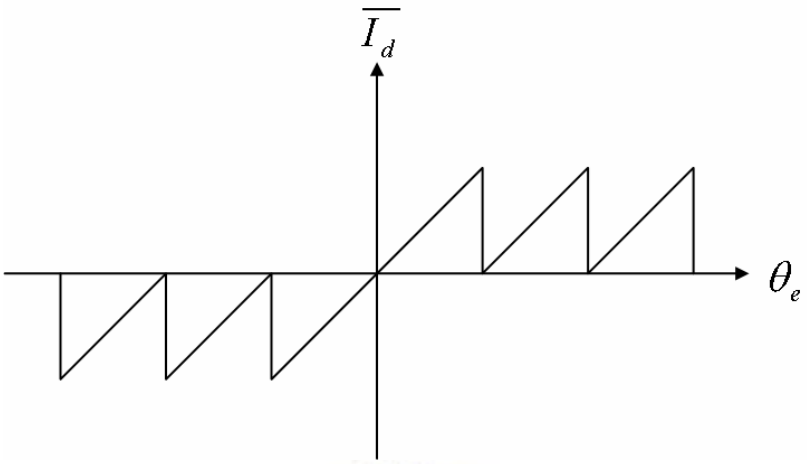


Figure 2.9 Average output current vs. phase error plot

The curve is linear between -2π to 2π, and then repeats every 2π. If θ_e exceeds 2π, the PFD behaves as if the phase error is rotated back to zero. Hence it is a periodic curve with a period of 2π. The gain of PFD is calculated as

$$K_d = \frac{I_P}{2\pi} \tag{2.12}$$

2.6. PLL Bandwidth

The bandwidth of a PLL determines how fast a PLL output will track the input frequency. This parameter is dependent on the characteristics of PD, VCO and the loop filter. Since the bandwidth is associated with the ac model, let us consider an ac model of PLL which is shown in Figure 2.10 [5].

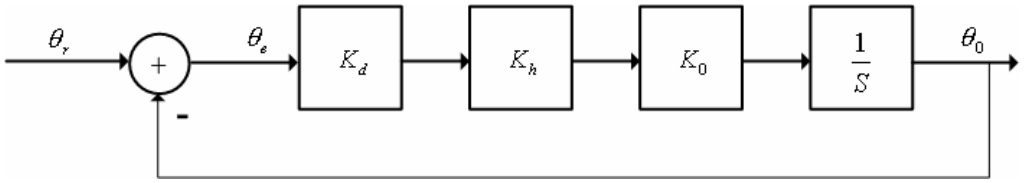


Figure 2.10 Linear model of a PLL

The VCO can be represented by an integrator whose transfer function is $\frac{1}{s}$, where s represents complex frequency. The closed loop transfer function $H(s)$ is given by

$$H(s) = \frac{\theta_0(s)}{\theta_r(s)} = \frac{G(s)}{1+G(s)} \tag{2.13}$$

where

$$G(s) = \frac{K_d K_h K_0}{s} \tag{2.14}$$

The bandwidth ω_{3dB} occurs when $|G(j\omega)| = 1$. From the above equation, this occurs when

$$\omega_{3dB} = K_d K_h K_0 \tag{2.15}$$

The bandwidth of the PLL is thus determined by

- Gain of PD, K_d
- High frequency gain of loop filter, K_h
- Gain of VCO, K_0

The design of PD , VCO and loop filter determine the bandwidth of the PLL. The selection of loop bandwidth is a trade-off between the frequency acquisition speed and noise rejection ratio. Since PLL pull-in speed is a function of the loop bandwidth, the simplest method for improving the lock time is to widen the loop bandwidth. Though wider bandwidth improves the lock time, it degrades the noise characteristics of the PLL. From the above description, it is known that an optimum bandwidth depends on the system architecture and requirements of the specification.

2.7. Design Parameters of the PLL-Based Frequency Synthesizer

PLL is essentially a feedback system as shown in Figure 2.11. How the PLL behaves with different input functions is dominated by the type and order of the low pass filter. In this thesis, the type-II charge pump PLL is adopted to implement the frequency synthesizer. However, since the order of the PLL is larger than 2, the loop stability should be taken into consideration How to adjust the loop bandwidth to suppress the output phase noise (or jitter) is a trade off between the reference input noise and the VCO. Thus, how to set the parameters of the PLL is an important issue.

The transfer function of the loop filter is given by

$$F(s)=\frac{1+SR_1C_1}{S(C_1+C_2)+S^2R_1C_1C_2} \tag{2.16}$$

Because C_1 is usually much larger than C_2, to simplify the PLL design, the transfer function of the loop filter can be simplified as

$$F(s)\approx\frac{1+SR_1C_1}{SC_1(1+SR_1C_2)}=\frac{1+\frac{S}{Z_1}}{SC_1(1+\frac{S}{P_1})} \tag{2.17}$$

where $Z_1=\frac{1}{R_1C_1}$ and $P_1=\frac{1}{R_1C_2}$. Thus, the open-loop transfer function of the PLL can be given by

$$G(s) = \frac{I_p K_o (1 + \frac{S}{Z_1})}{2\pi C_1 S^2 (1 + \frac{S}{P_1})} \tag{2.18}$$

And the close-loop transfer function of the PLL is given by

$$H(s) = \frac{I_p K_o (1 + \frac{S}{Z_1})}{2\pi C_1 (S^2 + \frac{I_p K_o R_1}{2\pi N} S + \frac{I_p K_o}{2\pi N C_1})} \tag{2.19}$$

The natural frequency and the damping factor can be derived as

$$\omega_n = \sqrt{\frac{I_p K_o}{2\pi N C_1}} \tag{2.20}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_o C_1}{2\pi N}} \tag{2.21}$$

The bandwidth of the PLL is usually implied in ω_n, but the real 3-dB bandwidth ω_{3dB} should be the open loop gain of the PLL that is given by

$$K = \frac{I_p R_1 K_o}{2\pi N} \tag{2.22}$$

According to [6], the loop bandwidth should be about 10 times smaller than the reference frequency. If ζ is too large, the acquisition process may be longer. If ζ is too small, the transient response may have ripples or becomes unstable. Since the acquisition time is not critical for the application. A larger ζ will be used in this design

for a stable operation.

In this thesis, $\zeta = 0.9 \sim 1.5$ and $\omega_n = \omega_{ref}/10 \sim \omega_{ref}/20$ are adopted to design the PLL frequency synthesizer.

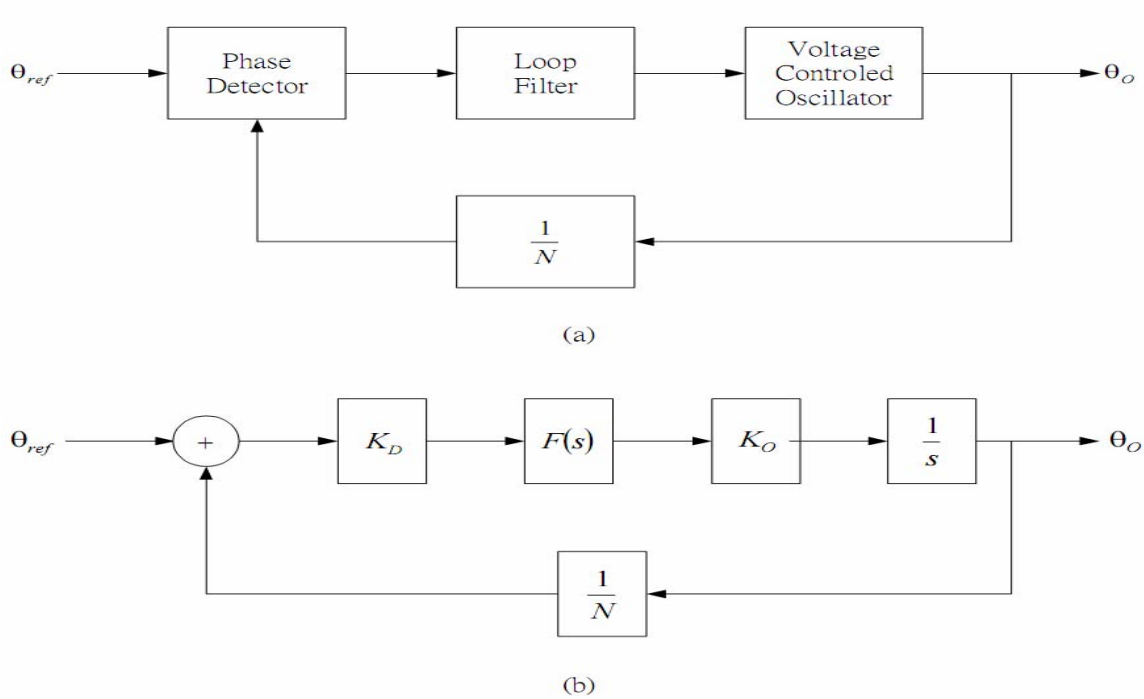


Figure 2.11 PLL-based frequency synthesizer (a) Block diagram. (b) Linear model.

2.8. Operation frequency range

The operation frequency will range from 31.059 MHz to 81.882 MHz. The damping factor and bandwidth of PLL will vary with the VCO gain, pump current, loop filter parameters, and feedback ratio. Since only a set of VCO is used and the VCO gain is decided and fixed when the circuit structure is chosen, the N value of programmable divider in the feedback path will influence the damping factor and bandwidth of the PLL. To compensate damping factor and bandwidth of the PLL to a stable value, an auxiliary current mirror is used to implement the requirement. The damping factor is designed within 0.9 ~ 1.5 and the loop bandwidth is within one-tenth of the reference frequency.

Chapter 3. Design and Analysis of the Circuits

3.1. Introduction

The basic building block and operation principle has been illustrated in the previous chapters. System architecture of the programmable PLL with variable output frequency will be provided in the following section. Circuit level design and analysis will be discussed in this chapter as well. HJ 0.18μm CMOS process is adopted for implementation. Design and simulation results of the circuit are accomplished in Hspice.

3.2. System Architecture

System architecture of the programmable PLL is provided in Figure 3.1. Since the output frequency of PLL will change with the feedback divider ratio. A 5-bits register, PLL[4:0], is used to control the feedback divider ratio. To synthesize the required frequency, a divide-by-17 divider is used to divide down the input frequency from the 24MHz crystal oscillator. A set of current source is injected directly to the VCO to raise the oscillation frequency of ring oscillator. The mapping table of control registers and output frequency is provided in Table 3.1.

As it is discussed in Chapter 2. , the design parameters of PLL will change with

the feedback divider ratio. In order to meet the requirement for building a stable PLL and still cover all the operation frequency range, the choose of all the design parameters must be calculated carefully. The parameters are provided as follows, the charge pump current is 10μA, the resistance and capacitance of loop filter are 240pF, 24pF and 32k Ω.

Since the VCO gain is fixed if only one set of ring oscillator is used. In order to have a stable PLL and wide frequency range without change the VCO gain, an extra current source is provided to raise the frequency level of ring oscillator. An illustration of this phenomenon is shown in Figure 3.2. In Figure 3.2, Iv_2i represents the current comes from V-I converter of VCO, I_0 and I_1 represent constant current source mirrored from other bias circuit. As it can be seen in the figure, the oscillation frequency will be raised up by the additional current source, I_0 or I_1. The slope represents the VCO gain (Kvco), which is not changed by I_0 or I_1. As it is illustrated, the operation frequency range is limited to delta f1 if there is only Iv_2i is used. The operation frequency range will be extended to delta f2 by using the addition current source.

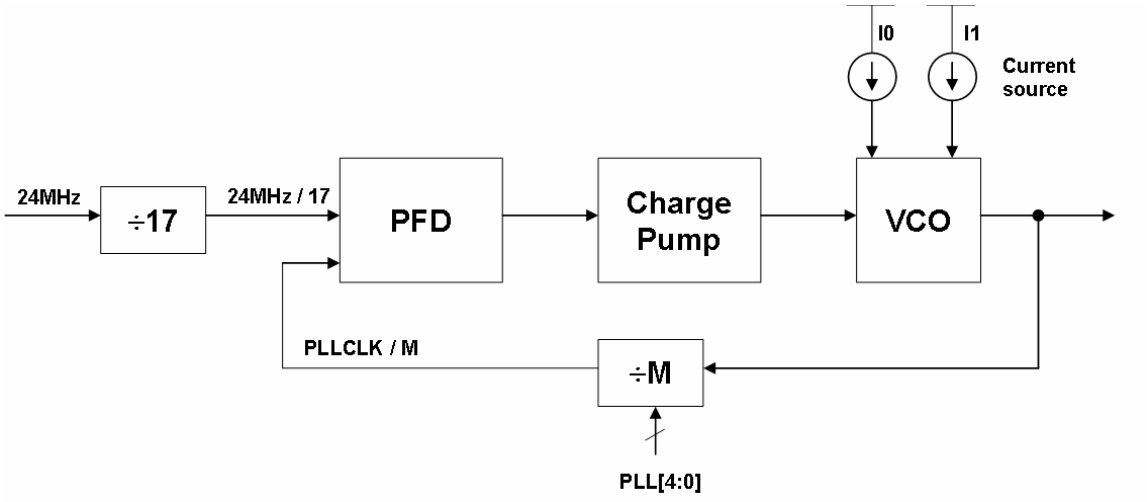


Figure 3.1 System architecture of the programmable PLL.

PLLCLK (MHz)	M	PLL[4:0]
31.059	22	0
33.882	24	1
36.706	26	2
39.529	28	3
42.353	30	4
45.176	32	5
48.000	34	6
50.824	36	7
53.647	38	8
56.471	40	9
59.294	42	10
62.118	44	11
64.941	46	12
67.765	48	13
70.588	50	14
73.412	52	15
76.235	54	16
79.059	56	17
81.882	58	18

Table 3.1 The mapping table of control registers to divider ratio and output frequency.

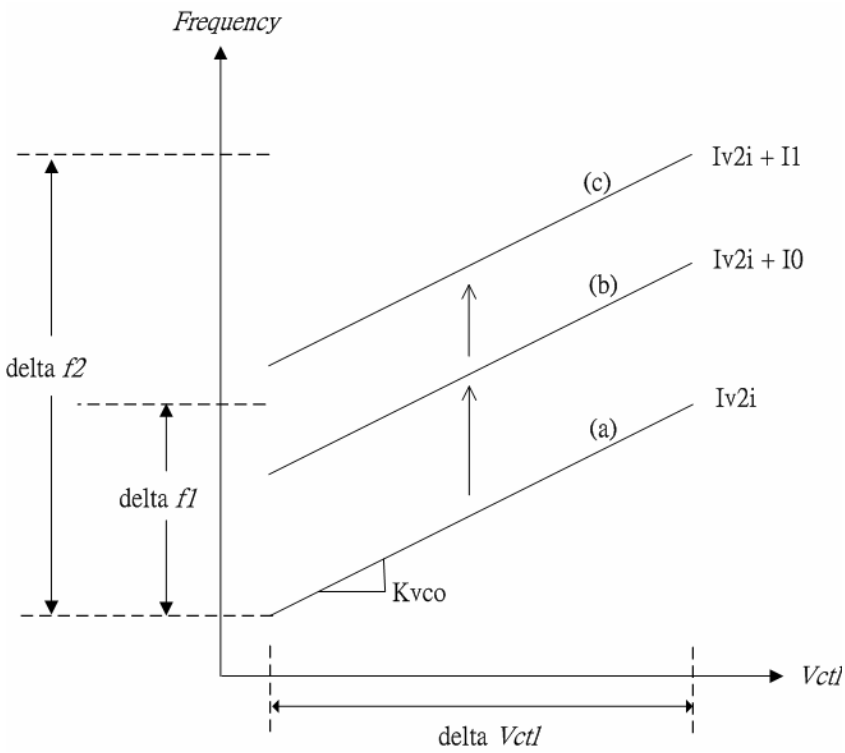


Figure 3.2 The operation frequency range of VCO to additional current source.

3.3. Circuit Description

3.3.1. Phase Frequency Detector

Many different types of phase detectors are available. In this thesis, phase frequency detector (PFD) is used for implementation. It offers an unlimited pull-in range which guarantees PLL acquisition even under the worst operating conditions. A conventional phase frequency detector is shown in Figure 3.3.

As shown in Figure 3.3, if there exists phase or frequency difference between F_{REF} and F_{FB} then the UP and DW will have related responses. For example, if F_{FB}

is slower than F_{REF} then the UP and DW will be 1 and 0 respectively. The output signals make the charge pump to increase charge on the loop filter, which makes F_{FB} higher to catch up with F_{REF}, and vice versa.

There is dead zone [4] in PFD circuit as shown in Figure 3.4. Dead zone happens as the phase difference between input signals, F_{REF} and F_{FB}, becomes too small, the corresponding output signals will not be generated. Since the pulse width of PFD output is too small for the charge pump to react before reset, there will be phase error accumulate in VCO. To solve this problem, a modified PFD circuit is shown in Figure 3.5. The added delay in Figure 3.5 makes PFD outputs reset later, which provides enough time for the charge pump to react. The delay element can be constructed by a buffer.

The simulation results are shown in Figure 3.6. As it can be seen in the figure, the UP and DW signals response to the small phase difference between F_{REF} and F_{FB} exactly.

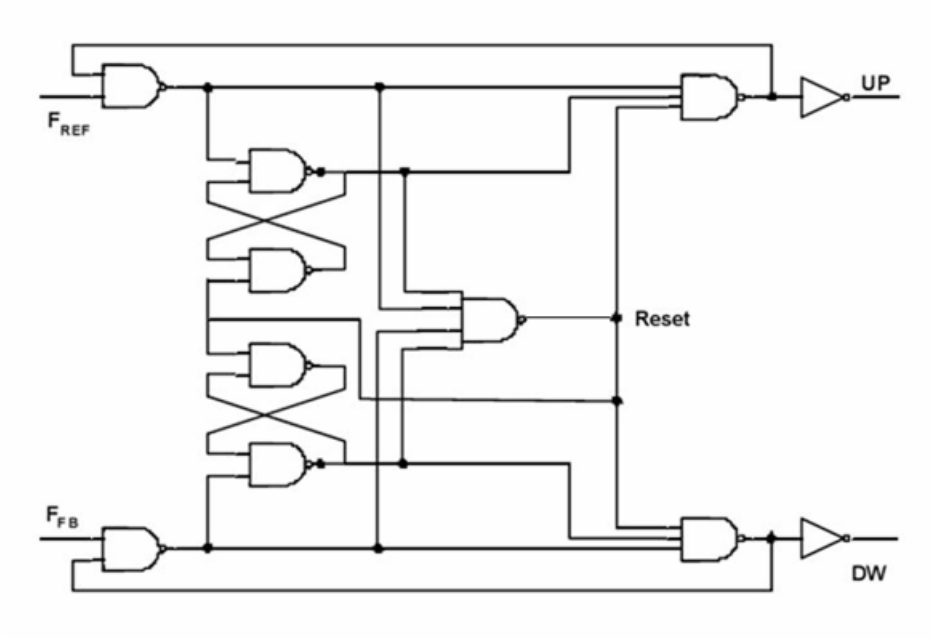


Figure 3.3 A conventional PFD circuit

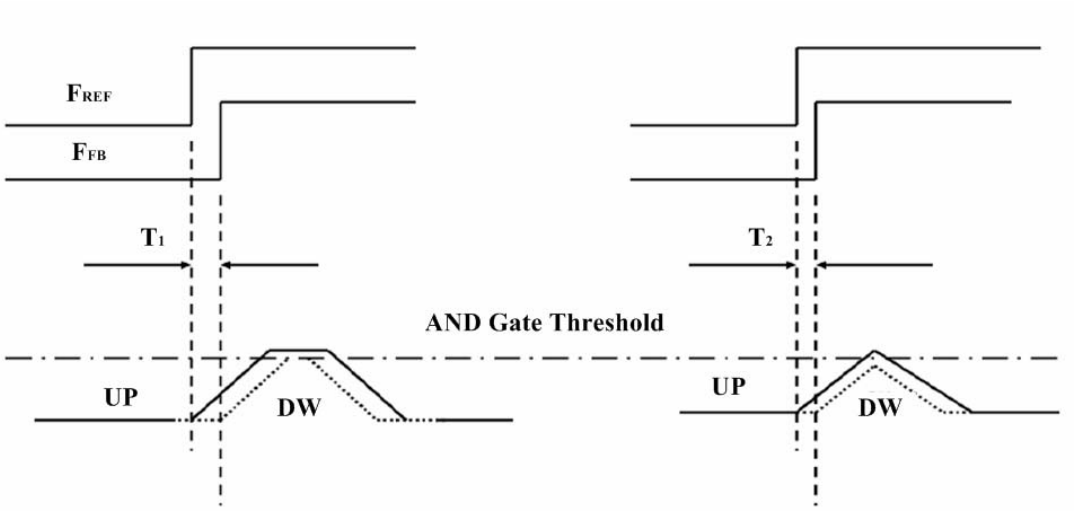


Figure 3.4 The illustration of dead zone

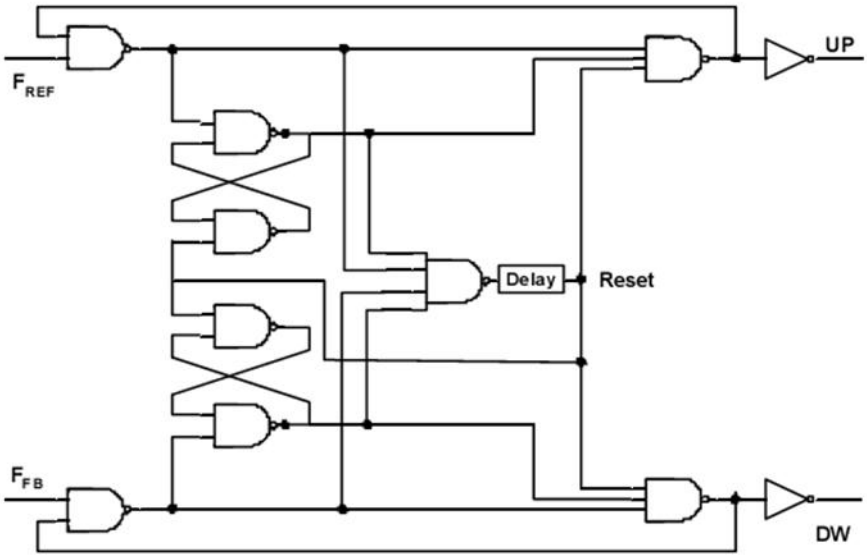
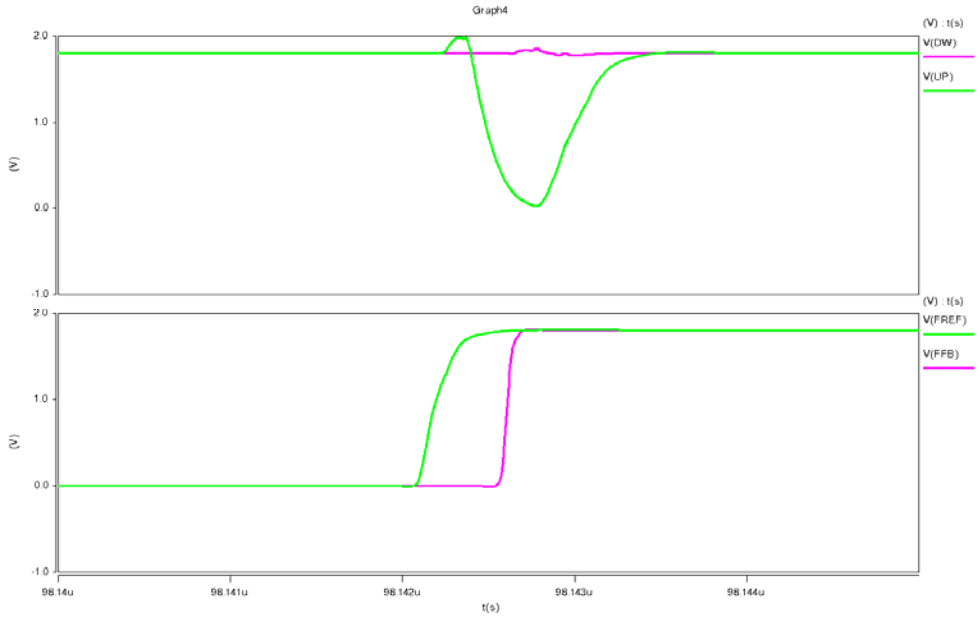
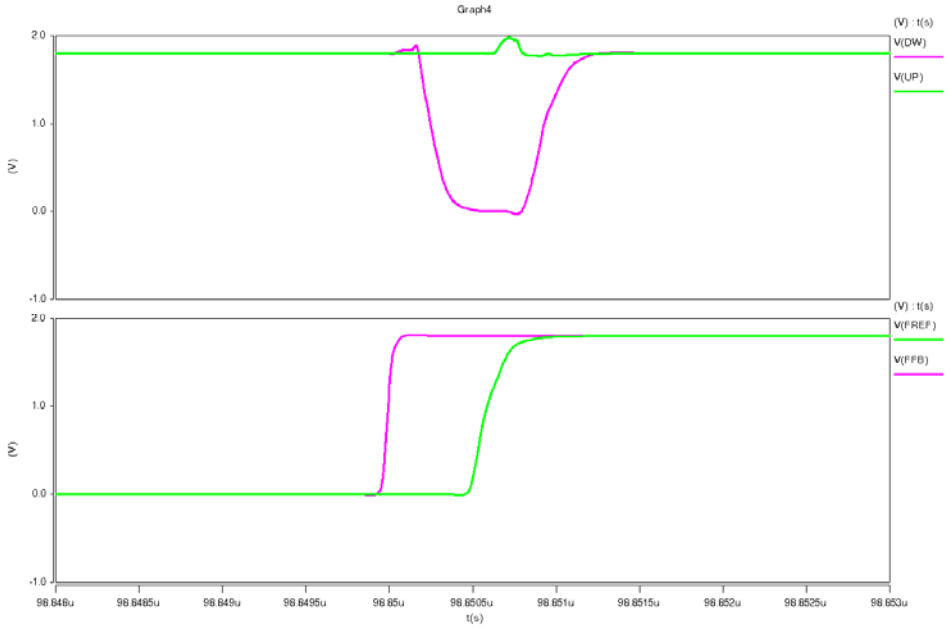


Figure 3.5 PFD circuit without dead zone


Graph4
(V) : t(s)
V(DW)
V(UP)
(V) : t(s)
V(FREF)
V(FFB)
(V)
2.0
1.0
0.0
-1.0
98.14u
98.141u
98.142u
98.143u
98.144u
t(s)

(a)


Graph4
(V) : t(s)
V(DW)
V(UP)
(V) : t(s)
V(FREF)
V(FFB)
(V)
2.0
1.0
0.0
-1.0
98.648u
98.6485u
98.649u
98.6495u
98.65u
98.6505u
98.651u
98.6515u
98.652u
98.6525u
98.653u
t(s)

(b)

Figure 3.6 Simulation results of PFD. (a) F_{REF} is phase lead and (b) F_{FB} is phase lag

3.3.2. Voltage Controlled Oscillator

The VCO is a critical building block in PLL and it is a main source of output jitter. The source of VCO noise is produced from devices, power source and substrate. The noises from devices include the thermal noise, the shot noise and flicker noise ($\frac{1}{f}$ noise). The main noises from power source and substrate are produced by the digital part of the whole circuits. The digital circuits in action produce very large currents that perturb power source and substrate, and then the noises are coupled into the VCO.

How to design a VCO with low noises from devices has been devoted by [7], [8], [9], and [10], which had analyzed in detail the clock jitter due to the noises from devices and derived several design principles.

1. The clock jitter is inversely proportional to $(V_{gs} - V_t)$ of the transistor.

2. For fixed output period, there is an inverse relationship between jitter and power consumption.

3. The up-conversion of low-frequency noise can be reduced by making the transitions more symmetric in terms of rise and fall time.

4. For fixed power consumption and fixed output period, increase in the number

of stages do not impact the jitter in single ended oscillators, but it increases the jitter in differential oscillators.

Utilizing these design principles, the VCO with low noises from devices can be designed. However, when the VCO is put next to a large digital circuit, the noises from supply and substrate dominate the noise of the VCO. The jitter due to the noises from devices is typically hundreds femto-seconds, but the noises from supply and substrate will result in a pico-second jitter. Therefore, how to design a VCO with low sensitivity to supply and substrate is an important issue.

The differential ring oscillator is used in our design for its lower sensitivity to supply and substrate noise [11]. The delay cell is shown in Figure 3.7. It uses a symmetric load to reduce supply noise, and the NMOS mirror is biased by a self-bias circuit to suppress the impact of subtract. Moreover, the delay cell has a first-order linearity to simplify the design of the PLL. The explanations about the VCO are shown as follow.

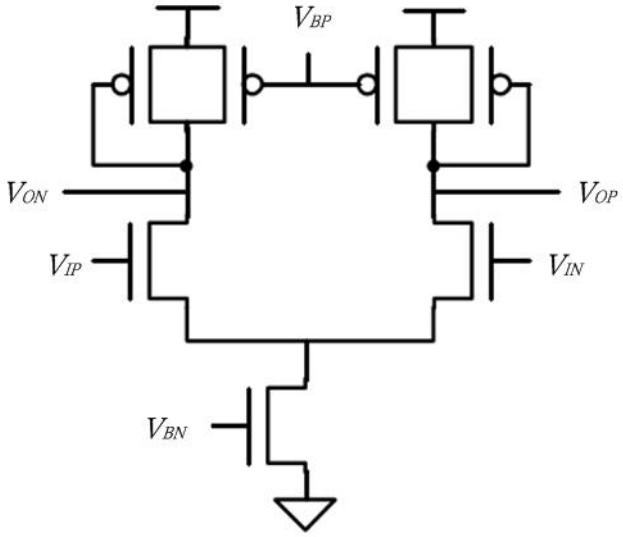


Figure 3.7 The delay cell of VCO

The bias generator of the VCO is shown in Figure 3.8. The bias generator provides correct voltage swing limitation of the delay buffer, and dynamically adjusts the bias voltage of the NMOS current source of the delay buffer so that this current is held constant and highly independent of supply voltage. It consists of a replica of half the delay buffer and a single-stage differential amplifier.

The differential amplifier is used as a unity gain buffer to force the voltage V_C of the half-buffer replica equal to V_{CTRL}, which produces the bias voltage V_{BN} of the NMOS current source and provide the correct lower swing limit of V_{CTRL} for the buffer stages. And the gate voltage of the NMOS current source has been dynamically adjusted by the differential amplifier, so it provides stable current and better immunity of the supply noise.

The bias circuit of the differential amplifier is a self-bias PMOS current mirror, which utilizes the bias voltage V_{BN} of the NMOS current source for producing the current of the self-bias current mirror. Because the bias voltage is not directly related with the supply, the self-bias current mirror is not sensitive to supply. The bias circuit, however, have two stable states, so it is necessarily to add a start-up circuit that prevent from the undesired condition. If the bias circuit has no current, the voltage V_X will be zero so that M_{X2} turns off, which forces a current through the bias circuit to start up the bias generator. Then, V_X will rise to turn on M_{X2} so that turn off M_{X1}, and the start-up circuit will not impact the bias generator at all.

The differential amplifier is used as a negative feedback, so the frequency response and the stability should be considered. The bandwidth of the bias generator is typically set equal to the operating frequency of the buffer stages so that the bias generator can track all supply and substrate voltage disturbances at frequencies that will affect the PLL designs. For the consideration of stability, the bias generator must be able to drive the delay buffer stages of the voltage controlled oscillator, and have enough phase margin and bandwidth. There is a dominant pole at V_X of the bias generator, which is inversely proportional to the number of the stages of the VCO. The bandwidth and the phase margin is in conflict, so the trade-off between the bandwidth and the phase margin should be considered. The driving capability of the bias

generator can be adjusted for optimization.

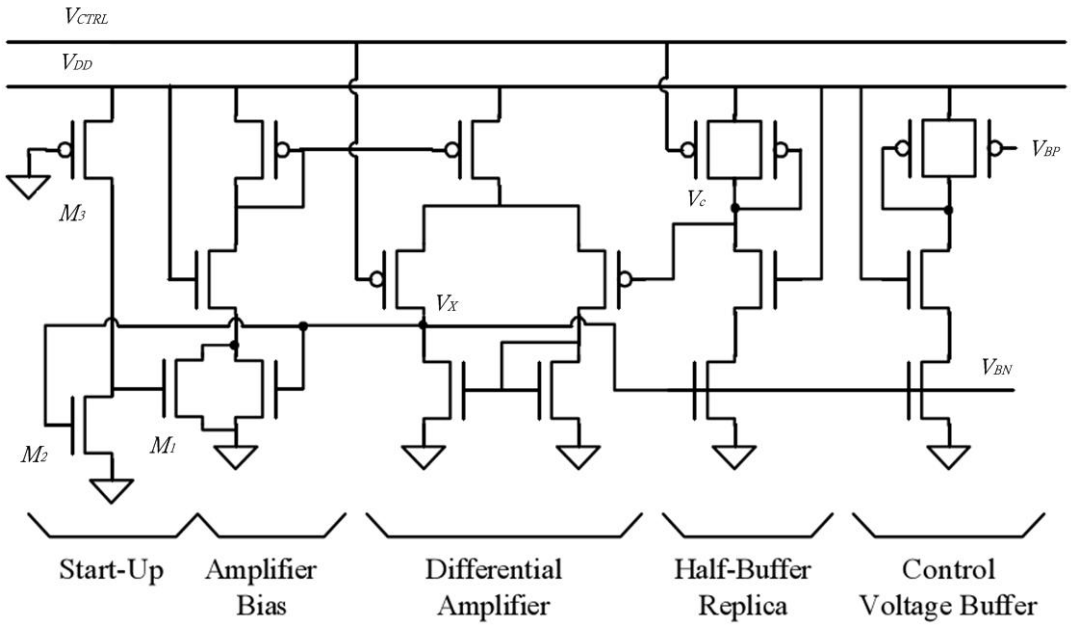


Figure 3.8 The bias generator of VCO

For the high immunity of the supply noise, the load of the differential delay cell should have a linear I-V curve, which makes the supply noise a common mode noise that can be rejected well by the differential delay cell. In practical, it is difficult to use MOS device as linear load, especially, in wide frequency range. Thus, the symmetric load is introduced here, though nonlinear, it can be used for achieving high supply noise rejection. Figure 3.8 shows the symmetric load I-V characteristics. Nonlinear load resistances normally convert common-mode noise into differential mode noise, which affects the buffer delays. With symmetric loads, however, due to the I-V curve is symmetry to the center of the output voltage swing, the first-order noise coupling terms cancel out, leaving only the higher order terms and substantially reducing the

jitter caused by common-mode noise from the supply.

The current of the PMOS biased by V_{CTRL} is $I_D = \frac{k_p}{2}(V_{CTRL} + V_{TP})^2$, so the bias current of the buffer biased by the bias generator is $2I_D$. It can be shown that the effective resistance of the symmetric load is directly proportional to the small signal resistance at the ends of the swing range which is just the reciprocal of transconductance g_m for one of the two equally sized devices when biased at V_{CTRL}.

The delay time of a delay cell is approximately defined as

$$t = R_{EFF} \cdot C_{EFF} = \frac{1}{gm} \cdot C_{EFF} \tag{3.1}$$

where C_{EFF} is the effective buffer output capacitance. Taking the derivative of the bias current with respect to V_{CTRL}, the transconductance is given by

$$gm = k_p(V_{CTRL} + V_{TP}) \tag{3.2}$$

The buffer delay is given by

$$t = \frac{C_{EFF}}{k_p(V_{CTRL} + V_{TP})} \tag{3.3}$$

Thus, the oscillator frequency is given by

$$f_{OSC} = \frac{1}{2nt} = \frac{k_p(V_{CTRL} + V_{TP})}{2nC_{EFF}} \tag{3.4}$$

where n is the number of the stages of the VCO. The gain of the VCO is given by

$$K_O = \frac{df_{OSC}}{dV_{CTRL}} = \frac{k_P}{2nC_{EFF}} \tag{3.5}$$

Thus the VCO has first-order tuning linearity.

3.3.3. Charge Pump

The charge pump is a circuit that supplies current to the loop filter to produce the control-voltage (V_C) of VCO. When the Up signal is high, the charge pump source current I_{up} into the loop filter that causes V_C to rise. When the Down signal is high, the charge pump sinks current I_{down} from the loop filter that causes V_C to decrease. To eliminate the dead zone as PLL is locked, there will be a short pulse, t_p, on the Up and Down signals. If I_{up} and I_{down} are the same, the phase error between the reference and the feedback signal will be zero. If I_{up} and I_{down} are not matched, the PLL will lock with a static phase error θ_{eo}. According to charge conservation, the source charge is equal to sink charge under locked condition. If $(I_{up} - I_{down}) = \Delta I > 0$, t_{up} will be equal to t_p and $(t_{up} - t_{down}) = \Delta t$ will be negative, where t_{up} is the pulse width of Up signal and t_{down} is the pulse width of Down signal. It is shown that $I_{up} \cdot t_p = I_{down} \cdot (t_p - \Delta t)$, so the static phase error can be derived as

$$\theta_{eo} = \left| \frac{\Delta t}{T_{ref}} \right| = \left| \frac{\Delta I \cdot t_p}{I_{down} \cdot T_{ref}} \right| \tag{3.6}$$

where T_{ref} is the period of the reference signal. On the other hand, if $(I_{up} - I_{down}) = \Delta I < 0$, t_{down} will be equal to t_p and $(t_{up} - t_{down}) = \Delta t$ will be positive.

The static phase error is

$$\theta_{eo} = \left| \frac{\Delta t}{T_{ref}} \right| = \left| \frac{\Delta I \cdot t_p}{I_{up} \cdot T_{ref}} \right| \tag{3.7}$$

Since the output frequency of VCO is proportional to V_C. There should be well isolation of V_C to supply noise. Otherwise, the output will be perturbed directly by the supply noise. The current source used here is a wide swing current mirror to suppress the impact of supply noise to V_C, it is shown in Figure 3.9. The output resistance of the current source is much larger than single MOS current source but it will reduce the headroom by $2V_{dsat}$.

The charge pump has charge-sharing problem. It is that when the Up or Down is high to source or sink current into loop filter, due to that the voltage of the parasitic capacitors on nodes N_1 and N_2 of charge pump is not the same as V_C, the charges of the parasitic capacitors will share instantaneously with the capacitor of loop filter. Then, V_C will show a large glitch that lead to a jitter in output of VCO. To reduce charge sharing, an operational amplifier connected as unity-gain buffer is adopted in the charge pump [13], shown in Figure 3.10. When nodes N_1 and N_2 are not switched to V_C, they are biased by the unity-gain buffer. This suppresses any charge sharing from the parasitic capacitance on N_1 or N_2 that can cause jitter in the locked state.

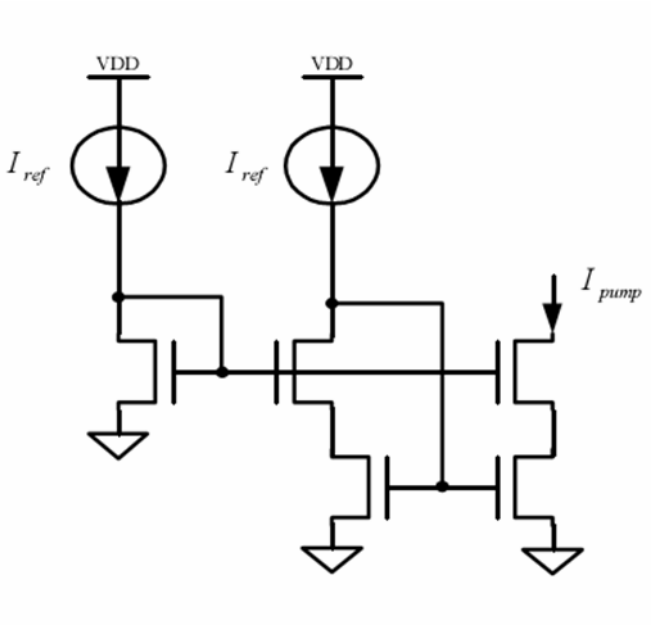


Figure 3.9 Wide swing current mirror

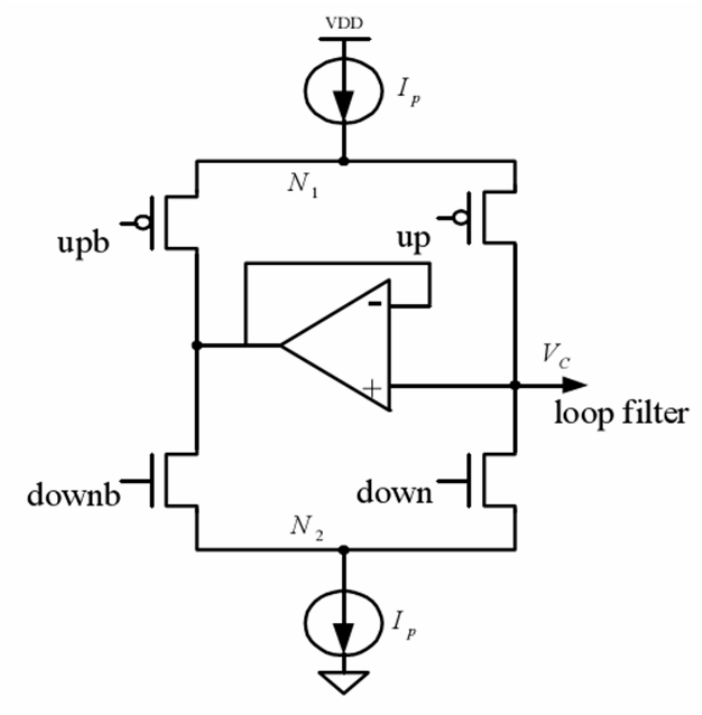


Figure 3.10 Charge pump with an unity-gain buffer

3.3.4. Loop Filter

The loop filter converts the charge pump current into the VCO control voltage V_C. The loop filter is simply a low-pass filter with two capacitors and one resistor, and it is depicted in Figure 3.11. If the loop filter only has C_1, the phase lock loop is a second order loop. (One pole is supported by VCO.) The phase lock loop is theoretically stable, however, due to parasitic pole, it may be unstable. For the consideration of stability, R_1 is included to put a zero in PLL that improves the phase margin.

If the loop filter is without C_2, there will be a ripple effect in the PLL. Upon

each cycle of the phase detector, the charge pump current is driven into the filter impedance, which responds with an instantaneous voltage jump of $\Delta V_c = I_p R_1$. At the end of the charging interval, the charge pump current switches off and a voltage jump of equal magnitude occurs in the opposite direction. The ripple will lead to frequency excursions for each pump pulse. To mitigate the ripple, the small C_2 is included for the ripple filter. Since C_2 is far smaller than C_1, the phase locked loop can be analyzed as a second order system. Figure 3.12 shows the frequency response of the PLL with this loop filter.

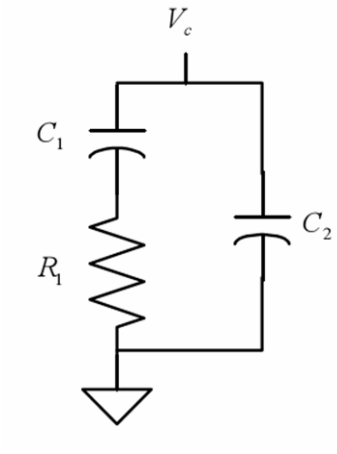


Figure 3.11 Loop filter

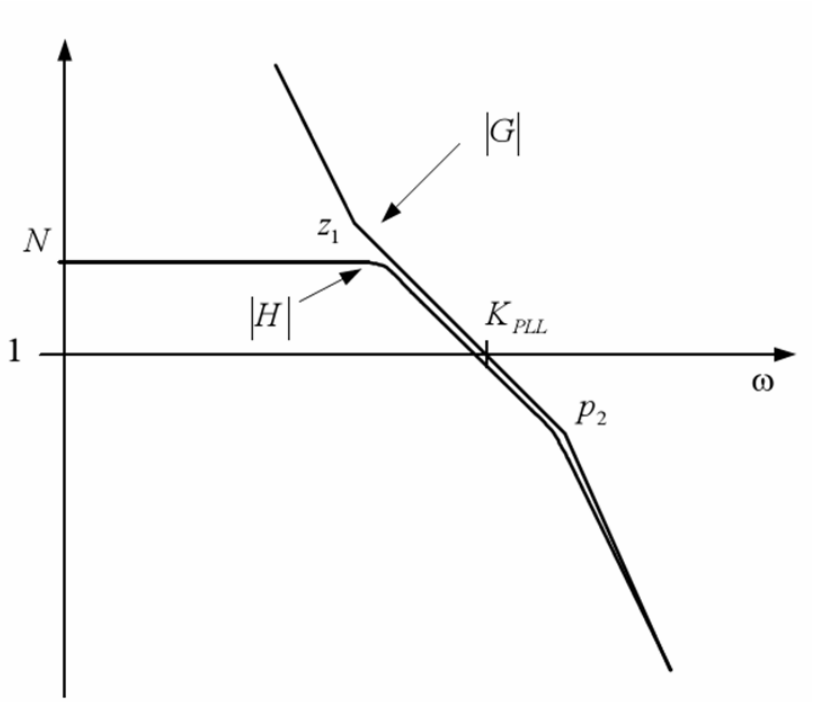


Figure 3.12 Frequency response of the PLL with loop filter in Figure 3.11

3.3.5. Programmable VCO

An illustration of the programmable VCO is shown in Figure 3.13. The programmable VCO consists of V-I converter and ring oscillator. The ring oscillator consists of seven delay cells, DLY1 to DLY7. In addition to the original V-I converter consists of MCN, MCP and RC, there is a 5-bit decoder used to switch the extra current path for the ring oscillator. Since the drain current of a MOSFET is related to the square of gate to source voltage (V_{GS}) of the MOSFET. In order to have a linear VCO gain, the nonlinear relationship between V_C and drain current of MOSFET MCN should be

solved. A source degeneration resistor RC is used between the source side of MCN and ground [5]. Furthermore, the width of MCN is made wider than others to mitigate the square relationship between drain current and gate-source voltage. The oscillation frequency can be derived as

$$F_{VCO} = \frac{Ic}{N \cdot Ctot \cdot V_{DD}} \qquad (3.8)$$

Where the oscillation frequency is proportional to the injected current generated from V-I converter (Ic) and inversely proportional to the number of delay cell (N), loading of each delay cell (Ctot) and voltage level of power source (V_{DD}). It can be seen that the VCO output frequency could be manipulated by changing these factors. The method used in this design is to manipulate the charging current Ic with extra current source I_1, I_2. The oscillation frequency is then modified as

$$F_{VCO} = \frac{(Ic + Ix)}{N \cdot Ctot \cdot V_{DD}} \qquad (3.9)$$

where Ix could be I_1 or I_2, which is independent of V_C. The PLL[4:0] decoder determines which extra current source, I_1 or I_2, to be injected into the delay cells. The value of Ic depends on the operation range of V_C. Based on the process and simulation result, V_C will approximately be limited in the range of 0.5V ~ 1.3V to make MCN operate in the saturation region. If the path of I_1 or I_2 is connected, the oscillation frequency F_{VCO} could be increased without changing the other factors. Based on the

above equation, Ix could be derived if a different F_{VCO} is required without changing the factor, Ic. The design method is based on the above equation to derive a required current (Ic + Ix) approximately. Then, fine tuning by simulation with a lower value of Ic and adding a constant current source I_1 or I_2 to have a matched F_{VCO}. The corresponding value of V_C to Ic should be designed within the range of 0.5V ~ 1.3V. The value of I_1, I_2 is designed as 2uA and 4uA, respectively. The VCO gain is designed to be 4.25×10^8 radians/V/second. In this method, the upper value of V_C could be reduced to a lower value. If a higher value of Ix is used, a higher value of F_{VCO} will be obtained without increasing V_C as it is illustrated in Figure 3.2. Although the specification of frequency in this design is only upper to 81.882 MHz. The output frequency could run up to around 150MHz but the PLL still locked according to the simulation testing. If a higher output frequency is required, the number of delay cells or size of each delay cells has to be modified.

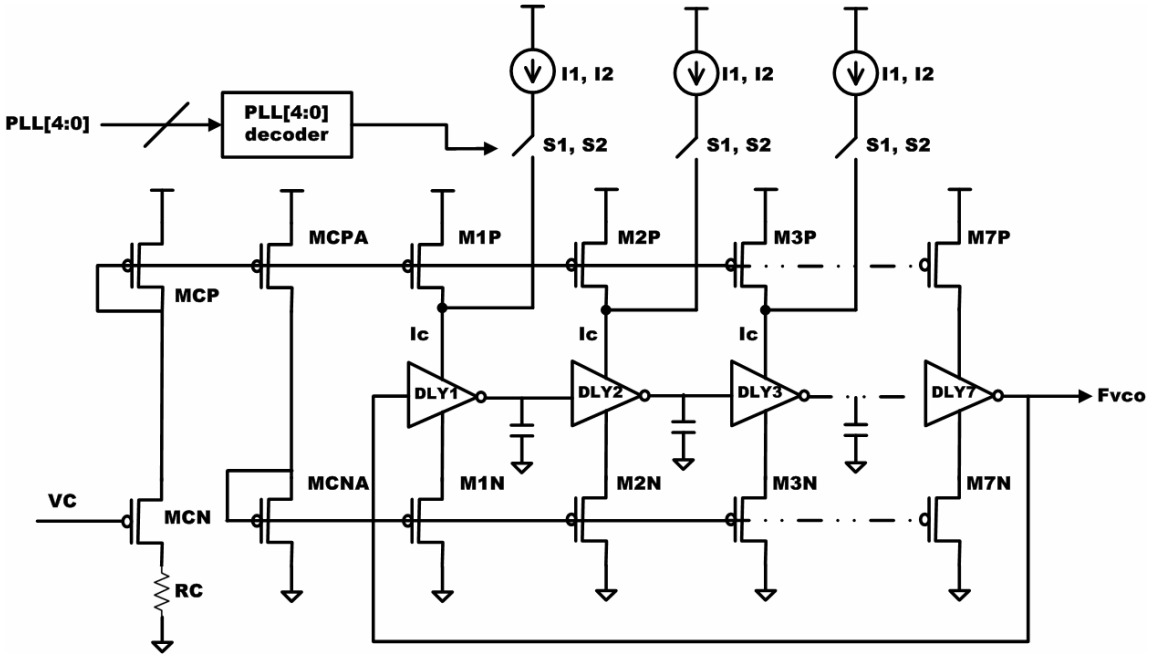


Figure 3.13 The programmable VCO

Chapter 4. Simulation Results

The frequency synthesizer is implemented by HJ 1P6M 0.18μm CMOS process. According to the close-loop transfer function, damping factor and bandwidth of the PLL will vary with the N value of feedback divider. An auxiliary current path is used to compensate for this variation. In order to check if the PLL lock in a stable state, the transient responses of the minimum, median and maximum output frequency condition are simulated and shown in the following paragraphs.

4.1. Output frequency: 31.059MHz; feedback divider factor: 22

The minimum output frequency is 31.059MHz with feedback divider factor of 22. A 24MHz crystal oscillator is used as the clock source to generate reference input frequency of the PLL. The 24MHz clock is further divided down by 17 before receiving by the phase frequency detector to synthesize the desired output frequency. The frequency of input reference clock is 1.411765MHz (24MHz/17), which is shown in the upper graph of Figure 4.1 as the name REFCLKIN. The VCO feedback clock waveform is also shown in the lower graph of Figure 4.1 as the name FFB for comparison. The UP and DW signal in Figure 4.2 is provided to illustrate the corresponding output response of PFD to the phase difference between REFCLKIN

and FFB.

The transient response of VCO control voltage is shown in Figure 4.3 as the name VCOCTL. When the VCO control voltage settles down and converges to a steady-state value, the PLL is indicated to be locked. The lock time is about 50μs as can be seen in Figure 4.3. The ripple of VCO control voltage in locked state is less than 4mV, which is shown in Figure 4.3 as well. The output clock waveform in steady state is shown in Figure 4.4.

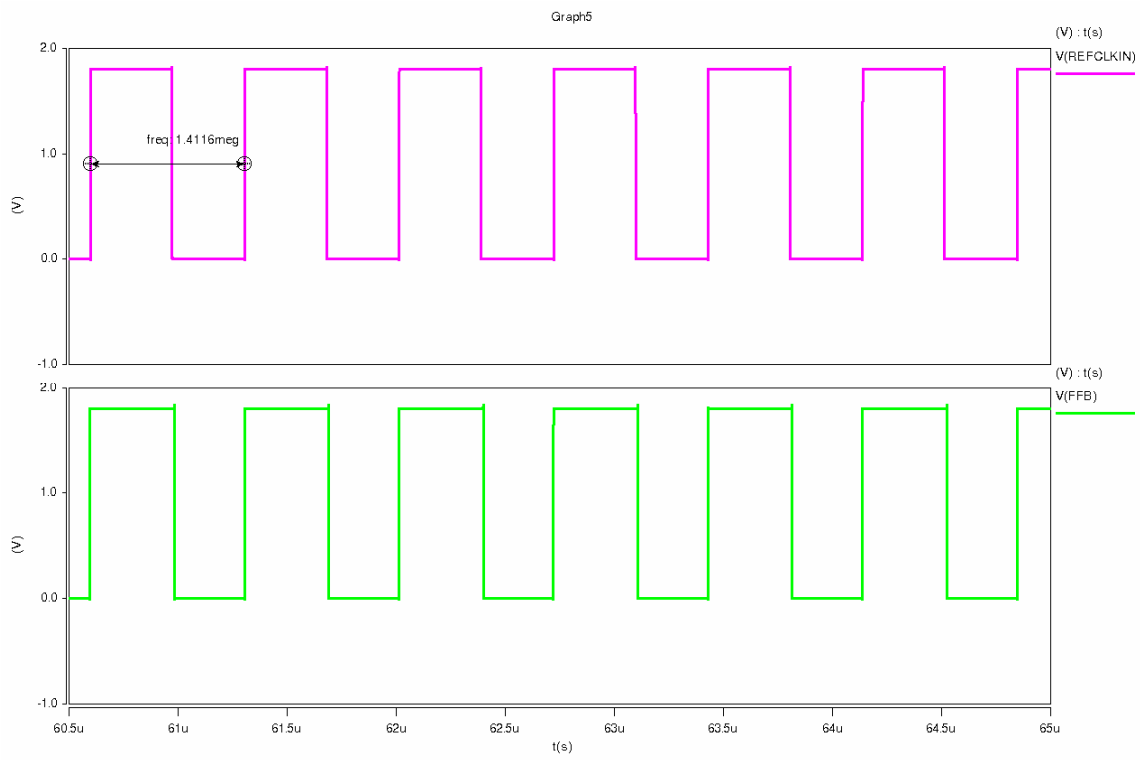
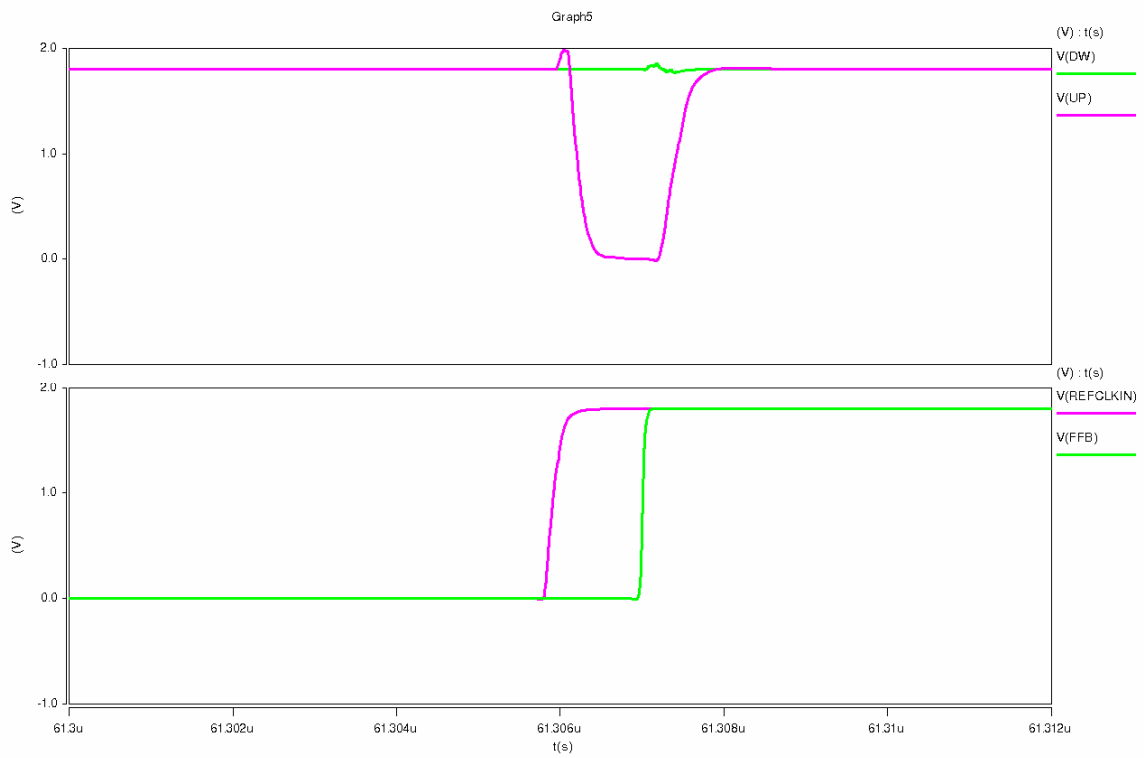


Figure 4.1 Input reference clock waveform and VCO feedback clock waveform


Graph5
(V) : t(s)
V(DW)
V(UP)
2.0
1.0
0.0
-1.0
(V)
(V) : t(s)
V(REFCLKIN)
V(FFB)
2.0
1.0
0.0
-1.0
(V)
61.3u
61.302u
61.304u
61.306u
61.308u
61.31u
61.312u
t(s)

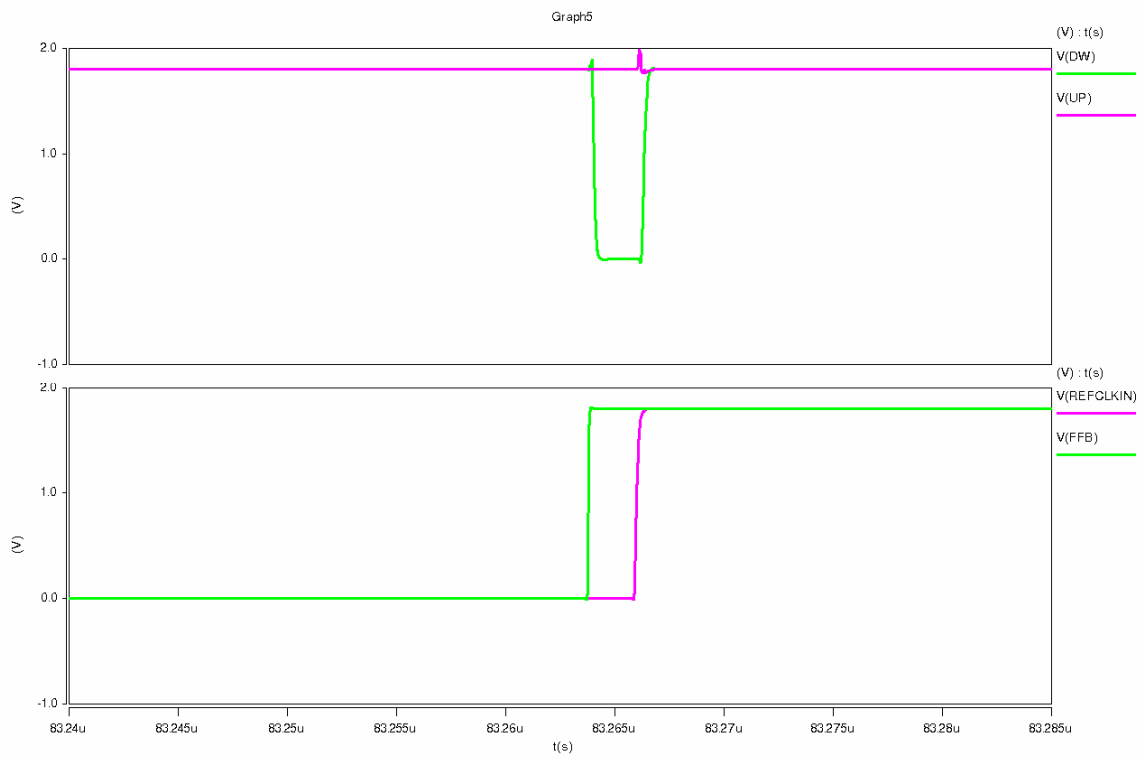


Figure 4.2 Up and down signals of PFD

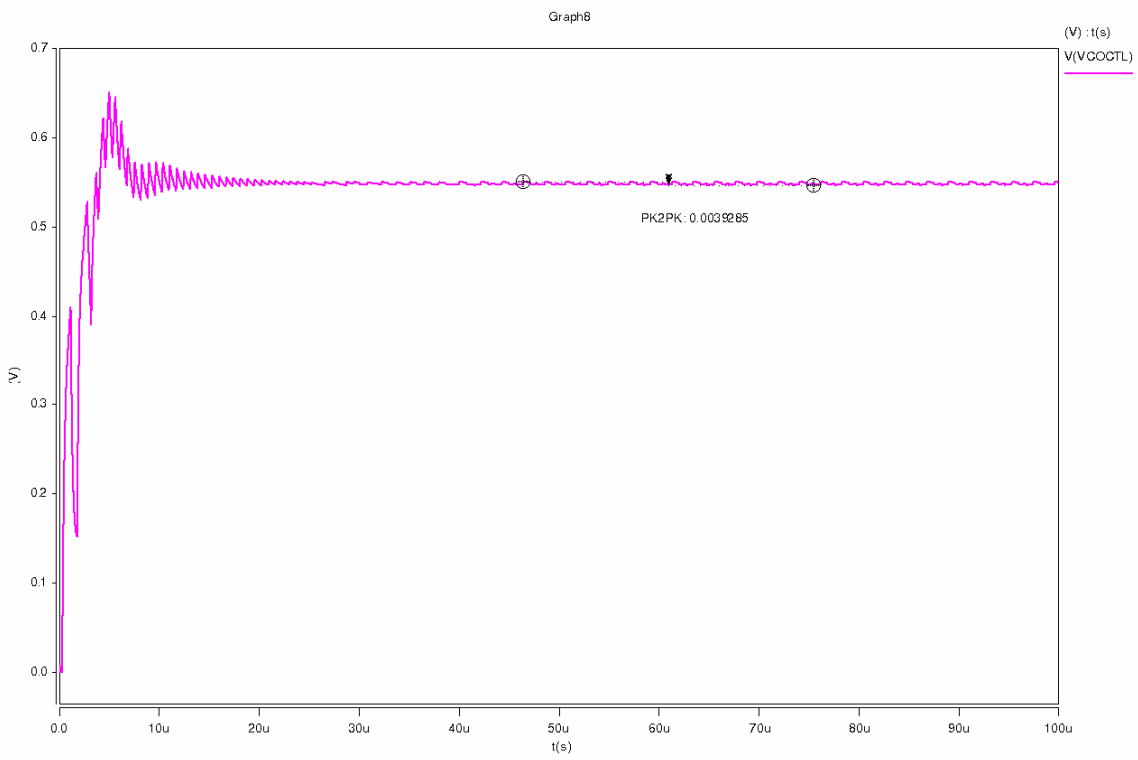


Figure 4.3 Control voltage of VCO

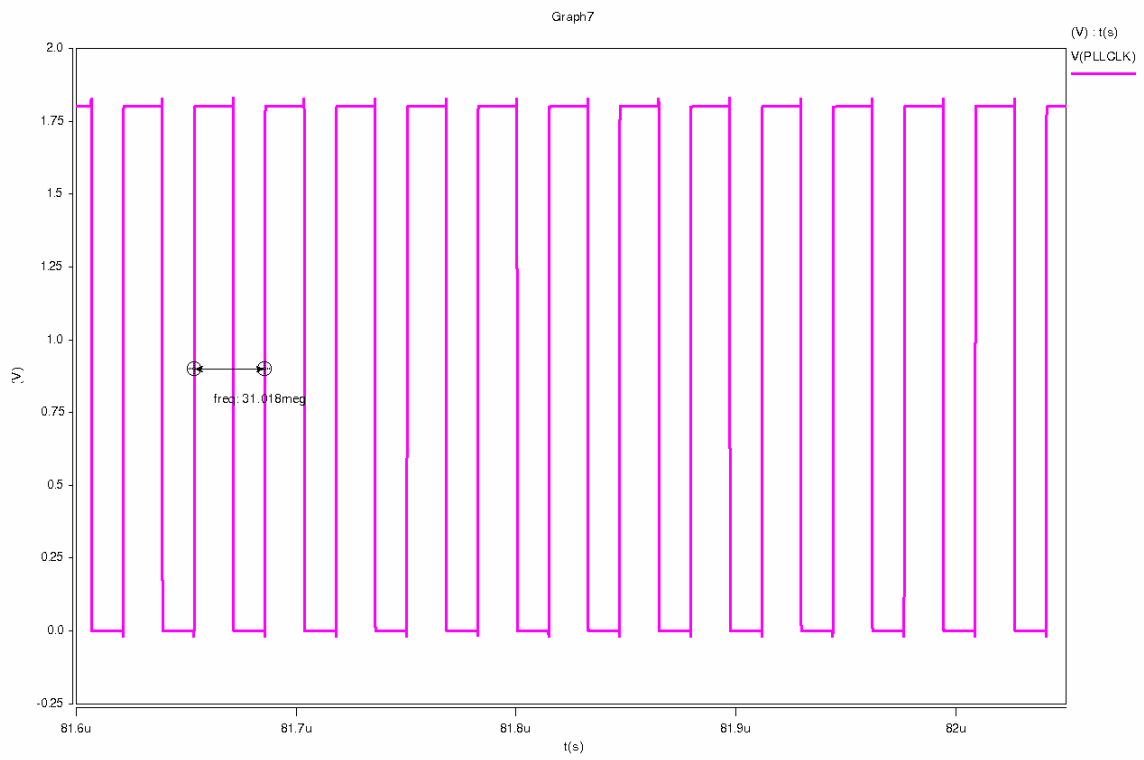


Figure 4.4 31.059MHz clock output of the PLL

4.2. Output frequency: 62.118MHz; feedback divider factor: 44

The median output frequency is 62.118MHz with feedback divider factor of 44. The frequency of input reference clock is 1.411765MHz (24MHz/17), which is shown in Figure 4.5 as the name REFCLKIN. The feedback clock waveform is also shown in Figure 4.5 as the name FFB for comparison. The UP and DW signal in Figure 4.6 is provided to illustrate the corresponding output response of PFD to the phase difference between REFCLKIN and FFB.

The transient response of VCO control voltage is shown in Figure 4.7 as the name

VCOCTL. When the VCO control voltage settles down and converges to a steady-state value, the PLL is indicated to be locked. The lock time is about 70μs as can be seen in Figure 4.7. The ripple of VCO control voltage in locked state is less than 4mV, which is shown in Figure 4.7 as well. The output clock waveform in steady state is shown in Figure 4.8.

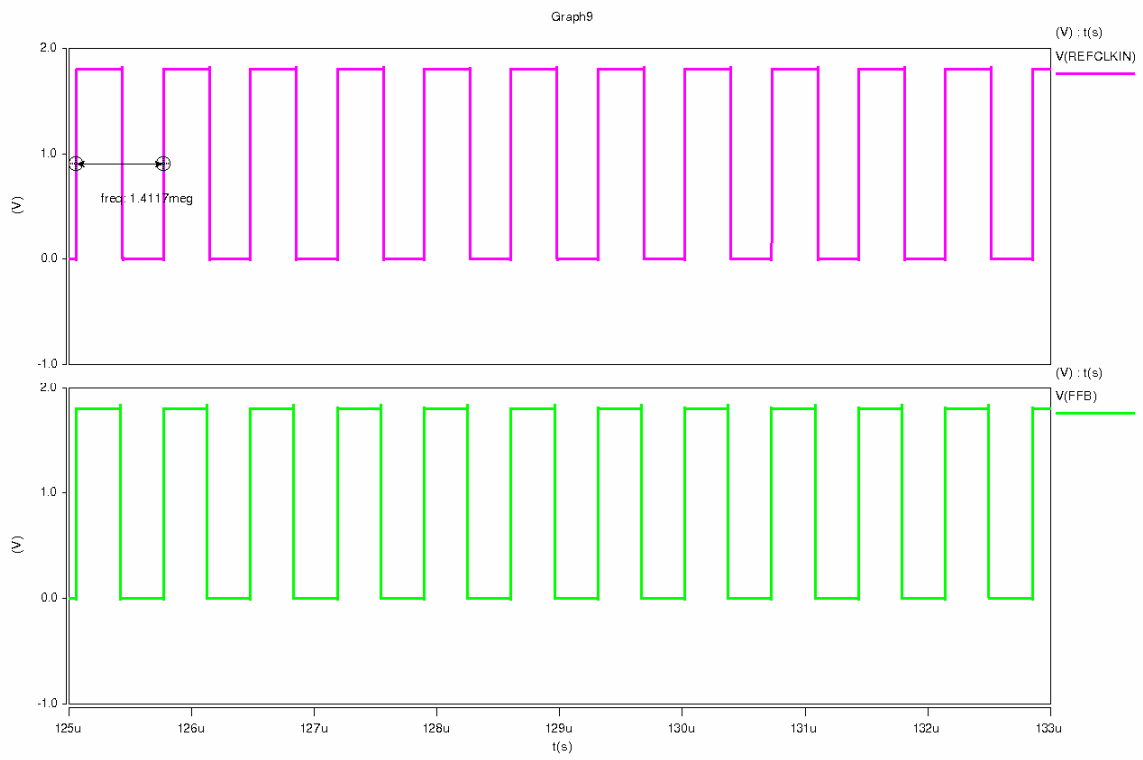
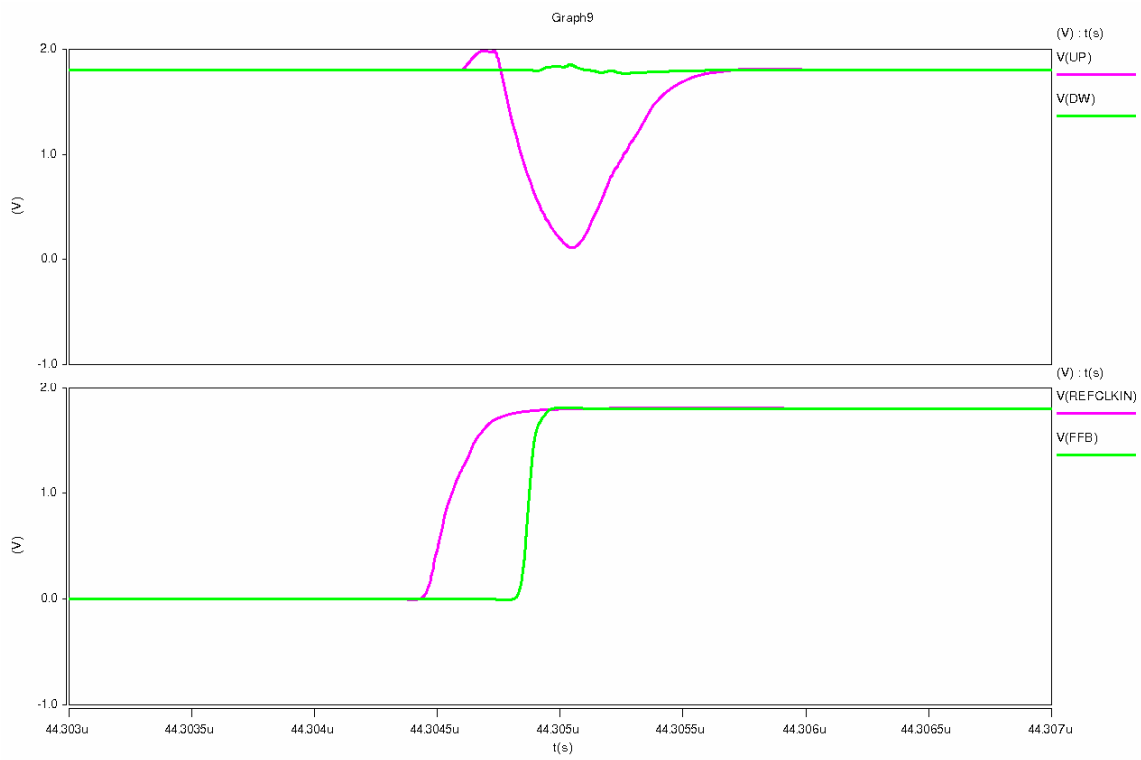


Figure 4.5 Input reference clock waveform and VCO feedback clock waveform


Graph9
(V) : t(s)
V(UP)
V(DW)
2.0
1.0
0.0
-1.0
(V)
(V) : t(s)
V(REFCLKIN)
V(FFB)
2.0
1.0
0.0
-1.0
(V)
44.303u
44.3035u
44.304u
44.3045u
44.305u
44.3055u
44.306u
44.3065u
44.307u
t(s)

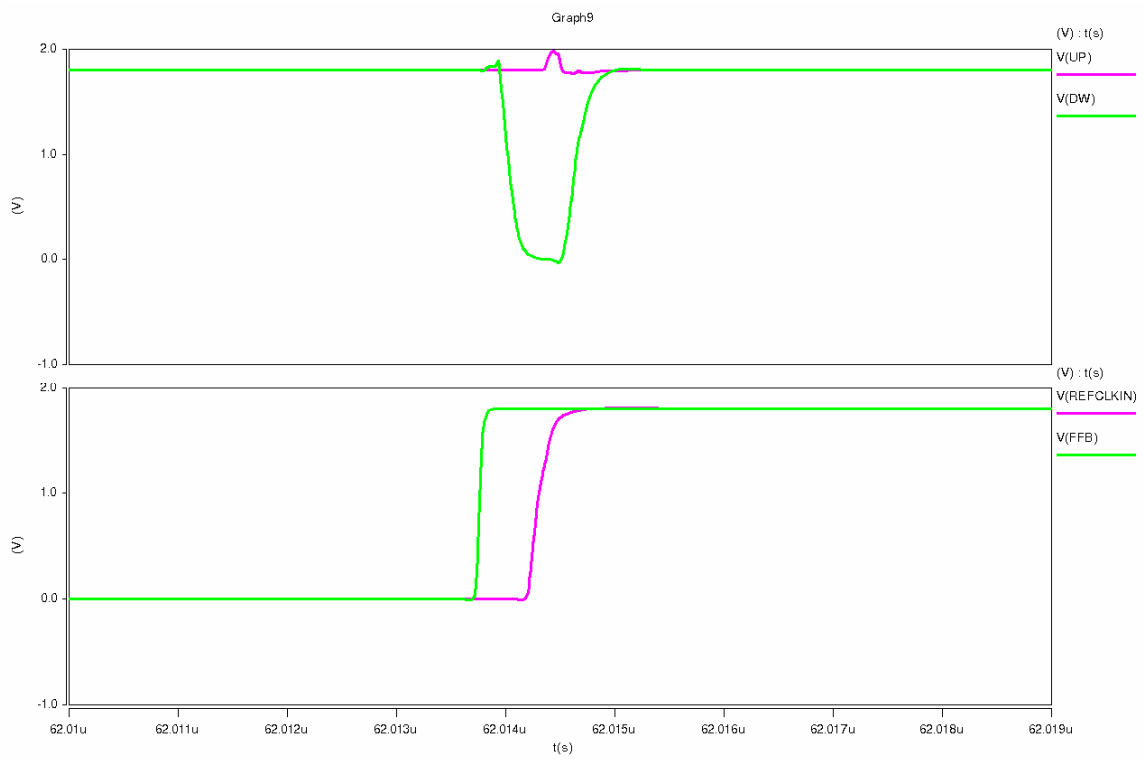


Figure 4.6 Up and down signals of PFD

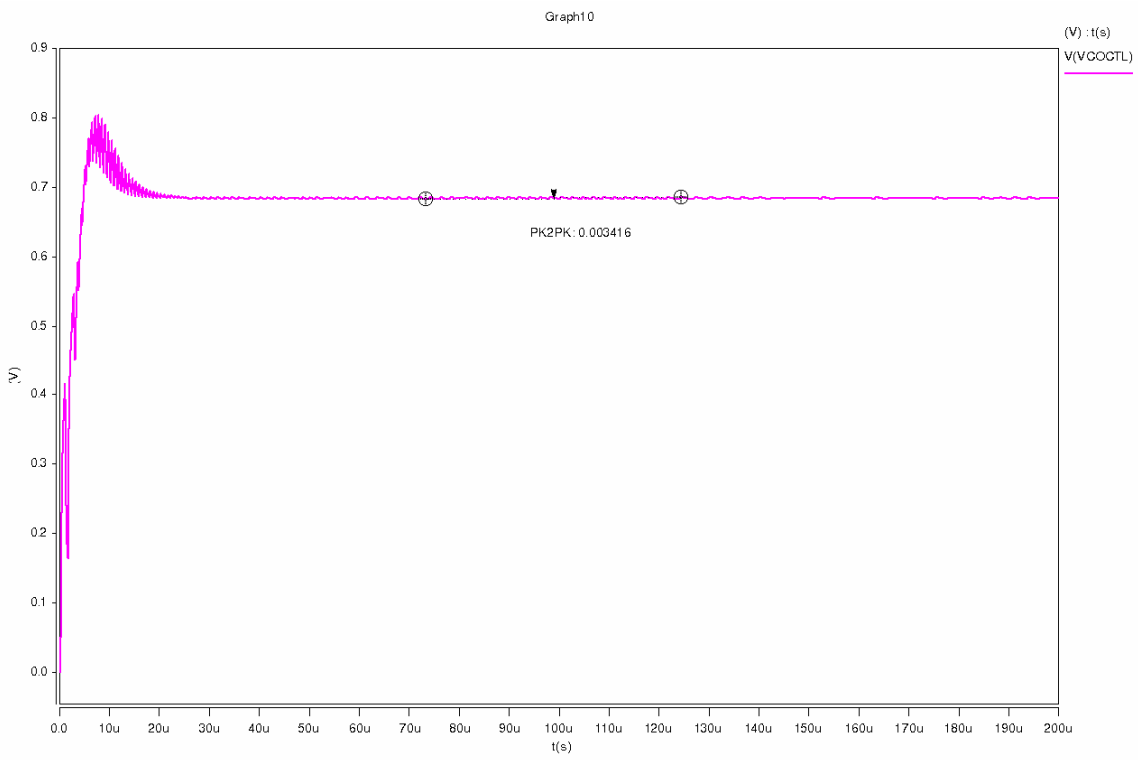


Figure 4.7 Control voltage of VCO

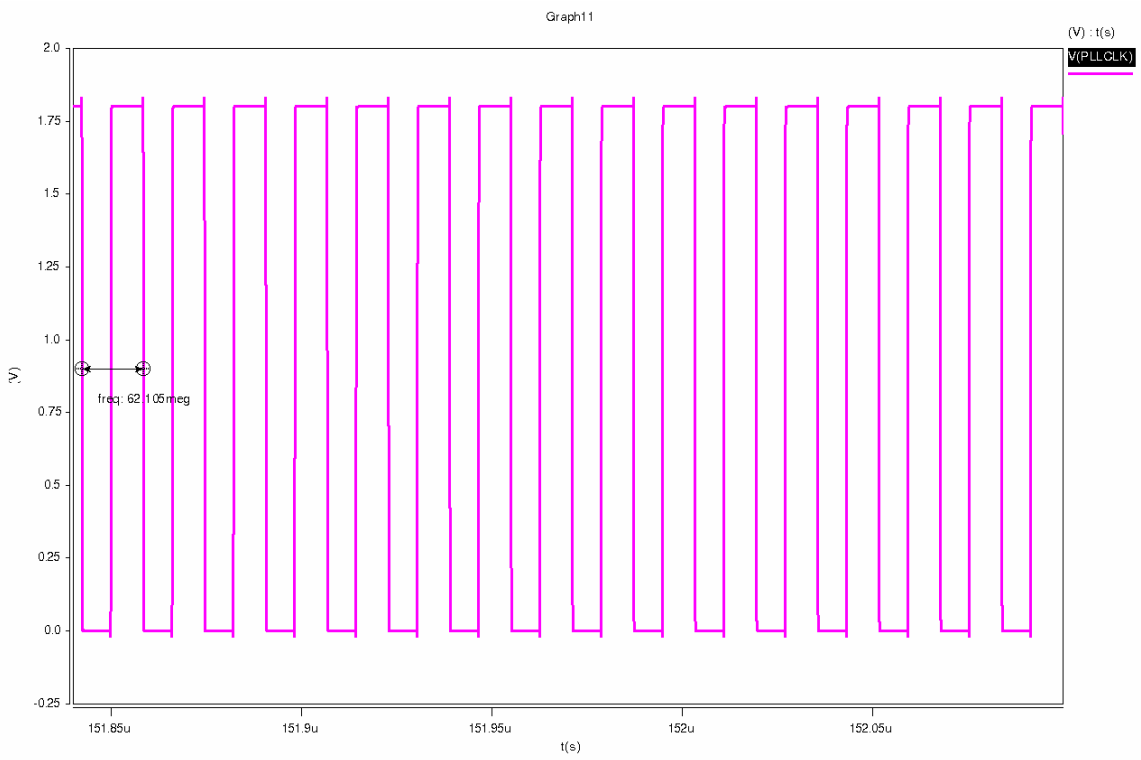


Figure 4.8 62.118MHz clock output of the PLL

4.3. Output frequency: 81.882MHz; feedback divider factor: 58

The maximum output frequency is 81.882MHz with feedback divider factor of 58. The frequency of input reference clock is 1.411765MHz (24MHz/17), which is shown in Figure 4.9 as the name REFCLKIN. The feedback clock waveform is also shown in Figure 4.9 as the name FFB for comparison. The UP and DW signal in Figure 4.10 is provided to illustrate the corresponding output response of PFD to the phase difference between REFCLKIN and FFB.

The transient response of VCO control voltage is shown in Figure 4.11. When the

VCO control voltage settles down and converges to a steady-state value, the PLL is indicated to be locked. The lock time is about 70μs as can be seen in Figure 4.11. The ripple of VCO control voltage in locked state is less than 3mV, which is shown in Figure 4.11 as well. The output clock waveform in steady state is shown in Figure 4.12.

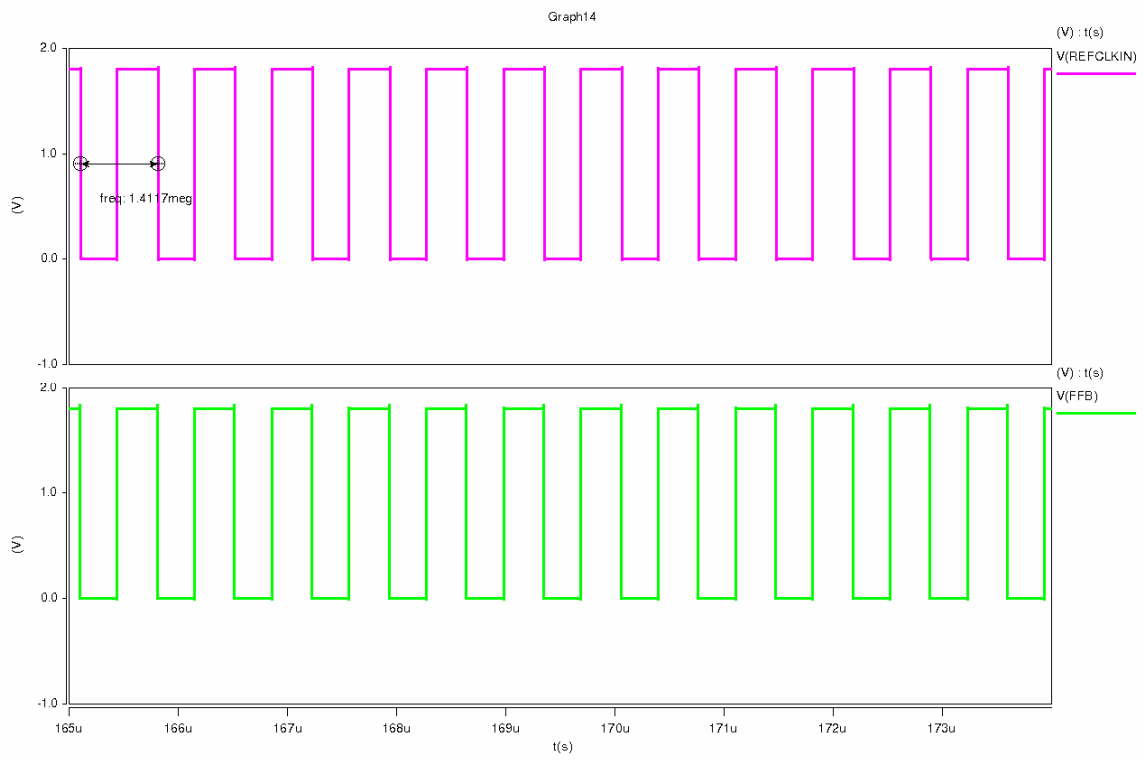
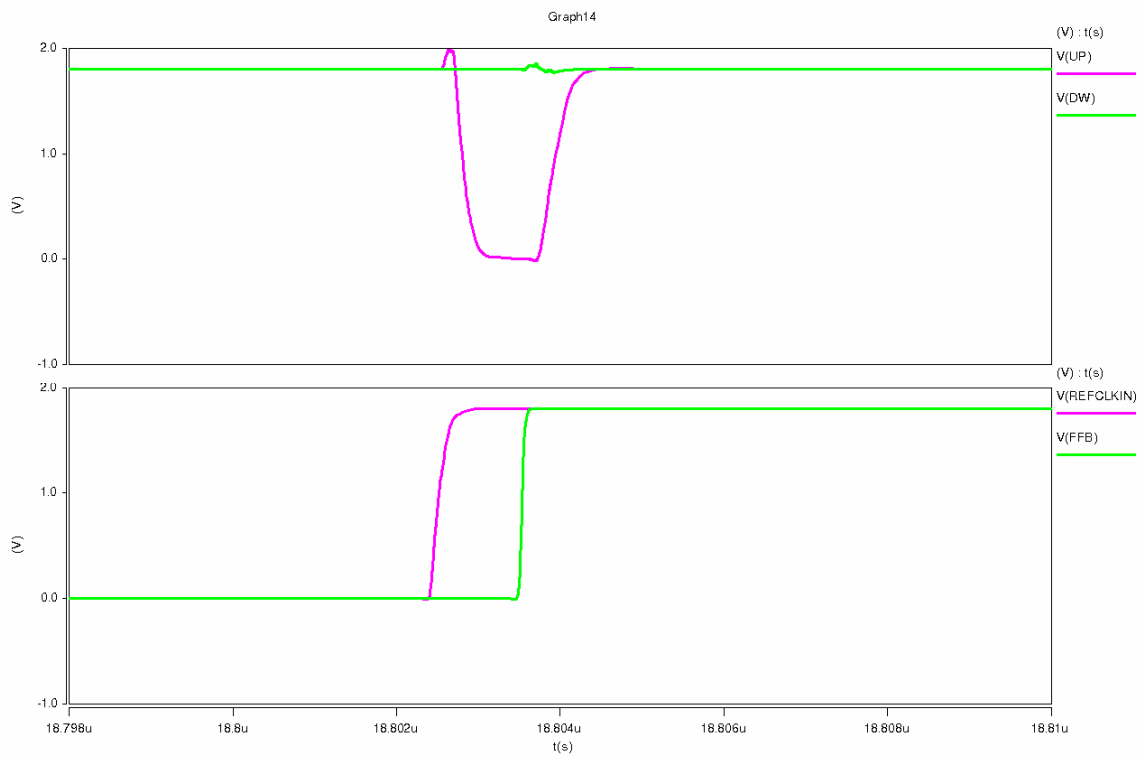


Figure 4.9 Input reference clock waveform and VCO feedback clock waveform


Graph14
(V) : t(s)
V(UP)
V(DW)
2.0
1.0
0.0
-1.0
(V)
(V) : t(s)
V(REFCLKIN)
V(FFB)
2.0
1.0
0.0
-1.0
(V)
18.798u
18.8u
18.802u
18.804u
18.806u
18.808u
18.81u
t(s)

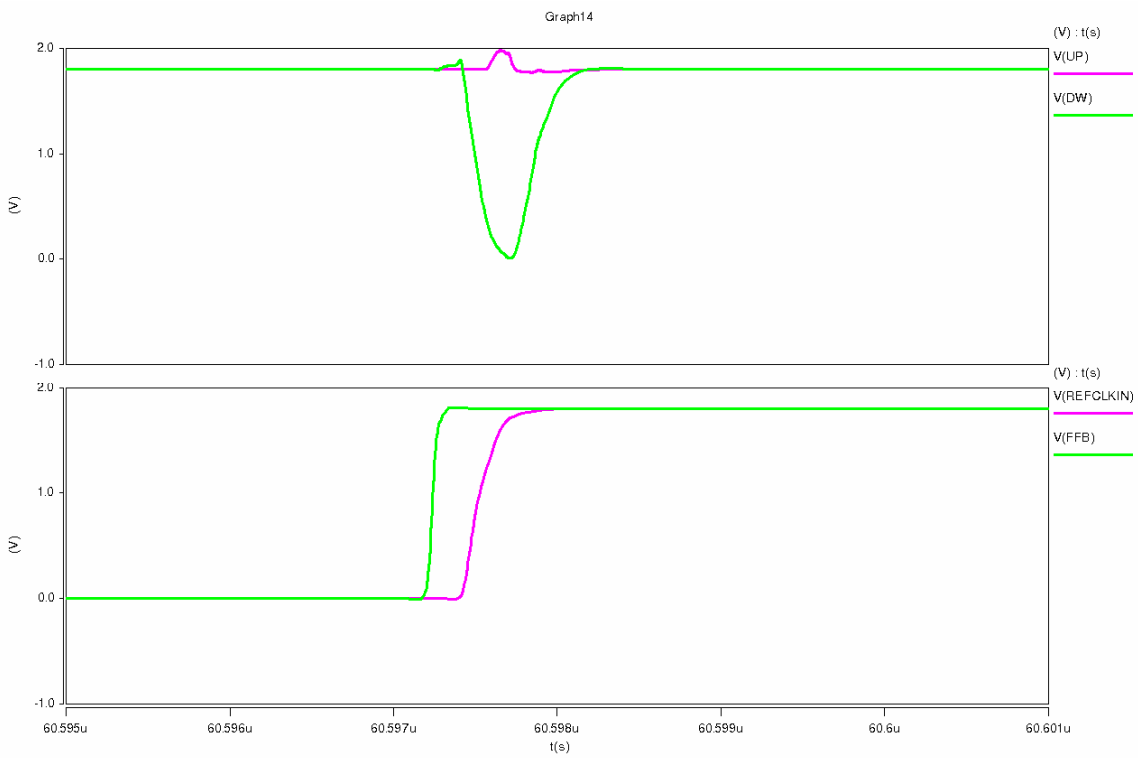


Figure 4.10 Up and down signals of PFD

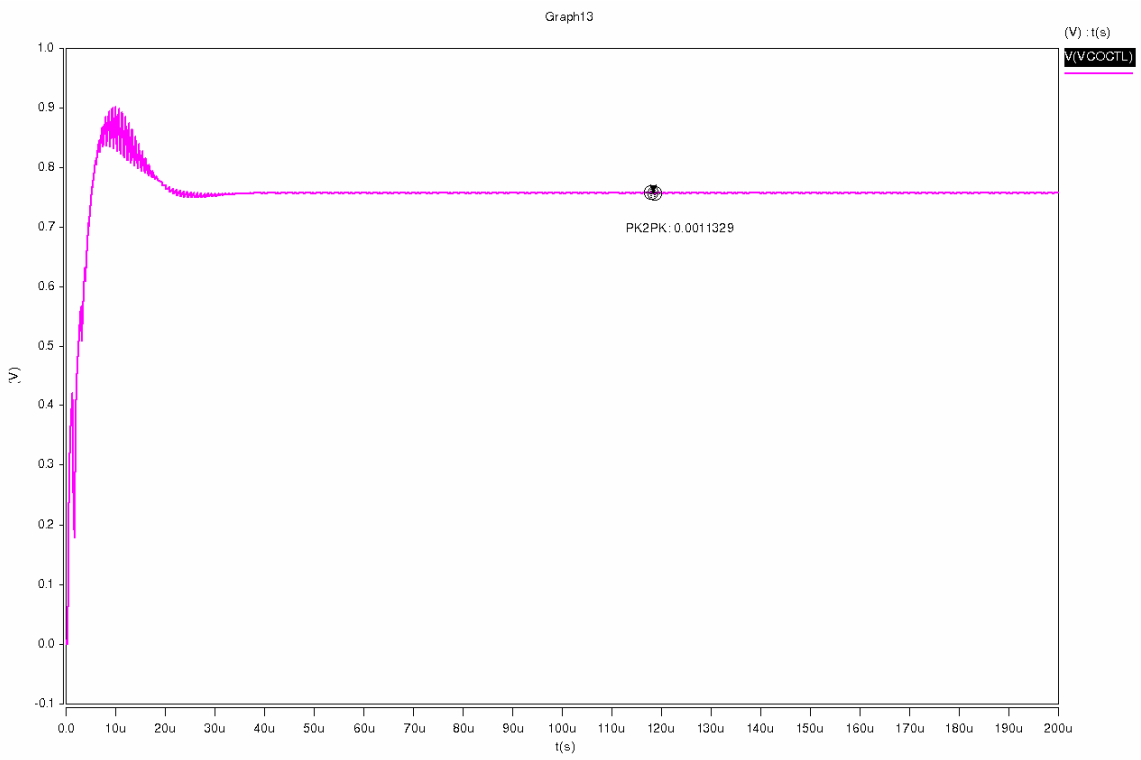


Figure 4.11 Control voltage of VCO

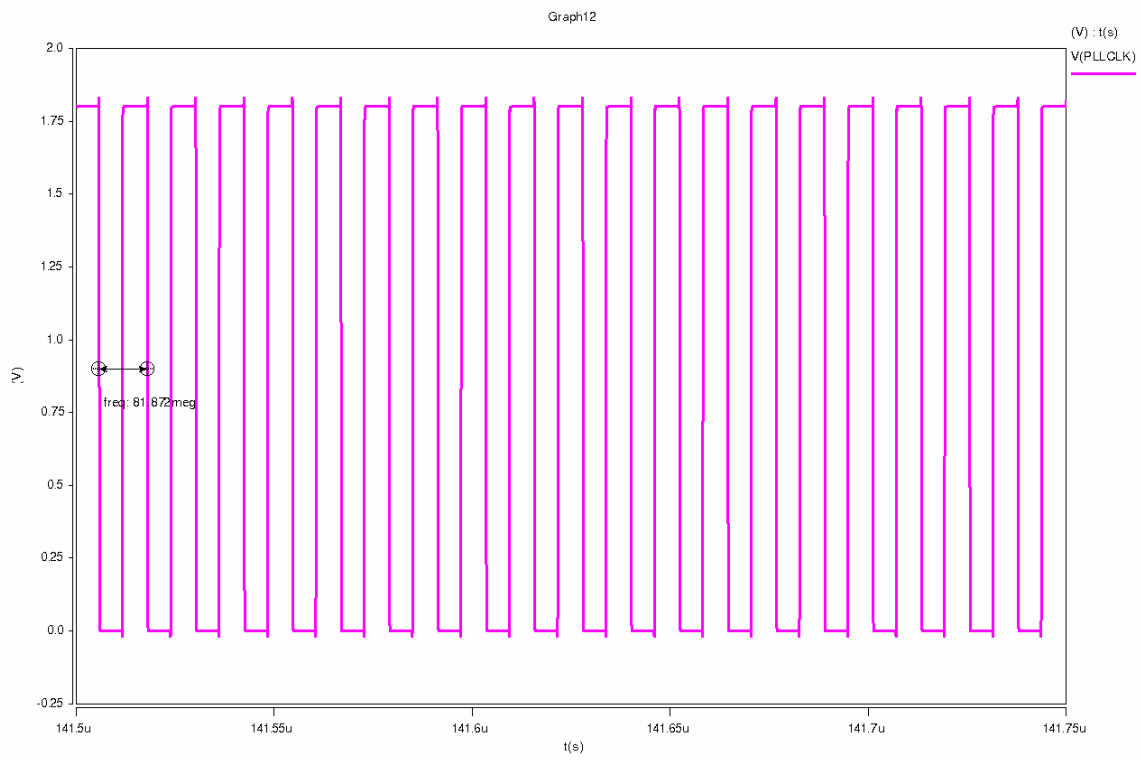


Figure 4.12 81.882MHz clock output of the PLL

4.4. Performance Comparison of the PLL with prior design

Performance comparison of the PLL with prior design is summarized in Table 3.1. In order to extend the operating frequency range, the loop parameters should be changed to meet the stability requirement and transient performance. As it is listed in Table 3.1, there are different design methods to manipulate the loop parameters. The method of variable loop filter, variable delay cell and programmable VCO will consume more die area. The method of variable charge pump is similar to ours, but the VCO gain will changed with the changing pump current. In our method, the VCO gain is not

changed but the operation frequency range is shifted by a constant current source. The power consumption of our design is 1.1mW (570μA with 1.8V power supply). The chip area is 0.26×0.46mm^2 in 0.18μm CMOS with on chip loop filter, bandgap reference and programmable logic control circuits.

As it is discussed in section 3.2. , the operating frequency range will be extended by using a set of constant current source. Since the value of constant current source used in this design is only 2~4μA, the current consumption is controllable and limited. Because the number of delay cells in ring oscillator is not changed with operating frequency and the layout of constant current source is not critical, the routing of VCO module will be more compact.

	Yiwu Tang ASIC/SOC	Ilya I. Novof JSSC	Ian A. Young JSSC
Process	0.5μm@3.3V	0.5μm@3.3V	0.8μm@6.0V
Frequency range	400-485MHz	15-240MHz	5-110MHz
Design method	Variable loop filter	Variable charge pump	Variable delay cell
Area	0.5mm^2	0.82 mm^2	0.31 mm^2
Power	26mW	33mW	16mW

	Jae Shin Lee consumer electronics	Oscal T.-C. Chen etc. JSSC	This work
Process	0.25μm@2.5V	0.18μm@1.8V	0.18μm@1.8V

Frequency range	60-375MHz	103M-1.02GHz	30-80MHz
Design method	Modified V-I converter	Programmable VCO	Additional constant current source
Area	1.98mm^2	0.16 mm^2	0.12 mm^2
Power	53mW	1.31~4.59mW	1.1mW

Table 4.1 Performance comparison of the PLL with prior design

Chapter 5. Measurement Results

The measurement results of jitter and power consumption under V_{DD}=1.8V is listed as follows. The maximum current consumption is around 570uA, which is suitable for battery powered hand-held MP3 players. After the final verification on the MP3 platform, the influence of jitter on every frequency is within tolerance of the DSP.

PLL[4:0]	PLLCLK	Jitter (ps)	Current (uA)
0	31.059	161	414.4
1	33.882	166	421.6
2	36.706	122	428.3
3	39.529	140	435.2
4	42.353	142	442.8
5	45.176	130	451.1
6	48.000	100	457.6
7	50.824	104	464.3
8	53.647	75	471.5
9	56.471	65	480.0
10	59.294	78	511.0
11	62.118	77	507.0
12	64.941	85	515.6
13	67.765	76	525.2
14	70.588	105	534.6
15	73.412	66	540.2
16	76.235	94	549.6
17	79.059	99	559.5
18	81.882	84	566.0

Table 5.1 Measurement results

Chapter 6. Conclusions and Future Work

6.1. Conclusions

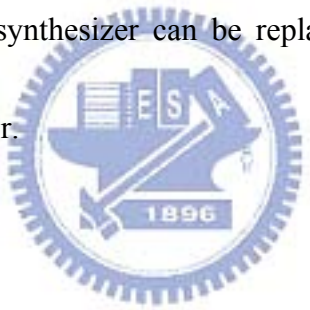
A PLL frequency synthesizer with wide operating frequency range is provided in this thesis. The damping factor and bandwidth of PLL will vary with the VCO gain, pump current, loop filter parameters, and feedback ratio. Since VCO gain is decided and fixed when the circuit structure is chosen, the N value of programmable divider in the feedback path will influence the damping factor and bandwidth of the PLL. To compensate damping factor and bandwidth of the PLL to a stable value, an auxiliary current path is used to implement the requirement. The damping factor is designed within 0.8 ~ 1.5, which is in a reasonable range.

Since there is a limitation to maintain gain linearity and obtain wide operating frequency range of VCO. The limitation will be more obvious especially for the low voltage process. This technique provides a solution for relaxing this issue without using a plurality of ring oscillators. Since the layout of current mirror circuit can be more compact than ring oscillator, it provides a method to have a compact layout as well.

6.2. Future Work

Although we have provides an alternative solution for PLL with wide operating

frequency range. The design parameters such as damping factor, loop bandwidth, and jitter are not optimized. The damping factor, for example, could be further optimized by changing the current of charge pump. There is trade-off between these parameters, and there are other circuit architectures can be used for optimizing the performance. For high-speed systems, jitter tolerant (or phase noise) will be a critical issue to deal with. The phase noise in the PLL-based frequency synthesizer can be reduced by using a fractional-N-divider in the feedback path. The fractional-N-divider allows the use of higher reference frequency and thereby reducing the phase noise. The integer divider in our PLL-based frequency synthesizer can be replaced by a fractional divider to suppress the phase noise further.



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