國立交通大學

電子工程學系 電子研究所

博士論文

具獨立雙閘極之多晶矽奈米線薄膜電晶體的研製與分析

Fabrication and Analysis of Independent Double-Gated Poly-Si Nanowire Thin-Film Transistors

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中華民國一○○年十月

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具獨立雙閘極之多晶矽奈米線薄膜電晶體的研製與分析

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摘要

本篇論文提出一簡易且低成本之製作多晶矽奈米線元件的方法。此法的特點在於利用將電感耦合電漿式(inductively coupled plasma)蝕刻機台中的偏壓電源(bias power)關閉並搭配使用六氟化硫(SF_6)的氣體以得到一具等向性與高蝕刻選擇比的蝕刻條件。將此參數用以側向蝕刻臨場摻雜多晶矽後便可形成寬度在10奈米~100奈米之向內凹陷的空隙，進而定義出奈米線的線寬。另外，當奈米線形成後，如果再沉積上第二層的介電層與閘極材料，此元件就具有獨立雙閘極的結構，可使元件的操作彈性大幅提升。

首先藉由控制側向蝕刻的時間，我們製備了具有不同寬度的奈米線元件，用以探討奈米線尺寸對元件電性的影響。與兩種單閘操作模式相比，實驗發現當奈米線越窄，在雙閘操作模式下電性改善的程度會有顯著的增加。經由量測分析，可得知這是由於奈米線尺寸會影響多晶矽的晶界能障受閘極調控的程度所導致。然而為了避免通道受到摻雜，原本所設計之元件製程卻會造成源/汲極的串聯電阻過大。因此，我們提出一種改良的流程，將臨場摻雜多晶矽取代離子佈值做為形

成源/汲極區的製備方法。採用此技巧所完成的元件除了具有明顯改善的導通電流與漏電流之外，更能夠達到只有 73 mV/dec 的次臨界擺幅(subthreshold swing)，這是目前文獻上多晶矽元件最佳的成果。

除了最佳化製程以改善元件特性外，為了探討奈米線載子傳輸特性，本研究也在製程中引入電子束微影技術，進而將通道長度微縮至 100 奈米以下，同時搭配低溫量測設備來完整分析元件導通機制。研究發現，當測量溫度低於約 100 K 時，有一單閘模式下的轉換曲線會展現出低於傳統金氧半場效電晶體(MOSFET)極限的次臨界擺幅，而且此現象只發生在通道長度小於 100 奈米的元件。經由模擬及實驗證實，這個效應是來自於閘極經過離子佈值後，雜質分佈不均而導致閘極對通道的控制能力會隨通道位置改變而變化，因此沿通道方向的能帶圖會形成一類似駝峰的曲線所致。

有鑑於近來三維記憶體技術多使用多晶矽做為主動層，本研究也討論獨立雙閘多晶矽奈米線結構應用於矽-氧化矽-氮化矽-氧化矽-矽(SONOS)非揮發記憶體時所衍伸的價值與各種操作上的可行性。首先，量測上發現當進行寫入/抹除時，除了在主動閘施加一偏壓外，寫入/抹除的速度會隨輔助閘偏壓的增加而明顯加快，其原因來自於輔助閘偏壓能夠有效的影響奈米線中的電子密度，因而影響穿隧電子的數目與其效率。另一方面，本研究所製作的記憶體元件其雙閘極介電層材料分別為二氧化矽與二氧化矽-氮化矽-二氧化矽，當採用具二氧化矽介電層之閘極為讀取閘時，寫入/抹除態的感測窗口會展現出與輔助閘施加偏壓的相關性，然而此現象並不會在傳統上以二氧化矽-氮化矽-二氧化矽為介電層之閘極做為讀取閘時發生。研究發現其根本原因為背閘效應(back-gate effect)。於此架構下，我們做了許多此兩種讀取模式的操作特性比較，包括寫入/抹除速度、保持性與耐操性。最後我們嘗試將二氧化矽-氮化矽-二氧化矽同時做為雙閘極之介電層材料以驗證單一元件具有二位元儲存(2-bit/cell)的可行性。

關鍵字: 奈米線， 獨立雙閘極，多閘，多晶矽，臨場摻雜，薄膜電晶體，次臨界擺幅，穿隧，雜質，低溫測量，遲滯，非揮發記憶體，矽-氧化矽-氮化矽-氧化矽-矽，背閘效應，單一記憶胞二位元儲存

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Abstract

A simple and low-cost method of fabricating poly-Si nanowire (NW) devices is proposed in this dissertation. The feature lies in turning off the bias power in an inductively coupled plasma etcher combined with the addition of SF_6 gas to obtain an isotropic etching recipe with high selectivity. A re-entrant 10~100 nm wide cavity inside the *in situ* doped poly-Si could then be formed with this recipe, which in turn determines the feature size of the NW. Following the formation of NWs, another gate stack could be deposited and patterned such that the device has two independent gates that help increase the functionality and flexibility of device operation.

To investigate the influence of the size of NW on device characteristics, NWs with varying widths were fabricated by controlling the duration of lateral etching. It is observed that as the NW gets narrower, the performance of double-gated mode would be enhanced to a larger extent compared with that of two single-gated modes. The root cause is identified to be related to the fact that the modulation rate of grain boundary barrier height of poly-Si by the gate is dependent on the NW dimension. Nevertheless,

in order to avert inadvertent channel doping, the original device process flow is designed in a way that the series resistance of the source/drain may become too significant. In this regard, we propose a modified version of process in which *in situ* doped poly-Si replaces ion implantation for forming the source/drain regions. Devices fabricated with this approach demonstrate evidently improved on- and off-current. What's more, a record-breaking value of subthreshold swing as low as 73 mV/dec could be obtained.

In addition to process optimization to better the device performance, in an attempt to probe into carrier transport characteristics of NW, e-beam direct writing is adopted in our process as well to reduce the channel length below 100 nm. Meanwhile, cryogenic measurement facilities are employed to provide a comprehensive analysis on device transport behavior. It is found that as the temperature of measurement is lower than 100 K, one of the single-gated modes displays subthreshold swing that is well below the theoretical limit of MOSFET. Plus, this kind of phenomenon is only exclusive to devices with channel lengths shorter than 100 nm. With the aid of simulation and experimental verification, it is identified that this intriguing effect is caused by the non-uniform distribution of dopants introduced by ion implantation such that the controllability of gate over the channel is a function of location along the channel and the electrostatic potential of the channel would exhibit a hump-like profile.

Given that most of the state-of-the-art 3D memory technology employs poly-Si as its active layer, the merit and operational feasibility coming from the implementation of independent double-gate scheme on SONOS non-volatile memory devices are also investigated. During programming/erasing, apart from the biases applied to the active gate, experimental results indicate that the programming/erasing speed is a monotonically increasing function of the auxiliary gate bias. This may be due to the

electron density within the NW channel that the auxiliary gate helps modulate, which in turn affects the number of tunneling electrons and the programming/erasing efficiency. The device fabricated has oxide and oxide-nitride-oxide stack as dielectrics for two independent gates, respectively. The V_{TH} window between P/E states shows a strong dependence on the auxiliary gate bias when the gate with oxide as dielectric is used as the read gate, which is in contrast to the fairly constant V_{TH} window observed in a conventional mode (*i.e.*, the read gate is with oxide-nitride-oxide as dielectric). Back-gate effect is recognized to be the major mechanism in play. To further delve into the implications, several comparisons between those two feasible read modes are made, including programming/erasing speed, retention, and endurance characteristics. Finally, proof-of-concept 2-bit/cell feature is demonstrated by utilizing oxide-nitride-oxide stack as the dielectrics for both gates.

Keywords: Nanowire, Independent Double-Gated (IDG), Multiple-Gated, Polycrystalline Silicon (Poly-Si), *In Situ* Doping, Thin-Film Transistor (TFT), Subthreshold Swing (SS), Tunneling, Dopant, Low Temperature Characterization, Hysteresis, Non-Volatile Memory (NVM), Back-Gate Effect, Silicon-Oxide-Nitride-Oxide-Silicon (SONOS), 2-bit/cell

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陳威臣
誌於風城交大
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Chapter 1

Introduction

To maintain the momentum of CMOS scaling, multiple-gated nanowire (NW) devices have been proposed as one of the most promising future transistor structures [1-1], due to the better gate controllability to suppress the short channel effects (SCEs). NW, basically, can be defined as a narrow stripe material with its cross-sectional feature size less than 100 nm. It has been conceived as an ideal building block for nanoelectronics and optoelectronics. One unique feature of NW lies in its very tiny volume and large surface-to-volume ratio, thus making it suitable for a wide array of applications. For memory applications, fast programming/erasing efficiency and low voltage operation can be facilitated and the large surface-to-volume ratio feature promotes high sensitivity for sensor applications. As a result of the tiny cross section of NW body, confinement of carriers in the plane perpendicular to the channel direction can occur. Already a plethora of intriguing phenomena are associated with this nano-scale structure, such as Coulomb blockade [1-2], quantized conductance [1-3], and reduced phonon scattering [1-4], to name just a few.

Though most of the previous works regarding NW research focused on single-crystalline Si based technology for realizing high performance CMOS transistors, recently a new concept of NW based thin film transistors (TFTs) has started to gain attention [1-5][1-6]. Compared to single-crystalline Si wafer technology, TFT devices completely eliminate the need for a high-cost substrate. This merit is especially profound when prohibitive silicon-on-insulator (SOI) architecture starts to emerge as another substrate alternative in order to promote the fabrication of multiple-gated device such as FinFETs [1-7]. For the macroelectronics industry where it is preferred to construct electronic devices and components over a large area substrate, TFT architecture is a promising option since it merely requires a thin active layer to be deposited onto an insulating substrate. Therefore, glass and plastic substrates become the primary choice as they are flexible, light weight, and most importantly, cheap. Below an overview of NW technology is briefly given.

1.1 Overview of Nanowire Technology

Gordon Moore in 1965 predicted that the number of transistors in a chip would double every two years [1-8]. Even though it takes eighteen months to be exact for the number to increase by twofold, this prediction has been termed “Moore’s law” and has become the guiding principle of the semiconductor industry for the past few decades. To follow this path mainly depends on the downsizing of transistors. The potential of constant electric field scaling was recognized in a renowned paper by Robert H.

Dennard *et al* [1-9] that underlies Moore's law. Yet as the last half-century has seen a relentless miniaturization of electronics in pursuit of high performance CMOS technology, the physical limit of geometric scaling is imminent as the transistor dimension approaches only a few tens of nanometers [1-10]. Among the various structures ever proposed, NW is recognized as the most promising one to suppress SCEs and sustain the scaling path for nano-scale MOSFETs [1-11]. With NW, many possible and interesting applications have also been explored [1-12]. There are generally two types of methods for the preparation of NW, termed top-down and bottom-up, to be described as follows.

1.1.1 Top-down Approach

This approach typically employs advanced lithographic tools (e-beam [1-13] or deep ultraviolet (DUV) [1-14]) to directly generate nano-scale photoresist patterns, which are then transferred to the underlying SOI substrate by dry etching. This kind of process can precisely control and align the structural parameters and minimize variations of devices, so it is suitable for mass production though at the sacrifice of high manufacturing cost. Current state-of-the-art technology is able to generate line width less than 40 nm and with the aid of some innovative skills including trimming, double-patterning, hydrogen annealing, self-limiting oxidation, and thermal flow, etc., critical dimension down to sub-10 nm can be achieved [1-14]-[1-16]. Major shortcomings of this procedure are the associated expensive exposure apparatus and substrate materials as well as the inflexible choice of NW material due to the limited selection of substrates.

1.1.2 Bottom-Up Approach

A detailed and comprehensive review of this approach can be found in [1-12] and [1-17][1-18]. This approach is mainly based on chemical processes to synthesize and grow NWs of various kinds of materials. After NWs are synthesized, they are harvested and dispersed into a solution, which are then deposited onto an oxidized substrate (to serve as the back gate) followed by metal electrodes attachment to complete a field effect transistor structure. Vapor-liquid-solid (VLS) [1-19] is the most well-established mechanism to produce NW. In this procedure, the metal nanocluster is first heated in the ambient of gas-phase reactants of the semiconductor material to be synthesized. When the nanocluster is heated to above the eutectic temperature, liquid droplet of the metal/semiconductor is formed. Continuous supply of semiconductor reactants then supersatures the cluster, resulting in nucleation and directional growth of a wire-like structure. The dominant growing direction (axial or radial) is found to be intimately related to the growth process conditions, such as the temperature, flow rate, reactant species, and pressure. Single-crystalline NW can be obtained using this method. In the case of growing Si NW, gold nanocluster and silane (SiH_4) are the most commonly used catalyst and reactant, respectively. Since the material of NW to be produced depends on the precursors used, III-V and II-VI NWs have also been prepared besides Si [1-20]. In this regard, in comparison with top-down, bottom-up is far more flexible in terms of the NW material that can be obtained. Nevertheless, metal contamination is a major concern for metal-catalyzed growth. Oxide-assisted growth [1-21] without the need for metal-catalyst could get rid of this issue, but the NW thus formed could contain plenty of defects.

In short, bottom-up approach is definitely the better choice for experimental purposes because it is cheap and can grow various kinds of materials. However, it is plagued by several shortcomings as well. First, reproducible transfer and precise control of structural parameters of NWs are very difficult to accomplish. Alignment and positioning are daunting tasks that are hard to overcome. To fabricate reliable contacts between metal and NWs requires sophisticated manipulation and poses as another showstopper for bottom-up approach.

To this end, in this dissertation we propose and develop a novel technique for the fabrication of Si NW devices that without any compromise combines all the merits of top-down and bottom-up approaches, namely, cost effectiveness, good reliability and reproducibility, and CMOS-compatibility.

1.2 Multiple-Gated Devices

Faced with an ever greater challenge of fabricating a “well-behaved” transistor for which SCEs are minimized in the era of 32 nm technology node and beyond, a number of new processing schemes have been embraced to address this issue. For the purpose of resolving poly-gate depletion and alleviating non-negligible gate dielectric tunneling current, high-κ/metal gate is being pursued actively and is already adopted in commercial 45 nm microprocessors of Intel [1-22]. Another option of relieving SCEs is to resort to multiple-gated configuration. As the name suggests, in a multiple-gated transistor, the active layer is controlled by more than one gate as opposed to planar single-gated counterparts. This kind of structure is capable of effectively preventing the drain field penetration that weakens the gate controllability over channels thereby leading to SCEs. On account of the better electrostatic control of channels, for a given channel width, larger driving current can be provided by multiple-gated configuration. Of all the multiple-gated structures ever proposed so far, FinFET is considered as the one most appropriate for practical applications because it is actually quasi-planar and is most compatible with modern ULSI (ultra large scale integration) technology [1-23]. Moreover, the conduction width in FinFET, which is determined by the fin height, is along a direction that is normal to the substrate plane. This vertical feature offers an improvement in density that is not restricted by the resolution of lithographic tools.

Evolving from the original double-gated structure, several variations of FinFET have been reported, including tri-gate [1-24] and Ω-gate [1-25]. In particular, the gate-all-around type device where the channel is fully wrapped by a surrounding gate is considered the most ideal structure to proffer the best gate controllability over the channel [1-26]. Selected devices of NW or FinFET structure with sub-20 nm channel length are listed in Table 1-I.

1.3 Transport Behavior of Nanowire Devices

The paradigm shift caused by NW creates whole new concepts and perspectives on device physics and possibilities that conventional planar counterparts have yet to offer. From a microscopic point of view, this kind of low-dimensional structure is suitable for studying quantum-mechanical effects. Many reports focused on the carrier transport properties in NW devices for which well-established theories of three- or two-dimensional materials are no longer appropriate. Energy bands are split into sub-bands and the energy levels become discrete by the tiny volume of NW [1-30]. Because of the nano-scale cross section that confines the wave functions of sub-bands, carriers in NW devices must transport through a large number of one-dimensional sub-bands. Quantum confinement, sub-band splitting, and surface and interface relaxation [1-31]-[1-33], *etc*. are among a plethora of effects that must be taken into account in order to correctly interpret the NW characteristics, including unexpected increase of threshold voltage (V_{TH}) with reduced NW width [1-34], oscillation of drain current and mobility [1-32], and reduced Stark effect [1-35]. Recently, dopant distribution has been identified as another major factor in influencing the carrier conduction behavior in ultra-short NW devices [1-36]. Simulation results have shown that NW transistors may approach ballistic transport [1-37], *i.e.,* a carrier does not experience any collision with other carriers or elastic centers during its traverse from the source toward the drain. In the quasi-ballistic model proposed by Lundstrom [1-38][1-39] where there is no sufficient scattering events occurring inside a short channel MOSFET device, backscattering effects near the source start to become prominent, but since this effect is linked to the source side mobility, the concept of mobility is still relevant. On the other hand, if the channel length is scaled further (less than 10 nm [1-40]), no scattering events would occur and in this scenario the transport of carriers operates in the full ballistic regime. Drain current under ballistic transport has been shown to depend only on the carrier concentration near the source and the injection velocity at the peak of the barrier at the source side [1-41][1-42], which is determined solely by the thermal velocity in the case of non-degeneracy. Thus, the concept of mobility becomes meaningless, leading to a profound change of mindset on how the carrier transport properties should be examined. For typical short channel planar devices, scattering defects associated with pocket implant near source/drain junctions result in mobility degradation as the channel length is made shorter [1-43][1-44]. Even though NW exhibits similar behavior that the "extracted" mobility tends to decrease with reduced channel length, this is essentially an artifact and can be explained by the "ballistic mobility" model [1-45]. As a matter of fact, since NW has entered into ballistic regime, the measured mobility no longer determines the transport property and the actual transport behavior will not degrade with channel length scaling [1-46]. In other words, not only does NW device possess better immunity against SCE, it is also promising to provide ballistic transport when being downsized to ultra-short channel lengths. Another intriguing effect exclusive to NWs is that the drain current of linear regime (low V_D) in strong inversion is found to decrease with decreasing temperature, which is shown to be caused by the inter-sub-band scattering induced by quantum confinement [1-32]. Yet, in saturation regime (high V_D), this effect is diminished and the mobility-temperature relationship again resorts to what is dictated by phonon scattering. In addition, differential conductance fluctuations are observed in output curves as the series resistance of the drain extension is changed by the interplay between inter-sub-band transitions and quasi-ballistic transport [1-47].

One concept called "quantum capacitance limit" introduced recently further highlights the performance advantage of 1-D NW device over bulk counterparts in terms of the power delay product improvement that can be achieved from scaling [1-48]. To realize a well-behaved device that exhibits electrostatic integrity, two major conditions should be fulfilled. First, the maximum of surface potential in the channel that governs the injection of carriers from the source is mainly modulated by the gate voltage instead of the drain voltage. Second, the oxide capacitance ought to be much larger than the inversion layer or quantum capacitance, which is the change of channel charge with respect to the surface potential. The first condition is always met as long as the channel length is much longer than the natural scaling length [1-49], whereas the second one is dependent on the operation state of the device. In the off-state, the quantum capacitance is nearly zero because the channel charge shows little variation. However, in the on-state, this capacitance is proportional to the density of states present in the channel [1-50], which increases with the gate voltage in a bulk device. Accordingly, the modulation of the surface potential is less efficient in the on-state, explaining the gradual increase of the subthreshold swing with a larger gate voltage of a conventional device. The scenario is vastly different in the case of 1-D NW device for which the density of states is inversely proportional to the square root of the difference between the carrier energy and surface potential [1-50]. Consequently, it is easier for NW to reach the so-called quantum capacitance limit, where the gate dielectric capacitance readily exceeds the quantum capacitance and the gate electrode is still able to provide ideal control of the surface potential in the on-state. In other words, the thickness of the gate dielectric in a 1-D NW transistor required to meet the criterion of quantum capacitance limit can be thicker and is much more technologically feasible than the bulk devices.

To fully capture the underlying physical mechanisms of NW requires devices with sub-10 nm channel length, which are still difficult to fabricate if not impossible [1-15], thus most works only use theoretical formalism to predict the transport behavior of NW devices. Some commonly utilized ones are Boltzmann transport equation [1-51], non-equilibrium Green's function (NEGF) [1-52][1-53], and quantum diffusion method [1-54]. Each of these approaches is suitable only for some specific conditions depending on the temperature and channel length considered. Additional approximations are needed as well to simplify the complexity of NW band structures and reduce the computational time. Hence, it still takes further advance in process technology and development of more precise theoretical modeling to gain a comprehensive insight into the potential of NW transistors.

1.4 Overview of Nonvolatile Memory Technology

As portable electronic products have already become indispensable components of daily life, nonvolatile memory technology is being used in a wide array of commodities, including cell phones, USB drives, memory cards, *etc*. Being one of the two types of semiconductor memory, nonvolatile memory retains its stored data even if the power is turned off as opposed to volatile memory where the data are immediately lost as soon as the power is turned off. This unique property makes nonvolatile memory an ideal choice for low power portable electronic products.

The first nonvolatile memory device was reported in 1967 by D. Kahng and S. M. Sze at Bell labs [1-55]. The gate stack is a five-layered structure consisting of metal-oxide-metal-oxide-semiconductor. As charges are stored in the metal that is surrounded by two dielectrics, this is called floating-gate (FG) type nonvolatile memory. Even though along the way there are plenty of variations in terms of the charge storage layer and the stack composition or thickness (e.g., MNOS [1-56], FAMOS [1-57], ETox^{TM} [1-58] and SAMOS [1-59]), FG is still the mainstream technology to date in which the storage layer is now made of poly-Si. Of all the different types of memory technology nowadays, Flash memory with FG structure has gained a lot of attention owing to its particular features, such as low cost, low power consumption, good endurance, high density, and long data retention capability. In Flash memory, program/erase stressing can be performed repetitively up to 10^5 cycles without significant degradation or loss of stored data. Another advantage involves the byte-selectable program operation and block “flash” erasure. Unfortunately, as the feature size is made smaller with each technology node, several scaling challenges have emerged. Hence, charge-trapping-type Flash, to be discussed below, was proposed to succeed FG as the next generation Flash memory technology by Samsung in 2005 [1-60].

1.4.1 Charge Trapping SONOS Memory

Aggressive scaling of conventional FG type memory device has encountered quite a few issues that must be seriously dealt with, including narrow FG-FG space to contain control gate, FG-FG interference coupling, read or program noise, stress-induced leakage current (SILC), and severe SCEs [1-61]. To address those issues, charge-trapping type nonvolatile memory devices, with nitride read-only memory (NROM) [1-62] and Si-oxide-nitride-oxide-Si (SONOS) [1-63] being the mainstream, have recently emerged as new promising candidates for continuing the miniaturization trend, together with other innovative nonvolatile memory concepts, including ferroelectric and magnetoresistive memories [1-64], phase-change memory [1-65] and unified random access memory [1-66] that has claimed to have both volatile and nonvolatile functionalities. Among these devices, SONOS, with a plethora of variations such as bandgap engineered (BE) SONOS [1-67], Ta-AlO-Nitride-Oxide-Si (TANOS) [1-68], *etc*, has shown its high performance and promising potential for future Flash memory applications.

In its basic structure, SONOS uses a non-conductive nitride layer for storing charges compared with conductive poly-Si in FG. As a consequence, charges are discretely stored in the nitride and a single defect present in the tunneling oxide would not cause all stored charges to leak out. Combined with the deep energy level of nitride for charge storage, retention characteristics can be dramatically improved. As in NROM, by storing charges at two different sites in the nitride (*e.g.,* source-side and drain-side), 2-bit/cell operation is feasible. In addition, because the stack height of SONOS is much more reduced over that of FG, interference coupling is suppressed to a great degree, which is helpful for further advancement of device scaling. Recently, TFT-based SONOS devices have been investigated in an effort to realize system-on-panel (SOP) or system-on-chip (SOC) applications [1-69]. TFTs could also facilitate 3D integration technology [1-70] which greatly improves interconnect density, reduces cost and provides a platform for heterogeneous integration.

1.4.2 Nanowire-Based Nonvolatile Memory

Besides being able to scale device dimensions down to nano-scale regime without sever SCEs, NW can be useful for nonvolatile memory technology as well. Owing to its large surface-to-volume ratio property, NW is highly sensitive to its surface conditions.

Making use of this feature, the threshold voltage of a memory device can be altered to a large extent by a small amount of stored charges, allowing reduced program/erase operation voltage and stressing time to obtain a sufficient memory window.

Most of the reports concerning NW nonvolatile memory devices rely on the formation of a charge storage layer upon the NW surface to adjust the threshold voltage of the device. For the purpose of achieving larger voltage drop across the tunneling layer, SONOS device integrated with gate-all-around configuration has been demonstrated [1-71]. And to prevent some undesirable effects such as electron back-tunneling from the gate electrode and insufficient electric field across the tunneling oxide, an optimized version called TAHOS (TaN/Al_2O_3/HFO_2/SiO_2/Si) was reported to significantly improve both programming and erasing speeds [1-72].

1.5 Motivation

NW transistors have revealed their promising potential in a wide variety of applications. Development of high performance NW devices with reliable and reproducible processes is urgently needed. To cope with the issues encountered in top-down and bottom-up approaches introduced in Section 1.1, our lab (Advanced Device Technology Laboratory) has proposed several innovative procedures of fabricating poly-Si NW TFTs using low cost and simple methods [1-73]-[1-76]. The first type in [1-73] employed sidewall spacer etching technique to define simultaneously poly-Si NW channels and source/drain regions followed by another modified version where inverse-T and top gates were formed to fulfill a multiple-gated configuration [1-74]. Though our proposed scheme belongs to the top-down category, it includes the merits of both top-down and bottom-up approaches without their drawbacks. In [1-73]-[1-75], after deposition and anisotropic etching, poly-Si NWs are formed along the sidewall of a pre-formed gate. Major benefits of this method are listed as follows.

1. Precise alignment and positioning of NWs.
2. Well-controlled NW size as it is related to the thickness of the deposited film and the etching duration.
3. Self-alignment between NW channels and source/drain regions.
4. CMOS compatibility.

In spite of all these advantages, its triangular shape may have hindered its practical applications and it may suffer severe SCE if the channel length is to be further scaled down since the electric field is very likely to be concentrated on a certain vertex. In the mean time the irregular shape makes it difficult for an accurate theoretical modeling. To solve this dilemma, we come up with a modified independent double-gated TFT with rectangular NW channels. Such a design allows more flexibility in device operation and may help improve reliability characteristics in nonvolatile memory applications.

1.6 Organization of the Dissertation

Six chapters are contained in this dissertation. Background and motivation are described in Chapter 1. Chapter 2 discusses the device structure, fabrication process, and basic electrical characteristics of the main device architecture proposed in this study. Source/drain engineering for performance enhancement is investigated and analyzed in Chapter 3. Study on the transport behavior at cryogenic ambient is conducted in Chapter 4. Chapter 5 details the merits offered by independent double-gated configuration in SONOS memory devices. In Chapter 6, major achievements and summary are stated, and suggested future works are listed. The following specifies the detailed content of each chapter.

In Chapter 1, overview of NW technology and multiple-gated devices are mentioned along with a brief description of NW transport properties and nonvolatile memory technology. As noted in the motivation, to deal with some dilemma of NW fabrication process and to optimize the structure of our previously reported device, a novel independent double-gated poly-Si NW transistor with rectangular channels is thus proposed.

Chapter 2 elucidates the structure and fabrication process of the proposed poly-Si NW devices. An isotropic and selective plasma etching technique is explored to form a rectangular-shaped NW. Subsequently, impacts of different operation modes associated with the double-gated configuration on device performance are discussed followed by the examination of the root cause for the size dependency, which is found to be intimately linked to the capability of the gates in adjusting the magnitude of grain boundary barrier height.

In Chapter 3, source/drain engineering is investigated to enhance device performance. Replacing ion implantation with *in-situ* doping for the formation of source/drain regions, it is demonstrated that the overall electrical characteristics are clearly improved and a record-breaking 73 mV/dec subthreshold swing is achieved.

In Chapter 4, to probe the underlying transport properties, devices with channel lengths ranging from 39 nm to 5 μm are fabricated and characterized under cryogenic ambient. A very intriguing abrupt switching phenomenon is observed when the device is operated under one of the two single-gated modes. In addition, this behavior shows a strong dependency on the channel length that is in obvious conflict with the conventional theory concerning SCE as the subthreshold current is reduced with shorter channel length. A simple model based on the barrier formation near the source/drain due to non-uniform gate doping is proposed to explain this phenomenon.

In Chapter 5, the influence of independent double-gated configuration on SONOS type nonvolatile memory applications is discussed. In contrast to the convention where the programming/erasing gate also acts as the read gate, a dedicated read gate with oxide-only dielectric is proposed in the new mode. Greatly improved programming speed is achieved while the erasing speed, albeit initially retarded, shows enhancement when the erasing time is larger than a certain value. Retention characterization indicates that this new read mode offers a larger memory window after 10-year extrapolation. In addition, a proper auxiliary gate bias applied during programming/erasing processes is found to improve the programming/erasing speed. Finally, by taking advantage of the separate-gated feature, 2-bit/cell functionality is realized as well.

Chapter 6 summarizes the results and contributions made in this dissertation and provides suggested items for future works.

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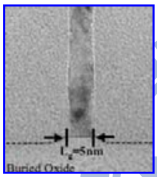
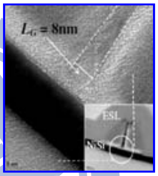
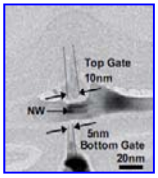
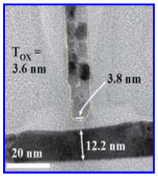
Table 1-I Comparison of selected NW transistors with sub-20 nm channel length.

Ref	**1-16**	**1-27**	**1-28**	**1-29**	**1-15**
NW diameter (nm)	**10**	**8**	**10**	**16**	**W/H=14/12**
Gate structure	**omega**	**GAA**	**GAA**	**GAA**	**Tri-gate**
L (nm)	**5**	**15**	**8**	**10**	**3.8**
Normalization method	**diameter**	**diameter**	**diameter**	**perimeter**	**perimeter**
I_{ON} (μA/μm)	**115**	**1940**	**3740**	**1494**	**976**
I_{ON}/I_{OFF}	**$>10^5$**	**$>10^5$**	**$>10^7$**	**$>10^5$**	**$>10^4$**
DIBL (mV/V)	**14**	**43**	**22**	**88**	**148**
SS (mV/dec)	**63**	**71**	**75**	**89**	**92**
V_{DD} (V)	**-1**	**-1**	**1.2**	**1**	**1**
Microscopic image					

Chapter 2

Double-Gated Poly-Si Thin Film Transistor with Twin Nanowire Channels

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2.1 Introduction

Acting as an important building block in drivers of liquid crystal display (LCD), polycrystalline-Si (poly-Si) thin-film transistors (TFTs) have become very attractive for future 3-D electronics integration [2-1]. Compared with single-crystalline Si-based microelectronics where expensive substrates are inevitable, high performance TFTs have emerged as a promising alternative for macroelectronics employing glass and plastic substrates where flexibility and light weight are primarily preferred [2-2]. It would be quite a breakthrough if poly-Si TFTs could display comparable performance to single-crystalline Si-based devices on account of its low fabrication cost. However, the granular structure inherent in poly-Si significantly degrades the carrier mobility [2-3] and limits its adoption and proliferation in advanced very large scale integration (VLSI) technologies. To address this intrinsic material issue, a plethora of recrystallization methods for grain enlargement have been proposed, with solid-phase crystallization (SPC) [2-4], metal-induced lateral crystallization (MILC) [2-5], and excimer laser annealing (ELA) [2-6] being the most commonly used. To continue the scaling trend while simultaneously improving poly-Si device characteristics, such extrinsic modification as ultra-thin body structures provides an effective solution for the aforementioned problem. From a microscopic perspective, one-dimensional nanowire (NW) structure also offers a unique platform for physical properties not easily observed in conventional devices. The unique characteristics of large surface-to-volume ratio and high sensitivity to surface conditions have rendered NW a functional device suitable for bio-sensing [2-7] and nonvolatile memory [2-8] applications.

Among the various methods for NW fabrication, top-down approaches avoid the misalignment and hard-to-manipulate issues frequently encountered in bottom-up processes, and meanwhile are more compatible with modern CMOS process flow. Moreover, when combined with multiple-gated scheme, the fabricated device exhibits enhanced drive current and steeper subthreshold swing due to improved control of electrostatic potential in the channel, as demonstrated in various works, including FinFET [2-9], omega-gate [2-10], tri-gate [2-11], and gate-all-around [2-12], *etc*. Meanwhile, CMOS-compatible performance has also been achieved using poly-Si NW devices [2-13][2-14]. To this end, we had presented several innovative top-down approaches for forming poly-Si NWs using conventional I-line based lithography [2-15]-[2-17]. The NW channels were formed by the sidewall spacer etching technique and for the independent double-gated structure in [2-17], the NW channels were surrounded by an inverse-T-shaped gate and a top gate. This kind of scheme has been shown to dramatically enhance the device performance under double-gated operation and provides more flexibility in device operation [2-18]. However, the cross-sectional shape of NW channels was triangular, which is irregular, and may lead to non-uniform carrier distribution inside the nanowire, making accurate theoretical modeling extremely difficult to perform. In view of this, a device with more regularly shaped NWs is highly demanded and in this study we propose a novel technique of forming rectangular NWs by adopting selective plasma etching.

In this chapter, the condition for isotropic plasma etching of poly-Si with high selectivity and controllable etching rate is first discussed. Then, based on the optimized condition, independent double-gated poly-Si NW TFTs with various NW dimensions are fabricated and characterized.

2.2 Experimental

Since we aim to fabricate a poly-Si NW transistor by forming a cavity at two sides of a nitride/poly-Si/nitride stack through selective etching of the sandwiched poly-Si followed by refilling with the active layer, in this section we would like to discuss some of the critical parameters that should be carefully adjusted. Subsequently, device fabrication process and measurement setup will be briefly mentioned.

2.2.1 Investigation of Selective Plasma Etching Conditions

The main feature in this structure lies in the fact that a sub-100 nm cavity could be formed by isotropic plasma etching using a high density plasma (HDP) etching apparatus. In this dissertation a transformer coupled plasma (TCP) reactor with model number TCP 9400 manufactured by Lam Research was used, which operates by inductively coupling RF power to plasma. This tool is equipped with two RF power generators. The top source RF power generates plasma and determines ion density, while the bottom bias RF power is responsible for controlling the ion bombardment energy. In other words, ion density and energy are independently controlled in this reactor, thus solving the inflexibility and poor efficiency of conventional capacitively-coupled reactors. In contrast to the typical anisotropic reactive-ion-etching (RIE) process in an HDP etching tool, the sub-100 nm cavity-forming technique is accomplished by turning off the bottom bias. In this way, the bombarding energy of ions would be reduced to achieve high etching selectivity between poly-Si and the other layers.

The process flow of the proposed two-step N^+ poly-Si etching scheme is depicted in Fig. 2-1. A stack of layers comprising 100 nm-thermal oxide/50 nm-nitride/100 nm-N^+ poly-Si/50 nm-nitride was deposited sequentially on a 6-inch Si wafer. Here the

N^+ poly-Si layer is formed by *in situ* doping. Next, the top nitride and N^+ poly-Si stack were patterned by anisotropic etching in a TCP reactor. Figure 2-2 (a) displays a scanning electron microscope (SEM) picture taken after this step. It is observed that the final etching profile is anisotropic. This is because chlorine etching mainly proceeds in an ion-induced manner and the applied bottom bias helps enhance the vertical ion bombardment; therefore the etched profile is essentially anisotropic.

Following the photoresist stripping, the wafer was loaded into the same reactor for performing the selective and isotropic N^+ poly-Si plasma etching. In this step, the bottom bias is turned off and fluorine-containing gas SF_6 is added along with chlorine for increasing the isotropic etching component, with the results shown in Figs. 2-2 (b)~(d) corresponding to different etching conditions. It has been well known that poly-Si can be etched by fluorine-based etchants because of high volatility of SiF_4 [2-19]. Meanwhile, F radicals are usually produced in large quantities in plasma along with little polymer formation so the final profile will be relatively isotropic. Representative images in Figs. 2-2 (b)~(d) indicate that fluorine addition indeed greatly enhances the isotropic profile and demonstrates high selectivity with respect to the nitride layers. This is quite reasonable because in addition to rendering the motion of bombarding ions a random manner, setting the bias power to zero also improves etching selectivity of poly-Si against other materials. It is noted that this isotropic etching is performed in the same reactor as that of anisotropic etching, suggesting the compatibility and convenience of this novel procedure. Nonetheless, the profiles in Figs. 2-2 (b) and (c) reveal that the etching parameters still need to be optimized given that the lateral etching depths are still too deep for both cases, probably owing to either the top power and SF_6 flow rate that are too large or the etching time that is too long. Even though reducing the etching duration can help decrease the etching depth down to sub-100 nm regime, as shown in Fig. 2-2 (d), the etching rate is still too fast to control if sub-50 nm dimension is demanded. In light of this, the etching recipe is adjusted to P = 5 mtorr, Cl_2 = 50 sccm, SF_6 = 10 sccm, and top power = 300 W. To demonstrate the merit of this approach in fabricating deca-nanometer NWs, Fig. 2-3 displays the lateral encroaching depth as a function of etching time as characterized by SEM, indicating that the NW dimension could be flexibly controlled. In fact, it is very hard to produce the same result each time for etching with duration less than 10 seconds since the condition of glow discharge is not yet stable in such a short period. However, it is believed that the proposed method will have more reproducible results provided that the etching condition is optimized. In other words, by carefully adjusting the flow rate of source gas, RF power, and etching time, the structural parameter can be easily and reliably shrunk into deca-nanometer regime.

2.2.2 Device Fabrication Process

The top view of the proposed device is shown in Fig. 2-4 along with the fabrication flow in Fig. 2-5 which is briefly described below. A 6-inch Si wafer capped with 100-nm-thick thermal oxide and 50-nm-thick SiN layer served as the substrate on top of which 100-nm *in situ* doped N+ poly-Si and 50-nm–thick SiN were next sequentially deposited. Subsequently, the topmost SiN hardmask and N+ poly-Si were patterned by lithography and dry etching (1st Gate in Fig. 2-4). Then, cavities underneath the nitride hardmask were formed by employing the selective plasma etching method discussed in the previous sub-section. With an eye to examining the impact of NW dimension on the device performance, through controlling the etching duration (8 sec, 10 sec, and 12 sec), devices with three different NW dimensions were fabricated. Afterwards, 20-nm TEOS (tetraethoxysilane) oxide and 100-nm amorphous-Si were deposited by low pressure chemical vapor deposition (LPCVD) to serve respectively as the 1st gate dielectric and active layer. Due to the excellent comformality offered by LPCVD, the cavities formed by selective plasma etching were completely filled with the deposited materials. The intention of inserting a SiN layer between the thermal oxide and N+ poly-Si becomes evident here in that it helps preserve the shape of the cavity during RCA clean process that involves HF dip prior to the deposition of the 1st gate dielectric. Solid phase crystallization (SPC) was then performed at 600 °C in N_2 ambient for 24 hours to transform the amorphous-Si into poly-Si. The reason that recrystallized poly-Si is adopted as the channel material instead of as-deposited poly-Si is that the poly-Si obtained through direct deposition exhibits smaller grain size and a larger number of defects [2-20]. Subsequently, source/drain (S/D) implantation was conducted by phosphorus with 15 keV energy at 5 × 10^{15} cm^{-2} dose. Here a low energy implantation was chosen in an attempt to avoid inadvertent channel doping which might cause degraded gate controllability and severe leakage current. Optimization for S/D doping will be discussed in more detail in Chapter 3.

After forming S/D photoresist patterns (S and D in Fig. 2-4), S/D regions and NW channels were simultaneously defined by a single anisotropic dry etching step. In this step, the portions of poly-Si residing in the cavities remained intact and would become the NW channels in the final structure. For multiple-gated operation, the 2nd gate stack consisting of 20-nm TEOS oxide and 100-nm *in situ* doped N+ poly-Si gate was next deposited and patterned (2nd Gate in Fig. 2-4). All devices were then covered with 300-nm-thick TEOS oxide passivation layer by LPCVD at 700 °C for 4 hours, which is sufficient for activating the dopants previously introduced into S/D regions. The device fabrication was completed after standard back-end processing, including contact hole opening and standard metallization steps. To further boost the device performance and reduce fluctuation, NH_3 plasma treatment at 300 °C for 3 hours was performed on all devices before characterization [2-21].

2.2.3 Measurement Setup and Electrical Characterization Methods

Before further investigation of the electrical characteristics, several important electrical parameters and extraction methods used in this dissertation are clarified. Electrical measurements were performed by HP 4156A semiconductor precision analyzer which was controlled by a personal computer through Interactive Characterization Software (ICS), and Agilent 5250A switch. During all measurements, the temperature was controlled and stabilized by a temperature-regulated chuck.

Based on the transfer curve measured, definitions for some of the important parameters are listed below.

1. Threshold voltage (V_{TH})

The threshold voltage (V_{TH}) is defined by the constant current method and is equal to the gate voltage when the drain current reaches a particular value, which is expressed as

$$V_{TH} = V_G @ I_D = \frac{W}{L} \times 10nA \quad , \tag{2-1}$$

where W and L represent respectively the channel width and length.

2. Subthreshold swing (SS)

It is defined as the magnitude of gate voltage required to alter (either increase or reduce) the drain current by an order of magnitude in the weak inversion region, which is given by

$$SS = \frac{\partial V_G}{\partial (log I_D)} \quad (2\text{-}2)$$

3. Field effect mobility (μ_{FE})

As in the equation relating the drain current to the gate voltage, the field effect mobility (μ_{FE}) can be derived as follows,

$$I_D = \frac{W}{L} C_{OX} \mu_{FE} (V_G - V_{TH} - \frac{1}{2} V_D) V_D \Rightarrow \mu_{FE} = \frac{G_M L}{W C_{OX} V_D}, \quad (2\text{-}3)$$

where G_M is the transconductance obtained by the derivative of the drain current with respect to the gate voltage and all the other symbols have their usual meanings.

4. Operation mode

Owing to the fact that the proposed device possesses two independent gates, during I-V measurement there are three feasible read modes as determined by the choice of the driving gate, which are termed SG-1, SG-2, and DG modes, as defined in Table 2-I. For SG-1 mode, the 1st gate acts as the driving gate while the 2nd gate is called the auxiliary gate (AG) with a fixed bias, and vice versa for SG-2 mode. For the following context, AG will be applied a bias equal to zero (grounded) unless otherwise specified. DG mode, on the other hand, stands for the scheme when both gates are tied together to drive the device simultaneously.

2.3 Results and Discussion

2.3.1 Impacts of Double-Gated Configuration on Device Performance

Shown in Fig. 2-6 is a cross-sectional transmission electron microscopic (TEM) image (along line A-B in Fig. 2-4) for one of the fabricated devices in which the selective plasma etching is performed for 6 sec. One can see that the NW channel thickness (or the width of NW between the two gate dielectrics) is around 18 nm and is nearly rectangular in shape. Transfer curves for this device are given in Fig. 2-7 where it is obvious that the DG mode demonstrates much enhanced performance over the other two SG modes in terms of lower V_{TH}, higher ON current (I_{ON}), and steeper SS owing to its stronger electrostatic gate controllability over channels. It is also worth noting that SG-1 mode exhibits much lower I_{ON} and degraded SS as compared with SG-2 mode, indicating that the proposed device is an asymmetric type double-gated field-effect transistor. This can be attributed to the larger S/D resistance under SG-1 mode as the conduction proceeds mainly at the inner channel interface of the NWs, which is consistent with the output characteristics in Fig. 2-8. To make it more clear, a cross-sectional view along the overlap region between the S/D and gates (line C-D in Fig. 2-4) is plotted in Fig. 2-9. During SG-1 mode of operation, the conduction electrons must transport across the offset (i.e., ungated) regions between the S/D and the inner channel, resulting in larger S/D series resistance [2-22]. Meanwhile, these ungated regions also serve as additional barriers that carriers have to overcome before inversion can occur, which translates to degraded SS. It is thus expected that under DG mode of operation, the current conduction is predominantly governed by the outer channels controlled by the 2nd gate. This statement will be more vividly demonstrated in the following sub-section where size dependency is examined. And for the purpose of fluctuation inspection, devices with different number of NW channels fabricated using a multi-finger layout [2-16] are characterized as shown in Fig. 2-10, which suggests that our NW TFT indeed possesses excellent uniformity from the nearly identical SS and V_{TH} for all the measured devices.

G_M characteristics under various modes are shown in Fig. 2-11. On account of more rapid shift of channel potential under DG operation, higher G_M is obtained as compared with two SG modes. Output curves in Fig. 2-8 reveal that DG mode provides the highest current drive among the three modes, which is reasonable considering that the conduction width is the largest in DG operation; thus, to have a more fair comparison, the drain current ratio defined as the drain current under DG mode divided by the sum of that under SG-1 and SG-2 modes is plotted against the drain voltage in Fig. 2-12. It can be observed that DG operation effectively offers additional current improvement since the resultant DG current is larger than two SG modes combined. In addition, it is interesting to note that the maximum ratio increases with decreasing magnitude of the gate overdrive, whose root cause will be discussed in Chapter 2.3.2. Thus, it can be inferred from the aforementioned information that for this double-gated NW device, there is a strong interaction between the two gates leading to much improved performance. As a matter of fact, recently our group has found that the origin of output current enhancement giving rise to the result in Fig. 2-12 can be analytically modeled by taking into account the body effect [2-23]. By inserting an additional term caused by the body effect into the formula of the drain current as a function of the gate/drain voltage under SG modes, the saturation voltage V_{Dsat} of two SG modes becomes smaller than that of DG mode for a given gate overdrive owing to the fact that there is no body effect under DG mode. Thus, the output current reaches saturation earlier under SG modes and the drain voltage at which the ratio saturates in Fig. 2-12 coincides with the V_{Dsat} under DG mode. Besides the early saturation phenomenon, it was shown that the larger-than-unity drain current ratio in the linear regime is also contributed by mobility enhancement under DG mode. One plausible mechanism leading to such mobility and G_M improvement in DG mode is volume inversion [2-24]. As opposed to the surface inversion in SG modes where carriers tend to be concentrated near the oxide/Si interface, under volume inversion in DG mode the charge centroid for a symmetric DG MOSFET would be located near the middle of the channel and the surface-scattering-limited mobility is increased as a result. The improved mobility then brings about the gain in current drive and G_M. However, double-gated SOI devices with ultra-thin body (less than 10 nm) are usually mandatory for volume inversion to assume a significant role [2-25]. Considering that the thickness of the NW characterized is still well above this value, the possibility of volume inversion can be ruled out and a detailed investigation of its origin will be given in the next sub-section.

2.3.2 Dependency of Performance Enhancement in Double-Gated over Single-Gated Operation on Nanowire Channel Dimension

To probe the impact of NW dimension, Figs. 2-13 (a) and (b) illustrate transfer curves for devices with 43- and 52-nm-thick NW channels, respectively. Evidently, for the 43-nm case, the enhancement from DG mode is still visible but the extent is smaller than that of the previous 18-nm one. On the other hand, when NW is widened to 52-nm, it comes as a surprise because no observable merit is obtained under multiple-gated operation since I_D-V_G characteristics for DG and SG-2 mode are essentially identical. Before further in-depth investigation of the root cause for this size-dependent effect, additional information can be gained from other aspects.

First, G_M enhancement is examined. Similar to the drain current ratio, G_M ratio can be defined as the G_M (with respect to gate overdrive) under DG mode divided by the sum of that under SG-1 and SG-2 modes. As shown in Fig. 2-14, the peak of G_M ratio is observed to be larger when NW size is smaller. For the device with 52-nm NW, the maximum ratio is only slightly larger than unity, implying that even under DG operation, the 1st and 2nd gates still control the channel in a rather independent way and the NW channel is only partially depleted in this case. On the contrary, the maximum ratio for 18-nm NW is seen to reach 2.4. From another viewpoint in terms of parasitic resistance, the total resistance is extracted in Fig. 2-15. S/D series resistance can thereby be determined based on the method in [2-26], in which a first order exponential curve fitting was adopted. Actually, under DG mode, the two conduction paths governed by 1st and 2nd gates can be conceived as flowing in parallel. Thus, for the simplest condition when two gates work independently, the S/D series resistance of DG mode (R_{DG}) should be approximately equal to the equivalent resistance (R_{EQ}) of two single-gated modes. To obtain R_{EQ}, the drain current as a function of the gate voltage under SG-1 and SG-2 modes is first summed up followed by employing the fitting method in [2-26] to determine R_{EQ}. The extraction procedures (only the 18-nm NW case) are shown in Fig. 2-15 and the results for devices with three different NW thicknesses displayed in Fig. 2-16 (a). The smaller S/D series resistance under DG mode as compared with SG modes can be partly ascribed to the larger conduction area between channels and S/D provided by DG mode, which helps reduce the spreading resistance. The ratio of the difference between R_{EQ} and R_{DG} to R_{EQ} is given in Fig. 2-16 (b). For DG mode of operation, it can be seen that the 18-nm, 43-nm, and 52-nm NW give 45 %, 35 %, and 17 % reduction in terms of S/D resistance improvement, respectively. It is noteworthy that the technique utilized here cannot provide very accurate determination of the S/D resistance under SG modes because the approach in [2-26] was based on a tie-gated device without the need to consider the body effect. This is apparently not the case in our device where the drain current under SG modes is intimately related to the applied bias of the auxiliary gate. However, even when normalization of the V_{TH} is undertaken as shown in the output curves in Fig. 2-12, DG mode is still able to offer larger output current than SG-1 and SG-2 modes combined, and therefore it justifies the methodology used in Fig. 2-15 though the data presented is only a rough estimate.

As another indicator of gate controllability, the extracted SS as a function of NW thickness is plotted in Fig. 2-17 where SS is observed to decrease with reduced NW thickness for all three modes. The above size dependency, in fact, has been treated in both fully-depleted double-gated SOI [2-27][2-28] and poly-Si devices [2-29]. For single-crystalline devices, more rapid variation of surface potential triggered by the larger vertical electric field induced in devices with smaller NW thickness leads to better short channel effects immunity as the NW dimension is reduced. However, in poly-Si based devices, potential barriers present in the grain boundaries are another major factor that needs to be accounted for so as to correctly interpret our results. This subject was recently treated in [2-23] where the origin of performance enhancement of a double-gated poly-Si NW transistor was investigated. And it was found that the major reason for the performance improvement under DG mode over SG modes stemmed from the different modulation capability of grain boundary barrier heights. To this end, using the similar analysis technique, the barrier height of grain boundary as a function of the gate voltage for three operation modes is shown in Fig. 2-18. Based on [2-30], the barrier height is extracted by using transfer curves measured at two different temperatures. Thanks to the increase of inversion carriers, the barrier height is monotonically made smaller with increasing V_G- V_{TH}. At strong inversion, the barrier of DG mode is the lowest among the three modes, demonstrating the merit of multiple-gated configuration in providing improved mobility and I_{ON} over SG modes. Another insight can be gained from the comparison of barrier height reduction capability under DG mode as a function of NW thickness, as shown in Fig. 2-19. The respective barrier height at V_G- V_{TH} of 3 V for 18-nm, 43-nm, and 52-nm NW is 12 mV, 30 mV, and 76 mV. It is obvious that there exists a very strong size dependency in terms of the barrier height reduction rate. The rate at which the barrier is lowered determines how fast the drain current is increased as the gate voltage is enlarged, which in turn defines SS. For the thinnest device, the gate-to-gate coupling effect is the most intense so that under DG mode the barrier can be very effectively lowered by the gate voltage, as evidenced in Fig. 2-19. As for the thickest case, there is very weak gate coupling effect and Fig. 2-18 (c) exhibits that even under DG mode the barrier height is still reduced in a similar rate as that of SG-2 mode. Hence, it becomes reasonable that the SS is reduced with thinner NW under DG mode.

Now that the detailed origin for the performance enhancement is clarified, the trend in Fig. 2-12 that shows reduced peak ratio with increased gate overdrive can be easily understood. As explained in the previous sub-section, the larger-than-unity drain current ratio is associated with the early saturation effect that occurs exclusively in SG modes, which only suffices to explain the reason that the peak ratio saturates beyond the drain voltage equal to the corresponding gate overdrive. Another prominent factor leading to the difference in output current of DG and SG modes should be their respective mobility values, which are an exponential function of the barrier height [2-30]. It is obvious from Fig. 2-18 (a) that the discrepancy of the barrier height between DG and SG modes gets smaller as the gate overdrive is increased; in other words, for a given drain voltage, the drain current ratio is expected to behave as a monotonically decreasing function of the gate overdrive, in agreement with Fig. 2-12. With regard to the constant peak current ratio irrespective of the gate overdrive observed in [2-23], it may have to do with the different shape of the NW channel between this work and [2-23] resulting in distinct distribution profile of carriers and barrier lowering rates among DG and SG modes. Further investigation is required to validate this point.

The proposed configuration with two independent gate electrodes also increases the flexibility in device operation. Taking advantage of additional freedom from the auxiliary gate, V_{TH} can be adjusted by tuning the applied bias of the auxiliary gate. This is illustrated in Figs. 2-20 (a) and (b) where the bias of the auxiliary gate varies from -3 V to 3 V in 0.5 V step for SG-1 and SG-2 modes, respectively. As can be seen, due to the tiny volume of NW, V_{TH} is efficiently shifted along with different auxiliary gate bias whereas SS shows weak dependence. Similar behavior has been reported in double-gated SOI devices and was attributed to the channel potential modulation by the auxiliary gate [2-31]. Shown in Fig. 2-21 is the V_{TH} as a function of the auxiliary gate voltage extracted from Fig. 2-20. Within the range of applied auxiliary bias from -3 V to 3 V, the V_{TH} of the device can be shifted from 4.2 V to -0.52 V and 6.1 V to -2.2 V when the 1st and 2nd gates assume the auxiliary gate, respectively. This is a direct consequence of better channel controllability of the 2nd gate than the 1st gate. With tunable V_{TH}, this kind of device has strong potential for low standby power circuits. For instance, in standby circuit operation, lower I_{OFF} can be obtained by raising the V_{TH} of the device.

And in active mode, the V_{TH} can be adjusted into a moderate value for providing sufficient drive current.

It is worth noting that in Fig. 2-20 the characterized device is with 18-nm NW. For the other two thicker cases in Figs. 2-22 (a) and (b), when adopting the same scheme, the shift rate of V_{TH} is much reduced and it is the I_{OFF} that is mainly altered by the auxiliary gate, which in turn modulates V_{TH}. This is so because when two gates are independent of each other, applying an auxiliary gate bias only determines the surface condition on its side; hence, as the bias of the auxiliary gate is increased, the surface also starts from being depleted to inversion and when to the point of strong inversion, which means that the surface on the auxiliary gate side is already conducting, the I_{OFF} as seen by the driving gate rises dramatically. A more quantitative treatment of this subject can be found in [2-18].

2.4 Summary

To sum up, a novel poly-Si TFT with rectangular NW channels is proposed and characterized. The main process feature is the clever use of plasma for the formation of cavities on two sides of a nitride/poly/nitride stack by selective etching of poly, which is then followed by refilling with an active layer. This scheme is highly beneficial for the dimensional control and alignment of NWs. Plus, the procedure is low cost since the critical dimension is only determined by the etching duration rather than the resolution of exposure apparatus.

To demonstrate the feasibility and optimize the condition of a selective plasma etching process, critical parameters in an HDP tool is first adjusted. Addition of SF_6 gas into Cl_2 is found to greatly increase the isotropic etching profile of poly-Si. And within 10 sec, the isotropic etching depth can be controlled to be below 38 nm, rendering this approach very suitable for the fabrication of deca-nanometer NW devices.

Base on this method, a poly-Si NW TFT with independent double-gated configuration was fabricated and characterized. Because of the inherent asymmetry of device structure, the electrical characteristics of SG-1 mode are inferior to those of SG-2 mode. As compared to two SG modes, significant performance enhancement under DG mode is obtained in terms of larger I_{ON} and G_M, steeper SS, reduced series resistance, and lower V_{TH}. Nonetheless, this phenomenon is observed to have a strong size dependency, with the degree of enhancement diminished for thicker NW devices. To probe the origin of this size-dependent behavior, the barrier height of the grain boundary is extracted by conducting I-V measurements at different temperature ambience. Under DG mode, the barrier height is shown to be lowered with a faster rate than the other two SG modes as the gate voltage is increased, demonstrating the merit of double gates in achieving better control of the channel. Yet for the thickest NW (52 nm) case, there is only marginal difference between the barrier height of SG-2 and DG modes. Hence, to truly obtain the advantages of double-gated configuration, it is preferable to have a device with NWs as thin as possible (quantum confinement is not considered here).

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Table 2-I Definition of operation modes in I-V characterization.

gate mode	1st gate	2nd gate
SG-1 mode	Driving gate	Auxiliary gate
SG-2 mode	Auxiliary gate	Driving gate
DG mode	Driving gate	Driving gate

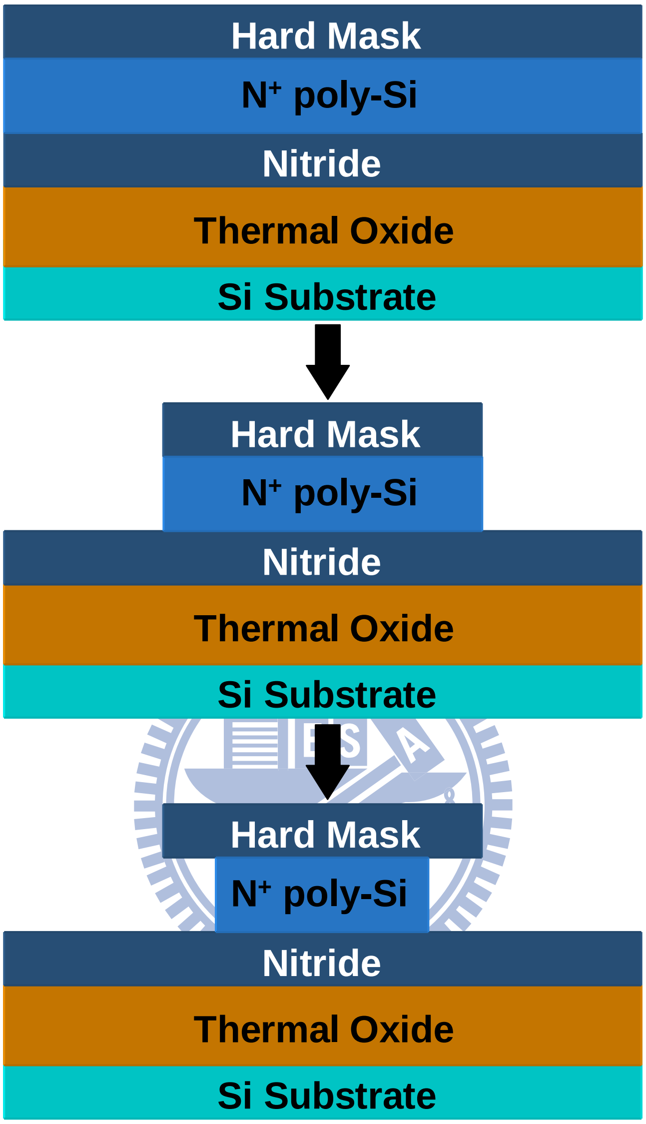


Fig. 2-1 Test structure used for investigating selective plasma-etching conditions.

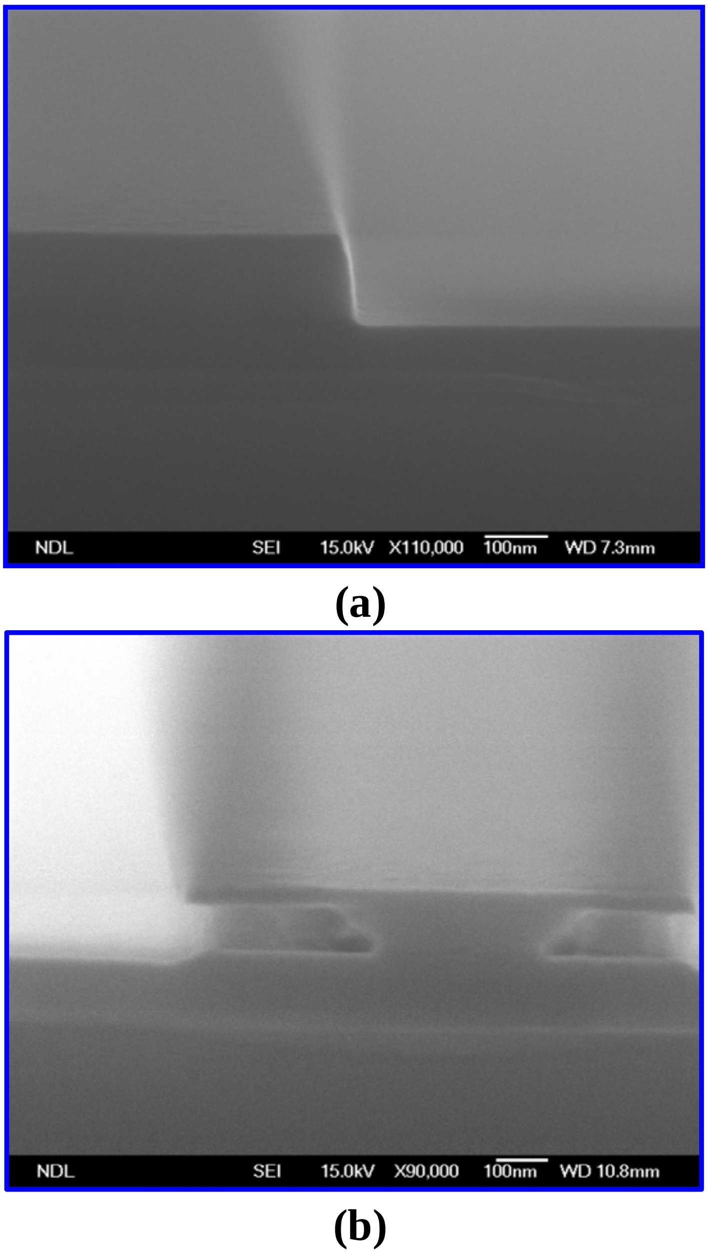
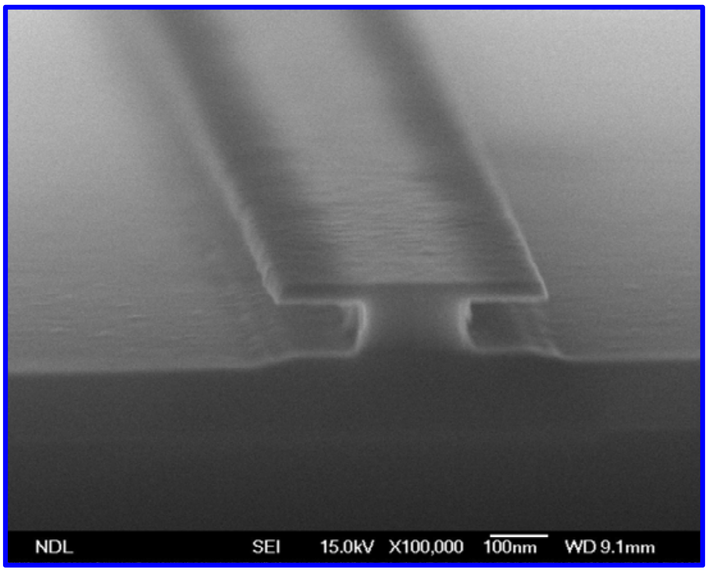
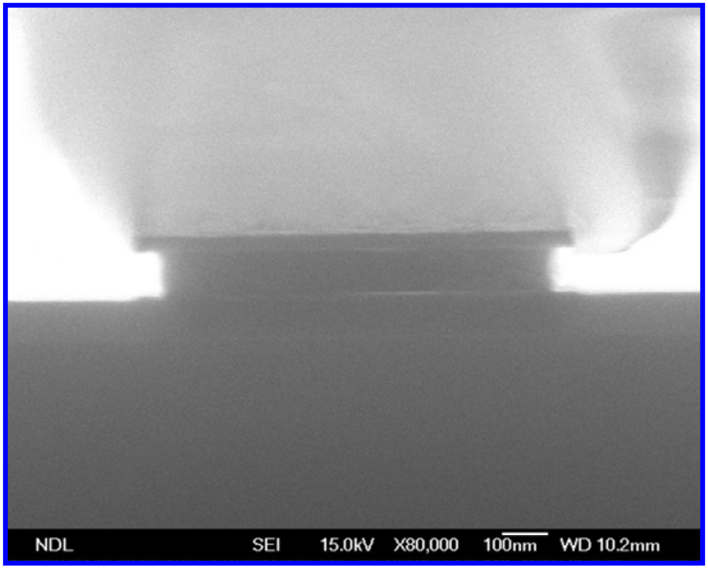


Fig. 2-2 Cross-sectional SEM images after plasma etching with different conditions. (a) The gate stack is anisotropically etched with the condition of P = 12 mtorr, Cl_2 = 35 sccm, HBr = 125 sccm, top power = 310 W, bottom power = 120 W, time = 31 sec. (b) In the aftermath of (a) step, the wafer is further subject to another etching step with the condition of P = 5 mtorr, SF_6 = 20 sccm, top power = 700 W, time = 30 sec. (Continued)



(c)



(d)

Fig. 2-2 Cross-sectional SEM images after plasma etching with different conditions. In the aftermath of (a) step, the wafer is further subject to (c) P = 5 mtorr, Cl_2 = 100 sccm, SF_6 = 20 sccm, top power = 700 W, time = 20 sec, and (d) P = 5 mtorr, Cl_2 = 100 sccm, SF_6 = 20 sccm, top power = 700 W, time = 6 sec. Isotropic etching component is seen to be enhanced by the addition of SF_6 gas.

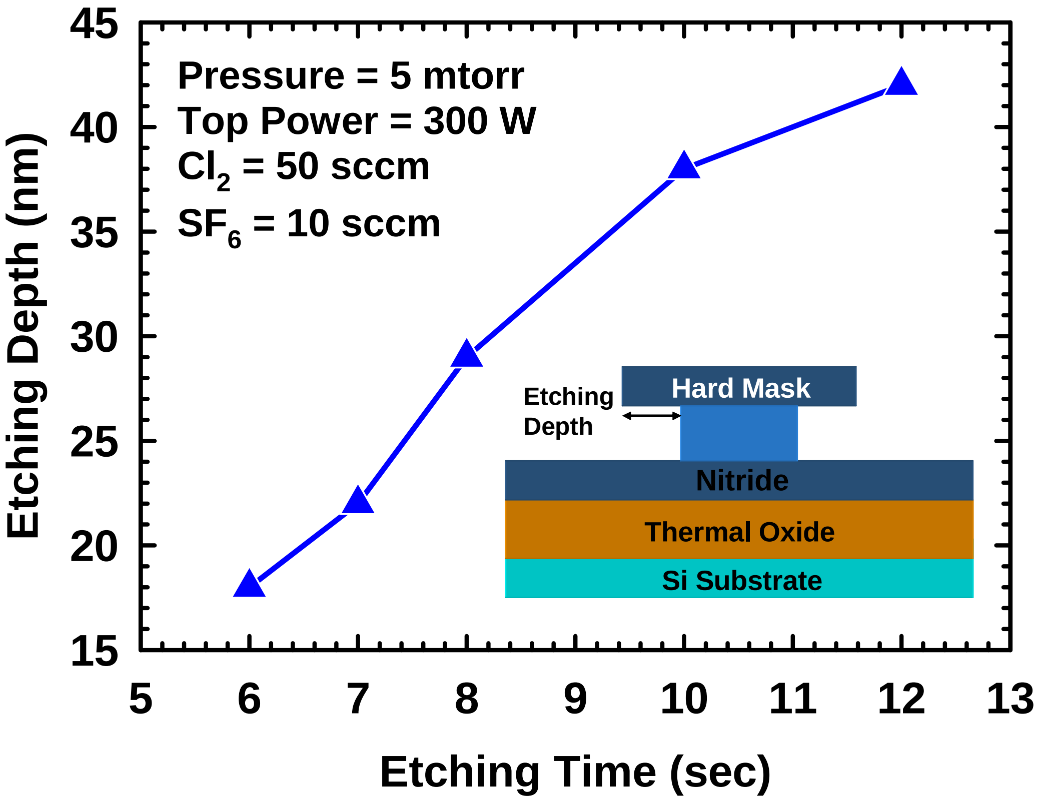


Fig. 2-3 Measured lateral etching depth as a function of etching time. The inset gives the definition of lateral etching depth.

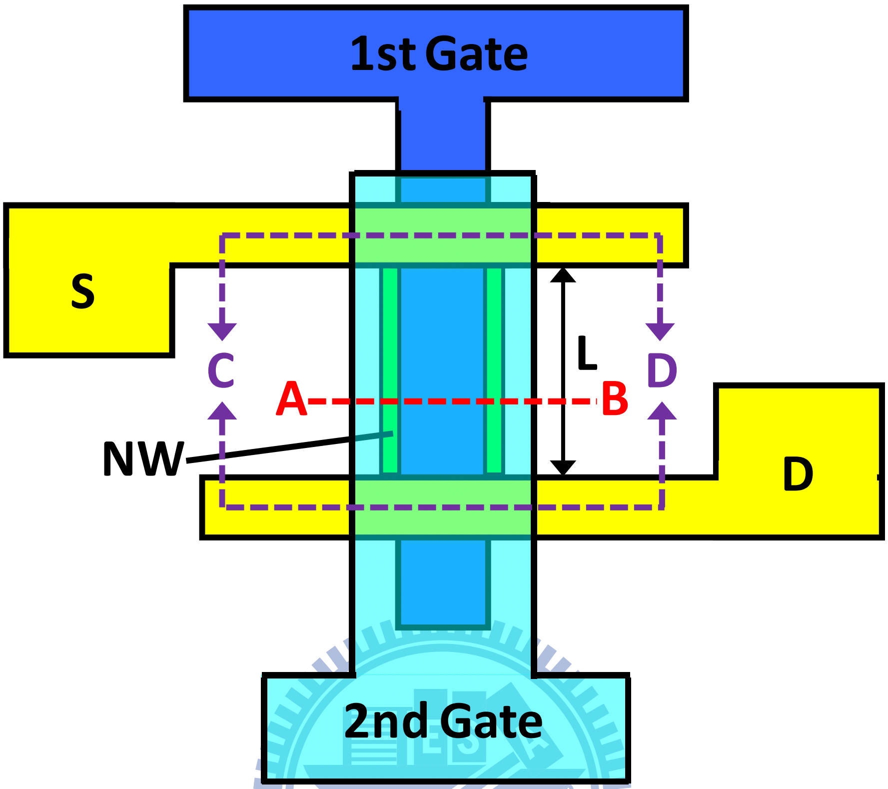


Fig. 2-4 Top-view layout of the proposed poly-Si NW device with two independent gates.

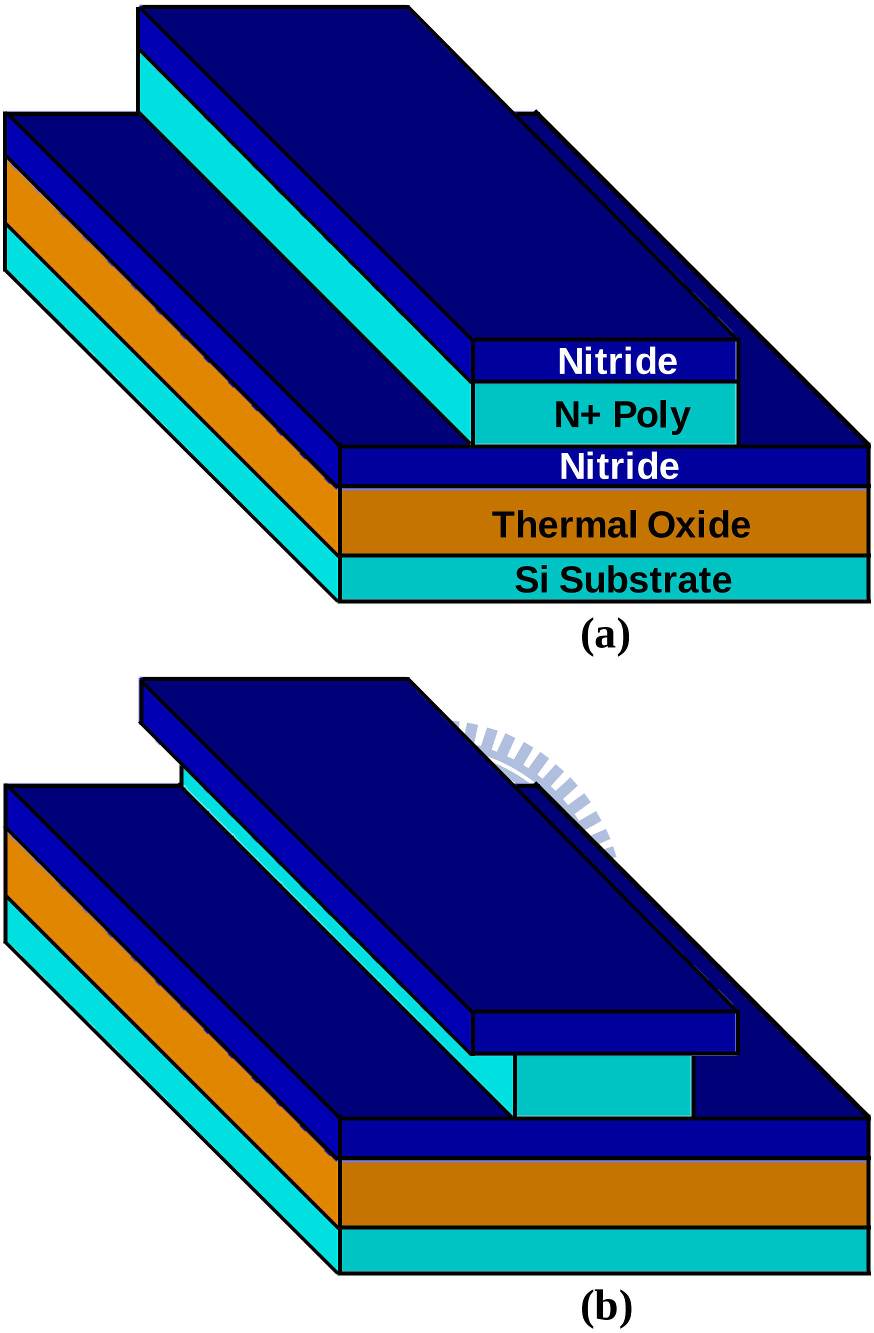


Fig. 2-5 Schematic process flow for the double-gated poly-Si NW TFT (viewed along line A-B in Fig. 2-4). (a) Sequential deposition of 100-nm thermal oxide, 50-nm nitride, 100-nm *in situ* doped N+ poly-Si, and 50-nm nitride on a 6-in Si wafer. First gate patterning was then performed. (b) Selective plasma etching of the first gate. (Continued)

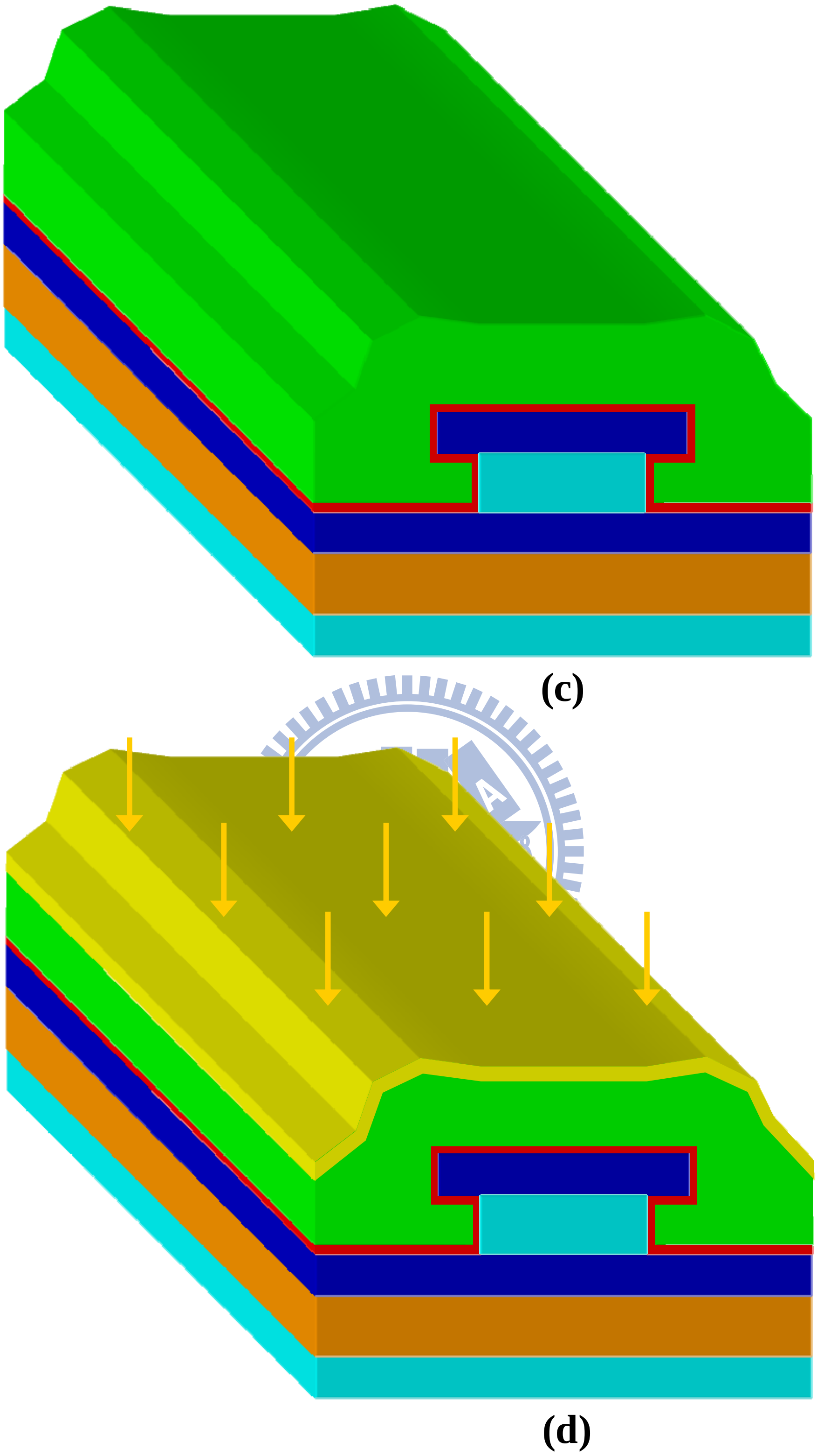


Fig. 2-5 (c) First gate dielectric (20-nm TEOS oxide) and 100-nm amorphous-Si layer deposition followed by SPC. (d) S/D implantation by phosphorous with 15 keV energy and 5×10^{15} cm^{-2} dosage. (Continued)

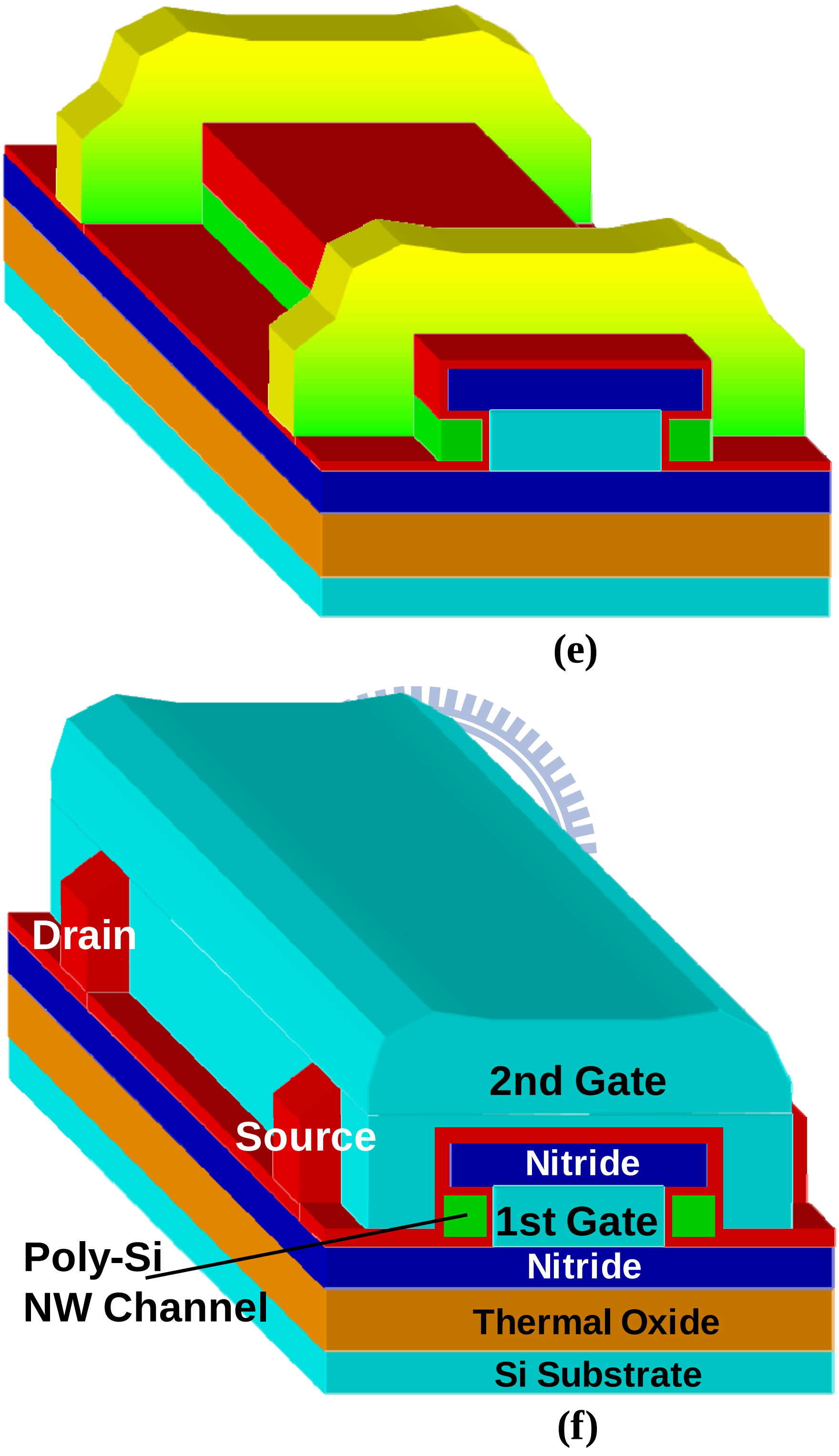


Fig. 2-5 (e) Simultaneous definition of NW channels and S/D regions using dry etching. (f) Second gate stack (20-nm TEOS oxide and 100-nm *in situ* doped N+ poly-Si) deposition and patterning.

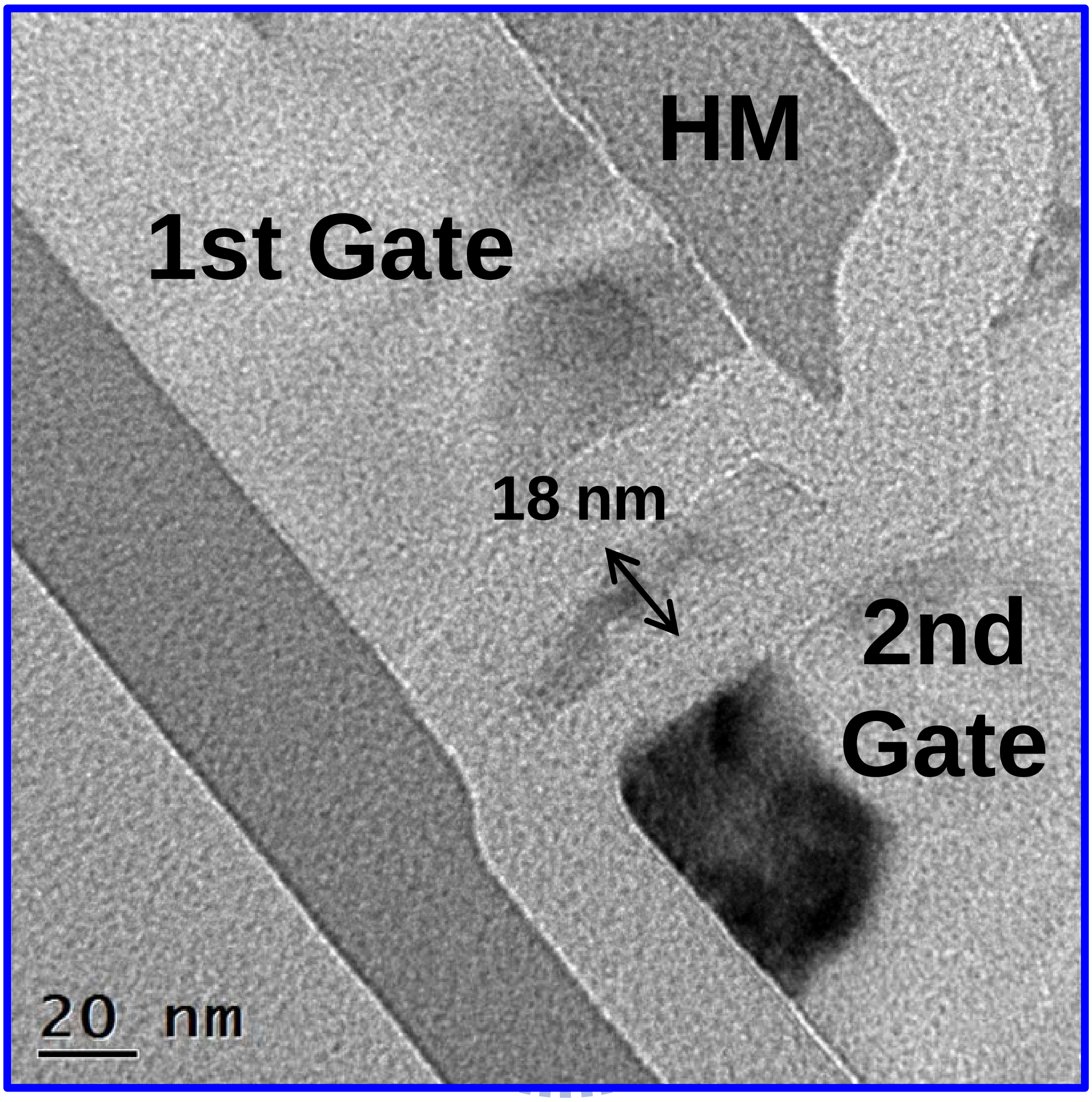


Fig. 2-6 Cross-sectional TEM image (along line A-B in Fig. 2-4) of an independent double-gated poly-Si NW TFT showing 18-nm NW thickness.

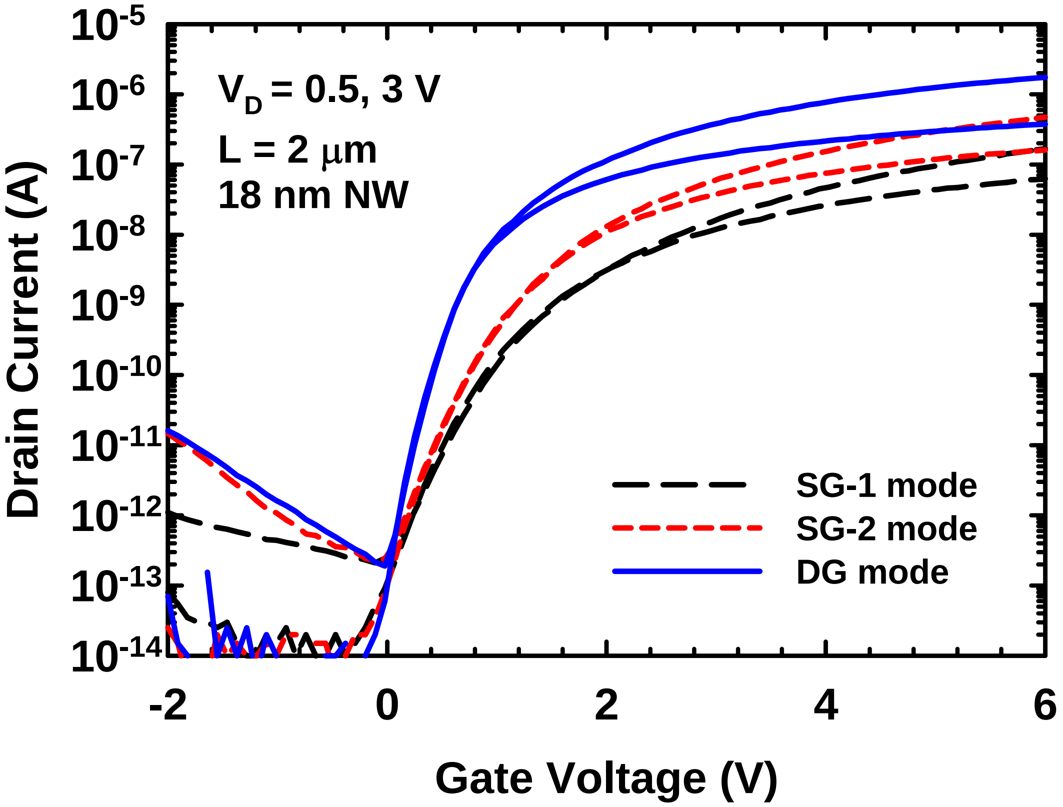


Fig. 2-7 Transfer characteristics of a fabricated device with 18-nm NW thickness.

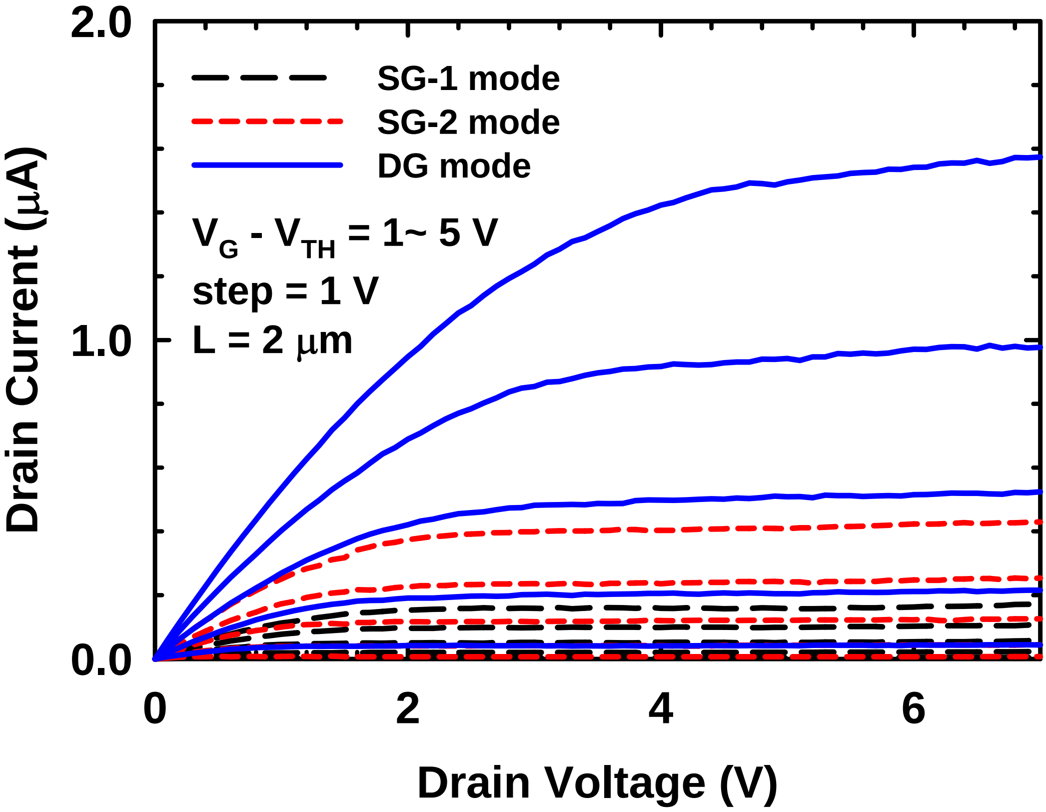


Fig. 2-8 Output characteristics of a fabricated device with 18-nm NW thickness.

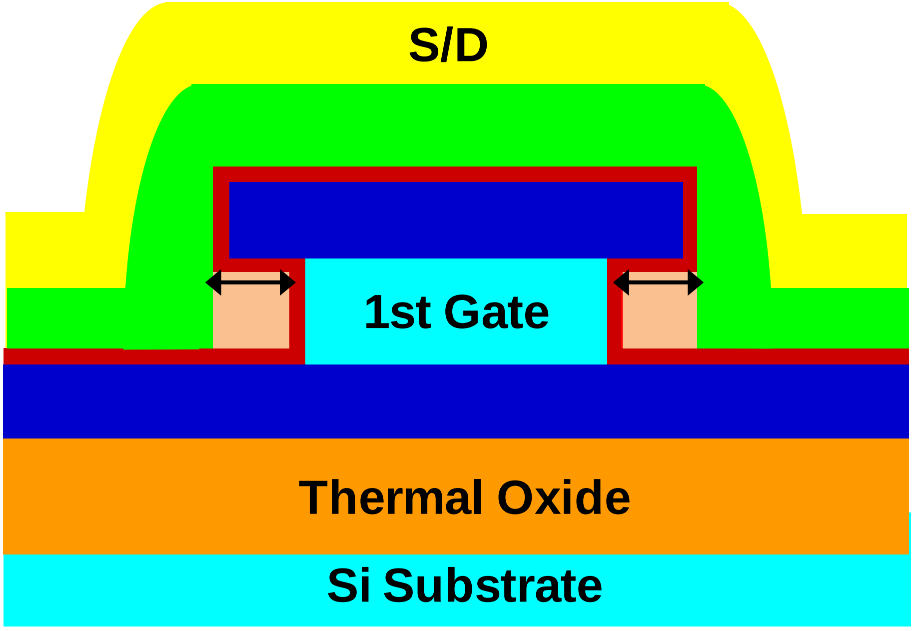


Fig. 2-9 Cross-sectional view of the device along the C-D lines shown in Fig. 2-4. The double-headed arrows indicate that there exist un-gated regions between the inner conduction channel (gated by the first gate) and S/D.

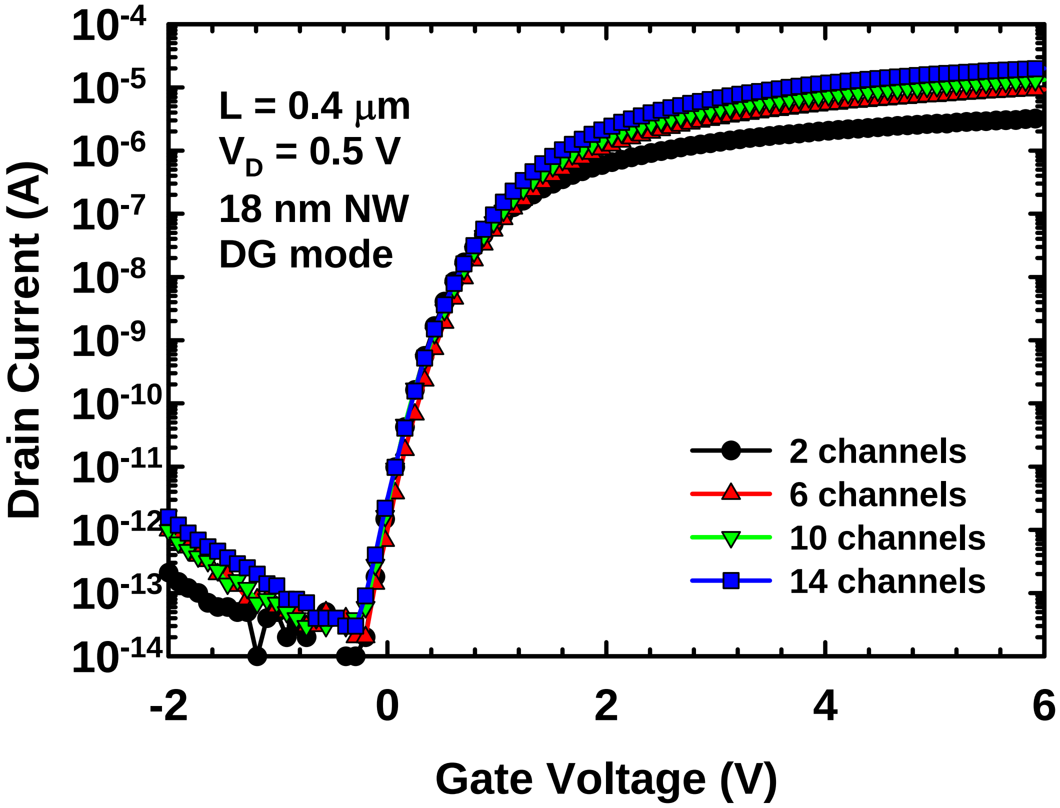


Fig. 2-10 Transfer characteristics for devices with various numbers of NW channels. It is seen that the V_{TH} and SS are independent of the number of NW channels, suggesting good uniformity among the measured devices.

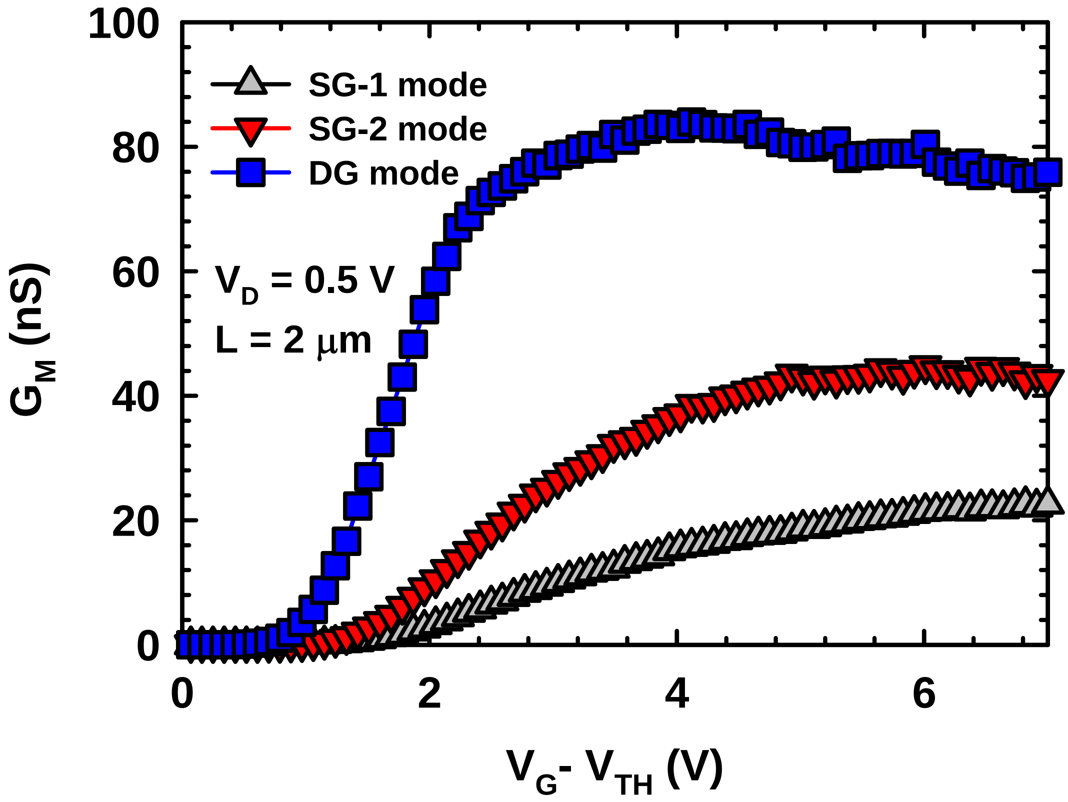


Fig. 2-11 G_M characteristics for a device with 18-nm NW extracted from Fig. 2-7. Higher G_M can be obtained in DG mode over the other two SG modes.

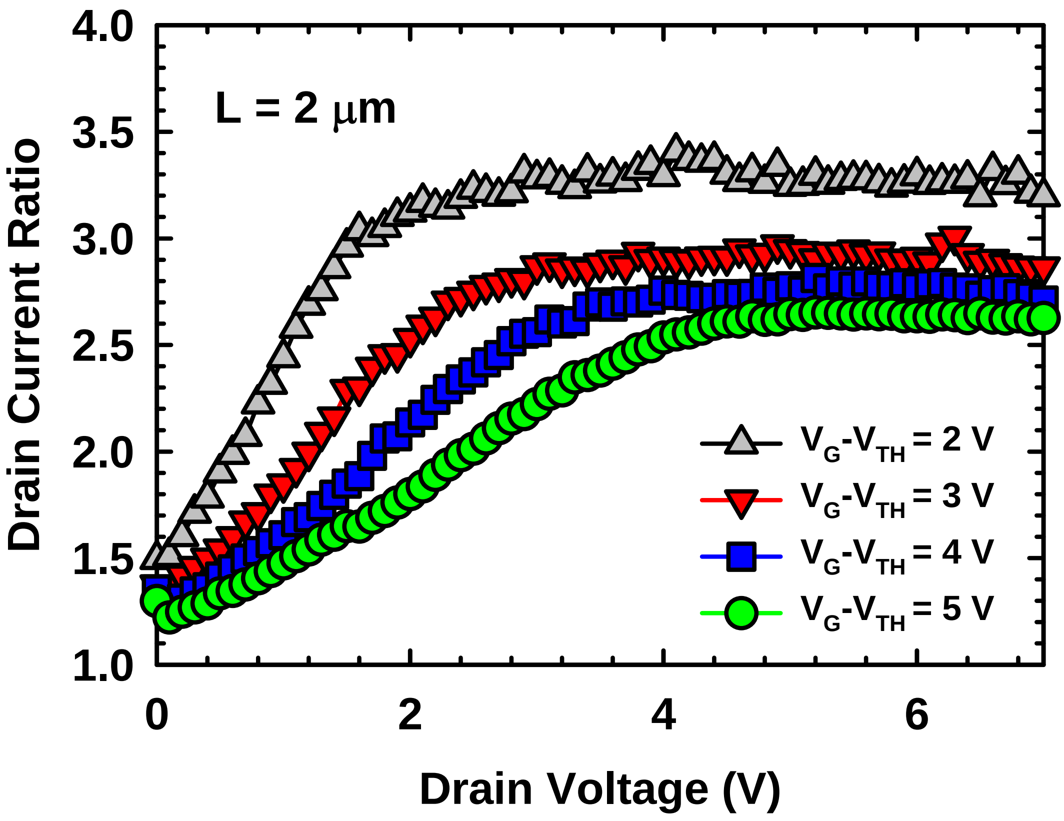


Fig. 2-12 Drain current ratio vs. drain voltage with gate overdrive as a parameter for a device with 18-nm NW extracted from Fig. 2-8. For all the measured drain voltage range, the output current under DG mode is larger than the other two SG modes combined. The drain voltage at which the ratio saturates increases with increasing gate overdrive, which is ascribed to the “early saturation effect” in SG modes [2-23].

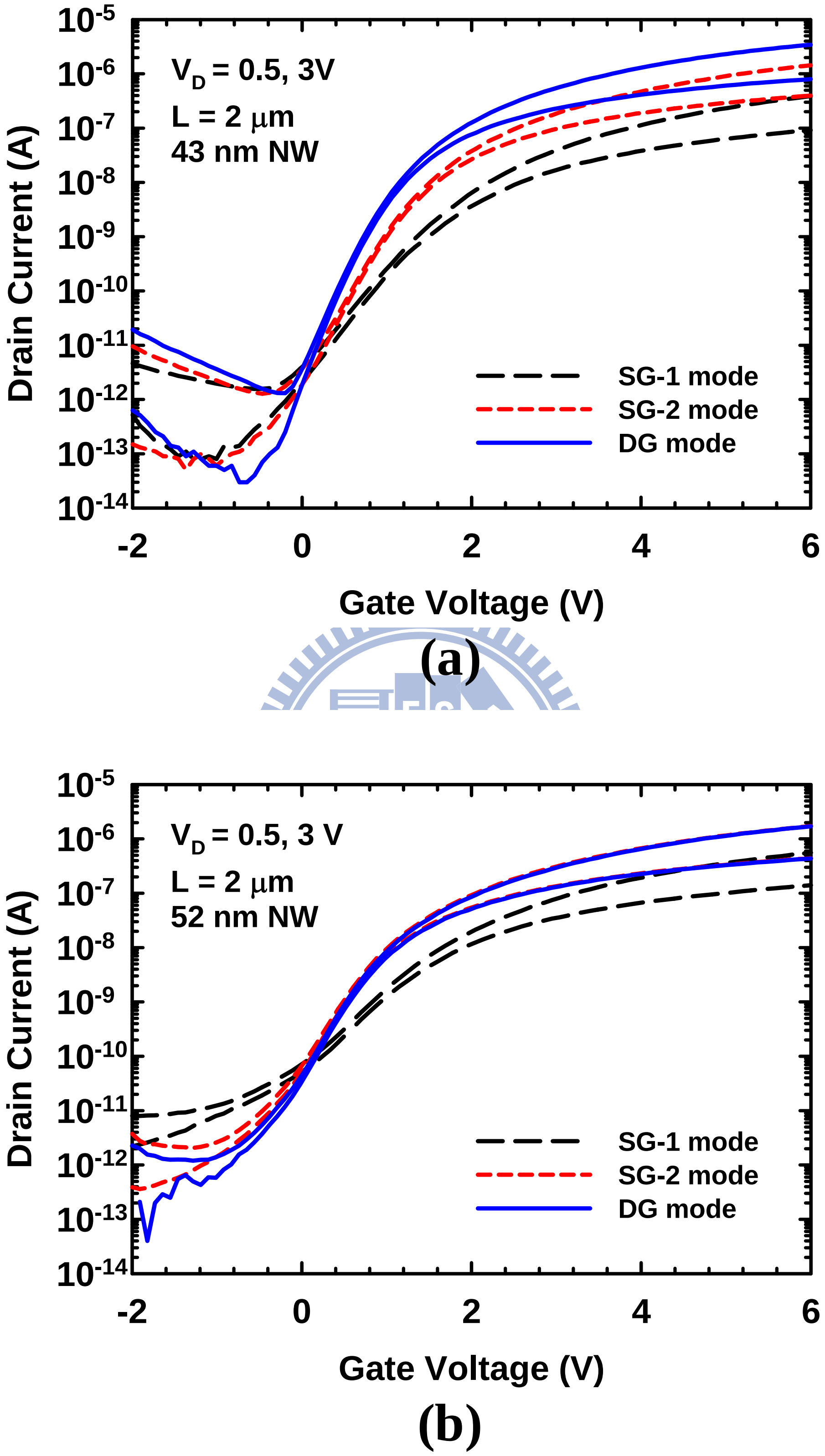


Fig. 2-13 Transfer curves for devices with (a) 43- and (b) 52-nm-thick NW channels.

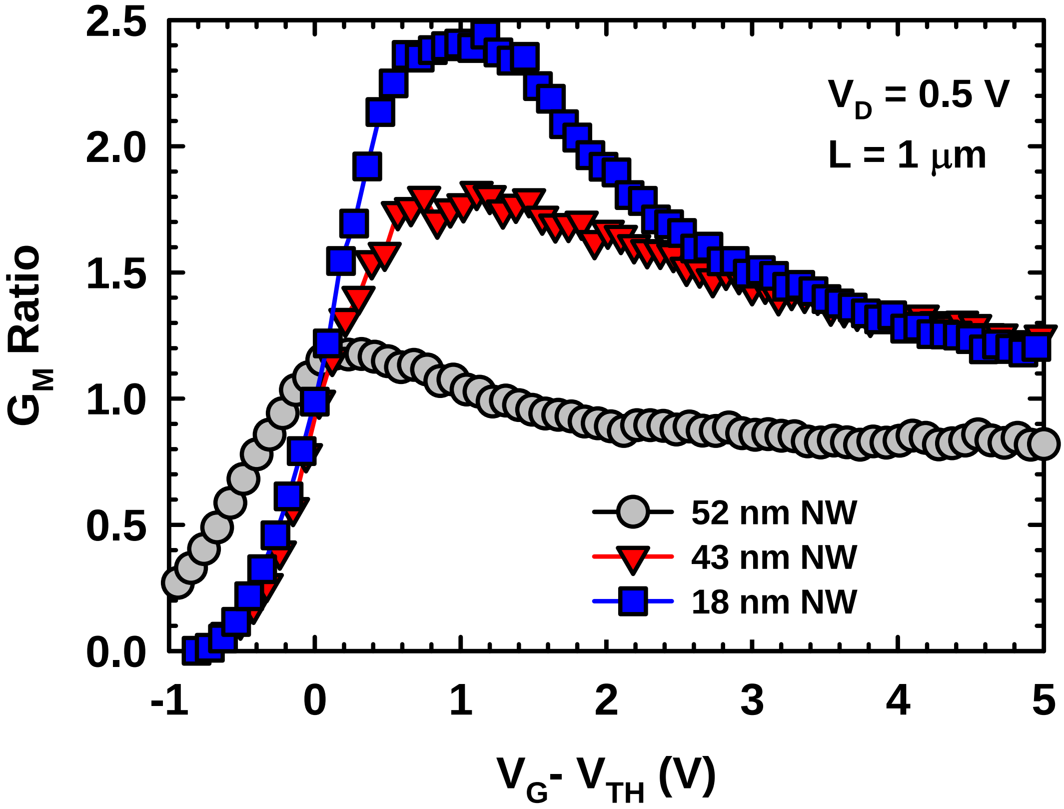


Fig. 2-14 Comparison of G_M ratio characteristics among devices with three different NW thicknesses. The peak of ratio is 2.4, 1.8, and 1.2 for a device with 18-, 43-, and 52-nm-thick NW channels, respectively.

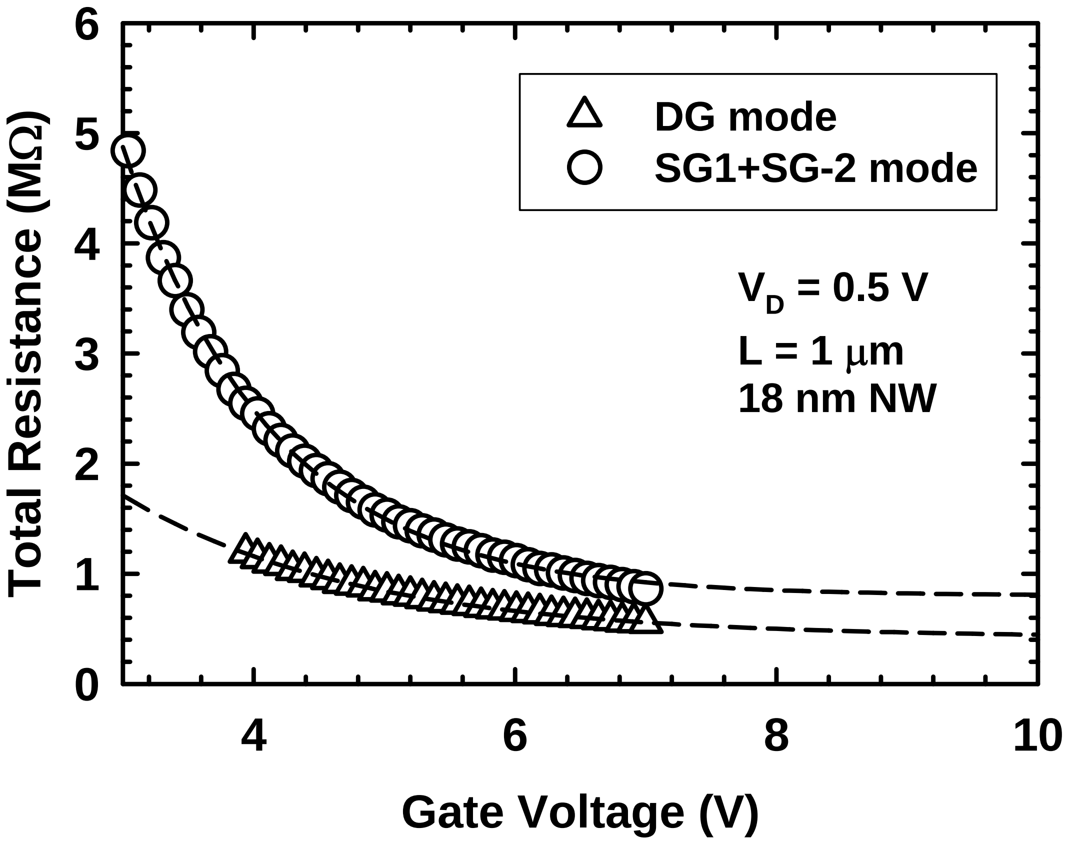
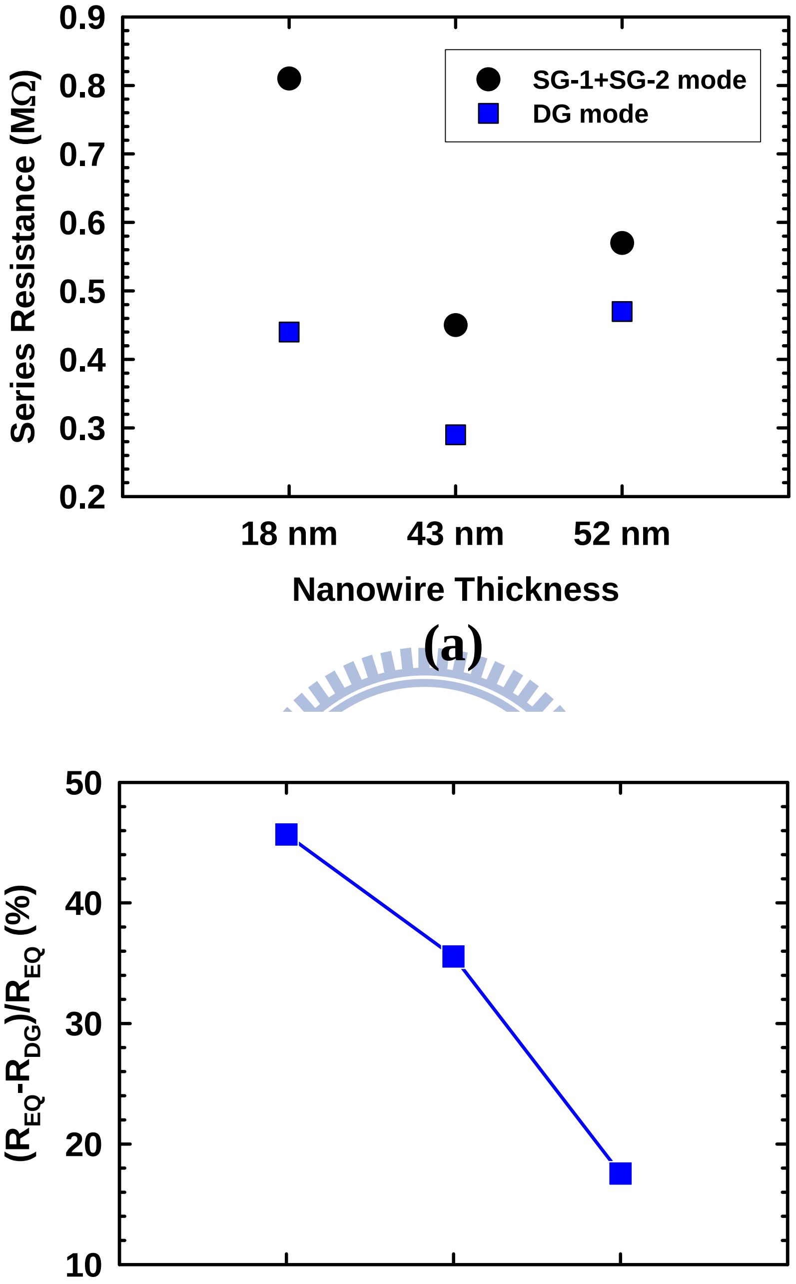


Fig. 2-15 Extracted total resistance as a function of the gate voltage under DG and SG-1+SG-2 modes.



(a)

(b)

Fig. 2-16 (a) Series resistance under SG and DG modes extracted by the procedure in Fig. 2-15. (b) Percentagewise series resistance reduction under DG mode in comparison with SG modes as a function of NW thickness.

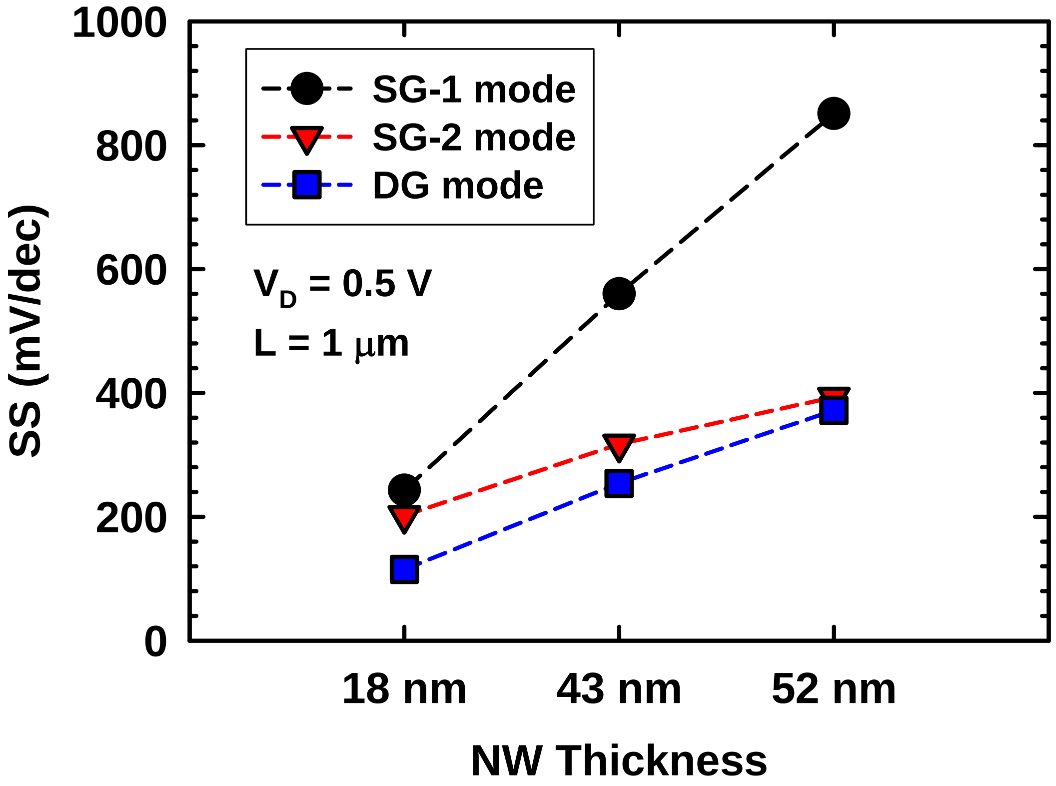


Fig. 2-17 SS under three operation modes as a function of NW thickness. For all three modes, SS is observed to decrease with reduced NW thickness.

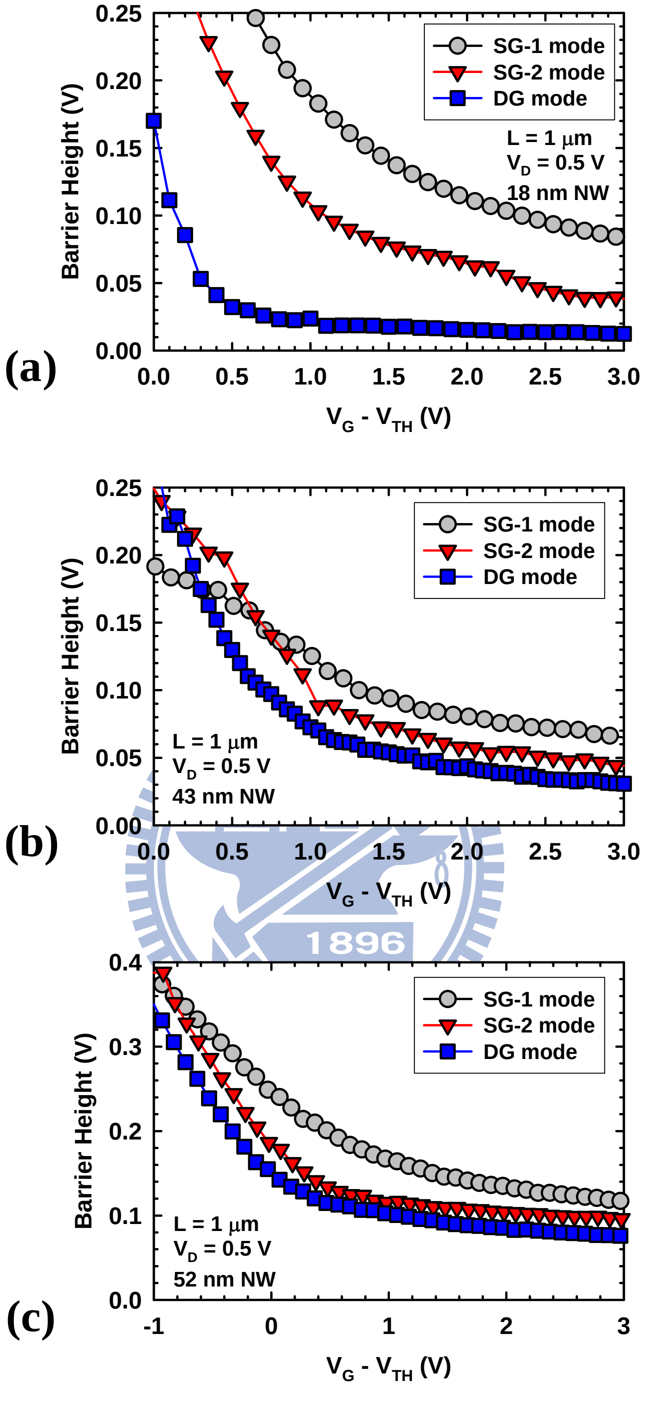


Fig. 2-18 Extracted barrier height under SG and DG modes as a function of the gate overdrive for devices with (a) 18-nm, (b) 43-nm, and (c) 52-nm NW channels.

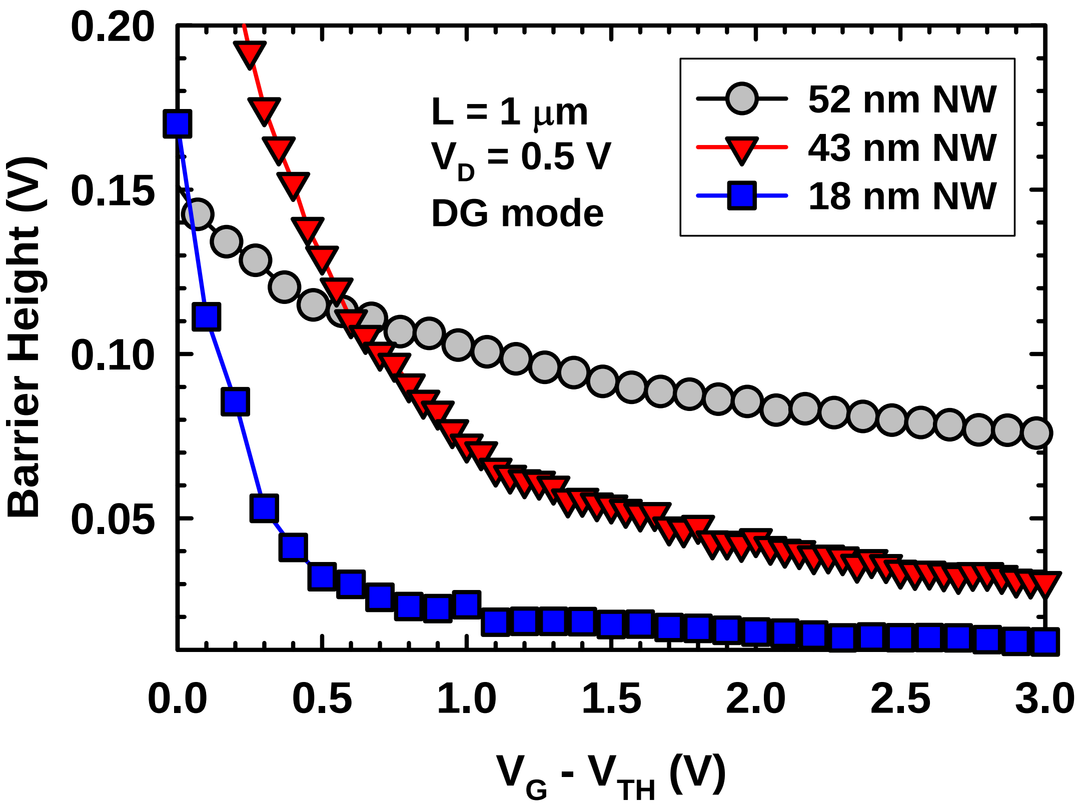
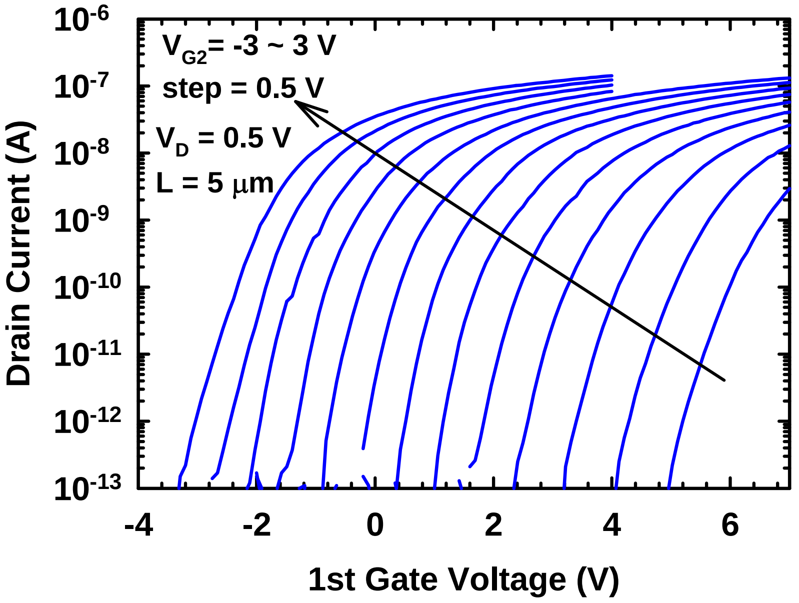
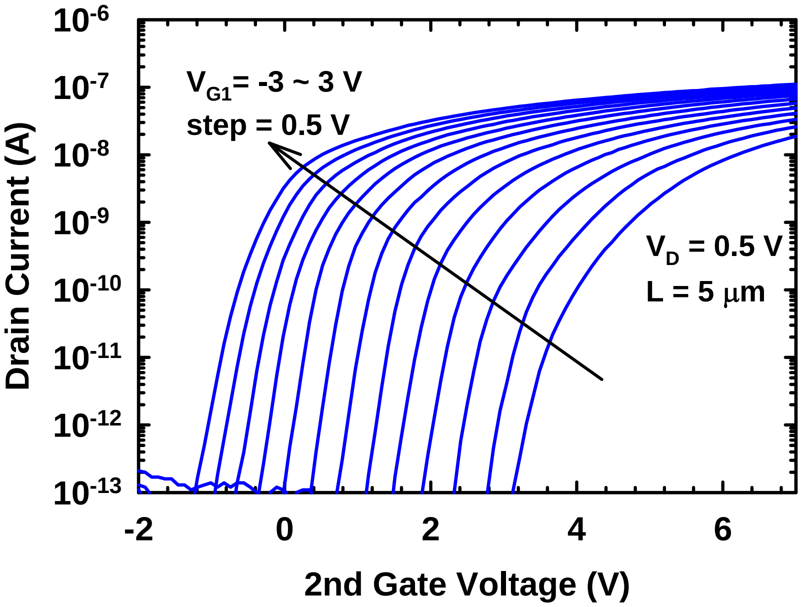


Fig. 2-19 Comparisons of size-dependent barrier height reduction capabilities under DG mode. The lowering rate is larger as the size of NW is thinner.



(a)



(b)

Fig. 2-20 Transfer characteristics of an 18-nm NW device with varying AG bias under (a) SG-1 and (b) SG-2 modes. AG bias ranges from -3 V to 3 V in step of 0.5 V. V_{TH} is seen to be effectively adjusted by different AG bias.

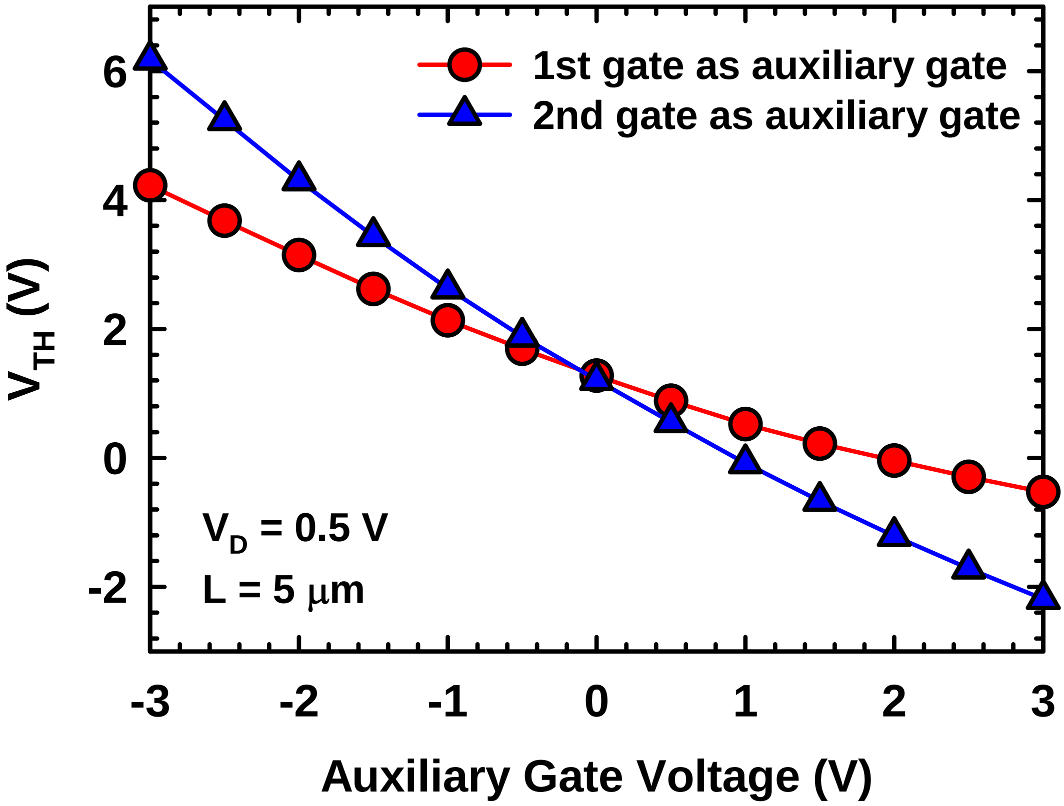
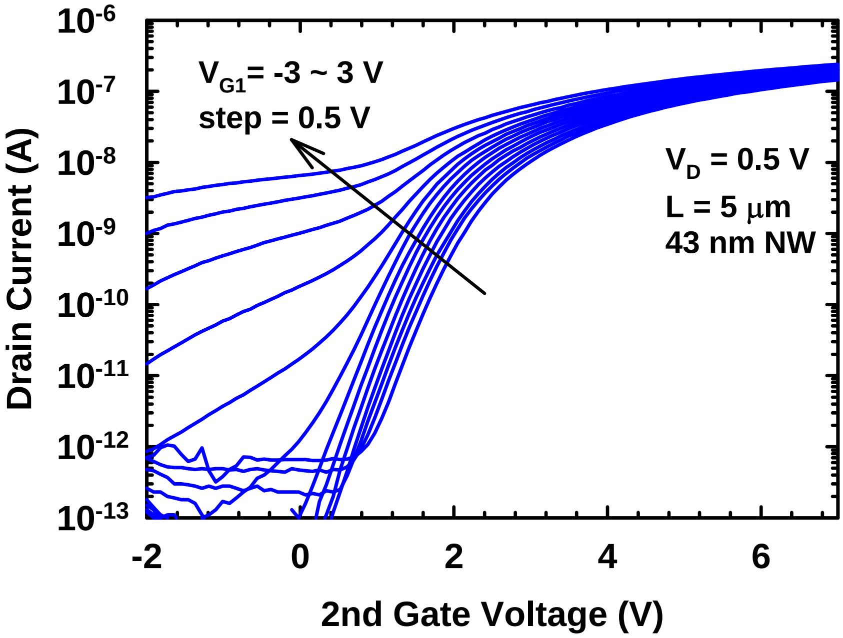
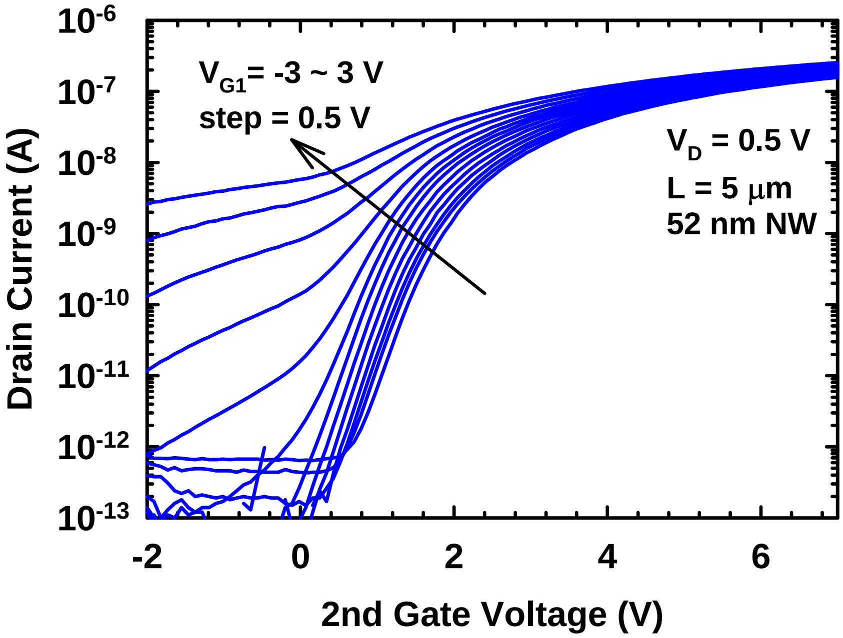


Fig. 2-21 Dependency of V_{TH} as a function of applied AG voltage when the 1st gate or 2nd gate assumes AG extracted from Fig. 20. The higher V_{TH} sensitivity to the 2nd gate voltage is a result of its stronger controllability over NW channels.



(a)



(b)

Fig. 2-22 Transfer characteristics of NW devices with NW thickness of (a) 43-nm and (b) 52-nm NW device with varying AG bias under SG-2 mode. In comparison with Fig. 2-20, the extent of V_{TH} distribution with respect to AG bias is much reduced.

Chapter 3

Analysis of *In Situ* Doped Source/Drain for Performance Improvement of Double-Gated Poly-Si Nanowire Thin Film Transistors

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3.1 Introduction

Although NW structures are becoming increasingly relevant in electronics, there must still be a link between these 1-D systems and the 3-D outside world. The delicate interface between source/drain (S/D) and NW channels then requires dedicated manipulation and understanding so as not to degrade the promising potential that NWs have to offer. In an effort to mitigate short channel effects, shallow S/D extension junction depth is required, which comes at the sacrifice of high series resistance though. To simultaneously engineer junctions with both shallow depth and low resistivity is such a daunting task that series resistance is being increasingly forecasted as one of the major showstoppers for CMOS scaling. A thorough and in-depth study of this subject can be found in [3-1] [3-2]. This issue is likely to be further aggravated in NW thanks to its inherently thin stripe feature.

Typically, to prevent S/D resistance that arises due to the narrow and thin active region of NWs from dominating the drive current, silicide [3-3] or raised S/D [3-4] have been widely adopted to help ameliorate this issue in the top-down approach while metallic S/D by liftoff [3-5] is commonly used in the bottom-up procedure, all of which lead to a semiconductor/metal contact. The Schottky barrier in the interface thus formed, whose magnitude depends on the work functions of both semiconductor and metal, impacts profoundly the carrier injection from the source into the channel. At a best scenario, the barrier height is low and the barrier width is narrow such that the contact can be treated as ohmic without exerting significantly detrimental effects on device performance. Generally speaking, there are two kinds of conduction mechanisms in the case of a Schottky contact: thermal emission over the barrier and tunneling through the barrier. Common belief is that tunneling makes only little contribution at room temperature for conventional metal/semiconductor contacts if the doping of semiconductor is low and thermal emission assumes the major role [3-6]. However, carbon nanotube, another promising 1-D structure, has been reported to operate based on tunneling alone [3-7]. As proposed in [3-8], the distinction between thermal emission and tunneling is blurred since tunneling is sometimes also a thermally-activated process depending on the material chosen. Making use of this feature with a Si NW device that has aluminum S/D, Q. Li *et al* observed sub-60 mV/dec subthreshold slope (SS) at room temperature operation on account of the enhanced tunneling current induced by gate-modulated Schottky barrier thinning [3-9]. Hence, important as it is in concentrating on the channel itself to boost the performance, the merit of S/D engineering should not be neglected and is worth more efforts and understanding to reveal its full possibilities instead of simply assuming S/D as reservoirs of carriers. To this end, as opposed to ion implantation, this chapter will investigate how another S/D doping technique, *i.e.*, *in situ* doping, helps enhance the overall characteristics of the proposed device.

As described in the fabrication process in Chapter 2, S/D regions were formed by a low energy ion implantation so that dopants were situated near the top surface to avoid compromising the gate controllability caused by inadvertent channel doping. Though this method attains good gate control over NW channels, it still inevitably leads to slight channel doping by the tail part of dopant distribution, and is achieved at the expense of S/D resistance as only a small portion of S/D is heavily doped. Besides, as reported in one of our previous studies [3-10], the major leakage current is identified to be the gate-induced-drain-leakage current (GIDL) that originated from the gate/drain overlap area in the structure. And since the portion of the drain that is most close to the gate is only moderately doped, this makes band-to-band tunneling (BTBT), the origin of GIDL, much easier to occur and results in severe leakage current, as can be apparently observed in Fig. 2-7. To alleviate this problem, here we propose a modified method to fabricate devices with an identical structure except the S/D regions are more uniformly and heavily doped by employing an *in situ* doping approach. In this way, the S/D resistance and gate controllability are not compromised any more, leading to a win-win situation

3.2 Fabrication Process for Devices with *In Situ* Doped Source/Drain

In this chapter, two types of devices with different S/D formation techniques are compared. For the implanted S/D type, detailed device fabrication process has been elaborated in Section 2.2.2 and illustrated in Fig. 2-5. The gradual variation of colors in the S/D regions shown in Fig. 2-5 (e) highlights that the doping concentration is not uniform and decreases from the topmost surface toward channel regions. Figure 3-1 schematically illustrates the modified process for which S/D is formed by using *in situ* doping technique. The process flow from Fig. 3-1 (a) to Fig. 3-1 (c) is identical to that shown in Fig. 2-5 down to the SPC step. Afterwards, without any photolithographic process, a spacer-like portion of poly-Si along the sidewall of the 1st gate, whose purpose will later be discussed, was created by carrying out a dry etching step with end-point detection (Fig. 3-1 (d)). Subsequently, *in situ* phosphorus doped poly-Si was deposited by LPCVD at 550 °C and 600 mtorr using 200 sccm PH_3 and 1 slm SiH_4 ((Fig. 3-1 (e))) followed by S/D region patterning (Fig. 3-1 (f)). In this way, since there was no implantation involved and NW channels underneath the hardmask were protected by the spacer-shaped poly-Si from being exposed to PH_3 during the *in situ* doped poly-Si deposition step, the entire S/D regions were doped heavily while the NWs remained unscathed (*i.e.*, undoped). The 2nd gate stack was then deposited and patterned to complete the device (Fig. 3-1 (g)). Dopant activation was fulfilled using the thermal budget of processing steps after dopant introduction, including the deposition of the 2nd gate stack (20-nm LPCVD TEOS oxide and 100-nm *in situ* doped N^+ poly-Si) and 350-nm passivation LPCVD TEOS oxide, approximately amounting to 700 ^{o}C annealing for 8 hours. To avoid possible dopant diffusion into NWs, we intentionally left a spacer-like poly-Si in Fig. 3-1 (d) instead of directly forming rectangular NWs as in Fig. 2-5 (e) so that even if diffusion occurred, this spacer-like portion, which was part of S/D actually, was doped first before channel doping happened. Also, channel doping should not be of significance as the highest temperature of the subsequent thermal budget was merely 700 ^{o}C in TEOS oxide deposition step. Control samples with implanted S/D were prepared as well for comparison.

3.3 Comparison of Electrical Characteristics between Devices with Implanted and *In Situ* Doped Source/Drain

Figure 3-2 depicts a TEM picture of a fabricated device from which the thickness of NW is observed to be 22 nm. Transfer characteristics for the control device with implanted S/D are shown in Fig. 3-3. Channel length and gate oxide thickness are 1 μm and 20 nm, respectively. It has been stated in Chapter 2 that additional non-gated routes would have significantly increased the series resistance of SG-1 mode. However, the nearly symmetric transfer curves between SG-1 and SG-2 modes indicate that this detrimental effect related to the NW thickness is dramatically reduced. Figure 3-4 shows the transfer characteristics of the device with *in situ* doped S/D having structural parameters nominally identical to the device characterized in Fig. 3-3. The on/off current ratio of DG mode at V_D = 2 V is over 10^7, an order of magnitude higher than that for the device with implanted S/D. Furthermore, SS is enhanced from 89 mV/dec to 73 mV/dec under DG mode when *in situ* doping technique is adopted. It should be noted that, to the best of our knowledge, this is the best value ever reported for a poly-Si based device. To prove that the above characteristics are indeed representative of the whole picture, we have conducted fluctuation analysis in Fig. 3-5 by showing transfer curves of 20 devices with similar characteristics collected from a total of 29 and 26 devices for implanted and *in situ* doped types, respectively, amounting to 69 % and 77 % chip yield. Those not shown have either larger-than-100 mV/dec SS or simply are not functional. As can be seen in the figure, the variation is not severe and this suggests the good uniformity offered by the selective plasma etching technique. The mean value and standard deviation of V_{TH} at $V_D = 0.5$ V for *in situ* doped and implanted devices are 0.33 V, 35 mV and 0.31 V, 46 mV, respectively. SS distribution with respect to the channel length is shown in Fig. 3-6 for *in situ* doped devices. Under DG operation, excellent immunity to short-channel effect is observed and the characterized devices demonstrate tight distribution.

Major device characteristics of both types of devices shown in Figs. 3-3 and 3-4 are summarized in Table 3-I. The difference in V_{TH} between the two devices is small and within the measured fluctuation value. Aside from this, all the other device characteristics of the *in situ* doped type are superior to those of the implanted type. For the SS improvement, *in situ* doping avoids unintentional channel doping by ion implantation. Meanwhile, more uniform and highly activated doping concentration gives rise to larger on/off current ratio due to smaller series resistance and reduced BTBT probability. This statement is further evidenced in the output characteristics shown in Fig. 3-7. At V_G - V_{TH} = V_D = 5 V, the saturation current improvement over the implanted control device under DG mode is 48 %. For SG-1 and SG-2 modes, under the same bias condition, the improvement is 107 % and 5.4 %, respectively. The large disparity between the extent of improvement for two SG modes is related to their different current paths from the source to the drain. If S/D is formed by ion implantation, carriers under SG-1 mode must transport across a long distance of only moderately doped S/D before reaching the topmost portion of S/D where the resistivity is the smallest. Under SG-2 mode, since the outer channel surface controlled by the 2nd gate is closer to the most heavily doped S/D regions than the 1st gate, it is easier for carriers to reach the topmost S/D without experiencing significant series resistance. This explains why output current is dramatically improved for SG-1 mode while only slightly increased for SG-2 mode when *in situ* doping results in S/D with lower series resistance. By using the measured output curve data, the total resistance can be plotted against channel length [3-11], as shown in Fig. 3-8. It can be seen that under DG mode there is approximately 5 times reduction in series resistance from 45 kΩ to 8.1 kΩ when S/D is formed by *in situ* doping.

For statistical analysis, I_{ON} - I_{OFF} plots under DG mode for the two types of devices are shown in Fig. 3-9. I_{ON} and I_{OFF} are the drain current at $V_D = 2$ V, $V_G = 3$ V and $V_G = -2$ V, respectively. At a fixed I_{OFF} equal to 3 pA, *in situ* doping method results in 252 % I_{ON} improvement by increasing I_{ON} from 1.46 μA to 5.14 μA, suggesting the significance of S/D engineering for performance enhancement.

The reason for the drastic GIDL current reduction with the adoption of *in situ* doped S/D is now discussed. As a matter of fact, there exists no absolute relationship between the GIDL current and S/D doping concentration [3-12]. At a given gate and drain bias, too low the S/D doping concentration would lead to severe band bending at the drain/oxide interface in the region overlapped with the gate. However, the depletion width is large as well because of the low doping concentration. This increases the tunneling width so the BTBT probability is diminished. On the other hand, for the highly doped case, although the depletion width is extremely small, the band bending is also curbed, which corresponds to the *in situ* doped S/D scenario in this study. Taking these factors into account, it is straightforward to understand that moderate S/D doping concentration is the one most susceptible to GIDL and this fits the implanted S/D type device.

The GIDL current difference can be explained from another perspective in terms of the effective conduction area of leakage current in Fig. 3-10. To make it more lucid, Fig. 3-10 (a) is the schematic structure before the 2nd gate stack deposition. Figures 3-10 (b) and (c) show, respectively, the major leakage current conduction paths in the gate/drain overlap regions corresponding to the circled areas in Fig. 3-10 (a) for implanted and *in situ* doped S/D type devices. Owing to the dissimilar doping profiles, the lightly doped region (in green), where GIDL easily occurs, is much more widespread in Fig. 3-10 (b) than Fig. 3-10 (c), posing as another factor accounting for the leakage current difference. Besides, the lightly doped areas are essentially non-gated and behave as additional transport barriers, which can also explain the improvement of SS by *in situ* doping technique.

To more quantitatively analyze the leakage mechanism, the activation energy of the leakage current as a function of the gate voltage normalized to V_{TH} is extracted in Fig. 3-11 by performing the characterization of temperature-dependent transfer curves and evaluating the activation energy by the slope of Arrhenius plots. The results indicate that as compared with the nearly gate-voltage-independent activation energy for the *in situ* doped S/D type device, the activation energy of the implanted S/D counterpart gradually decreases with a more negative gate voltage owing to the occurrence of GIDL.

One point worth emphasizing is that intuitively the magnitude of activation energy for the implanted doped S/D device should have been smaller than that of *in situ* doped S/D one if BTBT is the dominant mechanism for the I_{OFF} as tunneling is supposed to have minor temperature dependence, which obviously is not the case in Fig. 3-11. This can be interpreted from two aspects. First, in addition to pure BTBT in Fig. 3-12 (a), GIDL in a more general way of definition also includes the contribution from trap-assisted tunneling, the intensity of which is related to the distribution of trap states in intra-grain regions and grain boundaries. This trap-assisted tunneling is also termed thermionic field emission because electrons must be thermally excited first from the valence band to the trap state before tunneling through the barrier into the conduction band, as illustrated in Fig. 3-12 (b). It is thus expected that the larger activation energy of implanted S/D device is caused by the greater amount of trapping centers or defects present in S/D induced by ion implantation. On the other hand, when the doping concentration of poly-Si is higher than the number of carriers that traps can deplete (*i.e.*, the grain is partially-depleted), the potential barrier height in the grain boundary is shown to be inversely proportional to the doping concentration [3-13]. Given that the average grain size of poly-Si obtained by SPC (for the implanted S/D case) and *in situ* doped poly is around 60 nm and 200 nm, respectively, as shown in Figs. 3-13 (a) and (b), respectively, and the typical trap density of SPC poly-Si is 1.27×10^{12} cm^{-2} [3-14], the critical doping concentration above which this condition is met can be estimated to be 2.1×10^{17} cm^{-3} for implanted S/D devices and 6.3×10^{16} cm^{-3} for *in situ* doped S/D ones. Here the same trap density is applied for both cases for simplicity. The implantation dosage and the flow rate of PH_3 used in this dissertation can give rise to S/D with doping concentration at least one to two orders of magnitude higher than this value, readily fulfilling the criterion. Accordingly, the temperature sensitivity of thermionic emission, which is the preponderant conduction mechanism in poly-Si, is then higher as the doping concentration is reduced, explaining the larger activation energy for the implanted S/D device. As a brief summary regarding the origin of leakage current, it can be inferred that the major reason *in situ* doping method brings about reduced leakage as compared with implantation is because it provides higher doping concentration, which impedes BTBT occurrence, and is free of implantation damage, which lowers trap-assisted tunneling current.

3.4 Summary

In this chapter, the performance enhancement of a double-gated poly-Si NW transistor with *in situ* doped S/D is investigated. Because of the elimination of ion implantation that is likely to cause excessive dopant incorporation into the channel, the *in situ* doping technique has been shown to improve SS down to 73 mV/dec, the best result ever reported for a poly-Si based device (the previous record was 79 mV/dec in [3-15]). Due to the higher dopant concentration offered by the *in situ* doping method, compared with the control device five times reduction in series resistance under DG mode is achieved and the saturation current can be enhanced up to 48 %, 107 %, and 5.4 % under DG, SG-1, and SG-2 modes, respectively. In the mean time, leakage current that results from GIDL is substantially suppressed by the reduced BTBT probability in the *in situ* doped S/D device, which is consistent with the result of activation energy of I_{OFF} that shows much stronger gate voltage dependency for the implanted S/D counterpart. The fact that the activation energy is lower when using the *in situ* doping method suggests that the trap density within the poly-Si film is reduced since there is no structural damage inflicted by implantation.

Last but not least, it should be pointed out that recently a new device structure concept called junctionless transistor has been proposed to deal with the issue associated with the sophisticated S/D profile control in ultra-short channel devices [3-16][3-17]. It is essentially a gated resistor with channel and S/D sharing the same type of dopant with high concentration (in this situation, there is no need to distinguish between channel and S/D). This kind of scheme has been shown to rival and sometimes outperform conventional MOSFETs in terms of SCEs control both theoretically and experimentally provided that the channel is thin enough for it to be fully depleted by the gate. Our group was also engaged in this field recently; however, at the time of the writing of this dissertation, our preliminary results showed that junctionless devices with the same structure as proposed in this study are very sensitive to NW thickness, in agreement with [3-18], and start to exhibit appreciable subthreshold leakage current when the channel length is below 0.7 μm (data not shown). In this respect, we believe that although junctionless transistor may be one of the options to prolong the CMOS longevity, the control of overall device geometry and structural parameters is trickier, justifying the motivation for the configuration proposed in this chapter, *i.e.*, undoped channel and heavily doped S/D.

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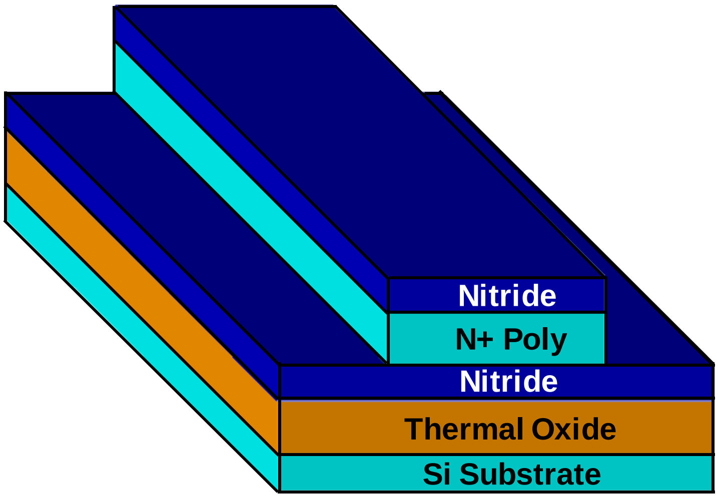
Table 3-I Summary of the major characteristics of devices with implanted (Fig. 3-3) and *in situ* doped S/D (Fig. 3-4).

	Implanted S/D			***In situ* doped S/D**		
	SG-1	**SG-2**	**DG**	**SG-1**	**SG-2**	**DG**
V_{TH} (V)	**0.51**	**0.45**	**0.29**	**0.59**	**0.56**	**0.31**
SS (mV/dec)	**184**	**171**	**89**	**153**	**149**	**73**
I_{ON} (μA)	**0.32**	**0.39**	**2.21**	**0.51**	**0.94**	**3.67**
I_{OFF} (pA)	**4.61**	**5**	**5.35**	**0.39**	**0.45**	**1.67**
DIBL (mV/V)	**26.6**	**13.3**	**12**	**18.1**	**12**	**10**

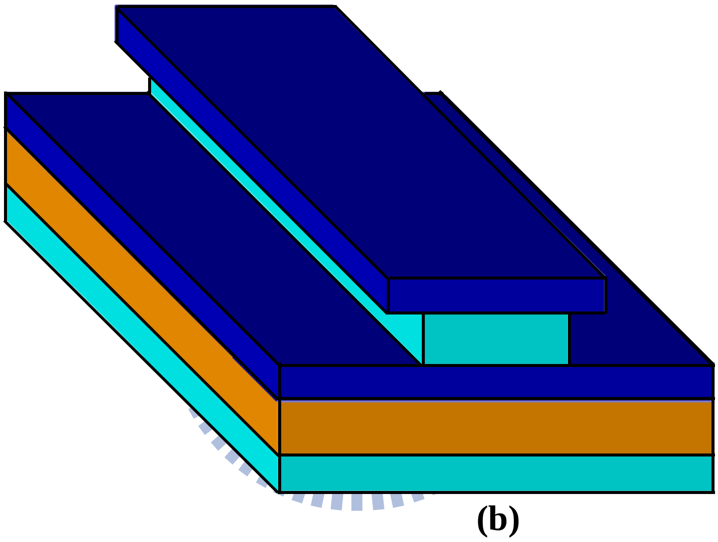
V_{TH} is equal to V_G @ I_D = 10 nA × W/L

V_{TH} and SS are extracted @ V_D = 2 V

I_{ON} and I_{OFF} are extracted @ V_G = 3 V, V_D = 2 V and V_G = -2 V, V_D = 2 V, respectively



(a)



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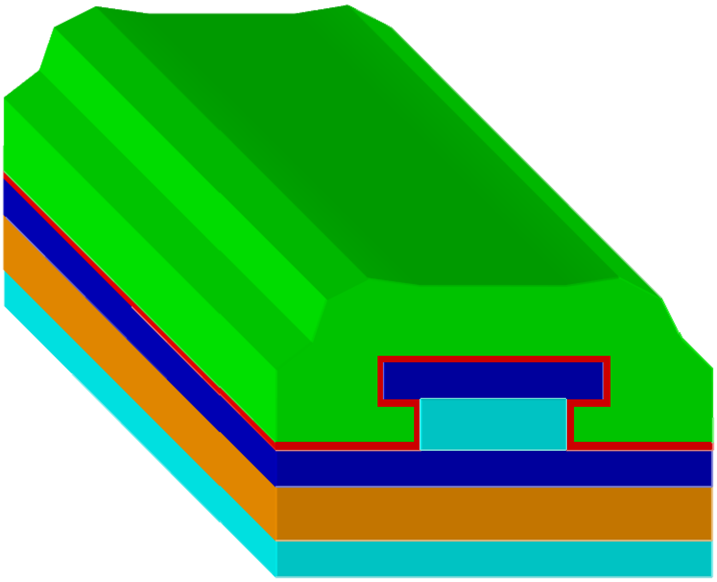
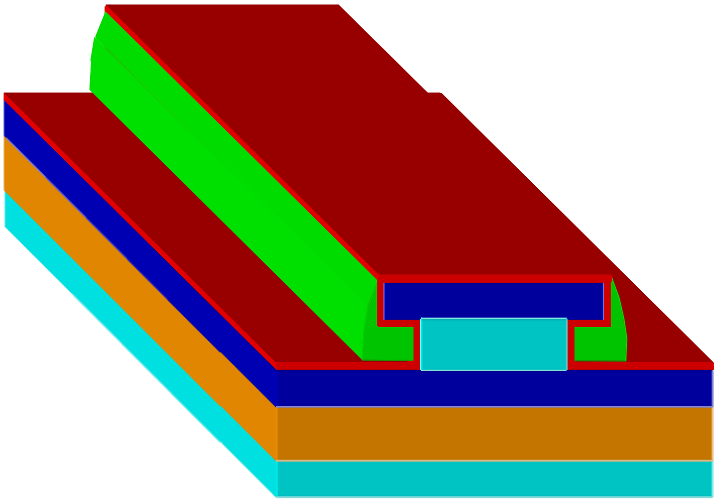
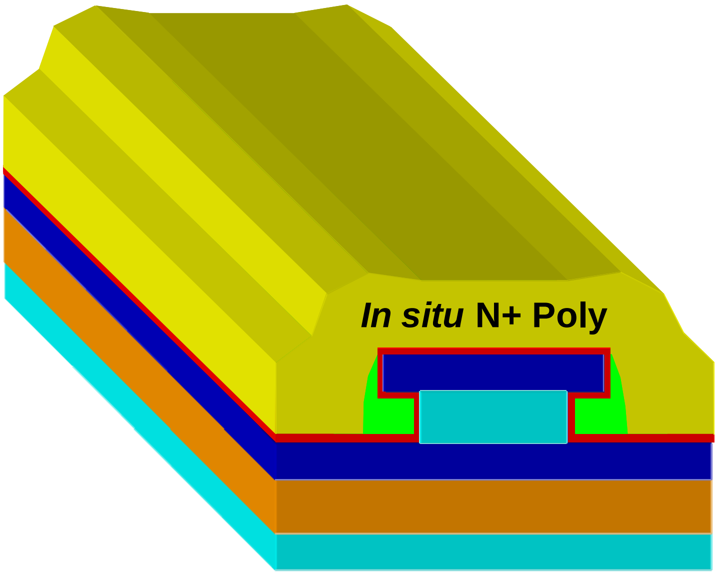


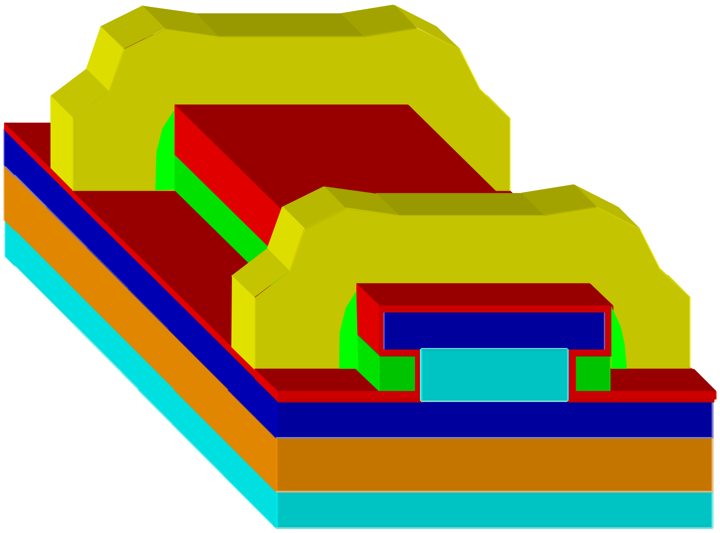
(c)



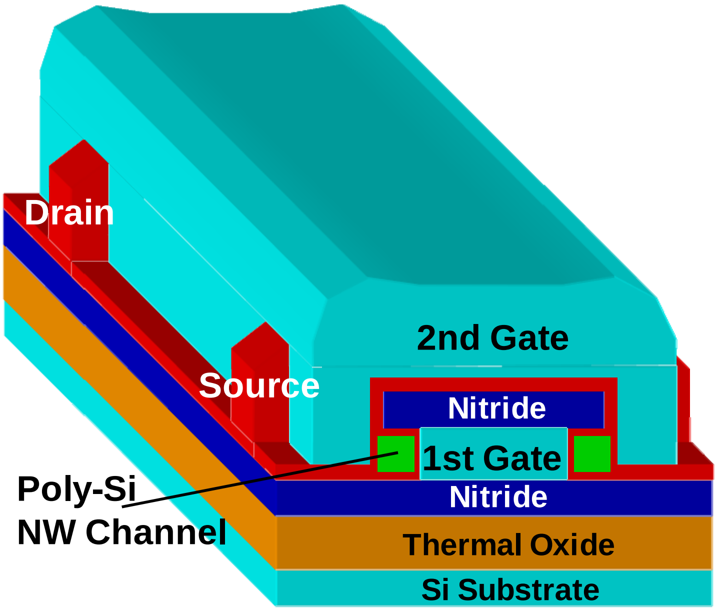
(d)



(e)



(f)



(g)

Fig. 3-1 Schematic process flow for the double-gated poly-Si NW TFT with *in situ* doped S/D. (a) Sequential deposition of 100-nm thermal oxide, 50-nm nitride, 100-nm *in situ* doped N+ poly-Si, and 50-nm nitride on a 6-in Si wafer. First gate patterning was then performed. (b) Selective plasma etching of the first gate. (c) First gate dielectric (20-nm TEOS oxide) and 100-nm amorphous-Si layer deposition followed by SPC. (d) Dry etching to form NWs underneath the hard mask and a spacer-like portion of poly-Si along the sidewall of the first gate. (e) Deposition of 100-nm *in situ* phosphorus doped poly-Si. (f) Simultaneous definition of NW channels and S/D regions using dry etching. (g) Second gate stack (20-nm LPCVD TEOS oxide and 100-nm *in situ* doped N+ poly-Si) deposition and patterning.

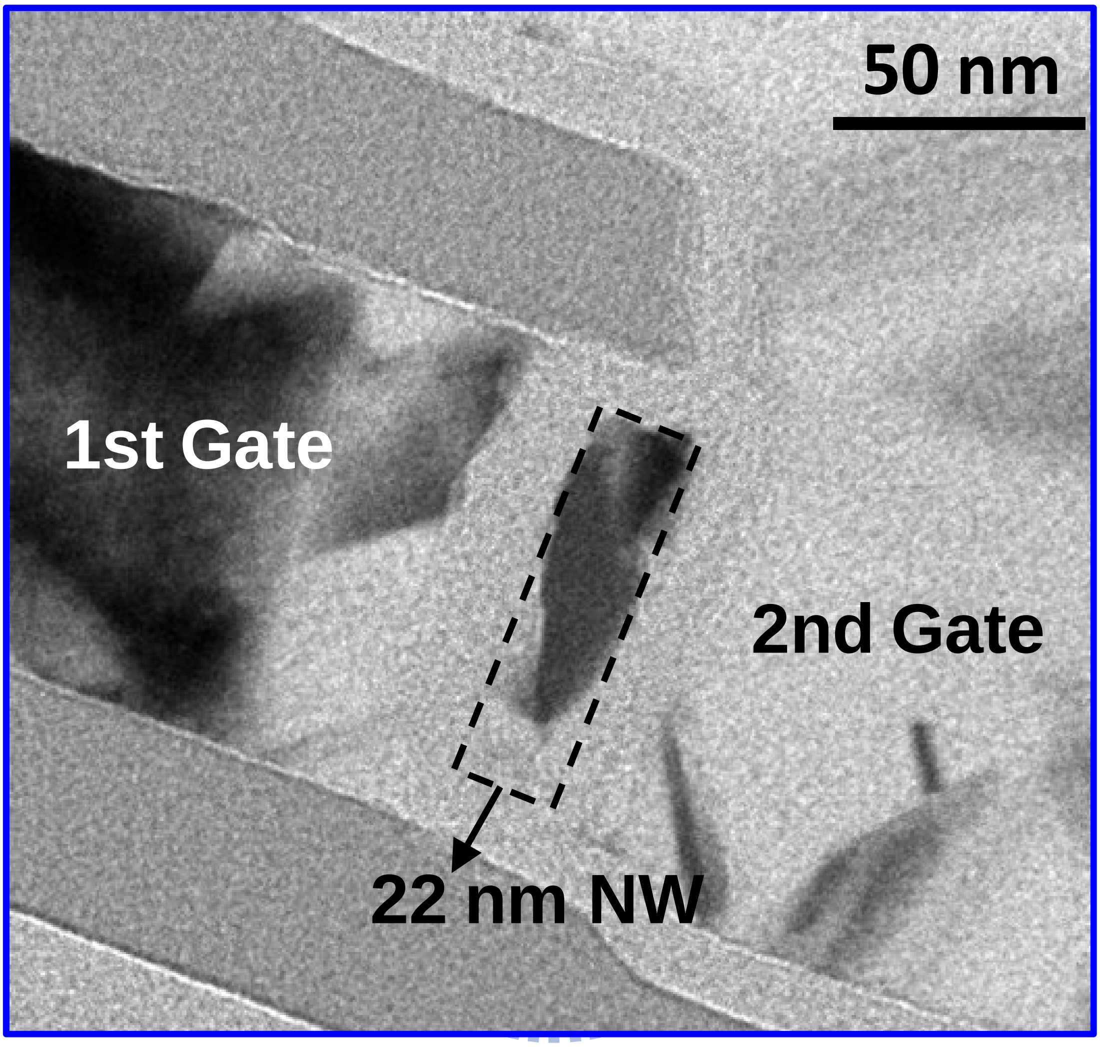


Fig. 3-2 Cross-sectional TEM image of an independent double-gated NW transistor with *in situ* doped S/D.

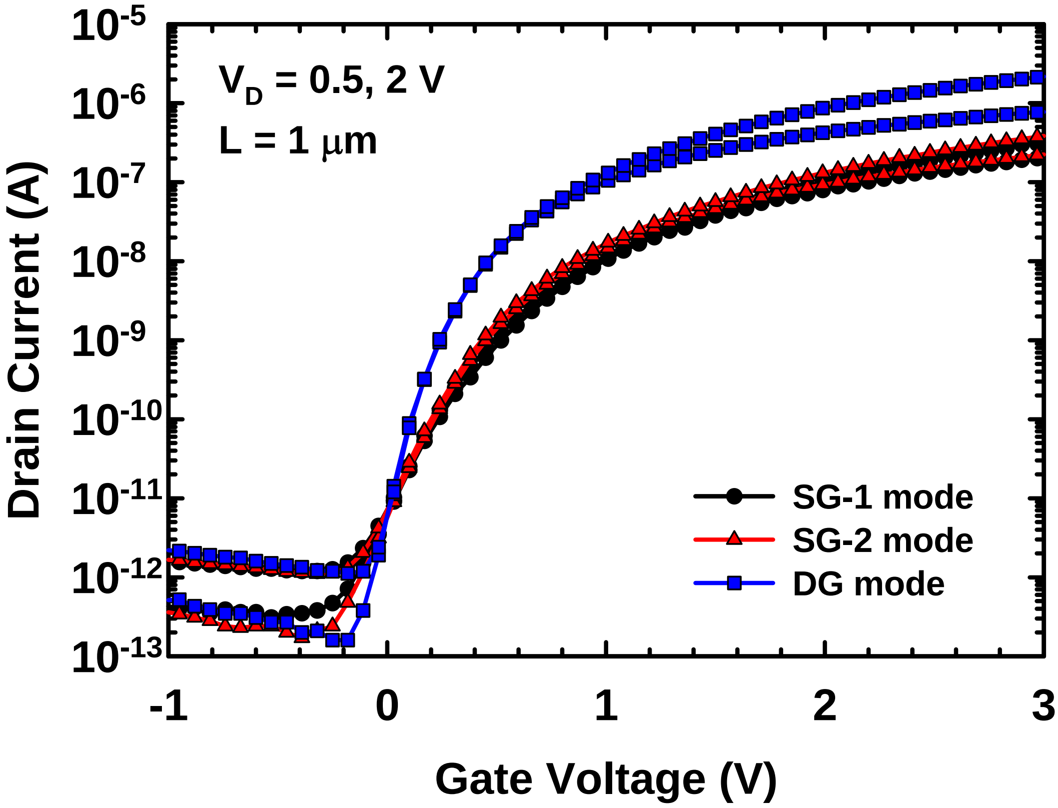


Fig. 3-3 Transfer characteristics of a fabricated device with implanted S/D.

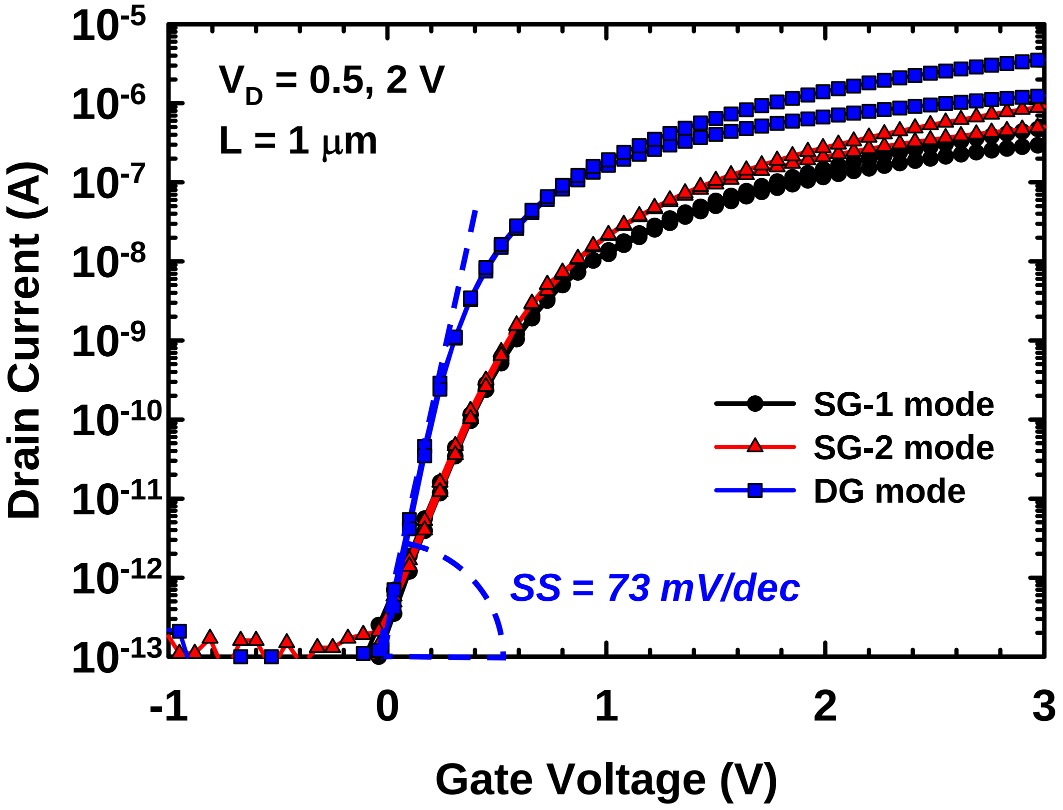
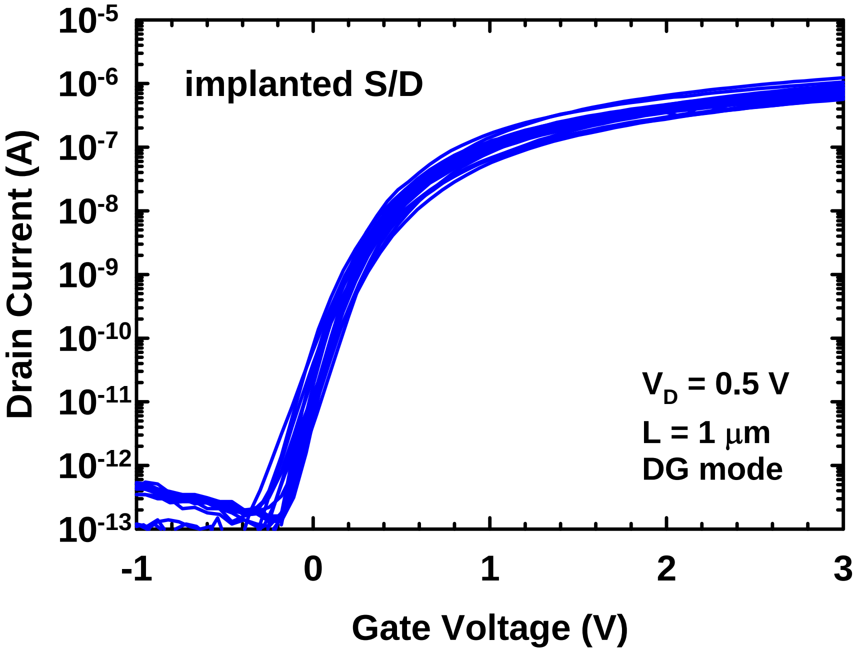
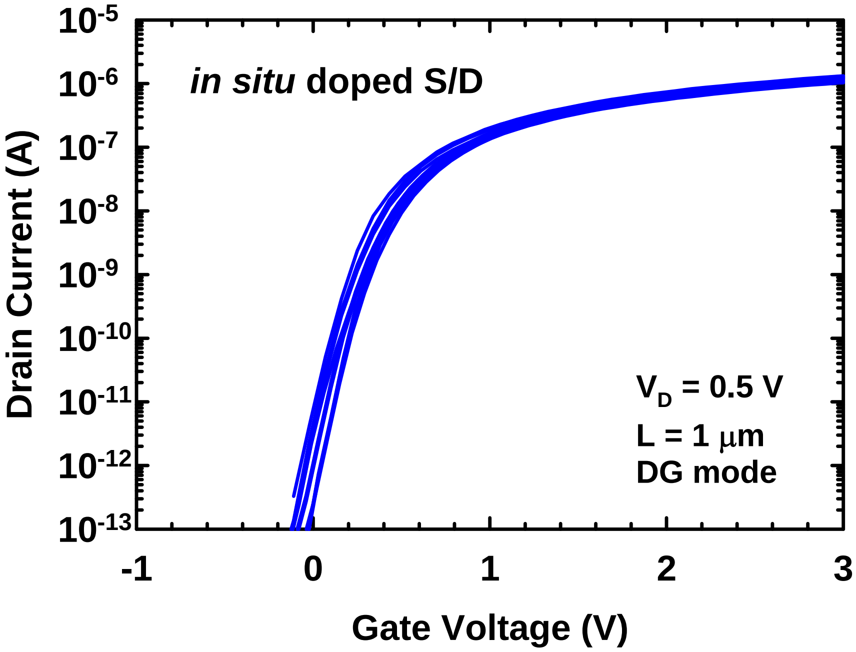


Fig. 3-4 Transfer characteristics of a fabricated device with *in situ* doped S/D. SS under DG mode is 73 mV/dec, the best value ever reported for a poly-Si based device.



(a)



(b)

Fig. 3-5 Fluctuation analysis of devices with (a) implanted S/D and (b) *in situ* doped S/D. Twenty devices are measured in each figure.

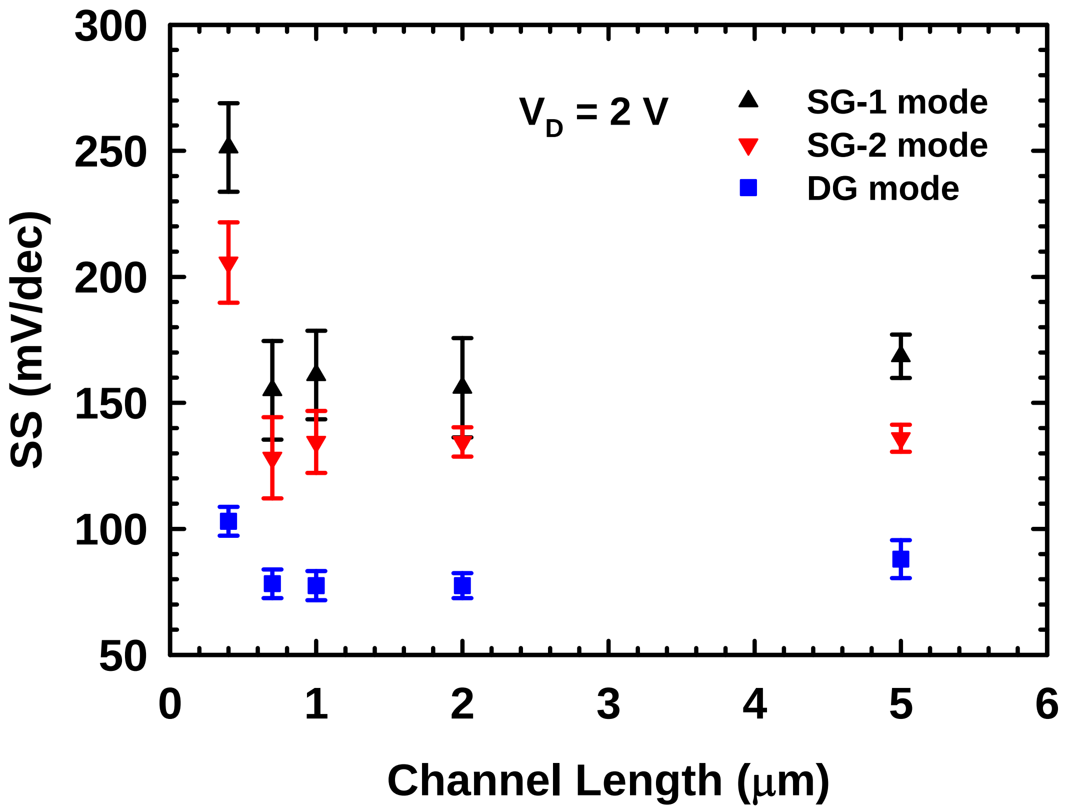
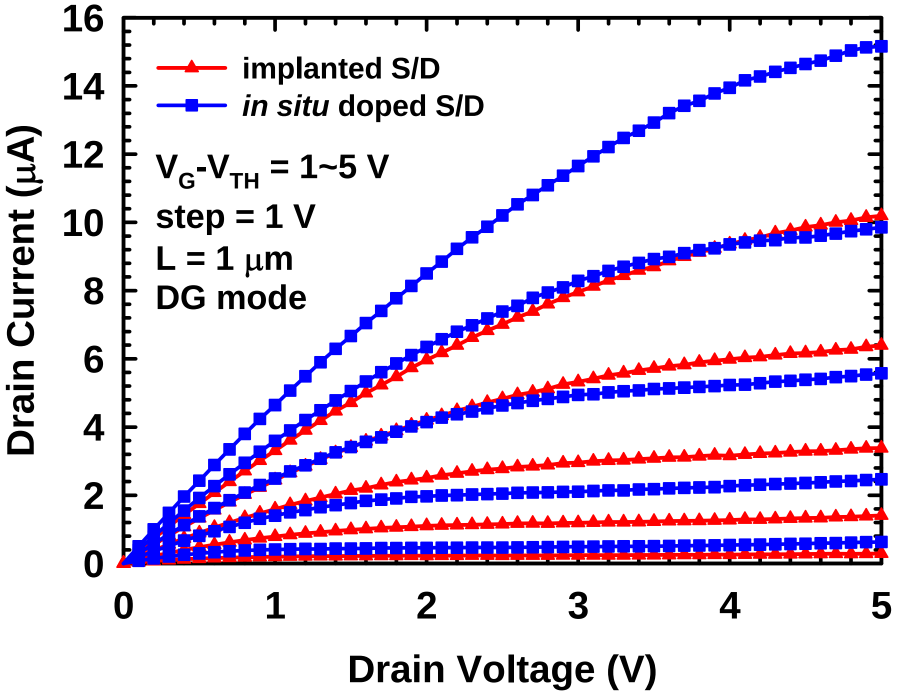
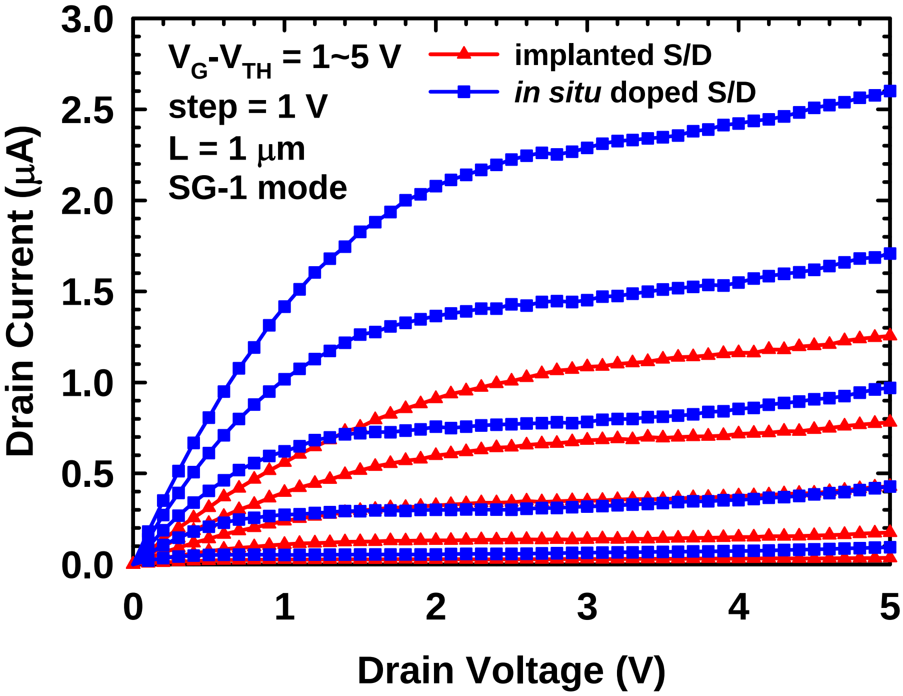


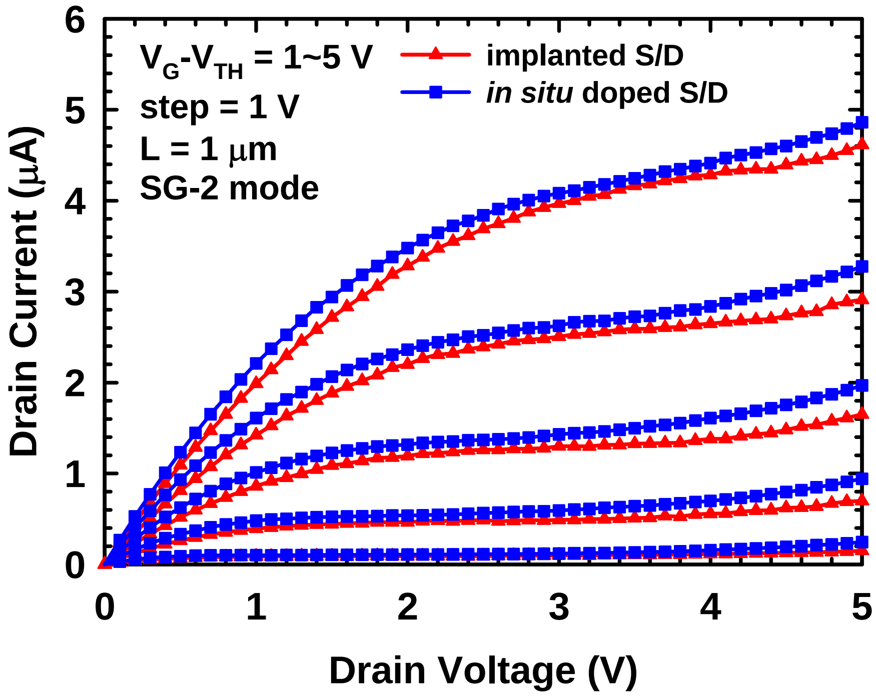
Fig. 3-6 SS as a function of channel length for the *in situ* doped device.


16
14
12
10
8
6
4
2
0
0
1
2
3
4
5
Drain Current (μA)
Drain Voltage (V)
implanted S/D
in situ doped S/D
V_G-V_TH = 1~5 V
step = 1 V
L = 1 μm
DG mode

(a)


3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
1
2
3
4
5
Drain Current (μA)
Drain Voltage (V)
V_G-V_TH = 1~5 V
step = 1 V
L = 1 μm
SG-1 mode
implanted S/D
in situ doped S/D

(b)



(c)

Fig. 3-7 Output characteristics comparison between devices with implanted and *in situ* doped S/D under (a) DG, (b) SG-1, and (c) SG-2 modes.

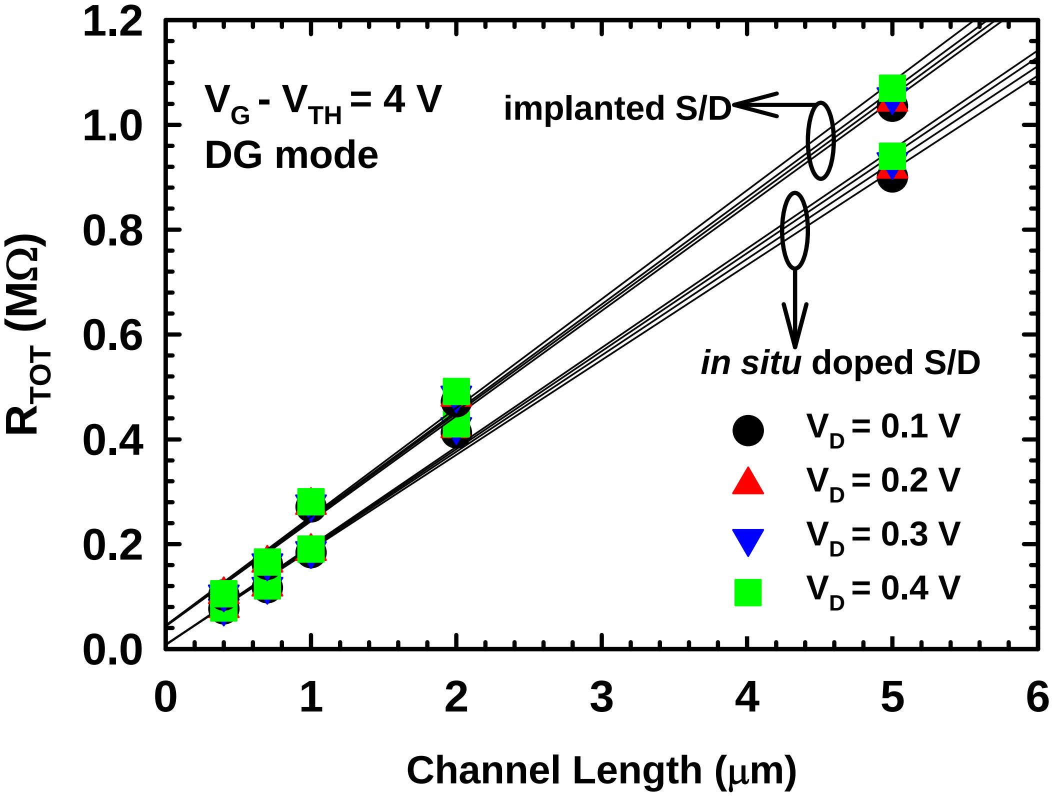


Fig. 3-8 Extraction of S/D series resistance showing five times reduction with the adoption of *in situ* doped S/D.

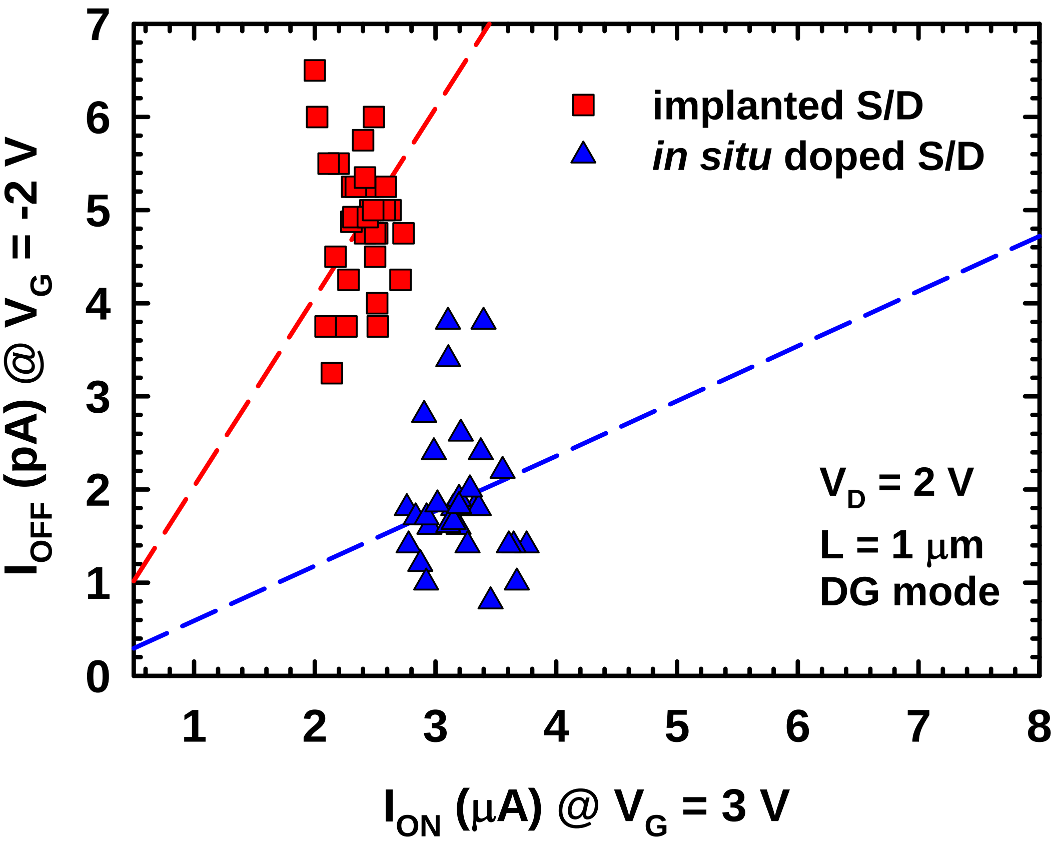


Fig. 3-9 I_{ON}-I_{OFF} statistical analysis comparison between devices with implanted and *in situ* doped S/D.

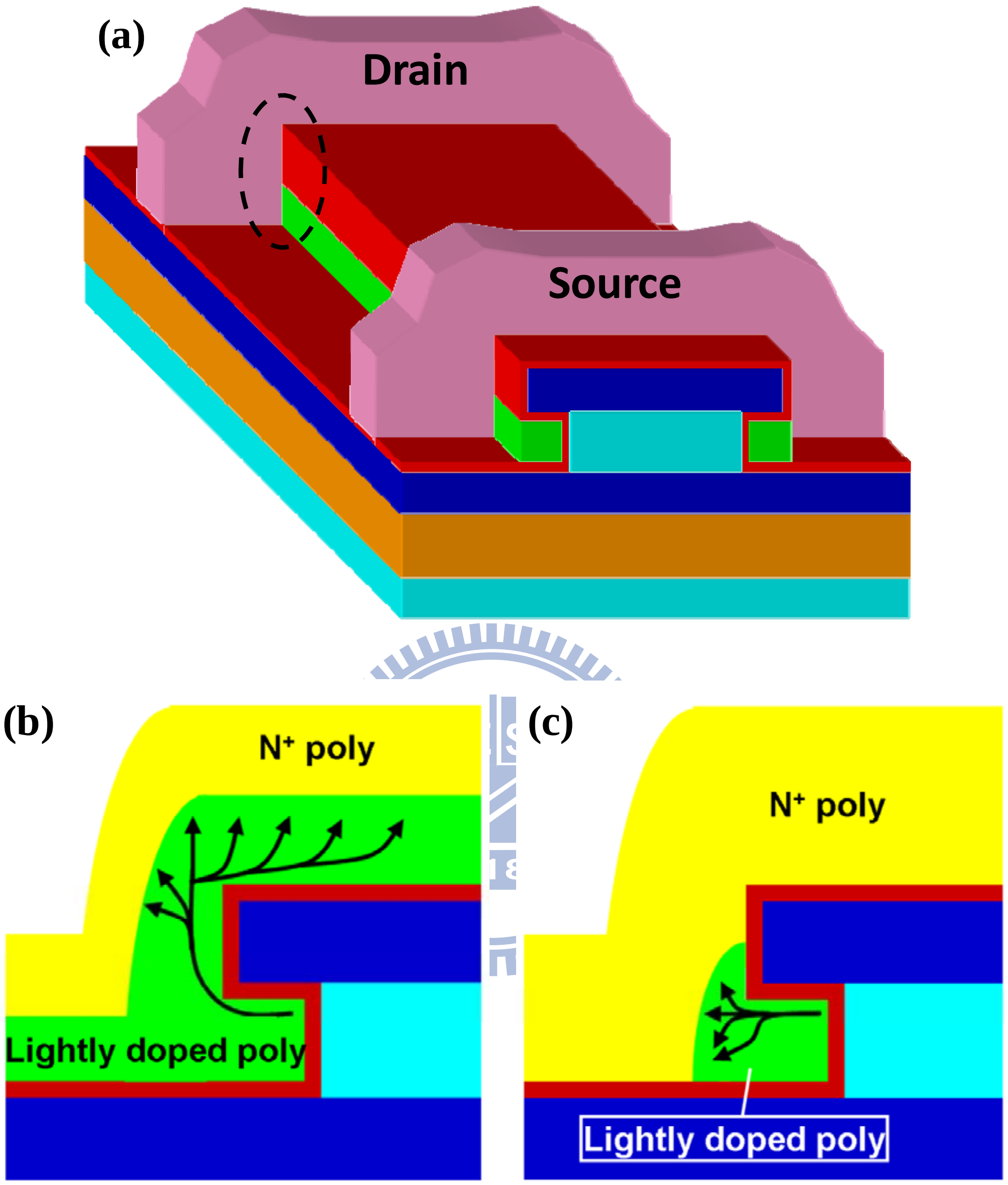


Fig. 3-10 (a) Schematic of the device structure before the 2nd gate stack deposition. GIDL current conduction paths in the circled area of (a) are depicted for (b) implanted S/D and (c) *in situ* doped S/D type devices.

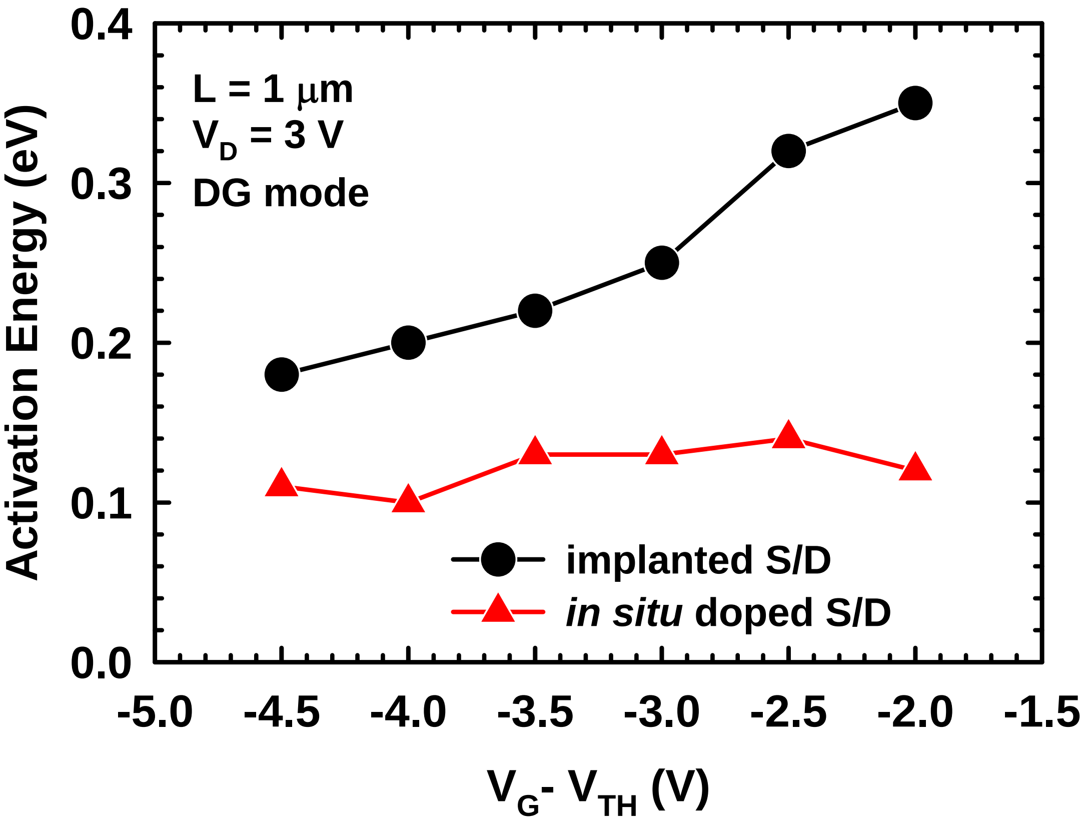


Fig. 3-11 Extracted activation energy of I_{OFF} as a function of gate underdrive for devices with implanted and *in situ* doped S/D. Implanted S/D type device displays a stronger dependency on the gate voltage, suggesting the dominant role of GIDL in determining I_{OFF}.

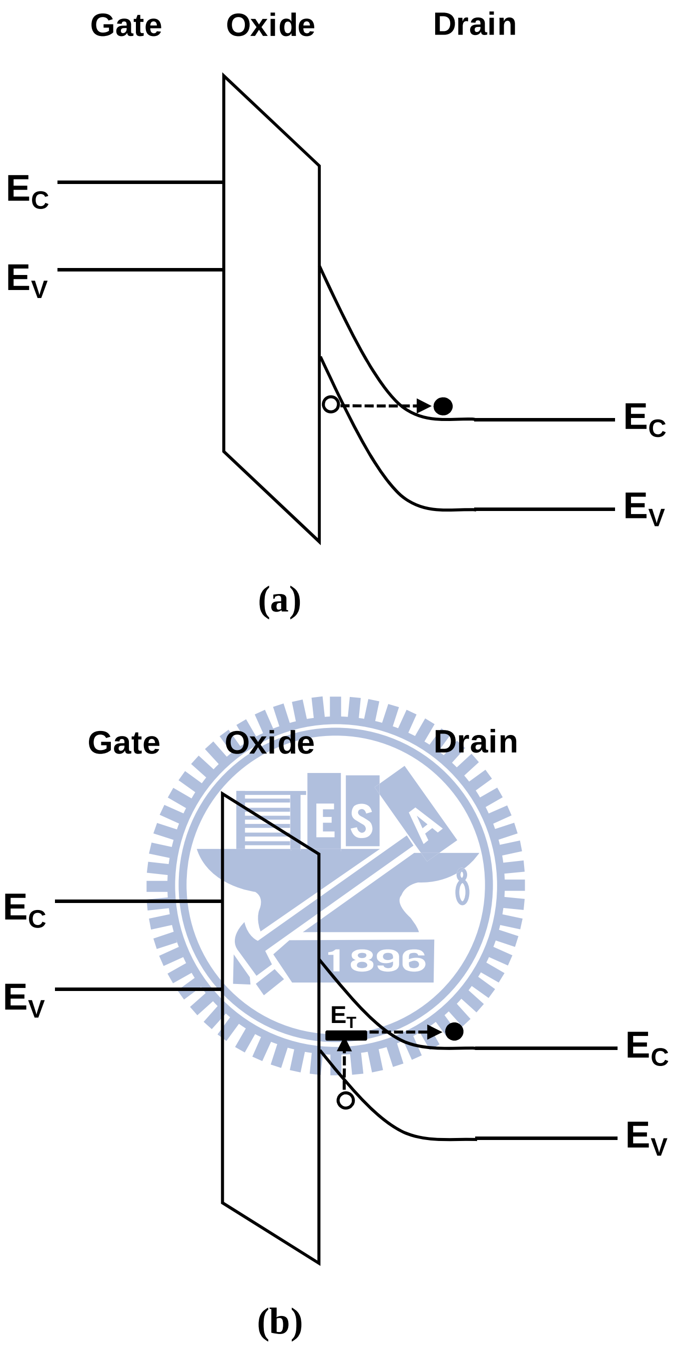


Fig. 3-12 Schematic band diagrams at the off state under two different gate biases. (a) For a sufficiently negative gate bias, BTBT dominates. (b) Under medium electric field regime, electrons are thermally activated to the trap state (E_T) followed by tunneling into the conduction band, also known as trap-assisted tunneling or thermionic field emission.

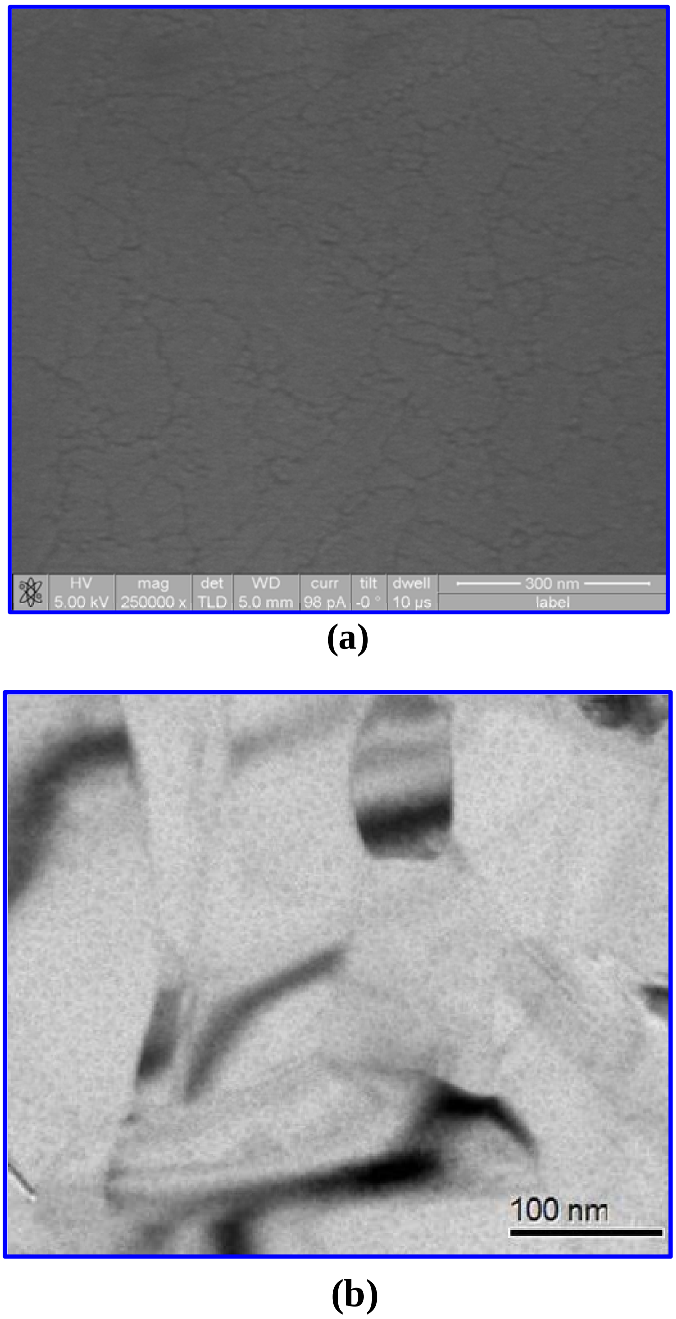


Fig. 3-13 (a) Plane-view SEM image of a 100-nm thick poly-Si layer obtained by SPC whose average grain size is around 60 nm. (b) Plane-view TEM image of a 100-nm thick *in situ* doped poly-Si layer whose average grain size is around 200 nm

Chapter 4

Investigations on Transport Properties of Double-Gated Poly-Si Nanowire Transistors under Cryogenic Ambient

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4.1 Introduction

The benefits offered by ultra-thin body are explicitly apparent from the scaling theory [4-1] which states that to maintain the same SS, the device should be designed in a way that the following α factor remains above a specific value

$$\alpha = \frac{L_G}{2\lambda} \tag{4-1}$$

where L_G is the gate length and λ is the so-called natural length, which is device-structure dependent. For DG SOI MOSFETs, λ is given by [4-2]

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{OX}}\left(1+\frac{\varepsilon_{OX}t_{Si}}{4\varepsilon_{Si}t_{OX}}\right)t_{Si}t_{OX}} \; . \tag{4-2}$$

And for cylindrical gate-all-around fully-depleted MOSFETs, λ is expressed as [4-3]

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{4\varepsilon_{OX}}\left(1+\frac{\varepsilon_{OX}t_{Si}}{4\varepsilon_{Si}t_{OX}}\right)t_{Si}t_{OX}} \; , \tag{4-3}$$

where t_{Si} and t_{OX} are the thicknesses of silicon and oxide, respectively, and ε_{Si} and ε_{OX} are the dielectric constants of silicon and oxide, respectively.

Regardless of the gate configuration, thinning t_{Si} is one of the most effective ways of keeping α constant as L_G is made shorter. At the same time, for a given t_{Si} and t_{OX}, it is obvious from equations (4-2) and (4-3) that the natural length of a gate-all-around device is 30 % smaller than that of a DG device, implying better scalability of the gate-all-around configuration owing to its cylindrical nature.

As the thickness and width of NW devices are scaled below 10 nm, some physical phenomena start to emerge, the most prominent of which is quantum confinement effect [4-4]. When this happens, the energy levels are no longer continuous in this scenario but become discrete sub-bands instead. For an N-channel device, electrons tend to populate the lowest sub-band whose energy difference between the conduction band edge increases with the scaling of NW dimensions. Consequently, V_{TH} becomes higher as NW is made narrower. The presence of discrete energy levels also leads to valleys in the drain current as the gate voltage is increased under low temperature regime because the sub-band must lie within the range of thermal energy from the previous sub-band that is already populated by carriers before further increase of the number of carriers is possible [4-5]. And in the situation when the energy separation between sub-bands is much larger than the thermal energy, the transport will be 1-D in which the density of states is a monotonically decreasing function of energy thereby making it easier to attain quantum capacitance limit [4-6]. This feature is particularly important in realizing steep subthreshold FETs such as tunneling FETs [4-7][4-8] where steep SS over *several decades* of the drain current is preferred.

Another interesting application of NW is in the study of single electron/hole effects. In a single electron/hole transistor, the active layer is essentially a zero-dimensional dot, known as an “island”, sandwiched by two tunneling junctions. The operational principle of single electron transistors is similar to a conventional FET except that the addition into or removal of an electron from the central island proceeds with integer precision. Because the potential (with respect to electron) of the island is raised each time an electron is added, which hinders further tunneling from the source due to non-availability of states, oscillation of the drain current as the gate voltage is varied can be observed, leading to the so-called Coulomb blockade. For this behavior to be clearly visible, the characteristic charging energy (the energy required to charge the island with one electron) as well as the energy level separation within the island must be larger than the thermal energy to avoid thermal excitation [4-9].

Given that most of the intriguing quantum-mechanical effects tend to occur in low temperature regime, in this chapter to investigate the underlying transport mechanism of the proposed independent double-gated NW poly-Si thin film transistors, devices with channel lengths (L) ranging from 39 nm to 5 μm were fabricated using mix-and-match lithography of I-line stepper and e-beam direct writing method, and characterized under cryogenic ambient. Electrical characterization performed in the temperature (T) range of 300 K to 78 K shows abnormal switching phenomena for one of the single-gated modes with very steep SS, which completely disappears when altering the gate-doping technique. It is also found that such phenomenon is related to a number of structural parameters. A simple model based on the process of electron trapping and detrapping in the channel is proposed.

4.2 Fabrication Process for Devices with Sub-100 nm Channel Length

By cleverly forming a cavity at two sides of a nitride/Si/nitride stack through selective etching of the sandwiched Si, followed by refilling with the active layer, we had demonstrated in Chapter 2 a novel and simple method for fabricating devices with decananometer NW dimensions using an optical I-line stepper. To overcome L limit set by the resolution of the I-line stepper which is merely 0.4 μm while maintaining a low cost approach, a slightly modified fabrication process by adding e-beam direct writing is adopted in this study to achieve sub-100 nm L with layout given in Fig. 4-1. It is worth mentioning that this new approach requires only one additional lithographic step, and can be easily integrated with the original version on the same wafer. In short, the new version is only different in the manner L is defined. That is, instead of directly forming source/drain (S/D) and channels in a single step, in the newly proposed method, mesa-isolation of active layer was first performed followed by another trench patterning to simultaneously define S/D and channels using e-beam writing with positive resist, which in turn also determined L.

4.3 Electrical Characteristics at Room Temperature

Plane-view and cross-sectional transmission electron microscopic (TEM) images of the fabricated device are shown in Figs. 4-2 (a) and (b), respectively. It can be seen from the plane-view picture that the grain sizes of 1st and 2nd gates are quite different which can be ascribed to the difference in doping methods [4-10]. Namely, the 1st gate of larger grain size is of *in situ* doped N^+ poly-Si, while the 2nd gate with smaller grain size is of implanted N^+ poly-Si. Note that the dielectrics for the 1st and 2nd gates are 15 nm and 5 nm tetraethyl orthosilicate (TEOS) oxide, respectively, while the thickness of NW (or the width between the two gate dielectrics) is 23 nm.

L-dependent transfer characteristics at 25 °C are shown in Fig. 4-3 and extracted SS versus L is depicted in Fig. 4-4. Among the three operation modes, SG-1 mode is the one most vulnerable to SCEs and thereby shows more severe SS degradation as L is reduced, in agreement with the results presented in Chapter 2. For SG-2 and DG modes, only minor SS enlargement is observed even when L is scaled to less than 100 nm. One point worth pointing out is that S/D regions of devices measured in the chapter are formed by low energy ion implantation, so instead of increasing with decreased L, the drive current is seen to saturate as L is below 0.7 μm, as can be clearly identified in SG-2 and DG modes of Fig. 4-3. This issue is expected to be relieved by silicided or *in situ* doped S/D, as discussed in Chapter 3.

4.4 Electrical Characteristics at Cryogenic Ambient

4.4.1 Evolution of Transfer Curves under Different Operation Modes with Respect to Temperature

Transfer characteristics measured at various T for a device with L = 70 nm are shown in Fig. 4-5. As compared with single-crystalline Si, carrier transport in poly-Si tends to experience additional scattering from trapping centers in grain boundaries, resulting in carrier depletion and the formation of potential barriers impeding carrier motion from one grain to another [4-11]. Therefore, thermionic emission over these energy barriers is usually considered as the major conduction mechanism when dealing with poly-Si, and our recent simulation results have shown that thermionic conduction indeed well describes the transfer and output characteristics of the proposed device at room T [4-12]. This kind of thermally activated process also manifests itself in a way that the mobility and V_{TH} would decrease and increase, respectively, as T is reduced

[4-13][4-14]. Transfer curves under SG-1 mode in Fig. 4-5 (a) are clearly consistent with the above statements. More importantly, an intriguing phenomenon is found in SG-2 mode. As shown in Fig. 4-5 (b), V_{TH} depicts an unexpected drastic increase for T below 200 K. Moreover, SG-2 mode displays a very abrupt turn-on phenomenon when T is lower than 150 K. Specifically, SS under SG-2 mode is 3.4 mV/dec at 78 K and 4 mV/dec at 100 K. Finally for DG mode in Fig. 4-5 (c), the contribution from the channel controlled by the 2nd gate also causes a sudden increase of I_D at 100 K and 78 K.

Extracted SS and V_{TH} as a function of T are shown in Figs. 4-6 (a) and (b), respectively. Ideal value of SS, which is equal to ln10 × kT/q where k is Boltzmann constant and q the elemental charge [4-15], is also plotted for comparison. From Fig. 4-6 (a), under 100 K and 78 K, SS of SG-2 mode is already smaller than the ideal value, an indicator that conventional drift-diffusion principle [4-16] is no longer the dominant mechanism governing the transport behavior in these cases. On the other hand, as explained in Chapter 2 and reported in [4-17], operation under SG-1 mode tends to exhibit larger V_{TH} than SG-2 mode due to additional non-gated routes in SG-1 mode *at room temperature*; however, the larger V_{TH} under SG-2 mode over SG-1 mode within the range of 200 K to 100 K in Fig. 4-6 (b) implies that some implicit effects in SG-2 mode may start to become prominent at low T regime. Transfer curves at 78 K in Fig.

4-7 reveal that the occurrence of this abrupt turn-on phenomenon has a strong dependency on L and in stark contrast to the widely accepted theory concerning SCE, the subthreshold current is seen to decrease with reducing L. Since all of the aforementioned unconventional features are exclusive only in SG-2 mode, the following discussion will focus on SG-2 mode unless otherwise specified.

4.4.2 Model Establishment and Discussion

A closer look at the process flow suggests this exclusivity is most likely caused by the different doping methods of the two gates. Namely, doping of the 1st gate was done by *in situ* technique that adds phosphine to silane during LPCVD (low pressure chemical vapor deposition) deposition of poly-Si, where very uniform and heavy doping concentration throughout the whole 1st gate electrode is achieved. As for the 2nd gate, dopants were introduced by phosphorus ion implantation with 15 keV at 5×10^{15} cm^{-2} dose. Taking into account the unique device structure measured, *i.e.*, one with raised S/D, a schematic device structure along L direction showing the 2nd-gate-controlled side of channel is depicted in Fig. 4-8 (a) for a long L (> 100 nm) device and Fig. 4-8 (b) for a short L (< 100 nm) device. For devices with L shorter than the thickness of the 2nd gate (100 nm), the central part of trench between S/D is filled with thicker poly-Si, compared with those with L longer than 100 nm, based on the nature of LPCVD deposition. As a result, for a given implantation energy, the doping concentration is distributed in a manner such that the portion of the 2nd gate farthest from the top surface (*i.e.*, closest to the channel) is only lightly doped, as in Fig. 4-8 (b), compared with the much higher doping concentration, as shown in Fig. 4-8 (a). In Figs. 4-8 (a) and (b), points A and C correspond to the regions of the channel adjacent to S/D controlled by the locally thickened gate, and point B to the middle of the channel. Since the 2nd gate is the thickest in the regions abutting S/D, the lightly doped area of the 2nd gate spreads to a larger extent in the channel edge than the middle of the channel. The above surmise is clearly confirmed by simulation results in Fig. 4-9.

This non-uniform dopant distribution then leads to variation in gate controllability along the channel, *i.e.,* gate to channel capacitance is the largest in the middle of the channel and decreases toward the channel edge. In this aspect, akin to [4-18] where the reported non-overlapped device leads to potential dip in the middle of the channel in Fig. 4-10, electrostatic potential along the channel exhibits two humps near S/D, as qualitatively depicted in Fig. 4-11. Due to the good step coverage offered by LPCVD, those segments of the 2nd gate of a long L device making contact with the central channel are still heavily doped (Fig. 4-8 (a)), explaining the reason the potential of the central channel is much lower in a long L device than that of a short one, as shown in Fig. 4-11. Meanwhile, even though the potential barriers from the two humps are always present for all the characterized L, the barrier height of the humps is smaller in a long L device owing to the stronger gate fringing fields from the more heavily doped gate for a given 2nd gate voltage. With this picture in mind, the behavior of transfer characteristics with strong L dependency shown in Fig. 4-7 becomes reasonable based on the model shown in Fig. 4-12. Before further discussion, it should be noted that the tunneling current in poly-Si is often expected to have minor contribution because in practical situations thermionic emission current is always the preponderant component [4-11]. Nonetheless, tunneling should become appreciable at cryogenic ambient and in the scenario when the tunneling barrier is narrow enough.

For a short L device, the large barrier height of the humps and the high channel potential in virtue of lower 2nd gate doping concentration render tunneling less likely to happen and thermionic emission then assumes a major role even at low T. In this regard, as T is lowered, the thermionic emission current is gradually reduced, which in turn increases V_{TH}, and because the barrier heights of the two humps are essentially independent of T, it is rational that below a certain T when thermal energy is far smaller than the barrier height, the 2nd gate voltage must be high enough ($V_{G2} = V_1$) to reduce the barrier height at point A in Fig. 4-11 to a extent that carriers are able to be thermally emitted from the source. Yet instead of directly transporting to drain, carriers coming from the source to the channel will get trapped therein (in point B of Fig. 4-11), raising the channel potential level and preventing further injection from the source, as illustrated in Fig. 4-12 (a). This scenario will persist until the barrier height present at point C is reduced significantly by a higher applied gate voltage ($V_{G2} = V_2 > V_1$) for the trapped electrons to overcome the barrier with ease and be released to the drain. As a consequence, the channel potential is lowered suddenly and an abrupt increase of drain current is observed (Fig. 4-12 (b)). To further validate our argument, the elimination of the barriers is achieved by *in situ* doping both the 1st and 2nd gates, and the characteristics in Fig. 4-13 evidently corroborate the previous model that implanted gate is indeed the culprit for the peculiar abrupt switching phenomenon.

With a long L device, the same theory still applies. As mentioned previously with respect to the channel potential profile, the potential difference between the central channel and the source is sufficiently small so that tunneling through the barrier is possible besides thermionic emission. The critical T below which thermionic emission is no longer possible without strong gate-induced barrier reduction is supposed to be lower for a long L device thanks to its smaller magnitude of barrier height. It is then expected that thermionic emission and tunneling are both the participating conduction mechanisms, explaining the larger subthrehold current for a long L device. Further lowering of the measurement T can help verify this statement by examining the evolution of mobility and V_{TH} with respect to T based on the fact that the degree of T dependence of thermionic emission and tunneling is drastically different; that is, tunneling should have little temperature dependence as opposed to thermionic emission, which as its name suggests is strongly temperature dependent. Accurate modeling of the shape and magnitude of barriers is of significance as well in distinguishing between the individual contribution from thermionic emission and tunneling processes, and is still under investigation owing to the complex structure of our proposed device. Nevertheless, the electron-trapping effect can also occur for a long channel device if T is low enough, so that an abrupt switching (*e.g.*, see L = 0.7 μm in Fig. 4-7), though with a larger SS compared with a device with short L, is attained. And the L = 5 μm device in Fig. 4-7 exhibits a change of SS at V_{G2} = 3.1 V as well on account of the onset of a sudden barrier lowering. Given that the dominant factor determining the occurrence of abrupt transition lies in the barrier height present at S/D, the impact of drain-induced barrier lowering (DIBL) is investigated in Fig. 4-14. Consistent with the proposed model, the profound influence exerted by DIBL which lessens the barrier height at the source side with increasing drain bias is apparently demonstrated. Making use of the separate-gated property, Fig. 4-15 (a) plots the transfer characteristics at 150 K as a function of the 1st gate bias (V_{G1}). V_{G1} here ranges from -1 V to 1 V in 0.5 V step. Subthreshold current becomes appreciable only when V_{G1} is higher than 0.5 V because under these conditions the channel controlled by the 1st gate starts to make contribution to the overall drain current, as can be seen from Fig. 4-5 (a). Nevertheless, SS remains the same irrespective of V_{G1} since the 2nd gate still provides the preponderant control over the channel and the maximum V_{G1} applied is less than what is required to invert the 1st-gate-controlled channel. Similar behaviors can be noted in 78 K in Fig. 4-15 (b) except that now even $V_{G1} = 1$ V only corresponds to accumulation for the channel on its side, and negligible IV curve shift is obtained as a consequence.

4.4.3 Observation of Hysteresis and Single Electron Effects

Since the proposed model implies that the conduction mechanism is similar to a feedback process, which has been utilized in achieving steep SS devices [4-19], the forward and reverse sweeping of the gate voltage is expected to result in hysteresis of transfer characteristics, as evidenced in Fig. 4-16 and Fig. 4-17 for L = 5 μm and 63 nm at 78 K, respectively. Here the applied drain voltages are 10 mV and 0.1 V. Negligible hysteresis in SG-1 mode indicates that it still obeys the drift-diffusion principle so that the turn-on and turn-off processes are reversible, and the effect of trapping in grain boundaries of poly-Si can be ruled out since plasma treatment was performed on the devices prior to characterization [4-20]. In contrast, SG-2 mode exhibits apparent hysteresis, with V_{TH} window at $V_D = 0.1$ V being 0.7 V and 3 V for L = 5 μm and 63 nm, respectively. This is because of the voluminous mobile charges existing in the on-state, so during the reverse sweeping, the device cannot be turned off at the same voltage as it is turned on. In Fig. 4-16 (b), reverse sweeping displays a steeper SS than the forward one probably due to the additional effect of interface charges. A more detailed interpretation will be given later. It is interesting to note that SS of the reverse sweeping is larger than that of the forward one in Fig. 4-17 (b), which is related to their dissimilar effective barrier profiles. At the outset of the reverse sweeping when the 2nd gate voltage is sufficiently large, the barrier heights present at both the middle and edges of the channel are small compared with the thermal energy. As the 2nd gate voltage is gradually decreased, the conduction band edge of the central channel is supposed to be raised at a more rapid rate over that of the portion that is adjacent to S/D. In this regard, the major conduction barrier profile as seen by carriers is similar to that of a conventional MOSFET and the depth of the potential well is reduced with decreasing gate voltage. For the same reason, the trapping of carriers is less severe in the reverse sweeping process and a smaller V_{TH} is obtained as a result. Even though the effect of trapping/detrapping is now dramatically diminished compared with the turn-on process, this mechanism still needs to be taken into account given that during the turn-off process, SS of a short channel device in Fig. 4-17 (b) is steeper than that of a longer one in Fig. 4-16 (b).

The above statement also provides another perspective on the characteristics in Fig.

4-16 (b). As noted in Section 4.4.2, the effect of trapping/detrapping is actually not negligible for a long L device; hence, in the forward sweeping curve from V_{G2} = 0.1 to 3 V, the subthreshold current suffers carrier trapping and beyond V_{G2} = 3 V, detrapping sets in along with a sudden jump of the drain current. Since electron trapping in this case does not completely suppress the drain current as in a short L device, SS of forward sweeping is reasonably larger than that of the reverse one.

V_D-dependent I_D-V_G curves plotted in Fig. 4-18 (a) imply that at 78 K hysteresis is observable at least up to V_D = 2 V and the hysteresis window is monotonically decreasing with T, as shown in Fig. 4-18 (b), which is consistent with the fact that the probability of trapping/detrapping process occurrence is reduced with higher T.

As a matter of fact, some of the measured devices exhibit drain current oscillation as the gate voltage is varied. Figure 4-19 (left vertical axis) depicts such a behavior by magnifying I_D-V_G curves in the strong inversion regime. The corresponding G_M characteristic is shown in Fig. 4-19 as well in the right vertical axis. Although our proposed device is not intended to operate as a single electron transistor (SET), the potential valley in Fig. 4-11 assumes the role of an island and the two humps to its side are essentially tunneling junctions. However, owing to the large gate voltage interval (25 mV), the directly-counted period of G_M oscillation shows only three different values and thus it is difficult to accurately perform a Gaussian fit, which is required for extracting the charging energy [4-18] [4-21]. Another factor that may contribute to the drain current oscillation is inter-sub-band scattering whose influence becomes greater as the carrier concentration is increased due to the larger number of occupied sub-bands [4-22]. Asymmetric kink points for a given gate voltage in Fig. 4-20 suggest that the magnitude of barrier height at S/D is not identical, which can also be verified by interchanging the applied biases of S/D for I_D-V_G characterization in Fig. 4-21.

4.5 Summary

Making use of the mix-and-match of I-line stepper and e-beam direct writing, independent double-gated poly-Si NW transistor with L ranging from 39 nm to 5 μm are successfully fabricated and demonstrate excellent SCE immunity in terms of insignificant SS roll-off. And the origin of abrupt turn-on characteristics observed in SG-2 mode at cryogenic ambient is comprehensively studied in this chapter. It is found that the occurrence of this behavior is greatly influenced by L, T, and drain bias. A model taking into account the dopant distribution of an implanted gate is proposed to interpret our findings. It suggests that the non-intentionally formed barriers at the channel edge give rise to carrier trapping effects until an adequately large gate voltage is applied to lower the magnitude of the barriers for the trapped electrons to flow to the drain. Furthermore, since the channel potential profile resembles that of an island confined by two tunneling junctions, single-electron effects are also observed. This kind of process-induced barrier is an attractive scheme to build SETs with simple CMOS-compatible process flow and with the aid of further surface engineering should help realize steep SS transistors at room temperature.

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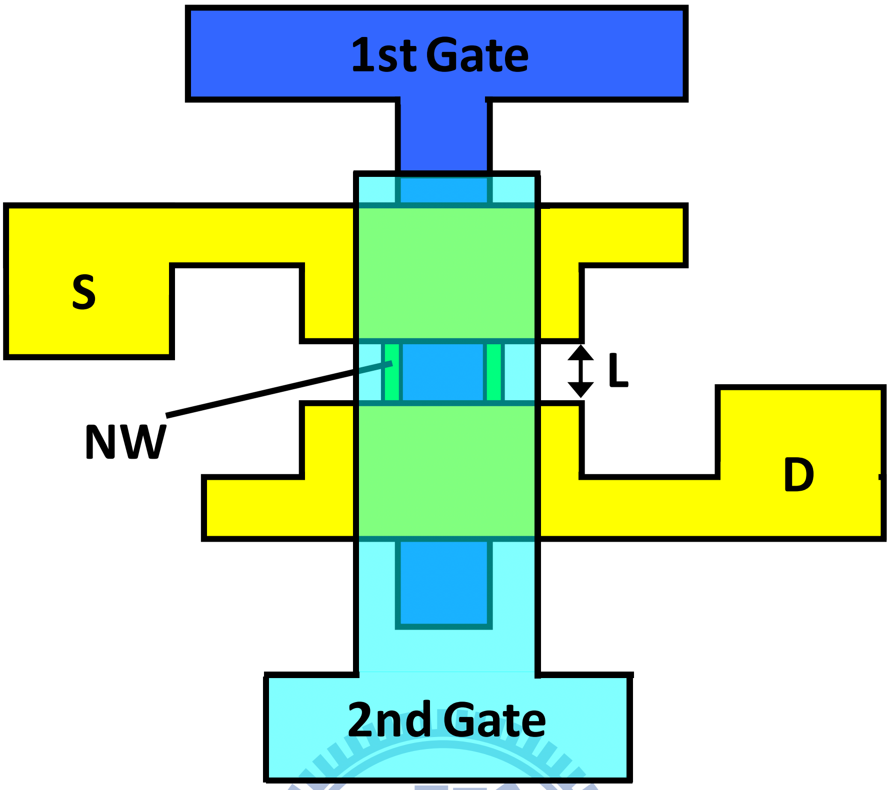
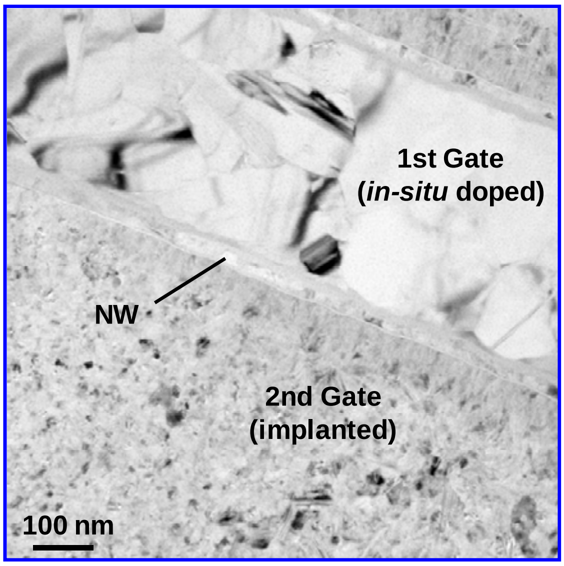
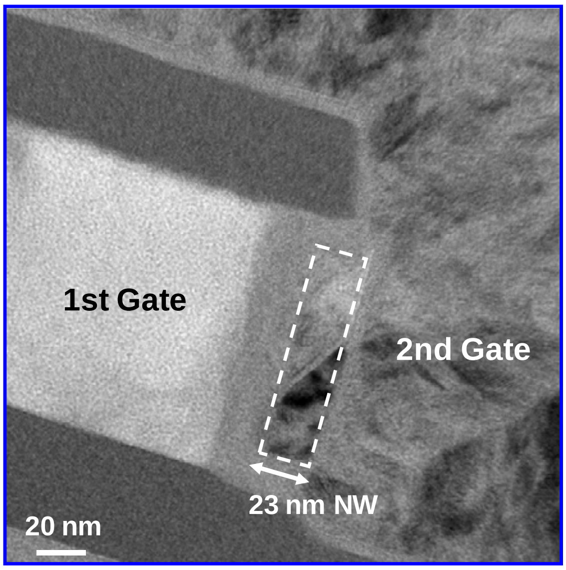


Fig. 4-1 Layout of the device fabricated using mix-and-match between e-beam and I-line. L defines the channel length, which is smaller than 100 nm in this case.



(a)



(b)

Fig. 4-2 (a) Plane- and (b) cross-sectional view images of a fabricated device showing a 23-nm-thick NW channel surrounded by the 1st and 2nd gates. The drastic grain size discrepancy between the 1st and 2nd gates is a consequence of the different doping method implemented: the 1st gate is by *in situ* doping while the 2nd gate by implantation.

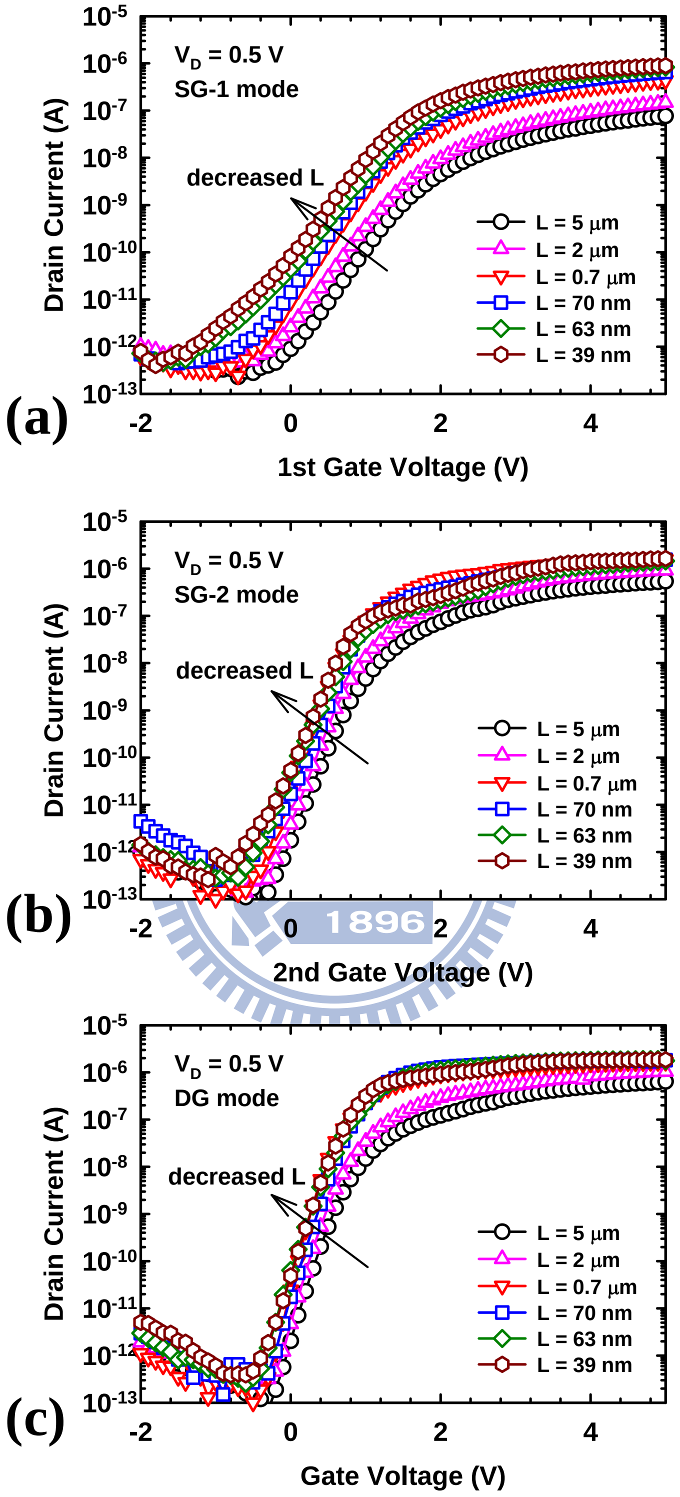


Fig. 4-3 Length-dependent transfer curves at 25°C under (a) SG-1, (b) SG-2, and (c) DG modes.

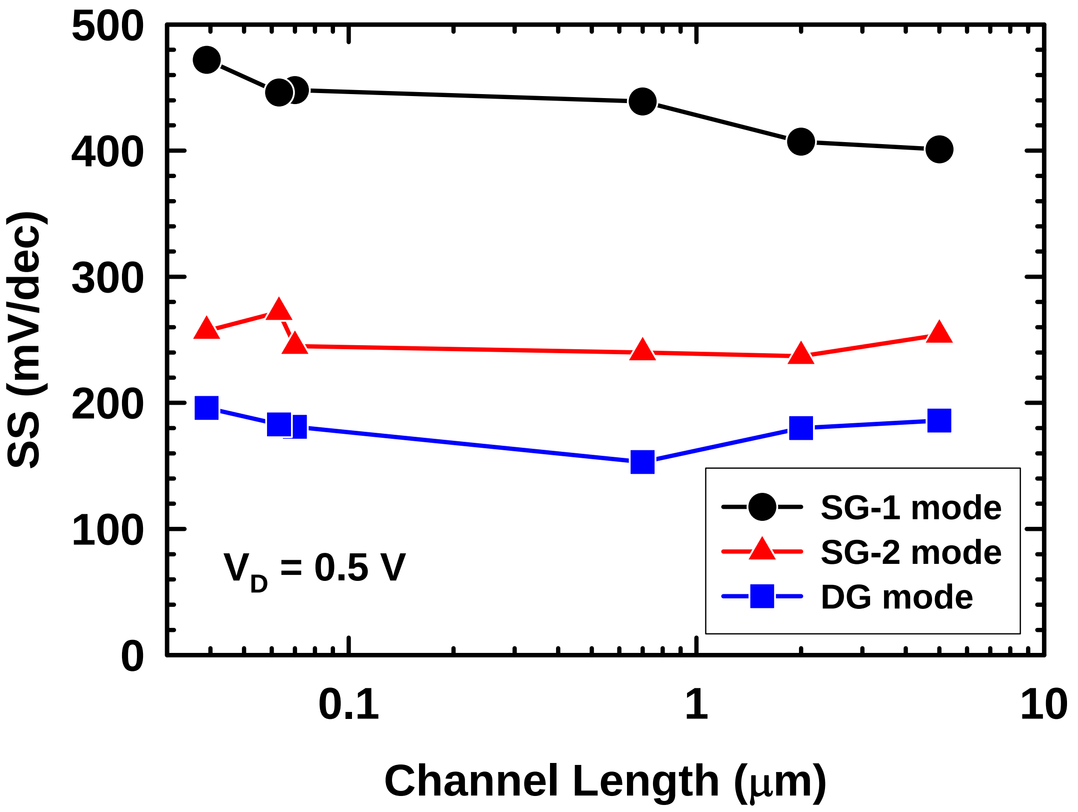
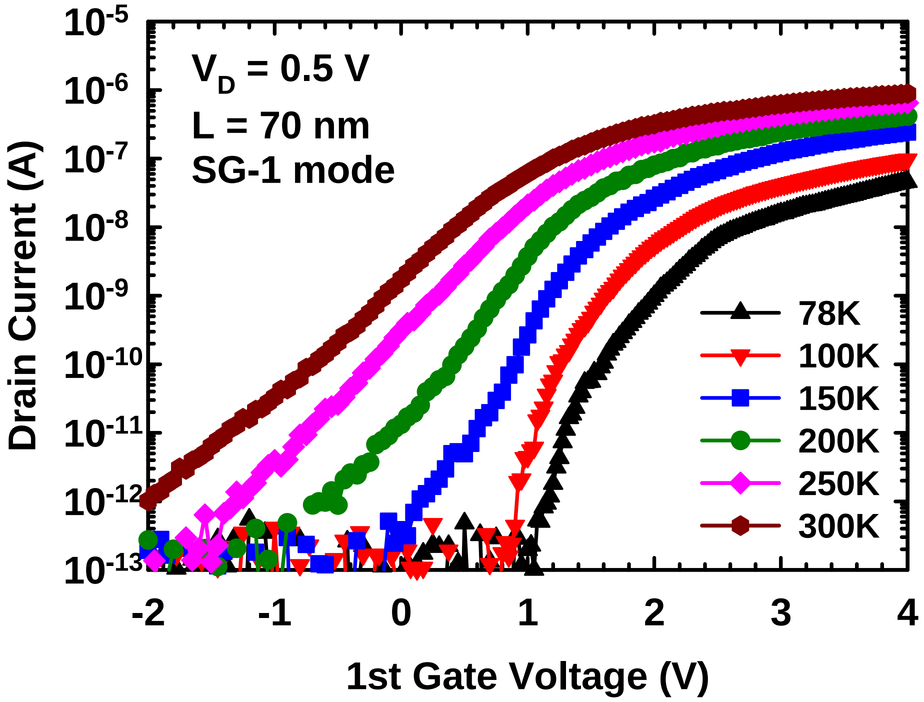
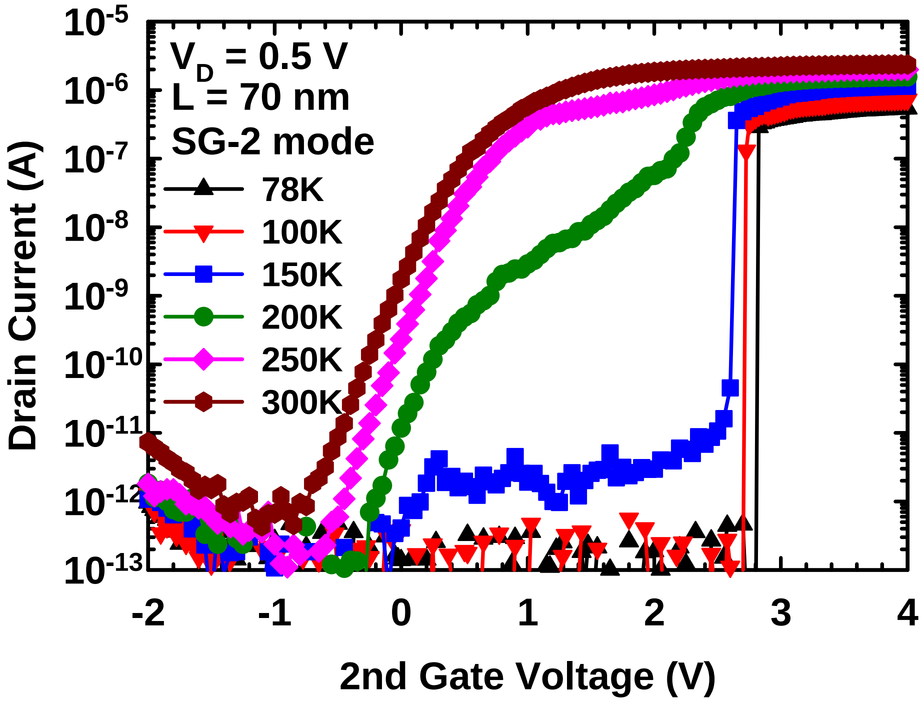


Fig. 4-4 SS as a function of L extracted from Fig. 4-3.



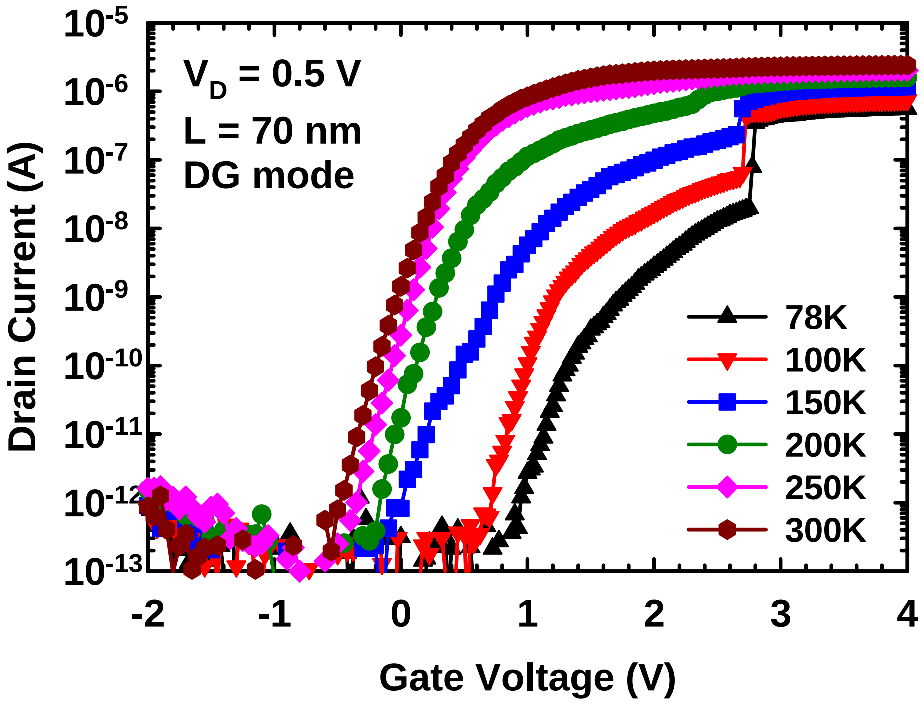
V_D = 0.5 V
L = 70 nm
SG-1 mode
78K
100K
150K
200K
250K
300K
Drain Current (A)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
-2
-1
0
1
2
3
4
1st Gate Voltage (V)

(a)



V_D = 0.5 V
L = 70 nm
SG-2 mode
78K
100K
150K
200K
250K
300K
Drain Current (A)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
-2
-1
0
1
2
3
4
2nd Gate Voltage (V)

(b)



(c)

Fig. 4-5 Transfer characteristics at various temperatures for a device with 70 nm channel length under (a) SG-1, (b) SG-2, and (c) DG modes. The behavior of SG-1 mode is in accordance with thermionic emission model while SG-2 mode starts to exhibit very steep SS when T is below150 K. Abrupt increase of I_D for DG mode at 100 K and 78 K is caused by the channel controlled by the 2nd gate.

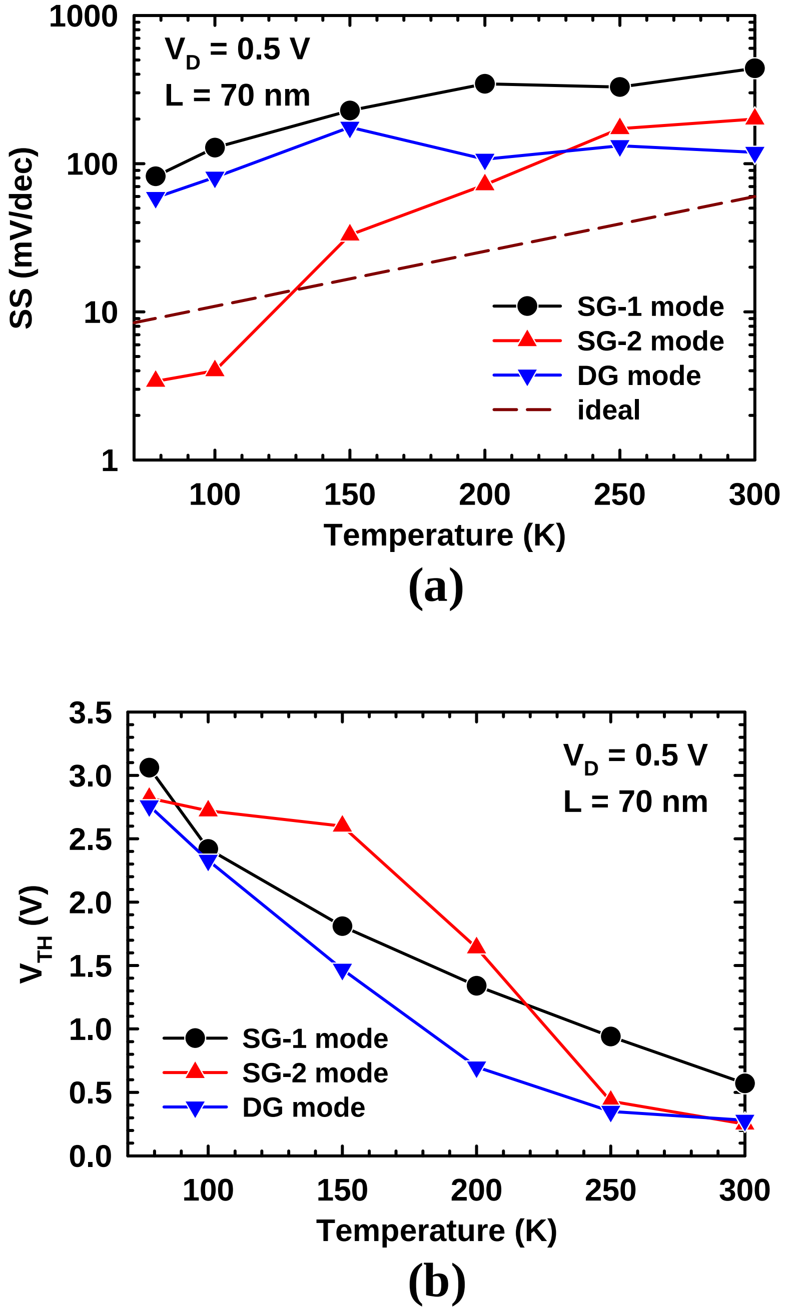


Fig. 4-6 (a) SS and (b) V_{TH} as a function of temperature for three operation modes extracted from Fig. 4-5. Ideal value of SS equal to ln10 × kT/q is also included for comparison in (a).

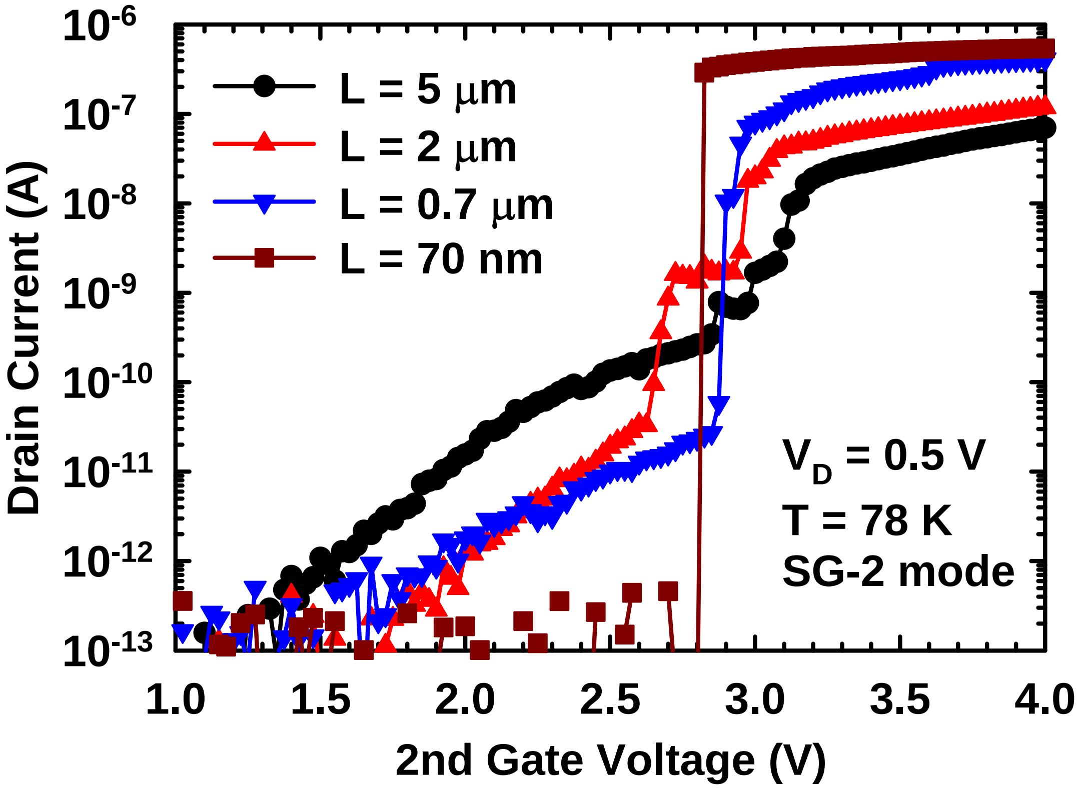


Fig. 4-7 Transfer characteristics at 78 K showing impacts of L in determining the occurrence of steep SS. In conflict with the conventional SCE theory, the subthreshold current is reduced as L is shortened.

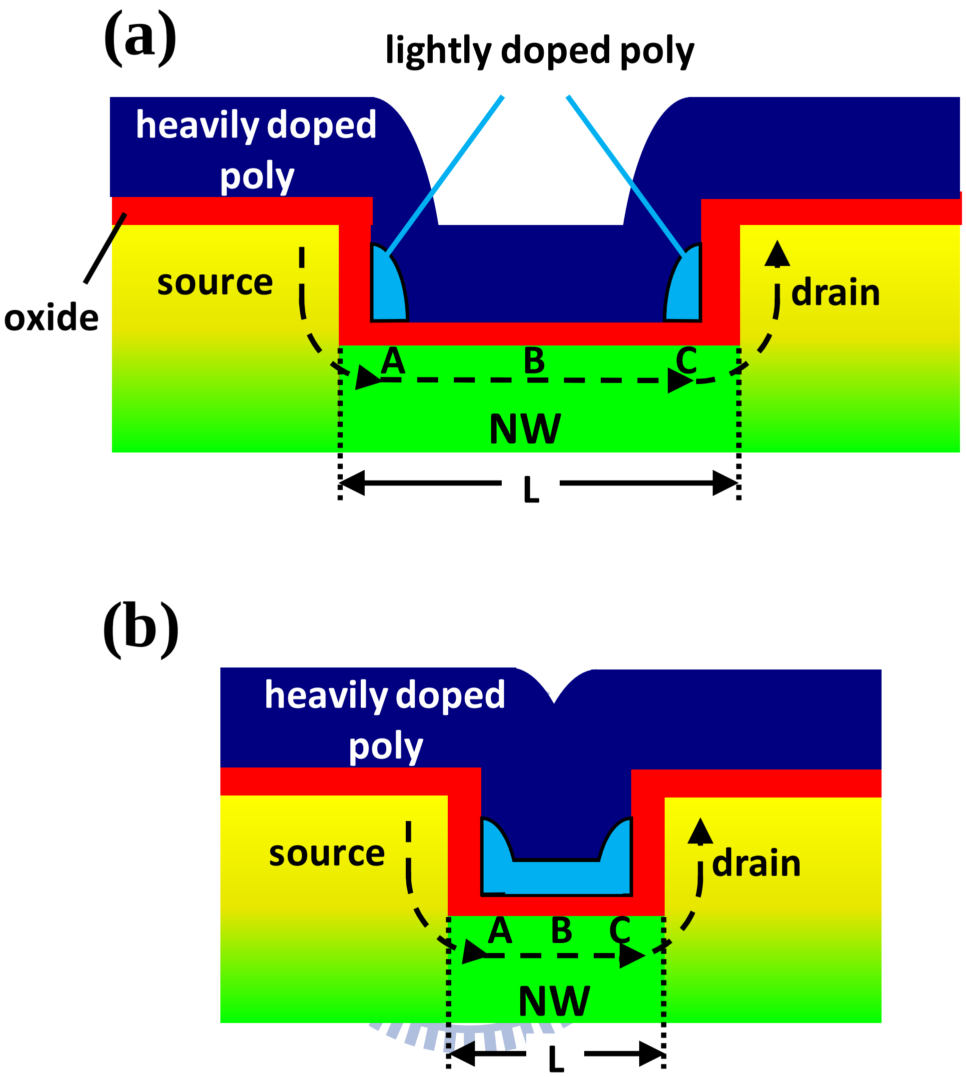


Fig. 4-8 Schematic structures along the length direction showing the 2^{nd} gate-controlled side of channel for a device whose L is (a) long (> 100 nm) and (b) short (< 100 nm). Points A and C correspond to regions of the channel adjacent to S/D controlled by the locally thickened gate and point B to the middle of the channel. Because the thickness of the 2^{nd} gate is 100 nm, the part of the 2^{nd} gate between S/D is thicker in (b) than in (a).

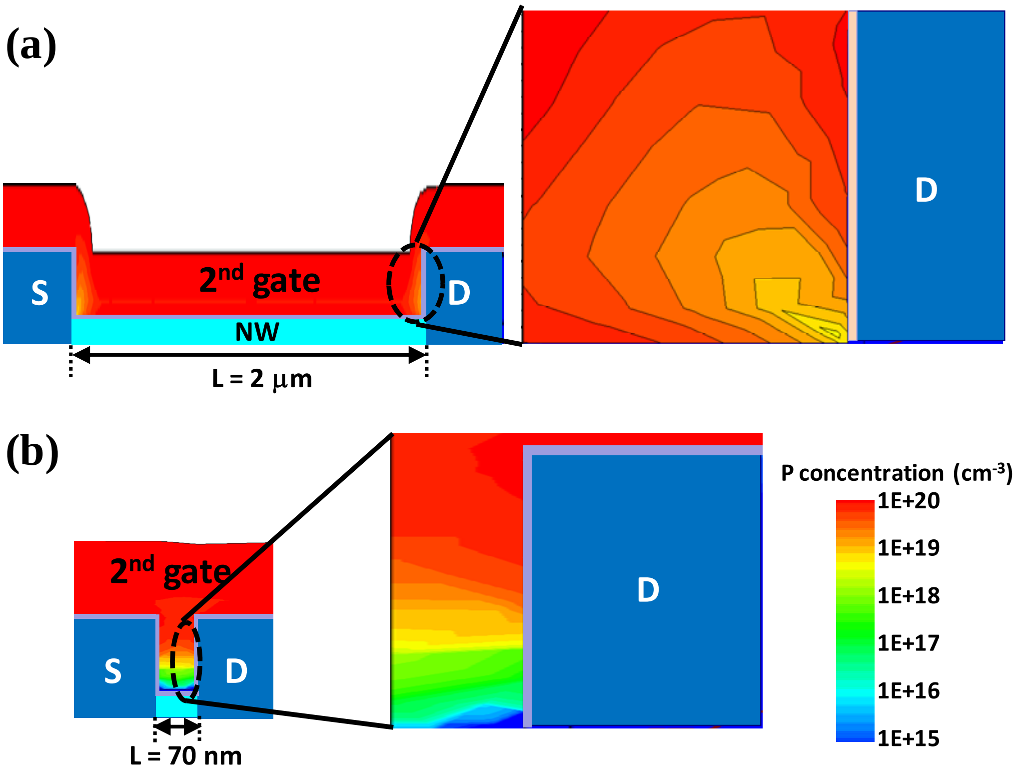


Fig. 4-9 Simulated dopant distribution in an implanted gate corresponding to a device with (a) L = 2 μm and (b) L = 70 nm. It is observed that the bottom portion of the 2nd gate has much lower concentration in (b) than in (a).

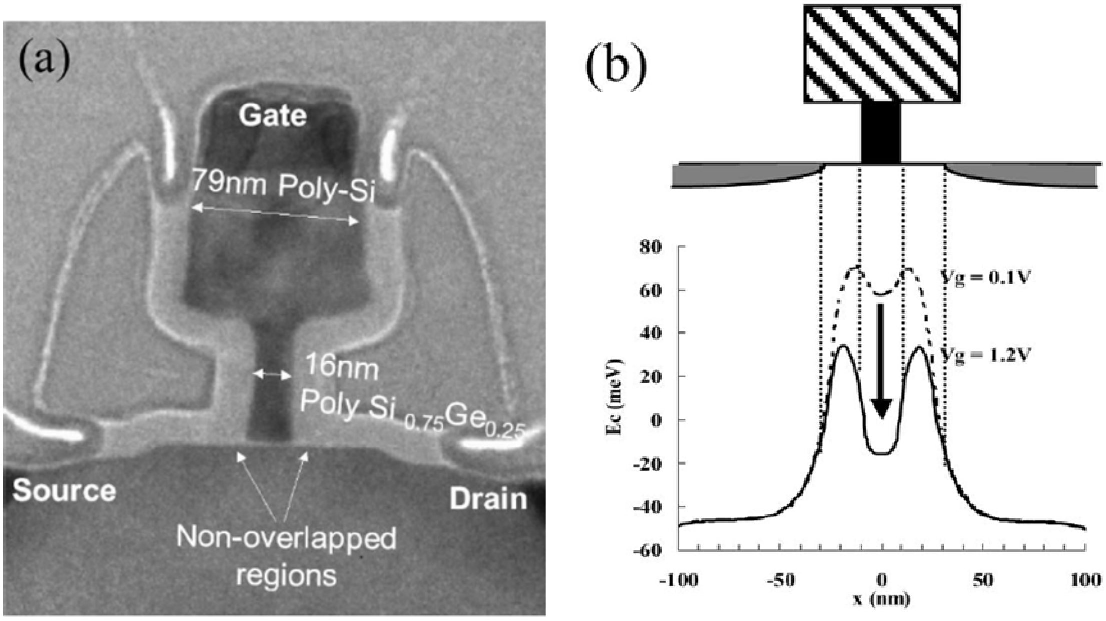


Fig. 4-10 (a) TEM image of a non-overlapped NMOSFET with 16 nm gate length. The notched gate is fabricated by selective etching of poly-SiGe. (b) Simulated electrostatic channel potential profile under two different gate voltages. As the gate voltage is increased, the potential valley drops to a larger extent than the humps in the non-overlapped regions, facilitating the formation of a quantum dot. Adapted from [4-18].

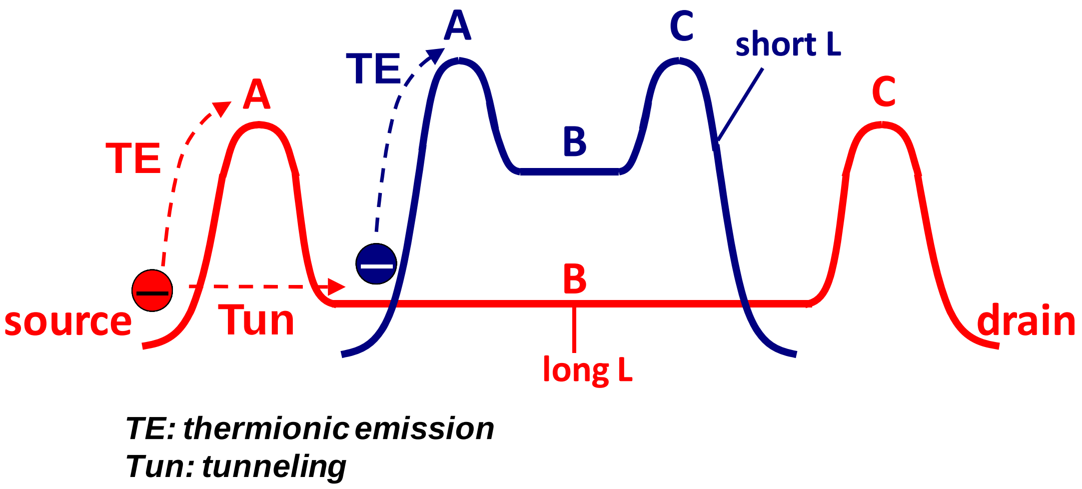


Fig. 4-11 Qualitative band diagrams for devices with long and short L. Points A, B, and C correspond to the regions labeled in Fig. 4-8. For a short channel device, thermionic emission is the dominant transport mechanism while both thermionic emission and tunneling should be considered for a long channel device.

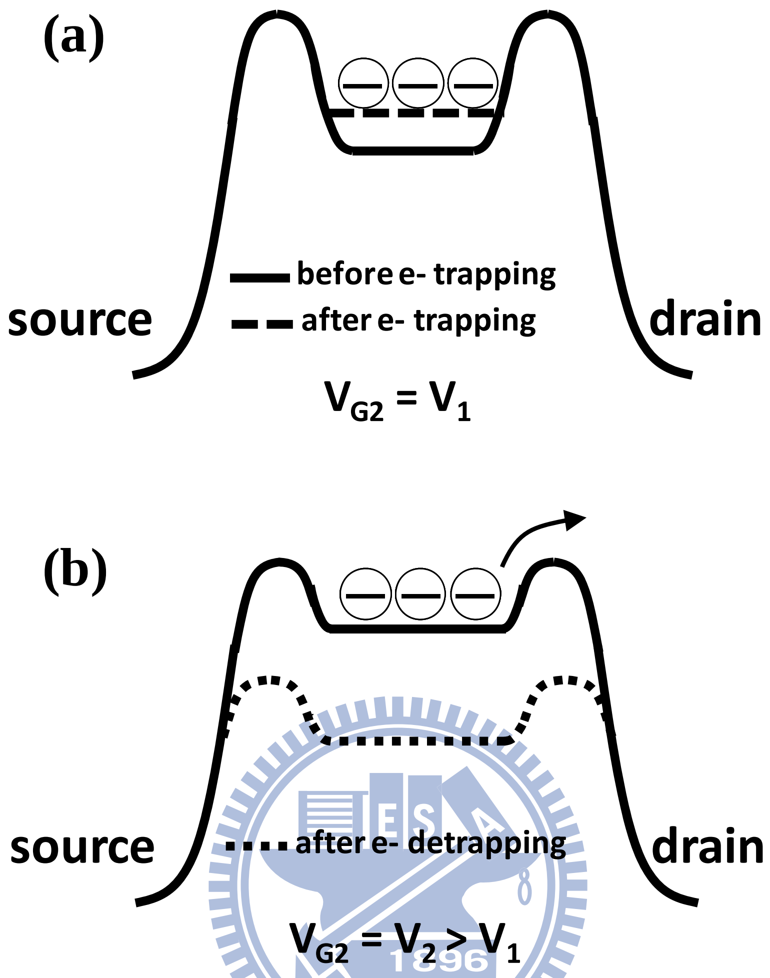


Fig. 4-12 Proposed model for the origin of steep SS. (a) For a low 2nd gate voltage ($V_{G2} = V_1$), after electron trapping in the channel (dashed line), the potential is raised from its original level (solid line), which deters further injection from the source. (b) For a larger 2nd gate voltage ($V_{G2} = V_2$) that considerably reduces the barrier height at drain side, electrons are detrapped and flow to the drain, leading to channel potential drop (dotted line) and an abrupt increase of drain current.

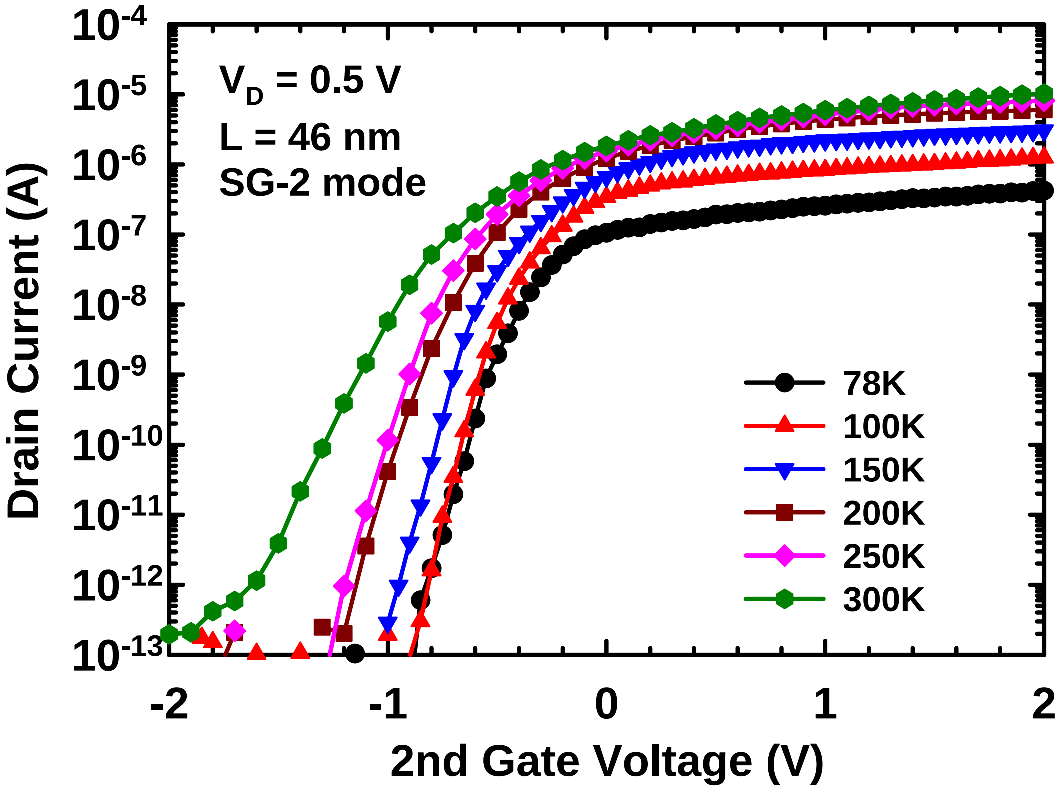


Fig. 4-13 Transfer characteristics as a function of temperature for a device whose 1st and 2nd gates are both *in situ* doped. Compared with Fig. 4-5 (b), steep SS completely vanishes owing to the removal of barriers when very uniform doping concentration throughout the whole 2nd gate electrode is achieved by *in situ* doping.

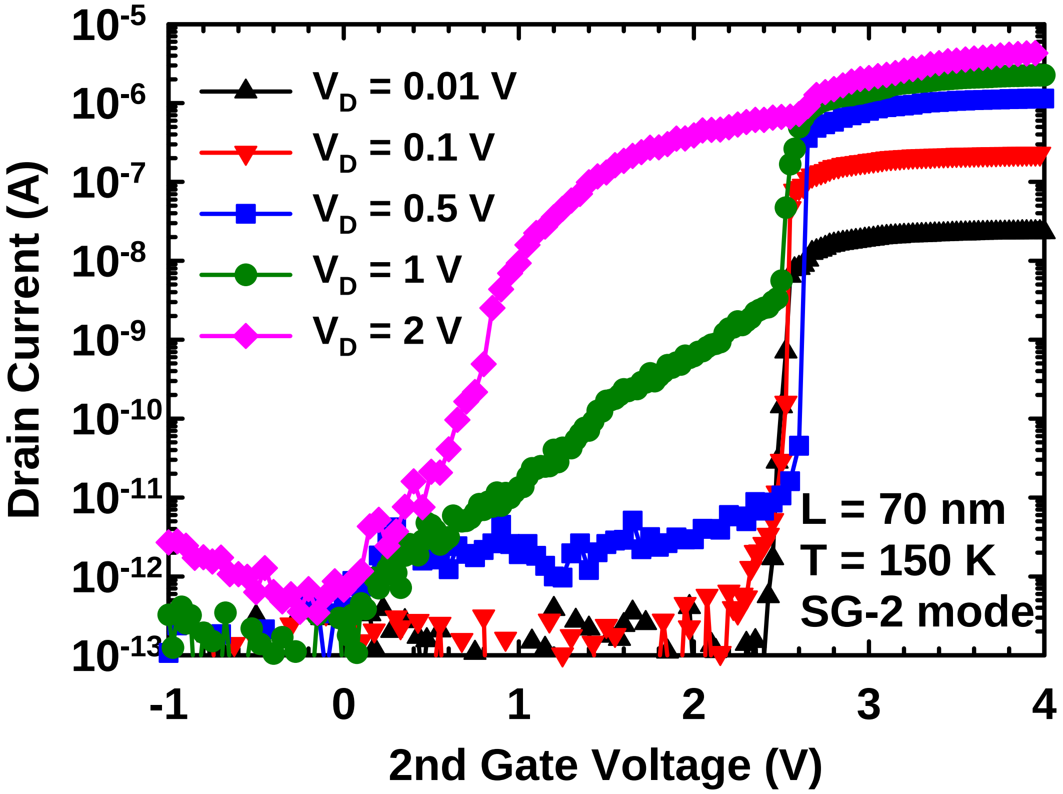
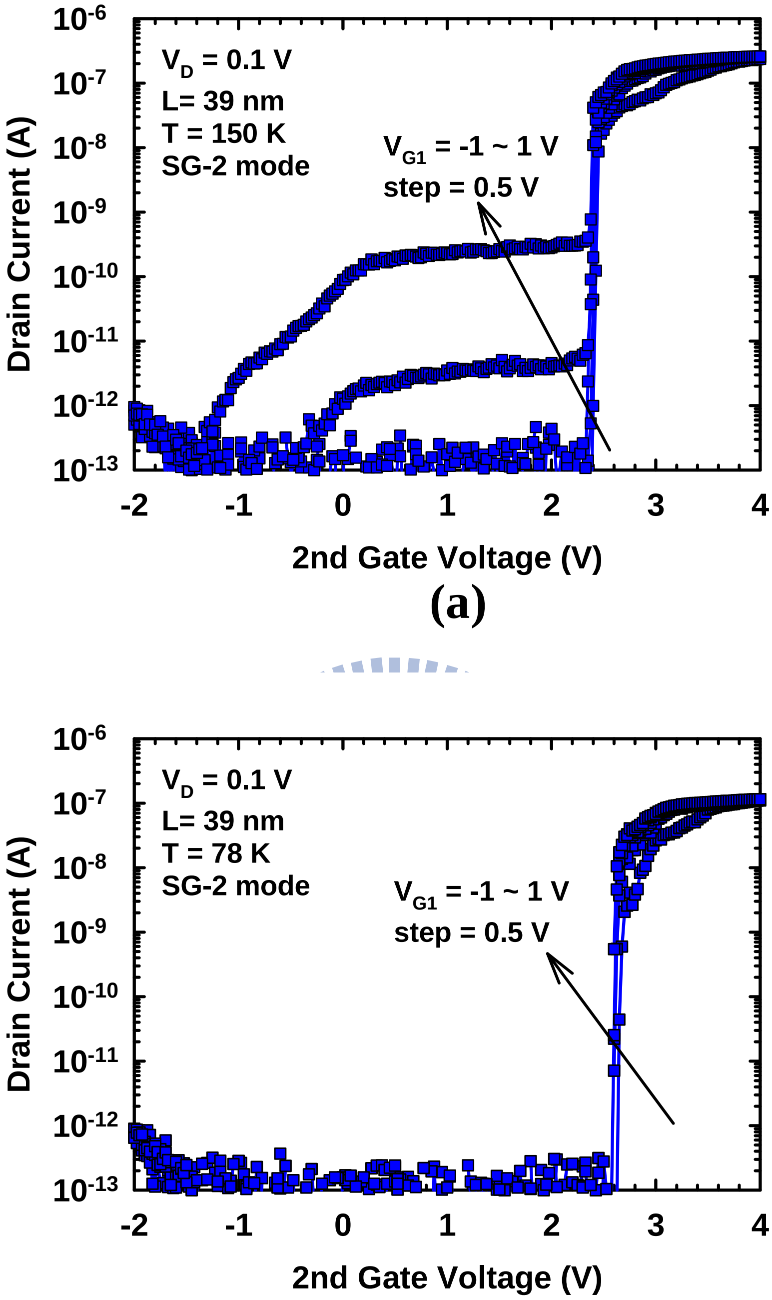


Fig. 4-14 Drain-voltage-dependent transfer characteristics suggest DIBL could eliminate the occurrence of steep SS, in agreement with the proposed model.



(a)

(b)

Fig. 4-15 Transfer characteristics under SG-2 mode for various V_{G1} at (a) 150 K and (b) 78 K. V_{G1} here ranges from -1 V to 1 V in 0.5 V step.

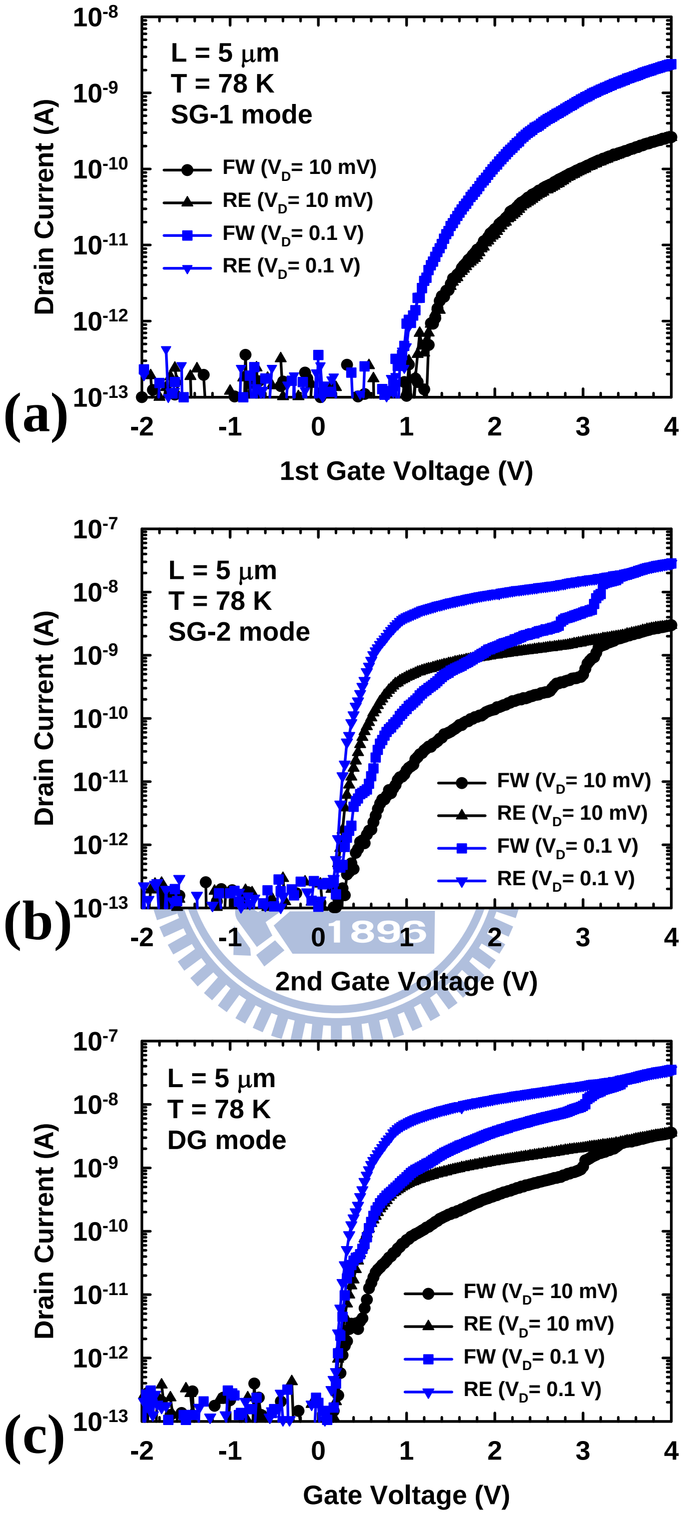


Fig. 4-16 Transfer characteristics for a device with L = 5 μm under forward and reverse sweeping of the gate voltage for (a) SG-1, (b) SG-2, and (c) DG modes.

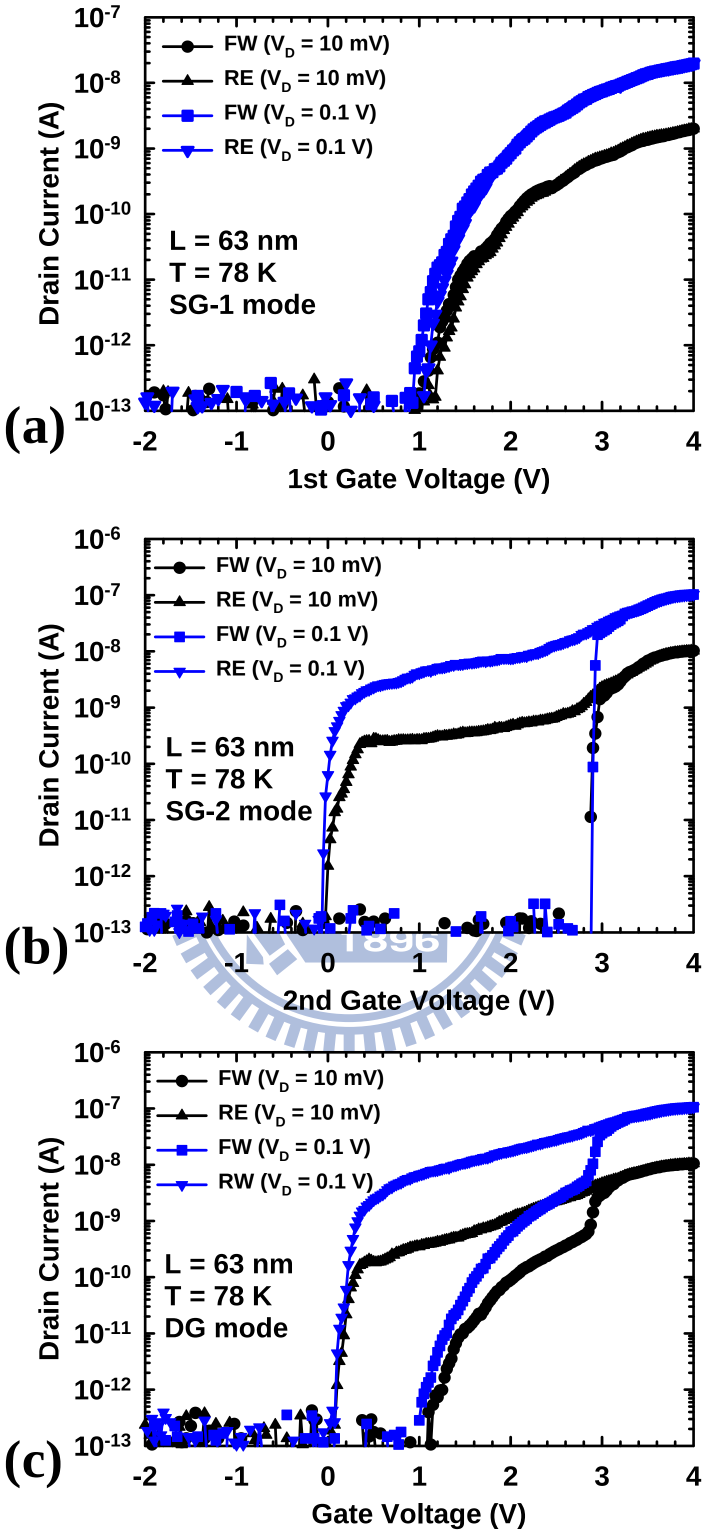


Fig. 4-17 Transfer characteristics for a device with L = 63 nm under forward and reverse sweeping of the gate voltage for (a) SG-1, (b) SG-2, and (c) DG modes.

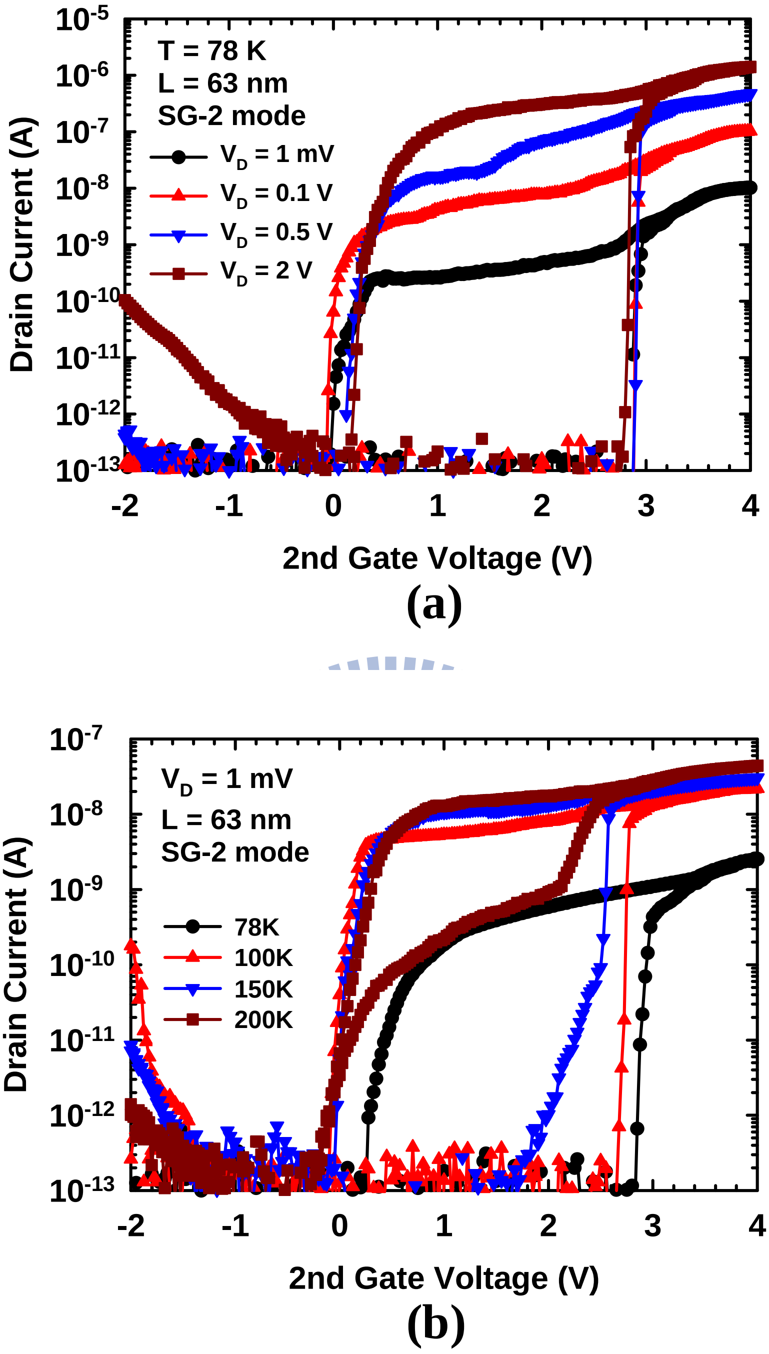


Fig. 4-18 Forward and reverse sweeping of transfer characteristics with (a) the drain voltage and (b) temperature as a parameter.

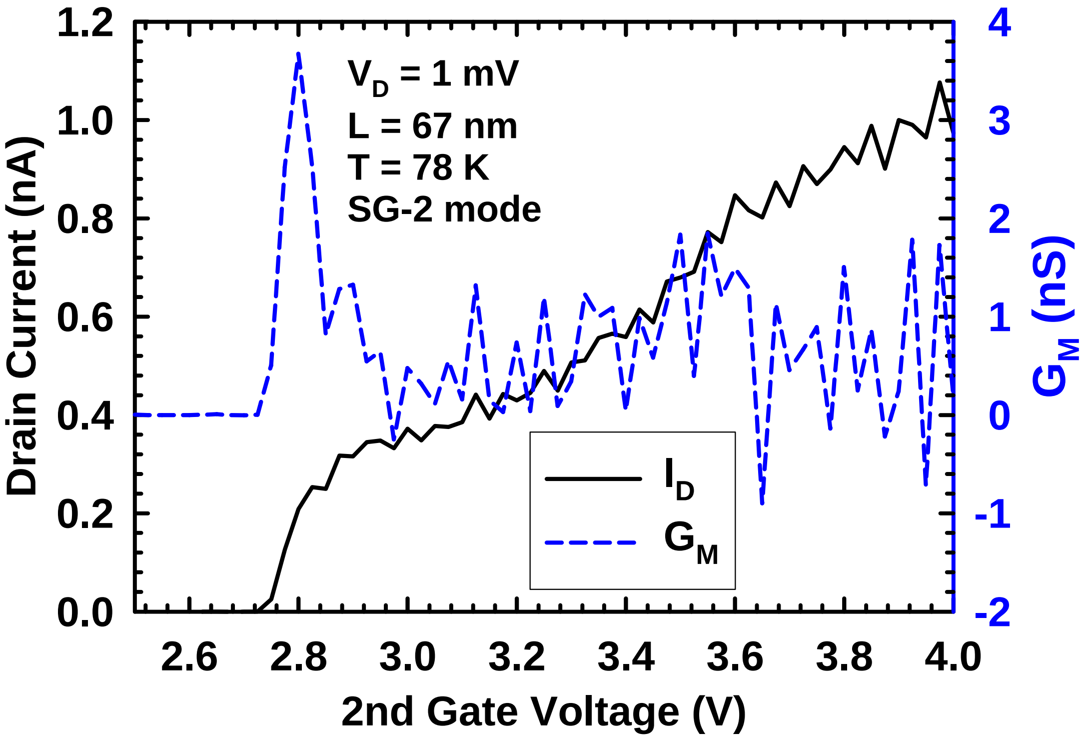


Fig. 4-19 Oscillation of the drain current and resultant G_M at 1 mV V_D.

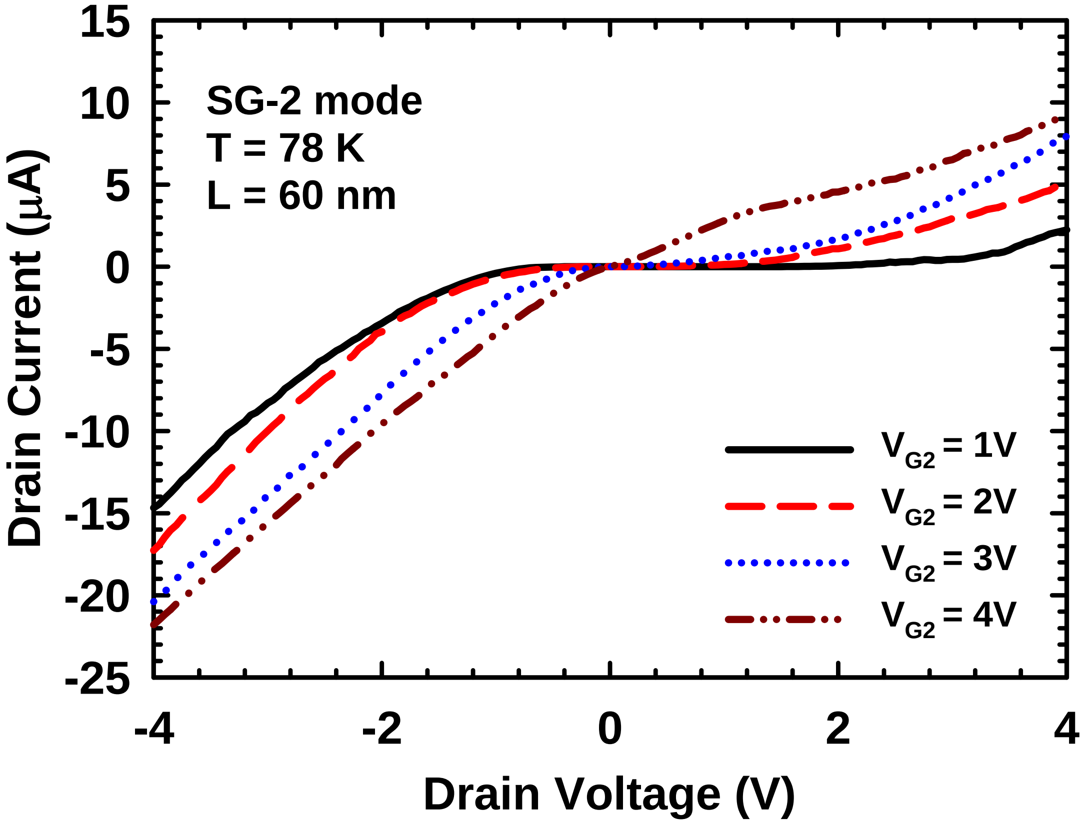


Fig. 4-20 Output characteristics showing a wider current blockade region at a lower gate voltage. Different kink points in the positive and negative drain voltage regime indicate the presence of asymmetric barriers.

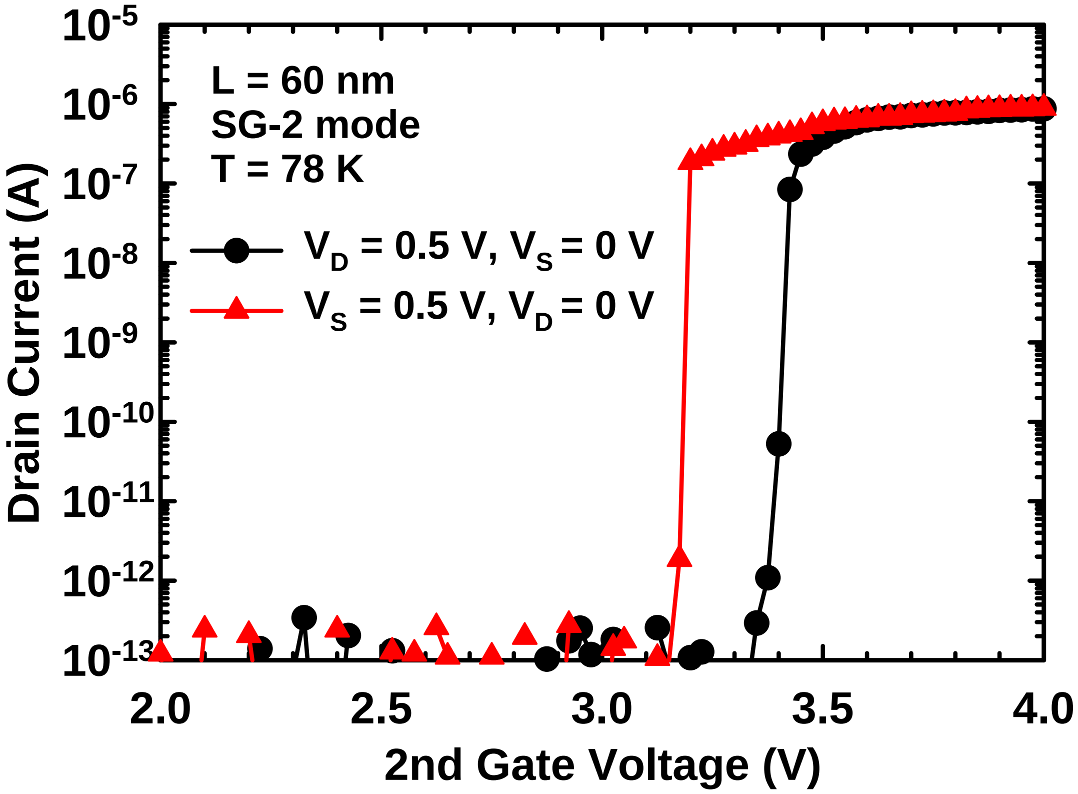


Fig. 4-21 Transfer characteristics measured by interchanging the applied biases to S/D showing two distinct curves, an indication of the asymmetry between source and drain barriers, in agreement with Fig. 4-20.

Chapter 5

Analysis on the Potential of Poly-Si Nanowire Thin Film Transistors Featuring Independent Double-Gated Configuration for Nonvolatile Memory Applications

5.1 Introduction

With ever increasing demand for flash memory products (*e.g.*, cell phones, USB drives, memory cards, *etc.*), cost reduction-oriented memory industries have devoted to circumventing the scaling limit [5-1]. Among the various nonvolatile memory (NVM) architectures, charge-trapping (CT) type device has demonstrated its high performance and strong potential to succeed the conventional floating-gate (FG) type device. Silicon-oxide-nitride-oxide-silicon (SONOS), in particular, has received renewed interests due to its less stringent limitation on the tunneling oxide thickness and stronger immunity against interference coupling [5-2]. Akin to nitride read-only memory (NROM) [5-3], SONOS relies on the nonconductive nitride to trap electrons coming from the channel. In contrast to conductive polycrystalline-Si (poly-Si) used in the FG device, this unique feature helps realize 2-bit/cell functionality by storing electrons at two different sites. In addition to trapping layer engineering, 3D technology is also under the spotlight as it not only is compatible with conventional planar processes by simply adding more layers in the vertical direction, but also greatly improves interconnect density, reduces cost and provides a platform for heterogeneous integration [5-4]. Recent works have demonstrated the feasibility and strong potential of 3D technology in NVM applications [5-5]-[5-7]. It is worth noting that in those 3D stacked structures, poly-Si is adopted for the channel material to avoid the complexity and difficulty in high temperature deposition of single crystalline Si layers. Though grain boundary effects are a concern in poly-Si, poly-Si based thin film transistors (TFTs) with nanowire (NW) channel and multi-gated scheme have been shown to perform comparably to their bulk-Si counterparts [5-8][5-9]. In addition, poly-Si TFTs greatly facilitate the integration of a wide array of circuit components, making possible system-on-panel (SOP) applications [5-10].

Most of the previous works regarding NW SONOS devices put emphasis on tie-gated structures owing to their better gate controllability and simpler fabrication procedure than separate-gated counterparts [5-11]-[5-13]. However, independent double-gated (IDG) type device has started to demonstrate its merits for more flexible operations based on the opposite gate bias effects [5-14]-[5-16]. In light of this and employing a very simple and low cost procedure, we propose an IDG poly-Si NW TFT as SONOS-type memory device in this chapter. It was found that the V_{TH} windows under two feasible read modes (*i.e.*, read by two different gates) show distinctly different dependency on the auxiliary gate (AG) bias. Here, AG refers to the gate with a fixed bias during I-V measurement in contrast to the driving gate. In the following context, we investigate the mechanism leading to different P/E efficiency of the two read modes in detail, discuss the merits of the unconventional read approach and its retention and endurance characteristics. Considering that the device studied in this work is programmed and erased by Fowler-Nordheim (F-N) tunneling, which is compatible with NAND type flash memory, for the purpose of realizing 2-bit/cell feature, ONO stack is used as the dielectrics of both gates.

The content of this chapter is arranged as follows. Section 5.2 gives a brief overview of the P/E operation principles in flash memory. Influence of AG bias on P/E speed is then investigated in Section 5.3. The underlying principle governing the different dependency of V_{TH} window on AG bias under two read modes is discussed in Section 5.4 along with its implications for P/E speed, endurance, and retention characteristics when different read modes are adopted. Section 5.5 demonstrates the proof-of-concept feature of 2-bit/cell functionality for our IDG NW device. Finally, a brief conclusion is drawn in Section 5.6. Through the analysis performed in this chapter, it is believed that the proposed concept will be highly advantageous in facilitating the advancement of 3D high density memory technology.

5.2 Programming and Erasing Operation Principles

Owing to the circuit design and the device wiring structure, NOR type flash memory is programmed by channel hot electron injection (CHEI) and erased by F-N tunneling while NAND type is programmed and erased both by F-N tunneling, as illustrated in Fig. 5-1. Operation features of NAND and NOR flash memory [5-17] are tabulated in Fig. 5-1(c). CHEI, as its name suggests, relies on a large lateral electric field to accelerate electrons to a point that they possess sufficiently high kinetic energy or become hot, which if lucky would then surmount the energy barrier between the gate dielectric and channel and get injected into the floating gate, giving rise to a V_{TH} shift [5-18]. A schematic diagram detailing CHEI is shown in Fig. 5-2. The merits of CHEI include faster P/E speed (as compared with F-N tunneling) and the possibility of realizing multi-bit per cell features for charge-trapping type memory. However, as CHEI is in progress, the oxide field may become repulsive and some or all of the electrons injected could be repelled back into the silicon, resulting in low injection efficiency [5-19]. Furthermore, the damage done to the dielectric is another factor causing concern for the characteristics of cycling endurance, including gate disturb, window opening, and eccentric erase, *etc*. [5-20][5-21]. Scalability is also something that acts as a showstopper for NOR flash. In 45-nm node, self-aligned contact technique has been adopted, but the physical gate length is still 110 nm due to the requirement of the drain voltage being above a certain value for CHEI to occur without inducing significant SCEs [5-22]. Hence, more sophisticated junction engineering and programming scheme needs to be utilized to promote aggressive gate length scaling for NOR flash [5-23].

When F-N tunneling occurs, conducting electrons in the channel tunnel through a triangular potential barrier into the floating gate via quantum mechanical tunneling, as shown in Fig. 5-3. An analytical formula in a simplified form relating the current density to the tunneling width and electric field is given by [5-24]

$$J = \alpha E_{ox}^{2} \exp(-\beta/E_{ox}) \tag{5-1}$$

$$\text{with } \alpha = \frac{m}{m^*}\frac{q^3}{8\pi h}\frac{1}{\Phi_b}, \text{ and}$$

$$\beta = 8\pi\sqrt{2m^*}\frac{\Phi_b^{3/2}}{3hq},$$

where h is the Planck's constant, Φ_b the energy barrier at the injecting surface, q the elemental charge, m the mass of a free electron, m* the effective mass of an electron in SiO_2, and E_{ox} the electric field at the injecting surface. Depending on the magnitude of the applied gate bias or the shape of the energy barrier seen by the carrier, direct tunneling and modified F-N tunneling are two other commonly observed gate tunneling mechanisms in devices with ultra-thin gate dielectric [5-25].

In contrast to CHEI where there is only local injection near the drain end, F-N tunneling accomplishes global write/erasure irrespective of the location. Making use of this non-uniform injection feature of CHEI, NROM with SONOS type structure and 2-bit/cell capability is already in production.

5.3 Merits of Independent Double-Gated Configuration in Enhancing Programming and Erasing Characteristics

Figure 5-4 (a) displays the TEM image of a fabricated IDG poly-Si NW SONOS device. Device fabrication process was elaborated in Chapter 2. Figure 5-4 (b) gives a graphic representation of the composition of the gate dielectrics and the applied biases to the 1st gate (V_{G1}) and 2nd gate (V_{G2}) during I-V measurements. A 12 nm oxide layer and a 3/8/13 nm ONO stack obtained by low pressure chemical vapor deposition (LPCVD) are employed as the dielectrics of the 1st and 2nd gates, respectively. The NW channel thickness is around 14 nm.

V_{TH} shift versus programming time with V_{G1} applied during programming as a parameter is shown in Fig. 5-5(a). Here the device is programmed by applying $V_{G2} = 16$ V and varying V_{G1}, and is read by SG-2 mode with $V_{G1} = 0$ V. Clearly, programming speed is enhanced with larger V_{G1}. This is expected as with thinner channel, there exists stronger gate-to-gate coupling; thus, during programming a positive AG bias can help induce additional number of electrons that are available for tunneling into the nitride layer while a negative one tends to deplete electrons present in the channel. In this regard, the V_{TH} shift for a given programming time in Fig. 5-5(a) is seen to increase with the applied AG bias. Figure 5-5(b) shows the corresponding transfer curves illustrating the influence of AG bias on programming efficiency. The effect of AG bias on erasing speed is also explicit in Fig. 5-6(a). Under the erasing scenario, electrons originally trapped in the nitride would be detrapped into the channel and flow to the grounded source/drain. A larger AG bias facilitates this out-draining process by forming an inverted channel to reduce the channel resistance experienced by the detrapped electrons, which is consistent with the scheme in [5-26] where a back-gate bias whose value is larger than V_{TH} of the back channel is applied to erase the front side charges. IV characteristics from which Fig. 5-6(a) is extracted are displayed in Fig. 5-6(b).

5.4 Concept of an Unconventional Read Scheme and Interpretation

5.4.1 Description of Principles

Figures 5-7 (a) and (b) show the resultant transfer curves for SG-1 and SG-2 modes with varying AG bias under P/E states. Here the AG bias ranges from -2 V to 4 V in 1 V step. Regardless of the read mode, a programmed device refers to one in which electrons tunneling from the NW body via F-N tunneling are trapped in the nitride layer of the 2nd gate dielectric; for an erased device, some portions of those trapped electrons are removed through tunneling back into the NW body, which then flow to the source and drain. In Fig. 5-7(a), the device is first programmed by applying V_{G1} = 0 V and V_{G2} = 16 V for 10 ms, after which the I_D-V_{G1} transfer curves are measured withV_{G2} as a parameter resulting in the curves shown as blue circles. Afterwards, V_{G1} = 0 V and V_{G2} = -12 V are applied for 100 ms to erase the device, and the I_D-V_{G1} transfer curves are again measured with V_{G2} as a parameter, giving rise to those shown in red triangles. The results in Fig. 5-7(b) were obtained in a similar manner except that during the I-V measurements, the roles of the 1st and 2nd gates are exchanged compared with those in Fig. 5-7(a).

Defining V_{TH} as the driving gate voltage when the drain current reaches 10 nA, it can be seen from Fig. 5-7 (b) that when the device is driven by the 2nd gate with ONO stack in SG-2 mode (*i.e.*, the conventional approach), the extent of V_{TH} distribution with respect to AG bias is similar in both P/E states. In stark contrast, V_{TH} of SG-1 mode (*i.e.*, the unconventional approach) is much less dependent on the AG bias in the programmed than the erased states. V_{TH} versus AG bias in P/E states corresponding to SG-1 and SG-2 modes is extracted on the left vertical axis of Figs. 5-8 (a) and (b), respectively. V_{TH} window, the difference between V_{TH} of P/E states, is also displayed in

Figs. 5-8 (a) and (b) on the right vertical axis. One can see that V_{TH} window under SG-1 mode shows a sudden increase for AG bias larger than 2 V whereas that of SG-2 mode is fairly independent of AG bias.

Qualitatively speaking, this discrepancy of V_{TH} window between two modes is caused by the location of storage charge relative to the driving gate. If the AG is the one with ONO stack, *e.g.*, the 2nd gate, then the trapped electrons in the nitride layer provide screening from the electric field penetration of the AG. Thus, the AG bias has weak influence on the channel potential and V_{TH} is independent of the AG bias in the programmed state. From another perspective, for a sufficiently positive AG bias, inversion would first occur at the channel surface near the AG and the read gate only slightly perturbs the already conducting channel. The effective gate capacitance is now composed of serial oxide and channel capacitance and is lower than the oxide capacitance alone. Hence, the read gate has less control on the channel and the V_{TH} window is enlarged as the AG bias is increased, which could be vividly evidenced by the extremely small V_{TH} of the erased states with V_{G2} above 3 V in Fig. 5-7(a).

Besides qualitative explanation, the aforementioned phenomena can be described in a more quantitative way using the back-gate effects in [5-27]. The V_{TH} adjustment rate by the back gate, the so-called back-gate factor (γ), strongly depends on the condition of the back gate/channel interface where there is a transitional point demarcating two piecewise linear V_{TH}-versus-back-gate-bias curves corresponding to the condition of depletion and inversion of the back surface. Inversion would take place first at the front or back surface for back-gate bias below or larger than this point. As a matter of fact, the back-gate bias of that point where the slope changes is the V_{TH} of the back surface. Calculated by the least squares fitting, the slope for each operation regime is indicated in Fig. 5-8. For the case considered, the AG assumes a role similar to that of the back gate. In SG-1 mode, the back interface is controlled by the 2nd gate so when the nitride is trapped with electrons in the programmed state, the transitional point shifts to a larger value compared with the erased situation. The curve of V_{TH} against AG bias then mainly shows a horizontal shift as depicted in Fig. 5-8(a). Even though this curve does not display a specific point where an obvious change in slope occurs, this point is believed to lie outside the range of the applied V_{G2} and will appear if the value of V_{G2} is further increased. A rather minor vertical shift can occur because the trapped electrons may still slightly affect the electrostatics of the front surface. On the contrary, the V_{TH}-V_{G2} curve for the erased state in Fig. 5-8(a) exhibits an evident transitional point separating two piecewise linear curves whose respective γ are 0.49 V/V and 3.18 V/V. Thus, an AG bias range rendering back surface inverted in the erased state but only depleted in the programmed state (V_{G2} within the range from 2 V to 4 V) will increase the V_{TH} window in a linear manner. A similar theory can be applied to SG-2 mode except the back surface is now essentially unchanged between P/E states, and the V_{TH} against AG bias curve shifts upward as a whole. The V_{TH} window then shows insignificant variation in the characterized AG bias range. The above statement is clearly illustrated in Fig. 5-8(b) where one can see that regardless of the state of the device (*i.e.*, programmed or erased), the γ values for the two piecewise linear curves are identical. However, as for Fig. 5-8(a), γ is 0.28 V/V in the programmed state and is smaller than that in the corresponding regime for the erased state, which is 0.49 V/V. This discrepancy is believed to be caused by the fact that for the applied V_{G2} bias range under SG-1 mode in the programmed state in Fig. 5-8(a), the device may have entered into the accumulation situation instead of depletion [5-28].

5.4.2 On Programming/Erasing Efficiency

To further probe the impact of such an intriguing effect, the result of P/E speed characterization will next be compared between the two feasible read modes. It should be noted first that F-N tunneling is utilized to program and erase the device in this work by applying appropriate biases to the 1st and 2nd gates while the source and drain are grounded. Programming speed is first depicted in Fig. 5-9 where for a given programming condition the characteristics of both SG-1 and SG-2 modes are measured from the same device. Here the respective AG biases for SG-1 and SG-2 modes are V_{G2}

= 3 V and V_{G1} = 0 V since these conditions have comparable V_{TH} window from Figs. 5-7(a) and (b), and there are two sets of programming conditions utilized in Fig. 5-9 (V_{G1} = 0 V/V_{G2} = 14 V and V_{G1} = 0 V/V_{G2} = 18 V). It can be observed that the V_{TH} shift as read by SG-1 mode with V_{G2} = 3 V is appreciably larger than that of SG-2 mode with V_{G1} = 0 V for at least up to 20 msec of programming time. For the programming condition of V_{G1} = 0 V/V_{G2} = 18 V applied for 10 μs, the V_{TH} shift in SG-1 mode is 3.61 V compared with 2.24 V in SG-2 mode, amounting to 61 % enhancement in programming speed. On the other hand, for the erasing speed in Fig. 5-10, a markedly different trend is obtained. As opposed to the gradually decreasing V_{TH} in SG-2 mode, SG-1 mode does not exhibit any V_{TH} alteration until around 10 msec, and then a rapidly decreasing rate of V_{TH} value is attained when read by SG-1 mode with V_{G2} = 3 V, reaching even smaller V_{TH} over SG-2 mode at 1 sec. In fact, the root cause for such dissimilar P/E speed behavior can be interpreted based on the back-gate effects as well. As illustrated in Fig. 5-11, the initial states before P/E stressing are a fresh (solid line in Fig. 5-11(a)) and pre-programmed (by applying V_{G1} = 0 V and V_{G2} = 16 V for 10 msec; dotted line in Fig. 5-11(b)) device, respectively, for which a V_{G2} bias of 3 V corresponds to the condition of inversion and depletion (or even accumulation from Fig. 5-8 (a)) of the surface adjacent to the 2nd gate. Dotted line in Fig. 5-11(a) indicates the V_{TH}- V_{G2} curve when the device has been programmed; while solid line in Fig. 5-11(b) represents the V_{TH}- V_{G2} curve when the device has been erased for a particular duration such that the surface governed by the 2nd gate for $V_{G2} = 3$ V is still in the depletion regime.

The V_{TH} difference of two intersection points determined by the arrow and two V_{TH}- V_{G2} curves in Figs. 5-11(a) and (b) is by definition the programming and erasing speed, respectively. It is obvious that the programming speed is much faster than the erasing speed, which can be interpreted as follows. A V_{G2} bias of 3 V that originally inverts the 2nd gate surface for a fresh device would result in the depletion of the 2nd gate surface instead when the device is programmed in Fig. 5-11(a). On the other hand, the 2nd gate surface is always depleted for $V_{G2} = 3$ V for both pre-programmed and erased states in Fig. 5-11(b). Accordingly, a small shift of the V_{TH}- V_{G2} curve in SG-1 mode will cause a decent shift during programming, whereas there will not be any significant V_{TH} shift during erasing until the device is sufficiently erased to the extent that $V_{G2} = 3$ V inverts the surface controlled by the 2nd gate. Considering that the magnitude of γ is strongly related to the chosen operation regime as discussed previously, it is then reasonable to initially observe faster programming yet slower erasing speed for the unconventional read method as compared with the conventional one. This also explains the erasing speed as read by SG-1 mode is enhanced with a larger V_{G2} in Fig. 5-10 since inversion would be reached earlier by a larger V_{G2} in a given erasing time. And the root cause leading to SG-1 mode displaying a faster initial programming speed than that of SG-2 mode in Fig. 5-9 is related to the chosen AG bias of SG-1 mode ($V_{G2} = 3$ V) situated in a regime yielding a large γ in the fresh state, so much so that a more sizable V_{TH} shift between the fresh and programmed state can be attained in SG-1 mode.

5.4.3 On Endurance Characteristics

Characteristics of cycled endurance are displayed in Fig. 5-12. It should be pointed out that the results in Figs. 5-12(a) and (b) correspond to two different devices with almost identical initial characteristics. Figure 5-12(b) suggests that the conventional read method is more stable in terms of the V_{TH} variation at the erased state, as evidenced by the large fluctuation of that of the SG-1 mode. One possible cause for V_{TH} variation during cycling is the generation of interface charges which then induces SS degradation. Nonetheless, as shown in Figs. 5-13(a) and (b) plotting the evolution of transfer curves with of the number of cycles as a parameter, there is no significant SS degradation for both read modes as endurance measurement proceeds. Moreover, even if the influence of interface charges cannot be neglected, the extent of V_{TH} variation ought to be milder for SG-1 mode which can be explained as follows. At the erased state where inversion channel forms at the 2nd gate side regardless of the read mode, the equivalent oxide thickness (EOT) of the gate dielectric for SG-2 mode with $V_{G1} = 0$ V and SG-1 mode with V_{G2} = 3 V are 20.4 nm (3/8/13 nm of ONO stack) and 16.5 nm (12-nm oxide and 14-nm Si body), respectively. Fundamental device physics dictate that SS is proportional to $(1+\frac{C_{dep}+C_{it}}{C_{OX}})$ where C_{dep}, C_{it}, and C_{OX} are the respective values of capacitance per unit area for the depletion layer, interface charges and gate dielectric [5-29]. In particular, C_{it} is directly related to the density of states for interface charges D_{it} (in cm^{-2} eV^{-1}) in the form of $C_{it} = q^2 D_{it}$ [5-30]. Then for a given D_{it} created by the cycling stress, it is apparent that the degree of SS enlargement (= $\frac{C_{it}}{C_{OX}}$) is more severe for SG-2 mode with V_{G1} = 0 V than SG-1 mode with V_{G2} = 3 V. In other words, interface charges alone would lead to larger V_{TH} fluctuation for SG-2 mode, which obviously is not the case in Fig. 5-12. In this regard, interface charges should not be the major culprit for V_{TH} variation.

Based on the above discussion, it is thus speculated that unequal amount of charges trapped or detrapped between each cycle accounts for the results in Fig. 5-12, which is also able to readily explain the origin of large V_{TH} alteration at the erased state in SG-1 mode. Consider the schematic diagram in Fig. 5-14 in which the thicknesses of blocking oxide, nitride, and tunnel oxide are T_{OX1}, T_N, and T_{OX2}, respectively. For simplicity, suppose that the sheet trapped electron charge density Q_{tot} (in cm^{-2}) in the erased state is located in the middle of the nitride layer [5-31][5-32]. Then the flat-band voltage difference between the erased and fresh state can be expressed as Eq (5-2) *under SG-2* *mode*.

$$\Delta V_{FB}\,|_{SG-2} = Q_{tot}\left(\frac{T_{OX1}}{\varepsilon_0 \varepsilon_{OX}} + \frac{T_N}{2\varepsilon_0 \varepsilon_N}\right), \tag{5-2}$$

where ε_0 is the vacuum permittivity, ε_{OX} and ε_N are the dielectric constants for oxide and nitride, respectively.

If now the density of trapped charge for a particular cycle is altered by an amount of ∂Q_{tot}, the shift of flat-band voltage at the erased state under SG-2 mode compared with Eq (5-2) would be

$$\partial(\Delta V_{FB})\,|_{SG\text{-}2} = \partial Q_{tot}\left(\frac{T_{OX1}}{\varepsilon_0 \varepsilon_{OX}} + \frac{T_N}{2\varepsilon_0 \varepsilon_N}\right). \tag{5-3}$$

That being said, for the erased state under SG-1 mode, the V_{TH}-versus-V_{G2} curve when considering the inhomogeneous trapping/detrapping can be plotted as shown in Fig. 5-15. The two solid curves correspond to the situation when different quantity of Q_{tot} is present in the device under the erased state. The transition point where the slope changes for each curve would then be horizontally shifted by an amount equal to $\partial(\Delta V_{FB})\,|_{SG-2}$ while keeping the slope of the right portion constant. Therefore, it is apparent from Fig. 5-15 that the corresponding V_{TH} shift at the erased state of SG-1 mode ($\Delta V_{TH}\,|_{SG-1}$) owing to this effect is equal to the value of $\partial(\Delta V_{FB})\,|_{SG-2}$ multiplied by the back-gate factor (= |-3.18V/V|). Here ∂Q_{tot} is assumed to be small enough so that the 2nd-gate-controlled side of channel remains strongly inverted. Hence at the erased state, the impact of unequal charges remaining within the nitride between each cycle would be enhanced in SG-1 mode, accounting for the much more serious V_{TH} variation in Fig. 5-12(a). Although SG-1 mode would suffer the same effect in the programmed state, the extent of variation in V_{TH} would be less severe for the back-gate factor in this case which is smaller than unity (= |-0.28 V/V|) as can be seen in Fig. 5-8(a). In other words, the V_{TH} at the programmed state ought to be more tightly distributed in SG-1 than SG-2 mode. However, the V_{TH} shift between the 1st and 10,000th cycle in the programmed state is smaller for SG-2 than SG-1 mode, which leads us to believe that mechanisms other than irregular trapping/detrapping are in play during programming. More statistical data analysis would be needed to clarify the exact cause.

Nevertheless, V_{TH} window of 2.4 V can still be maintained after 10^4 cycles for SG-1 mode. The V_{TH}-variation-magnifying issue mentioned above is expected to be relieved by optimization of process conditions, particularly the thickness of NW body, and dielectrics of the 1st and 2nd gate such that the back-gate factor is below a specific value dictated by the requirement of endurance while still being sufficiently large for attaining a decent memory window.

One thing to note is that as has been demonstrated in the previous section, the values of applied biases for programming and erasing are not optimized in the above discussion. That is, the programming/erasing speed and V_{TH} window presented hereinbefore are just for proof of concept and only serve as a preliminary assessment of the true potential the proposed technique has to offer. In addition, though our device is based on poly-Si, the underlying principle applies equally well to single-crystalline Si counterparts.

5.4.4 On Retention Characteristics

Figure 5-16 shows the baked retention characteristics of two read approaches. The initial V_{TH} windows are 2.6 V and 3.5 V for SG-2 mode and SG-1 mode, respectively, and shrink to 0.5 V and 1.8 V after 10-year-extrapolation. The V_{TH} reduction rate within 10^4 sec in the programmed state of SG-2 mode from 6.7 V to 5.8 V is larger than that of SG-1 mode, which is from 2.1 V to 1.6 V. It is so as in SG-1 mode with $V_{G2} = 3$ V, the effective capacitance between the stored charges and the inverted channel consists of a serial combination of tunneling oxide and NW body, which is smaller than tunneling oxide alone in SG-2 mode. Hence, identical amount of charge loss in the programmed state leads to less V_{TH} lowering in SG-1 mode. For the erased state, inversion tends to occur first at the 2nd gate/channel interface for both modes, so that comparable amount of V_{TH} uprising is obtained, *i.e.*, 0.3 V and 0.2 V for SG-1 and SG-2 modes, respectively.

From another viewpoint, the same principles as employed in the last section on endurance characteristics could also be used to interpret the retention behavior. First, when the device is programmed, the back-gate factor for SG-1 mode with $V_{G2} = 3$ V is lower than unity; thus, its V_{TH} variation is less serious than that of SG-2 mode. On the other hand, when the device is erased, the back-gate factor for SG-1 mode with $V_{G2} = 3$ V is raised to |-3.18 V/V|. In this regard, it is expected that there would be a greater degree of V_{TH} shift in SG-1 mode than that in SG-2 mode.

In fact, as the back-gate effects in [5-27] only offer a semi-quantitative way of explaining our device characteristics, a more accurate analytical model would be needed to gain a comprehensive insight into the origins of V_{TH} evolution during endurance and retention characterization.

As a brief summary of this section, simple and straightforward as the concept looks, this is the first time that such a scheme is used to help improve the performance of an NVM device, including the programming speed and retention characteristics. Although the erasing speed is degraded initially for the unconventional read approach, it is believed that this issue could be ameliorated by adjusting the value of γ so that the point where the V_{TH} starts to show a decent shift occurs earlier.

5.5 2-Bit/Cell Feature

To realize 2-bit/cell functionality in the proposed IDG NW device, 3/8/12 nm and 3/8/13 nm of ONO layers are used as the dielectrics for the 1st and 2nd gates, respectively. To minimize bit-to-bit coupling effects, the device used for 2-bit/cell measurement is with 50-nm-thick NW channels. With regard to the denomination of two bits, the bits stored in the nitride of the 1st and 2nd gates are referred to as bit-1 and bit-2, respectively, as illustrated in Fig. 5-17(a). Meanwhile, the programmed state is designated as “1” state and erased state as “0” state. As an example, state-11 indicates one in which bit-1 and bit-2 are both programmed simultaneously by applying gate voltage stress $V_{G1} = V_{G2} = 16$ V for 5 ms so that nitride layers in both 1st and 2nd gate dielectrics are trapped with electrons. State-10 is attained by erasing bit-2 from state-11 (i.e., removing electrons stored in the nitride of the 2nd gate dielectric) using the stress condition of $V_{G1} = 0$ V and $V_{G2} = -14$ V for 20 ms. By the same token, state-01 and -00 are accomplished by erasing bit-1 and bit-1&2, from state-11 through applying $V_{G1} = -14$ V and $V_{G2} = 0$ V for 20 ms, and $V_{G1} = V_{G2} = -14$ V for 20 ms, respectively. Characteristics of these four distinguishable states are shown in Fig. 5-17(b). The AG bias is 0 V for all the read modes in this section. V_{TH} difference between state-11 and state-00 is 5.3 V. The read mode assigned for each state is determined by first measuring each state with both modes and then choosing the one that maximizes the V_{TH} difference between each state. From another viewpoint, since in the fresh state SG-1 mode (with the AG bias $V_{G2} = 0$ V) already yields a higher V_{TH} than that of SG-2 mode (with the AG bias $V_{G1} = 0$ V) due to the inherent asymmetry of the proposed device, it is then reasonable that with the aim of enlarging the V_{TH} sensing window, SG-1 mode is to be used for reading out state-11 whereas SG-2 mode is for state-00. As for state-10 and state-01, unlike in [5-27] where an intentionally-formed asymmetric structure consisting of two gates with different work functions is exploited to differentiate state-10 from state-01, the device proposed in this dissertation is inherently asymmetric in terms of the controllability over channels offered by the two independent gates. Thus, SG-1 and SG-2 modes are directly applied to read out state-10 and state-01, respectively. P/E disturbance characterization shown in Fig. 5-18 suggests that decent P/E speed can be achieved without significantly altering the state of the other bit.

5.6 Summary

To sum up, impacts of IDG scheme on a poly-Si NW NVM device are comprehensively analyzed in this chapter. The origin of the varying V_{TH} window dependency on AG bias is investigated and is found to be a consequence of the back-gate effects. The same effect also explains distinct P/E efficiency for the two read methods where it is observed that the unconventional one yields a larger V_{TH} shift within the first 20 msec over the conventional one when being programmed while no significant V_{TH} shift is attained when being erased until 10 msec. Retention characterization suggests that the unconventional read mode is less vulnerable to V_{TH} window shrinkage. P/E speed is seen to be improved as the applied AG bias becomes larger, which is due to the increased number of electrons available for tunneling into the nitride and reduced channel resistance experienced by the detrapped electrons under programming and erasing scenarios, respectively. Using ONO as the dielectrics for both gates, 2-bit/cell feature can be realized with 5.3 V V_{TH} difference between state-11 and state-00.

In addition to the aforementioned features, IDG scheme could also eliminate the necessity of applying an extremely large voltage to pass transistors in a series string that is typically required to ensure sufficient read current. This merit also greatly relaxes the stringent requirement that the maximum V_{TH} after programming be safely lower than the read-pass voltage [5-33]. Moreover, with the aid of process modifications, the proposed concept could also be adopted in devices that are constructed in a vertical scheme.

It should be remarked that the P/E speed in this work is far from being optimized. Yet the fabricated device is a test vehicle that is highly beneficial for understanding the characteristics of SONOS under IDG operation. With further optimization of structural parameters to adjust γ for improving the initially retarded erasing speed of the unconventional read approach and the unstable V_{TH} distribution during cycling, the proposed concept combined with the TFT structure appears to be very promising for 3D stacked high density memory applications.

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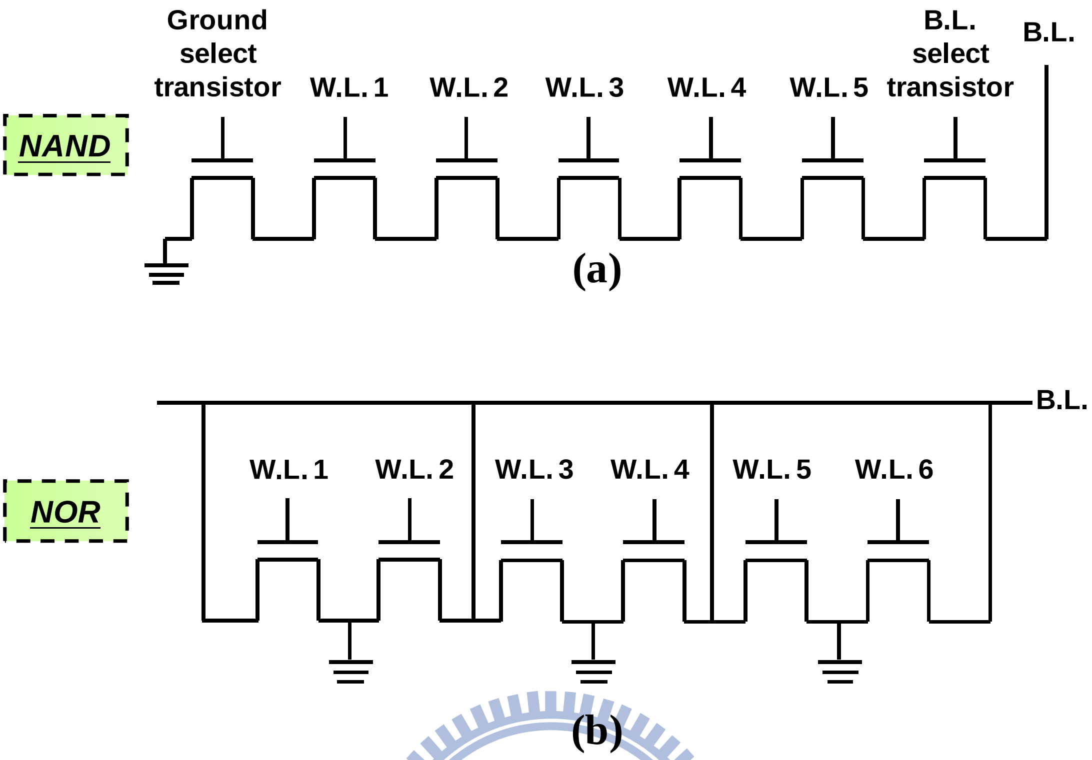

	Cell Size	Read Time	Write/Erase Time	Retention	Write Cycles	Write/Read Voltage
NAND	$5F^2$	50ns	1ms/0.1ms	>10yr	10^5	15V/2V
NOR	$10F^2$	10ns	1μs/10ms	>10yr	10^5	12V/2V

(c)

Fig. 5-1 Wiring of (a) NAND and (b) NOR flash memory. (c) Major operation features of NAND and NOR flash memory [5-17].

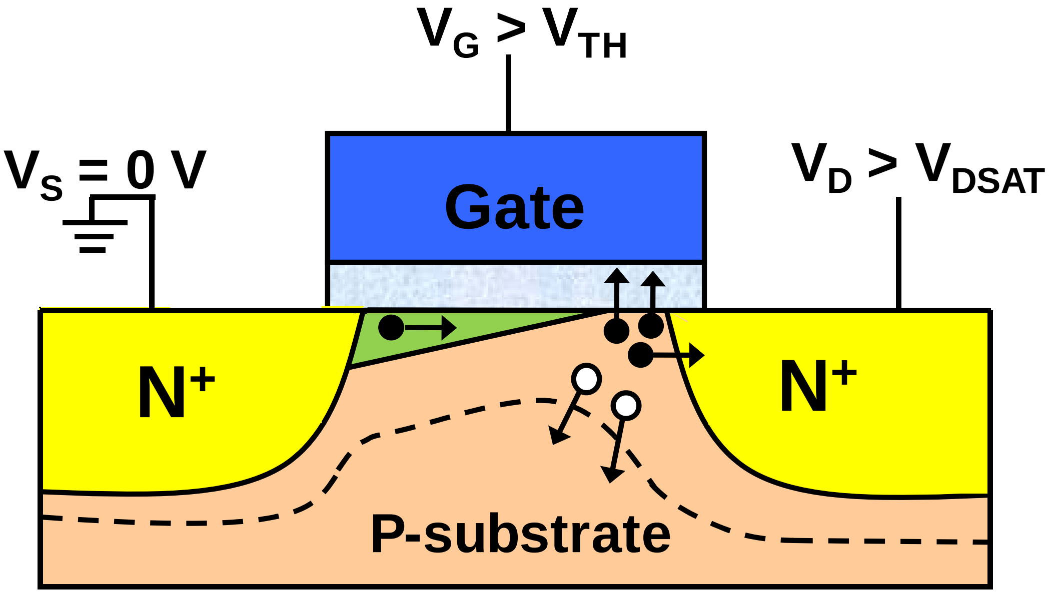

Fig. 5-2 Schematic diagram illustrating CHEI. The filled and hollow dots represent electrons and holes, respectively. Electrons in the inversion channel would be accelerated by the applied high drain bias and absorb significant amount of kinetic energy especially in the pinch-off region near the drain side where strong lateral electric field exists. Those "hot" electrons along with secondary electrons created by the impact ionization would then be injected into the gate dielectric provided they are "lucky" enough.

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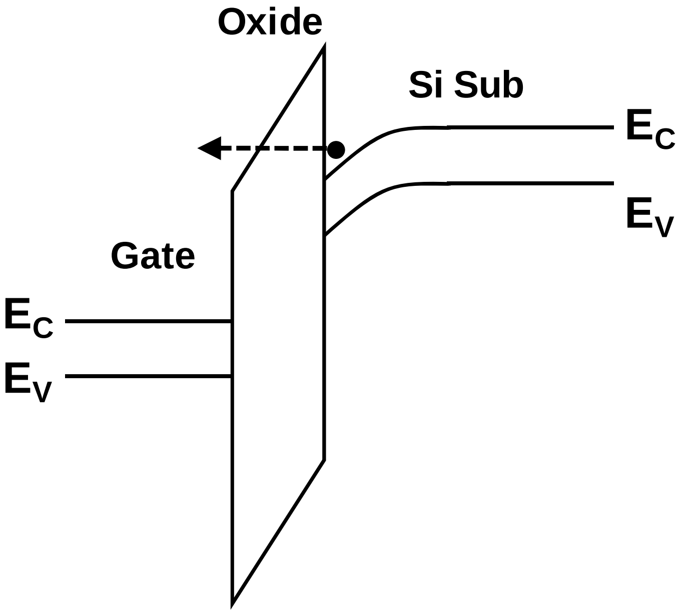


Fig. 5-3 An energy band diagram illustrating F-N tunneling. When a positive gate voltage bias is applied such that the voltage drop across the oxide is larger than the conduction band offset between Si substrate and the oxide, mobile electrons in the conduction band of Si see a triangular-shaped energy barrier and may tunnel through the oxide into the gate.

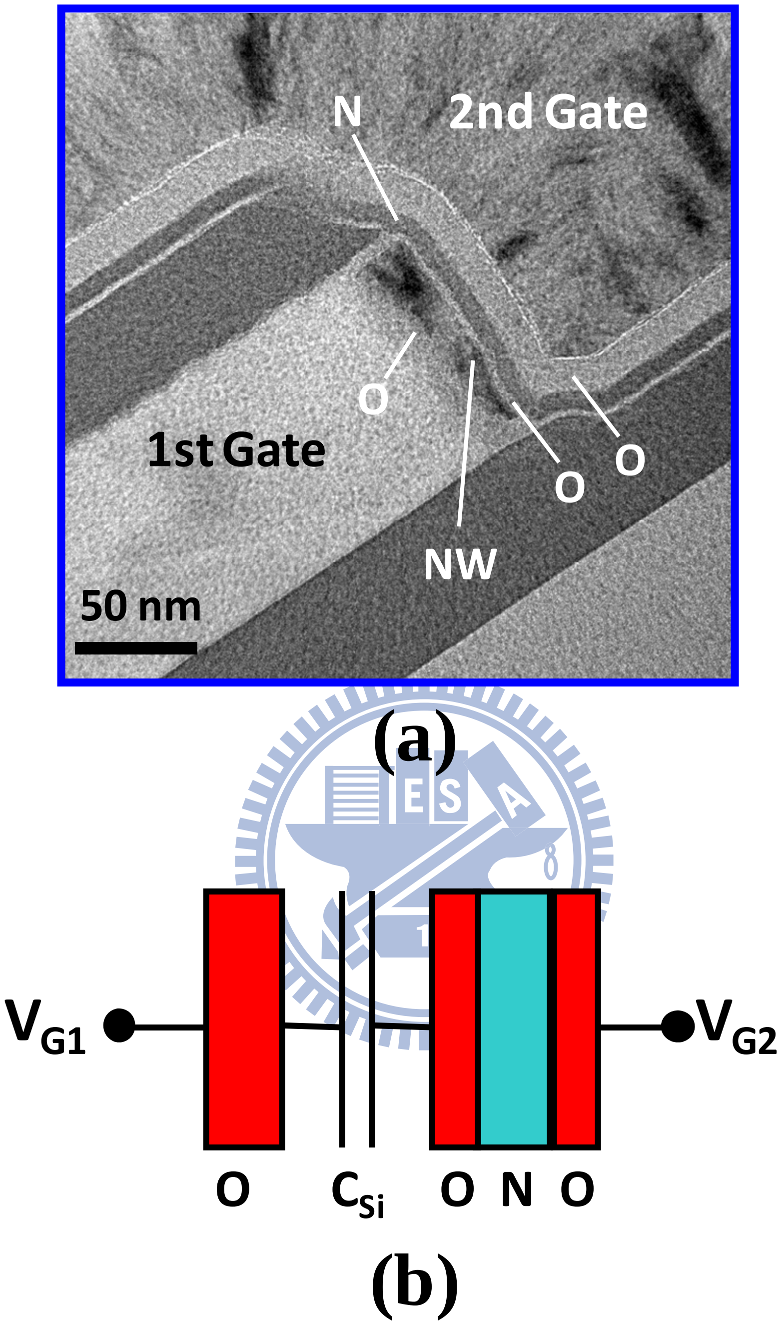


Fig. 5-4 (a) TEM image of a fabricated double-gated poly-Si NW SONOS TFT. (b) Graphic representation for indicating the composition of the gate dielectrics and notation for the applied biases.

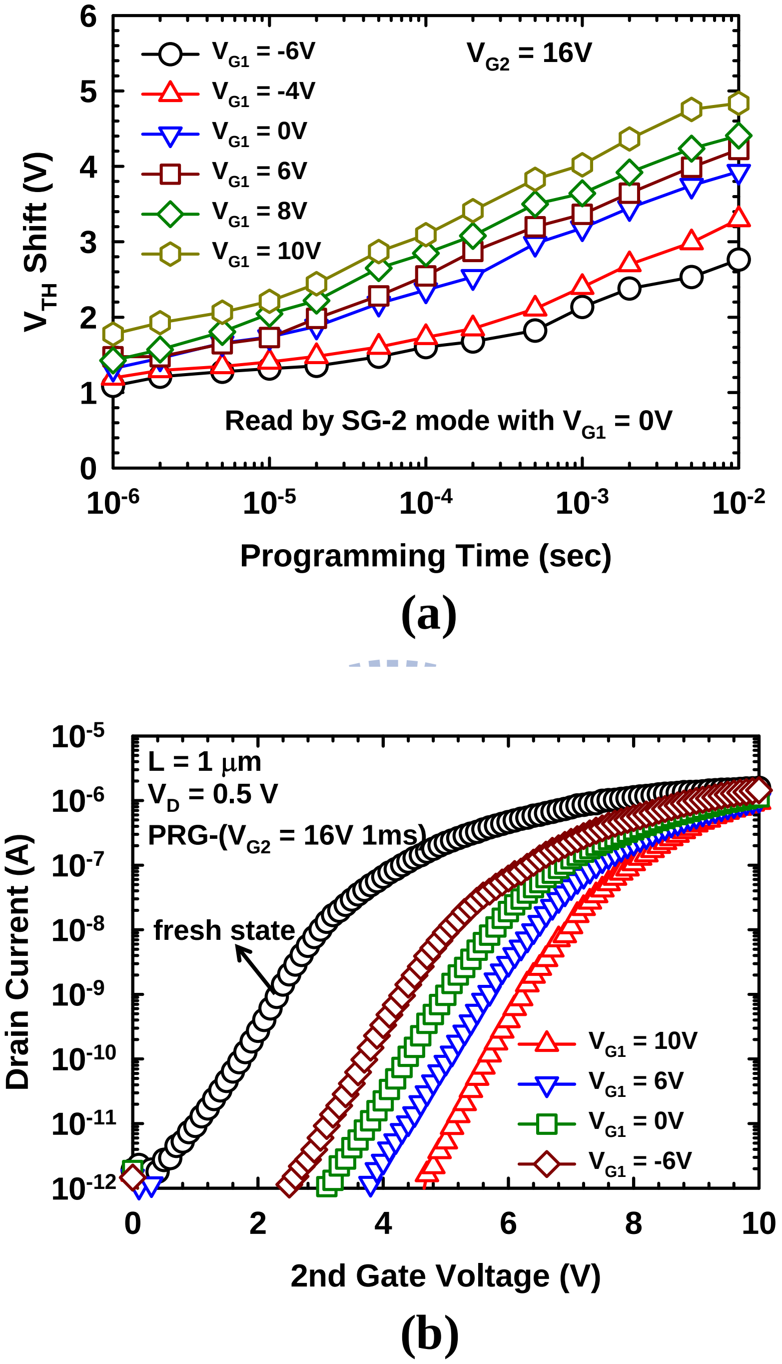
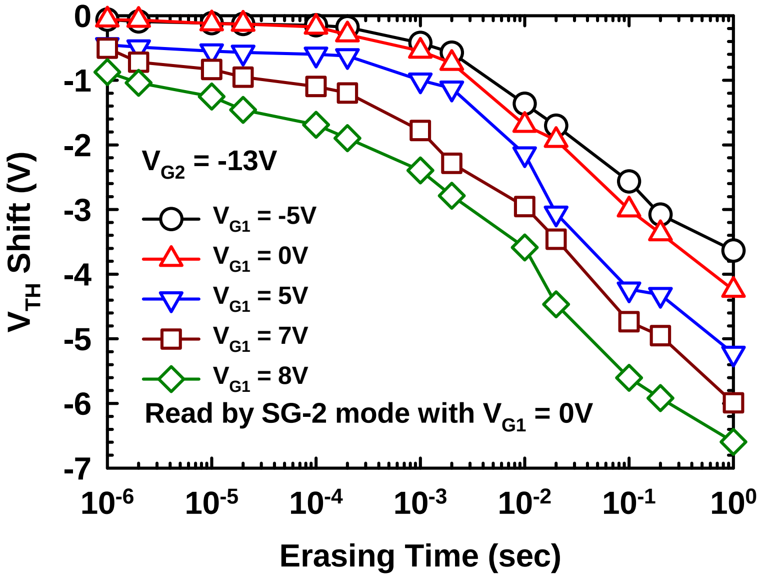
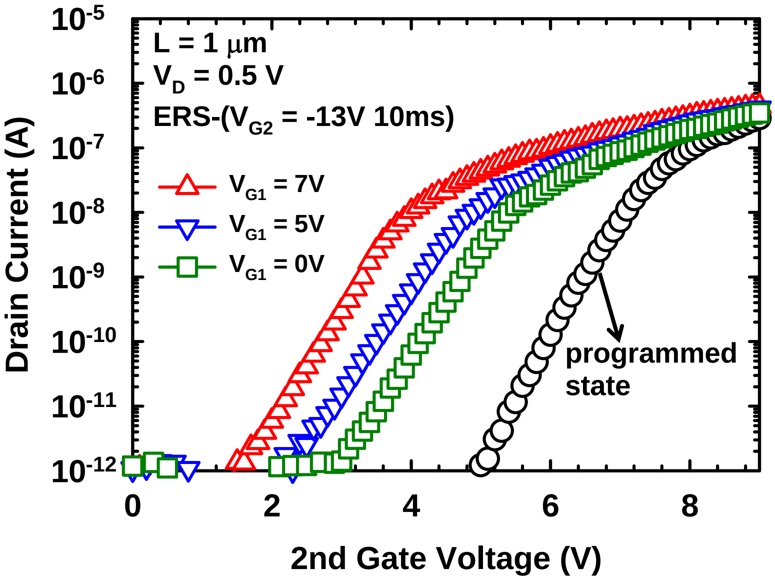


Fig. 5-5 (a) Programming speed characterization with V_{G1} as a parameter while V_{G2} is fixed at 16 V. (b) Transfer curves corresponding to (a) showing that a larger V_{G1} applied during programming stressing could result in an enhanced V_{TH} shift.

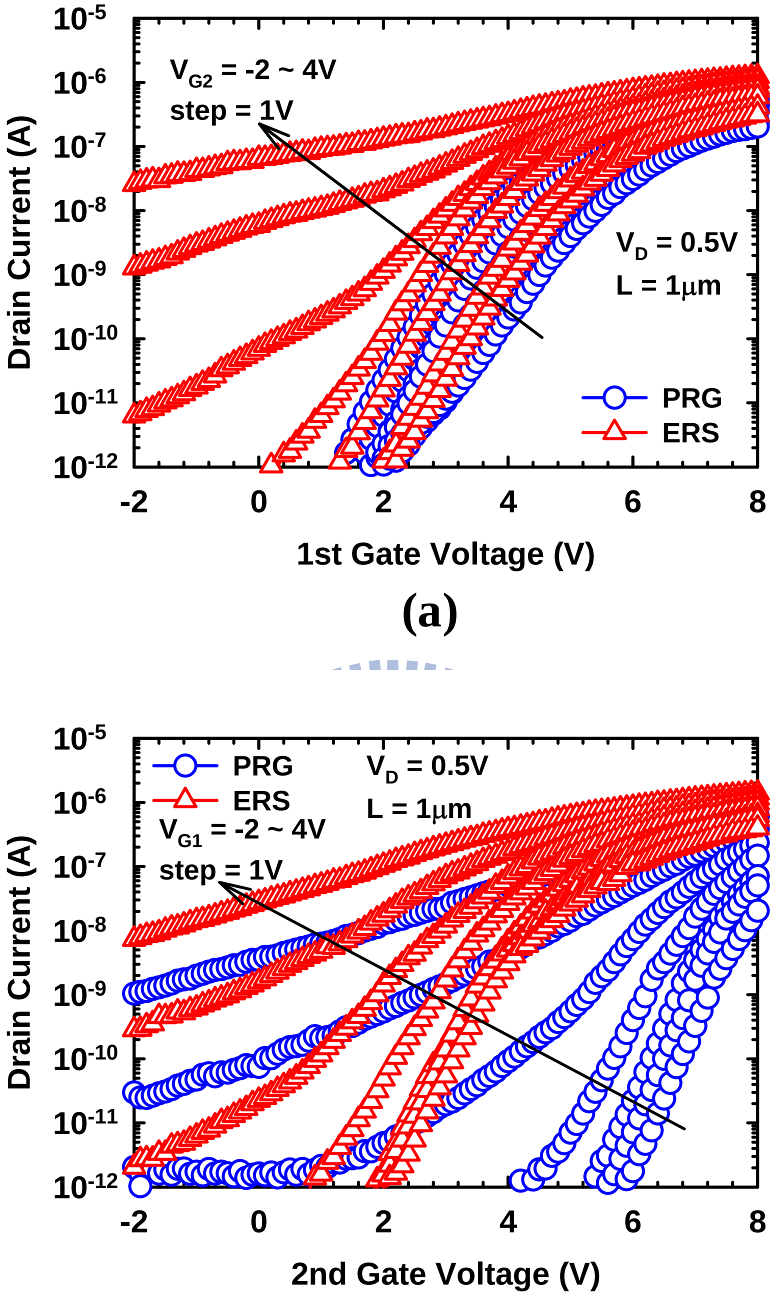


(a)



(b)

Fig. 5-6 (a) Erasing speed characterization with V_{G1} as a parameter while V_{G2} is fixed at -13 V. (b) Transfer curves corresponding to (a) showing that a larger V_{G1} applied during erasing stressing could result in an enhanced V_{TH} shift.



(a)

(b)

Fig. 5-7 Transfer curves under P/E states with varying AG bias when the device is read by (a) SG-1 and (b) SG-2 modes. Programming and erasing are achieved by applying $V_{G1} = 0$ V and $V_{G2} = 16$ V for 10 ms, and $V_{G1} = 0$ V and $V_{G2} = -12$ V for 100 ms, respectively.

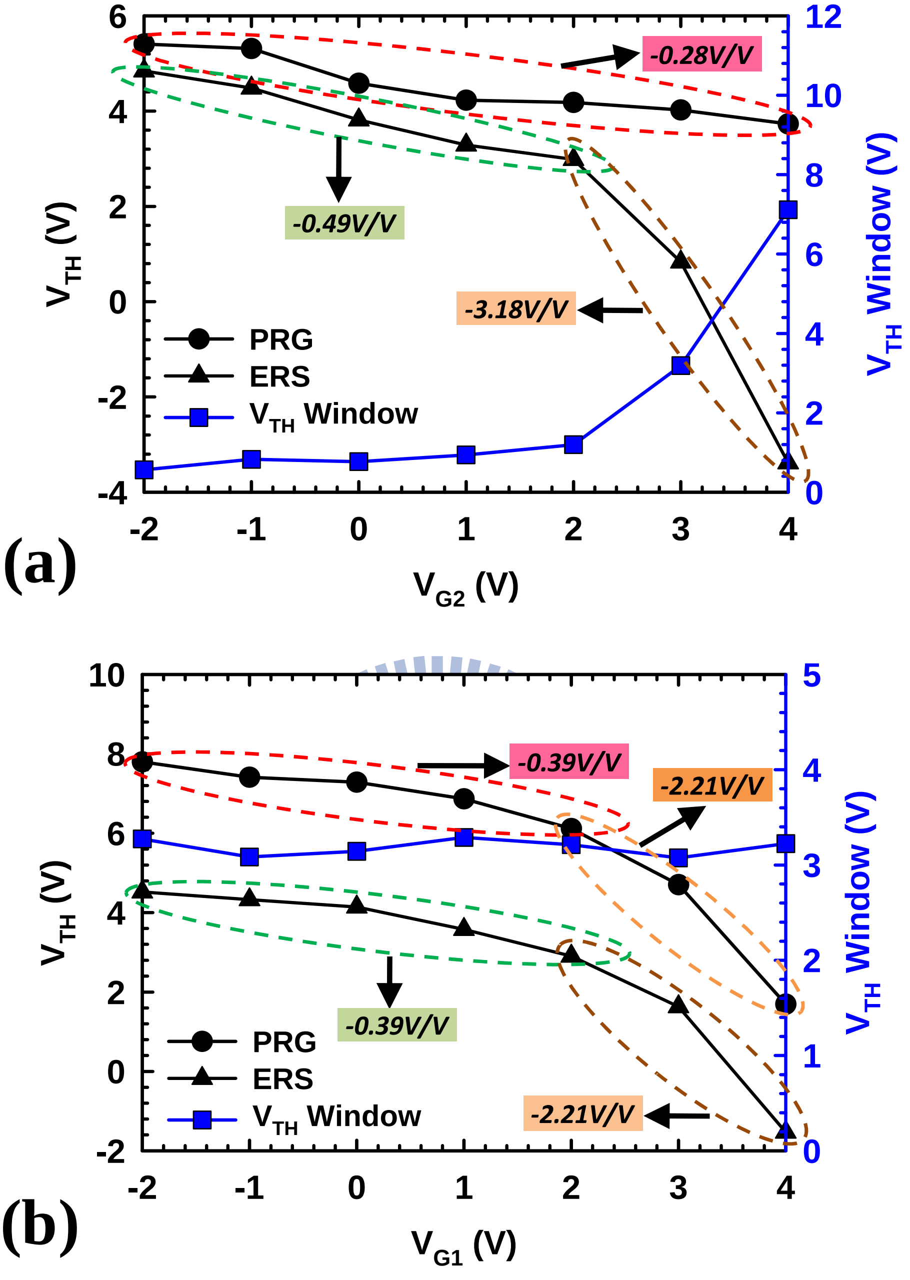


Fig. 5-8 Extracted V_{TH} under programmed and erased states (left vertical axis) from Fig. 5-7, and V_{TH} window (right vertical axis) as a function of AG bias in (a) SG-1 and (b) SG-2 modes. Depending on the condition of the back surface, the magnitude of γ for each operation regime is indicated.

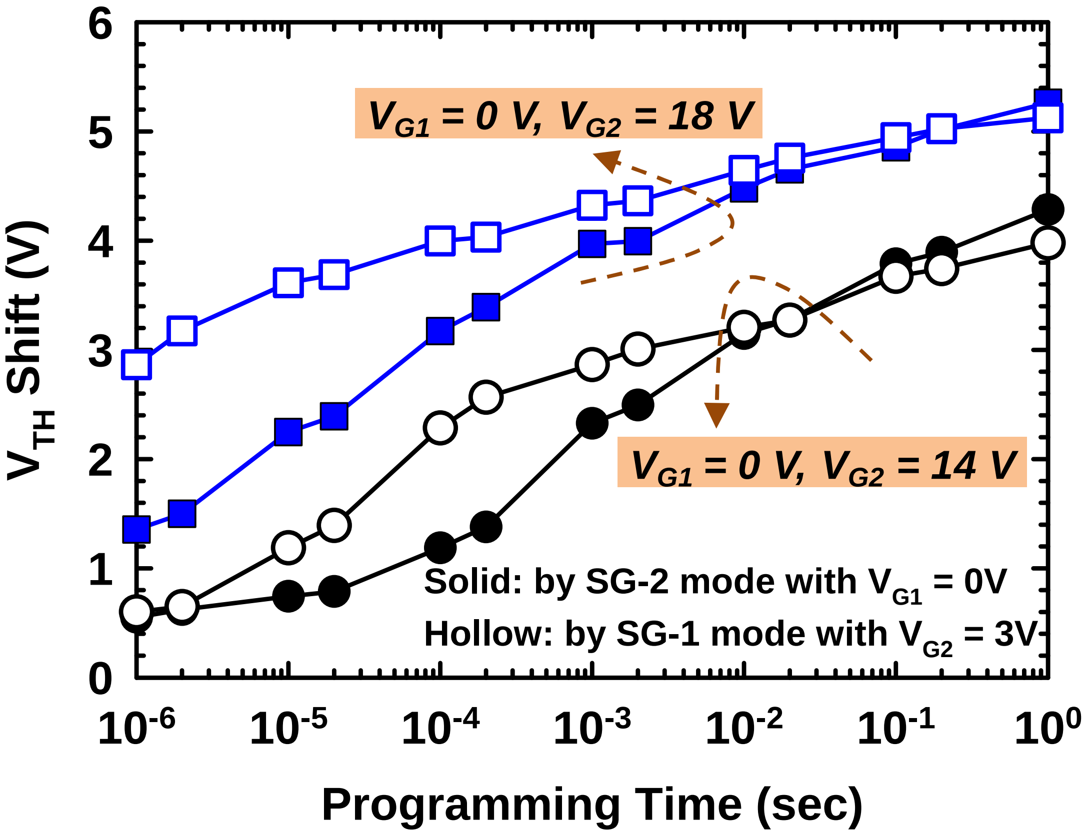


Fig. 5-9 Programming speed comparison between two read modes. The SG-1 mode shows higher efficiency than the SG-2 mode for up to 20 msec. Programming conditions are V_{G1} = 0 V and V_{G2} = 14 V, and V_{G1} = 0 V and V_{G2} = 18 V for curves with circles and squares, respectively.

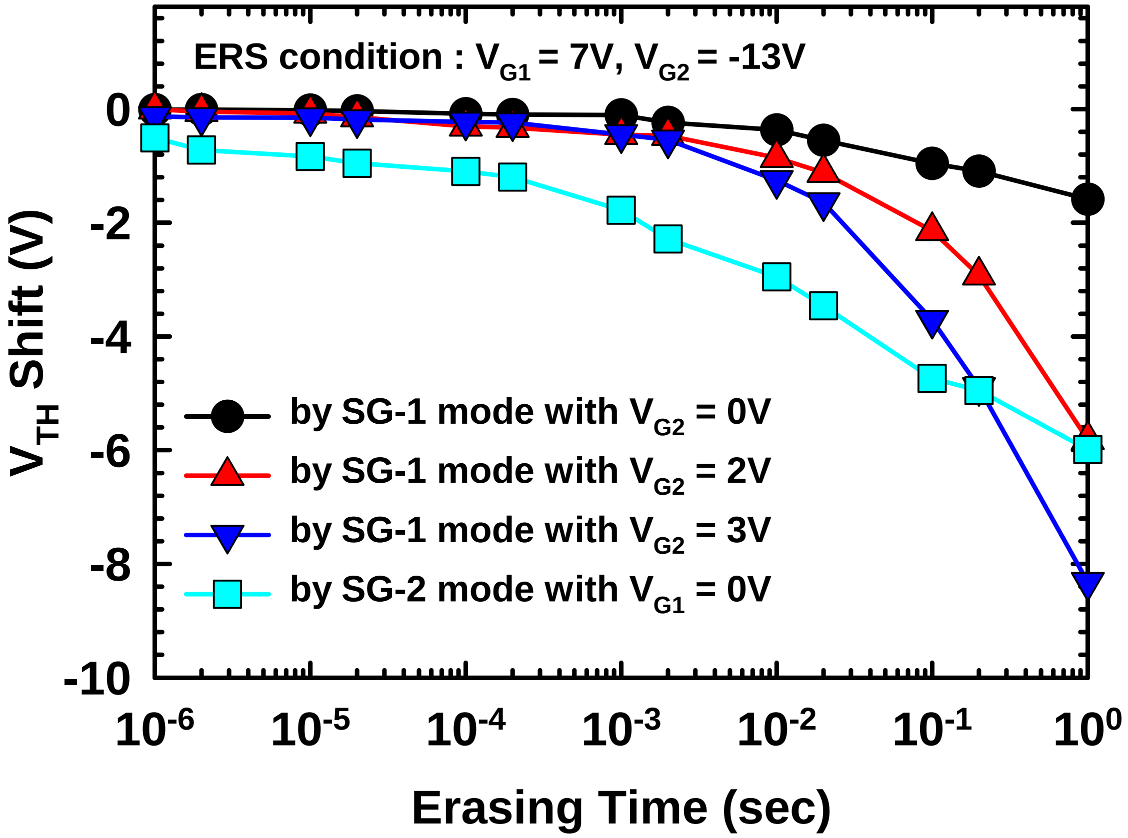


Fig. 5-10 Erasing speed characterization showing that SG-1 mode does not exhibit any V_{TH} shift until 10 msec after which a substantially decreased V_{TH} value is observed for SG-1 mode with V_{G2} = 3 V. Erasing speed as read by SG-1 mode is enhanced with a larger V_{G2} since inversion would be reached earlier by a larger V_{G2} in a given erasing time.

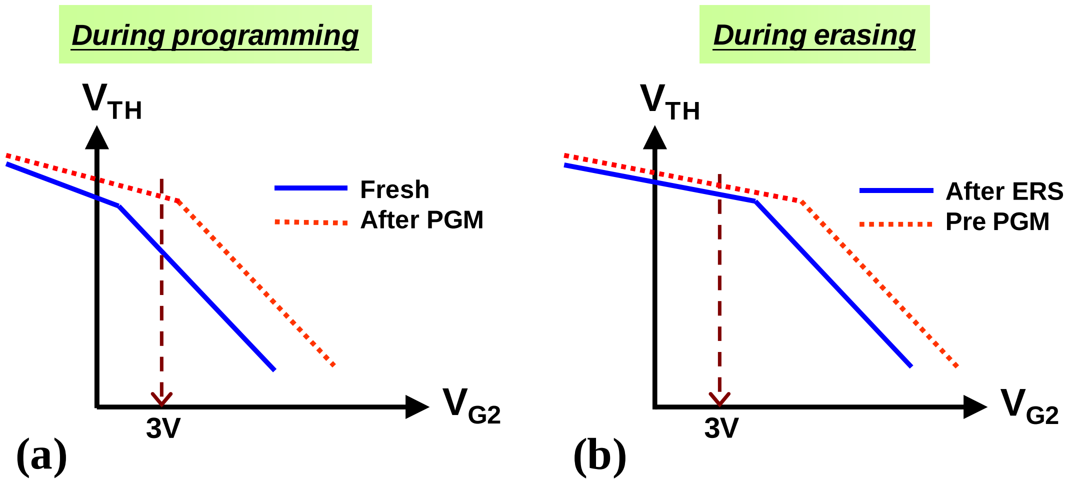
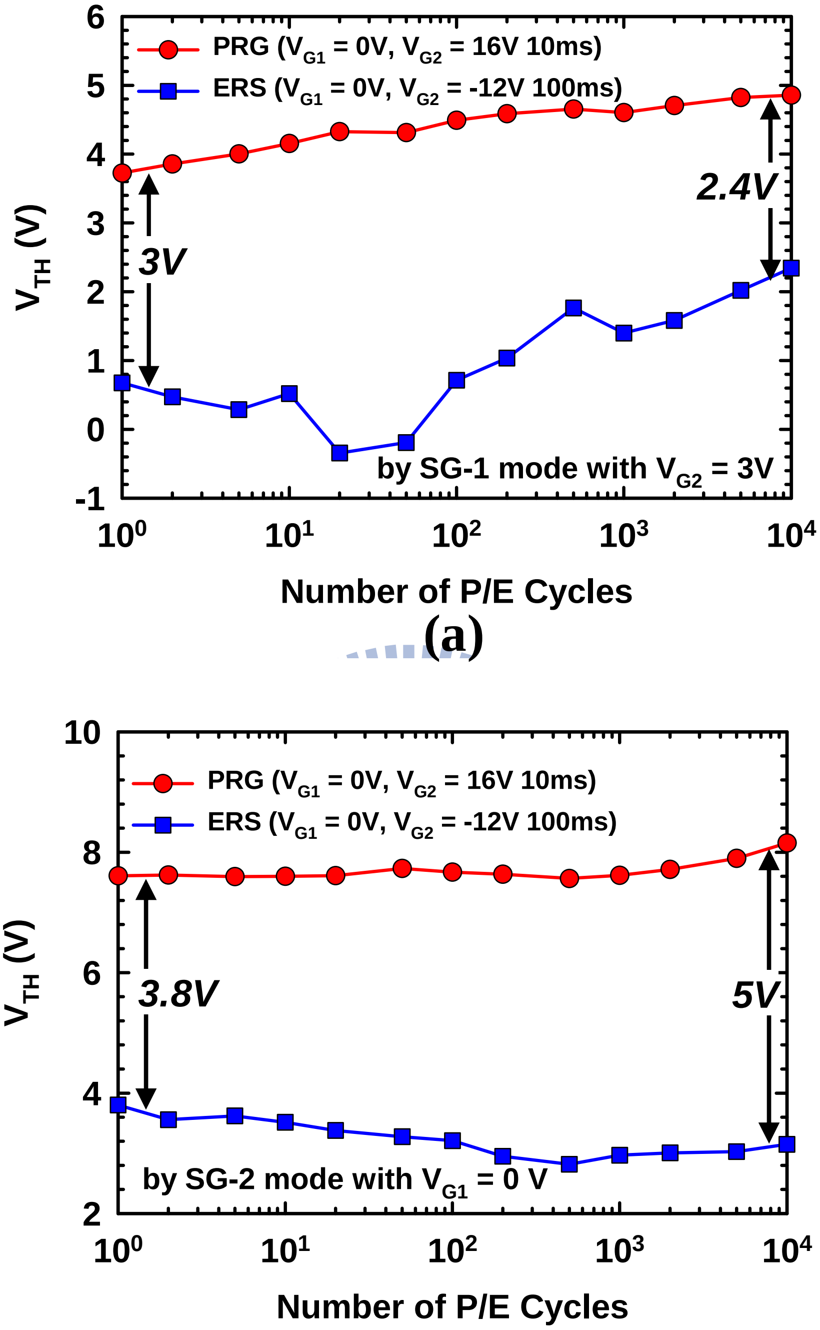


Fig. 5-11Schematic of the evolution of V_{TH}- V_{G2} curves during (a) programming and (b) erasing when read by SG-1 mode. Owing to the selected V_{G2} (= 3 V) and the back-gate effect, an appreciable V_{TH} shift during programming can initially be obtained compared with negligible V_{TH} shift during erasing.



(a)

(b)

Fig. 5-12 Endurance characteristics of (a) SG-1 and (b) SG-2 modes. The more serious variation of V_{TH} at the erased state of SG-1 than SG-2 mode is caused by the back-gate effect.

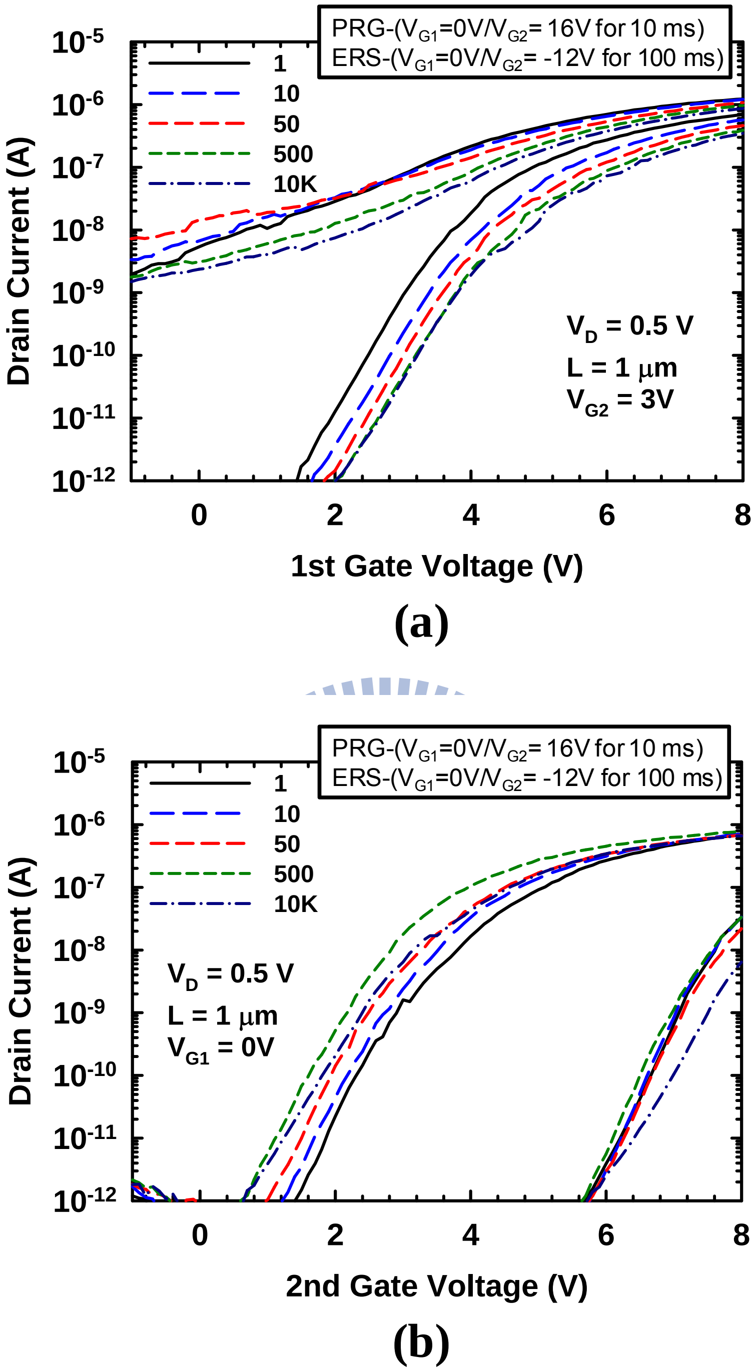


Fig. 5-13 Evolution of transfer curves in P/E states with the number of cycling as a parameter when the device is read by (a) SG-1 mode with V_{G2} = 3 V and (b) SG-2 mode with V_{G1} = 0 V.

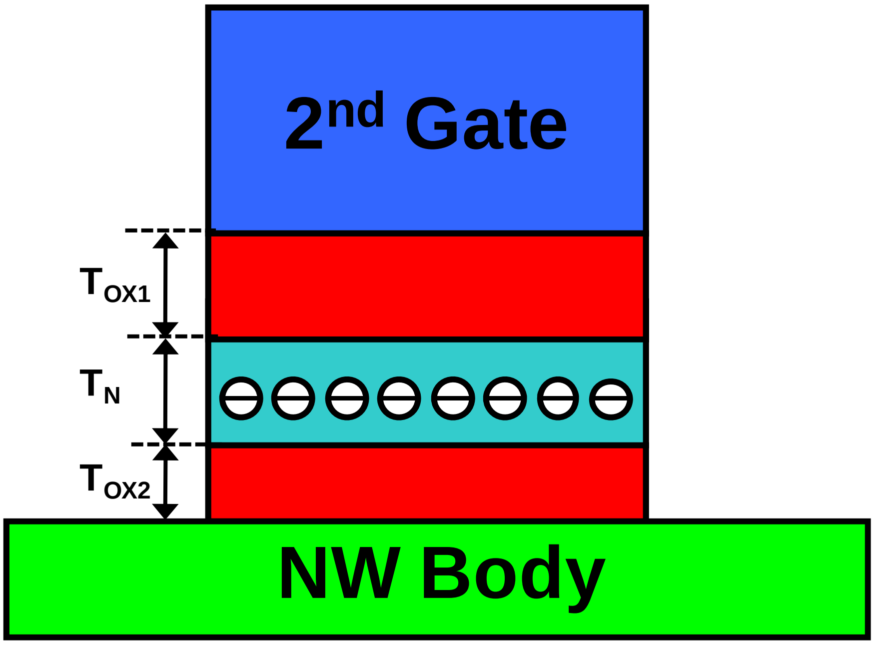


Fig. 5-14 Schematic diagram showing the 2nd gate stack. T_{OX1}, T_N, and T_{OX2} are the respective thicknesses of the blocking oxide, nitride, and tunneling oxide. If the trapped electron density located in the middle of the nitride is Q_{tot}, then the flat-band voltage shift as compared with the fresh state (*i.e.*, $Q_{tot} = 0$) is equal to $Q_{tot}(\frac{T_{OX1}}{\varepsilon_0\varepsilon_{OX}}+\frac{T_N}{2\varepsilon_0\varepsilon_N})$.

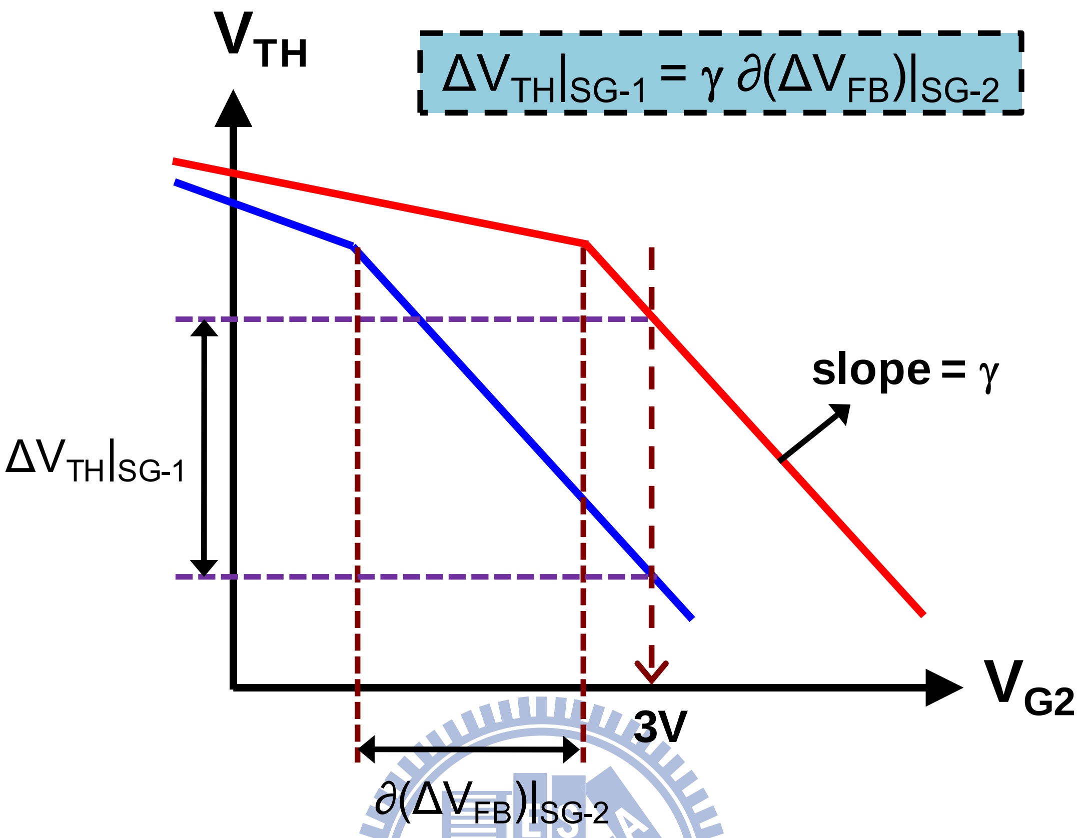


Fig. 5-15 Schematic illustration of how V_{TH} in SG-1 mode responds to the change in the storage charge. Blue and red lines represent the condition when the density of the storage charge in the nitride layer is varied such that the transition point is shifted horizontally by $\partial(\Delta V_{FB})|_{SG-2}$. The resultant V_{TH} shift under SG-1 mode would then be equal to $\gamma\partial(\Delta V_{FB})|_{SG-2}$.

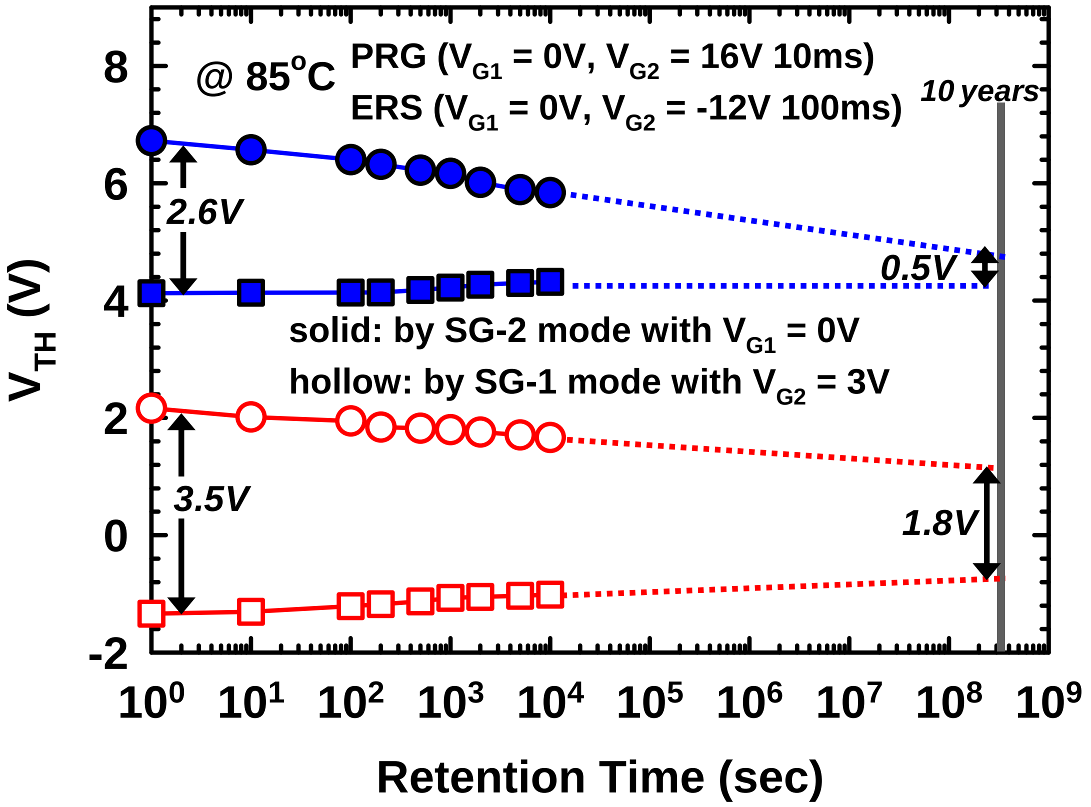


Fig. 5-16 Baked retention characteristics indicating that V_{TH} of the programmed state in SG-1 mode is lowered to a lesser extent than that of SG-2 mode while these two modes are comparable in terms of their V_{TH} enlargement at erased states.

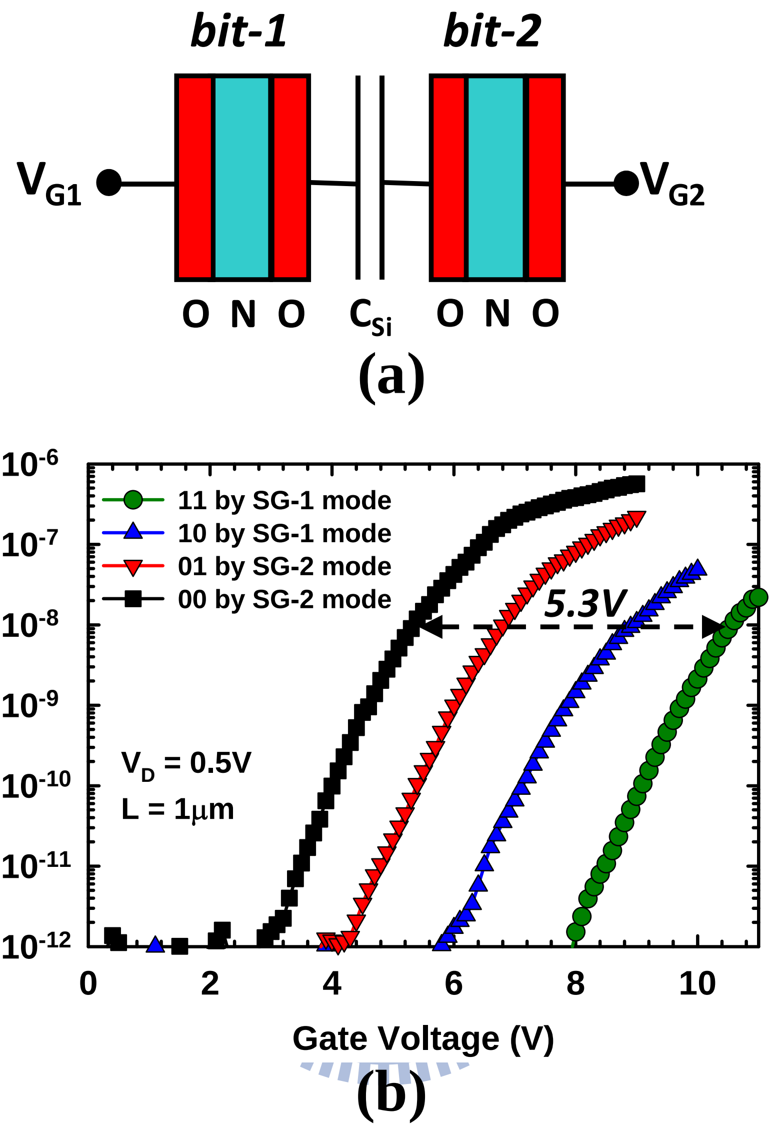


Fig. 5-17 (a) Schematic illustration of the device configuration for 2-bit/cell characterization. Bit-1 and bit-2 refer to the bit located in the nitride of the 1st and 2nd gate dielectrics, respectively. (b) Four distinguishable states can be observed when the dielectrics of both gates are made up of ONO, thus realizing the 2-bit/cell feature. V_{TH} difference between state-11 and -00 is 5.3 V.

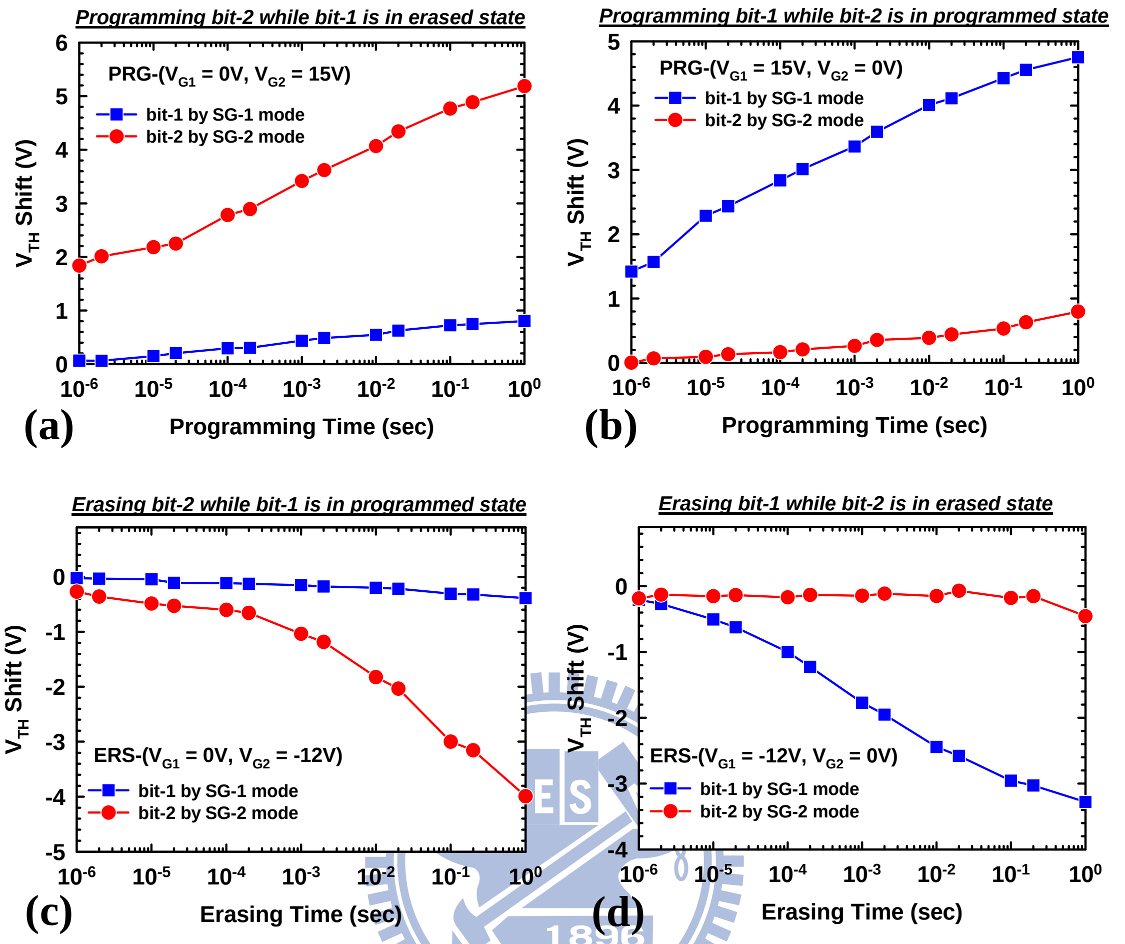


Fig. 5-18 (a)(b) Programming and (c)(d) erasing disturbance characterization for 2-bit/cell operation. Decent P/E speed is attained without significant disturbance. The measured device is with 50-nm-thick NW channels.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

To sum up, a novel and unique technique of manufacturing poly-Si NW transistors is proposed and demonstrated which combines the strengths of top-down and bottom-up approaches. The reported device scheme features rectangular NW channels and independent double-gated configuration. The fabrication procedure is simple without the need of resorting to advanced or prohibitive lithographic apparatus. Taking advantage of the optimized plasma etching condition which is selective and isotropic, this method could be accomplished in highly reliable and economical manners.

The size dependency of various electrical characteristics examined in Chapter 2 indicated that the narrower NW width is highly beneficial in enhancing the overall device performance as the grain boundary barrier height could be more effectively reduced by the gate voltage.

In an effort to mitigate the issue encountered in the original fabrication process --- the use of a low S/D implantation energy to avoid inadvertent channel doping yet at the sacrifice of S/D series resistance, a modified process flow incorporating *in situ* doped S/D was implemented to retain the merits of lightly doped channel and heavily doped

S/D in Chapter 3. Using this scheme, the smallest SS ever reported (73 mV/dec) for a poly-Si based device was attained and the resultant S/D series resistance was one-sixth of that of the implanted counterparts.

To demonstrate the scalability of the proposed NW transistor, devices with sub-100 nm L were fabricated and characterized in Chapter 4, which indicated that SCEs could be effectively suppressed by DG mode in terms of insignificant SS degradation whereas the driving current started to exhibit saturation as the channel length is below 0.7 μm. Abrupt switching characteristics under SG-2 mode were observed during cryogenic measurement and appeared only in devices with sub-100 nm L. With the aid of experiment and simulation, this exclusivity was verified to be caused by the dopants which were non-uniformly distributed in the gate.

Exploiting the unique feature of the IDG configuration, Chapter 5 comprehensively examined its implications for NVM operations. At the first section, it was demonstrated that an appropriate AG bias applied during P/E stressing could effectively improve the P/E speed. In addition, by using a dedicated read gate with oxide-only dielectric, it was found that as a consequence of back-gate bias effects, this unconventional read approach could offer enhanced programming yet retarded erasing speed compared with the conventional counterpart with the dielectric of its read gate made of ONO stack. Comparisons of reliability characteristics between those two feasible read modes were also made which showed that under the unconventional read mode, the programmed V_{TH} dropped to a lesser extent under retention test while the V_{TH} at the erased state exhibited more serious variation under cycling endurance test. A preliminary proof-of-concept characterization regarding 2-bit/cell functionality was performed by using ONO as the dielectric for both gates and showed promising results in terms of four distinguishable V_{TH} levels and insignificant P/E disturbance.

6.2 Future Work

This dissertation covers a wide range of subjects associated with the applications of NW devices. Yet there are still a couple of aspects that need to be addressed and optimized to facilitate the practicality and further improve the device performance.

6.2.1 Crystallinity of Poly-Si NWs

In this work, the poly-Si NW channel was obtained by re-crystallization of amorphous-Si through the so-called solid-phase crystallization (SPC) technique. This method offers simple process and is free of metal contamination. Nevertheless, the grain size thus achieved is only a few tens of nanometers rendering the intrinsic mobility low. To maximize the grain size which in turn improves the device characteristics such as drive current and SS, metal-induced crystallization [6-1] and laser annealing are two popular approaches [6-2] worth considering among other things.

6.2.2 Junction-Free Feature

In 3D NVM architecture, such as BiCS [6-3], owing to the concern of shadowing, the source/drain regions are formed by fringe field effects from gates of neighboring cells instead of ion implantation. Nonetheless, another issue regarding read current may arise with this kind of scheme. Since it is quite sophisticated to precisely control the electron density induced by such an effect, once the density becomes too low, the read current would be severely degraded. To this end, a novel concept termed junction-free feature has been reported to be very promising for expanding NAND flash applications [6-4]. In such a configuration, there is only one type of dopant with high concentration within the whole channel body. For an N-channel device, the dopant would be N-type leading to essentially a normally-on or depletion-mode device. An experimental work by our group with gate-all-around poly-Si NW structure has been published recently that utilized *in situ* doping to attain the junction-free possibility [6-5]. Other benefits of this feature include large disturb margins, no complicated self-boosting program-inhibit method, and improved cycling endurance [6-4]. One concern that needs to be noted is the implication for erasing speed. In [6-6], it was found that the erasing speed decreases as the channel doping of a junction-free device is increased. This detrimental effect could be attributed to the lower hole density available for tunneling during the erasing process.

Despite all those hype, there has not been a junction-free poly-Si NW SONOS device with IDG configuration reported. It is also expected that the above-mentioned retarded erasing speed could be mitigated to some extent with the aid of a proper AG bias applied during erasing, as demonstrated in Section 5.3. Hence, it would be very interesting and informative to investigate the characteristics and applications of junction-free functionality combined with our proposed IDG device.

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Appendix

Fabrication and Characterization of a Low Temperature Polycrystalline-Germanium Thin Film Transistor Using Ultra High Vacuum Sputtering

A.1 Introduction

Despite being the material on which the 1st functional transistor was based, Ge has not been widely adopted in the mainstream very large scale integration technology out of concern of the water solubility of its thermal oxide GeO_2. Si, on the other hand, when being thermally oxidized, forms high quality water-insoluble SiO_2 that is mechanically and thermally stable without significant leakage, thus making Si the preponderant material used in the semiconductor industry so far. Yet as the technology keeps its relentless scaling pace by reducing the device dimension for continuous performance improvement, the physical limit of geometric scaling is imminent as the transistor dimension approaches only a few tens of nanometers. Although various performance boosters that do not simply rely on scaling have been proposed through such innovative schemes as stressor, multiple-gate, *etc.*, these kinds of techniques are still subject to limitation and will become more and more difficult to implement with the reduced device dimension. For example, strain engineering is found to be closely related to the device geometry and may lead to complex circuit design and severe variation in electrical parameters [A-1]. For the multiple-gate device such as FinFET which is essentially a 3D device structure as opposed to planar counterparts in current CMOS technology, there are plenty of issues involved including non-conformal growth of gate dielectric and ion implantation on conduction surfaces [A-2] and the degradation of electron mobility when the fin width is too thin [A-3].

In line with this, Ge is once again brought back to the research agenda and emerges as a promising alternative material to replace Si, the most important reason of which is its around 4 X and 2.6 X respective possession of hole and electron mobility over Si [A-4]. The melting point of Ge, which is 937 ^{o}C as compared with 1412 ^{o}C of Si, can promote dopant activation at low temperature that helps form shallow junctions, mitigates degradation in high-κ/metal gate stacks, and facilitates 3D IC technology. However, the natural quantity of Ge is much less than Si and cannot be a sustainable source for the industry if Ge is indeed adopted in a scale of mass production. Thin film transistor (TFT) structure is highly immune to this issue by depositing only a thin layer of active material on top of an insulating substrate and is compatible with system-on-panel (SOP) applications and monolithic 3D integration. Most of the previous studies relied on Ge condensation [A-5] or rapid melt growth [A-6] to form such a germanium-on-insulator (GOI) structure. Yet Ge condensation requires a costly silicon-on-insulator substrate to act as the seed for epitaxy while rapid melt growth still utilizes a high temperature annealing process (near 937 ^{o}C) that is inappropriate for applications demanding low temperature processing. To help realize Ge-based TFT applications which were rarely focused in the literature, here we propose a low cost polycrystalline-Ge (poly-Ge) TFT with Ge deposited from ultra high vacuum (UHV) sputtering and recrystallized by solid phase crystallization (SPC) method at 500 ^{o}C. The content of this appendix is arranged as follows. Section A.2 discusses the material properties of the Ge film. In Section A.3, the fabrication process of the proposed device is described followed by electrical characterization. Finally, a brief conclusion and future work are given in Section A.4.

A.2 Material Analysis of the Ge Film

The starting substrate was a 6-inch Si wafer capped with a 200-nm thick thermal oxide layer. Following the standard cleaning process, amorphous-Ge (α-Ge) with 100 nm thickness was deposited through the UHV sputtering system operated with base pressure of 5×10^{-8} torr. Considering the possible out-diffusion of Ge in the form of GeO when subject to annealing, a 30-nm thick tetraethyl orthosilicate (TEOS) oxide layer was deposited onto the Ge film by plasma-enhanced chemical vapor deposition

(PECVD) prior to annealing. Another split without the oxide capping layer was also prepared for comparison. Then, all the samples underwent different annealing conditions at 400 ^{o}C -500 ^{o}C with duration ranging from 0.5 hr to 6 hr in N_2 ambient at atmospheric pressure. After removal of the oxide capping layer by buffered oxide etchant (B.O.E) solution, atomic force microscopy (AFM) was used for measuring the surface roughness while X-ray diffraction (XRD) in a θ-2θ geometry with Cu Kα radiation for identifying the grain orientation of the recrystallized film. The grain size of poly-Ge was estimated by using high resolution transmission electron microscopy (HRTEM) on a cross sectional view of the poly-Ge film.

Shown in Fig. A-1 is the XRD result for the oxide-capped samples annealed for 2 hr from 400 ^{o}C to 500 ^{o}C. It can be seen that major phases of Ge composed of (111), (220), and (311) orientations become apparent after 500 ^{o}C annealing. Besides, the intensity of those peaks increases with increasing annealing temperature and in virtue of the sharp peaks appearing after 500 ^{o}C annealing, the as-sputtered α-Ge has been transformed into poly-Ge. To further probe the impacts of annealing duration, the XRD profiles after annealing that was performed at 500 ^{o}C with different durations are given in Fig. A-2, from which the intensity of peaks increases with the annealing duration from 0.5 hr to 1 hr and then essentially remains constant with further increase of annealing time. The nearly identical full-width-at-half-maximum (FWHM) of XRD peaks after 1 hr annealing suggests that the grain size of poly-Ge only grew within the initial 1 hr and became saturated. HRTEM image of the Ge film annealed at 500 °C for 1 hr is shown in Fig. A-3. The grain size can be roughly estimated to be around 5 nm. Such a small grain size of poly-Ge is consistent with previous studies that poly-Ge tends to display a smaller grain size compared with poly-Si under the same SPC condition [A-7][A-8]. The grain size is expected to be enlarged by employing other recrystallization methods, such as metal-induced crystallization [A-9] and laser annealing [A-10]. TEM analysis performed on the sample annealed at 500 °C for 6 hr exhibits a similar grain size of 5 nm (not shown), in agreement with the XRD results that when being annealed at 500 °C, the peak intensity or the grain size is only enlarged within the initial 1 hr.

Effect of the oxide capping layer is examined in Fig. A-4. AFM analysis shows distinct difference between these two kinds of samples in terms of the magnitude of the root-mean-square (rms) surface roughness, which is 4.9 nm (Fig. A-4 (a)) and 0.8 nm (Fig. A-4 (b)) for the samples without and with the capping oxide, respectively. In accordance with the surface roughness results, sheet resistance measured from 4-point probe is 4100 ohm/square for the without-oxide-capped sample and 3050 ohm/square for the oxide-capped sample. It has been reported that when the annealing temperature is above 420 °C, Ge will react with GeO_2 to form volatile GeO [A-11]; thus, the large surface roughness and sheet resistance for the sample without the oxide capping layer can be inferred to be caused by the decomposition of GeO_2. For the oxide-capped sample, the decomposition of GeO_2 is hindered by the capping layer and a much smoother surface with lower sheer resistance is obtained as a result.

A.3 Electrical Characteristics of a Poly-Ge TFT

Before discussing the electrical characteristics of the proposed device, the fabrication process will be briefly described. To reduce the parasitic source/drain (S/D) resistance, a raised nickel silicide (NiSi) S/D scheme is adopted. First, a 200-nm thick oxide was thermally grown on a 6-inch Si substrate. Poly-Si with 100-nm thickness was then deposited by low pressure chemical vapor deposition. BF_2 implant was then carried out with 5×10^{15} cm^{-2} dose and 20 keV energy. Thermal annealing at 600 ^{o}C for 12 hr was next performed to activate the dopants. Subsequently, raised S/D regions were patterned followed by deposition of 30-nm Ni and rapid thermal annealing at 500 ^{o}C for 40 sec to form NiSi. After removal of unreacted Ni, 100-nm Ge was deposited by UHV sputtering. A 30-nm TEOS oxide capping layer was deposited by PECVD prior to Ge recrystallization performed at 500 ^{o}C for 1 hr as per the results in Section A.2. After stripping of the capping layer by B.O.E solution, poly-Ge active regions were patterned. Gate dielectric of 30-nm TEOS oxide was formed by PECVD followed by deposition and definition of Al to serve as the gate electrode. Self-aligned BF_2 S/D implantation was conducted with 5×10^{15} cm^{-2} dose and 40 keV energy. Annealing at 400 ^{o}C for 1 hr in N_2 ambient was then used to activate the dopants. The device fabrication was completed after standard backend processes including passivation layer deposition, contact hole opening, and metallization.

A schematic cross-sectional picture of the proposed poly-Ge TFT is shown in Fig. A-5 along with its transfer characteristics in Fig. A-6. The nominal channel length and width of the measured device is 10 and 20 μm, respectively. Instead of displaying a smooth turn-on behavior, the transfer curve shows sawtooth-like characteristics in the subthreshold regime. Dynamic trapping during the measurement process is speculated to be the root cause for this phenomenon because the extent of instability in the transfer curve is gradually reduced with each measurement sequence. But the overall characteristics including on-current (I_{ON}), off-current (I_{OFF}), and subthreshold swing (SS) remain constant regardless of the sequence of the measurement. Defining the I_{ON} as the drain current at a gate voltage of -12 V and the I_{OFF} as the minimum drain current in the characterized gate voltage range, one can see that the I_{ON}/I_{OFF} ratio is ~ 7.6×10^4 at -0.1 V drain voltage. Employing the basic MOSFET theory [A-12], the peak field-effect mobility can be determined from the transconductance and is estimated to be 1.95 cm^2/V s. Such a low value is associated with the small grain size of the poly-Ge film discussed in Section A.2. The large number of grain boundaries inherent in the poly-Ge severely degrades device performance as carriers tend to experience more scattering events than single-crystalline counterparts. Moreover, there are abundant dangling bonds and intra-grain strained bonds present in the film that are likely to trap conduction carriers. The effects mentioned above usually manifest themselves in low I_{ON}, large leakage current, degraded SS and reduced mobility, *etc*. Though the mobility of the proposed poly-Ge device is far inferior to the performance of devices reported by other groups, the I_{OFF} is the lowest and SS the smallest among the poly-Ge devices ever reported [A-13][A-14]. This suggests that the surface potential of poly-Ge characterized in this study can be well modulated by the applied gate voltage in the subthreshold regime while in the above-threshold situation, significant density of tail states near the band edge of poly-Ge due to strained bonds or structural disorders near grain boundaries accounts for the low mobility. Since both the leakage current and field-effect mobility are mainly influenced by the tail state distribution [A-15], it can be inferred that the number of tail states close to the conduction band is much less than that near the valence band based on the low mobility and small leakage current of the measured p-channel device. Nevertheless, detailed extraction of the density of states across the whole bandgap requires another n-channel device, which is relatively difficult to fabricate compared with p-type counterparts due to the low solid solubility and large diffusion coefficient of n-type dopants [A-16] and is still under investigation.

Comparison of major device characteristics between this work and other GOI devices is given in Table A-I. The highest process temperature of our device occurs in the stage of thermal annealing for activating the dopants in poly-Si used to form NiSi. Poly-Ge TFTs in [A-13][A-14] have a mobility much larger than that attained in this study even though the same SPC temperature (500 ^{o}C) was utilized. However, since the as-deposited α-Ge of [A-13][A-14] is by molecular beam technique with base pressure of 5×10^{-11} Torr (which is a thousandth of that of our UHV sputtering system), it is expected that the film quality is intrinsically better accounting for its larger mobility. For [A-17] which takes advantage of bonding to form single-crystalline GOI structure, the mobility is still degraded compared with bulk Ge PMOSFETs owing to the surface roughness of the Ge film and the poor dielectric/channel interface thus caused. Single-crystalline Ge obtained by rapid melt growth in [A-6] suffers high I_{OFF} coming from junction leakage and the high temperature required for melting renders this method unsuitable for 3D technology whereas the condensation method in [A-18] is still impractical from a cost-oriented perspective. In spite of the tiny grain size of our poly-Ge, our device exhibits the best performance in Table A-I in terms of the steepest SS and largest I_{ON} / I_{OFF} ratio. It should be noted that the processing temperature can be reduced to below 500 ^{o}C by using metal as the raised S/D material and replacing SPC with metal-induced crystallization scheme. In addition, defect-annihilation approaches such as NH_3 plasma treatment and forming gas annealing are expected to further promote the device performance.

A.4 Conclusions and Future Work

A.4.1 Conclusions

In this appendix, we have fabricated and characterized a low temperature poly-Ge TFT with raised S/D structure by UHV sputtering. The as-sputtered film is found to be amorphous and recrystallizes into polycrystalline state with 5-nm grain size after SPC performed at 500 ^{o}C for 1 hr. Surface roughness after recrystallization shows a strong dependency on the presence of the oxide capping layer. The sample without the oxide capping layer exhibits 4.9-nm rms surface roughness compared with only 0.8-nm for the oxide-capped sample. This is inferred to be caused by the decomposition of GeO_2 into GeO when the Ge film is directly exposed to the annealing ambient, which can be effectively suppressed when a capping layer is present. Small as the grain size achieved in this study may be, our device displays the steepest SS, lowest I_{OFF}, and highest I_{ON} / I_{OFF} ratio among the poly-Ge devices ever reported and even beats some of the single-crystalline counterparts. With further device optimization such as crystallinity enhancement and defect passivation procedures, the proposed device appears promising for realizing SOP applications and monolithic 3D IC technologies.

A.4.2 Future Work

Epitaxial growth has been a primary way of obtaining a single-crystalline film right on top of another layer which is also single-crystalline and most of the time is not exactly the same material as the film to be grown. This method is particularly useful for strained MOSFET technologies where SiGe on Si substrate, Si on SiGe virtual substrate, and source/drain stressors are commonly seen. Nonetheless, in order to ensure that the epitaxially-grown film is of high quality without defects, the typical temperature in Si epitaxial process could reach 1000 ^{o}C. This high temperature requirement to some degree limits the stage where epitaxy could be adopted and thus this step is only present in front-end processing.

As a matter of fact, literature has shown that it is not impossible to obtain device-grade Si at 300 ^{o}C by ion-assisted sputtering [A-19]-[A-22]. The fundamental physics behind is to take advantage of the bombarding ions in a way that the energy incident on the grown film helps fulfill activation/annealing and enhances the migration of sputtered atoms on the substrate surface. Therefore, the epitaxial growth could be promoted at a much lower temperature than in a conventional process. Furthermore, there was already a study on epitaxy of Ge on Si by sputtering in as early as 70s [A-23], and high-quality sputtered Ge on Si has also been reported that yielded carrier mobility (1280 cm^2/V s) comparable to the bulk value and the p-Ge/n-Si diode thus obtained exhibited a reverse breakdown voltage of 10 V [A-24]. Promising as this low temperature epitaxy may seem, no other follow-up report regarding *single-crystalline* Ge has appeared and the overall growth conditions still remain ambiguous.

We have also conducted a few experiments in an attempt to clarify the dependence of the crystallinity of the as-sputtered Ge on various process parameters, including the deposition temperature, the energy of bombarding Ar ions, and the pressure during sputtering. The basic sputtering process consists of the following. After being RCA cleaned, a 4-inch Si wafer was immediately loaded into a sputterer (Denton Vacuum Discovery 550) operated with a base pressure of 3×10^{-6} Torr. 90 sec of pre-sputtering was performed prior to opening the shutter to allow the sputtered atoms to reach the substrate. Subsequently, various conditions were used to sputter Ge off the target. During pre-sputtering, only the RF bias (source power) connected to the target was switched on while that to the substrate was grounded. Once the sputtering process was initiated, a certain value of RF bias was also applied to the substrate to adjust the energy of bombarding Ar ions.

Shown in Fig. A-7 are AFM images taken from two samples with different RF biases applied to the substrate during sputtering. These images were extracted from the phase mode that measures the phase shift of the cantilever oscillation during scan. Here only the substrate RF bias was varied; the other parameters are 300 W source power, 300 °C chuck temperature, 50 sccm Ar flow rate, and 3.5 mTorr pressure. It can be seen that in this case the one with higher RF bias (and thus higher DC bias) results in a larger grain size, which could be interpreted from the perspective of the energy imparted to the growing film from Ar ions. In other words, by further increasing the RF bias beyond 5 W such that more energy is transferred into the sputtered film, it is possible to obtain a film with better crystallinity and a larger grain size. However, as noted in [A-19] regarding the Si on Si growth, once the bombarding energy is above the sweet spot, the damaging effect from the impinging ions would start to become prominent; hence, care should be taken in finding the optimum RF bias yielding single-crystalline Ge on Si. Equally important is to ensure that this optimal value be safely below the sputter threshold; otherwise, physical sputtering would take place within the grown film resulting in an extremely low deposition rate and severe surface roughness. One useful technique to prevent this effect from happening is to increase the pressure so that more ion flux could reach the substrate surface and meanwhile the DC bias is reduced for a given RF bias. In this way, the overall energy flux reaching the wafer which is equal to the product of the number of impinging ions and their individual energies should not be altered much but the detrimental effect of high energy bombardment is able to be ameliorated significantly.

XRD spectrum for one selected sample that has been post-annealed by rapid thermal annealing at 600 ^{o}C for 2 min is shown in Fig. A-8. It was sputtered by 300 W of source power with 2 W RF bias (DC bias = 43 V) applied to the substrate for 700 sec resulting in 200-nm thickness. The fresh sample without annealing has been characterized by XRD as well (data not shown) but only exhibited very weak and broad peaks, possibly due to the film still being amorphous. Also included in Fig. A-8 is the bulk Ge (006) peak for reference. Although not very sharp, the peak position for Ge (006) in this sample was measured at 107.80^{o}, from which the out-of-plane lattice constant is extracted to be roughly 5.719 Å. Compared with the bulk lattice constant of Ge (5.657 Å), the fact that the sputtered film is elongated in the out-of-plane direction means that it is subject to in-plane compressive strain, which is reasonable since Si has a smaller lattice constant (5.43 Å) than Ge does. The extremely large FWHM of Ge (006) in Fig. A-8 implies that the post-annealed film is at best polycrystalline if not amorphous. To confirm this, electron backscatter diffraction (EBSD) is also used to inspect the crystallographic orientation of the sputtered film, as shown in Figs. A-9 (a)-(c), which are taken at three different spots at least 1 mm apart in the sample. First thing to note is that there is no single preferred orientation indexed from the kikuchi bands. Secondly, based on the simulated orientation of Ge unit cell in the insets of Figs.

A-9 (a)-(c), the Ge grains located at these three spots display random crystallographic orientations. Thus, it is concluded that this post-annealed film is still polycrystalline.

As a brief summary of this section, the results presented herein are just the first attempt to obtain single-crystalline Ge on Si by sputtering in a detailed manner. Preliminary experiments have demonstrated the possibility of altering the film quality through adjusting the energy of bombarding ions in the sputter tool. More detailed and thorough experimentation would be needed to attain the device-grade Ge on Si goal.

A.5 Acknowledgment

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Table A-I Comparison of major device parameters among Ge-on-insulator devices. Only those not from commercial vendors are listed.

	Ge crystallinity	**Highest process temperature (°C)**	**Mobility ($cm^2/V\,s$)**	**SS (mV/dec)**	**I_{ON}/I_{OFF}**
This work	Poly	600	1.95	812	7.6×10^4
[A-13]	Poly	500	100	3820	100
[A-14]	Poly	500	140	3843	375
[A-17]	Single	250	170	1430	22
[A-6]	Single	945	NA	2146	10
[A-18]	Single	400	400	1250	10^4

Mobility, SS, and I_{ON}/I_{OFF} are extracted in the linear region.

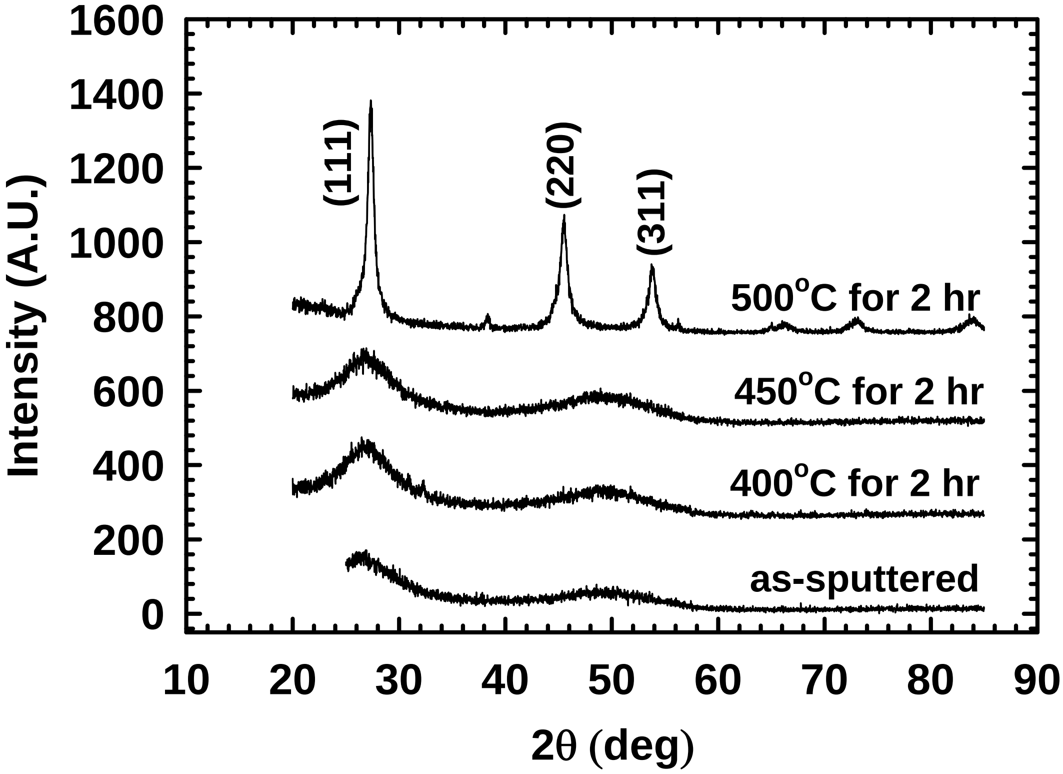


Fig. A-1 XRD profiles of samples undergoing SPC at different temperatures for 2 hr. Major orientations of poly-Ge are identified as (111), (220), and (311). The result for a fresh sample is also included for comparison.

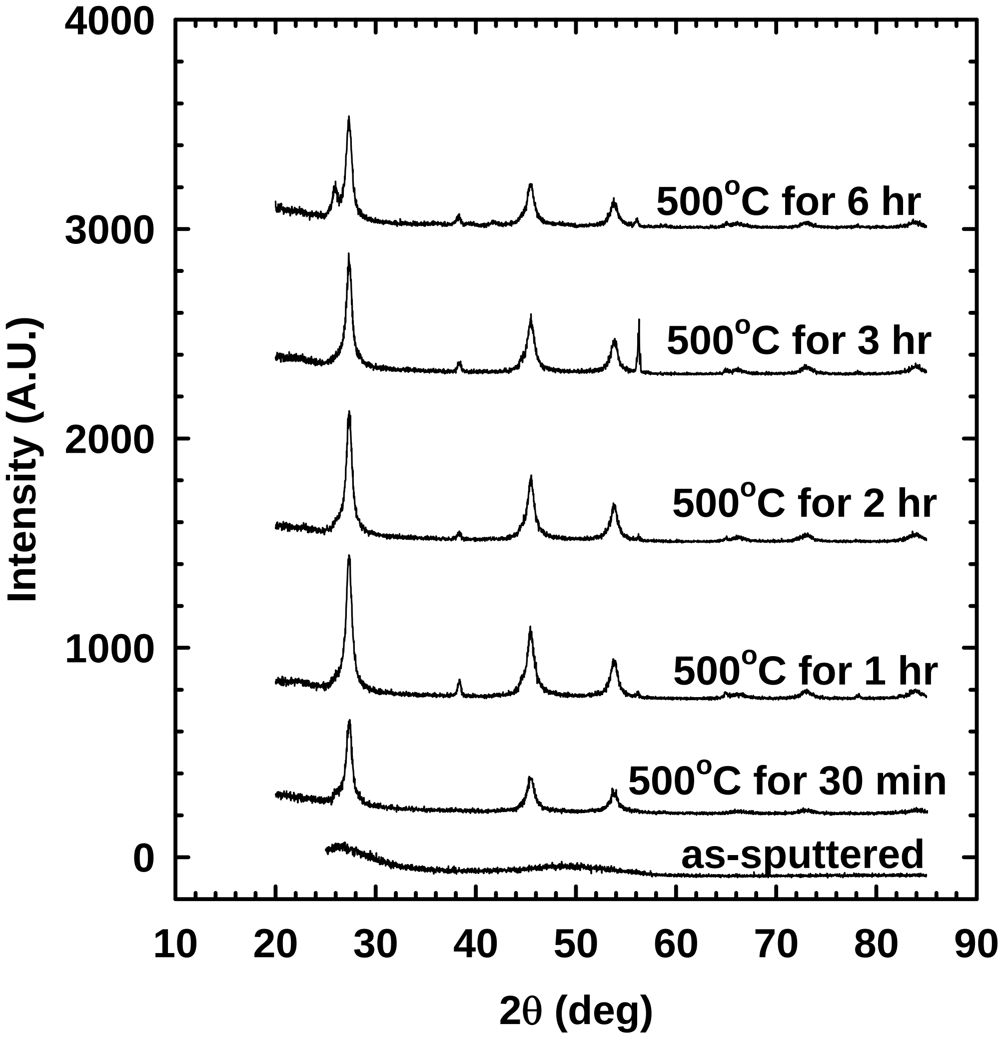


Fig. A-2 XRD results of samples undergoing SPC at 500 °C for different durations ranging from 0.5 hr to 6 hr. Peak intensities are observed to increase only within the initial 1 hr of annealing and then remain constant.

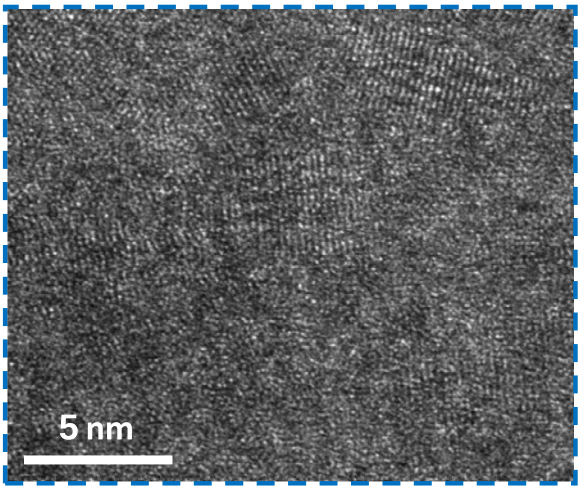
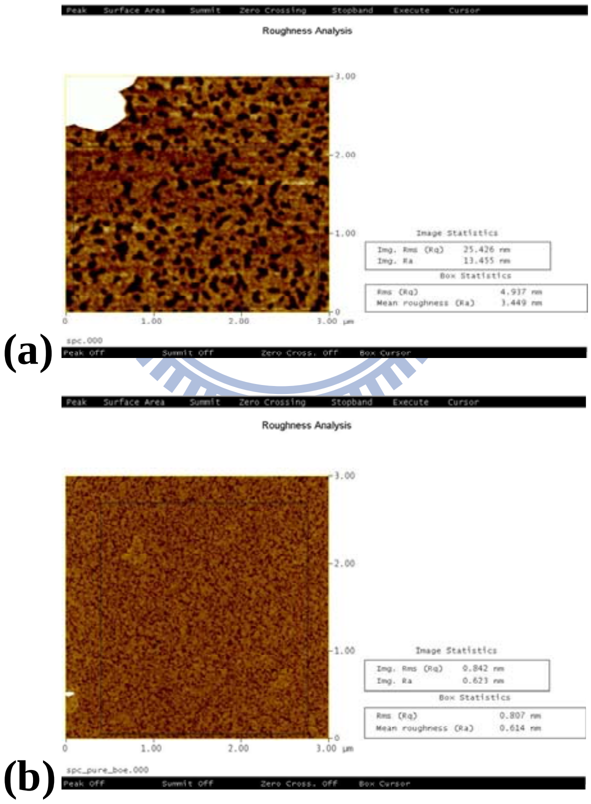


Fig. A-3 Cross-sectional TEM image of the poly-Ge film annealed at 500 ^{o}C for 1 hr.



(a)

Image Statistics

Img. Rms (Rq)	25.426 nm
Img. Ra	13.455 nm

Box Statistics

Rms (Rq)	4.937 nm
Mean roughness (Ra)	3.449 nm

(b)

Image Statistics

Img. Rms (Rq)	0.842 nm
Img. Ra	0.623 nm

Box Statistics

Rms (Rq)	0.807 nm
Mean roughness (Ra)	0.614 nm

Fig. A-4 AFM surface analysis of the poly-Ge film annealed at 500 ^{o}C for 1 hr for a sample (a) without and (b) with the oxide capping layer during annealing.

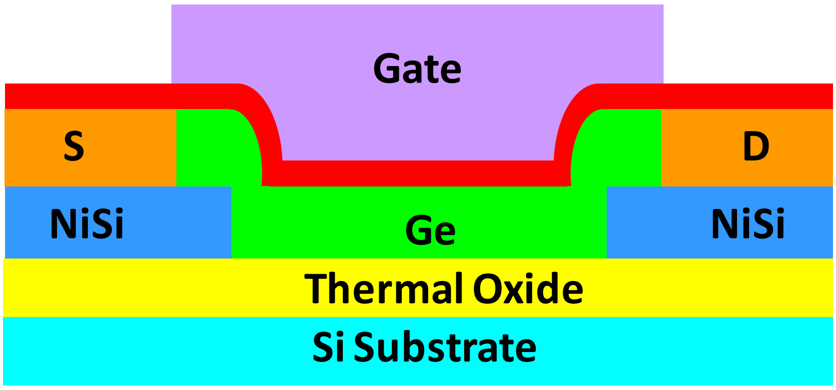


Fig. A-5 Schematic structure for the proposed poly-Ge TFT.

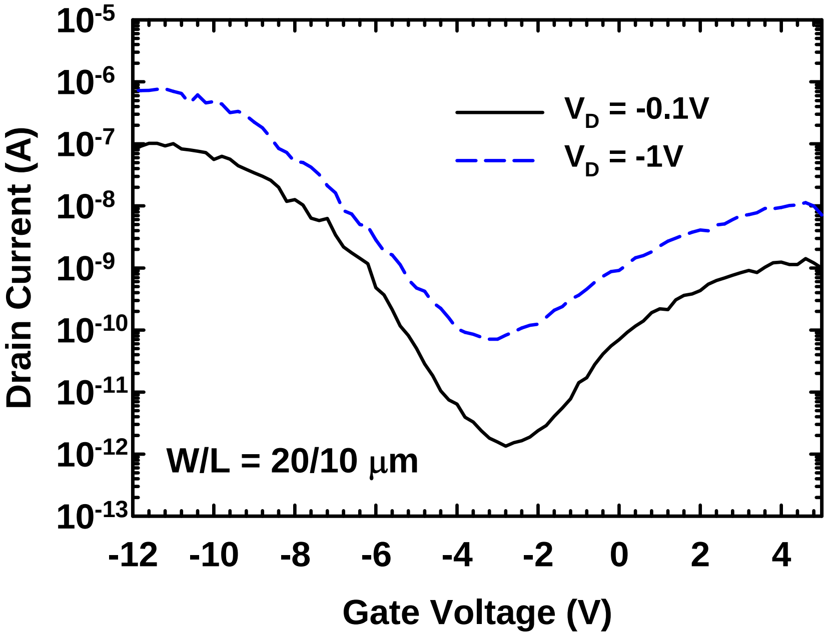


Fig. A-6 Transfer characteristics of the proposed poly-Ge TFT.

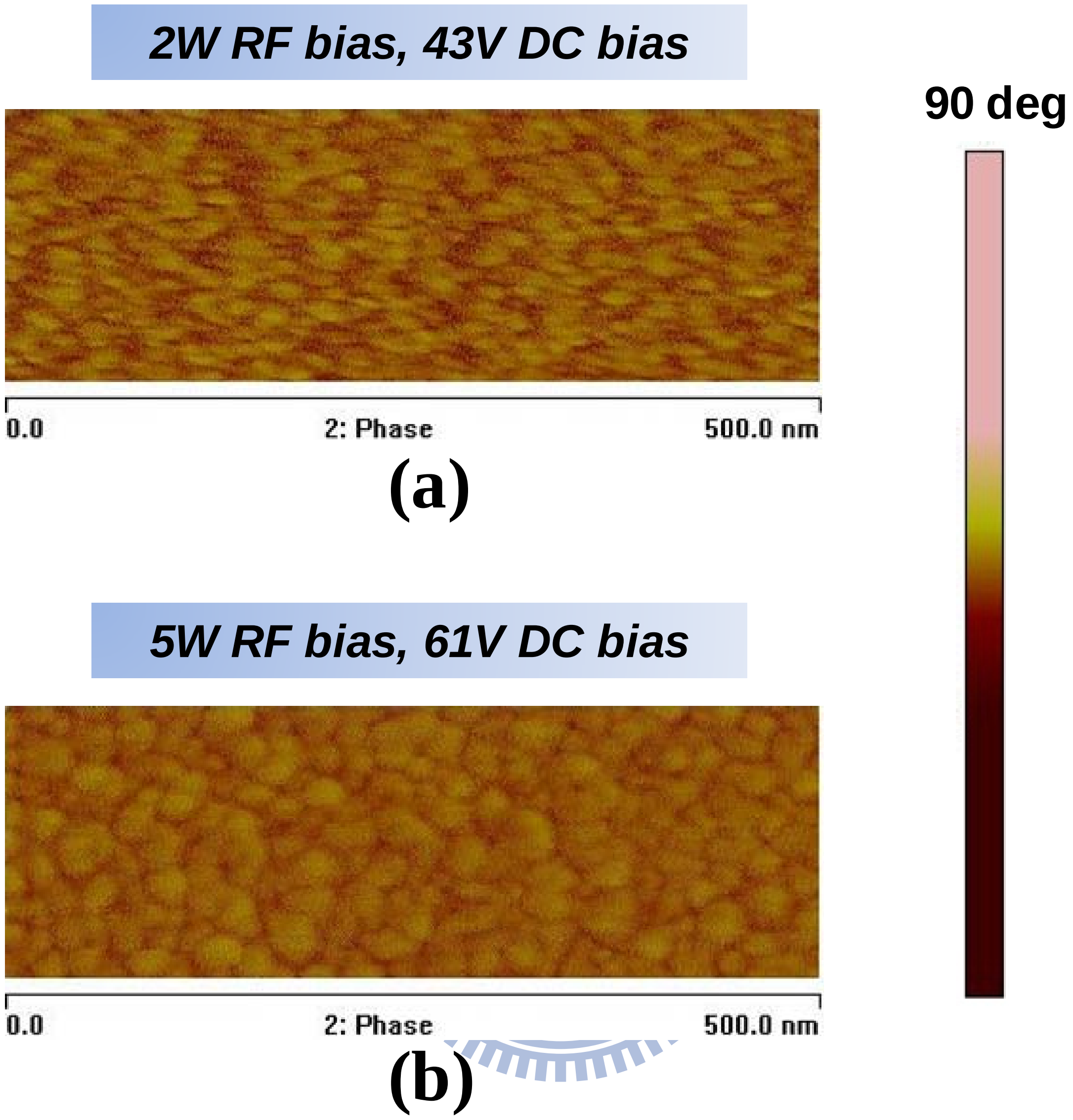


Fig. A-7 AFM images in phase mode of two sputtered Ge on Si samples deposited with (a) 2 W RF bias (DC bias = 43 V) to the substrate and (b) 5 W RF bias (DC bias = 61 V) to the substrate, respectively.

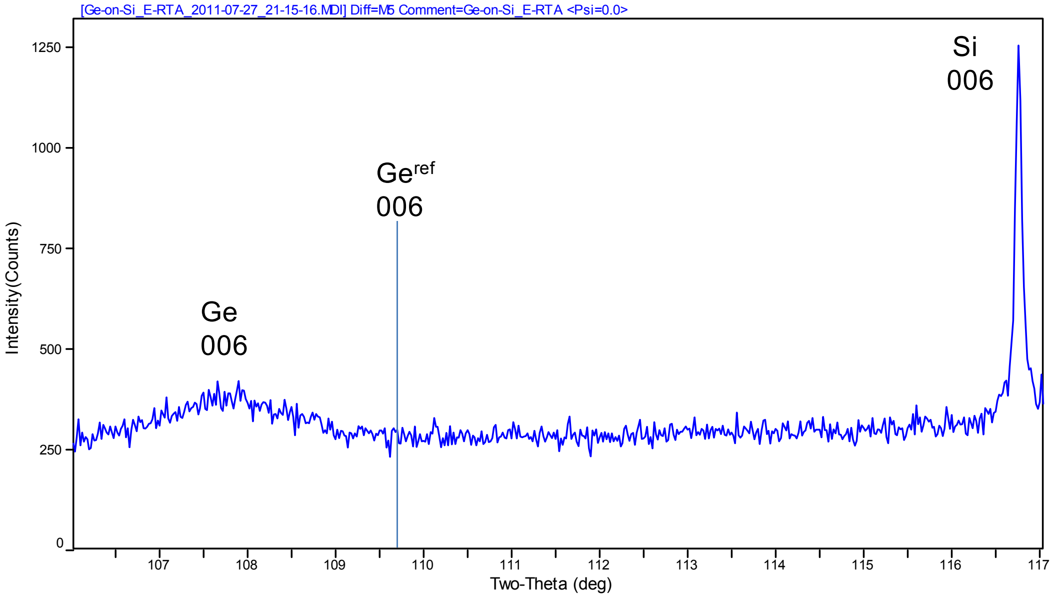


Fig. A-8 XRD profiles of one sputtered Ge on Si sample after 600 °C 2 min RTA annealing. It was sputtered by 300 W of source power for 700 sec with 2 W RF (DC bias = 43V) bias applied to the substrate. The final Ge thickness is 200 nm.

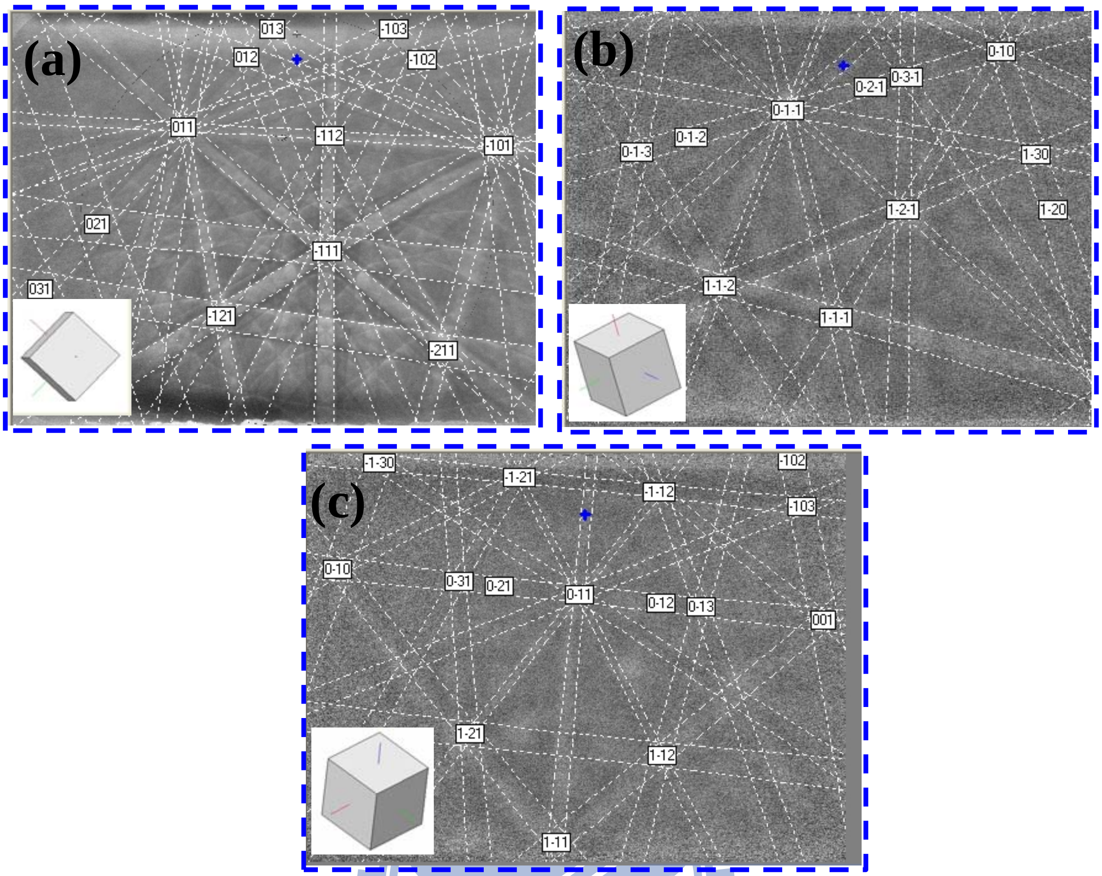


Fig. A-9 EBSD patterns of the Ge film at three different spots (a, b, c). Results: Ge film is polycrystalline with very small, tens of nm, grain size. Insets in (a, b, c) with simulated orientation of Ge unit cell indicate random crystallographic orientations of Ge grains.

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博士論文：具獨立雙閘極之多晶矽奈米線薄膜電晶體的研製與分析

Fabrication and Analysis of Independent Double-Gated Poly-Si Nanowire Thin-Film Transistors

Publication List

A. Journal Papers

1. H. C. Lin, C. H. Hung, **W. C. Chen**, Z. M. Lin, H. H. Hsu, and T. Y. Huang, "Origin of hysteresis in current-voltage characteristics of polycrystalline silicon thin-film transistors," *J. Appl. Phys.*, vol. 105, no. 5, pp. 054502-1– 054502-6, Mar. 2009.
2. A. Ortiz-Conde, A. D. L. Rey, W. Liu, **W. C. Chen**, H. C. Lin, J. J. Liou, J. Muci, and F. J. G. Sanchez, "Parameter extraction in polysilicon nanowire MOSFETs using new double integration-based procedure," *Solid State Elect.*, vol. 54, pp. 635-641, Jun. 2010.
3. **W. C. Chen**, H. C. Lin, Y. C. Chang, C. D. Lin, and T. Y. Huang, "*In situ* doped source/drain for performance enhancement of double-gated poly-Si nanowire transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1608-1615, Jul. 2010.
4. **W. C. Chen**, H. C. Lin, Z. M. Lin, C. T. Hsu, and T. Y. Huang, "A study on low temperature transport properties of independent double-gated poly-Si nanowire transistors," *Nanotechnology*, vol. 21, no. 43, pp. 435201-1–435201-7, Oct. 2010.
5. C. W. Luo, H. C. Lin, K. H. Lee, **W. C. Chen**, H. H. Hsu, and T. Y. Huang, "Impacts of nanocrystal location on the operation of trap-layer-engineered poly-Si nanowired gate-all-around SONOS memory devices," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 1879-1885, Jul. 2011.
6. **W. C. Chen**, H. C. Lin, and T. Y. Huang, "Investigations of an independent double-gated polycrystalline silicon nanowire thin film transistor for nonvolatile memory operations," *Jpn. J. Appl. Phys.*, vol. 50, no. 8, pp. 085002-1– 085002-7, Aug. 2011.

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B. Letter Papers

1. H. C. Lin, **W. C. Chen**, C. D. Lin, and T. Y. Huang, “Performance enhancement in double-gated poly-Si nanowire transistors with reduced nanowire channel thickness,” *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 644-646, Jun. 2009.
2. W. Liu, J. J. Liou, A. Chung, Y. H. Jeong, **W. C. Chen**, and H. C. Lin, “Electrostatic discharge robustness of Si nanowire field-effect transistors,” *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 969-971, Sept. 2009.
3. **W. C. Chen**, H. C. Lin, Y. C. Chang, and T. Y. Huang, “Effects of independent double-gated configuration on polycrystalline-Si nonvolatile memory devices,” *Appl. Phys. Lett.*, vol. 95, 133502, Sept. 2009.
4. Z. M. Lin, H. C. Lin, **W. C. Chen**, and T. Y. Huang, “Insight into the performance enhancement of double-gated polycrystalline silicon thin-film transistors with ultrathin channel,” *Appl. Phys. Lett.*, vol. 96, 072108, Feb. 2010.

C. Conference Papers

1. **W. C. Chen**, C. D. Lin, H. C. Lin, and T. Y. Huang, “Fabrication of novel nanowire field effect transistors,” in *proceeding of International Microprocess and Nanotechnology Conference*, pp. 16-17, Fukuoka, Japan, Oct. 2008.

2. **W. C. Chen**, C. H. Hung, Z. M. Lin, H. H. Hsu, and H. C. Lin,“ Origin of hysteresis in current-voltage characteristics of polycrystalline silicon thin-film transistors,“ *Int’l Electron Devices and Materials Symp.*, Taichung, Taiwan, 2008. (**Best Student Paper Award**)
3. **W. C. Chen**, C. D. Lin, H. C. Lin, and T. Y. Huang, “A novel double-gated nanowire TFT and investigation of its size dependency,” in *proceeding of International Symposium on VLSI Technology, Systems, and Applications*, pp. 121-122, Hsinchu, Taiwan, Apr. 2009.
4. **W. C. Chen**, H. C. Lin, Y. C. Chang, and T. Y. Huang, “Performance improvement of poly-Si nanowire transistors featuring *in situ* doped source/drain,” in *proceeding of International Conference on Solid State Devices and Materials*, pp. 1106-1107, Sendai, Japan, Oct. 2009.
5. **W. C. Chen**, Y. N. Chang, H. C. Lin, and T. Y. Huang, “Fabrication and characterization of a poly-germanium transistor,” *Int’l Electron Devices and Materials Symp.*, Taoyuan, Taiwan, 2009.
6. **W. C. Chen**, H. H. Hsu, Y. C. Chang, H. C. Lin, and T. Y. Huang, “Investigations of performance enhancement in a poly-Si nanowire FET featuring independent double-gated configuration and its nonvolatile memory applications,” in *proceeding of International Symposium on VLSI Technology, Systems, and Applications*, pp. 142-143, Hsinchu, Taiwan, Apr. 2010.
7. **W. C. Chen**, H. C. Lin, and T. Y. Huang, “The potential of poly-Si nanowire FETs featuring independent double-gated configuration for nonvolatile memory applications,” *IEEE Silicon Nanoelectronics Workshop,* pp. 147-148, Honolulu, Hawaii, Jun. 2010.
8. Y. L. Liou, **W. C. Chen**, H. C. Lin, and T. Y. Huang, “Fabrication and

characterization of a poly-germanium nanowire TFT," *Int'l Electron Devices and Materials Symp.*, Chungli, Taiwan, 2010.

9. J. P. Wu, **W. C. Chen**, H. C. Lin, and T. Y. Huang, "Fabrication and characterization of a p-type junction-free double-gated poly-Si nanowire transistor," *Int'l Electron Devices and Materials Symp.*, Chungli, Taiwan, 2010.
10. Z. M. Lin, **W. C. Chen**, H. C. Lin, and T. Y. Huang, "A study on abrupt switching phenomena of independent double-gated poly-Si nanowire transistors under cryogenic operation," in *proceeding of International Symposium on VLSI Technology, Systems, and Applications*, pp. 38-39, Hsinchu, Taiwan, Apr. 2011.