國 立 交 通 大 學

電子工程學系　電子研究所

碩　士　論　文

含奈米粒子之先進奈米元件結構應用於太陽能電池之研究

The Research of Advanced Nanodevice Structure with Nanoparticles for Solar cell Applications

研 究 生：詹政邦　　(Cheng-Pang Chan)
指導教授：吳重雨教授 (Prof. Chung-Yu Wu)
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中華民國九十七年十月

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A Thesis
Submitted to Department of Electronics Engineering and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao-Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master
in
Electronics Engineering
September 2008
Hsin-Chu, Taiwan, Republic of China

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摘 要

在本論文中，使用硒化鎘量子點和金奈米粒子，透過離子作用力建構多層太陽能電池奈米元件結構於矽基板上。並且以不同粒徑之硒化鎘量子點依序排列組成此奈米結構，用以實現寬頻吸收光譜太陽能電池。在掃描式電子顯微鏡的觀察下，證明其結構成功地生長於矽基板上。最後，此奈米元件再經過 0.16 mW/cm^2 日光燈照射後，於各種偏壓下皆有固定的光電流增加。在本研究中，太陽能電池功率轉換效率達 1.6 % (六層結構奈米元件，電極寬度為 30μm，長度為 0.5μm)，最大光電流為 664.42 pA，光電流量體積密度為 7.385×10^{-19} A/nm^3，以及單位體積產生功率為 4.256×10^{-23} W/nm^3。經過 24 天，太陽能電池效率衰減了 31.8%。而經過 26 天之後，衰減現象趨於平緩飽和。

根據實驗結果我們發現奈米元件之電極距離縮短有助於太陽能電池功率轉換效率之提升。再此同時，我們建構一個等效電路並成功地解釋奈米元件產生光電流的運作機制，我們稱之為三維「奈米蕭特基二極體」和電組陣列模型，而且 HSPICE 模擬結果與量測結果一致。理論上透過模擬可得到最佳化的奈米元件結構，具有較高的太陽能電池轉換效率。最後經過模擬計算此六層結構之奈米元件效率可達 36.87 % 當電極距離為 40 nm，而 51.17 % 當距離縮短至 30 nm。

The Research of Advanced Nanodevice Structure with Nanoparticles for Solar cell Applications

Student: Cheng-Pang Chan **Advisor: Prof. Chung-Pang Wu**
Prof. Yaw-Kuen Li

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ABSTRACT (English)

In this thesis, PDDA-capped CdSe/ZnS quantum dots and Au nanoparticles are used to construct the multi-layer solar cell nanodevice structure on a silicon substrate through ionic interaction. And an ordered assembly of PDDA-capped CdSe/ZnS QDs with different diameters was employed to realize the wideband solar cell. By SEM photographic, PDDA-capped CdSe/ZnS QDs and Au NPs were successfully deposited on the silicon substrate. Finally, the proposed nanodevices were illuminated by 0.16 mW / cm^2 daylight lamp. As a result, there was a constant photocurrent increment to the current measured in the dark for each voltage bias after illumination by 0.16 mW / cm^2 daylight lamp. In this work, the solar cell efficiency is 1.6% (6-layered PDDA-capped CdSe/ZnS nanodevice with 60 μm in width and 0.5 μm in length.) The maximum photocurrent is 664.42 pA. The highest PVD (photocurrent volume density) is 7.385×10^{-19} A/nm^3, and power volume density is 4.256×10^{-22} W/nm^3. After 26 days, 31.8% decrease in solar cell efficiency. And after 26 days, the decay tended to saturate.

Meanwhile, according to the experimental results, we knew that the shorter length of the nanodevice would benefit the performance of the solar cell efficiency. Furthermore, a three-dimensional "nano-schottky-diode" arrays equivalent circuit model was constructed and used to explain the photo-sensing mechanisms. Through HSPICE simulation, the higher

solar cell efficiency can be obtained based on the ideal inference. In conclusion, the optimized device dimension could be chosen, and we found that the solar cell efficiency was up to 36.87 % in 6-layered PDDA-capped CdSe/ZnS QDs and Au NPs with 30 μm in width and 40 nm in length. The solar cell can achieve high efficiency based on the model calculation.

ACKNOWLEDGEMENTS

致謝

在碩士生涯中，首先要感謝我的兩位指導教授吳重雨校長和李耀坤教授，兩年多來對我的耐心指導與諄諄教誨，使我於跨領域前瞻的研究過程中，得到源源不絕的靈感與專業知識的奧援，帶領我順利完成碩士學業。其次要感謝許鉦宗教授、張國明教授擔任我的口試委員，並提供許多寶貴的建議，使這篇論文的內容更加完整，真的很感謝您們！

接下來要感謝李耀坤老師實驗室的靜萍學姊，給予我最大的幫忙與經驗分享，以及多次提供 NPs、QDs 和實驗支援的沈模沅學弟，讓我在研究的路途中走得更加順利。感謝奈米所陳振嘉學長於實驗上的建議和協助；羅正忠老師實驗室的智仁學長、佳樺、欣富、小陸，在製程技術上幫助我解決很多問題；百忙中抽空幫我拍 SEM 的材料所學姊陳蓉萱；NDL 陳世哲先生協助我完成光罩設計與製作；刁維光老師實驗室的呂學沛學長提供 solar simulator，感謝你們總給予我不求回報的幫助，真的很謝謝你們。當然也要感謝『奈米電子與晶片系統實驗室』的林俐如、王文傑、虞繼堯、蘇烜毅、黃祖德、陳旻珓、陳勝豪、楊文嘉、蔡夙勇、陳緯明、金毛、顏承正等學長姊們，在各方面給予許多幫助與指導，也感謝碩士班的同學們，謝謝神童傳授的秘技、維德、順哥、阿部忠、晏維、宗裕、豪哥、松諭、巧伶學長姊在學業上給予我的指導。感謝我們 group 的小帆、宅帥、建名、諶哥，感謝北鴨與世範陪我一起健身，感謝幫我買衣服的小州哥，強大的歐威，人生經驗豐富的歐陽，偷偷來的科科和宗恩，FTP 很大的紹岐，強力嘴炮+小熱褲的塔哥與暴力老大，還有禽獸和帛哥。此外，謝謝筱妊、潮男昀、a-dair、天哥、林良、昕爺、kitty、佳琪、彥偉、小狗達、癡漢、明翰、慧君、子薰等學弟妹們，也感謝永遠的室友主任和老爹，大家在苦悶的碩士生活中帶給我許多歡笑。

最後，要獻上最深最深的感謝給我的父母親，詹明章先生與陳玉秀女士，我的妹妹蕙慈和孟儒，提供最棒的環境，使我無後顧之憂地專注於學業上。還要感謝貼心的彥琳，當我面臨龐大壓力時給予我的鼓勵與支持。感謝所有的親朋好友，謝謝你們的關心，成為我最大的後盾。

詹政邦

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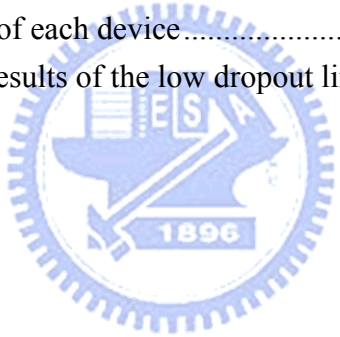


FIGURE CAPTIONS

Chapter 3

CHAPTER 1

INTRODUCTION

1.1 Background

Based on the fundamental chemistry, biotechnology and material science, people over three decades have developed powerful disciplines and knowledge that allow the engineering of advanced and functional substances for application in highly integrated electronic, mechanical and optical nanodevices, sensors or catalysts. “Where Nature finishes producing its own species, man beings, using natural things and with help of this nature, to create an infinity of species,” Nobel laureate Jean-Marie Lehn used these words to give an overlook of the future of highly interdisciplinary supramolecular chemistry [1]. Accordingly, when using natural things to produce new substances for further application, it is very important to utilize their nature. Another significant property of nanotechnology is its “interdisciplinary nature.” Chemistry is the central science for the development of applied disciplines such as material science and biotechnology as shown in Figure 1.1. Material science, which is based on classic chemical research fields and engineering technologies, has led to enormous advances modern material. Combined with tailored biomolecules, like proteins, and nucleic acids, people are able to develop future nanodevices composed of various advanced modern materials [1].

Nobel physicist, Richard Feynman, once pointed out morn than 40 years ago, “There is plenty of room at the bottom”, which best describes the central idea of nanotechnology [1]. The conventional *top-down* processes are always the main concepts in the development of human civilization. As human technology develops, people tend to fabricate more and more delicate tools or functional devices. However, this strategy will eventually reach a limit that people cannot easily go beyond based on available technologies, such as photolithography

currently on the range of about 32 nm, which is already the highest level of conventional top-down technology. In the foreseeable future, any further miniaturization process will lead to much more complicated problems, like quantum effects and power consumption, which will consequently cost much more effort to make a step to further miniaturization. As a result, it is reasonable and critical to change the way people used to develop thing from conventional *top-down* to *bottom-up* processes. Compared to top-down processes, bottom-up processes concern the assembly of molecular and colloidal building blocks to produce larger (10~100 nm) and functional devices. The forces that make the assembly to happen are similar to those that involve in the interaction between molecules, for example, hydrogen bonds, coulombic force, and van der Waals forces.

When talking about nanotechnology, it is referring to the size scale from 10 nm to 100 nm. As shown in Figure 1.2, the conventional top-down processes can hardly construct structure smaller than 32 nm, while the bottom-up processes also reach a limit about 2~5 nm. However, substances which are equal to or smaller than 2~5 nm are too small to be controllable and useful. Obviously, there is a gap existing in the range about 10~100 nm and both biotechnology and material science naturally meet at the same scale, which is about 5~200 nm. According to Christof M. Niemeyer, the two different compounds appear to be suited for addressing the gap: (1) biomolecular components, such as proteins and nucleic acids, and (2) colloidal nanoparticles comprised of metal and semiconductor materials [1].

In sum, nanotechnology today is best characterized by its interdisciplinary study. The combination of advanced materials (like nanoclusters and ceramics) and tailored biomolecules (like nucleic acids and proteins) will lead to the creation of future nanodevices.

Search for environmentally clean alternate energy resources is also an important issue at present. People effort to design ordered assemblies of semiconductor and metal nanoparticles as well as carbon nanostructures to utilize solar radiations. It is an ideal renewable energy but requires new initiatives to harvest incident photons with higher efficiency, for example, by

employing nanostructure composed of semiconductors and molecular assemblies

Recent efforts to design ordered assemblies of semiconductor nanostructures, metal nanoparticles, and carbon nanotubes pave the way for designing next-generation energy conversion devices. New initiatives are needed to harvest photons employing nanostructured semiconductors and molecular assemblies [2]. Hence, nanotechnology and synthesis techniques can be combined with solar cell to meet people's demand of green energy in the near future.

1.2 Reviews on Nanodevice

Recently, several methods to construct nanodevices have been proposed. One of them is the self-assembly techniques, which provide a means to realize structure such as quantum dots, nanoparticles, and other electronics or optoelectronic device configurations. Because these techniques do not rely on lithography to realize the specific nanostructures and assemblies, they can represent efficient, high throughput fabrication approached. For self-assembled semiconductor structures, the electronic device functionality has been limited by the difficulty in achieving suitable interfaces for passivating and contacting the resulting islands or dots [3]. A patterning method of trapping and deposition of nanoparticles in a submicron narrow gap has been developed. It was able to fabricate an ultra small light source to optical devices [4].

Now, we will review on the state of current and coming solar photovoltaic technology and their further development. Recent advances in concentrators, new directions for thin films, and materials/device technology issues are discussed in terms of technology evolution and progress. Insights to technical and other investments needed to tip photovoltaic to its next level of contribution as a significant clean-energy partner in the world energy portfolio [5]. The research progress over the past 25-30 years has been substantial and steady as shown in Figure 1.3.

On the basis of nanoparticle technology, nanoparticle or nanocrystal solar cells are

developed and researched. Nanocrystal solar cells or quantum dot solar cells are solar cells based on a silicon substrate with a coating of nanocrystals. Quantum dot based photovoltaic cells based around dye-sensitised colloidal TiO_2 films were investigated in 1991 [6] and were found to exhibit promising efficiency of converting incident light energy to electrical energy, and were found to be incredibly encouraging due to the low cost of materials in the search for more commercially viable/affordable renewable energy sources. A single-nanocrystal (channel) architecture in which an array of single particles between the electrodes, each separated by ~1 exciton diffusion length, was proposed to improve the device efficiency [7] and research on this type of solar cell is being conducted by groups at Stanford, Berkeley and the University of Tokyo.

Recent research in experimenting with lead selenide (PbSe) semiconductor, as well as with cadmium telluride (CdTe), which has already been well established in the production of "classic" solar cells. Other materials are being researched as well. These materials are unlikely to have an impact in generating clean energy on a widespread basis, however, due to the toxicity of lead and cadmium.

On the other way, people effort to design ordered assemblies of semiconductor and metal nanoparticles as well as carbon nanostructures to utilize solar radiations. Dye sensitization of mesoscopic TiO_2 has been widely used, and the power conversion efficiency up to 11% has been achieved for such photochemical solar cells. Figure 1.4 depicts the assembled TiO_2 and CdSe quantum dots using bifunctional surface modifiers of type HS-R-COOH [8]. In additional, an ultrathin donor-acceptor solar cell composed entirely of inorganic nanocrystals has been introduced. This type solar cell is stable in air, and post-fabrication processing allows for power conversion efficiencies approaching 3% in initial tests. The photovoltaic devices described used rod-shaped CdSe and CdTe NCs as shown in Figure 1.5(a) and (b) [9].

1.3 Motivations

In previous works, the photo-sensing nanodevice composed of negative-charged Au nanoparticles and positive-charged CdSe/ZnS quantum dots has been developed and proposed [10]. However, there are several drawbacks or limits in previous design. For example, the solar cell efficiency is very low, and they have reliability and stability issues [11].

For the purpose of higher solar cell efficiency, the shorter length electrodes and different-sized QDs are applied in the proposed solar cell nanodevices based on "self-assembly technology." Meanwhile, a low voltage, low drop-out regulator is designed to target the low power application and integrated with the proposed solar cell nanodevice. On other hand, to construct an equivalent circuit model of the proposed nanodevice is also one of the goals in the work.

1.4 Thesis Organization

In chapter 1, the background has been introduced in section 1.1, including the basic concepts, the definition, current trend of nanotechnology development in the world, and several assembly methods of NPs on silicon substrate. Then some reviews on the nanodevices and photovoltaic technologies in recent years have been discussed in section 1.2. At last, the motivations of this work and thesis organization are proposed in section 1.3 and 1.4.

In chapter 2, the fabrication technology will be discussed, including the process flow and the nanodevice structure design concepts. In section 2.1 and 2.2, the synthesis of Au NPs and PDDA-capped CdSe/ZnS QDs will be introduced. Then in section 2.3, the optical and electrical properties, including the mechanism of photoconductivity of PDDA-capped CdSe/ZnS QDs and the electron transportation between NPs will be demonstrated. In section 2.4, the design and fabrication flow of the advanced nanodevice structure will be proposed. And in section 2.5, the self-assembly process of Au NPs and PDDA-capped CdSe/ZnS QDs

will be discussed. And several reaction environment factors will be investigated in section 2.6.

In chapter 3, the experimental results will be showed and discussed. First the measurement environment is introduced in section 3.1. Secondly the SEM images, optical and electrical properties, for example absorption / emission spectra of the proposed nanodeviced will be demonstrated in section 3.2. And then the nanodevice performance measurement will be showed and discussed in section 3.3. Next, an equivalent circuit model of the proposed nanodevice will be constructed in section 3.4.

In chapter 4, a low voltage, low drop-out linear regulator is designed to target the low power conditions and integrated with the proposed nanoparticle solar cell. In section 4.1, the system design considerations and relevant analysis will be introduced. The circuit blocks will also be showed in section 4.2. And then the simulation results and chip layout will be demonstrated in section 4.3. The proposed regulator system was successfully fabricated in TSMC 1P6M 0.18-μm CMOS process. Finally the measurement results will be showed and discussed in section 4.4.

Chapter 5 brings forth the conclusions of the research as well as implications thereof. Finally, the chapter ends with a few concluding statements pertaining to the research as well as recommendations for future work in the area.

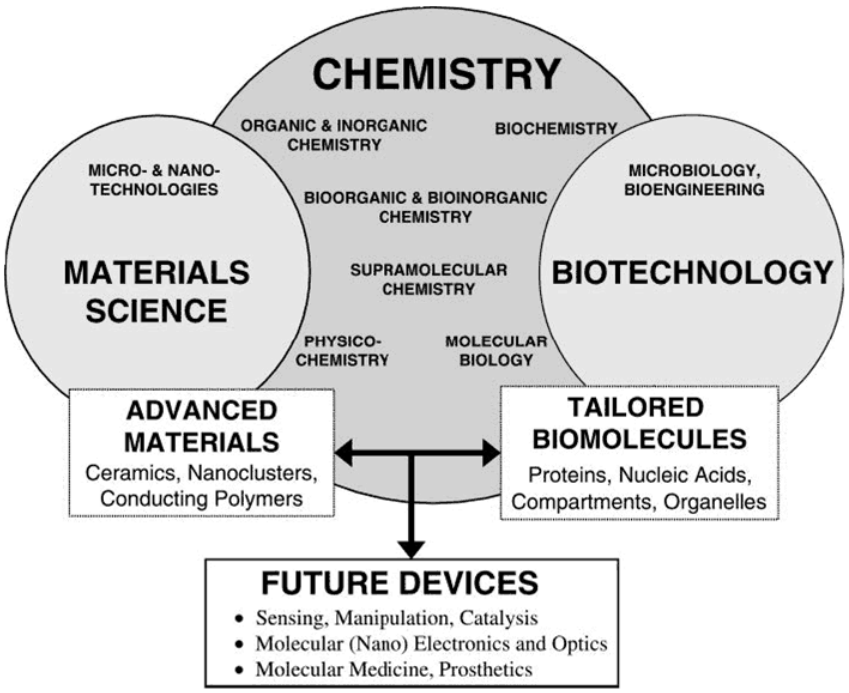


Figure 1.1 Chemistry is the central science for further applications such as materials science and biotechnology. The combination of advanced materials and tailored biomolecules will produce the future nanodevices [1].

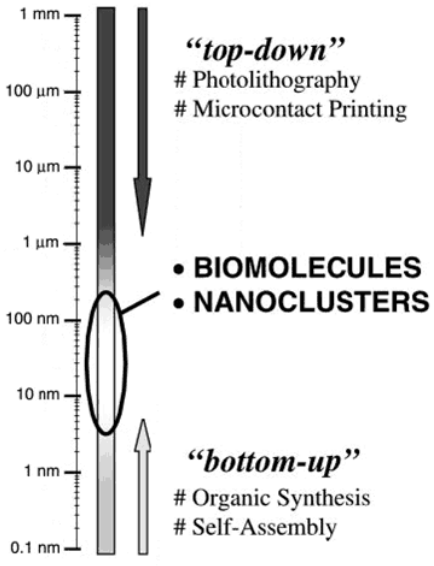


Figure 1.2 A gap currently exists in the engineering of small-scale devices. The top-down processes will have their limit below 100 nm, and the bottom-up processes will also have a limit at 2~5 nm. The gap will be filled by nanoclusters and biomolecules [1].

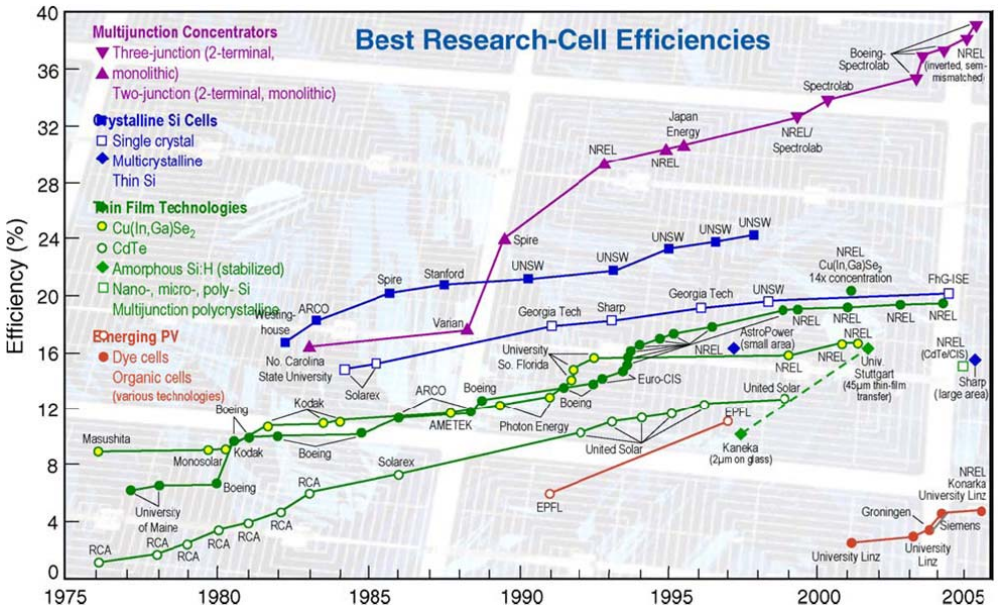


Figure 1.3 The efficiency evolution of best research cells by several of technology types. This figure identifies those cells that have been measured under standard conditions and confirmed at one of the word's accepted centers for standard solar-cell measurements [5].

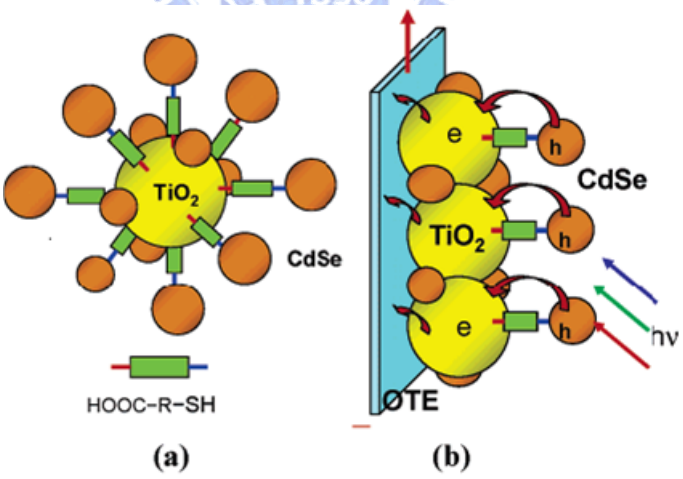


Figure 1.4 (a) Linking CdSe QDs to TiO2 particles with bifunctional surface modifier (HS-R-COOH); (b) Light harvesting assembly composed of TiO2 film functionalized with CdSe QDs on Optically Transparent Electrode (OTE) [8]. (Not to scale)

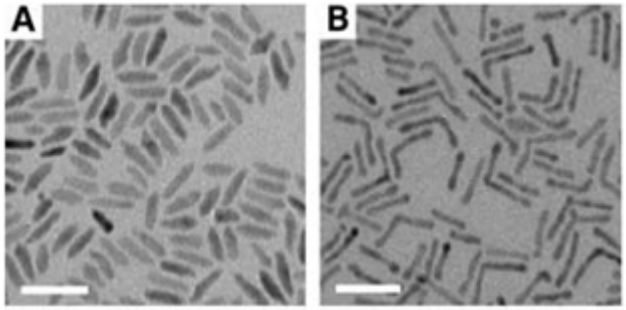


Figure 1.5 Transmission electron micrographs of (A) CdSe and (B) CdTe nanocrystals in ths investigation [9].

CHAPTER 2

NANOPARTICLE SYNTHESIS AND NANODEVICE FABRICATION TECHNOLOGY

In this chapter, the synthesis of Au nanoparticles and CdSe/ZnS quantum dots (QDs) will be discussed in section 2.1 and 2.2 respectively. And then the physical characteristics of the nanodevice will be demonstrated in section 2.3. In section 2.4, two kinds of electrode structures and nanodevice fabrication technology will be proposed. In section 2.5, the self-assembly process and experiment flow will be introduced. Finally, several reaction environment factors will be investigated in section 2.6.

2.1 The Synthesis of Citrare-Capped Au Nanoparticles

Au NPs with ~ 15 nm diameter were prepared by citrate reduction of $HAuCl_4$ as described in literature [12]. The pale yellow $HAuCl_4$ solution (1 mM, 500 mL) was prepared and brought to reflux while stirring for 20 minutes. A solution of citric acid (38.8 mM, 50 mL) was then quickly injected into the flask. The color of the solution changed from pale yellow to deep red indicating the formation of Au NPs. After color changing, the solution was kept in reflux for additional 20 minutes and then standing in room temperature for another 30 minutes. Finally, the solution was filtered through 0.45 μm nylon filter. The flow diagram of the Au NPs solution preparation is shown in Figure 2.1. The close photograph of the Au NPs solution is shown in Figure 2.2(a), (left). The TEM image of the approximately 15 nm diameter Au NPs is shown in Figure 2.3(a) and the UV-visible absorbance spectrum of Au NPs solution is shown in Figure 2.3(b).

2.2 The Synthesis of AET-CdSe and PDDA-CdSe Quantum Dots

The emission efficiency, spectrum and time evolution of QDs are strongly affected by the surface. A better surface structure of QDs can provide higher stability, higher quantum yield and longer lifetime. Mostly the CdSe QDs lose a large portion of emission efficiency because of electron leakage resulting from the surface defect. Therefore, ZnS layer, a large band gap semiconductor, is used to passivate the surface and improve the quantum yield of CdSe NPs. The band gap diagram and the surface structures of CdSe/ZnS QDs are shown in Figure 2.4(a). It shows the PL intensity spectrum, which confirms the superior quantum yield property of CdSe/ZnS structure over the other two structures, CdSe and CdSe/CdS. The approximately 5 nm diameter fluorescent water-soluble ((PDDA)-coated) and (2-aminoethane thiol (AET)-coated) CdSe/ZnS QDs are supported from *Prof. Yaw-Kuen Li's laboratory, institute of molecular science, National Chiao Tung University, Taiwan*. The surface of the AET-coated CdSe/ZnS QDs had positive-charged amino groups ($-NH3^{+}$).

- **Synthesis of water-soluble AET-capped CdSe/ZnS QDs**

In order to prepare positive charge on the QDs surface, the water stabilized amine terminating QDs ($NP-NH_2$) was fictionalized. Adding methanol washed off the HDA stabilizing layer and rendered a cloudy suspension which was centrifuged and the pellet containing QDs were washed with methanol 4 times to re-dissolve into chloroform. 1.0M 2-aminoethane thiol (AET) was added to the above solution and allowed to react for 2hrs. When ZnS capped CdSe QDs were reacted with AET, the mercapto group in AET bind to the Zn atoms and render the QDs hydrophilic, in addition to facilitating further functionalization possibilities. After the reaction, excess AET was washed off with methanol/chloroform mixed solution and store into the D.I. water.

The close photographs of the AET-CdSe/ZnS QDs solution are shown in Figure 2.2(a),

(right). Figure 2.2(b) shows the close photographs of the mixture of 100 μL Au NPs solution and 100 μL AET-modified CdSe/ZnS QDs solution just after mixing (right), the mixture after standing 6 hrs (middle) in room temperature, and the mixture after standing 5 days in room temperature (left). As we can see, the color of mixture just after mixing was like that of Au NPs solution. However, after 6 hrs, it became dark purplish red. After 5 days, there was obvious precipitate at the bottom and the supernatant became pale yellow. The TEM image of the approximately 5 nm diameter CdSe/ZnS QDs is shown in Figure 2.3(a) and the UV-visible/PL spectra of CdSe/ZnS QDs solution is shown in Figure 2.3(c). The detailed modification processes of AET-capped CdSe/ZnS QDs are shown in Figure 3.5.

2.3 The Physical Characteristic of Au Nanoparticles and CdSe/ZnS Quantum Dots

Recently, many nanoparticles (NPs) have been proposed and improved significantly. In order to achieve the nanodevices that have good performance, we must realize the electrical and optical properties as well as the size and the synthesis of the NPs. Metal particles comprise a fundamentally interesting class of matter in part because of an apparent dichotomy that exists between their sizes and many of their physical and chemical properties. For example, Au particles may be synthesized in diameters that span from the macroscopic down to the molecular scale (0.8 μm). Across almost the entire size regime, however, their electrical and optical behaviors are described with relatively simple classical equations, rather than the quantum mechanical concepts required understanding molecular entities. The classical free electron theory combined with optical constants for bulk gold is employed to successfully model the intense visible extinction of Au NPs. Moreover, the electrical and optical properties of metal particles can be tuned considerably simply by adjusting the size, shape, or extent of aggregation of the particles. For example, a typical solution of 13 nm diameter Au NPs is red

in color and exhibits a surface plasmon band centered at 518-520 nm. After aggregation, the extended polymeric Au NPs/polynucleotide aggregate shows a red to purplish blue color change in solution, due to a red shift in surface plasmon resonance of Au NPs [12]. The optical property of Au NPs is dominated by collective oscillation of conduction electrons resulting from the interaction with electromagnetic radiation. The electric field of incoming radiation induces the formation of a dipole in the NP. A restoring force in the NP tries to compensate for this, resulting in a unique resonance wavelength. The oscillation wavelength depends on particle size, particle shape and surrounding medium. [13]

In semiconductor nanocrystals, however, exhibit a wide range of size-dependent properties when the size regime is below 10 nm [14] [15]. Variations in fundamental characteristics ranging from phase transitions to electrical conductivity can be induce by controlling the size of the crystals [15]. There are two major effects to explain these size variation properties in nanocrystals. First, the number of surface atoms is a large fraction of the total atoms of a single nanocrystal. The high surface-to-volume ration will make a contribution to variations in thermodynamic properties of nanocrystals, such as melting point, and solid-solid phase transition. Second, nanocrystals with the same interior bonding geometry as the corresponding bulk material but with only a few hundred to thousand atoms exhibit dramatic size-dependent optical and electrical properties. These variations are because the density of states of electronic energy levels transforms as a function of the size of interior nanocrystal, known as quantization effects [15]. Nanocrystals lie in between the atomic and molecular limit of discrete density of electronic states and the extended crystalline limit of continuous bands.

The diagrams of density of states in metal and semiconductor nanocrystals are shown in Figure 2.6. In each case, the density of states is discrete at the band edges. The Fermi level is in the center of a band in a metal, and so kT will exceed the level spacing even at low temperature and small size. In semiconductor, however, the Fermi level lies between two

bands, so that the edges of bands dominate the low-energy optical and electrical behavior. Optical excitations across the gap depend strongly on the size, even for crystallites as large as 10,000 atoms. Besides, the HOMO-LUMO gap increases as the semiconductor nanocrystals become smaller (bellow 10 nm) [15].

In this work, we used positive-charged 2-aminoethane thiol (AET)-capped CdSe/ZnS (core/shell) NPs of approximately 5 nm in diameter as photoreceptors to detect lamination with above band gap photoexcitation [15]. We proposed two nanodevices composed of semiconductor QDs and/or metal NPs for self-assembly: (1) Au / AET-CdSe/ZnS. (2) Au / PDDA-CdSe/ZnS. However, some properties about CdSe QDs we must know that the **exciton Bohr radius r_b** is the spatial extent of the electron hole pair in material and is defined as

$$r_b = 4\pi\hbar^2\varepsilon / m^* e^2 \tag{2.1}$$

where ħ is the Plank's constant, ε is the permittivity in bulk material, and m* is the effective mass. For CdSe semiconductor, the electron's effective mass is 0.13 m_e and hole's effective is 0.45 m_e. So the exciton Bohr radius of CdSe is calculated to be 4.9nm [14] [16]. If the dimension of CdSe QDs is smaller than 4.9nm, the quantum confinement of electron hole pairs effects significantly. As size is reduced, the electron excitation shift higher energy, and there is concentration of oscillator strength into a few transitions [14]. The dynamic of the charge carriers in CdSe QDs have been in several reports. Monitored the electrons shuttling across the interface of CdSe QDs by femtosecond laser spectroscopy and showed that in CdSe QDs with no electron acceptors adsorbed on the particle surface, the excited electrons get trapped at the surface within 30 ps. Subsequently, electron-hole recombination takes place on a much longer time period > 10^{-7} s [17]. This is quite a useful knowledge for understanding the dynamics of electrons in CdSe QDs. The electrical transport properties of nanocrystals also depend strongly on size. On extended crystal, the energy required to add successive charges does not vary. In a nanocrystal, the presence of one charge prevents the addition of

another charge. Thus, in metal or semiconductor, the current-voltage curves of individual nanocrystal resemble a staircase, known as **Coulomb blockade effect** [15].

2.4 Nanodevice Fabrication Technology

For the purpose of measuring and utilizing the power generated from the nanodevices, the electrodes are required. Hence, the electrodes were prepared before the self-assembly process. First, the nanodevice structure is introduced, and the cross-section is illustrated in Figure 2.7. The aluminum is used as the conductor to collect the current. And the oxide layer is utilized as the dielectric to prevent the substrate current flow to the aluminum in case of incorrect result when measuring.

However, in previous work, some problems were generated when the self-assembly process was executed. As the Figure 2.8(a) shown, according to the SEM photograph, some NPs and QDs assembled on unexpected region [11]. The anticipated patterns of the electrodes were disturbed by connecting with other electrodes through the thin film composed of NPs and QDs. This phenomenon may be caused by the presence of the –OH groups on the surface of the electrodes, which can be modified by TMSPED molecules, making them suitable sites for NPs assembly. In order to solve this problem, the lift-off technology was utilized to remove the unexpected NPs and QDs.

The proposed nanodevices were fabricated in *National Nano Device Laboratory, Taiwan.* The fabrication flow, including the self-assembly process which will be introduced in next section, is illustrated in Figure 2.9, and the corresponding mask layout view is shown in Figure 2.10. The dimensions of all nanodevices are list in Table 2.1.

On the other hand, it should be possible to further improve the performance of quantum dot solar cell by optimizing the light absorption properties of the nanostructure. Because semiconductor QDs such as CdSe with tunable band edge offer the opportunities to harvest

light energy in the entire region of solar light. One such approach under consideration is the construction of wideband solar cell, which employs an ordered assembly of PDDA-capped CdSe/ZnS QDs of different diameters. Smaller-sized QDs (larger band gap) absorb the portion of the light with smaller wavelengths (blue region). Light with longer wavelengths (red region), which is transmitted through the initial layer, is absorbed by subsequent layer, and so on. By creating an ordinary gradient of quantum dots of different sizes, it should be possible to increase the effective capture of incident light. Based on the above theorem and assumption, the nanostructure could be modified as shown in Figure 2.11. The upper layer is smaller-sized and the bottom layer is larger-sized PDDA-capped CdSe/ZnS QDs.

2.5 Self-Assembly Process for Advanced Nanodevice Structure

In previous chapter, we have discussed the forces that direct the assembly of NPs is similar to those involving in the interaction between molecules, such as hydrogen bonds, coulombic force, and van der Waal force. In this work, we utilize the coulombic force system control the assembly of NPs on the silicon or ITO glass. In coulombic force system, we take advantage of the positive or negative charge on the surface of NP to induce repulsion or attraction force between different NPs or between NPs and the substrate. The repulsion force will prevent the NPs from random aggregation before assembled on the substrate. Based on the coulombic force, we are able to construct the structure of advanced nanodevice on the silicon substrate effectively. The overall self-assembly process of Au NPs / PDDA-capped CdSe/ZnS QDs on the substrate by ionic interaction system is shown in figure 2.12.

Now, the experiment flow will be introduced below. In order to modify the electrode surface with positive charges, the electrodes were immersed in 10% N-[3-(trimethoxysilyl)propyl]-ethylene diamine (TMSPED)/ deionized (DI) water solution over night to make the electrode surface provide amino groups ($-NH_3^+$) as the figure 2.12(a)

shown [18]. After immersion, the samples were cleaned by plenty of DI water to remove excess TMSPED staying on the surface, followed by dipping in dilute HCl solution for 3 seconds to protonate the amino groups. Finally, the samples were cleaned by using plenty of DI water for several times and dried. Subsequently, the TMSPED-modified samples were immersed in the citrate-capped Au NPs (~15nm) solution for 12 hours to make the negative-charged ($-COO^-$) Au NPs self-assembly on the positive-charged ($-NH_3^+$) substrate by ionic interaction. Therefore, Au NPs were coated on the entire substrate.

Next, the most important step of the experiment is to lift off the unexpected part where the Au NPs were on the photoresist. According to previous work, the acetone was used in lift-off process to dissolve the photoresist and brought out the substance attached to the photoresist as shown in Figure 2.12. And the acetone should not destroy the nanostructure [11]. Then the samples were immersed in the acetone for 5 minutes. The Au NPs on the photoresist were removed with the photoresist. After lift-off process the nanostructure is shown in Figure 2.13. And then, the samples were immersed in the Au NPs solution for 12 hours again to confirm if the Au NPs were coated with high density.

After 12-hour-immersion, the samples were cleaned by D.I. water for several times to remove free Au NPs and then immersed in PDDA-capped CdSe/ZnS QDs for 12 hours. So the positive-charged ($-NH_3^+$) QDs self-assembled to negative-charged ($-COO^-$) Au NPs also by ionic interaction. Theoretically, this process could be repeated for several times to form layers of closed packed PDDA-capped CdSe/ZnS QDs and Au NPs nanostructures. As a result, this nanostructure can be used as the photovoltaic nanodevice. The experimental results will de discussed in the next chapter.

2.6 Reaction Environment Investigation

There are several environmental factors which would have effects on the nanostructure, for example, reaction temperature and reaction time. These effects should be optimized.

Accordingly, some experiments to affirm the optimum reaction conditions for the nanodevices to fabricate were executed first.

As a matter of fact, to construct the nanostructure is like to build the building. The base of the nanostructure should have higher density. Therefore the first layer, Au NPs, plays an important role in self-assembly process. If the density and quality of the first Au NPs thin film is high, the second and subsequent layers would also get high.

Hence, two experiments were executed. One is to observe the reaction time effect on the nanostructure construction. The other is to investigate the reaction temperature effect. And then SEM photograph of the nanodevices helps us to determine which conditions are suitable.

In previous work, an experiment was to investigate the temperature effect on the nanostructure construction. Hence, two pieces of p-type silicon wafer was prepared. One was to be coated with Au NPs and PDDA-capped CdSe/ZnS QDs as a 2-layer basic nanostructure in the room temperature environment. The other was to be coated in the same way, but in the 4°C reaction environment. Figure 2.16 shows the experiment outcomes. As the Figure 2.14(a) shown, the nanostructure which was constructed on condition of the room temperature got lower density.

The other experiment is to observe if the different reaction time influence the nanostructure. Therefore, two pieces of quartz glasses were prepared. One was to be coated with Au NPs and PDDA-capped CdSe/ZnS QDs as a 4-layer basic nanostructure for 4 hours per layer. The other was to be coated in the same way, but 12 hours per layer reaction period. The result is shown as Figure 2.15. Figure 2.15(a) is the nanostructure that was fabricated with 4 hours reaction time per layer. Figure 2.15(b) is the nanostructure that was constructed with 12 hours reaction time per layer. As a result, the 12-hour-reaction-time one got high particle density. It benefits the nanodevice construction.

In conclusion, lower temperature and longer reaction period would benefit nanostructure. Therefore, these two factors would be adopted in the nanodevice fabrication technology.

Table 2.1 The dimensions of all horizontal electrodes fabricated in NDL are list in this table.

(unit:μm)

Pad Description				
Pad_7	Pad_8	Pad_10	Pad_11	
5x30	**0.5x30**	**1x30**	**2.5x30**	

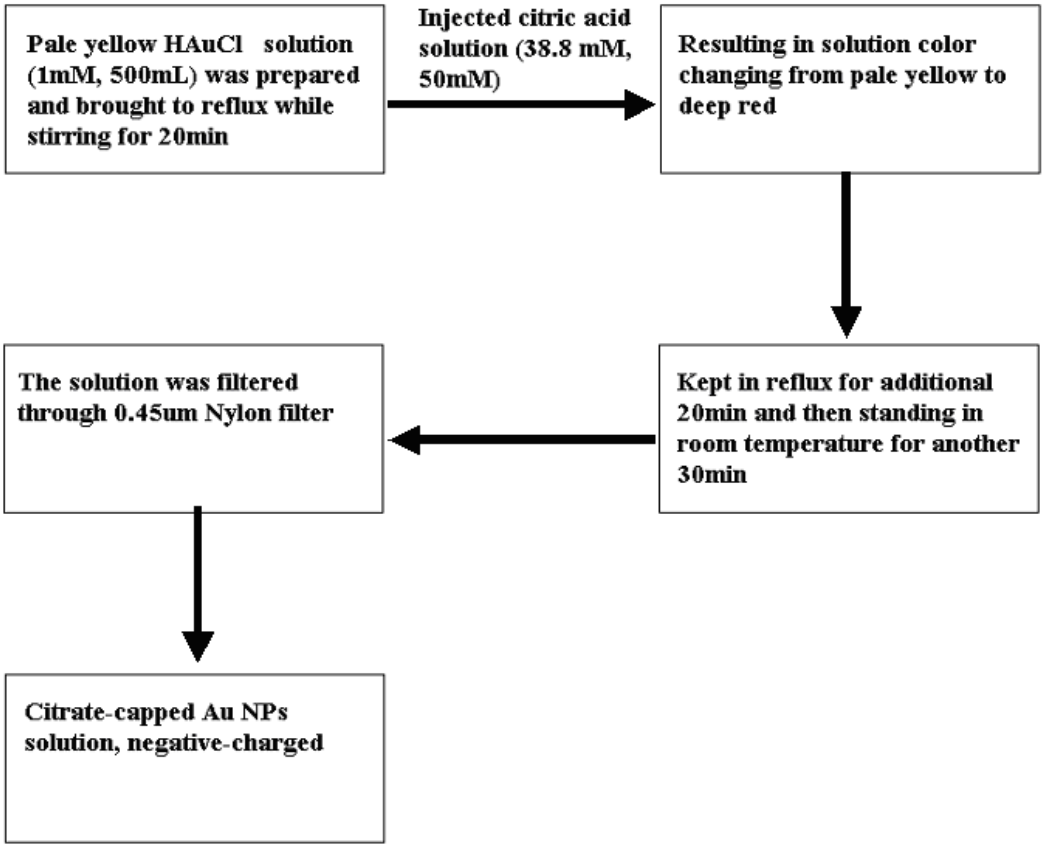


Figure 2.1 The flow diagram for preparing the citrate-capped Au NPs solution

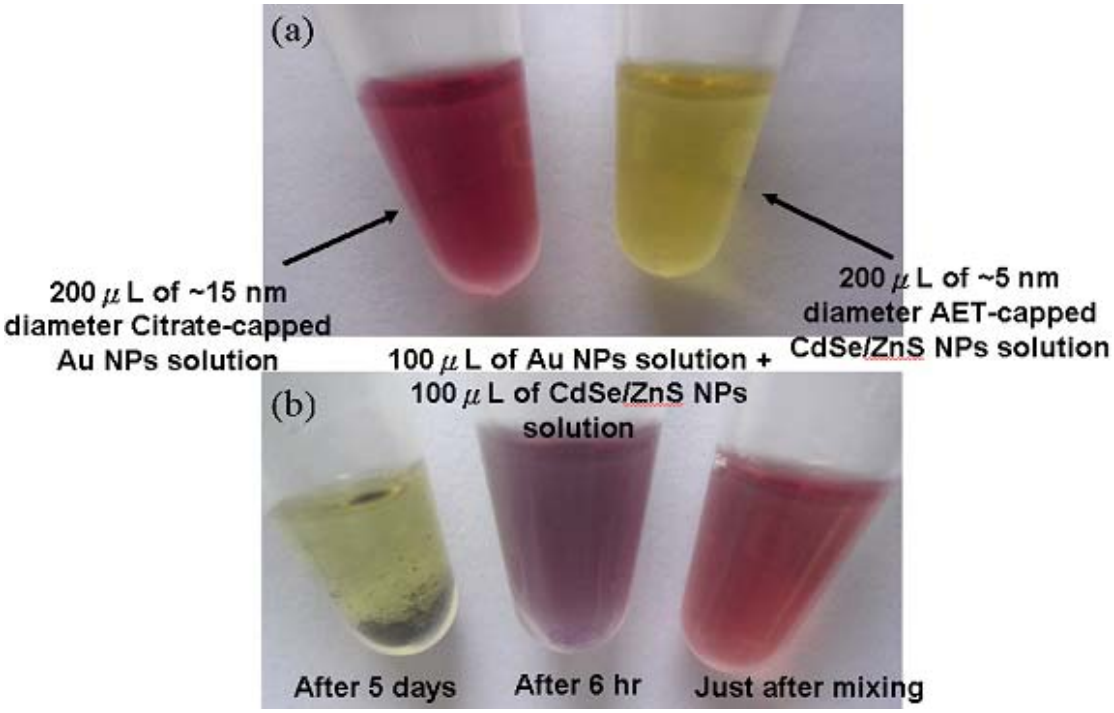
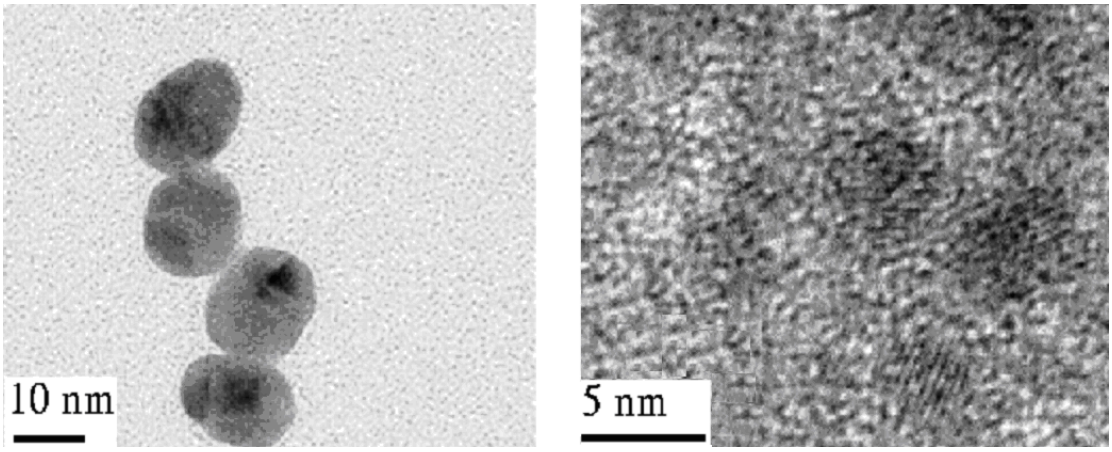
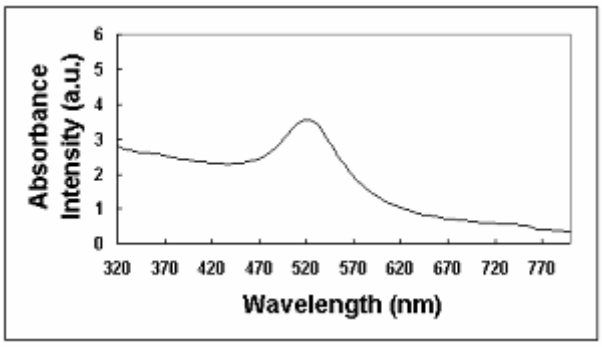


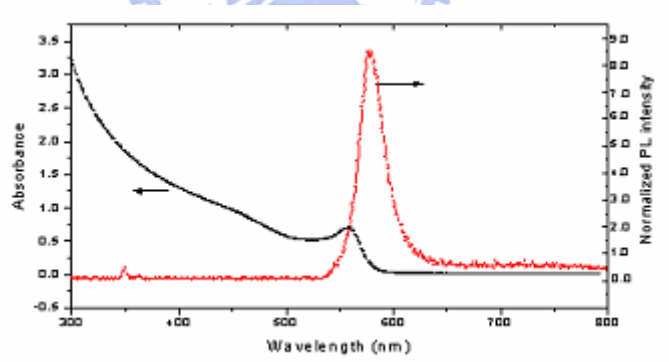
Figure 2.2 (a) The close photographs of 100 μL of approximately 15 nm diameter Au NPs solution + 100 μL DI water (left) and 100 μL of approximately 5 nm diameter AET-CdSe/ZnS NPs solution + 100 μL DI water (right). The Au NPs solution was in deep red while the AET-modified CdSe/ZnS NPs solution was in yellow. (b) The close photographs of the mixture of 100 μL Au NPs solution and 100 μL AET-modified CdSe/ZnS NPs solution just after mixing (right), the mixture after standing 6 hrs (middle) in room temperature, and the mixture after standing 5 days in room temperature (left). As we can see, the color of mixture just after mixing was like that of Au NPs solution. However, after 6 hrs, it became dark purplish red. After 5 days, there was obvious precipitate at the bottom and the supernatant became pale yellow.



(a)

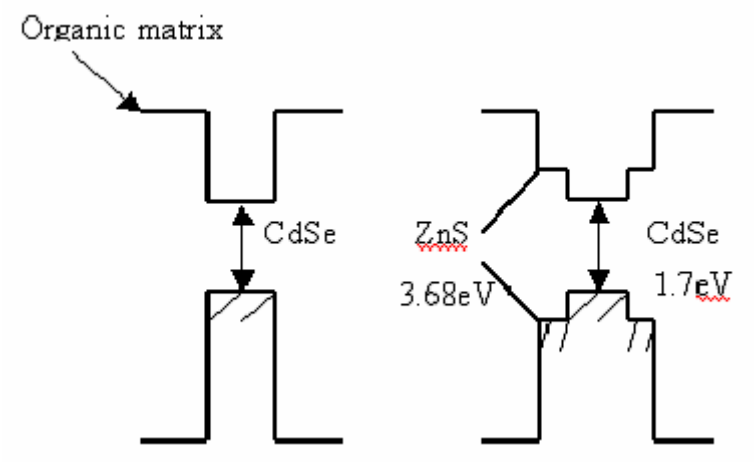


(b)

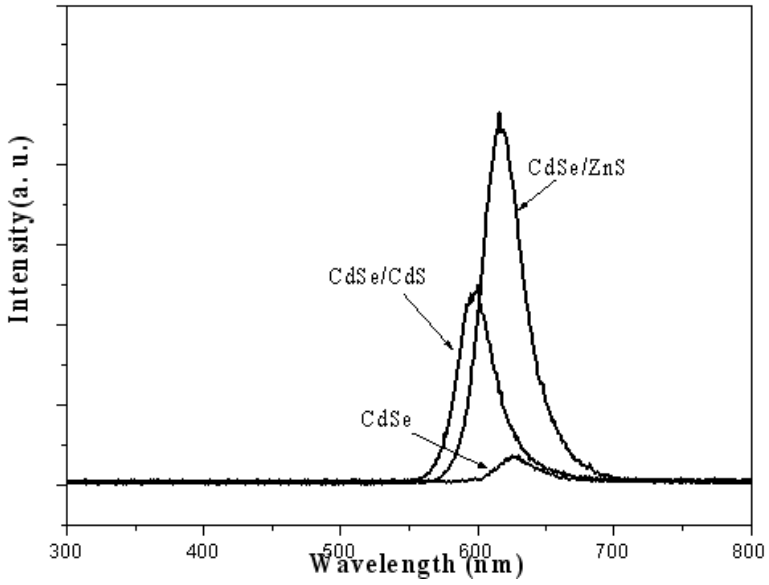


(c)

Figure 2.3 (a) The TEM image of Citrate-capped approximately 15 nm diameter Au NPs and the TEM image of AET-capped approximately 5 nm diameter CdSe/ZnS QDs. (b) The UV-visible spectrum of Au NPs solution. (c) The UV-visible and PL intensity spectrum of AET-CdSe/ZnS QDs solution.



(a)



(b)

Figure 2.4 (a) The band gap and surface structure diagram of CdSe/ZnS QD. (b) The PL intensity spectrum of different kind of surface capping method of CdSe QD

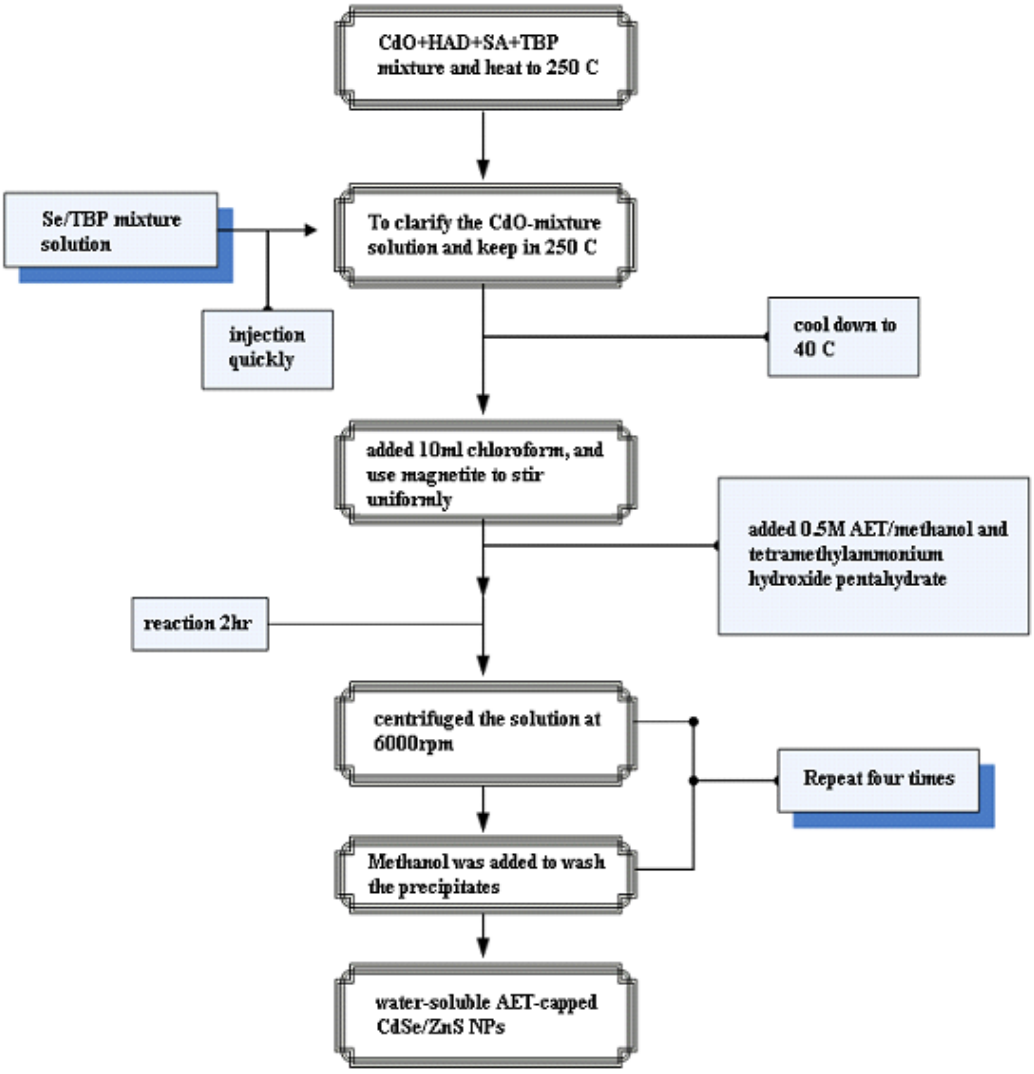


Figure 2.5 The flow diagram for preparing the AET-capped CdSe/ZnS QDs solution.

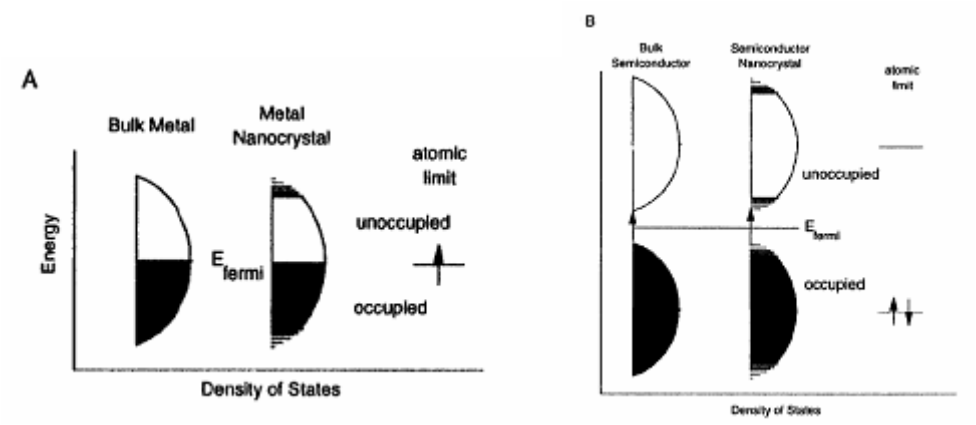


Figure 2.6 Density of states in metal (A) and semiconductor (B). In each case, the density of states is discrete at the band edges. The Fermi level is in the center of a band in a metal, and so kT will exceed the level spacing even at low temperature and small size. In semiconductor, the Fermi level lies between two bands, so that there is large level spacing even at large size. The HOMO-LUMO gap increases as the size of semiconductor nanocrystal decreases (bellow 10 nm). [11].

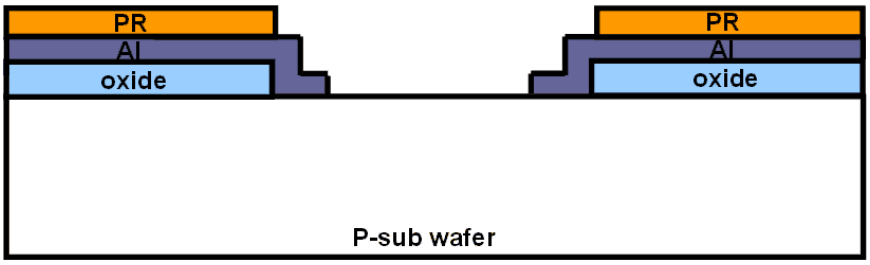
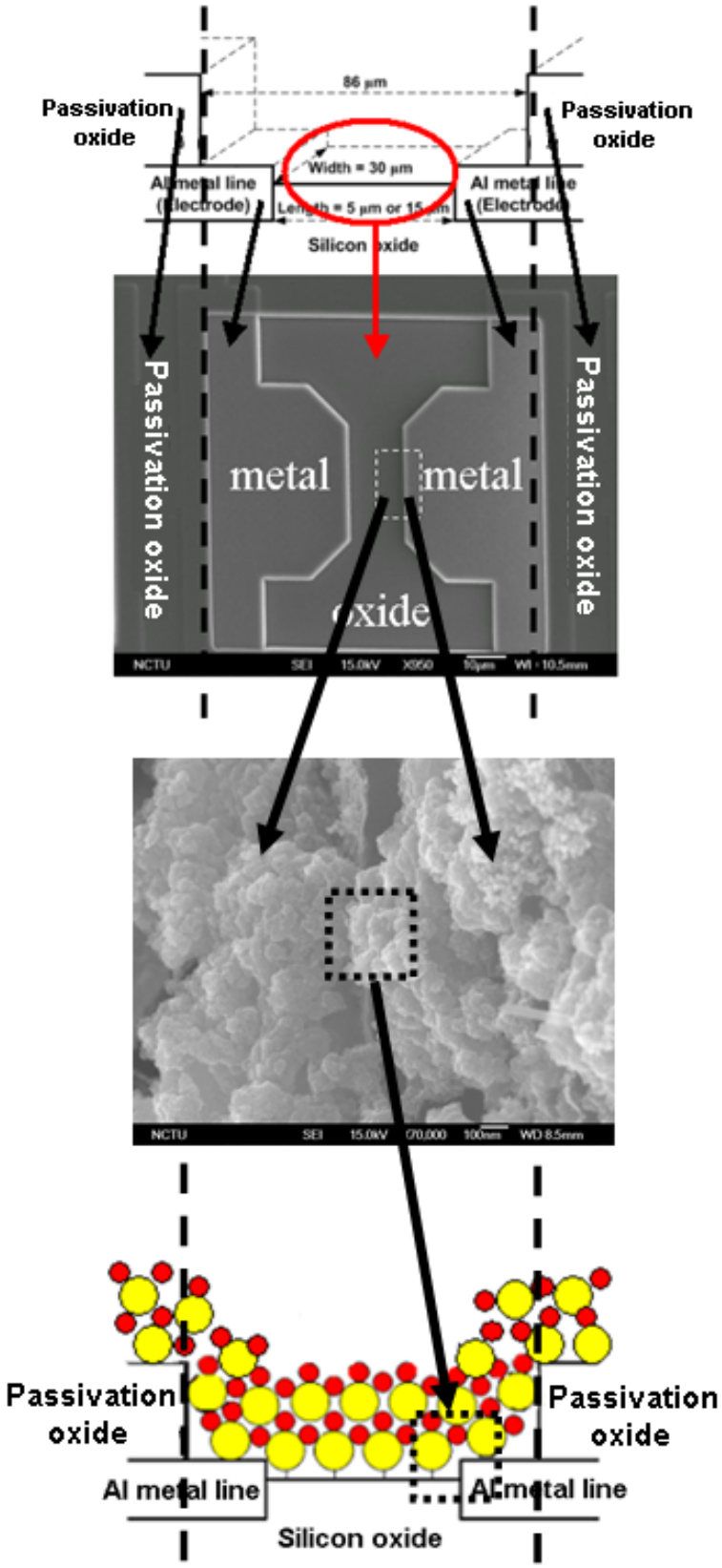
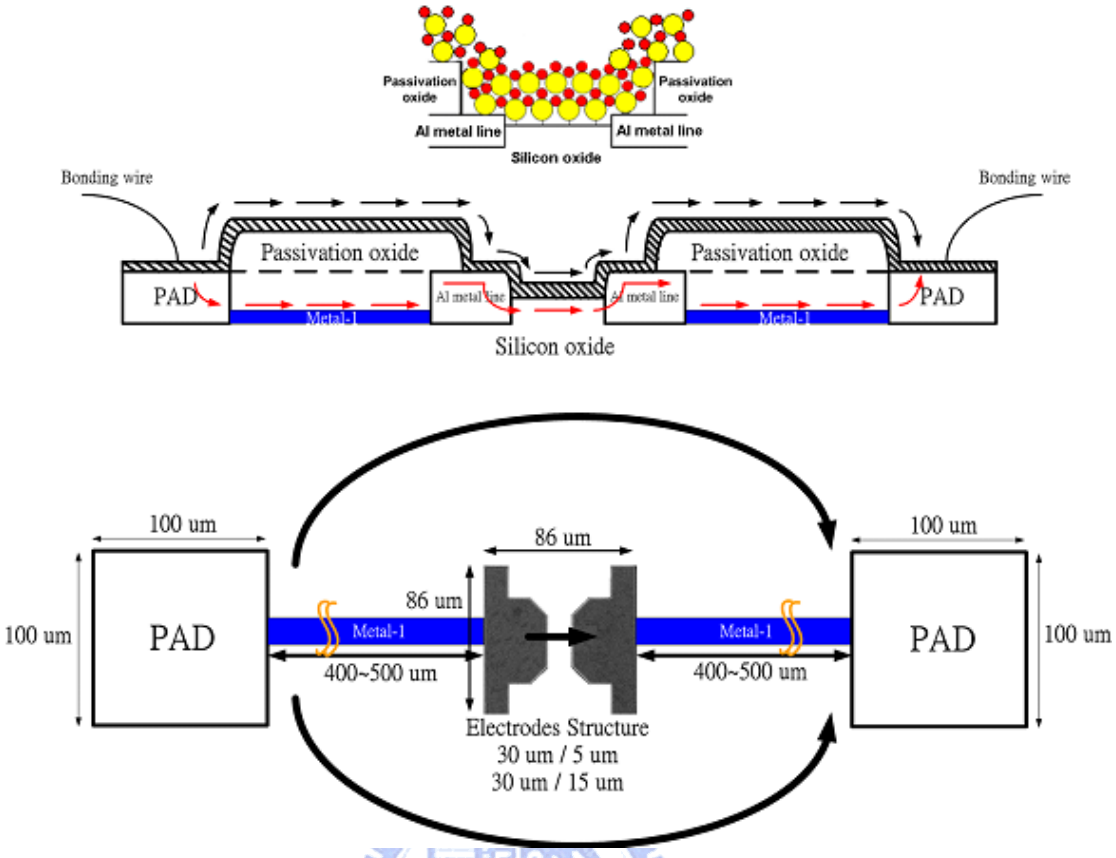


Figure 2.7 The cross-section view of the electrode structure and the PR is photoresistor for lift-off process.


86 μm
Passivation oxide
Passivation oxide
Width = 30 μm
Al metal line (Electrode)
Al metal line (Electrode)
Length = 5 μm or 15 μm
Silicon oxide
Passivation oxide
Passivation oxide
metal
metal
oxide
NCTU
SEI
15.0kV
X950
10μm
WD 10.5mm
NCTU
SEI
15.0kV
70,000
100nm
WD 8.5mm
Passivation oxide
Passivation oxide
Al metal line
Al metal line
Silicon oxide

(a)



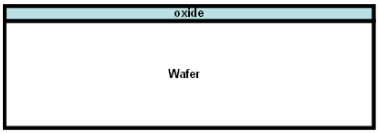
(b)

Figure 2.8 (a) The cross section figure of the electrodes structure corresponds to SEM image of the nanodevice-modified silicon chip. (b) The current flow trend of the nanodevice structure, and the electrodes dominated the source of the generated current. In the worse case, the whole chip area is considered, not the area of the electrodes. (The twill line means the thin film structure composed of NPs and QDs.).

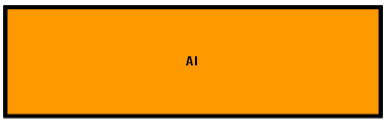

Wafer


oxide

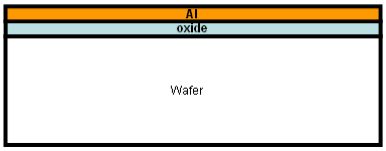

Wafer

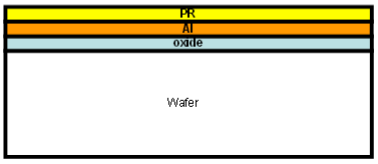

oxide
Wafer

(a) (b)

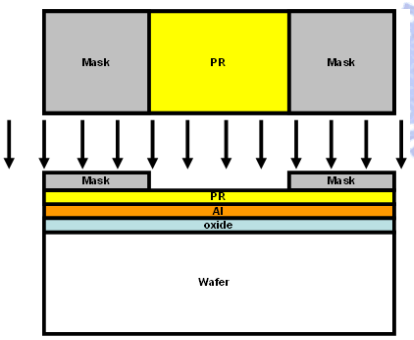

Al

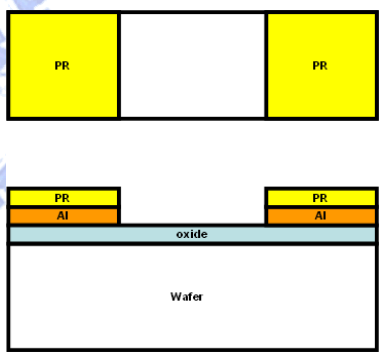

PR


Al
oxide
Wafer


PR
Al
oxide
Wafer

(c) (d)

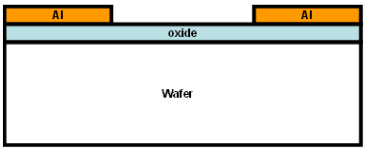

Mask
PR
Mask
Mask
Mask
PR
Al
oxide
Wafer

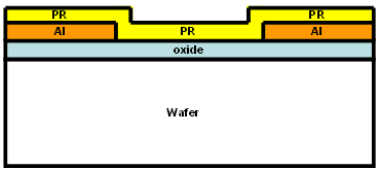

PR
PR
PR
Al
PR
Al
oxide
Wafer

(e) (f)


Al
Al


PR


Al
Al
oxide
Wafer


PR
PR
PR
Al
PR
Al
oxide
Wafer

(g) (h)

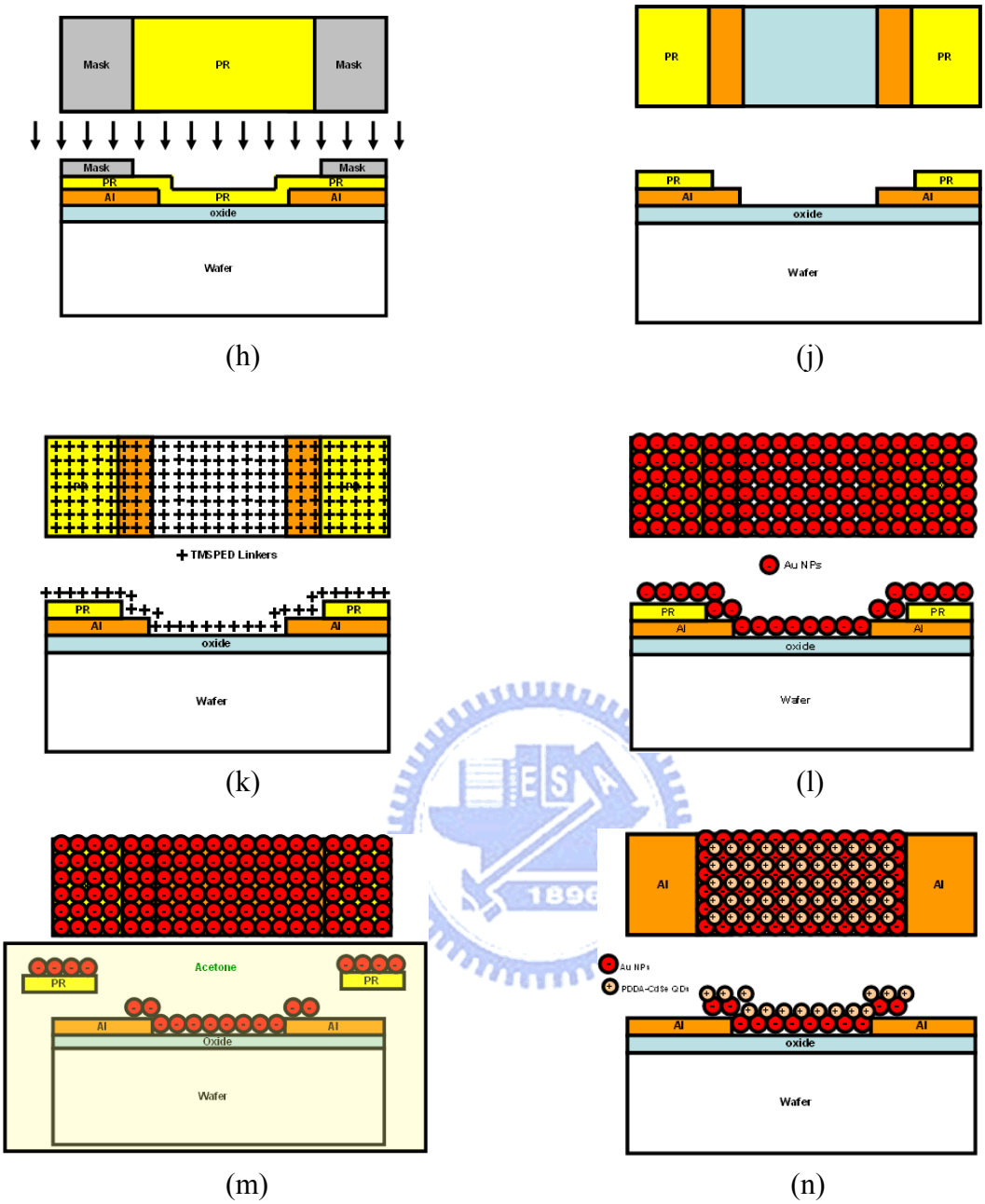


Figure 2.9 Fabrication flow of the proposed nanodevice (top-view and cross-section view). From (a) to (j) is the electrode fabrication process, and (k) to (n) is the nanostructure self-assembly (SAM) process.

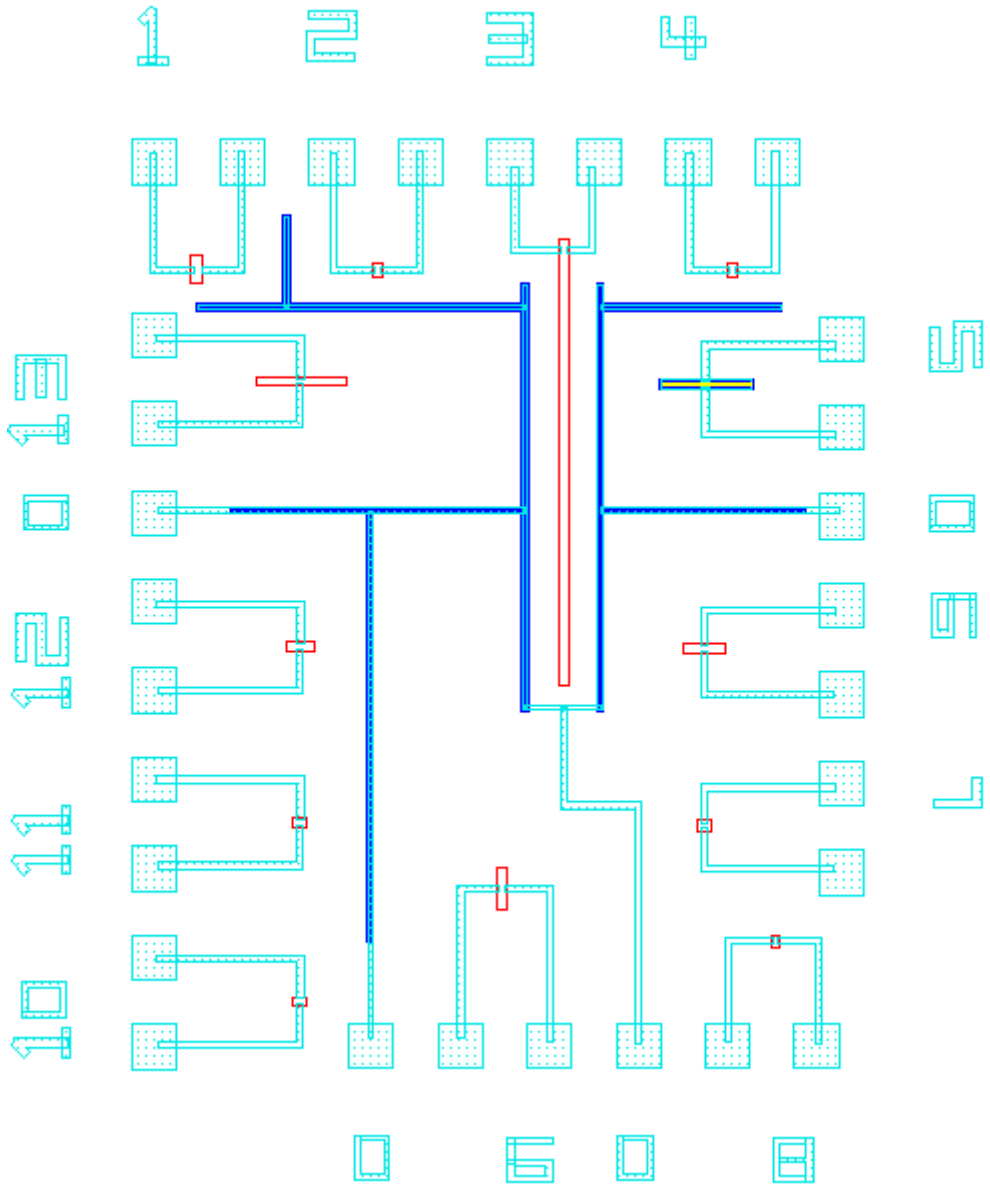


Figure 2.10 The corresponding mask layout view. There are six masks in this work, and all details are list in Table 2.1.

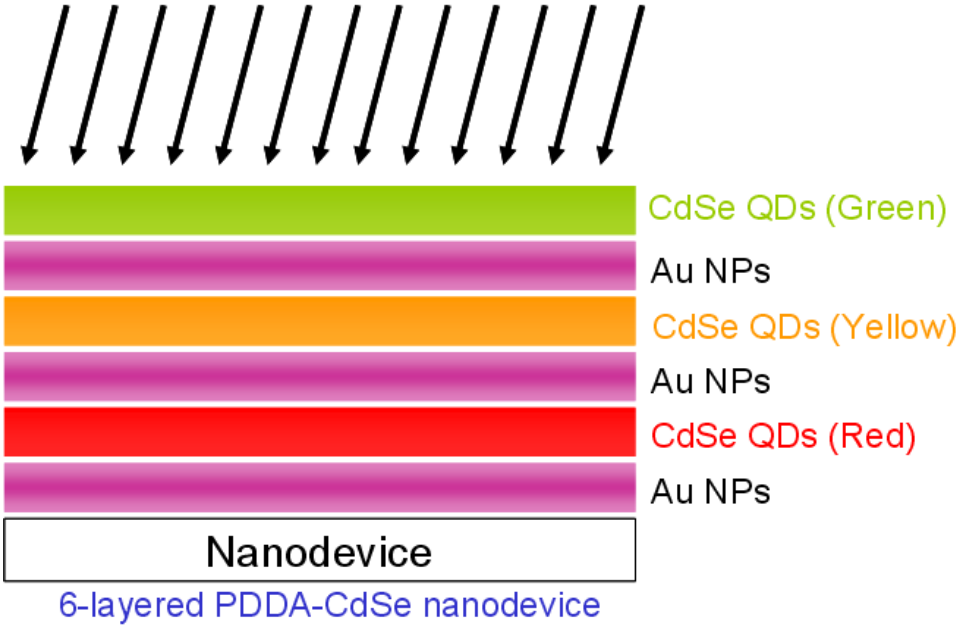
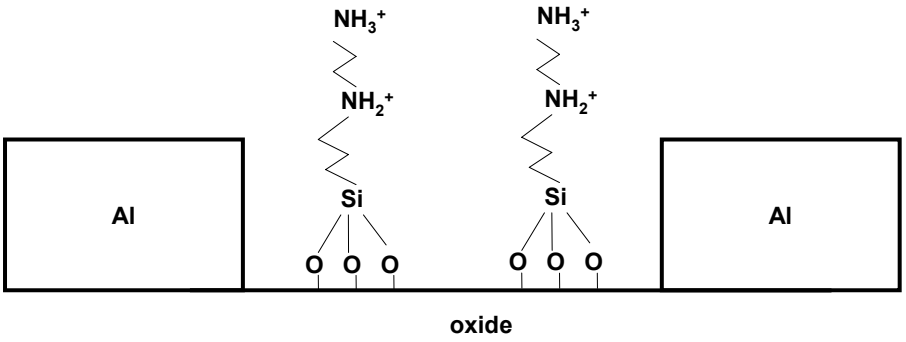
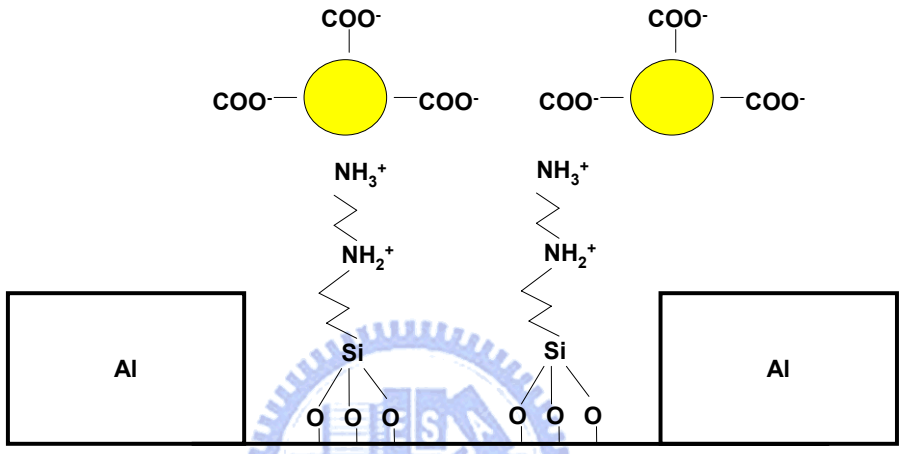


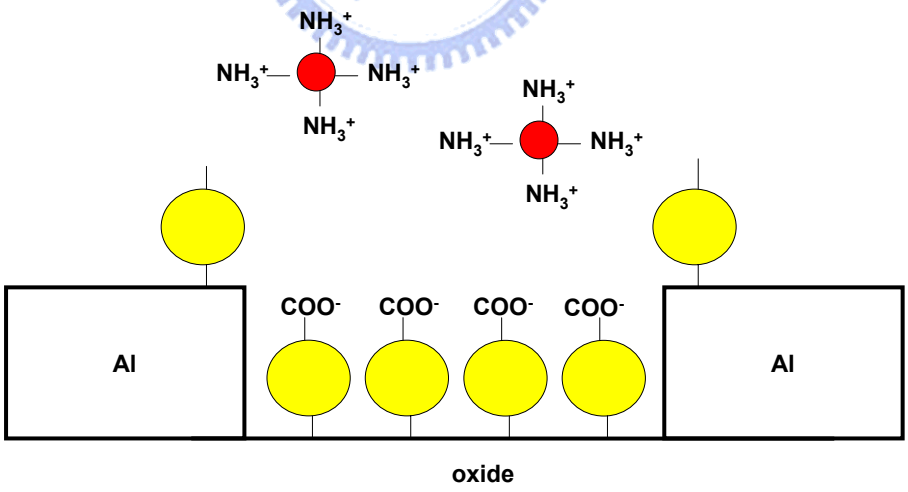
Figure 2.11 The cross-section view of modified nanostructure with Au NPs and three different-sized PDDA-capped CdSe/ZnS quantum dots. The bottom layer is composed of larger-sized QDs (smaller band gap, absorb smaller wavelength), and the top layer is composed of smaller-sized QDs (larger band gap, absorb longer wavelength). This is because light with longer wavelengths (ref region) is transmitted through initial layer.


NH3+
NH2+
Si
O O O
Al
Al
oxide

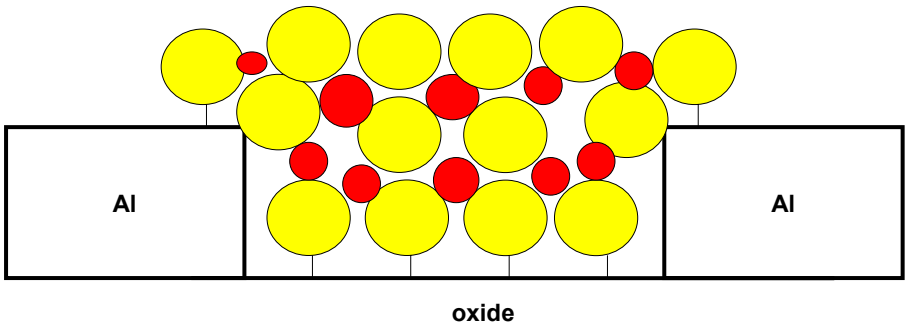
(a)


COO-
COO-
COO-
NH3+
NH2+
Si
O O O
Al
Al
oxide

(b)


NH3+
Al
Al
COO-
oxide

(c)



(d)

Figure 2.14 The fabrication process of the nanostructure by coulombic force system after lift-off process. (a) The modification of TMSPED on the silicon oxide surface and the protonation of amino ($-NH3^{+}$) groups, (b) The assembly of ~ 15 nm diameter Au NPs on silicon oxide substrate by ionic interaction, (d) The assembly of ~ 5 nm diameter AET-CdSe/ZnS NPs on the silicon oxide substrate by ionic interaction, and (e) The formation of the photo-sensing nanodevice structures after repeated assembly process. (Not to scale)

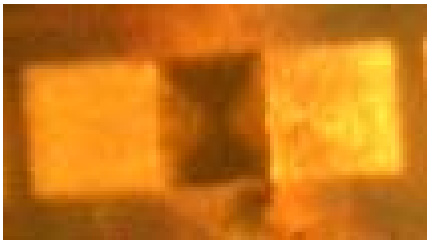
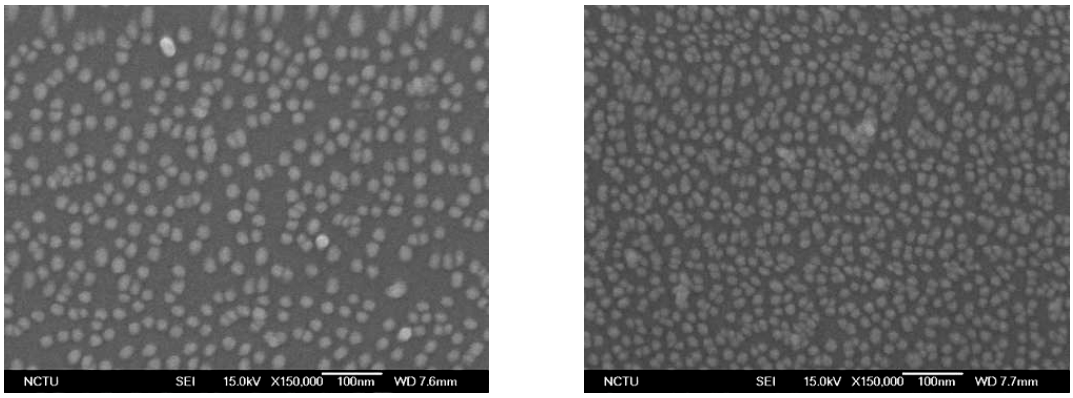
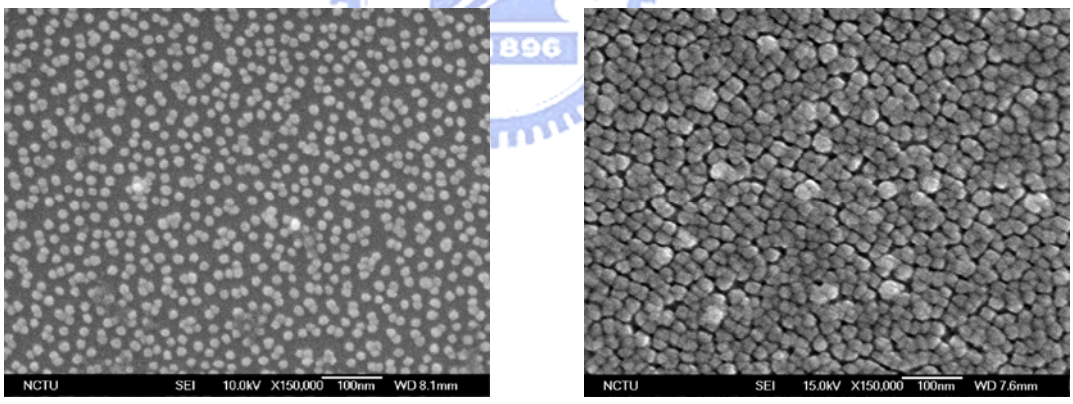


Figure 2.15 SEM photograph of nanodevice with lift-off process, the black part is the place where Au NPs and CdSe QDs deposit.



(a) (b)

Figure 2.16 The temperature effect on the nanostructure (SEM photograph). (a) the nanostructure constructed at room temperature (b) the nanostructure constructed at 4°C environment.[11]



(a) (b)

Figure 2.17 The reaction time effect on the nanostructure (SEM photograph). (a) the nanostructure with 4-hour-reaction time per layer (b) the nanostructure with 12-hour-reactime per layer

CHAPTER 3

EXPERIMENTAL RESULTS AND DISCUSSIONS

3.1 The Environment Setup for Measurement

At first, Figure 3.1(a) shows the photographic of the electrodes of the nanodevice fabricated in NDL. And Figure 3.2(b) demonstrates the enlarged view of one nanodevice. After fabrication, the nanodevice were observed and evaluated by using scanning electron microscopy (SEM) photographs.The SEM was performed with JSM-6500F high-resolution scanning microscope. In this work, daylight lamp and laser diode are used as illumination light source. The environment setup for I-V characteristics measurement is shown in Figure 3.2. The laser diode driver is PicoQuant POL 800D and the 375 nm laser diodes are PicoQuant LDH-P-C375. And I-V characteristic measurement instrument is HP 4156.

On the other hand, the specific optical characteristics of the nanostructure are confirmed by UV-visible and Photoluminescence (PL) spectra. The UV-visible absorption spectrum analysis is performed with Hitachi-U-3010 Spectrophotometer. The detecting wavelength is in the range from 190 nm to 1000 nm. The typical experimental setup is shown in Figure 3.3. A beam of light from a visible and/or UV light source (red colored) is separated into its component wavelengths by a prism or diffraction grating. Each monochromatic (single wavelength) beam in turn is split into two equal intensity beams by a half-mirrored device. One beam, the sample beam (colored magenta), passes through a small transparent container (cuvette) containing a solution of the compound being studied in a transparent solvent. The other beam, the reference (colored blue), passes through an identical cuvette containing only the solvent. The intensities of these light beams are then measured by electronic detectors and

compared. The intensity of the reference beam, which should have suffered little or no light absorption, is defined as I_0. The intensity of the sample beam is defined as I. Over a short period of time, the spectrometer automatically scans all the component wavelengths in the manner described. The ultraviolet (UV) region scanned is normally from 200 to 400 nm, and the visible portion is from 400 to 800 nm. If the sample compound does not absorb light of a given wavelength, $I = I_0$. However, if the sample compound absorbs light, I is less than I_0. And this difference may be plotted on a graph versus wavelength. Absorption may be presented as transmittance ($T = I/I_0$) or absorbance ($A = \log I_0/I$). If no absorption has occurred, T = 1.0 and A = 0. Most spectrometers display absorbance on the vertical axis, and the commonly observed range is from 0 (100% transmittance) to 2 (1% transmittance). The PL spectrometer analysis is performed with Jobin Yvon Instrument S. A. Inc. Spectrometer. The scanning range is from 200 nm to 1000 nm. The typical experimental setup for PL intensity spectrum measurement is shown in Figure 3.3. When light of sufficient energy is incident on a material, photons are absorbed and excite the electrons from ground state. If radiative relaxation occurs, the emitted light is called photoluminescence (PL). This light can be collected and analyzed to yield a wealth of information about the photo-excitation nanostructure. In this experiment, we used laser source with different wavelengths to photo-activate the nanostructures. Subsequently, the emitted light was passing through a filter lens that can filter out the wavelengths < 500 nm, then analyzed by spectrometer and got into a photo-detector. Eventually, the PL signal data are recorded into computer.

3.2 SEM Images And Optical Absorption / Emission Spectra

The SEM images of the surface of SiO_2/Si quartz fragments after repeated self-assembly process are shown in Figure 3.5. And through Figure (a) to (e), Au NPs and PDDA-capped CdSe/ZnS QDs were successfully deposited on the quartz. As we can see in

the images, the nanostructure became more and more compact while increasing the number of layers step by step. Besides, for Au NPs / PDDA-capped CdSe nanostructure, after multi-layered structure was formed, typically more than 3 layers, the gold color shining can be easily observed by naked eye. First, the sample (electrode) was modified by N-[3-(trimethoxysilyl)propyl]-ethylene diamine (TMSPED), which provided positive-charged amino ($-NH_3^+$) groups to attract negative ($-COO^-$) charged Au. Second, the modified PDDA-capped CdSe/ZnS QDs that had positive-charged amino groups on the particle surface were assembled on Au NPs. Theoretically, the assembly process can be repeated for several times to form multi-layered nanostructure of PDDA-capped CdSe/ZnS QDs and Au NPs. And then figure 3.6 shows the lateral SEM photographic of the nanodevice. The surface of the nanostructure is not smooth, since PDDA is capped the surface of CdSe/ZnS QD.

Furthermore, in order to prove that the closely packed nanostructure has superior optical properties, we observed the UV-visible and Photoluminescence (PL) intensity spectra of the different-sized PDDA-capped CdSe/ZnS quantum dots solution. From the absorption spectrum, we can see that the peak of absorbance was about 500nm ~ 600nm, as shown in Figure 3.6. Besides, the nanostructure retains the optical characteristics of CdSe QDs when they are bound to each other, which can be verified by identifying the characteristic absorbance peaks of Au NPs (~520 nm) and CdSe QDs (~580 nm) in the spectrum. However, in some cases, we observed the peaks of Au NPs (~520 nm) and CdSe QDs (~580 nm) are so close that they merge to form a board band in the spectrum for Au / CdSe nanostructure as shown in figure 3.7.

The PL intensity spectra of different-sized PDDA-capped CdSE/ZnS QDs were shown in figure 3.8. When we used 365 nm wavelength for optical excitation, there were three peaks, red, yellow and green respectively, as shown in figure 3.8. It means that different-sized quantum dots have different optical properties, and figure 3.9 shows the

photography of different-sized PDDA-capped CdSe/ZnS QDs. We can utilize these characteristics to design an order assembly multi-layer nanoparticles or quantum dots thin films to realize high-efficiency solar cell. However, during the dip-and-wash procedure, the instable bond between the NPs and QDs will cause the existence of defect. So the probability of defect will be reduced when the number of layers increases.

3.3 Nanodevice Performance Measurement

I-V characteristics of the proposed nanodevices are measured in this section. The measurement environment was introduced in the section 3.1. And the electrode sets we used, 30 μm / 5 μm, 30 μm / 2.5 μm, 30 μm / 1 μm, and 30 μm / 0.5 μm (width / length). After the fabrication process described in Section 2.4, the I-V measurement was performed by applying voltage biases to the electrodes and measuring the current flowing through the nanodevice while in dark or under 0.16mW / cm^2 daylight lamp illumination. The result of the nanodevice is shown as Figure 3.10 and 3.11. It is a resistive device in dark. After illumination, the photocurrent is generated. It is also linear but a y-axis direction shift. And then the shift quantity is the photocurrent.

According to the experimental results, the photocurrent was increased as the length of the nanodevice decreased. Therefore, the photocurrent volume density (PVD) was also increased as the length decreased. Another important specification of the nanodevice is the open-circuit voltage, and it increased as the length of the nanodevice decrease. And the most important specification is the solar cell efficiency because it remarks the performance of the nanodevice. All experimental and measurement results are list in Table 3.1. Figure 3.12 (a) (b) (c) (d) and (e) show the relation between the photocurrent, open-circuit voltage, PVD, power volume density, efficiency and length of the proposed nanodevice. And above figures demonstrate the error bar of the experimental results. As Figure 3.13 shown, after

24 days the performance of the nanodevice decayed. This phenomenon may result from destruction of nanostructure. Because these samples were not stored in a dry environment, the humidity or oxidation would decrease the reliability. However, after 26 days, the decay tended to saturate.

In this work, under the 0.16 mW/cm^3 illumination, the best solar cell efficiency is 1.6% (6-layered PDDA-capped CdSe/ZnS nanodevice with 60 μm in width and 0.5 μm in length). The maximum photocurrent is 664.62 pA. Then, the maximum photocurrent volume density (PVD) is 7.385×10^{-19} A/nm^3 and power volume density is 4.256×10^{-22} W/nm^3. Finally, table 3.2 compares the measurement results of this work and previous works [12].

3.4 Nanoparticle Solar Cell Efficiency Estimation and Nanodevice Model Construction

Figure 3.14(a) depicts the traditional p-n junction solar cell, and its I-V curve is shown in Figure 3.14(b). According to this I-V characteristic, an effective circuit model of p-n junction solar cell model is illustrated in Figure 3.14(c), where R_s is a small seris resistor and R_p is a very large parallel resistor. In this work, a resistive load is connected to the solar cell. Therefore, an operation point is obtained as shown in Figure 3.15. And the parameter, fill factor is defined.

$$\text{fill factor} = \frac{V_m \cdot I_m}{V_{oc} \cdot I_{sc}}, \tag{3.1}$$

where V_{oc} is the open circuit voltage of the solar cell. I_{sc} is the short current of the solar cell. V_m and I_m is the voltage and the current when the product of the voltage and current (power) is maximum. Then, the efficiency can be defined as

$$\text{Efficiency} = \frac{V_{oc} \cdot I_{sc}}{P_{in}} \times \text{fill factor}, \tag{3.2}$$

where P_{in} is the power of the incident light source. Now, we could define the formula of I-V curve and estimate its maximum power.

$$I = \frac{I_{sc}}{V_{oc}} \cdot V + I_{sc} \qquad \therefore \text{Power} = V \times I = V\left(\frac{I_{sc}}{V_{oc}} \cdot V + I_{sc}\right)$$

$$\text{Let } \frac{\partial \text{Power}}{\partial V} = \frac{2I_{sc}}{V_{oc}} \cdot V + I_{sc} = 0$$

$$\Rightarrow V = {V_{oc}}/{2}\,,\ I = {I_{sc}}/{2}\,, \text{ there is a maximum power of solar cell}$$

$$\text{fill factor}_{(\max)} = \frac{V_m \cdot I_m}{V_{oc} \cdot I_{sc}} = \frac{{V_{oc}}/{2} \cdot {I_{sc}}/{2}}{V_{oc} \cdot I_{sc}} = \frac{1}{4} \tag{3.3}$$

Based on the conventional p-n junction equivalent circuit model, the proposed Au NPs/ PDDA-capped CdSe/ZnS QDs nanodevice model could be constructed. An Au NP and a PDDA-capped CdSe/ZnS QD could be considered as a micro p-n junction solar cell or nano-schottky diode. As shown in Figure 3.16(a), there is a unit cell of the nanodevice between Au NPs and PDDA-capped CdSe/ZnS QD. Figure 3.17 depicts the 1-demensionan nanodevice model. It is a symmetrical structure. And R_{s1} and R_{s2} are small series resistors, R_{p1} and R_{p2} are very large parallel resistors. I_1 and I_2 are the photocurrent after illumination.

For HSPICE simulation, the metal-insulator-semiconductor diode model is employed. And then 2-dimension and 3-dimension nanodevice models could also be constructed in similar way. Figure 3.18 and 3.19 illustrate the 2-dimension and 3-dimension nanodevice equivalent circuit model respectively.

It is worth mentioning that 3-dimension nanodevice model is more complicated than 1-D and 2-D model. Figure 3.19 depicts the ideal 3-dimension nanostructure. The unit cells connect two of the 2-D nanodevice model to form a 3-D nanodevice model. The simulation parameters illustrate in Figure 3.20. First, for HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed. X-dimension unit cell : Rs=15kΩ, Rp=7MΩ, I=2.1nA; Y-dimension unit cell : Rs=0.918MΩ, Rp=289MΩ, I=2.1nA,

Z-dimension unit cell: Rs=3060Ω, Rp=25M, I=2.1nA. A 30 μm / 0.1 μm (width / length) 6-layered PDDA-capped CdSe/ZnS nanodevice is utilized as a unit cell. And then the length effect is discussed and simulated. The photocurrent decreases as the length increase (fixed width = 30 μm, and fixed number of layer = 6) as shown in Figure 3.21(a). The open-circuit voltage also decreases as the length increase as shown in Figure 3.21(b). Hence, PVD and power volume density both decrease as the length increase as shown in Figure 3.21(c) and (d) respectively. And the efficiency is shown in Figure 3.21(e).

In summary, decreasing the length will benefit the performance of the proposed nanodevice. On the basis of the ideal inference, the linear approximation is applied to optimize the dimension of the proposed nanodevice structure. However, the thickness of the nanostructure is not uniform. If the nanoparticles close together, the thickness might less then 60 nm; otherwise, the thickness might be more then 60 nm. Hence, we assume the thickness of the nanostructure is from 50 to 80 nm. And Figure 3.22 shows the efficiency simulation results as the length of the proposed nanodevice shrinks to 100, 50, 40, 30 and 20 nm. As a result, the 36.87 % efficiency solar cell can be realized when the nanodevice is 30 μm in width and 40 nm in length. Moreover, when the length is scaled down to 30 and 20 nm, the solar cell efficiency is up to 51.17 % and 80.18% respectively. Table 3.3 lists the simulation results with linear estimation approximately.

Table 3.1 The experimental and measurement results of the proposed 6-layered PDDA-capped CdSe/ZnS nanodevices. (PVD: photocurrent volume density, Power VD: power volume density)

W/L (mm/mm)	**30/5**	**30/2.5**	**30/1**	**30/0.5**
Vbias	-100mV~100mV			
Isc (pA)	178.10	382.10	406.66	664.62
Voc (mA)	0.34	0.52	0.77	2.31
Isc*Voc (pW)	0.061	0.199	0.313	1.535
Req (dark)	2.79MW	2.43MW	3.30MW	7.81MW
Req (light)	1.93MW	1.36MW	1.88MW	3.45MW
PVD (A/ nm^3)	1.979×10-22	8.491×10-20	2.259×10-19	7.385×10-19
Power VD (W/nm^3)	1.702×10-24	1.111×10-23	4.349×10-23	4.256×10-22
Efficiency (%)	0.007%	0.043%	0.163%	1.600%

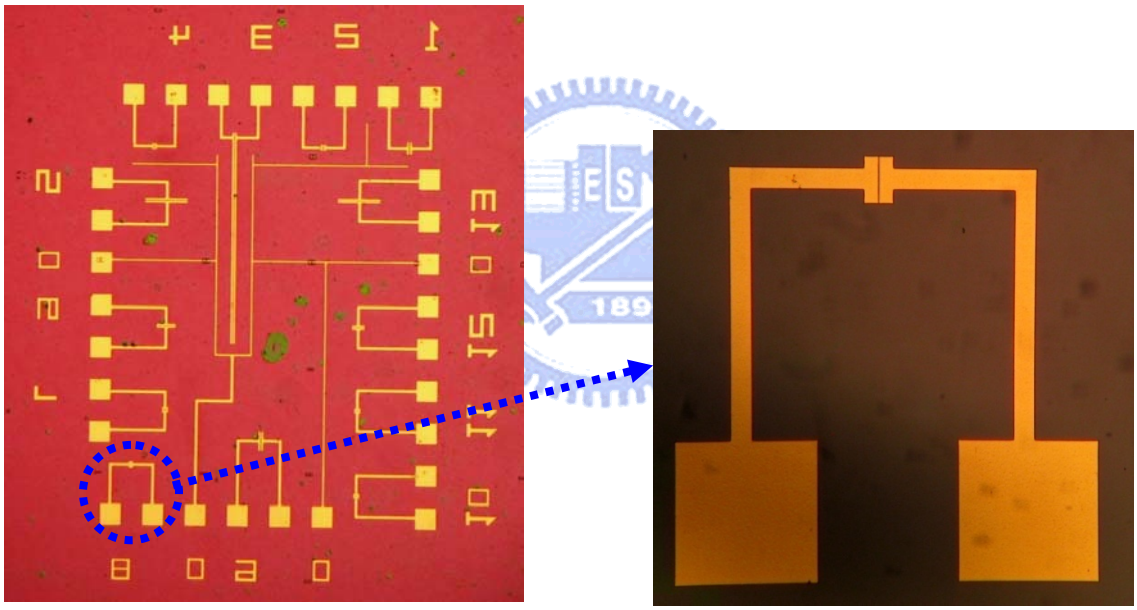
Table 3.2 Performance comparison table

	Previous work [19]*	**Previous work [11]****	**This work**	
Light Source	2.5 mW/cm^2 375nm-Laser	0.16 mW/cm^2 Daylight lamp	0.16 mW/cm^2 Daylight lamp	
Au/QDs Layer	8-layer Au/AET-capped QDs	24-layered Au/PDDA-capped QDs	Different-sized 6-layered Au/PDDA-capped QDs	
W/L (mm/mm)	30/15	30/5	30/5	30/0.5
Isc (pA)	93 nA	502.1 pA	178.10 pA	664.62 pA
Voc (mA)	0.64	14.7	0.34	2.31
Isc*Voc (pW)	59.52	7.381	0.061	1.535
PVD (A/nm3)	5.452×10^{-22}	2.092×10^{-23}	1.979×10^{-22}	7.385×10^{-19}
Power VD (W/nm3)	8.722×10^{-26}	9.611×10^{-26}	1.702×10^{-24}	4.256×10^{-22}
Efficiency (%)	0.0262×10^{-3}%	0.72% (3.24×10^{-3}%)***	0.007%	1.600%

*** Without lift-off process.**
**** Lift-off area was not exactly the same as the illuminated area.**
***** Calibrated efficiency.**

Table 3.3 The simulation results with linear estimation of the proposed 6-layered PDDA-capped CdSe/ZnS nanodevices.

Length (nm)	Estimated Efficiency (%)	
	Min.	Max.
100	10.90	12.19
50	25.56	28.40
40	33.45	36.87
30	46.94	51.17
20	74.60	80.18



(a) (b)

Figure 3.1 (a) Photographic of the electrodes of the proposed nanodevices. Pad 7: 30 μm / 5 μm, Pad 8: 30 μm / 0.5 μm, Pad 10: 30 μm / 1 μm, Pad 11: 30 μm / 2.5 μm (width / length). (b) Enlarged view. The nanoparticles or quantum dots deposit on the gap of two electrodes.

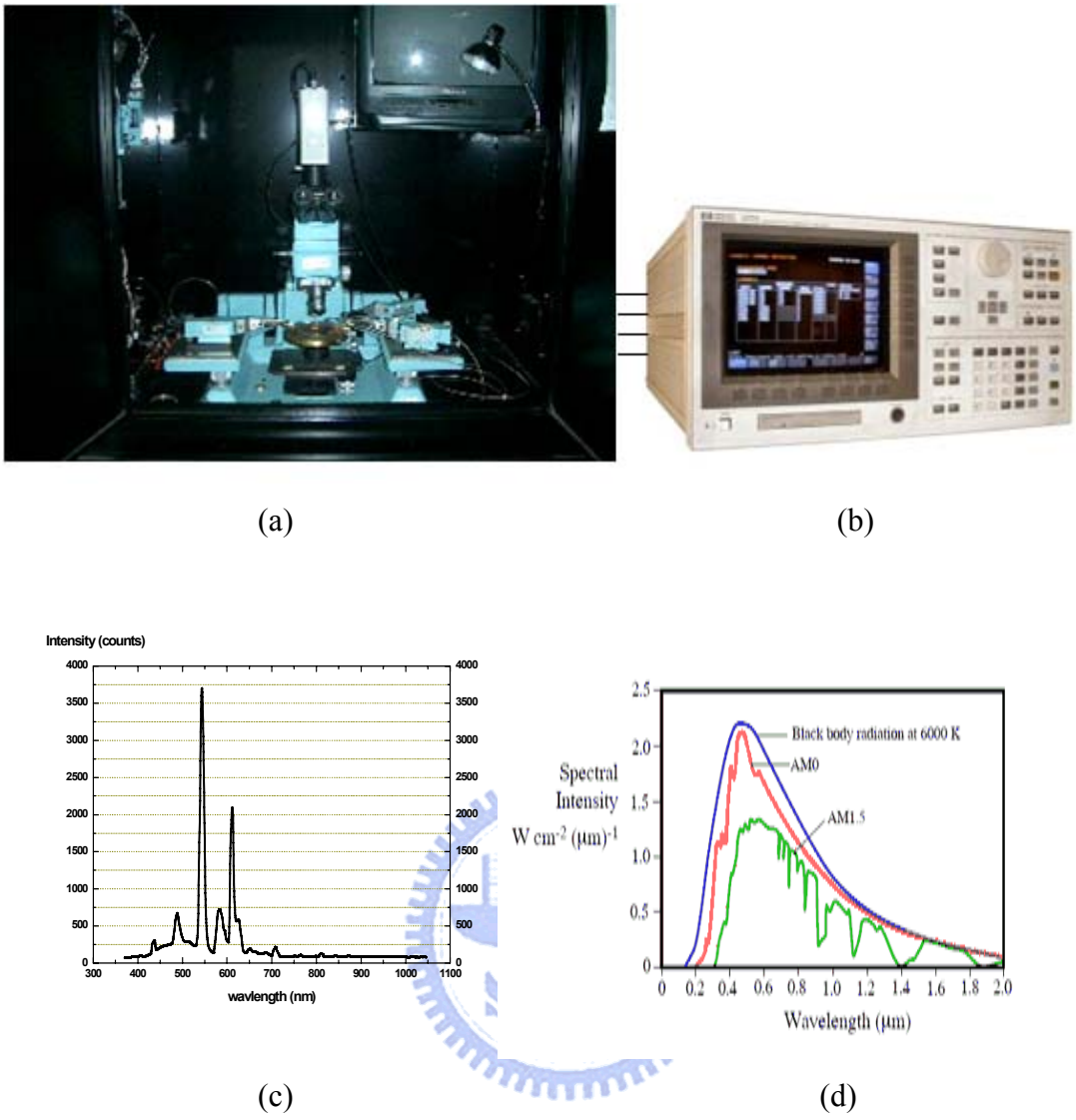


Figure 3.2 The environment setup for I-V characteristics measurement, (a) probe station (b) HP4156 (c) the spectrum of the daylight lamp (d) Solar Spectrum.

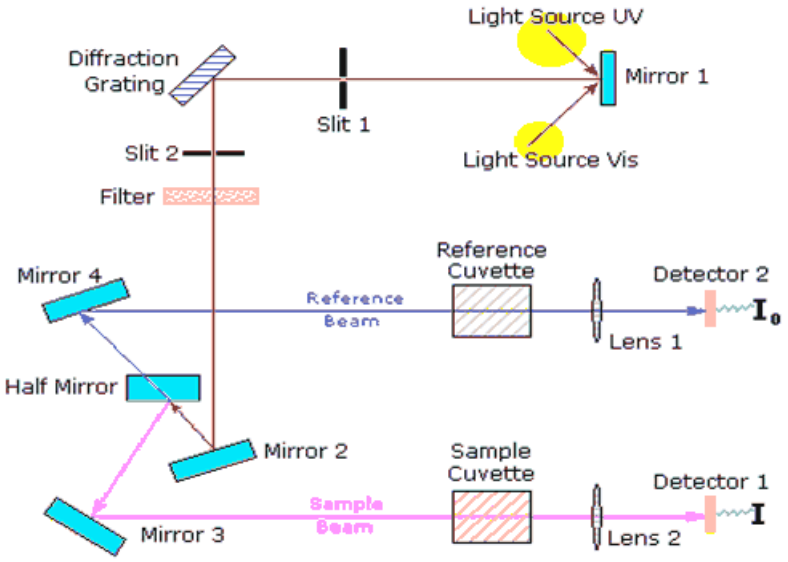


Figure 3.3 The environment setup for UV-visible absorbance spectrum measurement.

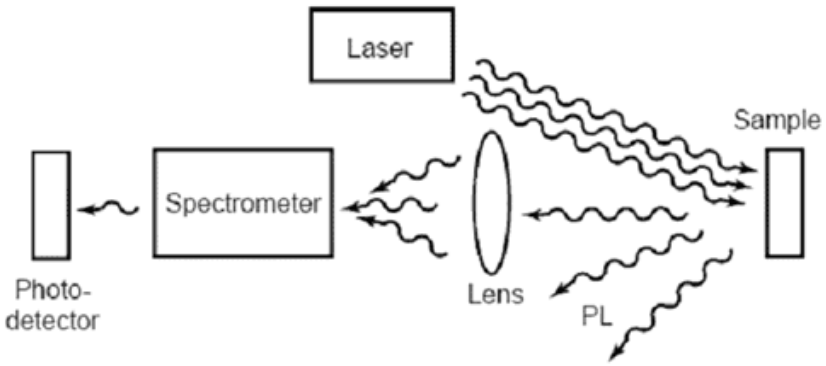


Figure 3.4 The environment setup for PL intensity spectrum measurement.

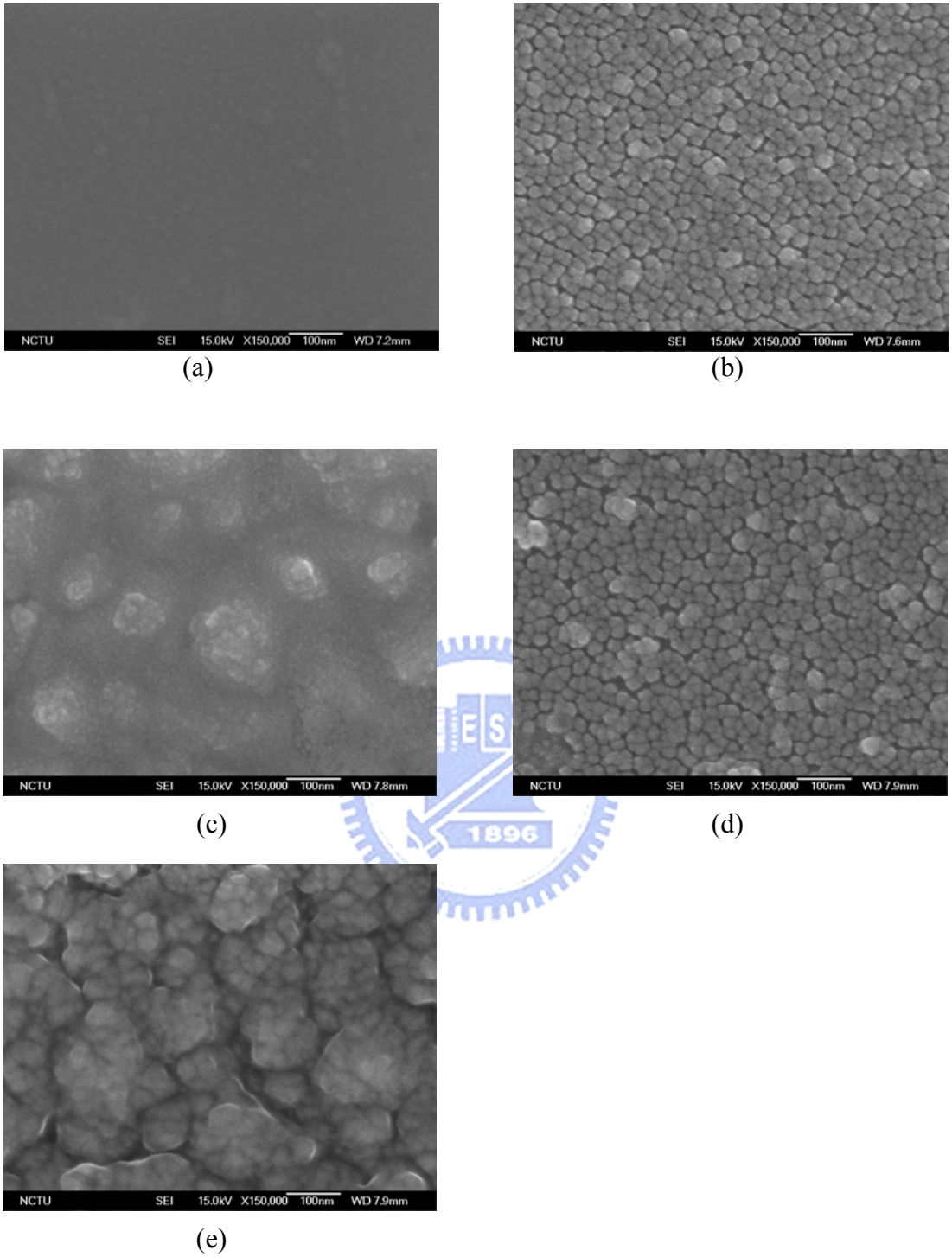


Figure 3.5 SEM images of the surface of SiO2 quartz fragments after repeated self-assembly process. (a) SiO2/quartz only, (b) Au + SiO2/quartz, (c) PDDA-capped CdSe + Au + SiO2/quartz, (d) Au + PDDA-capped CdSe + Au + SiO2/quartz, (e) PDDA-capped CdSe + Au + PDDA-capped CdSe + Au + SiO2/quartz

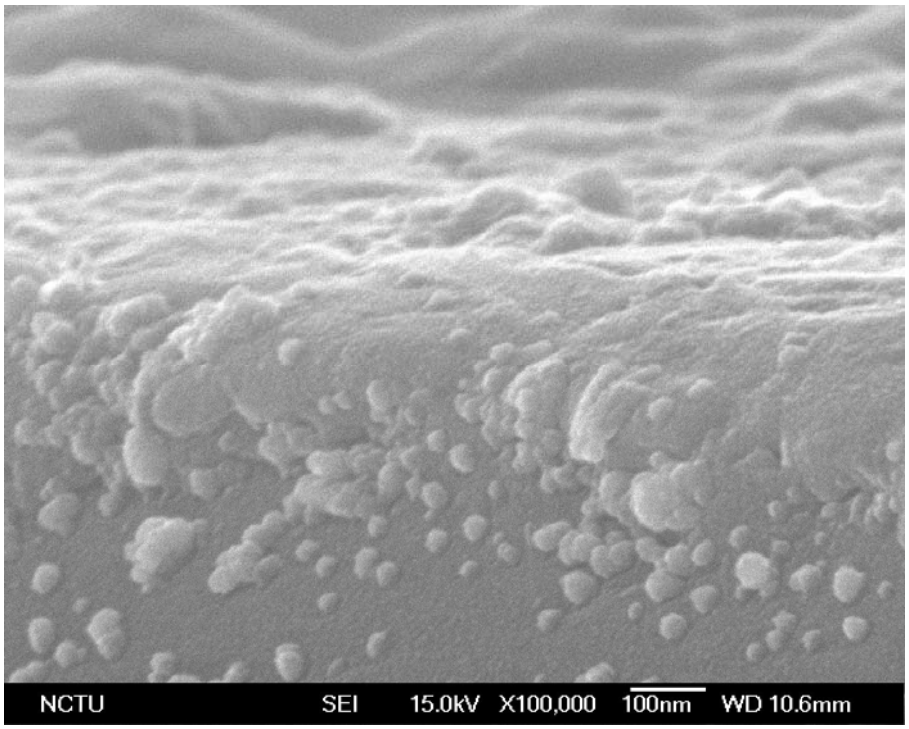


Figure 3.6 Lateral SEM images of the surface of wafer fragments after repeated self-assembly process. The surface of the nanostructure is not smooth, since PDDA is capped the surface of CdSe/ZnS QD.

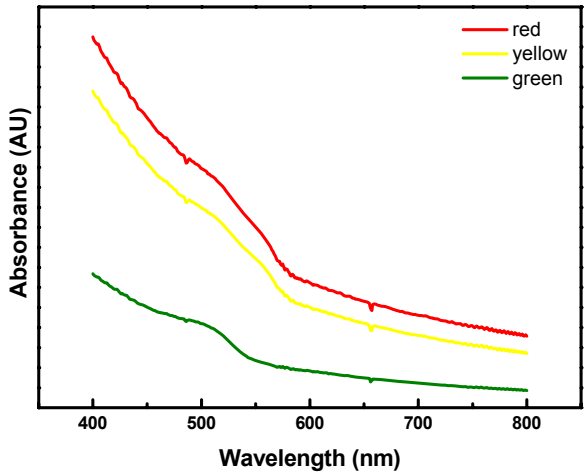


Figure 3.7 UV-VIS absorption spectra of different-sized PDDA-capped CdSE/ZnS QDs. From the absorption spectrum, we can see that the peak of absorbance was about 500nm ~ 600nm.

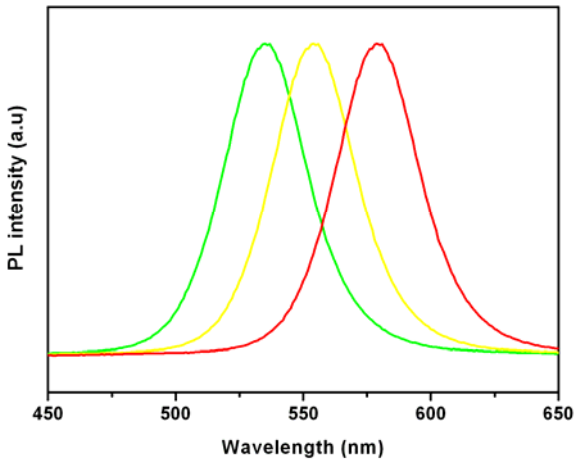


Figure 3.8 PL intensity spectra of different-sized PDDA-capped CdSE/ZnS QDs. Using 365 nm wavelength excitation light, we can observe three peaks.

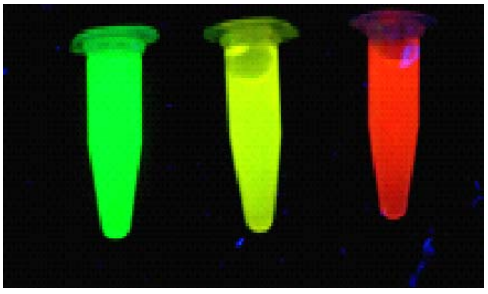


Figure 3.9 Photography of three different-sized PDDA-capped CdSe/ZnS QDs.

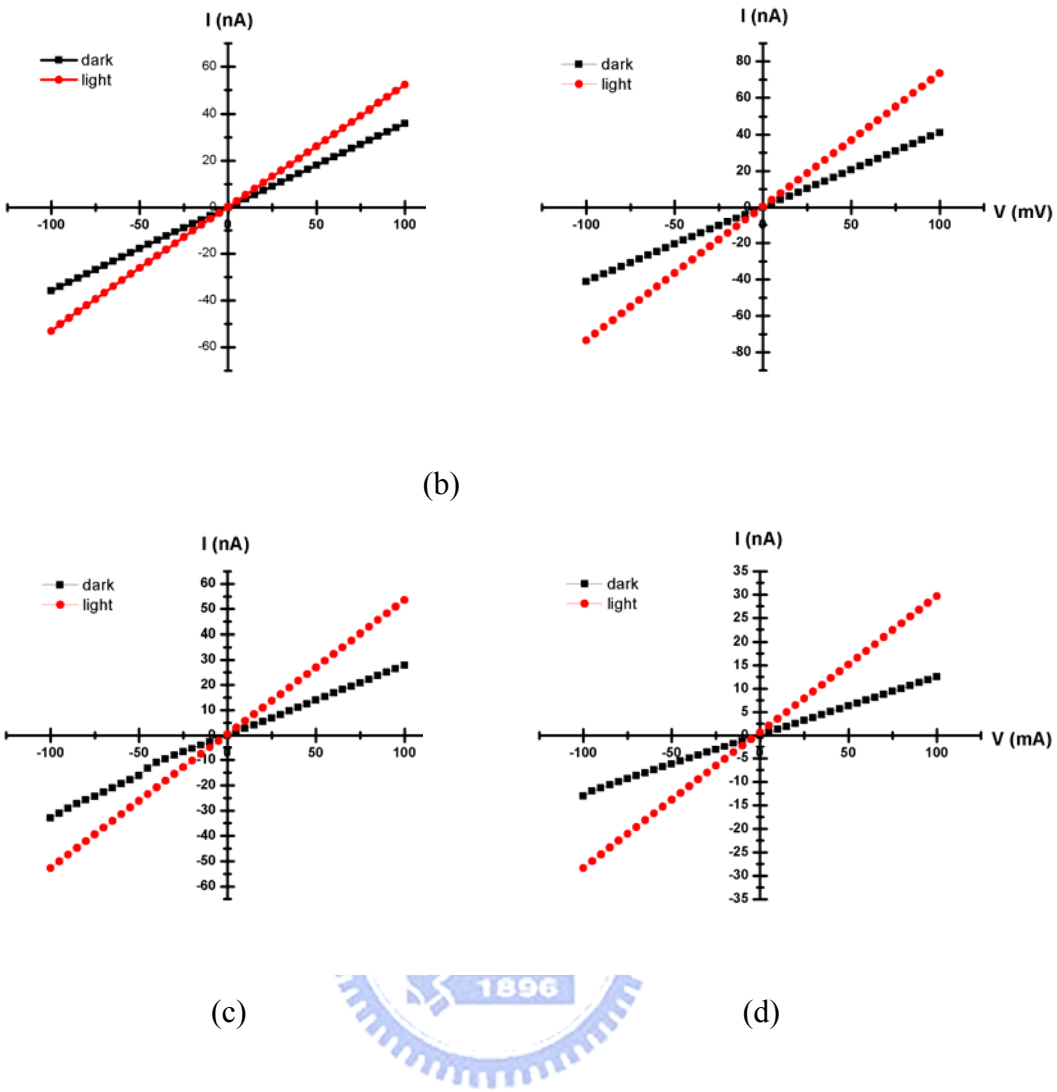


Figure 3.10 The I-V characteristics of the proposed 6-layered PDDA-capped CdSe/ZnS QDs and Au NPs nanodevices. (a) 30 μm / 5 μm, (b) 30 μm / 2.5 μm, (c) 30 μm / 1 μm, (d) 30 μm / 0.5 μm. (width / length)

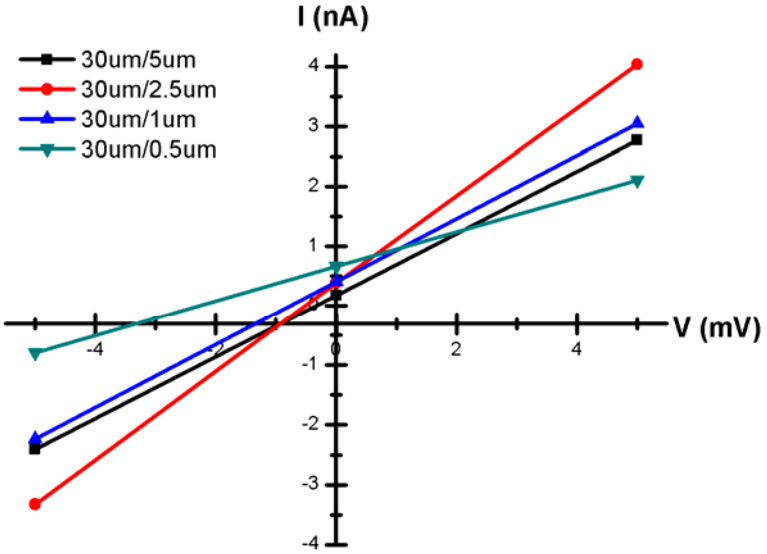
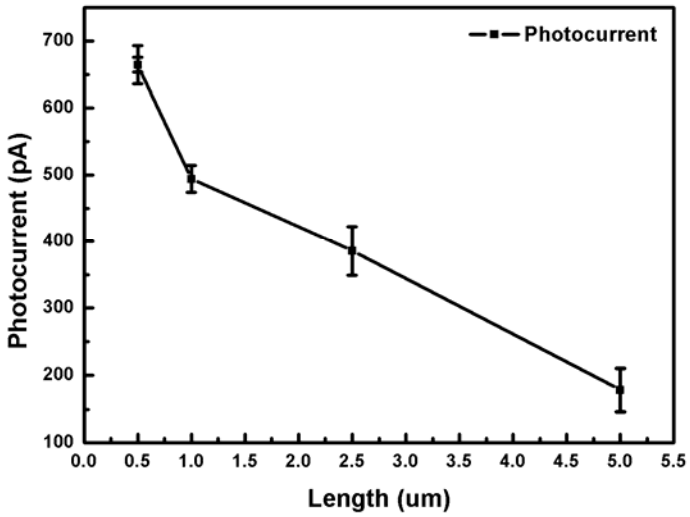
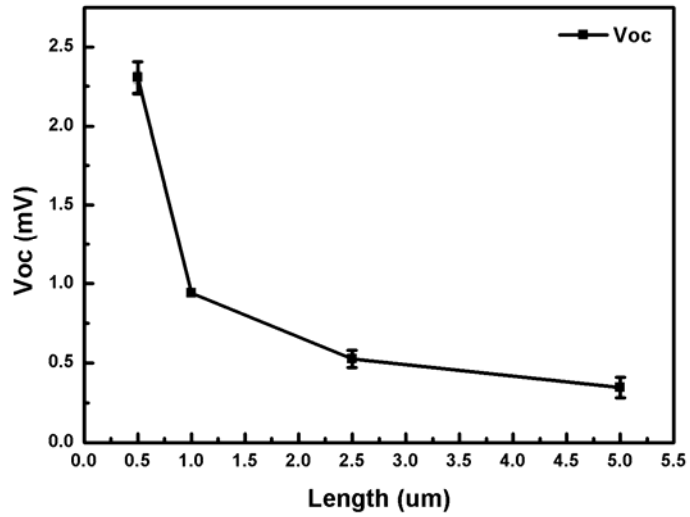


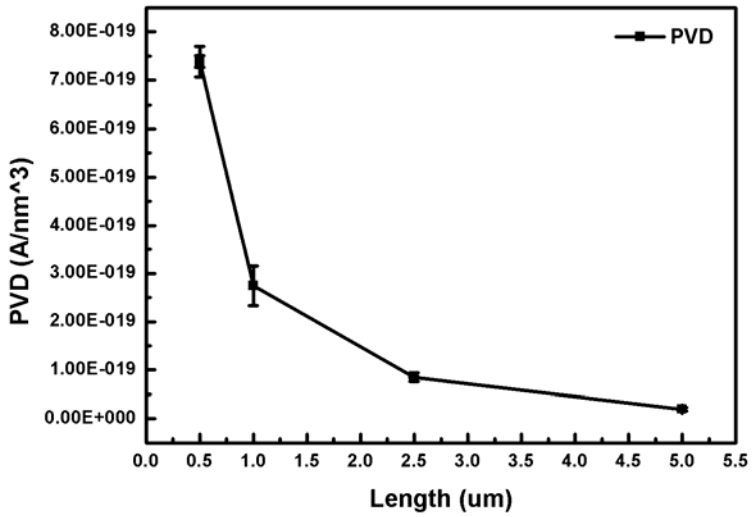
Figure 3.11 The I-V characteristics of the proposed 6-layered PDDA-capped CdSe/ZnS QDs and Au NPs nanodevices with different lengths.


Photocurrent
Photocurrent (pA)
700
600
500
400
300
200
100
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5
Length (um)

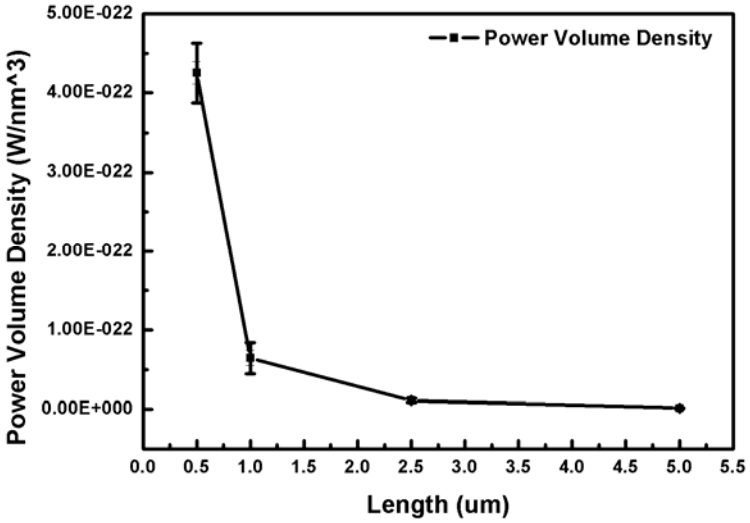
(a)


Voc
Voc (mV)
2.5
2.0
1.5
1.0
0.5
0.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5
Length (um)

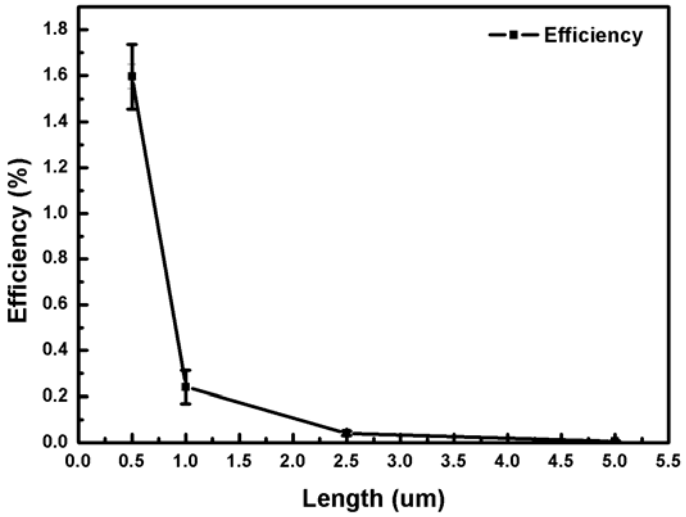
(b)


PVD
PVD (A/nm^3)
8.00E-019
7.00E-019
6.00E-019
5.00E-019
4.00E-019
3.00E-019
2.00E-019
1.00E-019
0.00E+000
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5
Length (um)

(c)

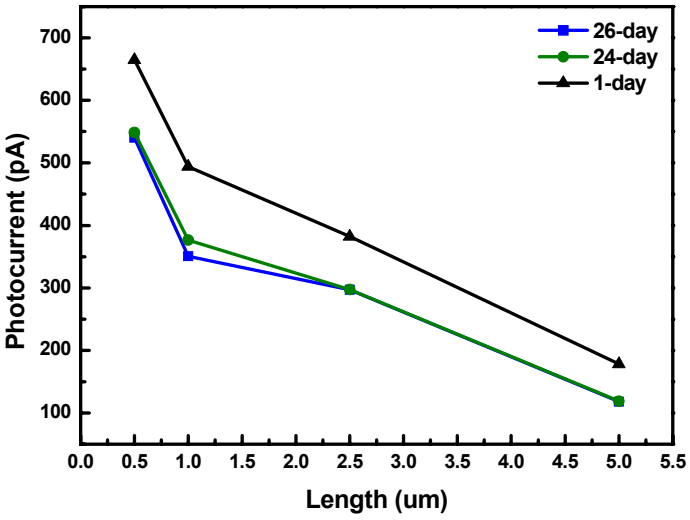


(d)

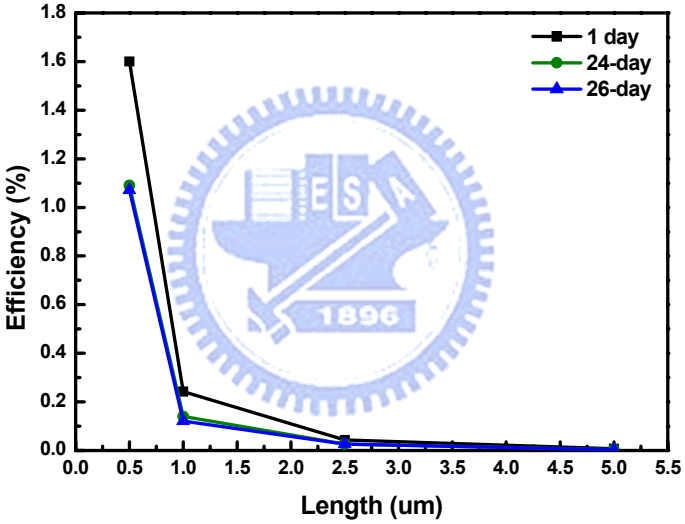


(e)

Figure 3.12 The relation between the main specifications and the length of the proposed 6-layered PDDA-capped CdSe/ZnS QDs / Au NPs nanodevices. (a) photocurrent, (b) open-circuit voltage, (c) PVD, (d) power volume density, and (e) power conversion efficiency.

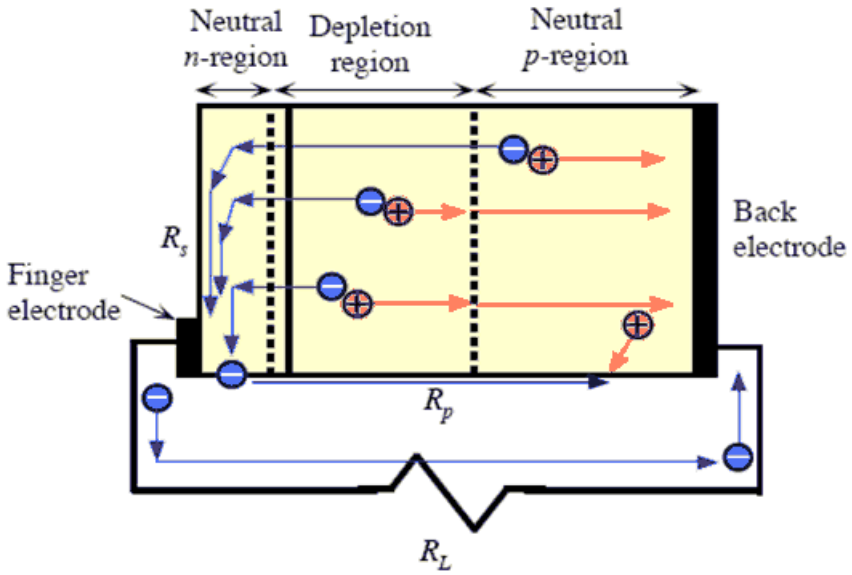


(a)

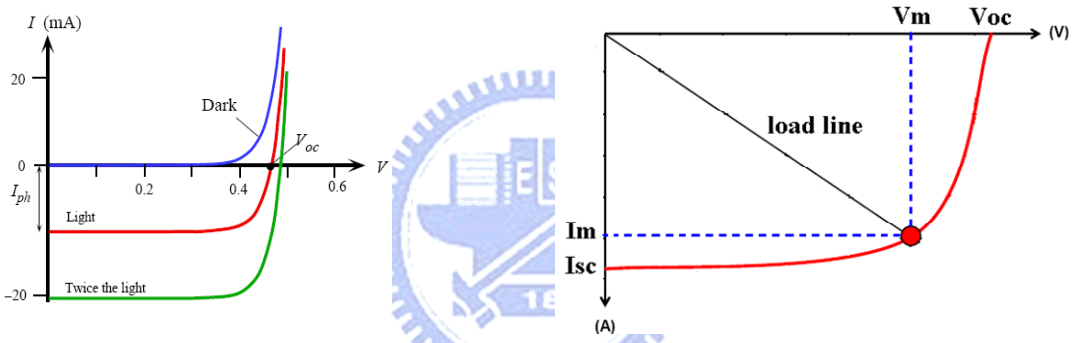


(b)

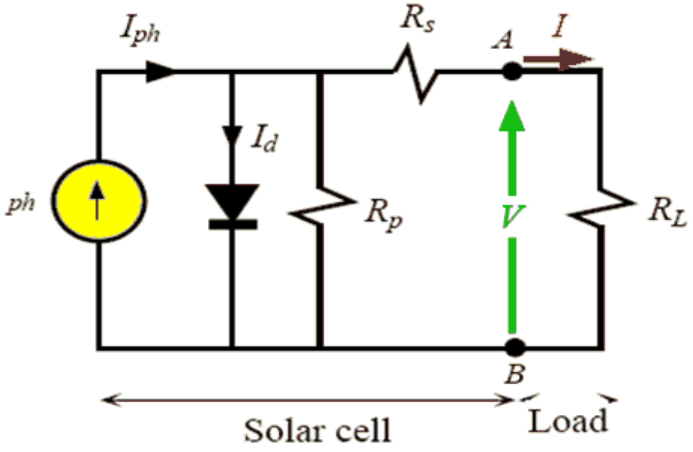
Figure 3.13 After 24 days, the performance of the nanodevice decayed. (a) photocurrent, and (b) power conversion efficiency. And after 26 days, the decay tended to saturate.



(a)



(b)



(c)

Figure 3.14 (a) The p-n junction solar cell structure, (b) the I-V curve of the p-n junction solar cell, (c) the equivalent circuit model of the p-n junction solar cell.

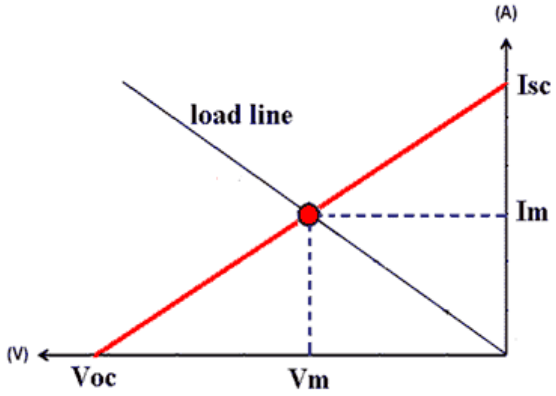


Figure 3.15 I-V characteristic of solar cell (including load line)

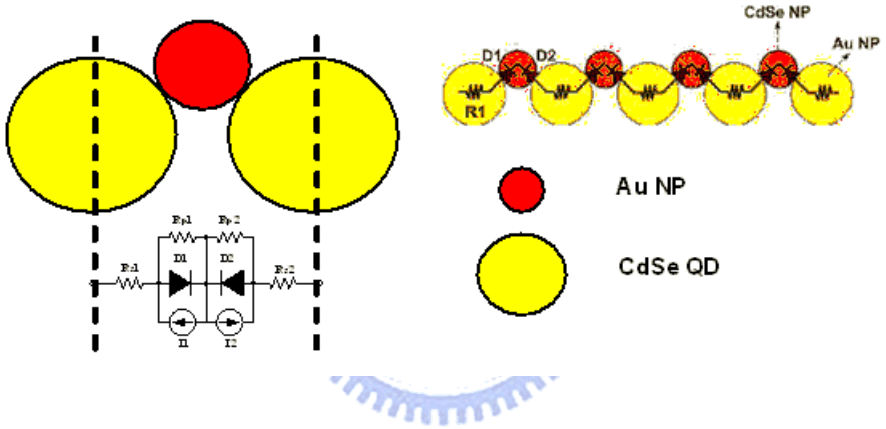


Figure 3.16 (a) A unit cell of the nanodevice model, (b) Symmetrical structure

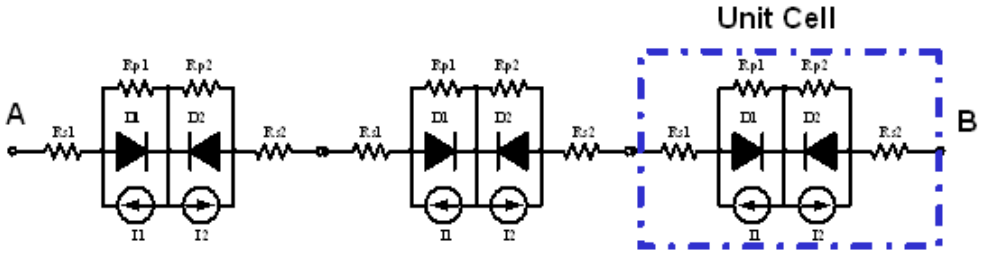
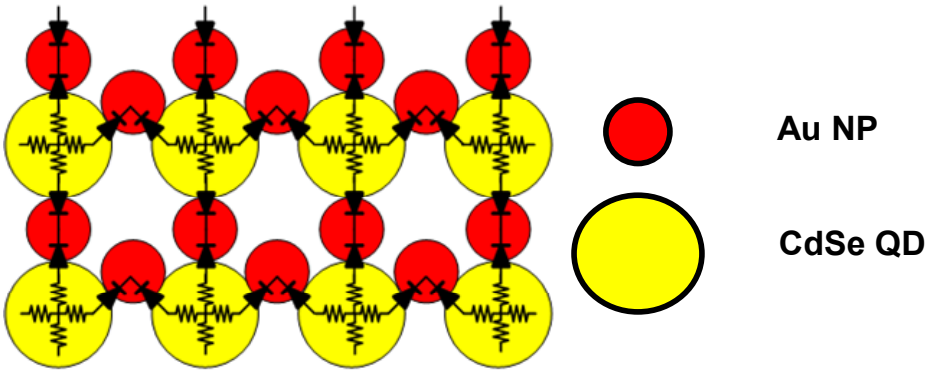
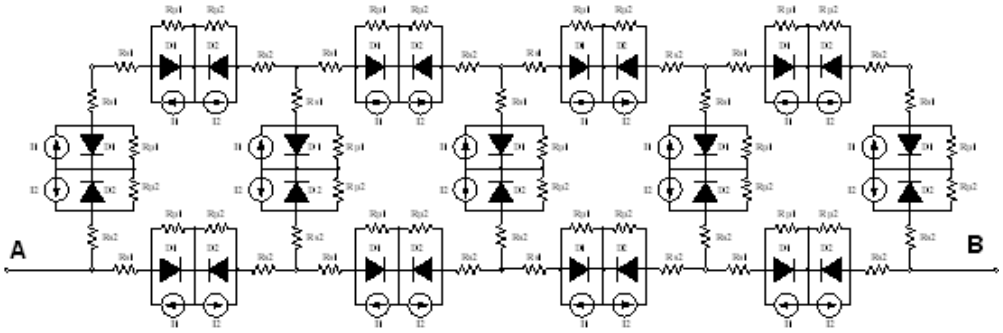


Figure 3.17 1-D nanodevice model, where Rs1 and Rs2 are small series resistors, Rp1 and Rp2 are very large parallel resistors. I1 and I2 are the photocurrent after illumination.



(a)



(b)

Figure 3.18 2-D nanodevice model. (a) 2-D nanostructure, (b) 2-D nanodevice equivalent circuit model.

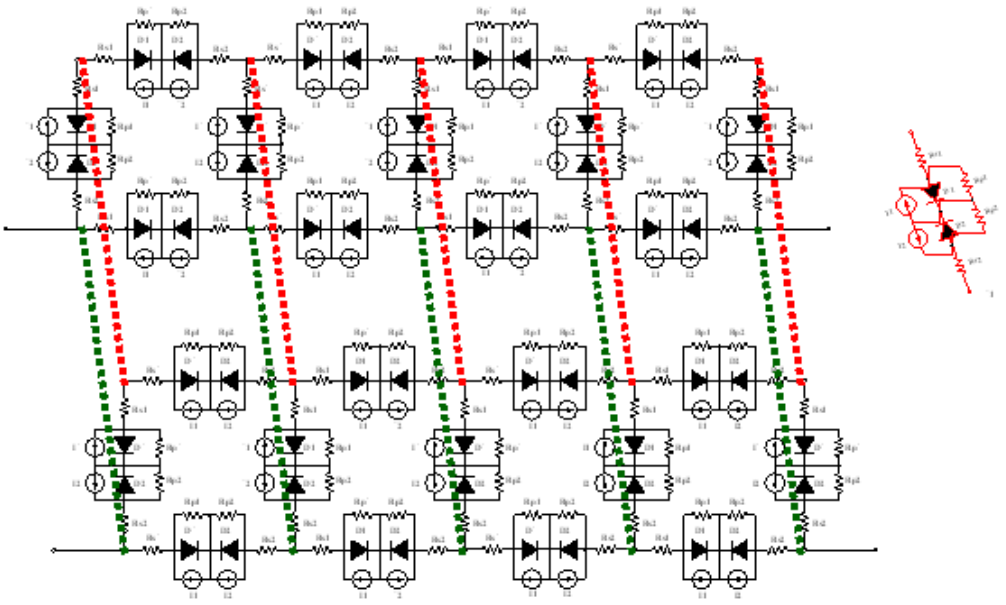


Figure 3.19 3-D nanodevice model. And the dash line parts are substituted for the unit cells.

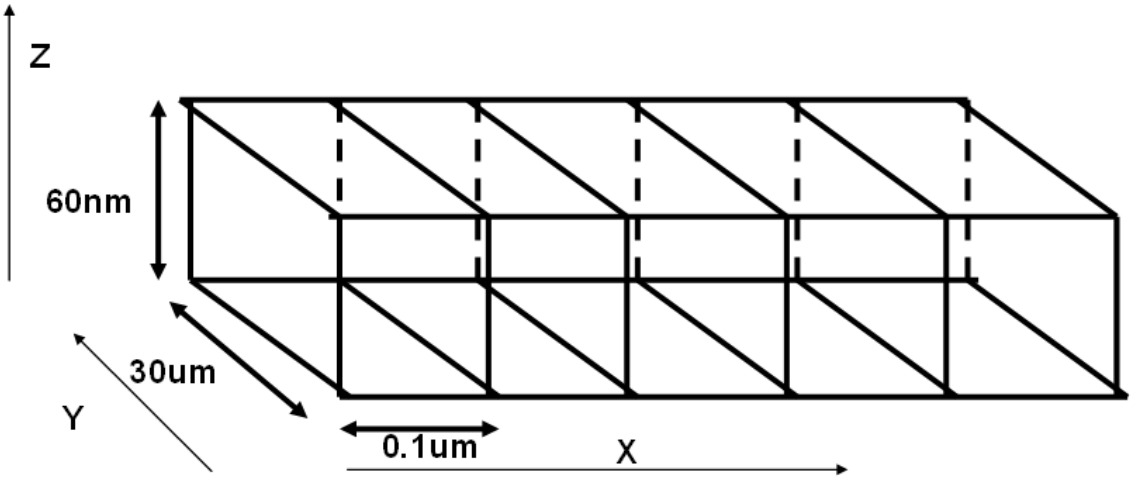
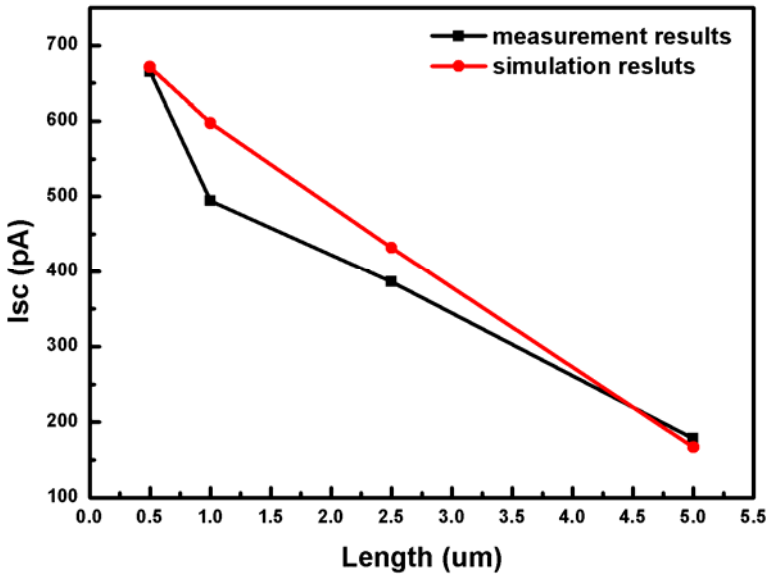


Figure 3.20 The 3-D nanodevice model. The line parts are substituted for the unit cells. For HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed.

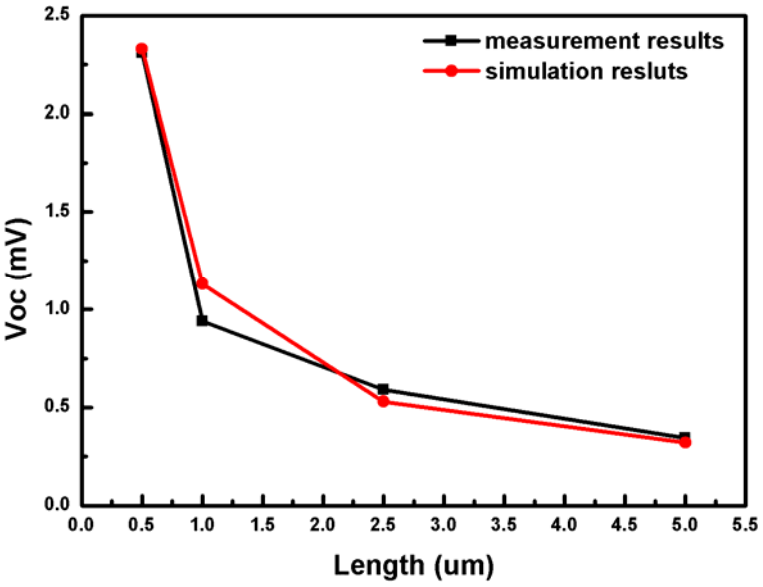
X-dimension unit cell : Rs=15kΩ, Rp=7MΩ, I=2.1nA,

Y-dimension unit cell : Rs=0.918MΩ, Rp=289MΩ, I=2.1nA,

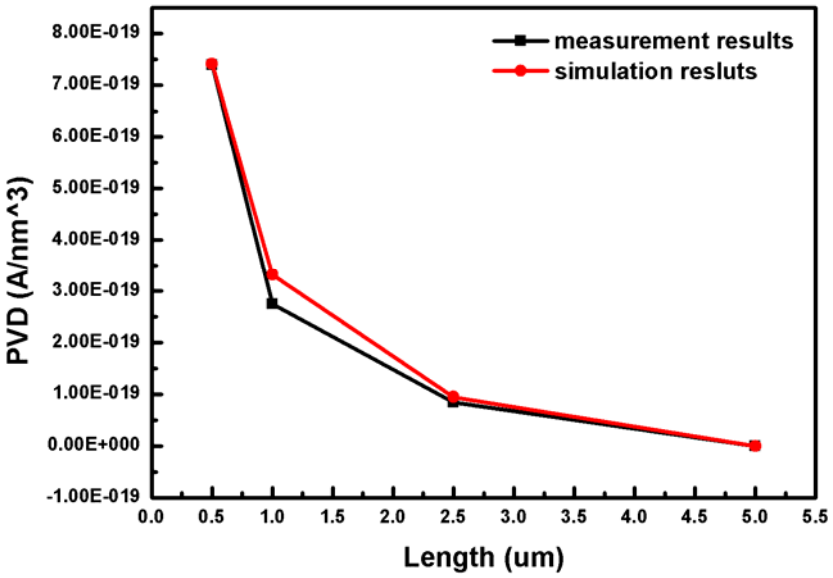
Z-dimension unit cell : Rs=3060Ω, Rp=25M, I=2.1nA.


measurement results
simulation resluts
Isc (pA)
Length (um)
700
600
500
400
300
200
100
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5

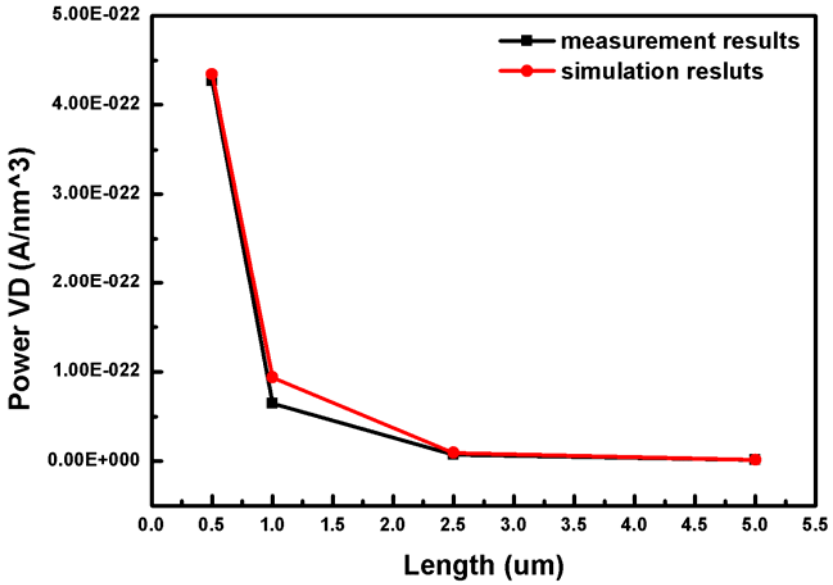
(a)


measurement results
simulation resluts
Voc (mV)
Length (um)
2.5
2.0
1.5
1.0
0.5
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5

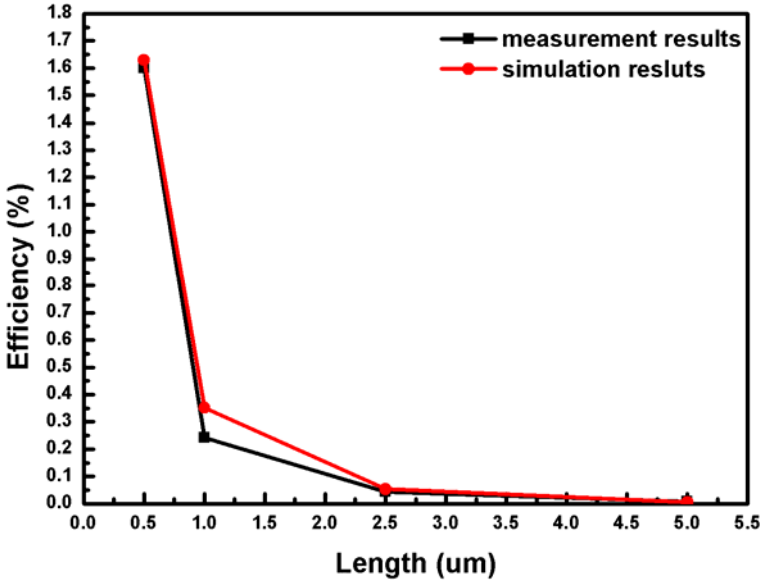
(b)


measurement results
simulation resluts
PVD (A/nm^3)
8.00E-019
7.00E-019
6.00E-019
5.00E-019
4.00E-019
3.00E-019
2.00E-019
1.00E-019
0.00E+000
-1.00E-019
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
Length (um)

(c)


measurement results
simulation resluts
Power VD (A/nm^3)
5.00E-022
4.00E-022
3.00E-022
2.00E-022
1.00E-022
0.00E+000
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
Length (um)

(d)



(e)

Figure 3.21 (Length effect) Comparison of the 3-D nanodevice model simulation results and measurement results of the proposed 6-layered PDDA-capped CdSe/ZnS QDs / Au NPs nanodevices. (a) photocurrent, (b) open-circuit voltage, (c) PVD, (d) power volume density, and (e) solar cell efficiency.

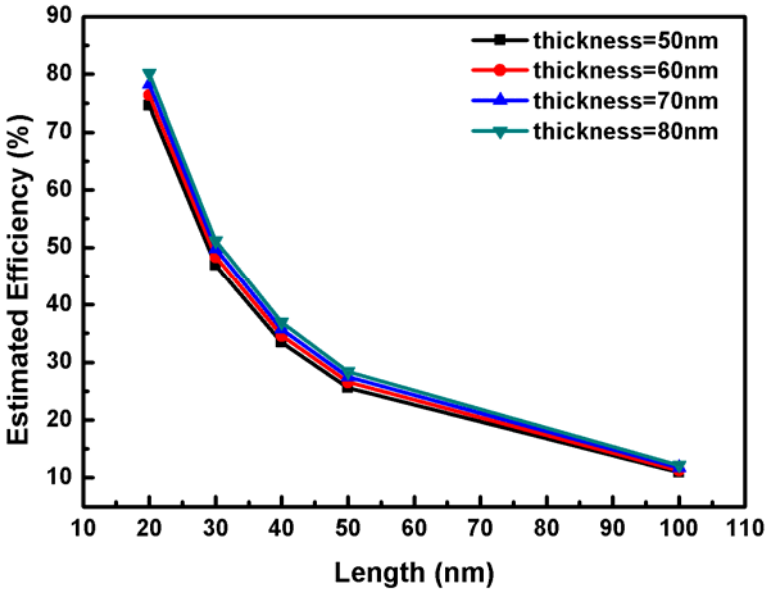


Figure 3.22 On the basis of the ideal inference, the linear approximation is applied to optimize the dimension of the proposed nanodevice structure. The length shrinks to 100, 50, 40, 30, and 20 nm. However, the thickness of the nanostructure is not uniform. If the nanoparticles close together, the thickness might less then 60 nm; otherwise, the thickness might be more then 60 nm. Hence, we assume the thickness of the nanostructure is from 50 to 80 nm.

CHAPTER 4

APPLICATION OF LINEAR REGULATOR ON NANOPARTICLE SOLAR CELL

Solar cells have been promising candidate for next generation alternative energy source. Therefore using solar cell to provide the power of portable devices has been considered as one of the potential architecture in the future. Regulators are an essential part of electrically powered system, which includes the growing family of applications of portable battery operated products. The widespread use of battery-powered devices in today's world has increased the demand for low-voltage, low drop-out linear regulator (LDO) [20].

The basic function of the regulators is to reduce the large voltage variation of battery cell and provide a reliable, constant output voltage to drive small sub-circuits. Absence of these power supplies can prove to be catastrophic in most high frequency and high performance circuit designs. As a result, regulators and other power supply circuits are always in high demand. Generally, linear regulators and switching regulators are widely used in the commercial electronic applications. Linear regulators are purely analog circuits. The operation of the circuits is based on feeding back an amplified error signal to control the output current flow of the power transistor driving the load. So the output can be adjusted to the desired voltage immediately. According to the configuration of the linear regulators, the magnitude of the respective output voltage is less than the input supply voltage. On other hand, switching regulators are essentially mixed-mode circuits which feed back an analog error signal and digitally gate it to provide bursts of current to the output. Furthermore, switching regulators can provide a wide range of output voltage including values that lower or

greater than the input supply voltage depending on the circuit configuration, buck or boost.

In this work, the linear regulator is adopted. There are some reasons why this configuration is chosen. First of all, the power consumption can be very low while in light load condition. This reason makes it appropriate for use in solar cell application. Second, this configuration dose not suffer form the switching noise generated by digital signals or clock. Finally the circuits are implemented without using any inductors, so the footprint area is also very small. And the linear regulator is inherently less complex and costly than the switching regulator.

In this chapter, a low voltage, low quiescent current, low drop-out regulator system is designed to target the low power operation and integrated with the proposed nanoparticle solar cell. The relevant analysis is introduced to design the system. The proposed regulator system was successfully fabricated in TSMC 1P6M 0.18-μm CMOS process.

4.1. System Design Considerations

Proper design of a low drop-out (LDO) regulator involves intricate knowledge of the system and its load. The task of maximizing load regulation, maintaining stability, and minimizing transient output voltage variations prove to be challenging and often conflicting. The system also has to target the low power consumption and integrate with the proposed solar cell device.

4.1.1. Architecture

As the Figure 4.1 shown, the system architecture is utilized in this work. The system is composed of an error amplifier, a pass element, feedback resistor network, bandgap voltage reference, off-chip compensating capacitor and associated electrical series resistor (ESR), and bypass capacitor.

4.1.2. AC Analysis

Because the low drop-out regulator is a feedback system, the stability issue should be concerned. Figure 4.2 illustrates the intrinsic factors that determine the stability of the system. The ESR of the by pass capacitors can typically neglected due to high frequency capacitor; in other words, the ESR value is low. The pass device is modeled as a circuit element exhibiting a transconductance of g_{mp} and an output impendance of $R_{o\text{-}pass}$. The value of R_1 is designed to define the quiescent current flowing through resistors R_1 and R_2, which is typically large to minimize the quiescent current consumption. And the value of R_2 is dependent on the desired value of the output voltage, i.e. the voltage of the output and V_{ref} determines the resistor ratio of R_1 and R_2.

- **Frequency Response**

For the purpose of analysis, the feedback loop can be broken at node "A" in Figure 4.2. The system must be unity gain stable, considering V_{ref} and V_{fb} to be the input and the output voltages respectively. So the open-loop gain can be described as

$$\left|A_V\right| = \frac{V_{fb}}{V_{ref}} = \frac{g_{ma} R_{oa} g_{mp} Z}{\left[1 + R_{oa} C_{par}\right]} \cdot \frac{R_1}{R_1 + R_2} \tag{4.1}$$

where g_{ma} and g_{mp} refer to the transconductance of the error amplifier and the pass element respectively, R_{oa} is the output resistance of the amplifier, C_{par} is refer to the parasitic capacitor introduced by the pass element, and Z is the impedance seen at node V_{out},

$$Z = R_X \,||\, \frac{1 + sR_{esr}C_O}{sC_O} \,||\, \frac{1}{sC_b} = \frac{R_X\left[1 + sR_{esr}C_O\right]}{s^2 R_X R_{esr} C_O C_b + s\left[R_X + R_{esr}\right]C_O + sR_X C_b + 1} \tag{4.2}$$

where C_O and R_{esr} are the capacitance and ESR of the output capacitor, C_b represents the bypass capacitors and R_x is the resistance seen from Vout back into the regulator defined as

$$R_X = R_{o-pass} \,||\, \left(R_1 + R_2\right) \tag{4.3}$$

where $R_{o\text{-}pass}$ is the output resistance of the pass element. The output resistance of the load (R_L) is commonly neglected because its value is considerably large than R_x. If C_o is assumed to be reasonably larger than C_b (typical condition), then Z approximates to

$$Z \approx \frac{R_X\left[1+sR_{esr}C_O\right]}{\left[1+s\left(R_X+R_{esr}\right)C_O\right]\cdot\left[1+s\left(R_X \parallel R_{esr}\right)C_b\right]} \tag{4.3}$$

It can be observed from equation (4.1) to (4.4) that the overall transfer function of the system consists of three poles and one zero, a potentially unstable system. Since R_1+R_2 is greater in magnitude (especially at high current), R_x simplifies to $R_{o\text{-}pass}$. The poles and zero can thus be approximated to be the following:

$$P_1 \approx \frac{1}{2\pi R_{o-pass}C_O} \tag{4.4.a}$$

$$P_2 \approx \frac{1}{2\pi R_{esr}C_b} \tag{4.4.b}$$

$$P_3 \approx \frac{1}{2\pi R_{oa}C_{par}} \tag{4.4.c}$$

$$Z_1 = \frac{1}{2\pi R_{esr}C_O} \tag{4.4.d}$$

and Figure 4.3 illustrates the typical frequency response of the system under two different loading current assuming that the output capacitor (C_O) is larger than the bypass capacitor (C_b).

- **Worst-case Stability**

The following step is to analysis the stability issue introduced from the low frequency poles. The worst case arises when the phase margin is at its lowest point, which occurs when the unity gain frequency is pushed out to higher frequency where the parasitic poles reside. This happens when the load-current is at its peak values. This is because the dominant pole (P1) usually increases at a faster rate ($R_{o\text{-}pass}$ decreases linearly with increasing current, $I/\lambda I_o$,where λ is the channel length modulation parameter of MOS devices) than the gain of

the system decreases (g_{mp} $R_{o\text{-}pass}$ decreases with the square roots of the increasing current for an MOS device) as showen in Figure 4.3. The type and value of the output capacitor determine the location of P_1, P_2, and Z_1. Therefore, the permissible range of values of ESR for a stable circuit is a function load-current and circuit characteristics.

- **Parasitic Pole Requirements**

The parasitic pole of the system can be identified as P_3 and the internal poles of the error amplifier. These poles are required to be at high frequency, at least greater than the unit gain frequency. The phase margin for the case where only one parasitic pole was at the vicinity of the unit gain frequency is at approximately 45°. Ensuring that P_3 is at high frequencies is an especially difficult task to undertake in a low current environment. The pole is defined by the large parasitic capacitance (C_{par}) resulting from a large pass element and the output resistance of the amplifier (R_{oa}). The output impedance of an amplifier is always a function of the circuit topology and he bias current of its output stage. As a result, low quiescent current and frequency design issue have conflicting requirements that necessitate compromises [19].

- **Load Regulation**

Load regulation performance (output resistance of the regulator, R_o) is a function of the open-loop gain (A_{ol}) of the system and can be expressed as

$$R_O = \frac{\Delta V_{LDR}}{\Delta I_O} = \frac{R_{o-pass}}{1 + A_{ol}\beta} \tag{4.5}$$

where ΔV_{LDR} is the output voltage variation arising from a load current variation of ΔI_O, $R_{o\text{-}pass}$ is the output resistance of the pass device, and β is the feedback factor. Consequently, the regulator yields better load regulation performance as the open-loop gain increase. However, the gain is limited by the close-loop bandwidth of the system, equivalent to the open-loop unit gain frequency (UGF). The minimum unit gain frequency is limited by the

response time required by the system during transient load current variations. Furthermore, the UGF is also bounded at the high frequency range by the parasitic poles of the system, i.e., the internal poles of the amplifier and pole P_3. In particular, the worst case condition occurs when Z_1 is at low frequencies and P_2 is at high frequencies, which corresponds to the maximum value of ESR and the lowest bypass capacitance (C_b). Moreover, the pass element associated input capacitance is significantly large. This places a ceiling on the value of the amplifier output resistance (R_{oa}). The pass element usually needs to be a large size device to yield low drop-out voltages and high output current characteristics with limited voltage drive in a low voltage and low power environment. Overall, load regulation is limited by the constrained open-loop gain of the system.

4.1.3 Transient Analysis

An important specification is the maximum allowable output voltage change for a full range transient load current step. Figure 4.4 shows transient response of the LDO under a sudden load current step change.

The worst case time required for the loop to respond is specified by the maximum permissible output voltage variation (ΔV_{tr}), which is a function of the output capacitor (C_o), the electrical series resistance (ESR) of the output capacitor, the bypass capacitors (C_b), and the maximum load current ($I_{Load\text{-}max}$),

$$\Delta V_{tr-max} \approx \frac{I_{Load-max}}{C_O + C_b}\Delta t_1 + \Delta V_{esr}$$

$$\text{thus} \quad \Delta t_1 \approx \frac{[C_O + C_b]}{I_{Load-max}}[V_{tr-max} - \Delta V_{esr}], \tag{4.6}$$

where ΔV_{esr} is the voltage variation resulting from the presence of the ESR of the output capacitor. The effects of ESR are reduced by the bypass capacitors (C_b), which are typically high frequency thereby exhibiting low ESR values. The duration Δt_1 is a function of bandwidth, internal slew-rate associated with the parasitic capacitance C_{par} of the pass

element. The resulting time can be approximated to be

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V}{I_{slew}}, \tag{4.7}$$

where BW_{cl} is the closed-loop bandwidth of the system, t_{sr} is the slew-rate associated with C_{par}, ΔV is the voltage variation at C_{par}, and I_{slew} is the slew-rate limited current. If the I_{slew} is large enough, the bandwidth of the close-loop will dominate Δt_1.

Once the slew-rate condition is terminated, the output voltage recovers and settles to its final value, ΔV_2 below the ideal value,

$$\Delta V_2 \approx R_{o-reg} I_{Load-max}, \tag{4.8}$$

where $R_{o\text{-}reg}$ is the closed-loop output resistance of the regulator. This is essentially the effect of load regulation performance. And the settling time (Δt_2) is dependent on the time required for the pass device to fully charge the load capacitors and the phase margin of the open-loop frequency.

In fact, the slew rate condition should be concerned. It typically occurs when load current steps from zero to full scale. The condition is dependent on the configuration of the output stage of the error amplifier and the output pass device. The output voltage variation (ΔV_3), whose magnitude is defined by the voltage charged on the capacitors and the voltage generated across the ESR of the output capacitor. This results because the momentary current supplied by the power device flows to C_o and C_b. Consequently, the capacitors are charged and a temporary voltage drop is created across R_{esr}. The transient voltage variation can be approximately expressed as

$$\Delta V_3 \approx \frac{I_{Load-max}}{C_O + C_b}\Delta t_3 + \Delta V_{esr} \approx \frac{I_{Load-max}}{C_O + C_b} \cdot \frac{1}{BW_{cl}} + \Delta V_{esr}. \tag{4.9}$$

Finally when the output transistor is shut off (afterΔt_3) the variation settles down to ΔV_4, the voltage charged on the capacitors ($\Delta V_4 \fallingdotseq \Delta V_3 - \Delta V_{esr}$). At this point, the output voltage takes time Δt_4 to discharge to its final ideal value,

$$\Delta t_4 \approx \frac{C_O + C_b}{I_{pull-down}} \Delta V_4 = \frac{[C_O + C_b]R_1}{V_{ref}} \Delta V_4 . \quad (4.10)$$

As a result, the additional off-chip bypass capacitors (low ESR capacitors) reduce the peak value of $\Delta V_{tr\text{-}max}$ and ΔV_3. This results because the current supplied by the output capacitor (C_o) during transient condition is decreased as C_b is increased thereby exhibiting a lower voltage drop across R_{esr}. The remaining current is supplied by the bypass capacitors, which have negligible ESR voltage drops [20].

4.2 Circuit Blocks

As the Figure 4.1 shown, LDO system is composed of an error amplifier, a pass element, feedback resistor network, bandgap voltage reference, off-chip compensating capacitor, associated electrical series resistor (ESR), and bypass capacitor. Based on the theoretical analysis, the circuit structure and schematic of each part in the system is introduced in this section. And then, the system can be separated into two parts, LDO core and bandgap voltage reference respectively.

First, the LDO core schematic is illustrated in Figure 4.5. The error amplifier plays an important role in LDO design. The specifications of the error amplifier that are relevant to the regulator as inferred from the previous discussions are: output resistance, gain, bandwidth, output slew-rate current, output voltage swing and quiescent current. The output impedance must be low enough to place the parasitic pole P_3 at a frequency greater than the unity-gain frequency. Due to the low voltage application, the number of stacked transistors should be minimized. Therefore the telescopic or cascade topology is not suitable for this work. The performance of the LDO is dominated by the loop-gain, which could be contributed from a single-stage operational amplifier and a PMOS pass device. Thus, the single-stage topology is chosen to satisfy low voltage and quiescent current as well.

On other hand, the pass element is also an issue in LDO system. Designing in a low voltage and low current environment provides difficult challenges that contradict performance and stability. The pass device should provide large amount of current while displaying low-drop characteristics. So the size of the transistor as the pass device must be large under low voltage condition. A large device is further demanded because voltage drive is reduced as a result of decreased input voltages. The phenomenon causes the parasitic pole P_3 to move to lower frequencies effectively deteriorating phase margin and compromising the stability of the system. In summary, the size of the pass device must be large for increased current capabilities but restrained by stability and slew rate requirements in a low quiescent current and low voltage environment. In this work, the PMOS is used because the drop-out voltage between the input voltage and the output voltage should be minimized.

Second, the bandgap voltage reference structure and schematic are illustrated in Figure 4.6 and Figure 4.7 [21]. The amplifier enforces nodes N_1 and N_2 to have equal potential. As a result, nodes N_3 and N_4 also have equal potential when $R_{2A1}=R_{2B1}$ and $R_{2A2}=R_{2B2}$. Therefore, the loop formed by Q1, Q2, R1, R_{2A1}, R_{2B1}, R_{2A2}, and R_{2B2} generates a current I given by

$$I = \frac{V_{EB2}}{R_2} + \frac{V_T \cdot \ln N}{R_1}, \tag{4.11}$$

where N is the emitter area ratio, V_T is the thermal voltage and $R_2 = R_{2A1}+R_{2A2} = R_{2B1}+R_{2B2}$. The current I is injected to R_3 by current mirror formed by M_1, M_2, and M_3. And the reference voltage is described as follows:

$$V_{ref} = \frac{R_3}{R_2} \cdot \left[V_{EB2} + \left(\frac{R_2}{R_1} \ln N \right) \cdot V_T \right]. \tag{4.12}$$

A scaled-down bandgap reference voltage can be obtained by an appropriate resistor ratio of R_3 and R_2. Moreover, this circuitry takes advantage of resistor ratio (ratio of R_2 and R_1) not only to achieve a good temperature coefficient but also reduce the supply voltage. The minimum supply voltage V_s is given by

$$V_{s(min)} = \left(\frac{R_{2B2}}{R_{2B1} + R_{2B2}} \right) \cdot V_{EB2} + \left| V_{thp} \right| + 2\left| V_{DS(sat)} \right|. \quad (4.13)$$

Moreover, bandgap voltage reference in CMOS technology suffers from the effect of MOS transistor offset due to the mismatches of transistor size and threshold voltage. If the effect of offset voltage is considered, the previous equation could be modified by

$$V_{ref} = \frac{R_3}{R_2} \cdot \left[V_{EB2} + \frac{R_2}{R_1} \cdot \left(V_T \cdot \ln N + \frac{R_2}{R_{2A2}} \cdot V_{OS} \right) \right]. \quad (4.14)$$

And then the complete LDO regulator schematic including self-bias and startup circuit is shown in Figure 4.8.

4.3 Simulation Results

The relevant simulation results of proposed regulator system are introduced in this section. The error amplifier simulation result is shown in Table4.1. The average current consumption of this amplifier is about 17 μA when the supply voltage is lowest. And the AC simulation concept of the loop-gain under loading condition is shown in Figure 4.9. The method is applying a very large capacitor and an inductor to block and short the DC signal respectively. And the simulation result is shown in Table 4.2.

To guarantee the regulator can properly work, the post-layout simulation conditions include process variation, temperature variation and supply variation. Figure 4.0 through 4.13 describe the performance of the LDO linear regulator. Figure 4.10 demonstrates the transient response of the LDO under the simulated condition that the supply voltage changes from 1.2 to 1.8 V, and the load-current is 1 mA. Figure 4.10(a) shows the result for C_o = 1 μF with R_{esr} = 50 Ω, and Figure 4.10(b) shows the result for C_o = 4.7 μF with R_{esr} = 50 Ω. It shows that this LDO could recover the output voltage within 40μs. And Figure 4.11 demonstrates the transient response of LDO under the simulated condition that a full load-current switching

from 0 to 10 mA, and the supply voltage is 1.2 V. Figure 4.11(a) and (b) show the results for different loading condition. According to the above results, the output voltage is still regulated at the desired voltage (1V), while the load-current varies extremely from 0 to 10mA and vice versa.

Figure 4.12 shows the input/output characteristics of the regulator under the simulation condition that the load-current is 1 mA, output capacitor is 4.7 μF, ESR is 0.5 Ω, and process variations are concerned as well. Table 4.3 demonstrates the specification of the LDO system including the process variations.

Temperature coefficient (TC) is an important parameter of the bandgap reference. Figure 4.13 shows the simulated temperature behavior of the bandgap reference under three process corners. And the simulated TC at V_{supply} = 1.2 V is 11.242 ppm/°C under TT corner.

4.4 Layout Description and Measurement Results

The proposed linear regulator system was successfully fabricated in TSMC 1P6M 0.18-μm CMOS process. Figure 4.14 shows the whole chip layout of the low dropout regulator. In this work, the output pass transistor (MP1) is the key to operation, performance, and reliability of all the circuit. Therefore the design and layout of the pass transistor require more attenuation. For example, every finger of this pass transistor should turn on or turn off simultaneously. The width of the metal lines of input and output node should be enough in case of metal migration problems. And the chip microphotograph is shown in Figure 4.15.

Figure 4.16 depicts the measurement setup to test the performance of the proposed linear regulator system. In the setup, some external components were added, including an output capacitors, a load resistors, and a power switch to switch the load current. The gate of the power switch was connected to a pulse generator to control the load current flow. And two power supplies were needed. One provides supply voltage for the linear regulator, and the

other provides a dc voltage to V_{sw} pad in order to control if turn on V_{ref} signal. The other performances of LDO linear regulator were tested by changing input voltage, or load current, and the output voltage is measured through the oscilloscope and multimeter.

In Figure 4.17(a), the line regulation was measured by changing the input voltage, V_{in}, when the load resistor was 1 kΩ. In other words, the load current was 1 mA. And the load regulation was measured by changing the load current, I_o, as shown in Figure 4.17(b). In sum, the measurement and simulation results of this low dropout regulator were listed in Table 4.5. Although output power of a unit nanodevice (30μm / 0.5μm, width / length) is not sufficient t, the parallel electrodes could be utilized to provide enough power for further applications.

Table 4.1 The specification of the error amplifier

Supply Voltage (V)	**1.2**	**1.5**	**1.8**
Current Consumption (μA)	17.00	18.19	19.28
DC Gain (dB)	47.6	49.3	49.6
Phase Margin (degree)	86.5	86.5	86.5
Unit-Gain Frequency (MHz)	2.08	2.16	2.23

Table 4.2 The specification of the feedback loop.

Load current (mA)	**2**	**4**	**6**	**8**	**10**
Loop-Gain (dB)	74.1	72.9	71.6	70.4	69.2
Phase Margin (degree)	32.2	36.6	39.8	42.2	44.3
Unit-Gain Frequency (KHz)	152	196	228	250	272

Table 4.3 Specification of the low dropout linear regulator system.

Corner	**SS**	**TT**	**FF**
Vout	1008 mV	1004.4 mV	992 mV
Vref	807 mv	800.5 mV	794 mV
$I_{Quiescent}$ (V_{in}=1.2)	36.49 μA	36.49 μA	40.02 μA
Drop-out voltage	149 mV	173 mV	200 mV
Line regulation	0.442% V/V	0.625% V/V	0.711% V/V
Load regulation	1.46 mV/mA	1.25 mV/mA	1.46 mV/mA
BGR Temp. coefficient	9.887-ppm/°C	11.242-ppm/°C	27.810-ppm/°C
BGR Line regulation	0.344% V/V	0.345% V/V	0.548% V/V
Stability	Yes	Yes	Yes

Table 4.4 The parameter of each device

MOSFET (μm/μm)					
M1	5/1	M2	5/1	M3	5/1
MA1	3/1 M=2	MA2	3/1 M=2	MA3	2/1
MA4	2/1	MA5	4/1	MA6	2/1 M=2
MA7	4/1	MB1	2/1	MB2	2/1 M=2
MB3	4/1	MB4	4/1	ML1	5/4 M=4
ML2	5/4 M=4	ML3	5/2 M=5	ML4	5/2 M=5
ML5	2/1 M=2	MS1	4/1	MS2	2/0.18
MS3	2/0.18	MS4	1/10	MS5	1/10
MP1	10/0.18 M=400			Mswitch	1/0.18
BJT					
Q1	pnp10 N=12	Q2	pnp10		
N-well resistor (ohmic)					
R1	30k	R2A1	257.1k	R2A2	42.9k
R2B1	257.1k	R2B2	42.9k	R3	185.7k
RF1	200k	RF2	800k		
MIM capacitor (farad)					
Cc	100f				
off-chip element					
Co	1~4.7 μF	Cb	20 pF	RB	8 kΩ
Resr	0.5 Ω				

Table 4.5 Measurement results of the low dropout linear regulator system.

Corner	Simulation-SS	Simulation- TT	Simulation-FF	Measurement*
Vout	1008 mV	1004.4 mV	992 mV	1011.32 mV
Vref	807 mv	800.5 mV	794 mV	753 mV
$I_{Quiescent}$ (V_{in}=1.2)	36.49 μA	36.49 μA	40.02 μA	31.5 μA
Drop-out voltage	149 mV	173 mV	200 mV	180 mV
Line regulation	0.442% V/V	0.625% V/V	0.711% V/V	5.72% V/V
Load regulation	1.46 mV/mA	1.25 mV/mA	1.46 mV/mA	2.94 mV/mA
Stability	Yes	Yes	Yes	Yes

*** When measuring this LDO regulator, an external voltage was applied in order to avoid the error effect induced by V_{ref}.**

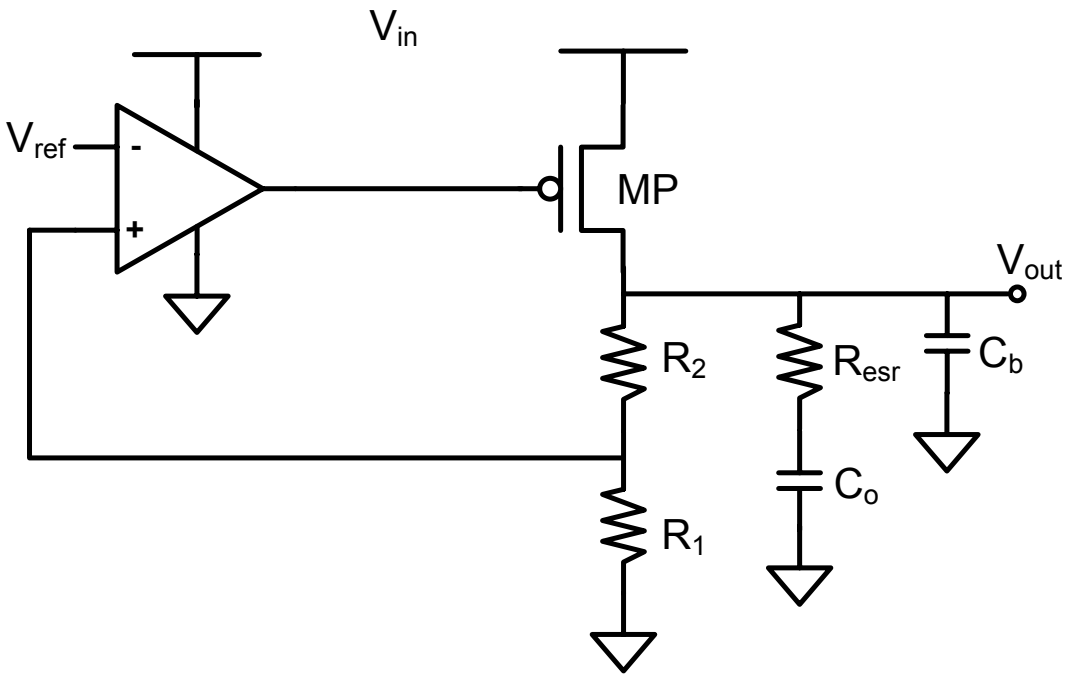


Figure 4.1 Low drop-out regulator architecture.

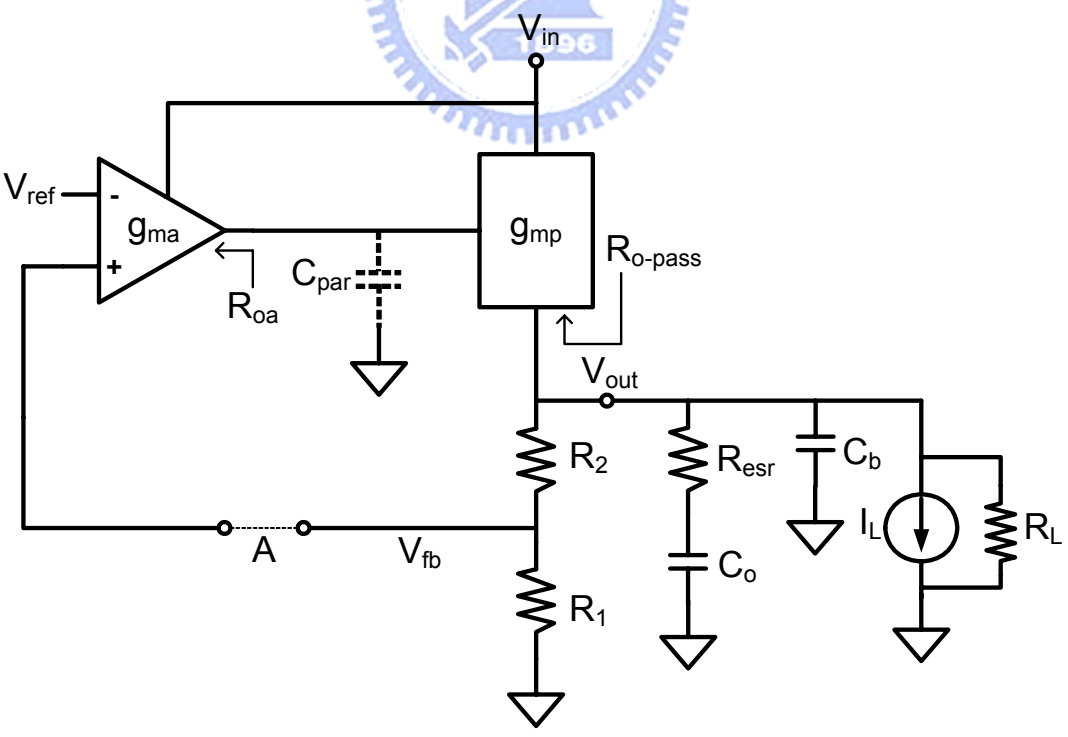


Figure 4.2 System model under loading conditions.

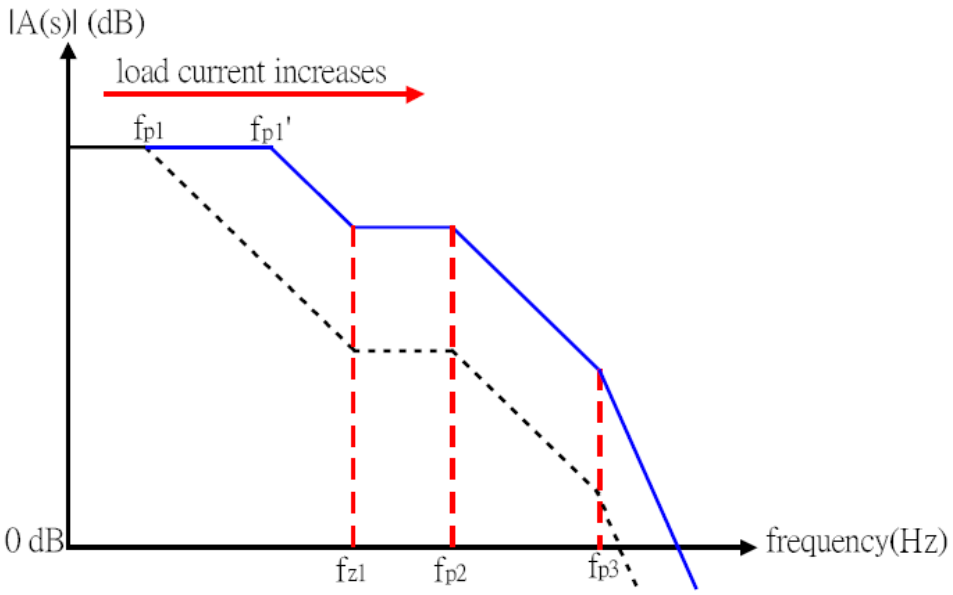


Figure 4.3 LDO frequency response under two different loading currents

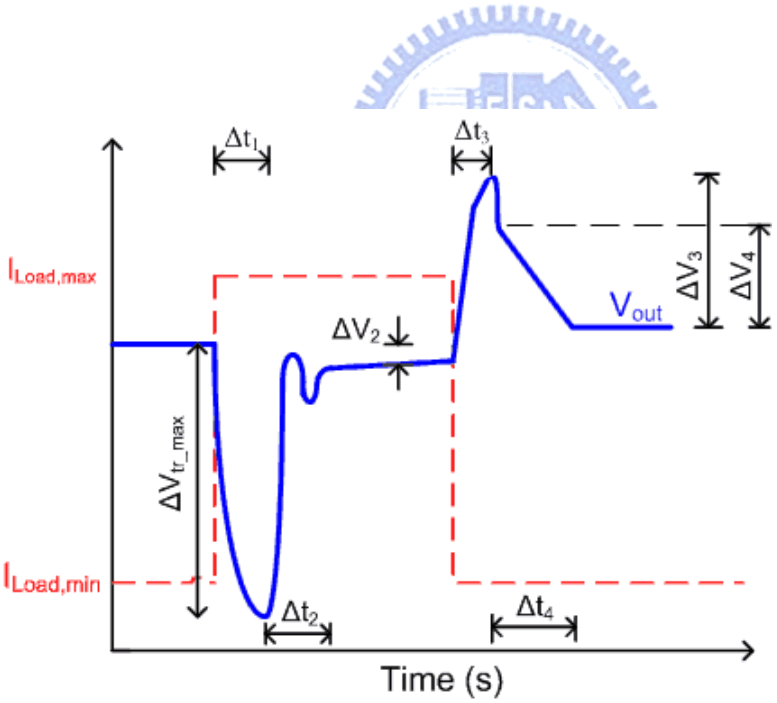


Figure 4.4 Transient response under a sudden load current step change

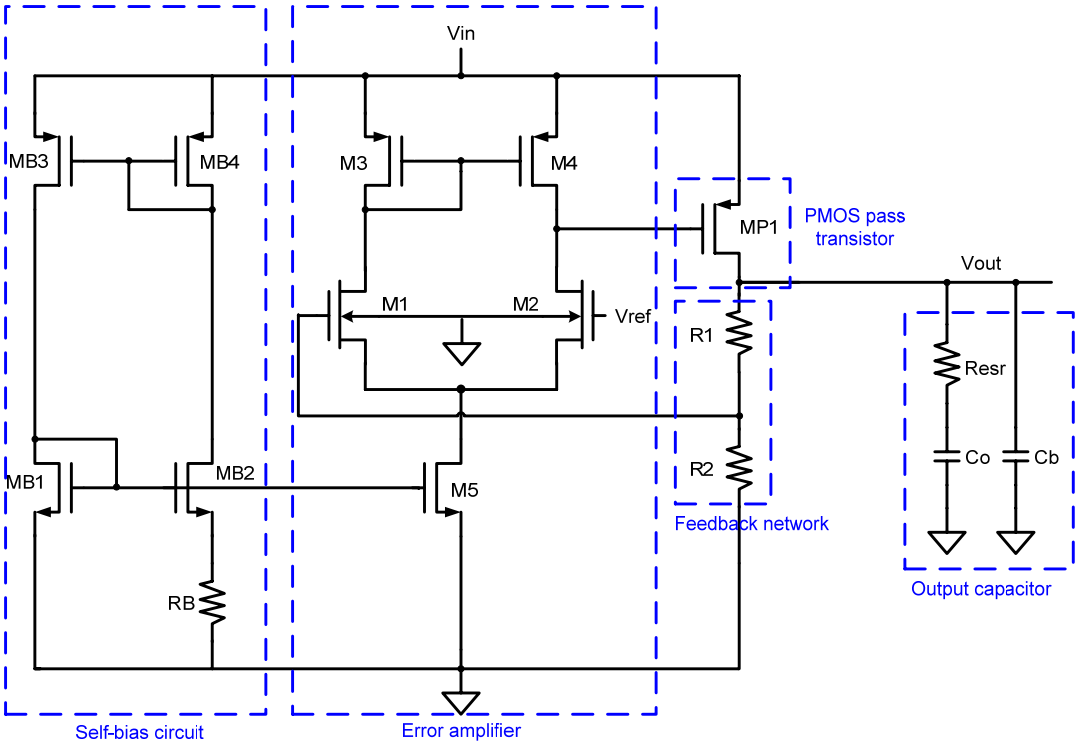


Figure 4.5 Schematic of the LDO core circuit, including the error amplifier, self-bias circuit, PMOS pass transistor, feedback network, and output capacitors.

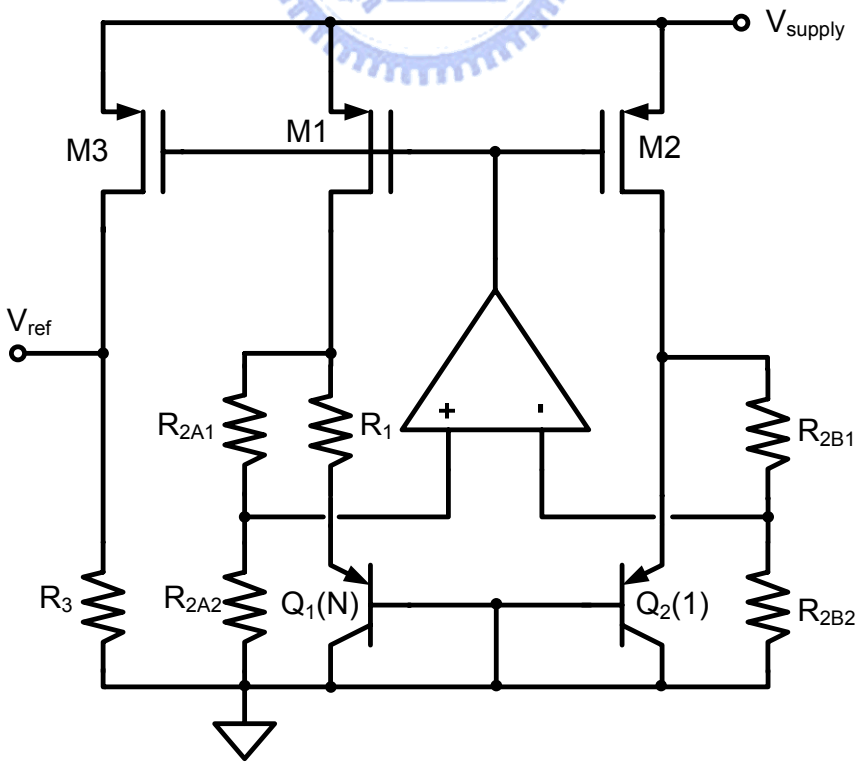


Figure 4.6 The implementation of bandgap reference with a low Vsupply topology.

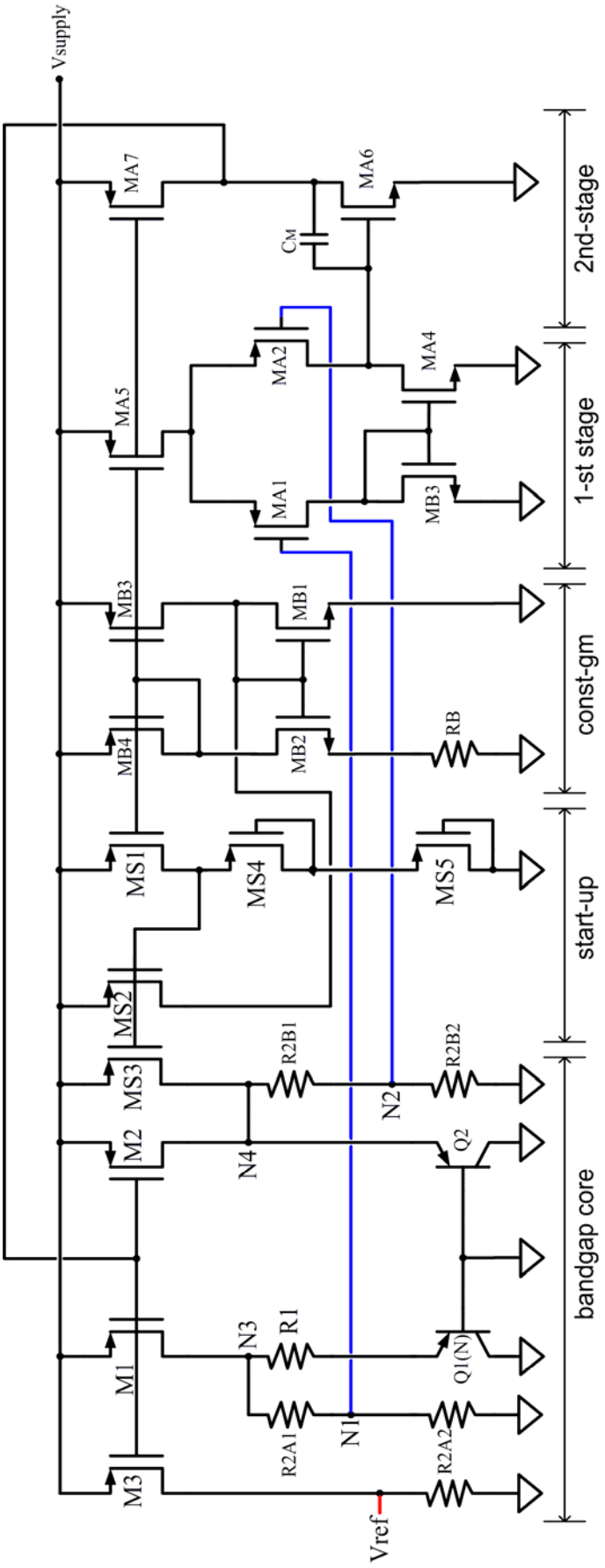


Figure 4.7 Schematic of low voltage bandgap reference.

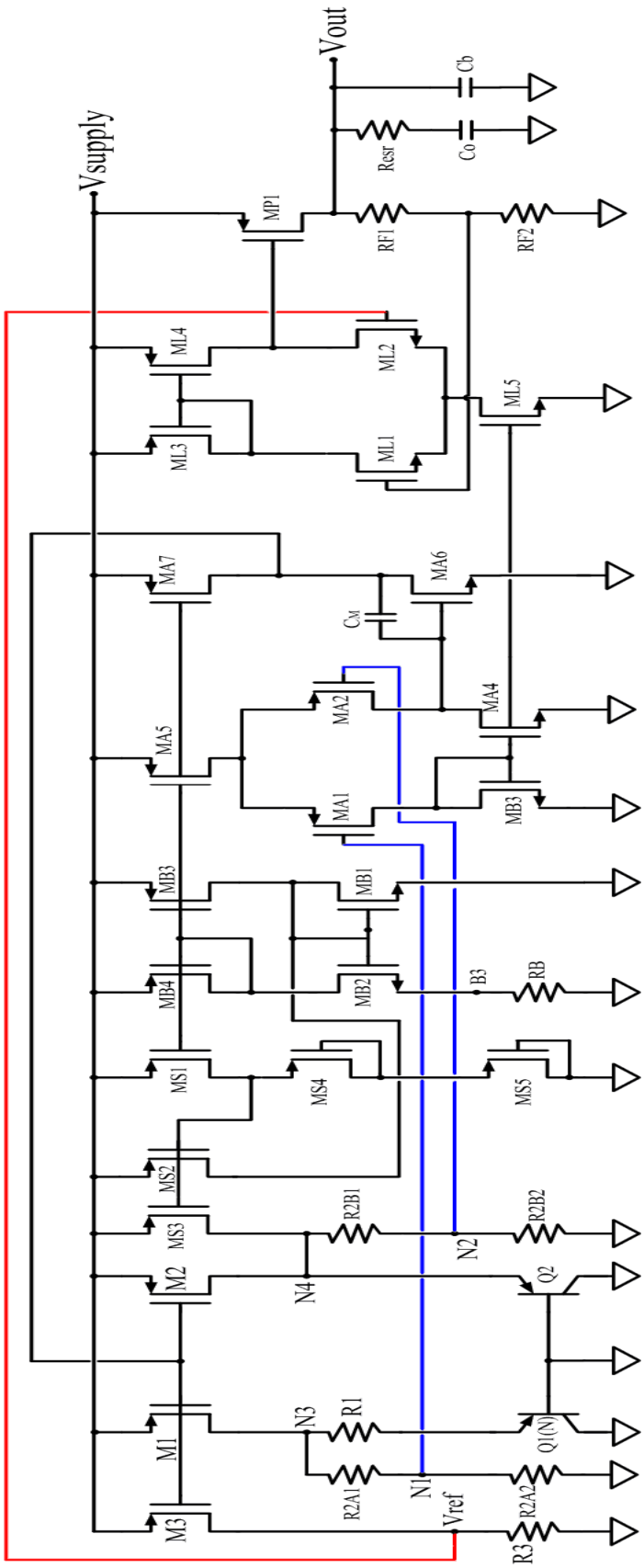


Figure 4.8 Schematic of complete LDO system.

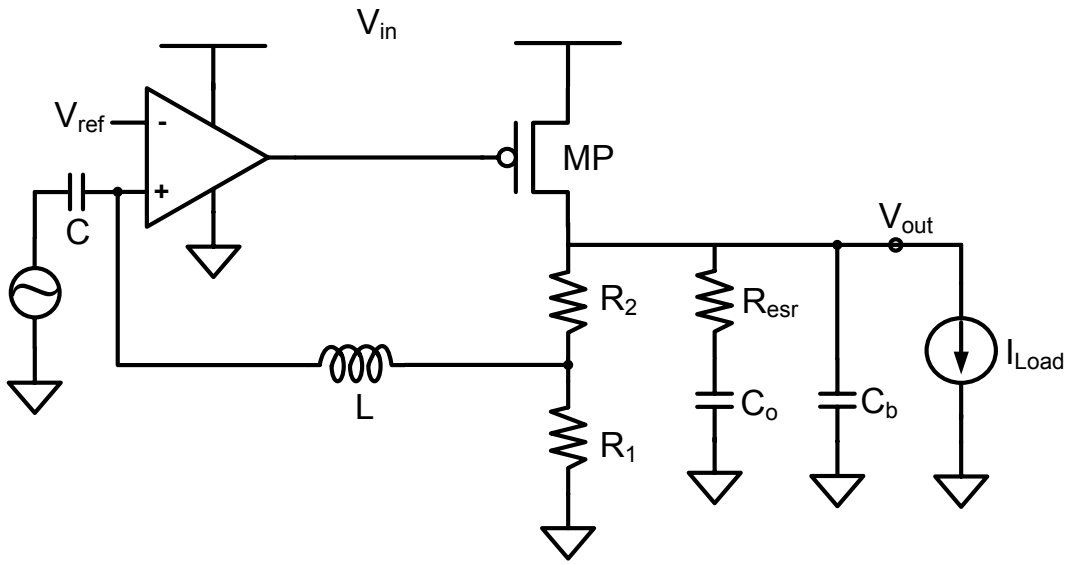
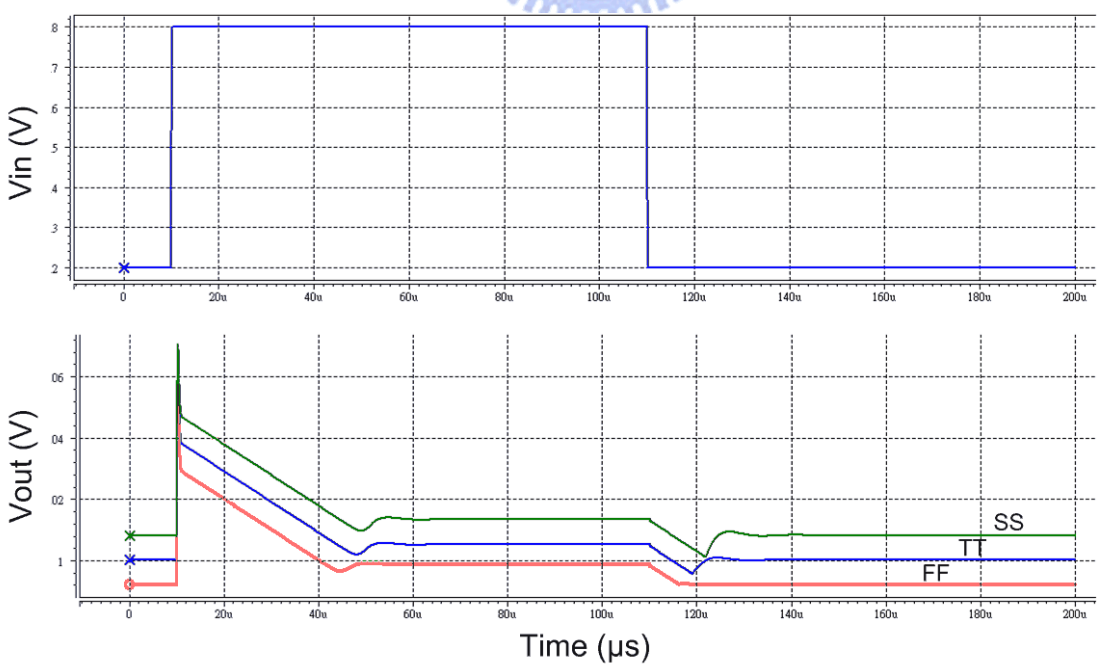
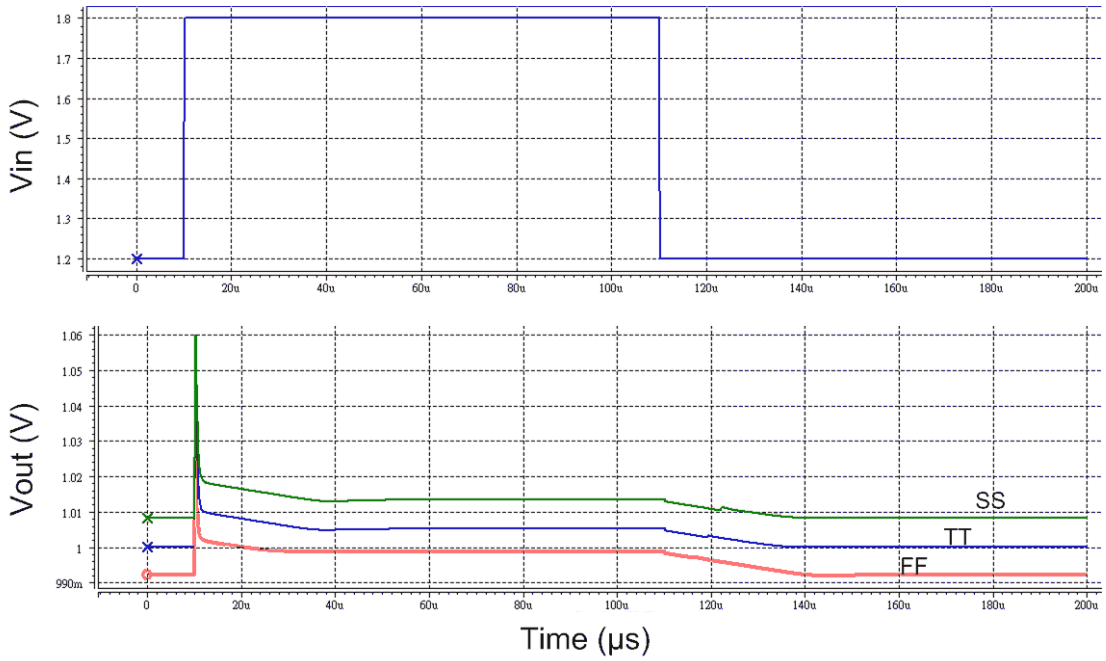


Figure 4.9 The AC simulation concept of the loop-gain.

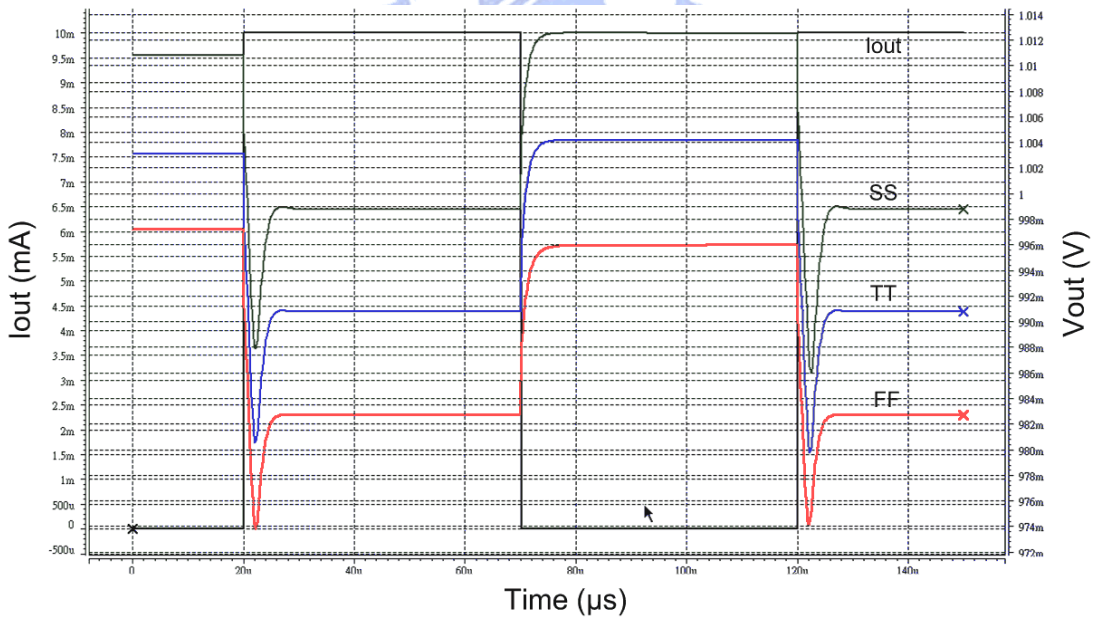


(a)

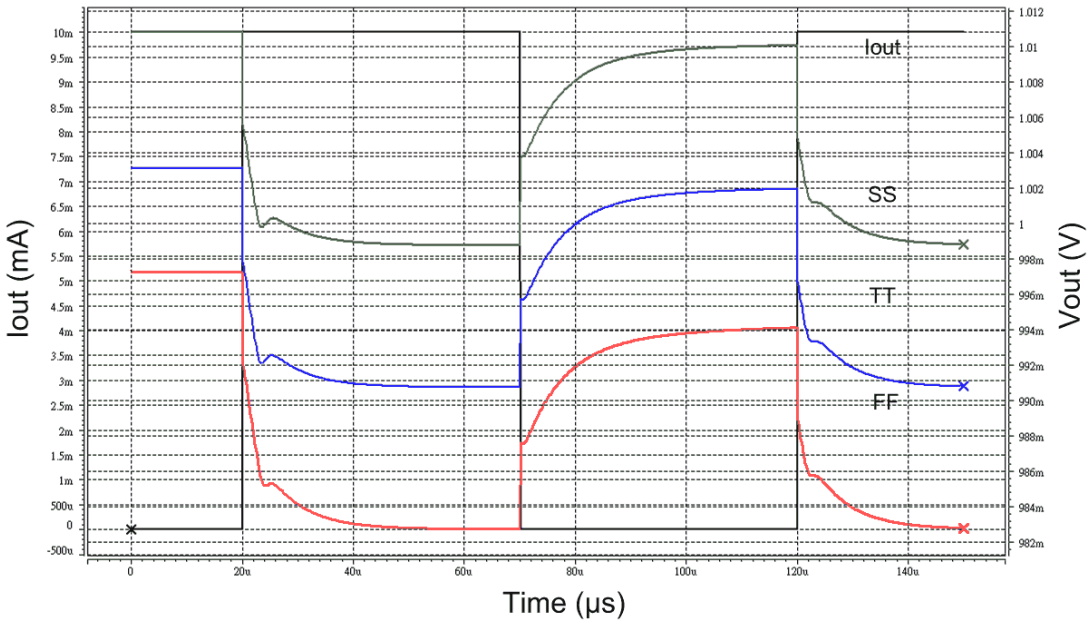


(b)

Figure 4.10 Output variation under a sudden chip supply voltage change. Under ILoad=1mA, Resr=0.5Ω (a) Co=1µF, (b) Co=4.7µF.



(a)



(b)

Figure 4.11 Output variations under a full load current change. Under Vsupply=1.2V, Resr=0.5Ω (a) Co=1µF, (b) Co=4.7µF.

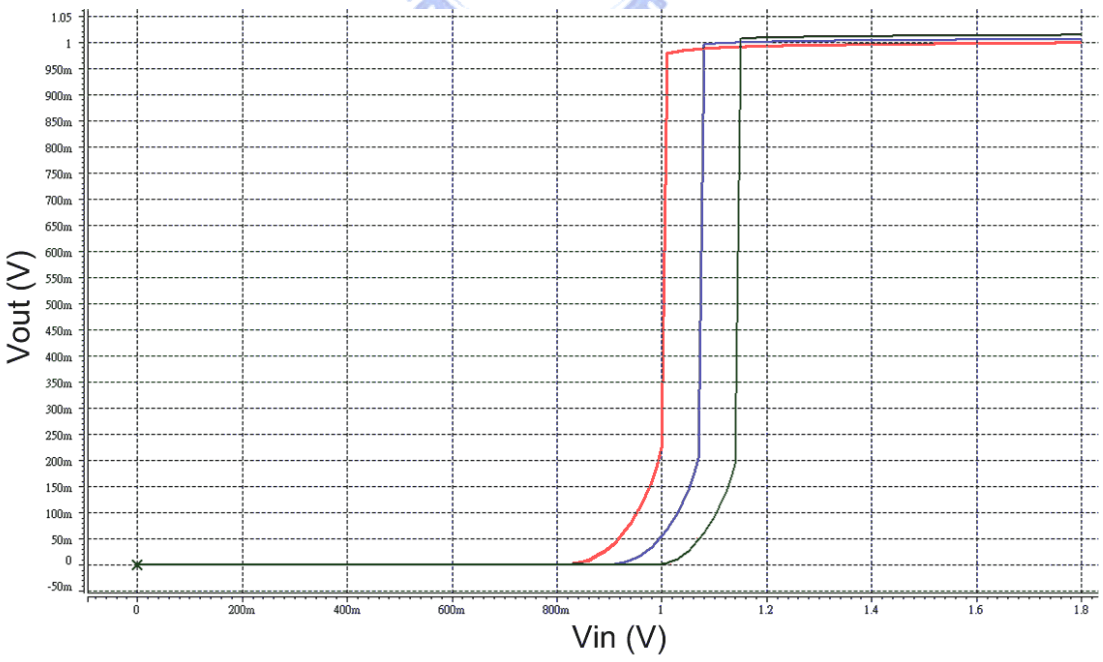


Figure 4.12 Simulated input/output voltage characteristics of the regulator

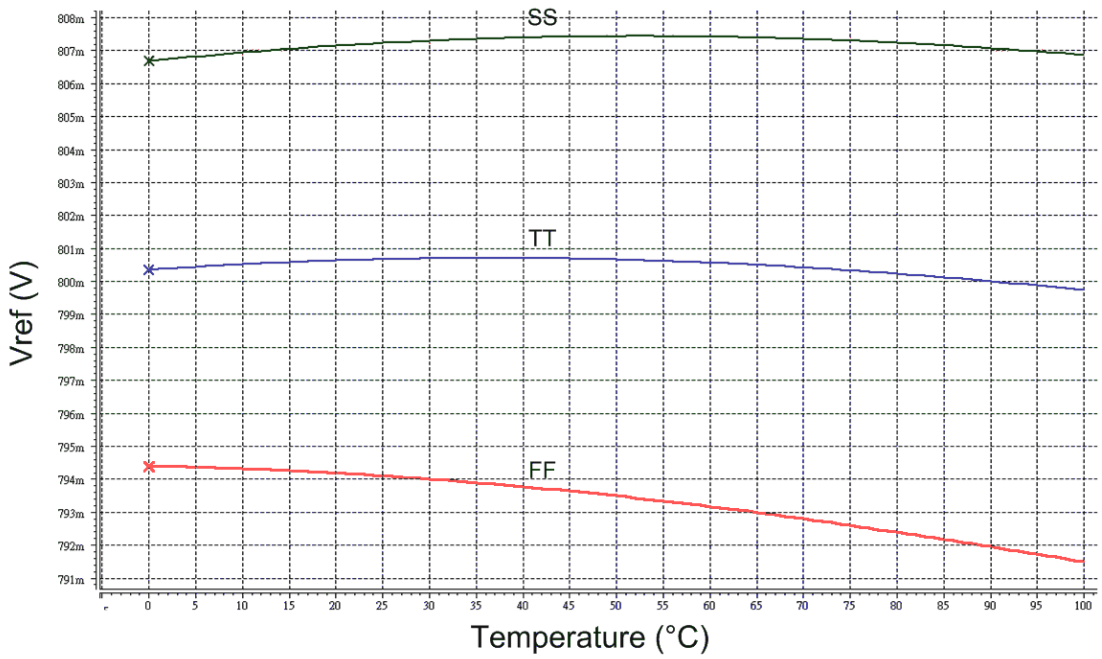


Figure 4.13 Simulated temperature behavior of the bandgap voltage reference.

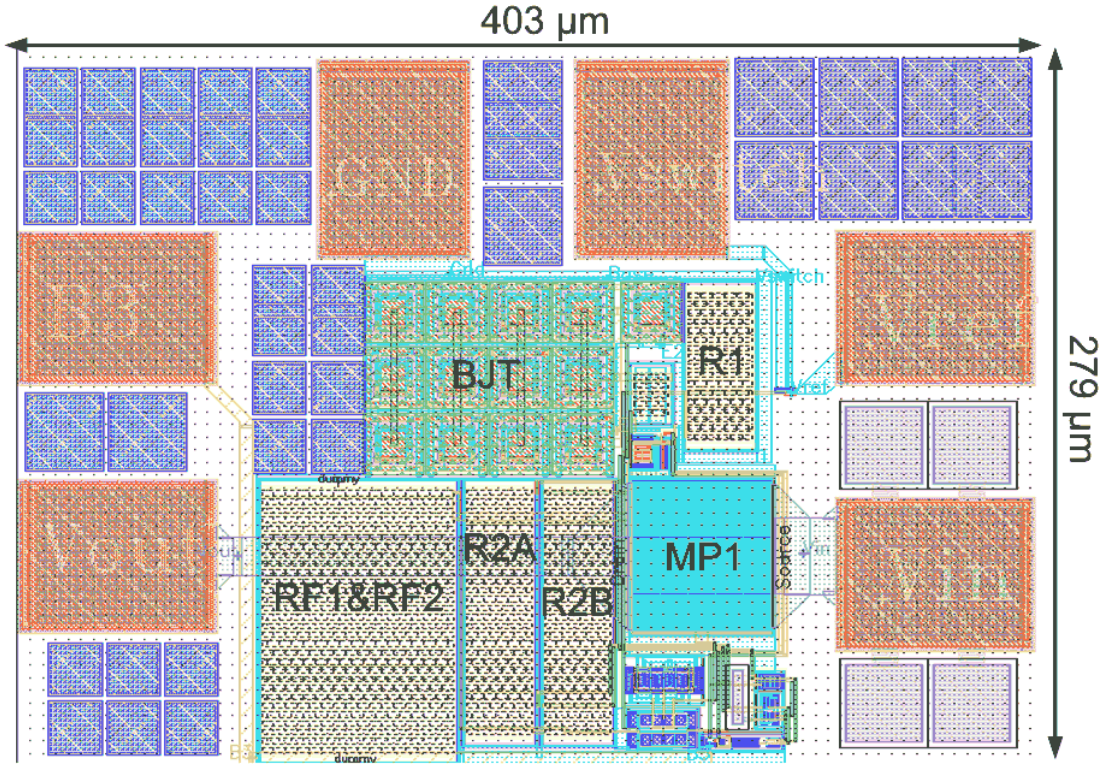


Figure 4.14 Layout of low drop-out regulator

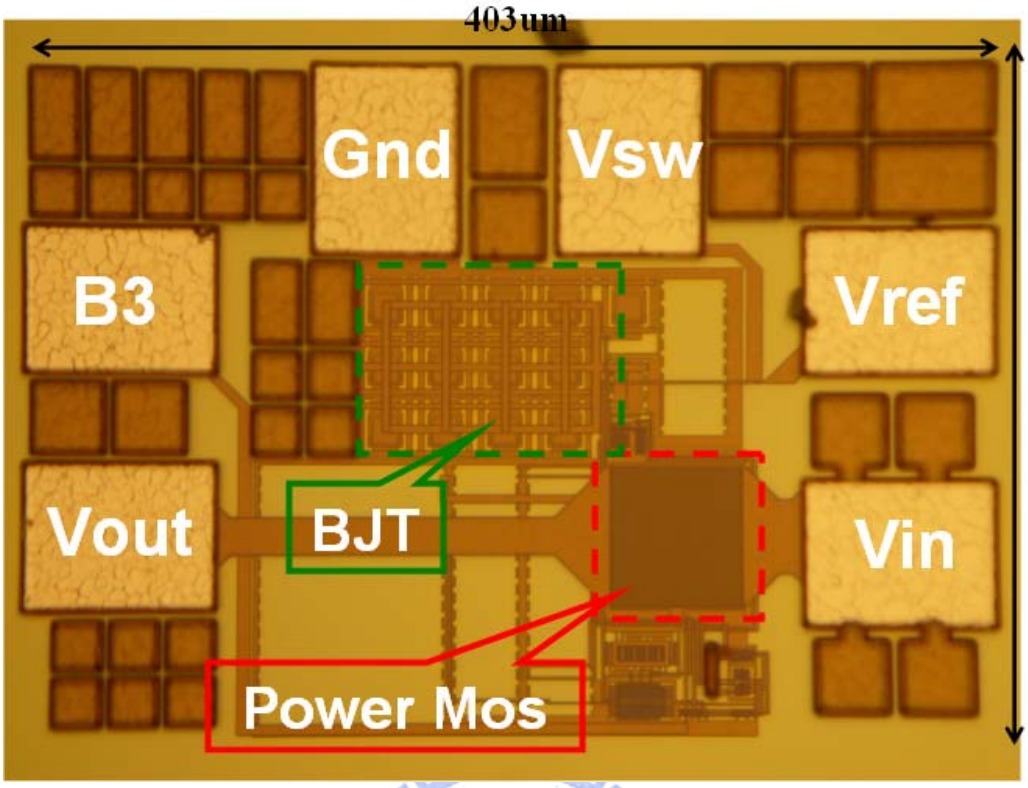


Figure 4.15 Chip microphotograph

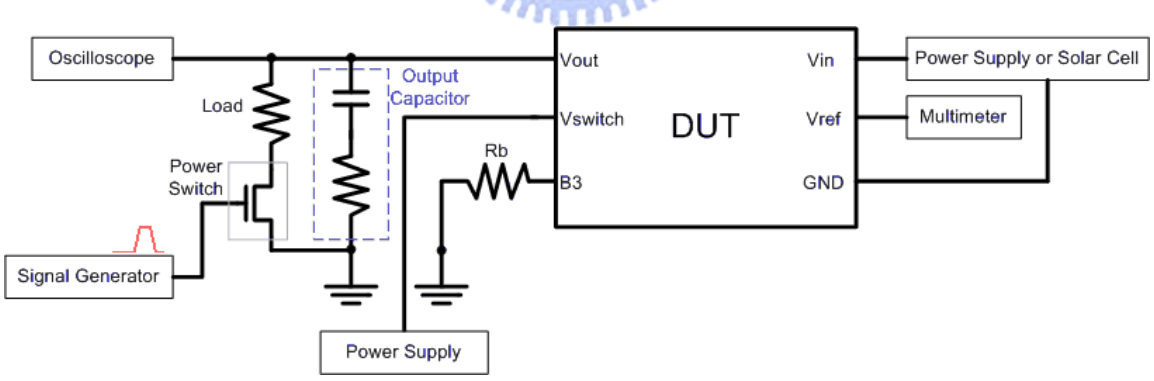
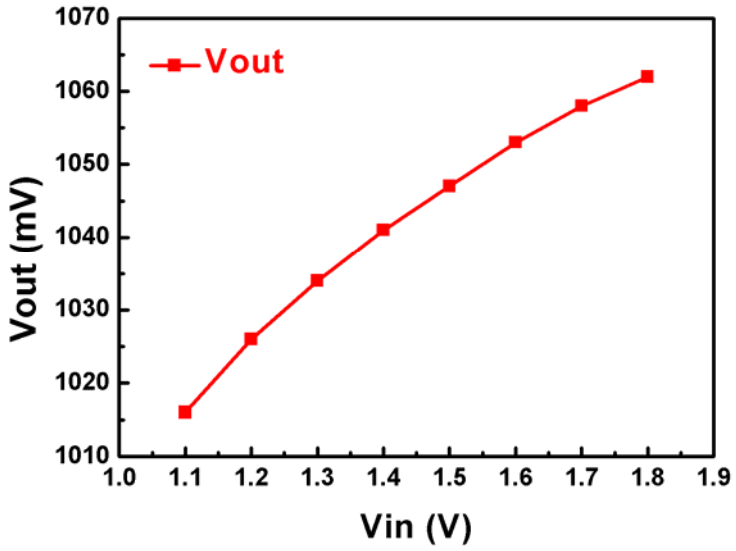
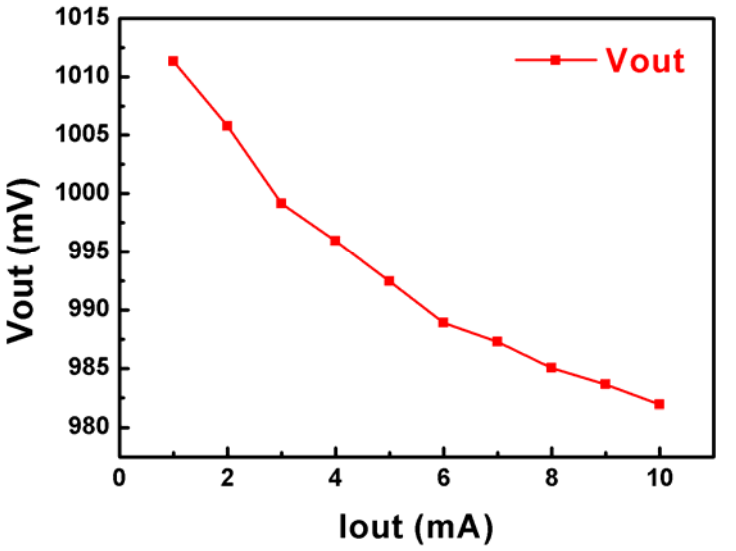


Figure 4.16 Measurement setup.



(a)



(b)

Figure 4.17 (a) Regulated voltage when load current was 1 mA under different input voltage, (b) regulated voltage when input voltage was 1.2 V under changing load current.

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 Conclusions

In this work, an advanced nanodevice structure with Au nanoparticles and PDDA-capped CdSe/ZnS quantum dots for solar cell application has been proposed. The function of PDDA layer was to improve the quantum yield of CdSe/ZnS QDs. And QDs with different diameters were applied to realize the wideband solar cell. Because semiconductor QDs such as CdSe with tunable band edge offer the opportunities to harvest light energy in the entire region of solar light, an ordered assembly of PDDA-capped CdSe/ZnS QDs with different diameters was employed. To control and assemble Au NPs and PDDA-capped CdSe/ZnS QDs into well-defined nanostructure, the ionic interaction between Au NPs and PDDA-capped CdSe/ZnS QDs or between Au NPs and silicon oxide substrate was used by dip-and-wash" procedure. The dip time was 12 hours per layer and the environment temperature was 4° C which was sufficient to deposit the high density structure for the nanodevice. First, the silicon chip was modified by N- [3-(trimethoxysilyl) propyl] ethylene diamine (TMSPED) to make the silicon oxide substrate provide amino groups ($-NH3^{+}$). Subsequently, citrate-capped Au NPs、PDDA-capped CdSe/ZnS QDs were self-assembled layer-by-layer, alternately, between the electrodes. The nanostructure after each layer was formed on the silicon oxide substrate and observed by SEM images. UV-visible and PL intensity spectra were used to verify the construction of each layer on quartz glass substrate. And the process of construction after formation each layer on silicon substrate was observed by SEM. Finally, the electrical properties of the solar cell nanodevices were observed. The electrodes sets, 30 μm / 5 μm, 30 μm / 2.5μm, 30 μm / 1 μm, 30 μm / 0.5 μm (width / length) which were employed for I-V

measurement. The daylight lamp was used as light sources for nanodevice photo-excitation. For the nanodevice composed of Au NPs and PDDA-capped CdSe/ZnS QDs, there was a constant increment of photocurrent after illumination throughout the applied voltage biases, which resembles the characteristics of a photodiode. Furthermore, the three-dimensional "nano-schottky-diode" arrays equivalent circuit model was proposed and used to explain the photo-sensing mechanisms, and the higher solar cell efficiency can be obtained based on the ideal inference.

In this work, under the 0.16 mW/cm^3 illumination, the best solar cell efficiency is 1.6% (6-layered PDDA-capped CdSe/ZnS nanodevice with 60 μm in width and 0.5 μm in length). The maximum photocurrent is 664.62 pA. Then, the maximum photocurrent volume density (PVD) is 7.385×10^{-19} A/nm^3 and power volume density is 4.256×10^{-22} W/nm^3. The power conversion efficiency can achieve 36.87% based on the ideal interference (6-layered PDDA-capped CdSe/ZnS nanodevice with 40 nm in length). In conclusion, there are some notable characteristics of the experimental results.

Au /PDDA-capped CdSe/ZnS nano-schottky diodes and resistors array performance trend

(1) For the same width / number of layer and excitation source

In dark: Length ↑ -> Conductivity ↓

Under illumination: Length ↑ -> Photocurrent ↓ , PVD ↓ , Efficiency ↓

Power Volume Density ↓

(2) Maximum PVD = 7.385×10^{-19} (A/nm^3),

in 6-layer nanodevice, 30 μm / 0.5 μm electrodes

(3) Maximum power volume density = 4.256×10^{-22} (W/nm^3),

in 6-layered nanodevice, 30 μm / 0.5 μm electrodes

(4) Maximum power conversion efficiency = 1.6 %,
in 6-layered nanodevice, 30 μm / 0.5 μm electrodes.

(5) After 24 days, 31.8% decrease in solar cell efficiency of proposed nanodevice, and
After 26 days, the decay tended to saturate.

(6) Estimated solar cell efficiency (ideal inference, not measurement data),
efficiency = 36.87 % in 6-layered nanodevice, 30 μm / 40 nm electrodes,
efficiency = 51.17 % in 6-layered nanodevice, 30 μm / 30 nm electrodes.

5.2 Future Works

The future works of this project can be divided into several parts:

(1) According to our conclusions, the length of the nanodevice could be shrunk to tens of nanometers to achieve high-efficiency solar cell. And the large area solar cell could be realized by parallel electrode-array. Furthermore, the transparent electrodes, for example ITO, could be used to increase the effective illuminated area. Beyond, the electrodes are fabricated in standard CMOS process, so regulator or sensor readout circuits could be integrated with electrodes.

(2) Since pH value of the quantum dots solution effects the attraction force strength of QDs, the positive-charged ($-NH_3^+$) PDDA-capped CdSe/ZnS QDs should be dissolved in a weak acid solvent, or buffer. And negative-charged ($-COO^-$) Au NPs should be dissolved in a weak alkali solvent, or buffer due to more $-OH^-$ charges. Therefore, the nanodevice structure could get higher density and better quality thin film.

(3) Annealing or baking process could be applied into fabrication process to increase the yield rate and reliability.

(4) The nanostructure could be confirmed through TEM.

(5) The accurate thickness of the thin film would be measured by x-ray diffraction (TF-XRD). And then the accurate photocurrent volume density and power volume density could be obtained.

(6) In this research, we have used the daylight lamp as excitation source to demonstrate the I-V characteristics of the proposed nanodevices. However, the standard solar simulator is still necessary to obtain the correct and dependable power conversion efficiency in the future.

(7) To involve material work function, doping, and carrier transportation effects into nanodevice simulations. Therefore we would obtain more precise nanodevice model.

(8) To study the mechanism of decay. Meanwhile, the nanodevice can be packaged to prevent oxidation or external interference, such as temperature, humidity, chemical and mechanical force, to extend the storage-time in air.

(9) The further works are to incorporate these inorganic nanodevices into nano-electronics system, like utilizing the nanodevice with nanoparticles as solar cell for the low-power and portable devices. Further applications and improvement on the proposed nanodevices are ongoing.

REFERENCE

[1] C. M. Niemeyer, "Nanoparticles, proteins, and nucleic acids: biotechnology meets material science," *Angew. Chem. Int. Ed*, vol. 40, pp. 4128-4158, 2001.

[2] A. Kongkanand, K. Tvrdy, K. Takechi, M. Kuno, and P. V. Kamat, "Quantum dot olar cells. Tuning photoresponse through size and shape control of CdSe-TiO_2 architecture," *J. Am. Chem. Soc.,* vol. 130 (12), pp. 4007-4015, 2008.

[3] D. B. Janes, T. Lee, J. Liu, M. Batistuta, Nein-Po Chen, B. L. Walsh, R. P. Andres, E. -H. Chen, M. R. Melloch, J. M. Woodall, and R. Reifenberger. "Self-assembly metal/molecule/semiconductor nanostructure for electronic device and contact applications." *J. Electronic Materials*, vol. 29 (5), pp. 565-569, May 2000.

[4] K. Yamada, K. Hoshino, K. Matsumoto and I. Shimoyama, "Electro-static trapping and deposition of nanoparticles in a submicron narrow gap for a laterial-electrode LED," *17th IEEE conference on MEMS*, pp. 49-52, 2004.

[5] L. L. Kazmerski, "Solar photovoltaics R&D at the tipping point: A 2005 technology verview," *Journal of Electron Spectroscopy and Related Phenomena*, vol. 150, pp. 105-135, 2006.

[6] B. O'Regan and M. Gratzel, "A low-cost, high efficiency solar cell based on dye-sensitized colloidal TiO_2 films," *Nature*, vol.353, pp. 737-740, Oct. 24 1991.

[7] J. S. Salafsky, "A channel design using single, semiconductor nanocrystals for efficient (opto)electronic devices," *Solid-State Electronics*, vol. 45, pp. 53-58, Jan. 2001.

[8] I. Robel, V. Subramanian, M. Kuno and P. V. Kamat, "Quantum Dot Solar Cells. Harvesting Light Energy with CdSe Nanocrystals Molecularly Linked to Mesoscopic TiO_2 Films," *J. Am. Chem. Soc.,* vol. 128 (7), pp. 2385-2393, 2006.

[9] I. Gur, N. A. Fromer, M. L. Geier and A. P. Alivisatos, "Air-stable all-inorganic nanocrystal solar cells processed from solution." *Science,* vol. 310, pp. 462-465, October 2005.

[10] C. C. Tu, Y. K. Li, T. M. Chen and C. Y. Wu, *Fellow, IEEE,* "Design and Fabrication of a photosensing nanodevice structure with CdSe and Au nanoparticles on a silicon chip," *IEEE Trans. Nanotechnology,* vol. 5, no. 3, pp. 284-290, 2006.

[11] T. W. Liao, "The research of advanced nanodevice structure for photo-sensing and solar cell application," *institute of electronics engineering*, *National Chiao Tung University*, master thesis, 2007.

[12] J. J. Storhoff, R. Elghanian, R. C. Mucic, C. A. Mirkin and R. L. Letsinger, "One-Pot colorimetric differential of polynucleotides with single base imperfections using gold nanoparticles Probes," *J. Am. Chem. Soc.*, vol. 120, pp. 1959-1964, 1997.

[13] L. M. Liz-Marzan, "Nanometals: Formation and color," *Materials Today*, vol. 7, issue 2, pp. 26-31, Feb. 2004.

[14] M. C. Beard, G. M. Turner, C. A. Schmuttenmaer, "Size-dependent photoconductivity in CdSe nanoparticles as measured by time-resolved terahertz spectroscopy," *Nano Lett.*, vol. 2, pp. 983-987, 2002.

[15] A. P. Alivisatos, "perspectives on the physical chemistry of semiconductor nanocrystals," *J. Phys. Chem.,* vol. 100, pp.13226-13239, 1996.

[16] C. Y. Wu, Y. K. Li, C. C. Tu, "A new photo-sensing nano-device structure with CdSe and Au nanoparticles on silicon substrate," *3rd IEEE Conference on Nanotechnology*, vol. 2, pp. 763-765, 2003.

[17] C Burda, T. C. Green, S. Link and M. A. El-Sayed, "Electron shuttling across the interface of CdSe nanoparticles monitored by femtosecond laser spectroscopy," *J. Phys. Chem. B.,* vol. 103, pp. 1783-1788, 1998.

[18] J. Zheng, Z. Zhu, H. Chen and Z. Liu, “Nanopatterned assembling of colloidal gold nanoparticles on silicon,” *Langmuir*, vol. 16, pp. 4409-4412, 2000.

[19] C. Y. Chang, “Advanced nanodevice structures with CdSe/ZnS and/or Au nanoparticles for photo-sensing applications,” *institute of electronics engineering*, *National Chiao Tung University*, master thesis, 2006.

[20] G. A. Rincon-Mora and P. E. Allen, “A low-voltage, low quiescent current, low drop-out regulator,” *IEEE J. Solid-State Circuits*, vol. 33, pp. 36–44, Jan. 1998.

[21] K. N. Leung and K. T. Mok, “A sub-1-V 15-ppm/°C CMOS bandgap reference without requiring low threshold voltage device,” *IEEE J. Solid-State Circuit*, vol. 37, pp. 526–529, April 2002

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