國立交通大學

電子工程學系 電子研究所

博 士 論 文

介面保護與雷射退火增進高效能 N 型鍺電晶體之研究

The Research of High Performance Ge nMOSFET
Improved by Interface Passivation and Laser Annealing

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中 華 民 國 九 十 九 年 十 月

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A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

Oct. 2010
Hsinchu, Taiwan, Republic of China

中華民國九十九年十月

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摘要

隨著半導體元件尺寸的不斷縮微，並且符合目前邏輯電路與高效能場效電晶體的發展，高效能的金氧半互補式場效電晶體 (CMOSFET) 的研發是勢在必行的。當以矽 (Si) 為基板與二氧化矽（SiO_2) 為介電材料的半導體元件發展到一個瓶頸時，為了符合未來尺寸的微縮與高效能電晶體與的趨勢，高介電系數材料與高載子遷移率材料的開發似乎是不二法門。但增加介電常數和減少元件厚度所伴隨而來的高漏電與如何整合這些高介電材料在新基板更是目前研究的主要議題。而目前許多高介電材料如 HfO_2、 Al_2O_3、 La_2O_3、 TiO_2 等都被廣泛的研究。除此之外，一些高電子遷移率的基板，如矽鍺 (SiGe)、鍺 (Ge) 與砷化鎵 (GaAs) 等，再近幾年也都陸陸續續被提出一些相關的研究文件，然而如何成功的整合這些新材料與新基板應用於大型積體電路上依然是一個困難的課題。

因此，我們針對新材料與基板所產生的問題，開發出一系列和氧化鑭相關(La_2O_3-based)的高介電材料，其中包括了鑭化鋁氧化物($LaAlO_3$)、鑭化鈦氧化物(TiLaO)和二氧化鋯(ZrO_2)。除此之外，我們也成功的研究出整合介面工程(Interface engineering) 與高介電材料的方法，成功的運用在鍺基板與高介電材料

之間沈積一層很薄的二氧化矽保護層來做出高性能的 N 型鍺互補式金氧半場效電晶體 (Ge nMOSFET)，不但在漏電上有大幅的降低，更改善了鍺基板介面的一些平帶電壓(Flatband Voltage)的不理想效應，大大的增進了電容密度，使等效氧化曾厚度(EOT)在鍺基板可以微縮到 0.85 奈米 並且得到了高的電子遷移率。最後，由於前面成功的實驗，我們再加以運用雷射退火(Laser Annealing)的方式，使電晶體的特性更進一步的改善。

The Research of High Performance Ge nMOSFET Improved by Interface Passivation and Laser Annealing

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Abstract

The development of the high performance complementally metal-oxide-semiconductor field effect transistors (CMOSFET) is expected to be imperative as the semiconductor devices continuously decrease in size along with the development of current logical circuits and high performance MOSFET. However, the size reduction of the Si-substrate and silicon dioxide (SiO_2)-dielectric-material-based semiconductor devices has come to a bottleneck due to their low carrier mobility and the lower dielectric permittivity constants (κ =3.9), hence the development of materials with higher dielectric constant materials and higher carrier mobility is unavoidable.

The high leakage currents accompanying the reduction of the thickness of the devices and the increase in the dielectric constants, and the integration of these high dielectric constant materials onto the new substrates have been the main subjects of

the recent studies. The researches of high dielectric constant materials, such as HfO_2, Al_2O_3, La_2O_3, and TiO_2 have been studied for decades. Furthermore, high carrier mobility substrates, such as SiGe, Ge, and III-V compounds (GaAs), have been widely proposed in some recent research articles. Nevertheless, successful integration of high dielectric constant materials onto new substrates for the VLSI technology still proves to be quite a difficult issue.

In order to overcome the problems of integrating the new high dielectric constant materials and the substrates, we used a series of Lanthanum Oxide (La_2O_3)-based high-κ materials such as $LaAlO_3$, TiLaO and ZrO_2. We had also studied the interface engineering and successfully fabricated high performance Ge nMOSFET by depositing an ultra thin SiO_2 passivation layer between the Ge substrates and the high dielectric materials. Using the interface passivation not only reduces the electric leakages, but also improves the unwanted flat-band voltage (V_{fb}) shifts on the Ge substrates as well as the capacitance density, enabling the equivalent oxide thickness (EOT) to scale down to 0.85 nm with higher carrier mobility. Finally, we used the laser annealing (LA) method to further improve the transistor characteristics of the gate stack structures.

Acknowledgements

首先我要感謝我的指導教授荊鳳德教授，我才能順利的完成此博士論文。在荊教授耐心的教導之下，學到了許多實驗的研究方法，遇到問題學會去思考並且尋求解決之道，以及待人處世應有的腳踏實地與務實的態度，讓我博士班生涯受益良多。

再來我要感謝淳護、迺超和明峰等學長的指導和思麟同學的相互鼓勵，還有竣揚、坤億、博璿、柏君、智偉、阿爆、和佳芸各位學弟妹在實驗上熱情的幫忙與給我意見，讓我可以更有信心並且順利的完成我的實驗。由於也因有為你們這群好學長、好同學與好學弟妹讓我4年的碩博士班生涯過的很充實也很有意義，也希望你們未來的實驗都很順利。同時也感謝Joyce Chiang英文撰寫的幫忙。

我也由衷感謝交通大學奈米中心與國家實驗研究院-國家奈米元件實驗室，能讓我有完善的儀器設備與環境來達成我的實驗。

最後我要對我親愛的父母親以及大姊莉玲，大哥維新以及盈燕一路無悔的支持我念完博士班致上最高的感謝，並且支持我所做的一切，讓我可以全心全力無後顧之憂的朝自己的夢想努力與邁進。

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Chapter 5 High Field Mobility Metal-Gate/high-κ Ge *n*-MOSFETs

Chapter 1

Introduction

1.1. Motivation of High-κ Dielectrics

The scaling down of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFETs) using metal gate with high κ has been the major way to improve the performance of integrated circuits in the last few decades. Si dioxide (SiO_2) as a gate dielectric offers some merits in CMOS processing including a thermodynamically and electrically stable, high-quality Si–SiO_2 interface as well as superior electrical isolation properties. In order to scale down the MOSFETs, reducing the thickness of gate dielectric becomes the trend for the state-of-the-art devices. However, the direct tunneling of gate leakage at 2V bias exceeds 1A/cm^2 below the 2.0 nm thickness of SiO_2 (Fig.1-1) which becomes the critical issue for CMOS scaling down [1-1].

From the below electrical fundamental equation, we can solve the obstacle by using the materials with high dielectric constant (high-κ):

$$C = \frac{\kappa \varepsilon_0 A}{t} \quad (1)$$

Where ε_o (8.85x10^{-14} f/cm^2) is the permittivity of free space, κ is the dielectric constant (also referred to relative permittivity in this article), *A* is the area of capacitor, and *t* is the oxide thickness. The physical thickness of the dielectric in the devices can

be increased without the reduction of capacitance density if using the higher dielectric constant material. Higher *C* value enables the MOS structure to gain more inversion carriers and reaches the higher drive current of MOSFETs. In the other hand to increase the *C*, we can reduce the overall *t* thickness. The components of *t* can be represented as the following equation,

$$t = t_{qm} + t_{ox} + t_{poly\text{-}si} \quad (2)$$

where $t_{poly\text{-}si}$ is from the poly-Si depletion, t_{ox} is the equivalent oxide thickness (EOT) of the dielectric and t_{qm} is the quantum effect of carriers in the channel. t_{qm} is the intrinsic physic quantum effect and is not avoidable. We can reduce t_{ox} and $t_{poly\text{-}Si}$ to increase the capacitance density. Using metal gates to replace the poly-Si gate have been proposed to solve the issue in recent years. Reducing the EOT becomes the most important way to reach higher *C*. The EOT of materials is defined as the thickness of SiO_2 required to reach the same capacitance. EOT can be written as an equation,

$$\mathbf{EOT} = t_{high-k\ dielectric} \times \frac{K_{SiO_2}}{K_{high-k\ dielectric}} \quad (3)$$

where $t_{high\text{-}\kappa\ dielectric}$ and $\kappa_{high\text{-}\kappa\ dielectric}$ are the high κ material of physical thickness and relative dielectric constant, respectively.

According to the ITRS (*International Technology Roadmap for Semiconductor*) shown in Fig. 1.2, the EOT for metal gate has to be below 10 Å after 2010. Therefore, the continual scaling down of gate dielectric becomes an inevitable trend in CMOS

technology.

Although a lot of researches of high dielectric constant materials have been reported, we still need to understand before these materials can be adopted by industry. There are some key points listing below [1-2].

- **Permittivity**

  The relative dielectric constant of the new material should be between 10 and 30. Higher κ dielectric materials will give rise to fringe fields from the gate to the drain or source and it will degrade the short channel device performance.

- **Band gap**

  The band gap of new dielectric materials must be greater than 5 eV and the band offsets with silicon must be sufficient. Generally, Fig. 1.3 shows the higher κ value materials will have a smaller band gap, and there is an inverse relationship between band gap and dielectric constant. Fig.1.4 shows that increasing dielectric constant will cause lower conduction band and valence band when in contact with silicon. In order to reduce the leakage current from each band, the barrier height must be bigger than 1 eV.

- **Thermodynamic stability**

  Good thermodynamic stability is required for new high dielectric materials to directly contact with silicon for the fabrication of advanced CMOS devices.

High-κ dielectric materials must have a large Gibbs free energy to prevent interaction with silicon, and the diffusion coefficient of materials must be low with less interface reaction.

- **Interface quality**

  The interface between high dielectric material and silicon is also an important issue. Interface states will cause flat-band voltage shift and degrade the mobility of MOSFETs. Low interface trap defect density, D_{it}, should be lower than 10^{11} cm^{-1} eV^{-1}.

- **Compatibility with the current or expected materials to be used for CMOS devices**

  Therefore, alternate high κ dielectric materials such as Si_3N_4 (κ = 7.5), $Si_xO_yN_z$ (κ = 3.9-7.5), Al_2O_3 (κ = 10), HfO_2 (κ = 26), La_2O_3 (κ = 30), Ta_2O_5 (κ = 25), TiO_2 (κ = 50), and ZrO_2 (κ = 25) [1-3]-[1-8], or other dopant metal oxides have been proposed to replace SiO_2 for gate dielectric materials in the recent researches. Fig. 1-5 shows the bond enthalpies for various metal/dielectric combinations. High dielectric constant materials have higher bond enthalpies, which can prevent higher leakage currents and degradations after high temperature processes. In general, the metal oxides exhibit strong bond enthalpies than other compounds.

  However, some of these materials are not all suitable for compatibility of

CMOS devices. Such as, Al_2O_3, is not thermodynamically stable in direct contact with Si with a lower dielectric constant and Ta_2O_5 has a smaller conduction band offset with silicon (ΔE_c~0.3 eV) that will cause the increasing leakage currents from electron tunneling.

In this study, we used different high k dielectric $LaAlO_3$ (LAO) and TiLaO for gate dielectrics for comparisons. As we know, La_2O_3 has a high k value (k ~30) and the negative flat-band voltage for nMOSFETs [1-9]. However, La_2O_3 easily absorbed water vapor from air and results in an uncontrolled reaction [1-10]. Moreover, the band gap of La_2O_3 is relatively small (4.3 eV) and the structure transition from the amorphous to crystalline phase occurs at a lower temperature than that of Al_2O_3 [1-11] which induces large leakage current from the grain boundary after high thermal budget. Lanthanum aluminate $LaAlO_3$ (LAO), as a compound of La_2O_3 and Al_2O_3, has a reasonably larger κ value of 25, band-gap of over 5 eV, high thermal stability up to 2100^{o}C. It presents the chemical and dielectric properties of La_2O_3 and Al_2O_3 and overcome the obstacles of individual materials [1-12]-[1-14].

On other hand, although TiO_2 has a high dielectric constant value of 86, it is easily to form anatase phase at the temperature of 400^{o}C with high leakage current and low bandgap (3.5 eV) for amorphous film [1-15]. Besides, the smaller conduction band offset is also the concerned for alternative gate dielectric. In this research, using

the La_2O_3 dopant into TiO_2 with a κ value of 45 and maintains the high permittivity constant of TiO_2 and negative flat-band voltage from La_2O_3 [1-16]. We will focus on the Lanthanum (La) based high κ dielectric for advanced gate stacks application with alternative channel material in this thesis.

1.2. Overview of Metal Gate Electrode

As complementally metal oxide semiconductor field effect transistors (CMOSFETs) scaling down to 100 nm technology node or beyond, the conventional poly-Si gate electrode has concerned due to following issues [1-17]:

- **Poly-Si depletion effects.**
- **Boron penetration effects.**
- **High sheet resistance.**

An obvious way to alleviate the problems of poly-Si is to use metal or metal nitride gates. The requirement of the new technology metal gates should suit for the follows:

- **Favorable work functions (Φ_m) [candidate metals need to have vacuum work-functions smaller (larger) than 4.05 V (5.17 V) for the NMOS (PMOS)]** [1-16]**.**
- **Low sheet resistance.**
- **Thermal stability**

- **Compatibility with high-κ dielectric and integration with VLSI technology.**

In selecting metal-gate materials for device integration, the metal work function (Φ_m) is an important consideration since it directly affects the threshold voltage and the performance of a transistor. Using TaN for gate electrode has been widely studied for recently years. It shows promising results as gate electrodes for high-κ gate dielectrics in terms of thermal stability and compatibility with the high-*k* gate dielectrics. Besides, there is a significant variance in reported work-function from 4.13 eV (close to n^+ poly-Si) to 5.05 ev (close to p^+ poly-Si) [1-17]-[1-18]. Causing these large discrepancies are due to different deposition methods, different nitrogen ratios and post metal deposition annealing (PMA). In this article, we used the TaN for integration of metal gates / high-κ to study the characteristics of MOSFETs.

1.3. The Challenge of Ge n-type MOSFETs

As we knew, carrier mobility is an important issue for high performance devices. Many studies of strained-Si had been proposed to enhance the mobility of devices. Germanium as channel is attractive because of its significant enhancement in bulk mobility relative to Si. It can enhance the electron mobility (2X) and hole mobilities (4X) higher than Si. Besides, the Ge has ~50X higher density of state than InGaAs to deliver high transistor current. Although the III-V compounds show the higher electron mobility than Ge, the lower hole mobility and lager interface states are the

obstacles which degrade the MOSFET performance and cannot meet the trend for ITRS. The comparisons of Si, Ge and GaAs are listed in the Table 1 [1-19]. Therefore, several successful demonstrations of high κ materials gate stacks on Ge have been reported recently [1-20]-[1-25]. However, there are still some problems on Ge substrates for the MOSFET fabrication needed to be solved and listed below [1-25]:

(a) Germanium oxide (GeO_x $x < 2$) is thermal unstable and water soluble.

(b) Large off state leakage currents due to small bandgap (0.66 eV).

(c) The poor interface between Ge and high-κ dielectric materials.

(d) Activation is insufficient for source/drain and the low contact resistivity is hard to form for Ge nMOSFETs.

Therefore, reduction of interface reaction between Ge and high-κ dielectric material to form GeO_x is becoming a critical issue. There are some reports demonstrate the Ge surface passivation to suppress the unstable GeO_x formation during high-κ deposition. Surface nitridation using NH_3 for Ge passivating had been studied [1-26]. However, the nitrogen involvement caused the degradation of mobility. Using a thin Si passivation layer on Ge also had been proposed to solve the interface states [1-27]. Unfortunately, the Si layer is not easily to control during the process thermal budget and causes the equivalent oxide thickness (EOT) degradation. Using the thick high quality Ge negative oxide (GeO_2) or high pressure GeO_2 for gate stacks

are also alternative ways for the solution [1-28]-[1-29]. Such reports have been successfully proposed the high performance devices and show the high low-field mobilities. However, the degradation of EOT is still the issue for Ge technology. As mention above, another obstacle for Ge MOSFET is about the dopant activation of source/drain junction. As we knew, the boron activation using conventional rapid thermal annealing (RTA) is at a low 400^{o}C temperature. However, the higher activation temperature is needed ($\geq$600^{o}C) for phosphorus or arsenic [1-30]. Such high temperature not only caused the unwanted interface reaction but also degrade the device performance. Besides, the insufficient n type dopant activation by using RTA had also been reported [1-31]. Furthermore, the diffusion coefficient for the n-type dopant (phosphorus or arsenic) is faster than the p-type dopant (boron) [1-30]. Therefore, it is hard for n type dopants to form the shallow junction with a low sheet resistance by RTA [1-31]. In order to increase the efficiency of dopant activation, the method of using Excimer laser annealing (LA) had been demonstrated successfully to enhance the source/drain complete activation [1-32]-[1-33]. We had demonstrated the LA for S/D junction activation. Furthermore, the LA also was applied for increasing the κ value for gate stacks due to crystallization-induced.

1.4. Dissertation Organization

The dissertation is organized as followed:

In chapter 2, we discussed the n MOSFET for depositing the high-κ dielectric $LaAlO_3$ for the gate material without passivation layer on Ge channel. Although it was successful for surface passivation for Ge channel MOSFET, the EOT degraded.

In order to further scale down the EOT for Ge channel MOSFET, we used the TiLaO higher κ material and SiO_2 interfacial layer for surface passivation. These not only improved the interface but also reached the same mobility. Therefore, we discussed the effect of SiO_2 passivation layer and less flat-band (V_{fb}) shift in chapter 3 and the performance of Ge n channel MOSFET in chapter 4.

However, the mobility was still not high for strained-Ge. In chapter 5 and chapter 6, we used the La_2O_3 with SiO_2 for gate stacks on Ge substrate by conventional RTA and laser annealing (LA) for source and drain activation.

Finally, we used the $ZrO_2/La_2O_3/SiO_2$ on Ge substrate for further EOT scaling down by LA in chapter 7. The LA was applied on gate stacks for increasing the capacitance density due to the crystallization-induced and the efficient activation for source/drain.

A summary of these experiments is given in chapter 8.

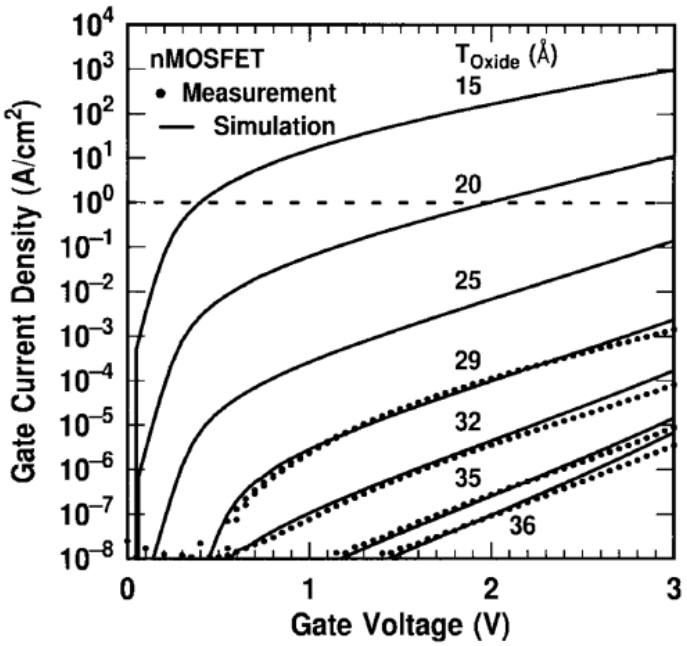


Fig. 1.1 Leakage current versus voltage for various thicknesses of SiO_2 layers.

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
Surface control limits for trace metals for bulk silicon and SOI top silicon layer. FEP Table 68 Critical GOI metals (concentration in atoms/cm2)	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}
EOT (Extended planar bulk) for High Performance MPU/ASIC for 1.5E20 doped Poly-Si [FEP Table 69]	1.1	0.5					
EOT (Extended planar bulk) for High Performance MPU/ASIC for 1.0 E20 doped Poly-Si [FEP Table 69]	1.1	1	1				
EOT (FDSOI) High Performance MPU/ASIC for metal gate [FEP Table 69]				0.7	0.6	0.55	0.5
EOT (FDSOI) High Performance MPU/ASIC for metal gate [FEP Table 69]							0.7
EOT (multi-gate) High Performance MPU/ASIC for metal gate [FEP Table 69]					0.8	0.7	0.6
EOT (multi-gate) High Performance MPU/ASIC for metal gate [FEP Table 69]							
Low operating power EOT (bulk) for 1.5E20 doped poly-Si [FEP Table 69]	1.2	0.8	0.7	0.6	0.5	0.5	

Fig. 1.2 *International Technology Roadmap for Semiconductor* (ITRS), [Online] Available: http://public.itrs.nrt/

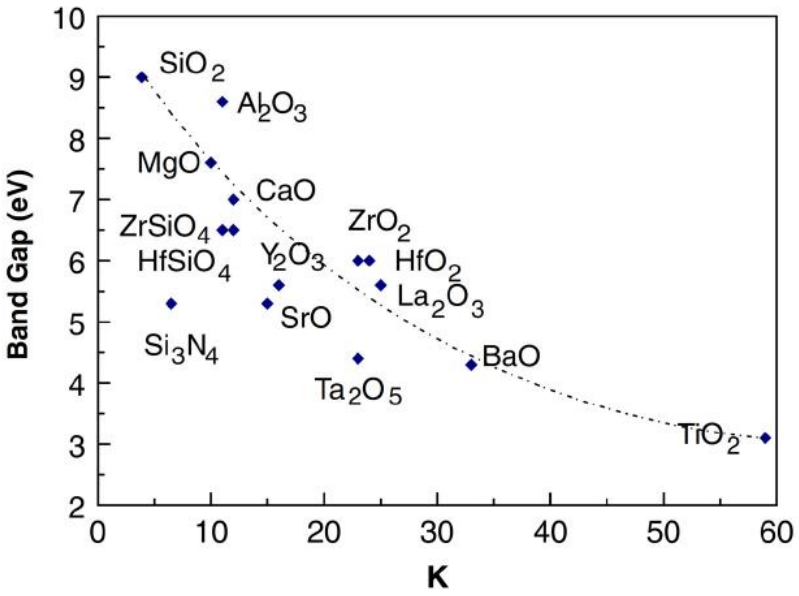


Fig. 1.3 Static dielectric constant versus band gap for candidate gate oxides [1-34].

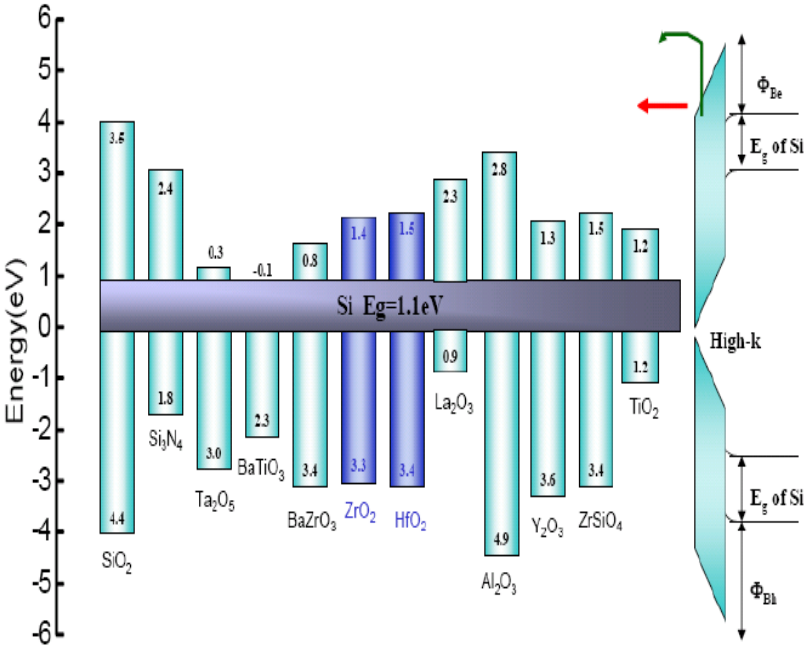


Fig. 1.4 The band offset of popular high-κ materials.

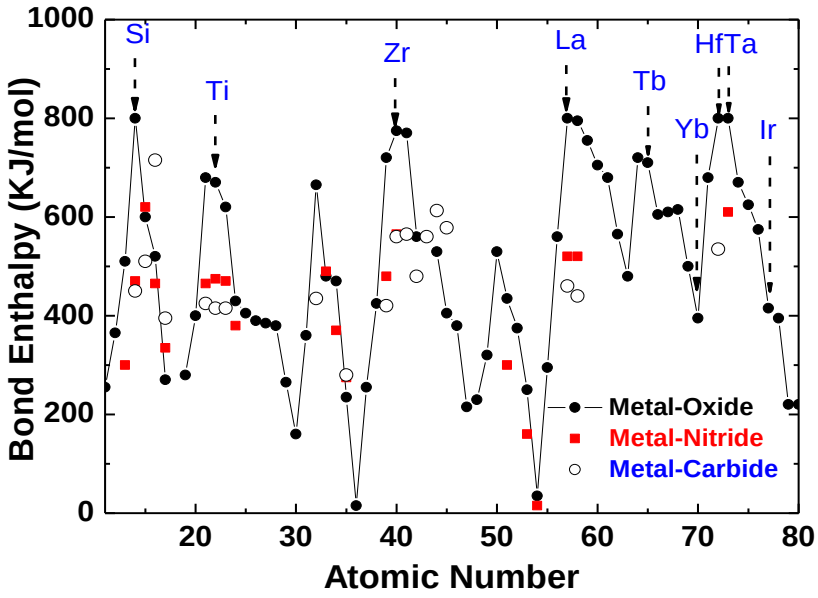


Fig. 1.5 Bond enthalpy for M-O, M-N and M-C in the Periodic Table.

	Si	Ge	GaAs
Dielectric constant (κ)	**11.9**	**16**	**13.1**
Band gap (eV)	**1.12**	**0.66**	**1.42**
Hole mobility (cm^2/Vs)	**480**	**1900**	**400**
Electron mobility(cm^2/Vs)	**1350**	**3900**	**8500**
Density of states in valence band (cm^{-3})	**1.04×10^{19}**	**6.0×10^{18}**	**7.0×10^{18}**
Density of states in conduction band (cm^{-3})	**2.8×10^{19}**	**1.04×10^{19}**	**4.7×10^{17}**

Table 1-1 Comparisons of Si, Ge and GaAs [1-19].

Chapter 2
High Performance Gate-First Epitaxial Ge n-MOSFETs on Si with $LaAlO_3$ Gate Dielectrics

2.1. Introduction

New channel materials with higher mobility are required to improve the performance of strained Si MOSFETs. The small band-gap (E_G) Ge [2-1]-[2-24] had a higher electron and hole mobility than Si, and ~50 times higher density of state than InGaAs for higher current. However, overcoming the large transistor leakage current in small E_G Ge and low electron mobility at high effective electric field (E_{eff}) were major challenges. The leakage current of small E_G Ge MOSFETs could be lowered by decreasing the Ge body thickness in a Ge-on-insulator (GOI) structure [2-1], [2-9] or using thin-body epitaxial Ge on Si [2-21]-[2-22]. Mobility, higher than that of Si universal mobility has been reported recently, at large equivalent-oxide thickness (EOT) [2-18]-[2-20]. Nevertheless, achieving good electron mobility in small EOT was still a challenging issue especially at high E_{eff}. Such high-field operations were unavoidable for 45~32 nm CMOS nodes with highly scaled 1 nm EOT. Several interface passivation methods have been used to improve mobility [2-6], [2-10], [2-12], [2-21]-[2-22]. However, these interface treatments resulted in an extra interfacial layer on Ge that degrades the important EOT and limits EOT down-scaling.

This paper reported good high-field mobility of Ge n-MOSFETs without using interfacial layer. This was achieved in *gate-first* metal-gate/high-κ/Ge/Si n-MOSFETs with $LaAlO_3$ dielectric [2-25]-[2-27]; high electron mobility of 218 cm^2/V-s at 0.5 MV/cm E_{eff}, very low transistor off-state leakage (I_{OFF}) of 7×10^{-10} A/μm, small sub-threshold swing (*SS*) of 108 mV/dec and a small EOT of 1.6 nm were reached simultaneously. Here the $LaAlO_3$ was formed by mixing Al_2O_3 and La_2O_3 that that have been used widely to form the Al_2O_3/HfSiO(N) and La_2O_3/HfSiO(N) gate dielectrics for low-V_t *gate-first* high-κ/Si p- and n-MOSFETs used for 32~28 nm nodes. Such good *SS* and high-field mobility were even better than those using a SiO_2 interfacial layer [2-22] that had one of the best reported results of *gate-first* Ge n-MOSFETs [2-1]-[2-24]. In sharp contrast, much higher gate leakage current at larger EOT was measured using HfAlO dielectric [29]-[30] that indicating how important it was to choose high-κ gate dielectric for Ge n-MOSFET.

2.2. Experimental procedure

This study used 6-inch p-type Si wafers (5×10^{15} cm^{-3} doping) in these experiments. After RCA cleaning, the 200 nm undoped Si buffer and 6 nm Ge were epitaxially grown on Si substrate by ultra-high vacuum chemical-vapor-deposition (UHVCVD) at 500°C [2-21]-[2-22]. After dipping in dilute HF, a 5 nm thick $LaAlO_3$ [2-25]-[2-27] was deposited by sputtering and followed by a 400°C post-deposition anneal (PDA) in an oxygen ambient for 5 min. A 200 nm TaN was deposited by

sputtering and patterned to form the metal gate. High-κ HfAlO capacitors were fabricated [2-29]-[2-30], for comparison. After gate patterning, the n^+ source-drain regions were formed by using a 25 KeV As^+ implant at a dosage of 5×10^{15} cm^{-2} and a 550^{o}C RTA activation for 30 sec. Such a low temperature RTA ensured the epitaxial Ge on Si substrate under pseudomorphic conditions with a smooth surface and reduced generation of dislocations. Finally, Al contact metal was added on the source-drain. The fabricated devices were characterized by capacitance-voltage (*C-V)* and current-voltage (*I-V)* measurements using an HP4284A precision LCR meter and HP4156C semiconductor parameter analyzer.

2.3. Results and discussion

Fig. 2.1 (a) shows *C-V* characteristics of TaN/HfAlO/Ge/Si and control TaN/HfAlO/Si n-MOS capacitors after different RTA temperatures. Compared with control device on Si, the HfAlO dielectric on Ge had a lower capacitance density and lower unwanted flat-band voltage (V_{fb}) shift of ~0.7 V even at a low temperature 450^{o}C RTA. Increasing the RTA temperature to 550^{o}C led to severe *C-V* distortion by high density interface states and was accompanied by a greater V_{fb} shift. However, such annealing temperature was required for doping activation at the ion-implanted source-drain. The severe V_{fb} shift and interface trap generation at only 550^{o}C were related to the strong interface reaction shown in the cross-sectional TEM of following sections. Fig. 2.1 (b) showed the TaN/$LaAlO_3$/Ge/Si n-MOS capacitors after different

RTA temperatures. The negative V_{fb} is the unique characteristics of La_2O_3-containing high-κ gate dielectric [2-31]-[2-32]. Although similar V_{fb} shift and slightly lowered capacitance density were detected in TaN/$LaAlO_3$/Ge/Si n-MOS capacitors, the *C*-*V* distortion and V_{fb} value were significantly better than TaN/HfAlO/Ge/Si device. An EOT of 1.6 nm was obtained from Quantum-Mechanical (QM) *C*-*V* simulation with Ge parameters [2-22].

Fig. 2.2 shows the measured gate dielectric leakage current of TaN/$LaAlO_3$/Ge/Si and TaN/HfAlO/Ge/Si capacitors. A leakage current of 6×10^{-4} A/cm^2 at -1 V was reached for TaN/$LaAlO_3$/Ge/Si capacitor with a small 1.6 nm EOT that was 67 times lower than that of TaN/HfAlO/Ge/Si capacitor after the same 550^{o}C RTA with a larger 2.6 nm EOT. The poor current leakage with HfAlO gate dielectric was related to the much-degraded interface property by large EOT and V_{fb} shift as shown in Fig. 2.1(a). Although detailed mechanism is still under investigation, such degradation may have been related to the interface reaction of GeO_2 with HfO_2 to form volatile GeO [2-23]-[2-24] and charged oxygen-deficient GeO_x. This in turn generated interface charge [2-31], increased the Ge diffusion into HfO_2 and roughened the interface [2-23]-[2-24]. The poor interface and gate dielectric quality also degraded the leakage current of the gate capacitor. Fig. 2.2(b) shows the leakage current as a function of EOT, for TaN/$LaAlO_3$/Ge/Si capacitors with smaller EOT

down to 1.05 nm. The extrapolated leakage current at 1.0 nm EOT was >3 orders of magnitude lower than that of SiO_2. This permitted the addition of interfacial GeO_2 or SiO(N) [33] to reduce the remote phonon scattering from high-κ gate dielectric, similar to Intel's device [2-34].

To grasp the large differences between capacitor using $LaAlO_3$ and HfAlO gate dielectrics on Ge/Si, these high-κ capacitors were examined by cross-sectional TEM. Figs. 2.3(a), 2.3(b) and 2.3(c) show cross-sectional TEM images of TaN/HfAlO/Ge/Si, control TaN/HfAlO/Si and TaN/$LaAlO_3$/Ge/Si capacitors after the same 550^{o}C RTA, respectively. The HfAlO on Ge/Si had a thicker high-κ layer than HfAlO on Si, deposited side-by-side after the 550^{o}C RTA, suggesting a strong interface reaction or Ge out-diffusion between HfAlO and Ge/Si [2-23]-[2-24]. The thicker interfacial layer formed on Ge/Si than Si was not due to the oxygen diffusion since the same HfAlO gate dielectric was used and deposited side-by-side on Ge/Si and Si. The Ge out-diffusion [2-21] may have been due to the lower melting point of Ge than Si that, in turn, scaled with cohesive energy (372 kJ/mol for Ge and 446 kJ/mol for Si) to separate a single atom from the crystal lattice. However, the $LaAlO_3$ on Ge/Si showed very close high-κ thickness with the control HfAlO on Si, although a very thin interfacial layer was formed. This was consistent with the much smaller EOT and higher capacitance density than HfAlO on Ge. Since the only difference between

these two high-κ dielectrics was the addition of La_2O_3 or HfO_2, this suggested a stronger reaction between HfO_2 and Ge to enhance interface reaction or Ge out-diffusion. Although no data of Hf-Ge or germanide formation could be available in the literature, the bond enthalpy to group-IV Carbon was significantly higher for Hf-C (540 kJ/mol) than for La-C (462 kJ/mol). The formed interfacial layer of $LaAlO_3$ on Ge/Si explained the V_{fb} shift after a higher 550°C RTA temperature that was also found in high-κ/Si after RTA [2-31].

Based on the largely improved high-κ dielectric property, we fabricated the Ge n-MOSFETs using $LaAlO_3$ gate dielectric. Figs. 2.4(a) and 2.4(b) present the I_d-V_d and I_d-V_g characteristics, respectively. Small sub-threshold swing (*SS*) of 108 mV/dec and very low I_{OFF} of 7×10^{-10} A/μm were measured. This small I_{OFF} leakage and good *SS* were vital for small E_G and high mobility new channel MOSFET used for low power Green Transistor application. Further improving I_{ON}/I_{OFF} may be reached by chemical interface passivation using H, S, or Se. It is noticed that the *SS* was one of the best-reported data for *gate-first* Ge n-MOSFET [2-1]-[2-24] that was even better than the TaN/TiLaO/SiO_2/Ge/Si n-MOSFET using SiO_2 interfacial layer at a smaller EOT of 0.81 nm. Here the *SS* is expressed as [2-32]:

$$SS = \frac{KT}{q} \times \ln 10 \times (1 + \frac{C_{dep} + C_{it}}{C_i}) \quad (1)$$

where C_{dep} was the depletion capacitance density, C_{it} was the capacitance density from charged interface traps and C_i was the gate capacitance density. The improved *SS* at larger EOT was an indication of improved interface properties of $LaAlO_3$ gate dielectric on Ge/Si compared with previous $TiLaO/SiO_2$ with an ultra-thin SiO_2 interfacial layer on Ge/Si [2-22].

Fig. 2.5 shows mobility as a function of E_{eff}. The mobility was calculated directly from the I_d-V_g curves [35]. For comparison, the mobility data from related literatures were also plotted [2-10], [2-13]-[2-14], [2-22]. The lower peak mobility could be attributed to the remote phonon scattering in the high-κ dielectric that was also found in high-κ/Si MOSFET. Therefore, an ultra-thin SiO(N) [2-33] or GeO_2 [2-14]-[2-17], [2-19]-[2-20] interfacial layer was needed to further improve the peak mobility and I_{ON}/I_{OFF}. Although higher peak mobility values were published [2-10], [2-13]-[2-14], the mobility decreased rapidly with an increase in E_{eff} due to the interface scattering. However, the MOSFET was destined to operate at high E_{eff} due to the small 1 nm EOT used for 45~32 nm nodes [2-34]. In sharp contrast, the Ge n-MOSFET using $LaAlO_3$ showed the superior high field mobility of 218 cm^2/Vs at 0.5 MV/cm that was one of the best reported high-field mobility data for *gate-first* Ge n-MOSFETs [2-1]-[2-24].

Fig. 2.6 shows the reliability of TaN/$LaAlO_3$/Ge/Si n-MOSFETs under

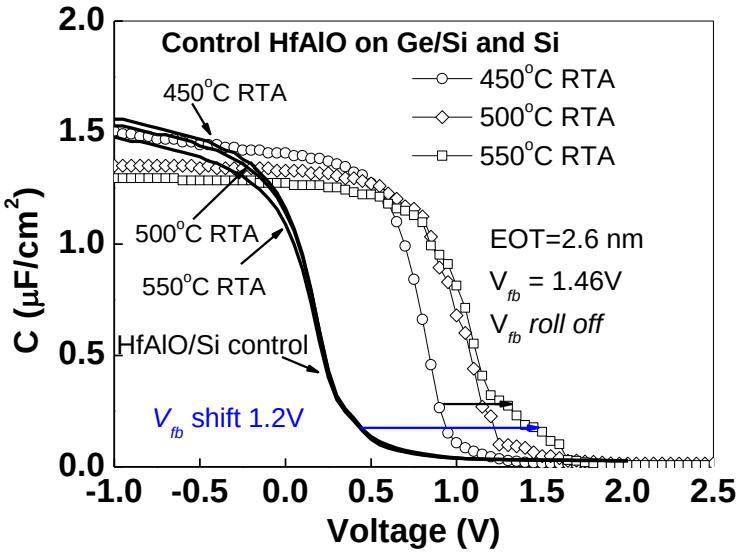
bias-temperature instability (BTI) testing. A small threshold-voltage shift (ΔV_t) of 31 mV was measured at a 1.2 V gate overdrive (V_g-V_t) and 85°C for 1 hr. Table 1 summarizes and compares the important device parameters of metal-gate/high-κ Ge n-MOSFETs [2-10], [2-13]-[2-14], [2-17]-[2-20], [2-22]. The TaN/$LaAlO_3$/Ge/Si n-MOSFET had superior high-field mobility of 218 cm^2/Vs at 0.5 MV/cm, record low *SS* of 108 mV/dec, small 1.6 nm EOT, very low I_{OFF} of 7×10^{-10} A/μm, simple *gate-first* process and useful for 12-in integration.

2.4. Conclusion

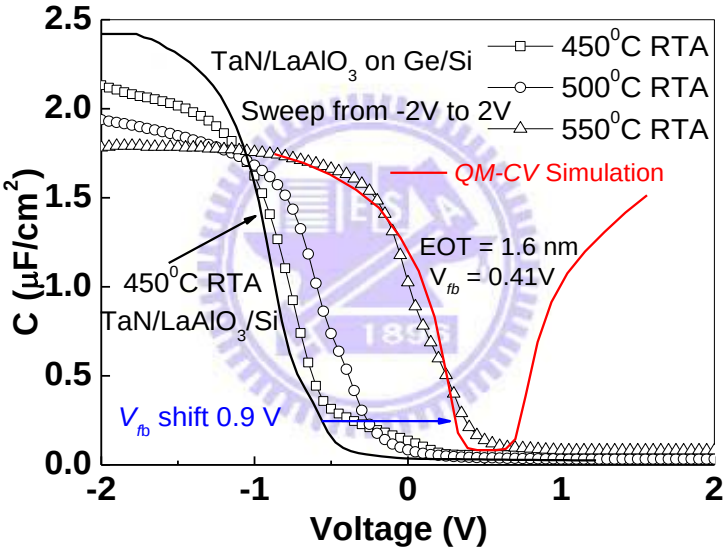
This study has demonstrated a high performance *gate-first* epitaxial Ge n-MOSFET on Si. Using high-κ $LaAlO_3$, this study achieved good device performance of a record small *SS* and high mobility at high E_{eff} among reported *gate-first* Ge n-MOSFETs, as well as the very low I_{OFF} for low power application and a small 1.6 nm EOT. The self-aligned, gate-first TaN/$LaAlO_3$/Ge/Si n-MOSFETs had the advantage of simple processing and compatibility with current VLSI lines.

	Process	**Metal Gate**	**High-κ**	**EOT (nm)**	**I_{off} (A/μm)**	***SS*** **(mV/dec)**	**Peak Mobility (cm^2/V-s)**	**Mobility 0.5 MV/cm (cm^2/V-s)**
[2-10]	*Gate-first*	TaN	HfAlO	3.0	-	110	412	low
[2-13]	Gate-last	Au	GeO_2	large	-	-	270	low
[2-14]	*Gate-first*	Al	Al_2O_3+ GeO_2	large	$1.24x10^{-9}$	-	404	133
[2-17]	*Gate-first*	Al	Al_2O_3+GeO_2	large	$9x10^{-10}$	-	488	363
[2-18]	Gate-last	Al	GeO_2(70-atm)	large	-	125	790	460
[2-19]	Gate-last	Al	Al_2O_3+GeO_2	large	$7x10^{-11}$	193	804	269
[2-20]	Gate-last	Al	SiO_2+GeO_2	large	$8.3x10^{-10}$	-	540	201
[2-22]	*Gate-first*	TaN	TiLaO+SiO_2	0.81	$3.5x10^{-10}$	126	271	201
This work	***Gate first***	**TaN**	**$LaAlO_3$**	**1.6**	**$7x10^{-10}$**	**108**	**296**	**218**

Table 2-1. Comparison of device integrity data for various metal-gate/high-κ Ge *n*-MOSFETs.

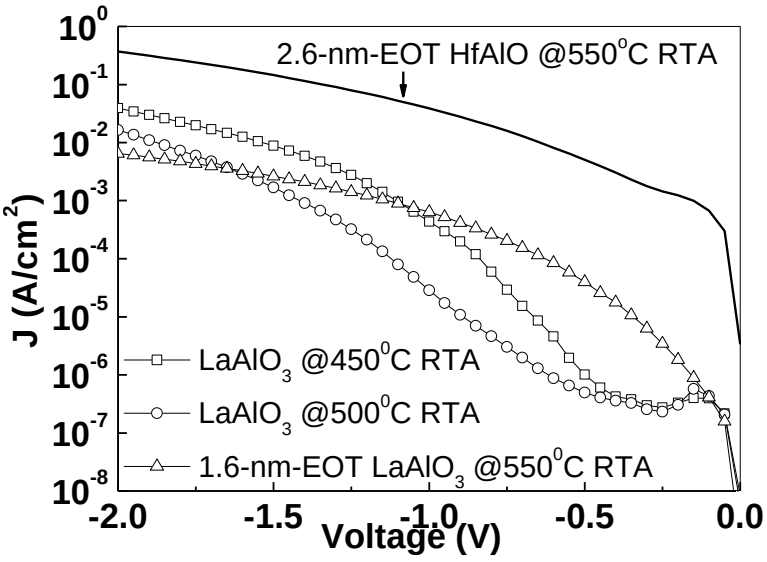


(a)

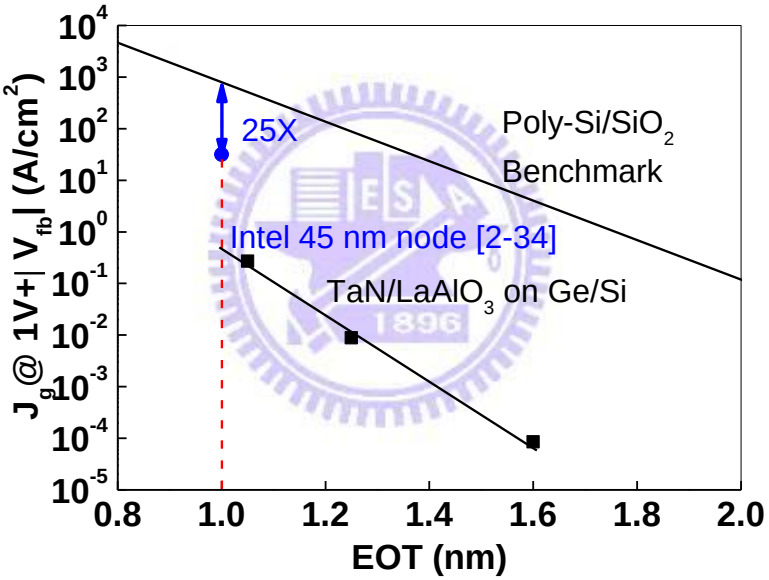


(b)

Fig. 2.1 *C-V* characteristics of (a) TaN/HfAlO/Ge/Si and control TaN/HfAlO/Si n-MOS capacitors and (b) TaN/$LaAlO_3$/Ge/Si n-MOS capacitors at 100 kHz after 450~550°C RTA

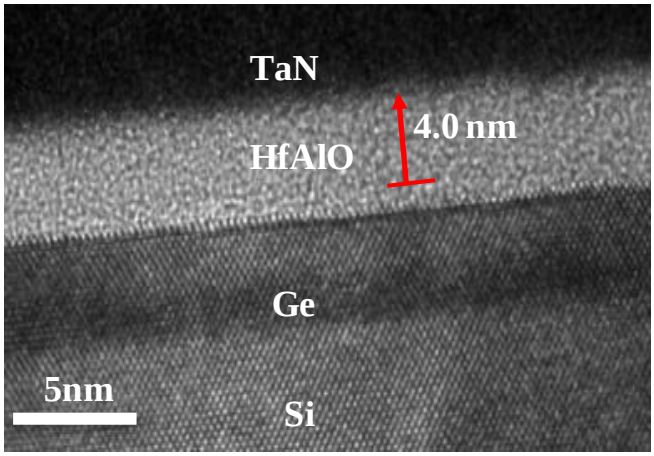


(a)

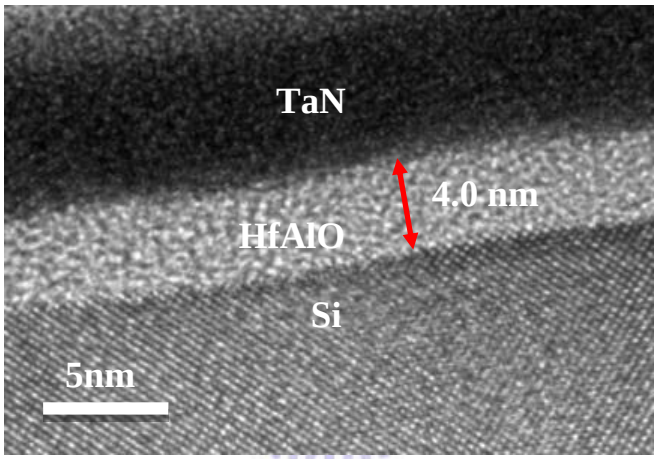


(b)

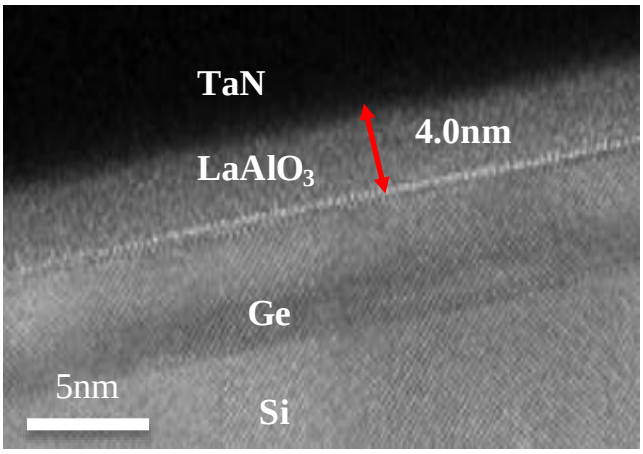
Fig. 2.2 (a) *J-V* characteristics of TaN/$LaAlO_3$/Ge/Si and TaN/HfAlO/Ge/Si n-MOS capacitors after 450°C~550°C RTA. (b) *J-EOT* characteristics of TaN/$LaAlO_3$/Ge/Si n-MOS capacitors after550°C RTA.



(a)

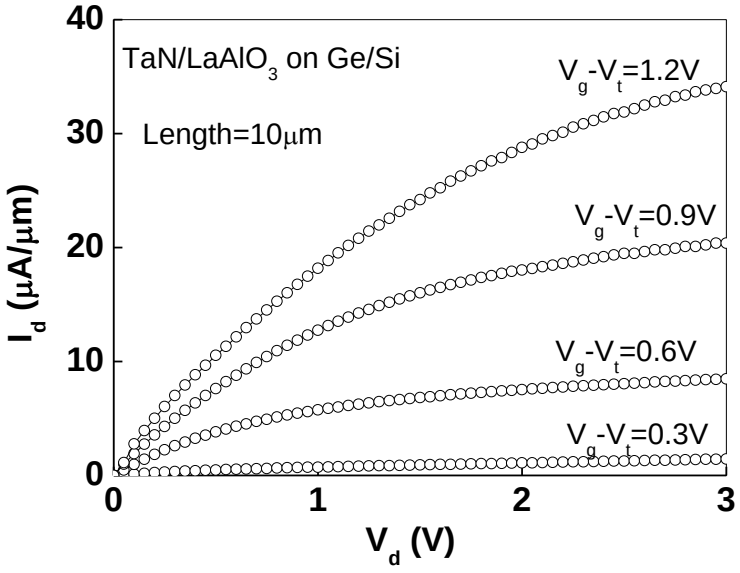


(b)

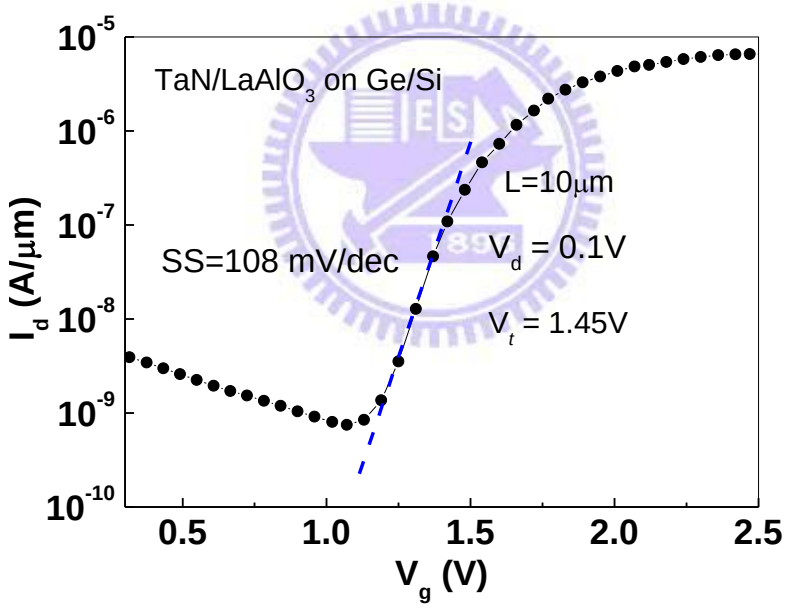


(c)

Fig. 2.3 Cross-sectional TEM of (a) TaN/HfAlO/Ge/Si capacitor, (b) control TaN/HfAlO/Si and (c) TaN/$LaAlO_3$/Ge/Si capacitors after 550^{o}C RTA.



(a)



(b)

Fig. 2.4 (a) I_d-V_d and (b) I_d-V_g characteristics of gate-first TaN/$LaAlO_3$/Ge/Si *n*-MOSFETs after 550°C RTA. The gate length and width are 10 and 100 μm, respectively.

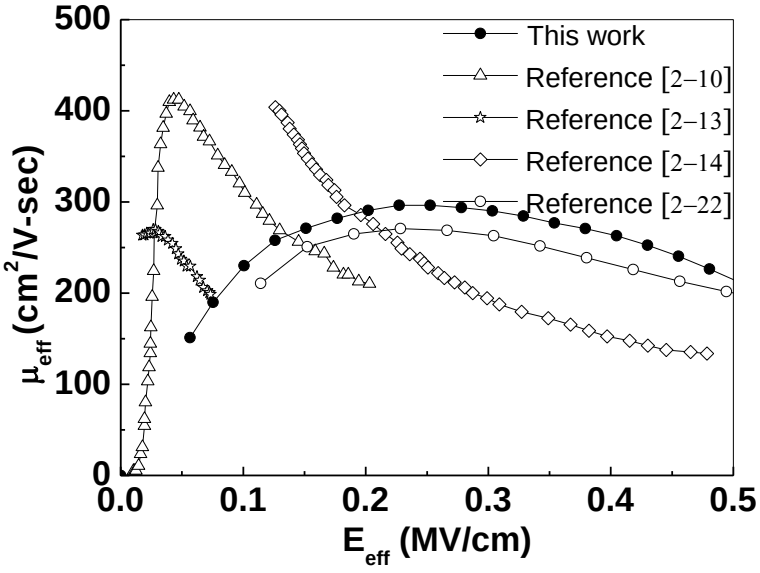


Fig. 2.5 Electron mobility vs. effective electric field of TaN/$LaAlO_3$/Ge/Si *n*-MOSFET and other published data for comparison.

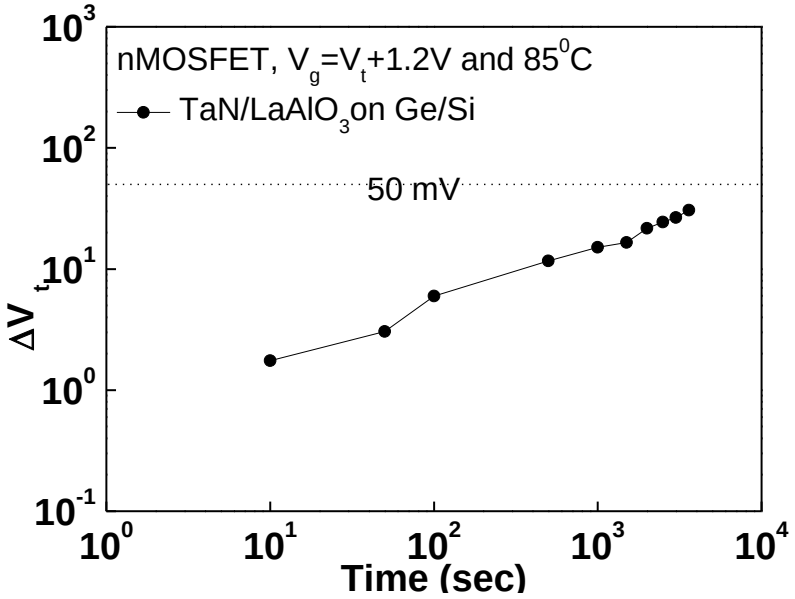


Fig. 2.6 V_t shift of TaN/$LaAlO_3$/Ge/Si *n*-MOSFET stressed at 85^oC for 1 hour.

Chapter 3
Interfacial Layer Dependence on Device Property of High-κ TiLaO Ge/Si *N*-Type Metal-Oxide-Semiconductor Capacitors at Small Equivalent-Oxide Thickness

3.1. Introduction

Germanium (Ge) has attracted much attention for Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [3-1]-[3-14] application due to both higher electron and hole mobilities than Silicon (Si). However, the difficult challenges are the high leakage current of small energy bandgap (E_G) Ge and the poor interface property with high dielectric-constant (κ) material. To lower the leakage current, we pioneered the defect free Ge-on-insulator (GOI or GeOI) [3-1] structure, and the leakage current decreases with decreasing the Ge body thickness [3-5]. Nevertheless, the degraded interface property is still a tough challenge especially for the Ge *n*-type MOSFET (*n*-MOSFET) [3-6]-[3-12] at a small equivalent oxide thickness (EOT). The interface property is highly dependent on high-κ dielectrics, where Al_2O_3 [3-1] and La_2O_3 [3-8]-[3-11] show lower interface trap density than HfO_2. This is related to the different Metal-Oxygen-Ge and defect formations [3-11] after a rapid-thermal anneal (RTA). To improve the interface, several passivation methods have been proposed

such as plasma nitridation,[3-4]-[3-8] NH_3 treatment, SiH_4 annealing and interfacial GeO_2 layer [3-8]-[3-10], [3-12]-[3-14] at larger EOT, but small EOT less than 1 nm is needed for 32 nm node and beyond. In this paper, we have applied the ultra-thin GeO_2 and SiO_2 interfacial layers [3-15] into high-κ TiLaO [3-16] epitaxial-Ge/Si *n*-type MOS (*n*-MOS) capacitors, where the ultra-thin body Ge of 5 nm is directly grown on Si to reach low leakage current. The TiLaO gate dielectric has the merits of unique negative flat-band voltage (V_{fb}) from La_2O_3 [3-17] and the much higher κ by adding TiO_2 [3-16]. Such negative V_{fb} is needed for low threshold voltage (V_t) MOSFET. The control TaN/TiLaO/Ge/Si *n*-MOS capacitor without the ultra-thin GeO_2 or SiO_2 interfacial layer showed poor EOT and large V_{fb} degradation after a 550°C RTA, which is required to activate ion-implanted source-drain in the MOSFET. Such degradations are related to interface reaction and oxygen vacancy formation [3-18]-[3-19] that are much improved by inserting the ultra-thin GeO_2 or SiO_2 [3-15] interfacial layer. However, the high-κ TiLaO Ge/Si *n*-MOS capacitor with interfacial GeO_2 showed much poorer capacitance-voltage (*C*-*V*) hysteresis than that using SiO_2 at a smaller EOT less than 1 nm. This is due to the Ge out-diffusion and intermixing of high-κ TiLaO/GeO_2 as observed by cross-sectional Transmission Electron Microscopy (TEM) and Secondary Ion Mass Spectroscopy (SIMS).

3.2. Experimental procedure

After RCA cleaning, a 200 nm undoped Si buffer, 5 nm Ge and 1.5 nm Si

capping layer were epitaxial grown on 6-in p-type Si substrate (10 ohm-cm) by ultra-high-vacuum chemical-vapor-deposition (HUVCVD). After removing the native oxide of Si-capping layer, various thick GeO_2 or SiO_2 and 5 nm high-κ TiLaO [3-16] were deposited by physical vapor deposition (PVD) and followed by post-deposition annealing (PDA) at 400^{o}C in oxygen ambient to improve gate dielectric quality. Here the ultra-thin Si capping is used to prevent Ge oxidation and process loss, where no interfacial Si was found by cross-sectional TEM after device process. Then a 50 nm TaN was deposited and patterned to form the metal gate. The formed gate stack was applied by a 550^{o}C RTA that is needed for Ge *n*-MOSFET fabrication. Finally, Aluminum (Al) was deposited on wafer backside to form the MOS capacitors. For comparison, control device without GeO_2 or SiO_2 interfacial layer was also made. The fabricated gate stack was examined by SIMS, TEM, X-ray Photoelectron Spectroscopy (XPS) and *C-V* measurements to investigate the physical, chemical bonding and electrical properties, respectively.

3.3. Results and discussion

Figure 3.1 shows the measured *C-V* characteristics of high-κ TiLaO Ge/Si *n*-MOS capacitors with or without the interfacial GeO_2 or SiO_2 layer. For device without the inserted GeO_2 or SiO_2 layer, both the capacitance density and V_{fb} were severely degraded. Such V_{fb} roll-off at high temperature was previously reported due to the interface reaction between high-κ and semiconductor [3-19]. In contrast, the

capacitor with GeO_2 or SiO_2 layer shows much improved V_{fb} roll-off even after a 550°C RTA. Besides, the needed negative V_{fb} of -0.48 V is obtained and important for low V_t Ge *n*-MOSFET. However, the device with GeO_2 interfacial layer shows poorer *C-V* hysteresis of 93 mV at 1.1 nm EOT than the much improved 19 mV hysteresis at smaller 0.81 nm EOT for device using SiO_2 interfacial layer, by taking account of quantum-mechanical effect with parameters of Ge [3-7]. The *C–V* hysteresis and negative V_{fb} value are among the best reported data for Ge *n*-MOS capacitors at the smallest EOT and after a 550°C RTA [3-1]-[3-14], to our best knowledge.

We have used TEM to study the better electrical performance for device using interfacial SiO_2 layer. Figures 3.2(a) and 3.2(b) show the TEM images of TaN/TiLaO/GeO_2/Ge/Si *n*-MOS structure before and after a 550°C RTA. Sharp GeO_2 interfacial layer of 0.76 nm thickness was found for *as-deposited* sample but becomes blurred after the 550°C RTA. The high-κ layer is also thicker after the 550°C RTA, where intermixing of high-κ TiLaO and GeO_2 is observed. The thicker high-κ layer explains the lower capacitance density after a 550°C RTA. In strong contrast, sharp SiO_2 interface shown in Fig. 3.2(c) is still preserved even after the 550°C RTA.

We have further used SIMS to study the large difference for devices with different interfacial GeO_2 and SiO_2. Figures 3.3(a) and 3.3(b) show the measured SIMS profiles of TaN/TiLaO on Ge/Si structure with interfacial GeO_2 and SiO_2 layers,

respectively. Severe Ge out-diffusion was found for device structure with interfacial GeO_2 layer after a 550°C RTA, while much improved Ge out-diffusion was achieved using ultra-thin SiO_2 interfacial layer even at a smaller 0.81 nm EOT.

The degraded interface property with ultra-thin interfacial GeO_2 was also examined by XPS. Figure 3.4 shows the Ge $2p^3$ XPS spectra of TiLaO/GeO_2/Ge/Si *n*-MOS structure before and after the 550°C RTA. The *as-deposited* sample shows a strong Ge peak at 1217.4 eV, and a small higher energy side peak is attributed to Ge-O bonds of GeO_2 [3-20]. However, this Ge-O peak becomes much weaker for the sample after the 550°C RTA. This is consistent with the largely thinned GeO_2 and intermixed TiLaO/GeO_2 interface found from cross-sectional TEM and the large Ge out-diffusion measured by SIMS. The thinner interfacial GeO_2 after the high temperature 550°C RTA may be related to the measured reaction at 758~589K [3-21]:

$$GeO_{2(s)} + Ge_{(s)} \rightarrow 2\ GeO_{(g)} \quad (2)$$

In contrast, the interface reaction between ultra-thin SiO_2 layer and Ge is unfavorable due to the much higher bond enthalpy of SiO_2 (800 kJ/mol) than GeO_2 (659 kJ/mol) [3-22].

3.4. Conclusion

In conclusion, we have studied the high-κ TiLaO on Ge/Si MOS structure with GeO_2 and SiO_2 interfacial layers. Low EOT of 0.81 nm, small *C-V* hysteresis of 19 mV and needed negative V_{fb} are obtained using ultra-thin SiO_2 interfacial layer. The

device with ultra-thin interfacial GeO_2 shows inferior device performance of larger EOT and poor *C-V* hysteresis, which is due to the severe Ge out-diffusion through GeO_2 from SIMS profile, thicker gate dielectric from TEM observation and thinned interfacial GeO_2 after a 550^{o}C RTA from TEM and XPS analysis.

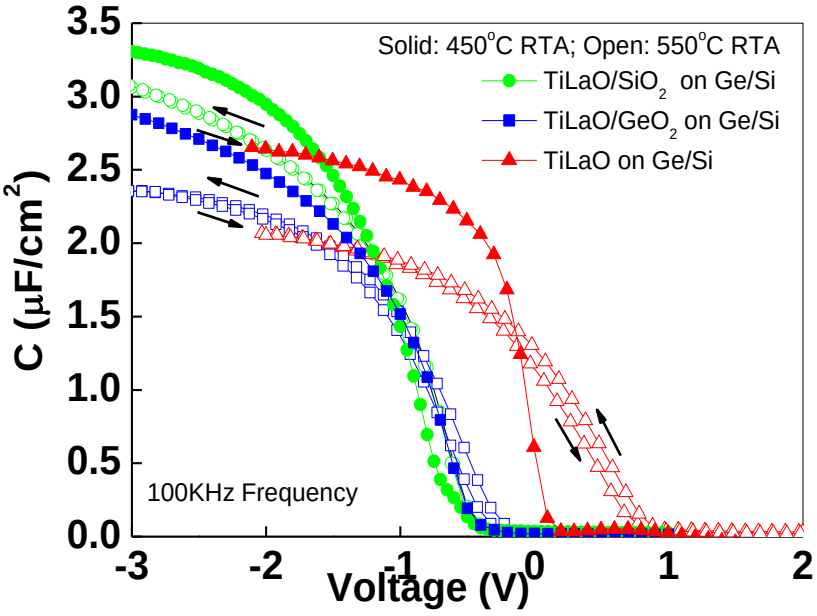
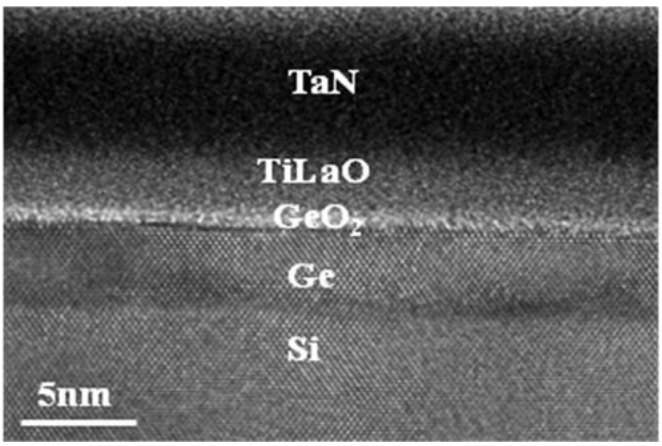
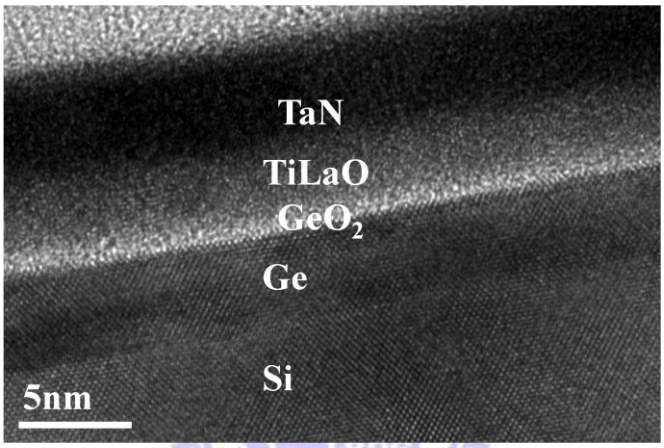


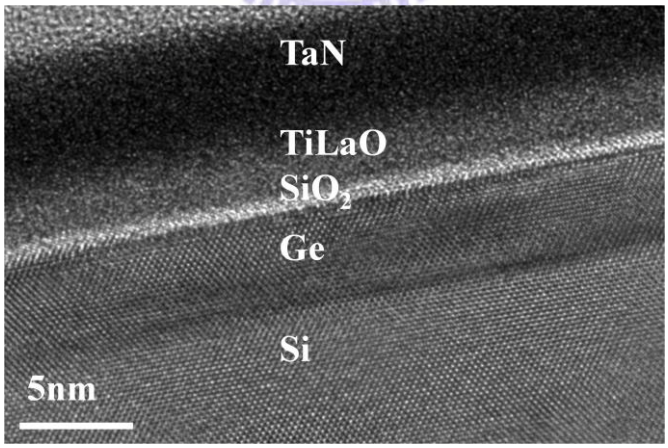
Fig. 3.1. *C-V* characteristics of TaN/TiLaO Ge/Si *n*-MOS capacitors with or without the inserted GeO_2 and SiO_2 interfacial layer and after 450 or 550°C RTA. The device size is 100-μmx100-μm.



(a)

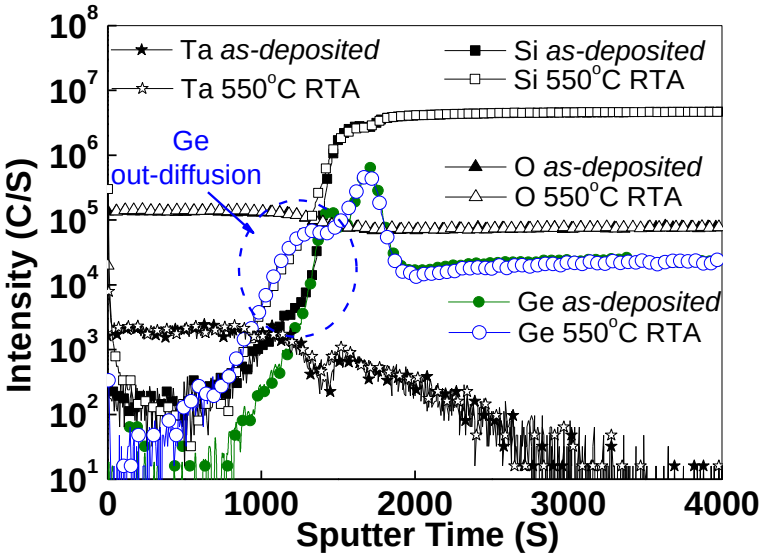


(b)

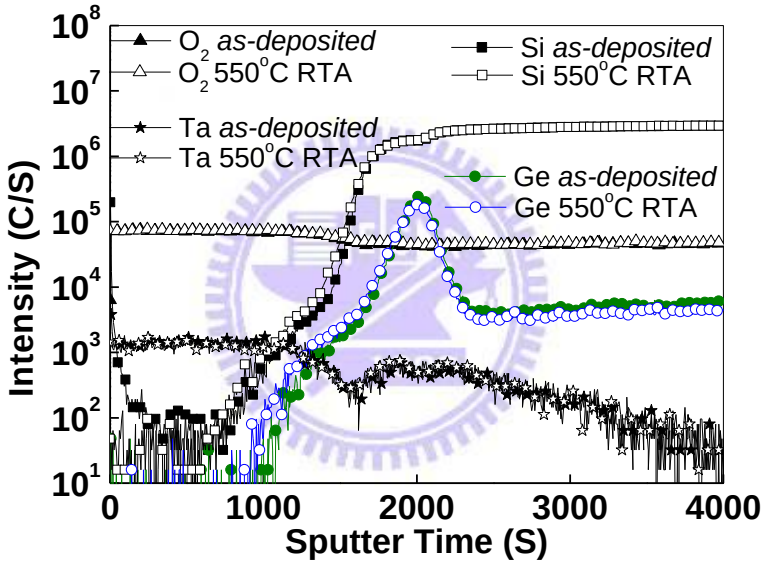


(c)

Fig.3.2. Cross-sectional TEM images of TaN/TiLaO/GeO_2/Ge/Si *n*-MOS capacitors (a) before and (b) after 550^{o}C RTA. (c) TaN/TiLaO/SiO_2/Ge/Si *n*-MOS capacitors after 550^{o}C RTA.



(a)



(b)

Fig. 3.3. SIMS profile of TaN/TiLaO Ge/Si *n*-MOS structure with inserted (a) GeO_2 and (b) SiO_2 interfacial layer before and after 550°C RTA.

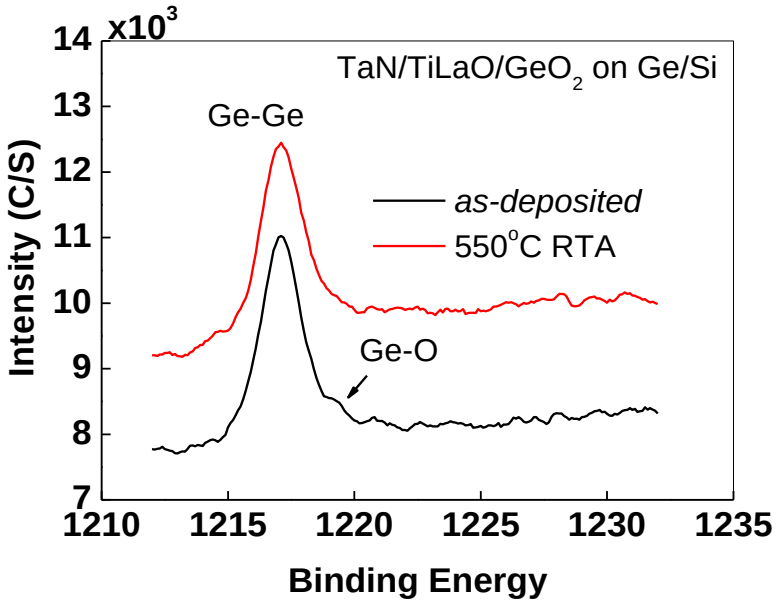


Fig. 3.4. The Ge $2p^3$ XPS spectra of TiLaO/GeO_2/Ge/Si structure before and after 550°C RTA.

Chapter 4

High Performance of Ge n-MOSFETs Using SiO2 Interfacial Layer and TiLaO Gate Dielectric

4.1. Introduction

The Ge channel MOSFETs [4-1]-[4-11] have attracted much attention due to higher bulk electron and hole mobilities than Si counterparts. Nevertheless, the technical challenges for Ge MOSFETs are severe, which include the integration of defect-free Ge on Si substrate, the large leakage current of small energy bandgap (E_G) Ge and the poor electron mobility at high effective electric field. The integration of defect-free Ge on Si was demonstrated by us using wafer-bonded Ge-on-insulator (GOI or GeOI) technology [4-1]. The leakage current of small E_G Ge MOSFET is also lowered by thinning Ge body thickness in GOI [4-5]. However, the electron mobility degradation at high effective field is still a severe issue, which is especially important for MOSFET at small equivalent-oxide thickness (EOT). In order to improve the mobility, many interface passivation methods have been proposed such as NH_3 surface treatment, SiH_4 annealing [4-4], Si capping layer [4-6], [4-9] and GeO_2 interfacial layer [4-7]-[4-8]. Unfortunately, these methods still got relative low mobility at high effective field. The SiO_x interfacial layer has been used for Ge p-MOSFET [4-10], but the small EOT, low off-state leakage (I_{OFF}) and good high

field mobility are still the major challenges for Ge n-MOSFET. In this paper, we report high mobility at high effective field for Ge n-MOSFETs with small capacitance-equivalent-thickness (CET), which was achieved by using higher κ TiLaO dielectric [4-12]-[4-13] and SiO_2 interfacial layer. In contrast, much degraded CET and unwanted flat-band voltage (V_{fb}) shift were measured for control device without the SiO_2 interfacial layer.

4.2. Experimental procedure

After standard clean, an undoped 200 nm Si buffer, undoped 5 nm Ge and undoped 1.5 nm Si capping layer were grown on p-type (100) Si wafers (5×10^{15} cm^{-3} doping) by ultra-high-vacuum chemical-vapor-deposition (HUVCVD) at 500°C and 5×10^{-4} torr. An ultra-thin 0.8 nm SiO_2 was deposited by Physical Vapor Deposition (PVD) using Electron-Beam Evaporation at the room temperature and 2×10^{-6} torr pressure [3-14], where the native oxide of Si-capping layer was removed using dilute HF solution. Here the Si-capping is to prevent the thin Ge loss during process, since Ge can be oxidized by water and air similar to Si case and GeO_2 is dissolvable by water. No Si-capping layer was found by cross-section TEM after process. A 5 nm thick $Ti_xLa_{1-x}O$ (x~0.67) [3-12] with κ of 45 was deposited and followed by a 400°C post-deposition anneal (PDA) in an oxygen ambient for 5 min. Then a 200 nm TaN was deposited by PVD and patterned to form the metal gate. For comparison, the capacitors without SiO_2 interfacial layer were also fabricated. After that, self-aligned

25 KeV As^+ ion implantation was applied at a 5×10^{15} cm^{-2} dosage and 550°C RTA. From the X-Ray Diffraction (XRD) study, the TiLaO is amorphous after 550°C RTA. Finally, non-alloyed Al contact metal was added. The fabricated devices were characterized by capacitance-voltage (*C-V)* and current-voltage (*J-V)* measurements.

4.3. Results and Discussion

In Fig. 4.1 we showed the *C-V* characteristics of TaN/TiLaO on Si-capped Ge/Si capacitors after 450~550°C RTA. These devices showed severe degradations of capacitance density, V_{fb} shift, and hysteresis after a 550°C RTA, which was related to interfacial layer formation as found by TEM. However, this temperature is required to activate the ion implanted dopants at source-drain of Ge MOSFET.

To address the interface reaction, we added an ultra-thin SiO_2 interfacial layer between high-κ and Ge. Figures 4.2(a) and 4.2(b) showed the *C-V* and *J-V* characteristics of the TaN/TiLaO/SiO_2 on Ge/Si *n*-MOS devices. Much smaller unwanted V_{fb} shift and less interface states generation are reached than the devices without SiO_2 interfacial layer shown in Fig. 4.1. The good high-κ and interface quality is also evident from the small *C-V* hysteresis of only 19 mV from -3 to 1 V sweep. Such large difference is due to the dense and strong bonding SiO_2 to prevent the Ge out diffusion during the process, from SIMS measurements. Besides, a small 1.1 nm CET is obtained after 550°C RTA with 4 orders of magnitude lower leakage current than poly-Si/SiO_2.

Figures 4.3(a) and 4.3(b) show the respective I_d-V_d and I_d-V_g characteristics. Good transistor characteristics of relatively high drive current, small sub-threshold swing (*SS*) of 126 mV/dec and a record low I_{OFF} leakage of 3.5×10^{-10} A/μm [4-6]-[4-8] were measured simultaneously. This is due to the ultra-thin body (UTB) of conductive Ge channel on Si substrate that is well predicted by UTB GOI MOSFETs [4-5]. Such low leakage current is mandatory for future generation low power green transistor.

Figure 4 shows the electron mobility versus effective electric field, where the data was directly derived from measured I_d-V_g curves [4-15]. Good high field mobility at 0.5 MV/cm is 201 cm^2/V-s [4-6]-[4-8] at a small 1.1 nm CET. The good high field mobility is consistent with the needed negative V_{fb}, small *C*-*V* hysteresis and *SS*; here the *SS* of 126 mV/dec is one of the best reported data for Ge *n*-MOSFET in literature [4-1]-[4-11]. The good high field mobility is vital for MOSFET at a small EOT, where a still high 0.65 V drain voltage is needed even for 11 nm node technology according to *ITRS*.

4.4. Conclusions

We have demonstrated high performance epitaxial Ge *n*-MOSFET on Si using higher κ TiLaO and SiO_2 interfacial layer. Good device performance is reached in terms of small CET, record low I_{OFF} and the highest mobility at high effective electric field. Besides, this self-aligned and gate-first transistor has the advantages of simple processing and compatibility with current VLSI lines.

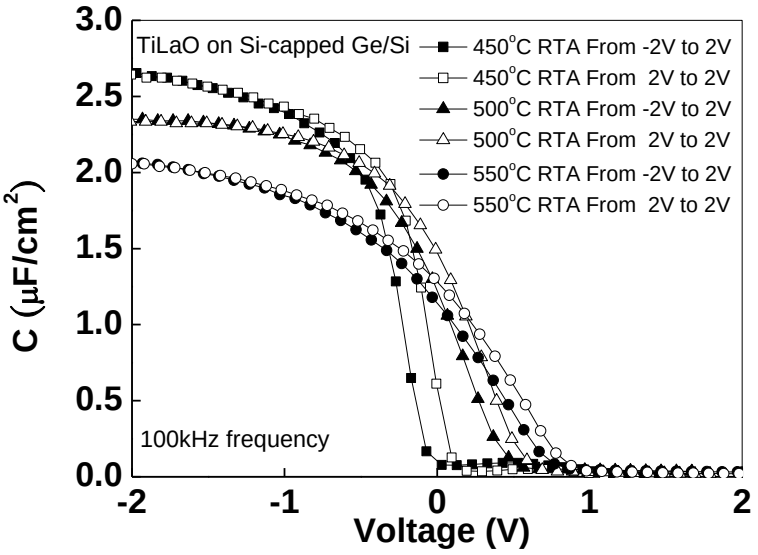
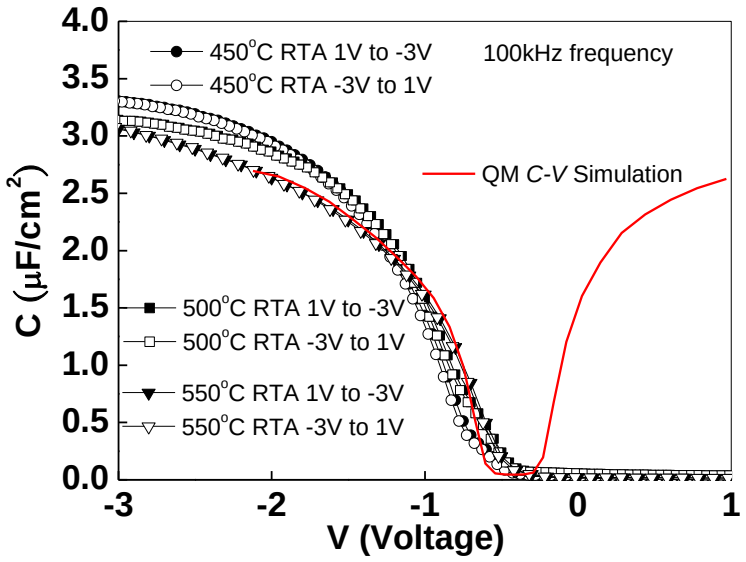
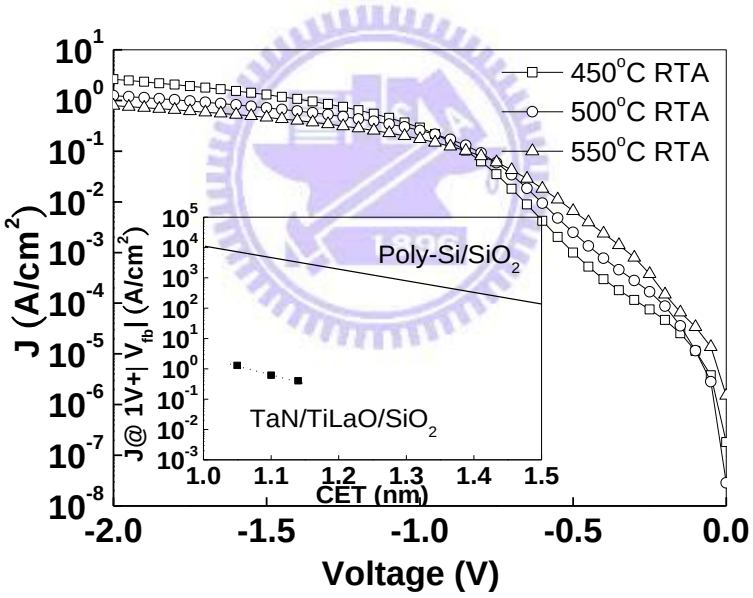


Fig. 4.1. *C-V* and of the TaN/TiLaO on Si-Capped Ge/Si *n*-MOS capacitors after 450~550°C RTA.

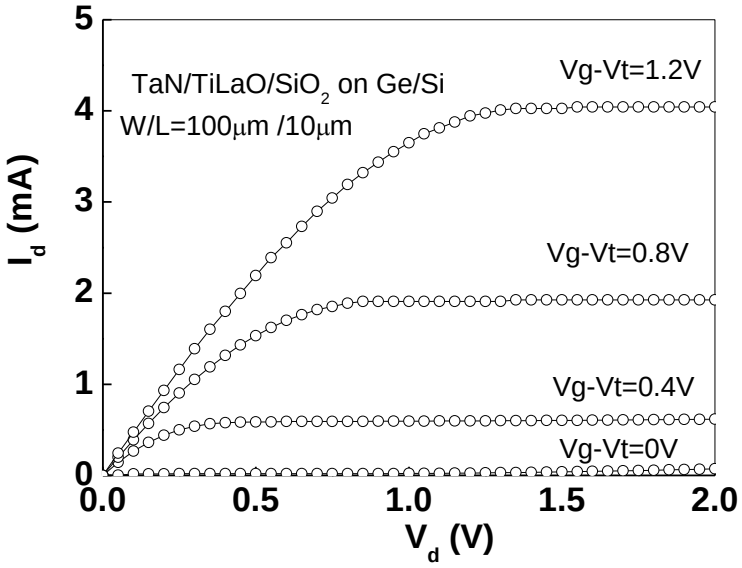


(a)

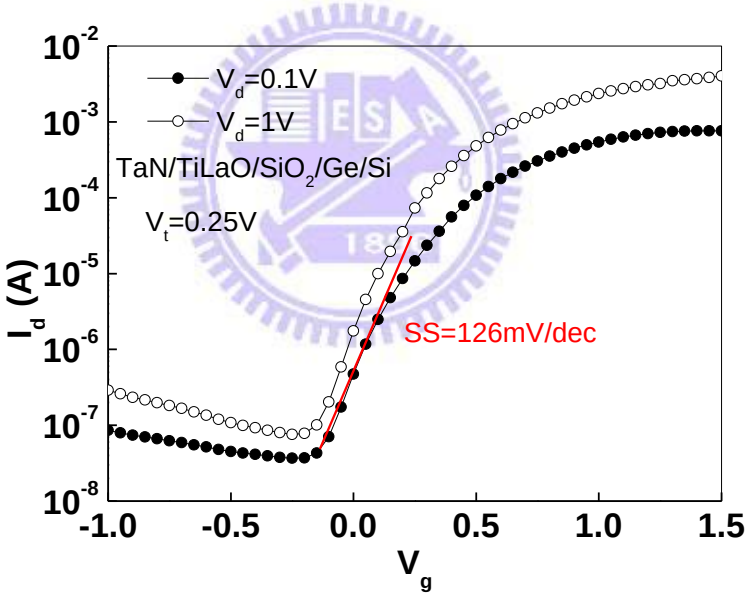


(b)

Fig. 4.2. (a) The *C-V* and (b) *J-V* characteristics of the TaN/TiLaO/SiO_2 on Ge/Si *n*-MOSFETs 450~550°C RTA. The inserted figure in (b) is the *J-CET* plot at 1 V above V_{fb}.



(a)



(b)

Fig. 4.3. (a) The I_d-V_d and (b) I_d-V_g characteristics of the TaN/TiLaO/SiO_2 on Ge/Si *n*-MOSFETs.

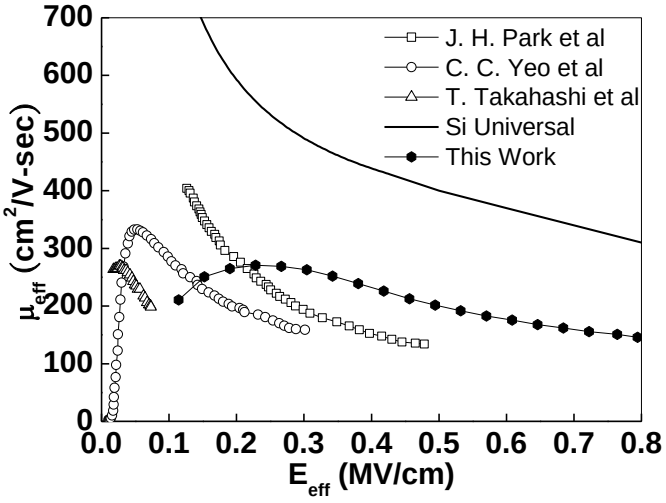


Fig.4. 4. The electron mobility as a function of effective electric field for the TaN/TiLaO/SiO_2 on Ge/Si *n*-MOSFETs.

Chapter 5

High Field Mobility Metal-Gate/high-κ Ge *n*-MOSFETs with Small Equivalent-Oxide-Thickness

5.1. Introduction

Recently, the high performance Metal-Oxide-Semiconductor field effect transistors (MOSFETs) with using high-κ materials such as La_2O_3 [5-2], Al_2O_3 [5-3], [5-19], HfO_2 [5-5] and mixed metal oxides have been proposed to replace the conventional SiO_2 MOSFETs for EOT (equivalent oxide thickness) scaling. However, the scalable performance enhancement depends on channel length scaling, gate dielectric scaling and optimized strain engineering like SiGe source-drain and compressive contact etch stop layer (CESL). Ge channel is expected to additionally boost the mobility at thin EOT. Thus, much attention has been focused on Ge channel complementary metal oxide semiconductor field effect transistors (CMOSFETs) [5-1]-[5-22], which is due to 2-4 times higher electron and hole mobility than those of Si devices. Besides, the densities of states are ~ 50 times larger than III-V InGaAs substrate for higher drive current. However, the challenging issues of the small-bandgap-induced high leakage current, sensitive to process temperature and poor interface quality due to Ge out-diffusion are the major challenges.

To address these issues, the defect-free Ge-on-insulator (GOI or GeOI) [5-3] and

thin body Ge-on-Si [5-17], [5-18] are proposed. Nevertheless, the low electron mobility at high effective electronic field (E_{eff}) and poor equivalent-oxide thickness EOT scaling are still the unsettled issues. The lower peak mobility could be attributed to the Coulomb scattering in the high-κ dielectric that was also found in high-κ/Si [5-27], [5-29]. Such challenges become worst at gate-first process, where the high thermal budget degrades the mobility originated from interface reaction and Ge out-diffusion. Although several surface passivation approaches such as NH_3 surface treatment and Si-capping on Ge channel [5-8], [5-10], [5-12], [5-21], [5-22] were proposed, high field mobility at small EOT still needs to be developed.

In this study, we reported the high-field mobility of Ge n-MOSFETs using TaN/La_2O_3/SiO_2 gate stack. The La_2O_3 dielectric [5-2], [5-23], [5-24] with high-κ value and negative flat band voltage (V_{fb}) are important for n-MOSFET. The metal-gate/device show high field mobility of 258 cm^2/Vs at 0.75 MV/cm with a small 1.9-nm EOT. The results are ascribed to the SiO_2 barrier layer and low thermal budget process to suppress the Ge out-diffusion into high-κ dielectric.

5.2. Experimental Procedure

We used a 2-in p-type Ge (100) wafers with a doping concentration of 5×10^{14} cm^{-3} in these experiments. After standard clean, 500 nm isolation oxides were deposited by Plasma-enhanced chemical vapor deposition (PECVD). Then active

areas were defined by lithography and wet etching. After that As^+ was implanted at source and drain region at 25 KeV and a dosage of 5×10^{15} cm^{-2} and followed by a 550^oC rapid thermal annealing (RTA) for dopant activation. A 0.8 nm thick SiO_2 and 6 nm La_2O_3 were deposited by dual E-Gun evaporation system at a pressure of 2 x 10^{-6} torr and followed by a 400^oC post-deposition anneal (PDA) in an oxygen ambient for 5 min to densify the gate dielectric quality. A 150-nm-thick TaN metal was deposited and patterned to form the gate electrode by a sputter system at a pressure of 9 x 10^{-7} torr. Finally, the Ge n-MOSFET was formed by adding 300-nm-thick Al metal contacts to source-drain by thermal evaporation coater and annealed at 400^OC for 25 min in an N_2 ambient. Figures 5.1 (a) and (b) show the schematic image and process flow. The fabricated devices were characterized by *C-V* and *I-V* measurements by HP4284A precision LCR meter and HP4156C semiconductor parameter analyzer, respectively. The devices were also analyzed by SIMS (Secondary ion mass spectroscopy), and cross-sectional transmission electron microscopy (TEM).

5.3. Result and Discussion

Figures 5.2(a) and 5.2(b) show the *C-V* and *J-V* characteristics of TaN/La_2O_3/SiO_2/Ge devices. The increasing PDA temperature from 350 to 450^oC improves the gate leakage current for several times, with only slight V_{fb} shift. The

slight EOT increase with increasing PDA temperature is related to interfacial layer formation. At 400°C PDA temperature, a capacitance density of 1.54 μF/cm^2 was measured that gave an EOT of 1.9 nm from quantum-mechanical *C-V* (*QM*-CV) simulation using Ge material parameters. Besides, a low leakage current of 8×10^5 A/cm^2 was reached at 1 V above V_{fb}. The *C-V* curves spreading with different PDA were mainly attributed to interface reaction. Compared to 350°C and 450°C, the capacitor with an optimized 400°C PDA shows a corresponding thinner EOT of 1.9nm and lowest leakage current at 1 V above V_{fb} shift. The large leakage and small capacitance density caused by serious interface oxidation for over high-temperature 450°C explain the importance of thermal budget control during dielectric activation. The combined effect of thicker interfacial layer and poor interface state may lead to the performance degradation on capacitance density and leakage current. Thus, an appropriate PDA temperature not only can effectively activate the defect-rich dielectric but also suppress the serious interface oxidation, especially for Ge substrate.

We further analyzed the gate stack on Ge substrate by SIMS and TEM. Figures 5.3 (a) and (b) show the SIMS depth profile and cross-sectional TEM image, respectively. No apparent Ge out-diffusion was found by SIMS that is important to reach mobility and low gate leakage for Ge MOSFET [5-22]. This is further confirmed by the sharp interface between La_2O_3/SiO_2 and Ge as observed by

cross-sectional TEM. The sharp SiO_2-like layer formation may result from intermixing effect near Si interface which can reduce the Ge out-diffusion into high-κ La_2O_3 dielectric during optimized 400°C PDA. Such SiO_2-like interface layer is also related to the low leakage current and *C*-*V* characteristics in Figure 5.2.

Figures 5.4(a) and 5.4(b) present the I_d-V_d and I_d-V_g characteristics of TaN/La_2O_3/SiO_2/Ge n-MOSFET respectively, fabricated at a PDA low-temperature of 400°C. Well-behaved transistor characteristics were reached, where a low threshold voltage (V_t) of -0.22 V was measured. The negative threshold voltage results from the negative V_{fb} shown in Fig. 1, which is important for Ge n-MOSFETs. Further V_t adjustment to positive can be obtained using higher work-function gate electrode in the future work. From the following sub-threshold swing (*SS*) equation, it gives an interface trap density (D_{it}) of 9.5×10^{12} $eV^{-1}cm^{-2}$ [5-25]. The *SS* is degraded with the relative high D_{it} and the further improvement is required in the future.

$$SS = kT/q\times\ln10 \text{ x } [1 + (C_{dep}+C_{it})/C_i]$$

where C_{dep}, C_{it} and C_i are the depletion capacitance density, capacitance density of charged interface traps, and gate capacitance density, respectively.

Figure 5.5 shows the mobility as a function of E_{eff} over a wide range for the TaN/La_2O_3/SiO_2/Ge n-MOSFET. High peak mobility of 486 cm^2/Vs and 0.75 MV/cm mobility of 258 cm^2/Vs were measured at a small EOT of 1.9 nm. The mobility was

directly calculated from the I_d-V_g curves and the equations are shown as the following [5-26]:

$$\mu_{eff} = I_d/(W_{eff}/L)C_{ox}(V_{gs}-V_t)V_{ds} \quad \text{(a)}$$

The effective normal field can be expressed as:

$$E_{eff} = (Q_{inv}/2 + Q_B)/\varepsilon_{Ge} \quad \text{(b)}$$

where Q_{inv} is the inversion layer charge, Q_B is the bulk depletion-layer charge and ε_{Ge} is the permittivity of Ge. Here the I_d versus V_g is extrapolated to zero drain current (I_d =0) and the threshold voltage (V_{th}) is determined from intercept gate voltage (V_g). Although many studies have been proposed for high performance and high peak mobility, the scaling down is also the issue for large EOT. High transistor current (I_d) due to the following relation:

$$I_d=WC_{inv}v_{eff}(V_g-V_t)$$

Here the v_{eff} is effective source velocity and related to high - field effective mobility [5-28], since the MOSFET is biased at $V_g=V_{d,sat}$ for higher I_d rather than at a low V_g with good peak mobility. Such high field operation is inevitable for MOSFET at highly scaled EOT used for advanced Ge CMOSFETs technology node.

Table 5-1 summarizes the important device parameters of metal-gate/high-κ Ge n-MOSFETs [5-17]-[5-20]. Figure 5.6 shows the peak mobility comparisons of references in Table 5-1. Our TaN/La_2O_3/SiO_2/Ge n-MOSFET has high-field mobility

of 258 cm^2/Vs at 0.75 MV/cm at the smallest 1.9-nm EOT.

5.4. Conclusion

We have demonstrated a high performance Ge n-MOSFET using high-κ La_2O_3/SiO_2 stack dielectric, suitable for future EOT scaling. Device performance of high 258 cm^2/Vs at 0.75 MV/cm and small EOT of 1.9-nm are reached simultaneously, which is due to the smooth interface observed by TEM.

Gate stack	**Junction**	**EOT (nm)**	**Peak Mobility (cm^2/Vs)**	**Mobility @ 0.75 MV/cm (cm^2/Vs)**
$Al/Al_2O_3/GeO_2/Ge$ [5-17]	P^+-implant, 350°C RTA	-	488	258
Al/GeO_2(70-atm)/Ge [5-18]	P^+-implant, 580°C RTA	-	790	366
$Al/Al_2O_3/GeO_2/Ge$ [5-19]	600°C gas phase doping	-	804	~210
$Al/SiO_2/GeO_2/Ge/Si$ [5-20]	600°C *in-situ* doping	-	540	~134
$TaN/La_2O_3/SiO_2/Ge$ (This work)	**As^+-implant, 550°C RTA**	**1.9**	**486**	**258**

Table 5-1. Comparison of device integrity data for various metal-gate/high-κ Ge *n*-MOSFETs.

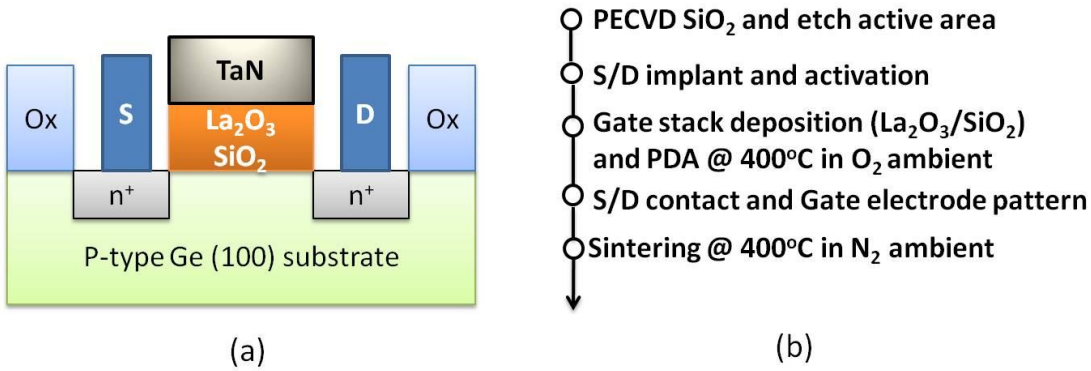
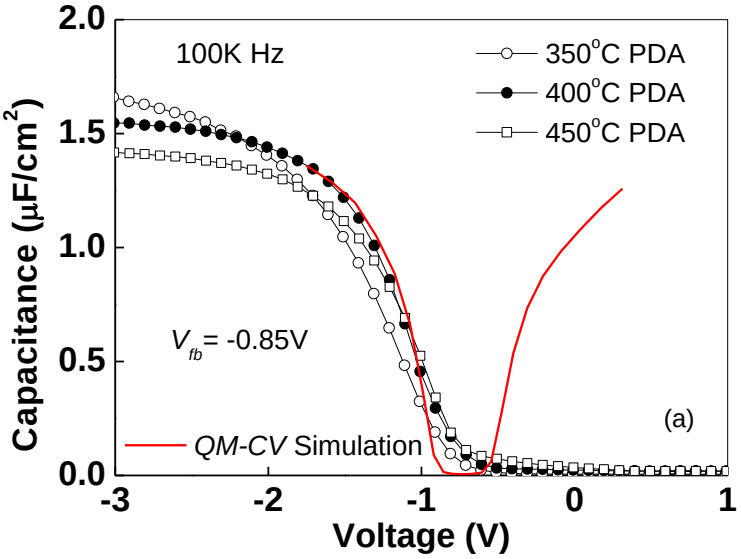
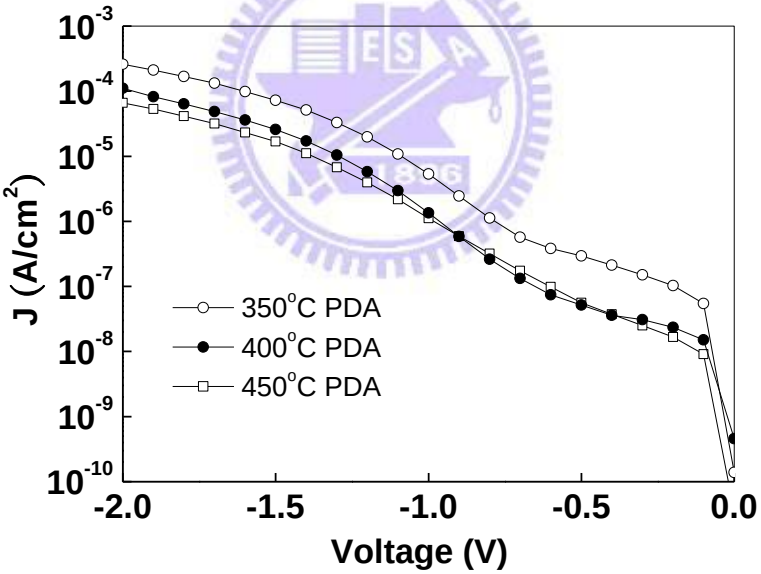


Fig. 5.1. (a) Schematic image of TaN/La_2O_3/SiO_2/Ge n-MOSFET and (b) process flow of *gate-last* Ge-n MOSFET

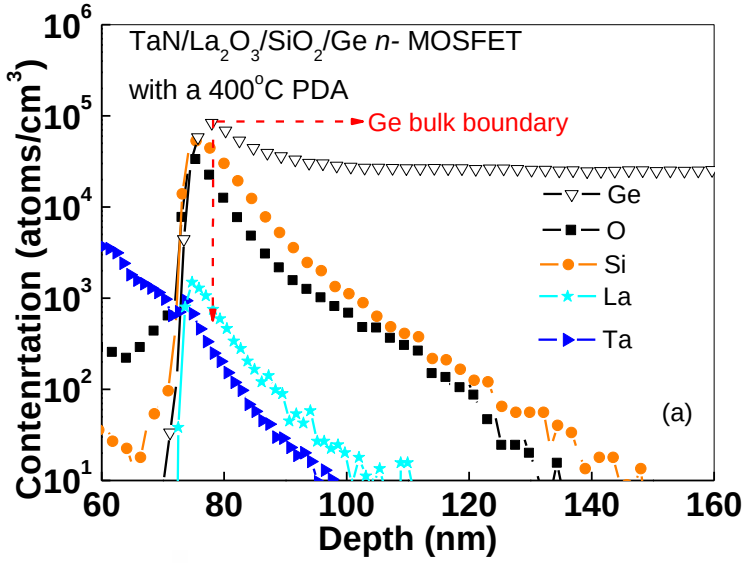


(a)

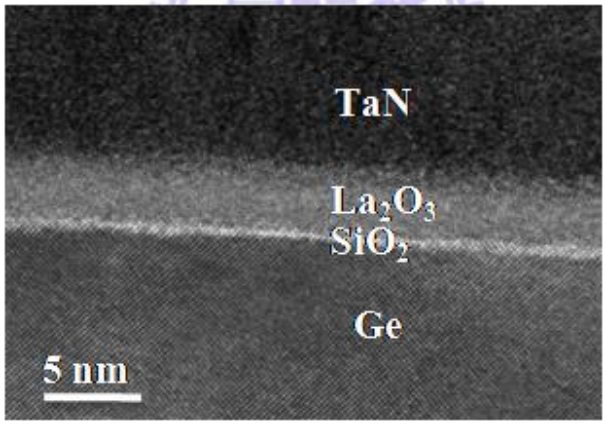


(b)

Fig. 5.2. (a) *C-V* and (b) *J-V* characteristics of TaN/La_2O_3/SiO_2/Ge n-MOS capacitors with different PDA temperatures.

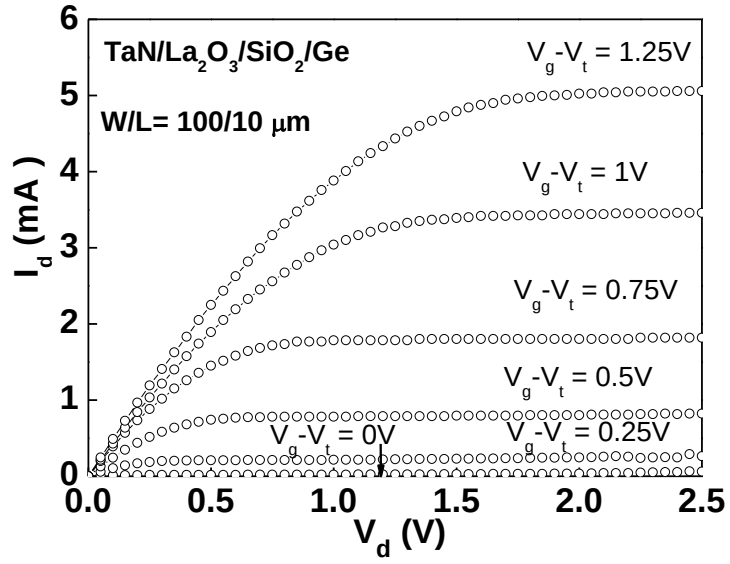


(a)

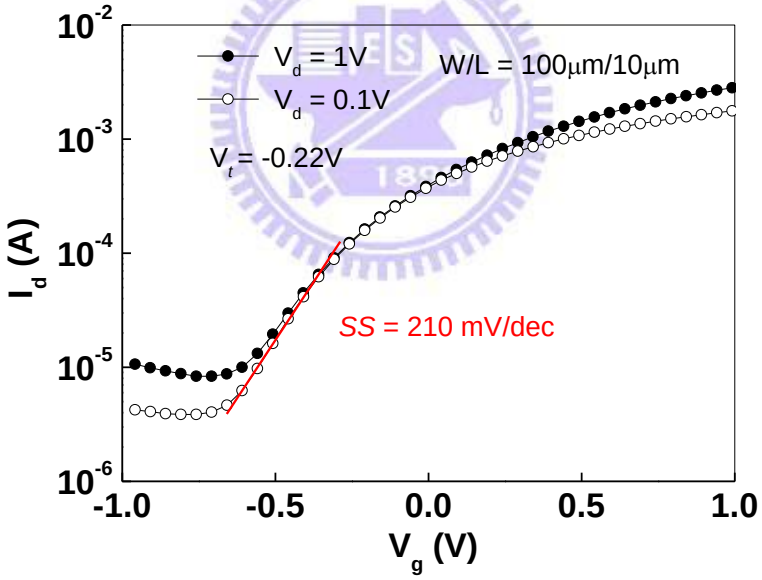


(b)

Fig. 5.3. (a)SIMS depth profile of TaN/La2O3/SiO2/Ge at a 400°C PDA. (b) Cross-sectional TEM of TaN/La2O3/SiO2/Ge after a 400°C PDA.



(a)



(b)

Fig. 5.4. (a) I_d-V_d and (b) I_d-V_g plots of TaN/La_2O_3/SiO_2/Ge *n*-MOSFET.

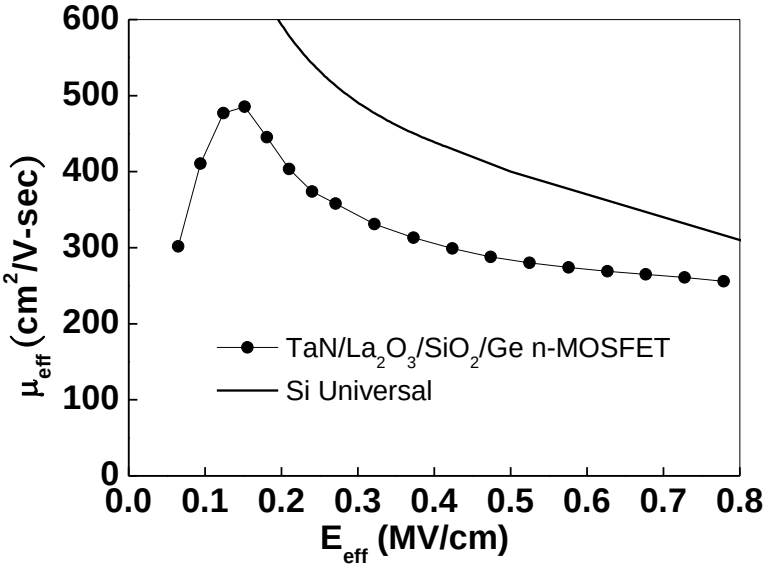


Fig. 5.5. The electron mobility as a function of effective electric field of TaN/La_2O_3/SiO_2/Ge *n*-MOSFETs.

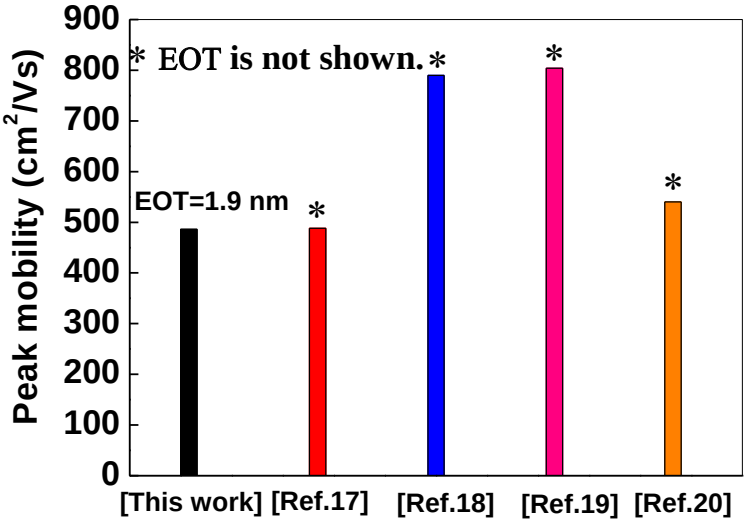


Fig. 5.6. The comparison of electron peak mobility of Ge *n*-MOSFETs

Chapter 6

Gate-First TaN/La_2O_3/SiO_2/Ge n-MOSFETs Using Laser Annealing

6.1. Introduction

The small bandgap (E_G) Ge shows high potential for MOSFET application due to both higher electron and hole mobilities than Si. However, the difficult challenges are the high leakage current of small E_G Ge, poor high-κ/Ge interface property, and low doping activation at ion-implanted source-drain [6-1]-[6-14]. To lower the leakage current, we pioneered the defect-free Ge-on-insulator (GOI or GeOI) [6-1] and ultra-thin body Ge-on-Si [6-14]. Nevertheless, the low doping activation by RTA and poor high-κ/Ge interface property are still the issues, while the high temperature RTA degrades the mobility by Ge out-diffusion and forms poor interface. Although a gate-last process with GeO_2 dielectric was developed for this purpose [6-9]-[6-10], the *gate-first* process is still attractive due to the much simpler process. Besides, the filling high-κ and metal in narrower gate opening may be another concern using gate-last process, since Ge is expected to implement in 15~10 nm node CMOS.

In this chapter we have used low energy laser annealing [6-7], [6-15]-[6-19] to improve the doping activation of ion-implanted source-drain and preserve good high-κ/Ge interface, while laser annealing is also essential for ultra-shallow junction

[6-15]-[6-16]. High performance *gate-first* TaN/La_2O_3/SiO_2/Ge n-MOSFET was obtained using laser annealing, with high peak mobility of 603 cm^2/Vs and 0.75 MV/cm mobility of 304 cm^2/Vs at small 1.9 nm EOT. The good mobility at high effective electric field (E_{eff}) is necessary for highly scaled MOSFET at small EOT. These results are beyond the best reported data for *gate-first* metal-gate/high-κ/Ge n-MOSFET at small EOT <2 nm.

6.2. Experimental Procedure

The 2-in p-type Ge (100) wafers were used for the experiments. After standard clean, an ultra-thin 0.8 nm SiO_2 and a 6 nm high-κ La_2O_3 were deposited by physical vapor deposition (PVD) [6-14] and followed by post-deposition anneal under oxygen ambient. After 150 nm TaN gate-metal deposition and patterning, the n^+ source-drain regions are formed by As^+ implantation at 25 KeV and 5×10^{15} cm^{-2} dose. Then scanned KrF laser annealing (248 nm, ~30 ns pulse) was applied to activate the implanted dopant [6-14]. The junction characteristics and sheet resistance (R_s) were measured to characterize the effect of laser annealing. Finally, Al metal contacts were added to source-drain and form the Ge n-MOSFET. The fabricated devices were characterized by *C-V* and *I-V* measurements using an HP4284A precision LCR meter and HP4156C semiconductor parameter analyzer, respectively.

6.3. Result and Discussion

Figures 6.1(a) and 6.1(b) show the R_s and n^+/p junction characteristics of As^+-implanted Ge after laser annealing. The increasing laser fluence (energy/area) improves R_s, the junction ideality factor (n) and forward current, while still maintaining a low reverse leakage current. The R_s decreases rapidly with increasing laser fluence to 0.16 J/cm^2. This value is significantly lower than our previous 0.36 J/cm^2 for laser annealing on Si MOSFET [6-16], which is due to the much lower melting temperature of Ge than Si. The lower laser fluence is important to decrease the energy absorption by TaN gate that can cause unwanted interface reaction and V_{fb} roll-off [6-16]. The R_s as low as 68 Ω/sq was obtained at 0.2 J/cm^2 laser fluence that is 40% better than the 112 Ω/sq value using RTA at 550^{o}C. Small n-factor of 1.3 and very large 10^5 forward/reverse current ratio are measured for n^+/p junction using laser annealing. An effective Schottky barrier height of 0.6~0.62 eV and a low contact resistance of 2×10^{-6} Ω-cm are obtained from J-V curve and Transfer Length Method, respectively. The higher forward current in the n^+/p junction with good doping activation is crucial to reach the higher drive current for Ge n-MOSFET.

Figures 6.2(a) and 6.2(b) show the C-V and J-V characteristics of TaN/La_2O_3/SiO_2/Ge devices, where the V_{fb} shift and increasing gate current were found by laser annealing. The V_{fb} shift after laser annealing is due to the interface

reaction [6-16], but a negative V_{fb} is still obtained for low threshold voltage (V_t) n-MOSFET. An EOT of 1.9 nm was obtained from quantum-mechanical *C-V* calculation with Ge material parameters [6-7], [6-14]. The effect of laser annealing on gate dielectric was also examined by cross-sectional TEM. Still sharp interfacial SiO_2 layer was observed by laser annealing that gives the good *C-V* characteristics. This is due to the low 0.2 J/cm^2 laser fluence, although it is high enough to melt and crystallize the ion-implanted Ge. Besides, ~1/3 energy was reflected at top TaN surface from the measured reflectivity [6-16]. These further lower the energy absorption by high-κ/Ge interface. More detailed study is necessary to understand the higher gate leakage current after laser annealing.

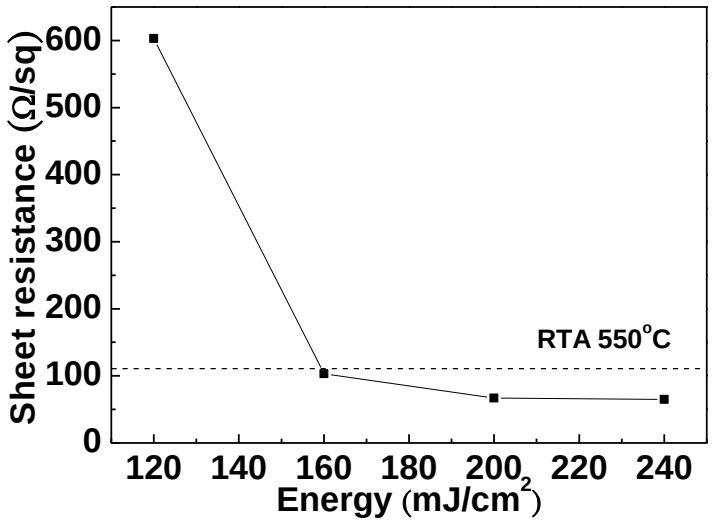
Figures 6.3(a) and 6.3(b) show the I_d-V_d and I_d-V_g characteristics of La_2O_3/SiO_2/Ge n-MOSFETs using laser annealing. Well behaved transistor characteristics and a good sub-threshold swing of 125 mV/dec were reached, which gives an interface density (D_{it}) of 9×10^{12} eV^{-1}cm^{-2} [6-20]. The small *SS* is due to the high gate capacitance density even with relative high D_{it}. A V_t of -0.47 V is due to the negative V_{fb} measured from *C-V* curves in Fig. 2(a). Further adjusting the V_t to positive is needed. Figure 6.4 shows the mobility versus E_{eff}. High peak mobility of 603 cm^2/Vs and 0.75 MV/cm mobility of 304 cm^2/Vs are reached using laser anneal, which is one of the highest electron mobility for *gate-first* Ge n-MOSFET.

6.4. Conclusion

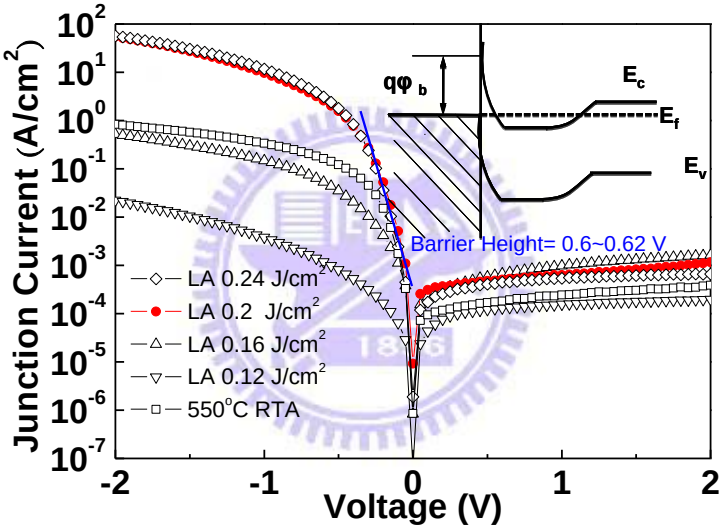
By applying low energy laser annealing on TaN/La_2O_3/SiO_2/Ge n-MOSFETs, small junction *n*-factor of 1.3, large 10^5 forward/reverse current of n^+/p junction, high 603 cm^2/Vs peak mobility and good high-field (0.75 MV/cm) mobility of 304 cm^2/Vs were reached simultaneously at small EOT of 1.9 nm.

Gate stack	Junction	EOT (nm)	Peak Mobility (cm^2/Vs)	Mobility @ 0.75 MV/cm (cm^2/Vs)	Process
$Al/Al_2O_3/GeO_2/Ge$ [6-10]	600^oC gas phase doping	large	804	~210	Gate last
$Al/Al_2O_3/GeO_2/Ge$ [6-11]	P^+-implant, 350^oC RTA	large	488	258	*Gate-first*
Al/GeO_2(70-atm)/Ge [6-12]	P^+-implant, 580^oC RTA	large	790	366	Gate last
$Al/SiO_2/GeO_2/Ge/Si$ [6-13]	600^oC *in-situ* doping	large	540	~134	Gate last
$TaN/La_2O_3/SiO_2/Ge$ (this work)	**As^+-implant, laser anneal**	**1.9**	**603**	**304**	***Gate-first***

Table 6-1. Comparison of device data of various metal-gate/high-κ/Ge *n*-MOSFETs.

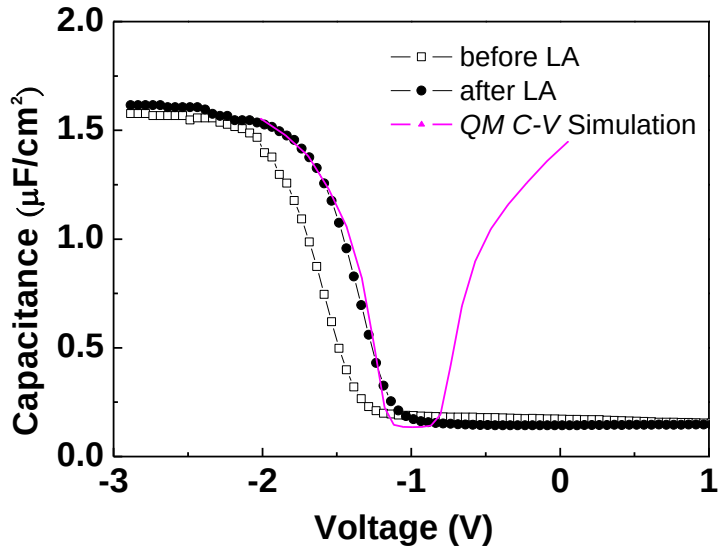


(a)

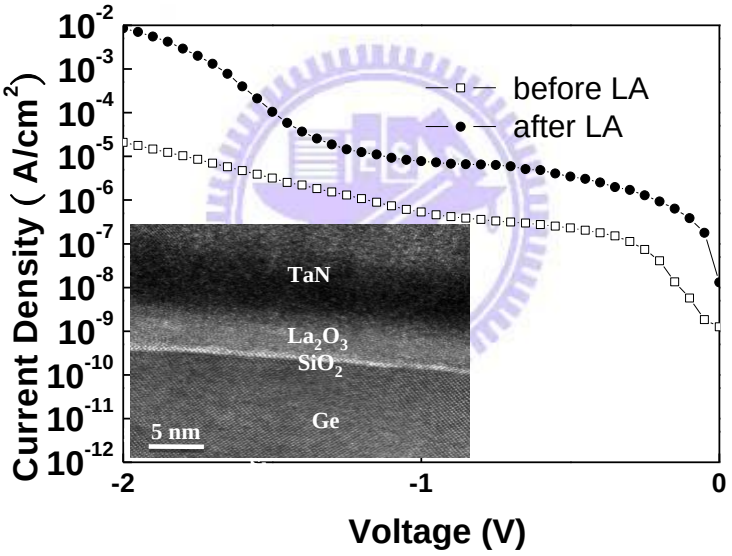


(b)

Fig. 6.1. (a) Sheet resistance and (b) n^+/p junction characteristics of As^+-implanted Ge after laser annealing.

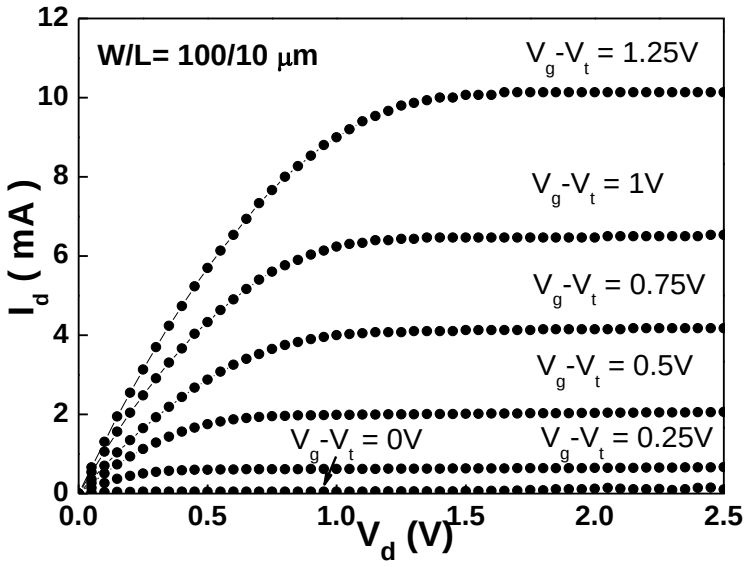


(a)

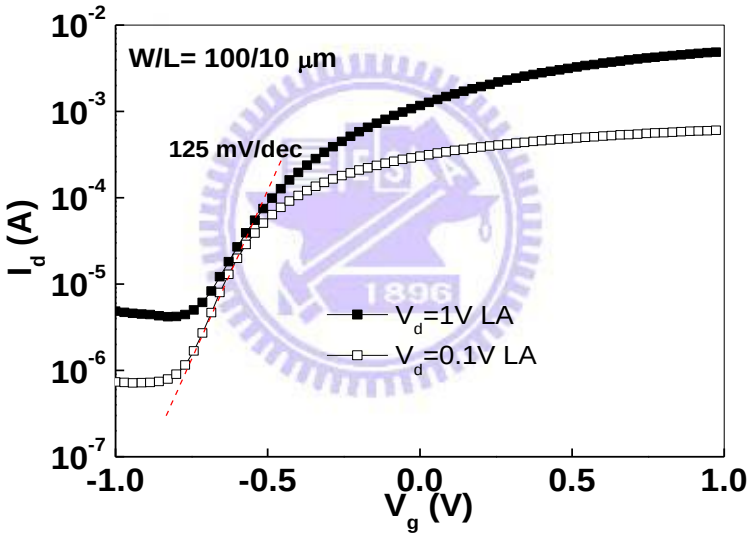


(b)

Fig. 6.2. (a) *C-V* and (b) *J-V* characteristics of TaN/La_2O_3/SiO_2/Ge n-MOS capacitors before and after laser annealing. The insert figure is the cross-sectional TEM after laser annealing.



(a)



(b)

Fig. 6.3. (a) I_d-V_d and (b) I_d-V_g of *gate-first* TaN/La_2O_3/SiO_2/Ge *n*-MOSFET using laser annealing.

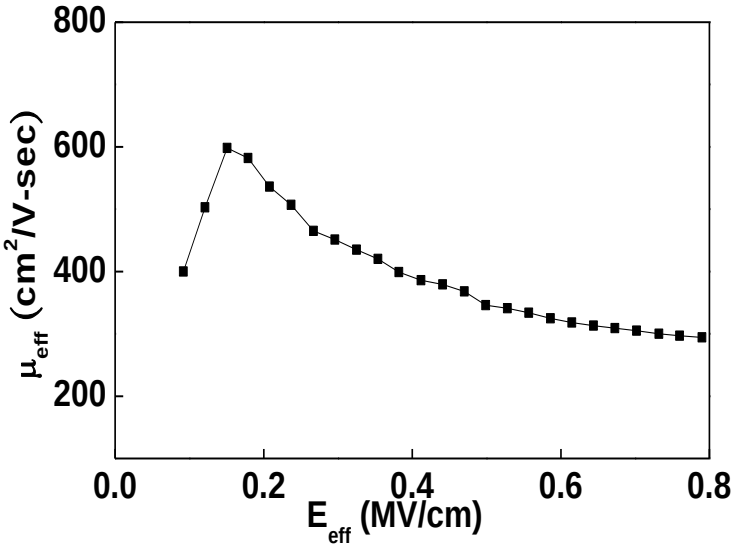


Fig. 6.4. The electron mobility as a function of effective electric field of TaN/La_2O_3/SiO_2/Ge *n*-MOSFETs using laser annealing.

Chapter 7

Higher Gate Capacitance Ge n-MOSFETs Using Laser Annealing

7.1. Introduction

Ge has attracted much attention due to its features of both higher electron (2X) and hole mobilities (4X) than Si [7-1]-[7-15]. Furthermore, Ge has ~50X higher density of state than InGaAs to deliver high transistor current. The integration of Ge on Si can be realized by using a Ge-on-insulator (GOI or GeOI) structure [7-1], where defect-free Ge has been realized. This GeOI structure can also suppress the leakage current of small energy bandgap Ge and is useful for device-level 3D IC [7-16]. The Ge p-MOSFET also shows 2.5X better high-field hole mobility at 1 MV/cm than SiO_2/Si universal mobility at small 1.4 nm EOT [7-16]. Nevertheless, achievement of good high-field electron mobility for Ge n-MOSFET at small EOT is still under development, but the small EOT of ~0.95 nm is needed to compete with metal-gate/high-κ/strained-Si n-MOSFET at 32 nm nodes. The poor Ge n-MOSFET is due to the low source-drain doping activation by RTA and poor high-κ/Ge interface property.

In this paper we have used laser annealing (LA) [7-7], [7-17]-[7-21] to improve both gate capacitance and n^+/p junction of Ge n-MOSFET [7-15]-[7-16]. Application

of LA on gate dielectric lowers EOT from 1.6 to 0.95 nm. Using LA, TaN/ZrO_2/La_2O_3/SiO_2/Ge n-MOSFET shows 645 cm^2/Vs peak mobility and 1 MV/cm mobility of 285 cm^2/Vs at 0.95 nm EOT. Such a good high-field mobility is necessary for highly scaled MOSFET at small EOT, operated at high effective electric field (E_{eff}).

7.2. Experimental Procedure

We used 2-in p-type Ge (100) wafers with 10 Ω-cm resistivity in the experiments. After standard cleaning, isolation oxides were formed by plasma-enhanced chemical vapor deposition (PECVD). After source and drain were defined with the SiO_2 dummy gate, Phosphorus ion was implanted at source-drain region at 35 KeV and 5×10^{15} cm^{-2}, followed by KrF LA (248 nm, ~30 ns pulse) for source-drain activation [7-16]. After pre-gate cleaning in cyclic diluted HF (1:50) and rinsing in DI water, ultra-thin 0.8 nm SiO_2, 1 nm high-κ La_2O_3 and 3 nm high-κ ZrO_2 were deposited by physical vapor deposition (PVD) [7-15] and followed by post-deposition anneal (PDA) under oxygen ambient. Then the second LA was applied to increase the gate capacitance density. The LA was performed under air ambient. The laser spot sizes were 0.3 cm^2 after focus and 0.9 cm^2 without focus for n^+/p junction and high-κ dielectrics annealing respectively, where continuous stepping in X and Y directions were used for the whole sample. Finally, the TaN gate electrode and source-drain Al

contacts were deposited to form Ge n-MOSFET. The contact window on source-drain was formed using BOE to remove gate dielectric.

7.3. Result and Discussion

Figures 7.1(a) and 7.1(b) show the *C-V* and *J-V* characteristics of TaN/ZrO_2/La_2O_3/SiO_2/Ge MOS capacitors formed by PDA and followed by LA and control 550^{o}C RTA. The LA significantly increases the gate capacitance from 1.7 μF/cm^2 (control 550^{o}C RTA) to 2.7 μF/cm^2 that gives a capacitance-equivalent-thickness (CET) of 1.27 nm. Such 59% improvement of gate capacitance is attributed to the crystallization-induced higher κ shown in the cross-sectional TEM inserted in Fig. 7.1(b), where similar crystallization-induced higher capacitance density and κ value were also found in ZrO_2 MIM capacitors by LA [7-21]. Sharp gate-stack/Ge interface after LA was also observed by TEM. In addition, only small *flat-band* (V_{fb}) shift and increasing gate current were found by LA as compared with those of control 550^{o}C RTA. The necessary negative V_{fb} value for low threshold voltage (V_t) n-MOSFET is due to the unique property of La_2O_3 gate dielectric [7-22]. The good high-κ quality after LA is evident from the small *C-V* hysteresis of only 21 mV, from −3 to 1 V sweep, and better than the 73 mV in control RTA device. An EOT of 0.95 nm was obtained from quantum-mechanical *C-V* calculation with Ge material parameters [7-7], [7-15].

LA can also improve the source-drain junction characteristics. Figure 7.2 shows n^+/p junction characteristics of P^+-implanted p-Ge after LA. At a laser fluence of 0.25 J/cm^2, small junction ideality factor (n) of 1.10 and the largest forward current were obtained, while still maintaining a low reverse leakage current. These results were better than those of control 550^{o}C RTA devices. In addition, low sheet resistance (R_s) of 73 Ω/sq was measured after LA and better than the 105 Ω/sq using 550^{o}C RTA. This LA fluence is lower than the previous 0.36 J/cm^2 to activate the ion-implanted Si MOSFET [7-18], which is due to the lower melting temperature of Ge than Si.

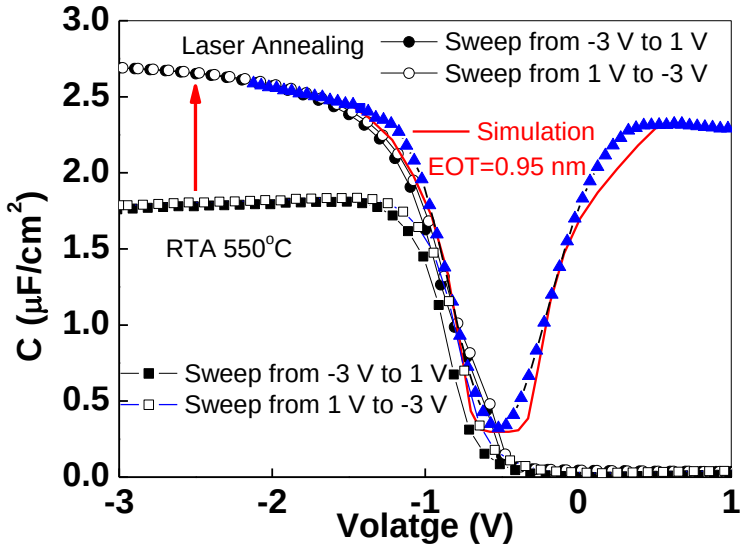
Figures 7.3(a) and 7.3(b) show the I_d-V_d and I_d-V_g characteristics of TaN/ZrO_2/La_2O_3/SiO_2/Ge n-MOSFETs using LA. Well-behaved transistor characteristics were reached, with a good sub-threshold swing of 106 mV/dec. A small threshold voltage (V_t) of 0.18 V is due to the negative V_{fb} measured from C-V characteristics shown in Figure 7.1(a).

Figure 7.4 shows the mobility as a function of E_{eff} over a wide range, which was obtained from split C-V data. High peak mobility of 645 cm^2/Vs and 1 MV/cm mobility of 285 cm^2/Vs are reached for the metal-gate/high-κ/Ge n-MOSFETs using LA at the small 0.95 nm EOT. It is important to note that the electron mobility was slightly higher than Si universal mobility at 1 MV/cm E_{eff}, which is also one of the highest reported levels of electron mobility of Ge n-MOSFETs at the smallest EOT

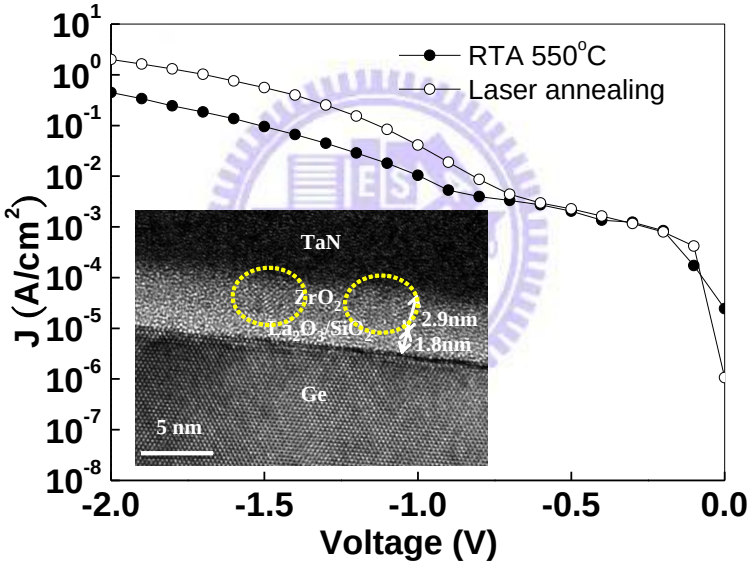
[7-1]-[7-15]. Even slightly higher mobility and capacitance density can be reached by considering the gate leakage current [7-23], where the gate leakage current is more than 3 orders of magnitude lower than SiO_2 at 0.95 nm EOT. The better high field mobility using LA than control RTA may be due to the 5.0 eV laser energy absorbed in the Ge, which in turn heats up the gate dielectrics and thereby improves the interface.

7.4. Conclusion

By applying low energy LA on TaN/La_2O_3/SiO_2/Ge n-MOSFETs, small junction *n*-factor of 1.10, small 106 mV/dec *SS*, and good 1 MV/cm high-field mobility of 285 cm^2/Vs were reached simultaneously at a small EOT of 0.95 nm.



(a)



(b)

Fig. 7.1. (a) *C-V* and (b) *J-V* characteristics of TaN/ZrO_2/La_2O_3/SiO_2/Ge n-MOS capacitors after 550°C RTA & LA. The insert figure is the cross-sectional TEM after LA.

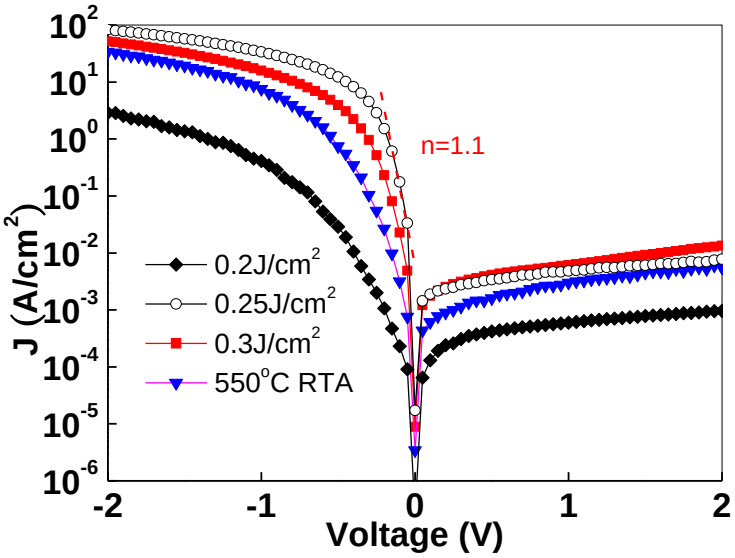
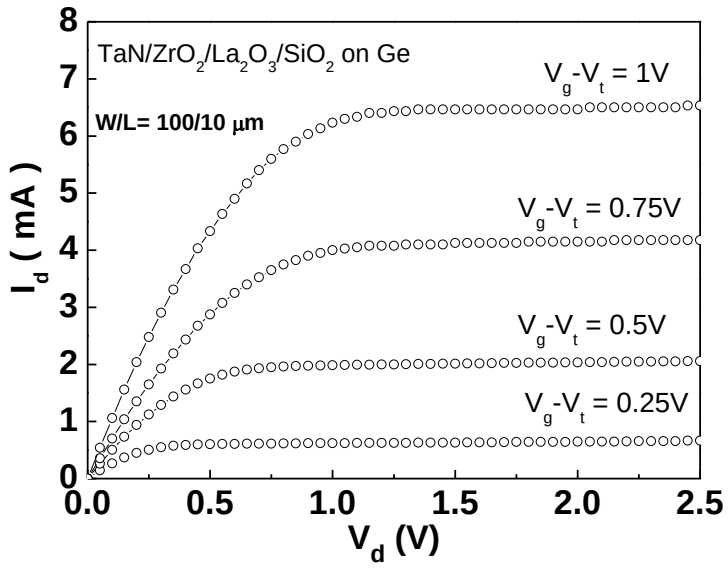
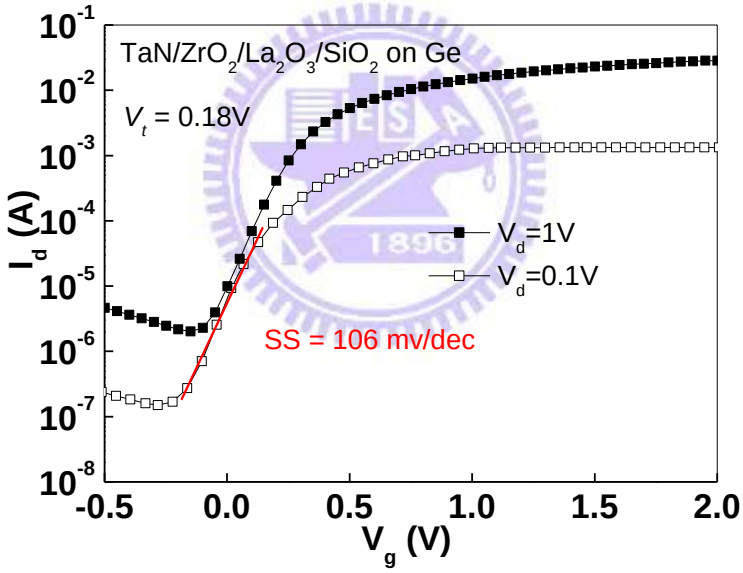


Fig. 7.2. The n^+/p junction characteristics of P^+-implanted Ge after LA.



(a)



(b)

Fig. 7.3. (a) I_d-V_d and (b) I_d-V_g of TaN/ZrO_2/La_2O_3/SiO_2/Ge *n*-MOSFET using LA.

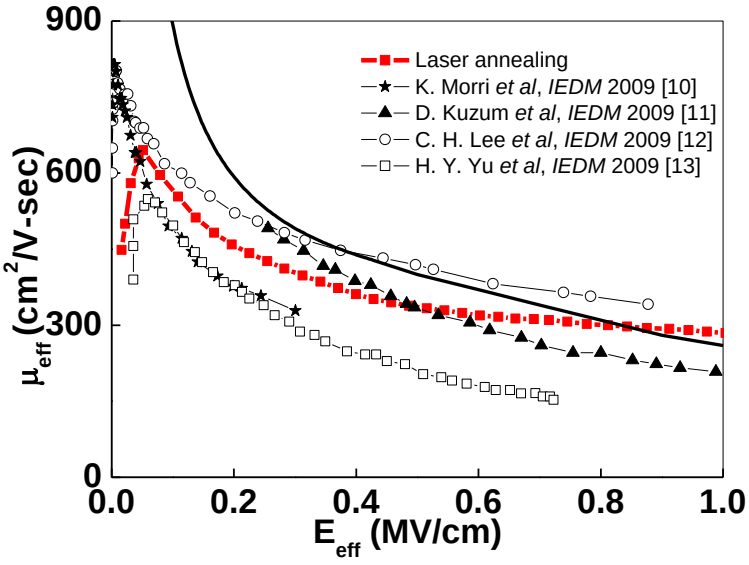


Fig. 7.4. The electron mobility as a function of effective electric field of TaN/ZrO_2/La_2O_3/SiO_2/Ge *n*-MOSFET using LA.

Chapter 8

Conclusion

We have developed successfully the interface passivation to reduce the unwanted interface reaction and used the laser annealing (LA) to improve the electrical properties of Ge n MOSFETs. First, using the $LaAlO_3$ high κ dielectric on Ge channel reached a 1.6 nm EOT and a 108 (mV/dec) sub-threshold swing for the *gate-first* process. In order to scale down the device sizes, we used the higher κ value dielectric TiLaO to replace the $LaAlO_3$. However, the passivation layer was very important between high k dielectric and Ge channel due to the process thermal budget. Therefore, we had also applied the an ultra thin SiO_2 interfacial layer. Using SiO_2 between Ge and TiLaO high k dielectric improved the EOT from 1.6 nm to 0.85 nm and small *C-V* hysteresis of only 19 mV from -3 to 1 V sweep was observed.

Although the device had scaled down to meet the ITRS for VLSI technology, the mobility was still not high enough for the Ge MOSFETs. Therefore, we used the Excimer laser to improve the junction characteristics and enhance the drive current. We had also used the *gate-last* process for La_2O_3 high k dielectric material with SiO_2 passivation layer to fabricate the Ge nMOSFETs. The conventional RTA and LA were applied for comparison. Using the laser annealing (LA) improved the peak mobility from 486 cm^2/Vs to 603 cm^2/Vs. Finally, we improved the previous device structure

by using ZrO_2 with gate stack on La_2O_3/SiO_2. We applied the LA not only on junctions but also on high κ dielectrics. The capacitance density increased from 1.7 $\mu F/cm^2$ (control 550^oC RTA) to 2.7 $\mu F/cm^2$ that gives a capacitance-equivalent thickness (CET) of 1.27 nm. Such 59% improvement of gate capacitance is attributed to the crystallization-induced higher κ. Here we reported the high performance with small EOT in this dissertation.

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Publication Lists

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(B) Conferences & Proceeding

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