國立交通大學

電子工程學系　　電子研究所

碩士論文

於鍺基板製作n^+–p型二極體及n型金氧半場效電晶體之電性研究

Electrical characteristics of n^+-p junction and nMOSFETs on bulk Germanium

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中華民國九十七年九月

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摘　　要

我們已經最佳化出在鍺基板上製作n^+-p型二極體的熱製程，並且進一步地成功製造出在鍺基板上的n型金氧半場效電晶體。在我們一開始的二極體研究中，我們在光罩上設計不同大小的離子佈值區域之面積去觀察二極體的漏電路徑。藉由總漏電流爲「面積漏電」(J_A)和「邊界漏電」(J_P)兩者所組成的觀念，我們可以定性地了解在對某種製程下的漏電，究竟是被「面積漏電」亦或是「邊界漏電」的分量所主導。除此之外，對於面積漏電和邊界漏電的定量萃取，也展現出和定性上所得的結果有一致的結論，並且我們發現，無論是否在活化前沉積一層SiO_2，沿著離子佈值區域的邊長上之缺陷應該被消除掉，否則將會因嚴重的邊長漏電而導致反向漏電流的增加。然而，即使是這些缺陷被消除的非常好，邊長漏電對於總漏電的比例還是和我們離子佈值區域的大小有關。因此，當我們微縮電晶體的時候，這些沿著源極和汲極(S/D)的邊長分布之缺陷應該要被活化更好。另一方面，我們發現活化前所沉積的SiO_2層的作用是減少Al和Ge間的接觸電阻。因此，較高的順偏電流和較好的汲極飽和電流(drain saturation current)可以被達成。

藉由利用前面所得的活化製程最佳化的結果，我們接下來以高介電參數之介電層

Al_2O_3爲閘極介電層，去製作出以鍺爲基板的n型金氧半場效電晶體，並進一步地研究它們的電性。無論是汲極電流對閘極電壓(I_d-V_g)、汲極電流對汲極電壓(I_d-V_d)和電容對電壓(C-V)的特性，或者是一些電性參數，如：源極和汲極的電阻(source-drain resistance)、載子內擴散長度(dopant in-diffusion length)和次臨界擺幅(sub-threshold swing)也被萃取出來以了解元件的特性。雖然我們可以達到開關電流比(on-off ratio)對於汲極電流和源極電流分別爲 10^3和 10^4，但是嚴重的源極和汲極的電阻仍被觀察到。

最後，我們考慮使用氮氫混合氣體退火(FGA)製程去改善高電阻的缺點。一些參數被萃取出來比較經過氮氫混合氣體退火前後的差異。結果顯示無論是源極和汲極的電阻或者通道電阻(channel resistance)皆可被改善很多。不幸地，二極體接面漏電變得難以控制並且大幅劣化我們的場效電晶體特性。確切的原因應該藉由進一步的物理分析來證實。

Electrical characteristics of n^+-p junction and nMOSFETs on bulk Germanium

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ABSTRACT

We had optimized the thermal processes to form n^+-p junction on bulk Germanium and further succeeded in fabricating Ge nMOSFETs. At the beginning of our diode studies, we designed different areas of implantation region on our masks to observe the leakage paths. By the concept which states total junction leakage currents were composed of J_A and J_P, we could know that the leakage current for certain fabrication process was dominated by "area" or "perimeter" component qualitatively. Besides, an quantitative extraction of J_A and J_P also consisted with these qualitative results, and we found no matter if a capping layer SiO_2 was deposited before annealing, it exhibited defects along the perimeter of implantation region should be eliminated well, or an increasing reverse current would appear due to a severe J_P. However, the ratio of perimeter current to total leakage current was still dependent on the dimension of our implantation area even if the defects were activated very well. Hence, as shrinking the transistors, the defects along the perimeter of S/D should be activated better. In addition, we found the influence of capping layer SiO_2 which was deposited just before activation was to reduce the contact resistance between Al and Ge. Accordingly, a higher forward current and a much improvement on drain saturation current could be achieved.

By utilizing the results of optimization of the activation processes, we subsequently fabricated Ge nMOSFETs with Al_2O_3 as our high-k gate dielectric and further investigated their electrical performances. Not only I_d-V_g, I_d-V_d, and C-V performances, but also some electrical parameters, such as source-drain resistance, dopant in-diffusion length, and

sub-threshold swing, were extracted to realize the device characteristics. Although we could achieve on-off ratios about 10^3 and 10^4 for drain and source currents, respectively, a severe source-drain resistance was also observed.

Finally, we considered the forming gas annealing (FGA) process to improve the drawback. Some parameters were also extracted to compare together before and after FGA. It actually demonstrated not only source-drain resistance but also channel resistance could be much improved. Unfortunately, the junction leakage current became out of control and much degraded the electrical performances on our Ge nMOSFETs. The exact cause should be investigated by some further physical analysis.

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Chapter 1

Introduction

1-1 General Background

In order to keep up with the rapid development of CMOS technology, transistors should be continuously scaled down. This phenomenon is also the famous “Moore’s law”, which states that the number of components per chip doubles roughly every two years [1]. The tendency results from the requirement of better performance (maximize I_{on}) including well-controlled I_{off} and drain induced barrier lowering (DIBL) after one generation; moreover, the most important thing is the decreasing cost per chip. Actually, scaling technology relates to not only the horizontal designs, which is usually limited to lithography abilities, but also the vertical structures. Most shrinking targets could be achieved by the former in the past; or say, the lithography was almost a key point for CMOS technology. However, it became more difficult to accomplish the goal due to the optic limit. In order to improve this, Taiwan Semiconductor Manufacturing Company (TSMC) made its debut in 193 nm immersion lithography technology in 2004 year [2]. This is much valuable to scaling art.

But in the 21st century, we has encountered great bottleneck. According to International Technology Roadmap for Semiconductors (ITRS) 2007 version (Table 1-1), as shrinking the dimensions of the transistors for every technology node, lots of difficult issues should be solved adequately and imminently [3]. One of these problems is that vertical parameters should be also much scaled down with planar designs. For example, if the present gate dielectric, silicon dioxide (SiO_2), still follows the ITRS roadmap, its thickness will less than 1.5nm soon, and an exponentially increasing gate leakage current (tunneling current) will

occur. This not only results in larger power dissipation but degrades the electrical performances under operation. Consequently, to realize a thinner thickness and an acceptable gate leakage current, high-k materials such as ZrO_2, Al_2O_3, and HfO_2 seem like hopeful solutions due to their larger dielectric constants compared to SiO_2 [4-5]. Hence, we can utilize a thicker high-k dielectric film to prevent the tunneling current but with a smaller equivalent oxide thickness (EOT). However, high-k materials own worse interfaces between them and substrates. This may contribute an unacceptable interfacial density of states (D_{it}) and then degrade saturation current by severe carrier scattering. In addition, some high-k materials have unstable chemical properties contrast to SiO_2, and they may also have outstanding inter-diffusion which degrades the performances. Also, a larger dielectric constant is usually related to a narrower energy band gap (E_g) and smaller band offset that perhaps results in a significant Fowler-Nordheim (FN) tunneling, Schottky emission, or Frankel-Poole emission, etc. Hence, it may be required to deposit an interfacial layer which can supply an interface with low D_{it}, an inter-diffusion barrier, and a larger E_g between a high-k dielectric and a Si substrate. But using an interfacial layer, it should have a lower dielectric constant essentially relative to high-k materials, and total EOT would be larger. To improve this, metal gates with much smaller poly depletion and lower resistances become good choices compared to the conventional poly-Si gates. Although metal gates have obvious problems, e.g. thermal budget and the stability with high-k gate dielectrics, they still have enormous potential for the future COMS technology.

Today's thickness of gate dielectric is only tens angstroms (Å), and it will be thinner after scaling. Therefore, how to deposit a high quality ultra-thin film uniformly will also become a significant goal. To achieve this, atomic-layer-deposited (ALD) technique is a research direction [6-7]. As implied by its name, the main mechanism is that only one atomic layer will be deposited per reaction cycle; it's different from the traditional chemical vapor deposition (CVD) which controls the thin film by time or deposition rate. Or more precisely saying, the

growth rate is related to surface reaction kinetics for CVD, but isn't for ALD. The important two things which should be noticed during ALD process are the surface temperature and reactant exposure that must be enough in the chamber for a complete reaction cycle to make sure the reaction can be proceeding everywhere on the substrate. Accordingly, we can just control the number of reaction cycles to accomplish desired thickness precisely by ALD system. On the other hand, the prospects of ALD tech are brightening in the future for dynamic random access memory (DRAM) fabrication involving in three dimensional structures with high aspect ratios.

Besides, to achieve a great improvement on performance, some novel substrate materials have been also researched in recent years. In Table 1-2, it shows lots of properties of semiconductors such as germanium (Ge) and gallium Arsenide (GaAs) which own much higher carrier mobility than Silicon (Si). Because of their high cost, the epitaxy layer of Ge or GaAs on Si will be necessary for manufacture. Moreover, lots of difficult issues must be found suitable solutions. For example, Ge has an intrinsically low melt point and an unstable native oxide compared to Si [8]. Hence, how to keep the high mobility without degrading characteristics and integrate compatible processes with traditional CMOS are the purposes in the future.

All researches about CMOS encounter a revolution for new materials. Maybe Ge-channel and high-k materials with metal gate will become the main stream before long.

1-2 Motivation – Why nMOSFETs on bulk Germanium?

We have known the necessity for the development of new materials so far. One of hopeful research directions is Germanium, which provides excellent carrier mobility and a similar position of band gap to Si. Perhaps this makes Ge more adequate for integrating with conventional processes. Indeed, numbers of references has been published on this topic, and the detailed characters are shown on Table 1-2. By considering the first order approximation of drive current (I_{ds}) at saturation operation, it is given by

$$I_{ds} = \frac{1}{2} C_{ox} \mu \frac{W_{eff}}{L_{eff}} (V_g - V_{th})^2 \quad (1.1)$$

,where C_{ox} is the gate dielectric capacitance per unit area, μ is the carrier mobility, W_{eff} and L_{eff} are the effective channel width and length, respectively, V_g is the applied gate voltage, and V_{th} is the threshold voltage. From this equation, Ge n-type MOSFET should perform a better operating current than p-type MOSFET ideally due to the higher mobility of electrons. However, there are many intrinsic issues of Germanium during processes, and it seems unlikely easy to solve.

The most different thing between Ge and Si is the natures of their native oxides. Unlike SiO_2 with a highly thermal stability, Ge owns an unstable native oxide GeO_x which is solute in H_2O and can be decomposed under 300~400℃ [9]. In addition, as Table 1-2 which shows Ge has a smaller band gap than conventional Si substrate, it will results in a higher junction leakage current proportional to intrinsic carrier concentration n_i (generation current) or n_i^2 (diffusion current). This also implies the formation of source and drain (S/D) junctions will play an important role for the performance of the devices. Actually, p-type dopants for forming p^+-n junction in Ge can be almost completely activated with a low temperature annealing about 550℃. Numbers of researches about pMOSFETs on Ge have been published

and indicated its potential on replacement for traditional Si-based pMOSFETs; however, topics about Ge nMOSFETs are still fewer [10]. The conventional n-type dopants, such as Phosphorus (P) and Arsenic (As), have lower solid solubilities in Ge than in Si. Hence, in order to completely activate these dopants, a higher annealing temperature will be considered. Unfortunately, a relatively low melting point of Ge compared to Si makes the process window much small. Moreover, a higher activation temperature also causes significant dopant loss, junction diffusion, and degrades gate stack integrity [11-14].

On the other hand, it indicates that I_{ds} is also related to parameter C_{ox} from Eq. (1.1), where C_{ox} is determined by gate dielectric constant (ε) and its thickness (d). Because we have mentioned that the thickness should not be thin enough to contribute a tunneling leakage current, a high-k dielectric thin film may the last choice to improve the gate capacitance. In order to achieve high quality thin film with a well controlled thickness, we exploited an ALD system to deposit Al_2O_3 which has a similar band gap and band offset compared with SiO_2. The E_g and band alignment of some dielectric materials respective to Si are shown in Fig. 1-1. In other words, we can obtain a SiO_2-like film but with a higher dielectric constant. Besides, ALD also provides a lower reaction temperature due to its mechanism – self-limiting atomic layer controlled growth [15-16] and avoids excess thermal budget as much as possible.

In brief, the related processes about Ge nMOSFETs have been known. Hence, we tried to fabricate n^+-p junction diodes on bulk Germanium, and furthermore, with these results we would also investigate the Ge nMOSFETs by deposing Al_2O_3 and metal gate Al.

1-3 Organization of this thesis

In chapter 2, we tried to seek adequate annealing conditions for the formation of n^+-p junction on bulk Ge. During the optimization, the sample activated at 500℃ for 30sec was estimated the number of remainder defects inside. Besides, by utilizing the concept which states total junction leakage currents were composed of J_A and J_P, we could know that the leakage current was dominated by "area" or "perimeter" component qualitatively. An quantitative extraction of J_A and J_P also consisted with these results, and we found no matter if a capping layer SiO_2 was deposited before annealing, it exhibited defects along the perimeter of implantation region should be eliminated well, or an increasing reverse current would appear due to a large J_P. However, the ratio of perimeter current to total leakage current was dependent on the dimension of our implantation area even if the defects were activated very well. In addition, we found the influence of capping layer SiO_2 which was deposited just before activation was to reduce the contact resistance between Al and Ge. Hence, a higher forward current could be achieved. Subsequently, we obtained some conditions which presented very similar electrical performances of diodes, and they would be chosen to form source/drain in next chapter. Finally, an ideal value of reverse current was estimated, and it was very close to our results.

In chapter 3, we followed these results of optimization in chapter 2 to form source and drain in our Ge nMOSFETs study. By comparing with the electrical performances of I_d-V_g, I_d-V_d, and some electrical parameters such as source-drain resistance, dopant in-diffusion length, and sub-threshold swing, we tried to consist with our observation. However, it still showed an unacceptable series resistance.

In chapter 4, we considered the FGA process to improve the drawback in pre-chapter. It actually demonstrated both source-drain resistance and channel resistance could be much

improved. Unfortunately, the junction leakage current became out of control and much degraded the electrical performances on our Ge nMOSFETs. Some parameters were also extracted to compare together before and after FGA.

In chapter 5, it gave the conclusions for our studies and some suggestions of the thesis for the future work.

Year of Production	2007	2008	2009	2010	2011	2012	2013
L_g (nm) Physical gate Length	25	22	20	18	16	14	13
EOT (Å) Equivalent oxide thickness	11	9	7.5	6.5	5	5	
Gate poly depletion & inversion layer thickness (Å)	7.4	3.4	2.9	2.8	2.7	2.6	
$J_{g,\ limit}$ (x 100 A/cm²) Max. gate current density	8	9.09	10	11.1	12.5	14.3	
$I_{SD,\ leak}$ (μ A/um) S/D off-state leakage current	0.34	0.71	0.70	0.64	0.74	0.68	
$I_{d,\ sat}$ (x 1000 μ A/um) Effective NMOS drive current	1.211	1.513	1.639	1.807	1.824	1.762	
τ = CV/I (psec) NMOSFET intrinsic delay	0.64	0.55	0.51	0.46	0.43	0.4	

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Table 1-1 ITRS 2007 Process Integration, Devices, and Structures (High-Performance Logic Technology Requirements—Near-term)

Quantity	*Symbol*	*Ge*	*Si*	*InAs*	*InP*	*GaAs*	*GaP*	*GaN*	*(Unit)*
Crystal structure		D	D	Z	Z	Z	Z	W	–
Gap: Direct (*D*) / Indirect (*I*)		*I*	*I*	*D*	*D*	*D*	*I*	*D*	–
Lattice constant	a_0 =	5.64613	5.43095	6.0584	5.8686	5.6533	5.4512	a_0 = 3.189 c_0 = 5.185	Å Å
Bandgap energy	E_g =	0.66	1.12	0.354	1.35	1.42	2.26	3.4	eV
Intrinsic carrier concentration	n_i =	2×10^{13}	1×10^{10}	7.8×10^{14}	1×10^{7}	2×10^{6}	1.6×10^{0}	1.9×10^{-10}	cm^{-3}
Effective DOS at CB edge	N_c =	1.0×10^{19}	2.8×10^{19}	8.3×10^{16}	5.2×10^{17}	4.4×10^{17}	1.9×10^{19}	2.3×10^{18}	cm^{-3}
Effective DOS at VB edge	N_v =	6.0×10^{18}	1.0×10^{19}	6.4×10^{18}	1.1×10^{19}	7.7×10^{18}	1.2×10^{19}	1.8×10^{19}	cm^{-3}
Electron mobility	μ_n =	3900	1500	33,000	4600	8500	110	1500	cm^2/Vs
Hole mobility	μ_p =	1900	450	450	150	400	75	30	cm^2/Vs
Electron diffusion constant	D_n =	101	39	858	120	220	2.9	39	cm^2/s
Hole diffusion constant	D_p =	49	12	12	3.9	10	2	0.75	cm^2/s
Electron affinity	χ =	4.0	4.05	4.9	4.5	4.07	3.8	4.1	V
Minority carrier lifetime	τ =	10^{-6}	10^{-6}	10^{-8}	10^{-8}	10^{-8}	10^{-6}	10^{-8}	s
Electron effective mass	m_e^* =	1.64 m_e	0.98 m_e	0.022	0.08 m_e	0.067 m_e	0.82 m_e	0.20 m_e	–
Heavy hole effective mass	m_{hh}^* =	0.28 m_e	0.49 m_e	0.40	0.56 m_e	0.45 m_e	0.60 m_e	0.80 m_e	–
Relative dielectric constant	ε_r =	16.0	11.9	15.1	12.4	13.1	11.1	8.9	–
Refractive index	$\overline{n}$ =	4.0	3.3	3.5	3.4	3.4	3.0	2.5	–
Absorption coefficient near E_g	α =	10^3	10^3	10^4	10^4	10^4	10^3	10^5	cm^{-1}

- D = Diamond. Z = Zincblende. W = Wurtzite. DOS = Density of states. VB = Valence band. CB = Conduction band
- The Einstein relation relates the diffusion constant and mobility in a nondegenerately doped semiconductor: $D = \mu\,(k\,T / e)$
- Minority carrier diffusion lengths are given by $L_n = (D_n\tau_n)^{1/2}$ and $L_p = (D_p\tau_p)^{1/2}$
- The mobilities and diffusion constants apply to low doping concentrations ($\approx 10^{15}$ cm^{-3}). As the doping concentration increases, mobilities and diffusion constants decrease.
- The minority carrier lifetime τ applies to doping concentrations of 10^{18} cm^{-3}. For other doping concentrations, the lifetime τ is given by $\tau = B^{-1}\,(n+p)^{-1}$, where $B_{GaAs} = 10^{-10}$ cm^3/s and $B_{Si} = 10^{-12}$ cm^3/s.

Table 1-2 Some material parameters of semiconductors at room temperature

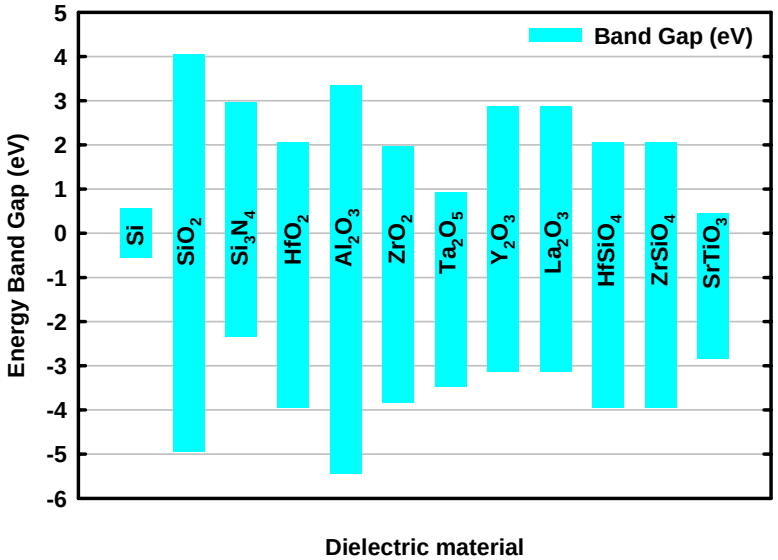


Fig. 1-1 Energy band gap and band alignment of some high-K dielecrics relative to Si

Chapter 2

Optimization of bulk Germanium n^+-p junction

2-1 Introduction

We have known the intrinsic performances of Ge in chapter 1. In order to accomplish nMOSFETs on bulk Ge successfully, the foremost target is to fabricate the n^+-p junction with an acceptable leakage current. Conventional n-type dopants, such as Phosphorus (P) and Arsenic (As), are almost used in Si-based transistors and have high solubilities, insignificant diffusion and especially little dopant loss. However, all of these advantages are gone while Ge substrate is substituted for Si. The primary issue is that P has a relatively lower solubility, which amounts to about 10^{20} cm^{-3}, in Ge than in Si [12-13]. To improve this, a higher implantation dose or a higher activation temperature will be considered. Unfortunately, a higher annealing temperature will give rise to significant diffusion and dopant loss for P in Ge. Besides, the lower melting point of Ge (939℃) than Si (ca. 1400℃) makes the thermal process window more narrow.

In this chapter, P was implanted into bulk Ge to form the n^+ region, and we tried to optimize the thermal budget during activation in order to achieve perfectly electrical performances of the n^+-p junction. Not only activation time and temperature, we also studied if they leaded to different electrical performances for implantation energy at 30keV and 60keV in section 2-3-3. Furthermore, we utilized the analysis of leakage paths to understand where the defects will dominate the leakage current. The detail about the method will be introduced in section 2-3-1. On the other hand, to prevent the dopant loss during activation, we deposited a capping layer SiO_2 before annealing. Its effect will be shown in section 2-3-2.

Besides, we also used the analysis of secondary ion mass spectroscopy (SIMS) and four-point probe system to realize the electrical results. After above experiments, an ideal reverse leakage current will be estimated at last.

2-2 Experimental Procedures

In our diode study, p-type (Gallium (Ga), concentration ~ 2×10^{15} /cm^3) Ge substrates were prepared. After broking a new wafer into adequate size, we cleaned them in diluted HF solution (HF:H_2O = 1:100) and rinsed in deionized (D.I.) water alternately for several cycles. Then we treated them by a HF dip and N_2 drying in order to form an H-bond passivation layer on Ge surface. Furthermore, by using a Plasma Enhanced Chemical Vapor Deposition (PECVD) system we deposited SiO_2 as the field oxide and hard mask for following implantation. Then we defined the implantation region for n-type dopant – Phosphorous (P) – by Mask 1 and etched SiO_2 by Buffer Oxide Etchant (BOE). Next, P was implanted into these samples with dose 2×10^{14} /cm^2 or 1×10^{15} /cm^2 at 30 or 60 keV. Subsequently, samples were activated in N_2 ambient at various temperatures ranging from 500 to 700 ℃ for 30sec, 60sec, or 90sec by a rapid thermal annealing (RTA) system. Besides, the effect of capping 500 Å-thick SiO_2 just before RTA process was also discussed. Then we used Mask 2 to define contact hole and etched SiO_2 till Ge surface was exposed by BOE. Without removing photoresist (P/R) after etching, we continuously used it as lift-off mask, so the samples were directly deposited an aluminum (Al) layer as electrodes by a thermal coater system. Finally, they were proceeded the last step – lift-off – in Acetone solvent (ACE) to remove P/R and define electrodes spontaneously by Ultrasonic Sieving system. The overall fabrication processes of the n^+-p junction were illustrated in Fig. 2-1 with a brief way.

To study the performances of n^+-p junction, we measured the current-voltage (I-V) by HP 4156 system. Furthermore, the information of secondary ion mass spectrometry (SIMS) and the sheet resistance (R_s) of some samples was also considered to consist with the electrical characteristics.

2-3 Results and Discussion

2-3-1 n^+-p junction formation on bulk Ge with different activation temperatures

Fig. 2-2(a) indicates that the electrical characteristics of diodes are as a function of the activation temperature. We found that activation at 700℃, compared with 500℃, obviously contributed to a lower leakage current. This improvement could result from more completed dopant activation with increasing annealing temperature. Furthermore, our electrical performances, compared with some recent publications [17-18], are more excellent due to a leakage current about 10^{-4} A/cm^2 independent on voltage bias till 1 volt can be achieved. It implies the leakage current is dominated by ideal diffusion current, and we can give a hopeful perspective on Ge nMOSFET due to the stable drain leakage current. However, the forward current is actually degraded slightly with a higher annealing temperature as well. Considering the SIMS shown in Fig. 2-2(b), it exhibits samples activated at 700℃ for 30sec accompany more significant dopant diffusion and dopant loss than those at 500℃. Therefore, a lower surface concentration for samples at 700℃ leads to a higher sheet resistance (R_s) shown in Fig. 2-2(c). It seems that the forward current for annealing at 700℃ is degraded because of the higher R_s. But the main reason is not R_s actually. It will be further demonstrated the degradation is related to the contact resistance (R_c) in next section. How to improve it is also the essential topic in Ge nMOSFET fabrication, and a simple method will be introduced in next section, too.

Besides, in order to estimate the number of defects after annealing at 500℃, we considered the equation shown as below.

$$R_s = \frac{1}{\int q\mu(x)n(x)dx}, \tag{2.1}$$

where R_s is the sheet resistance, $n(x)$ is the concentration of the mobile carriers from surface (x = 0) to bulk, q is the magnitude of the electronic charge, and $\mu(x)$ is the carrier mobility. To simplify the condition, we assumed $\mu(x)$ is the same for all cases and independent on x. Finally, it becomes as below.

$$R_s = \frac{1}{q\mu\int n(x)dx} \tag{2.2}$$

Subsequently, we also assumed all the dopants annealing at 700℃ are totally activated, so the total concentration of these carriers ($\int n(x)dx$, unit: #/cm^2) would be 3.47×10^{20} cm^{-2}, which was calculated by integrating the Gaussian form, which is the fitting curve of 700℃, in Fig. 2-3 (SIMS). The detail is shown as below.

$$C(x, t = 30s) = \frac{S}{\sqrt{\pi Dt}}\exp\left\{[-(\frac{x - x_0}{2\sqrt{Dt}})^2]\right\}, \tag{2.3}$$

where C is the SIMS profile, S is the limited source, D is the diffusion coefficient, t is activation time, and x_0 is the position of the peak value.

$$\int_{0nm}^{500nm} 1.354\times10^{18}\times\left\{\exp[-(\frac{x-121.6}{86.2})^2]\right\}dx = 3.474\times10^{20}\ \ (\text{nm}\times\#/\text{cm}^3),$$

where the integration range is from 0 (surface) to 500 nm depth. Because the concentration is almost 1% of the peak value at 500nm, and it has less contribution on this integration. For the case of annealing at 500℃, it is almost box-shaped till 100 nm where is 1% of the peak value. Hence, the integration $\int n(x)dx$ for activation at 500 ℃ becomes just $n_{500}\times100$ (nm×#/cm^3) independent on x. Eq. (2.2) indicates R_s is inversely proportional to $\int n(x)dx$. Finally, we had the relation as below.

$$R_s^{500} : R_s^{700} = 75.74 : 130.3 = \frac{1}{n_{500}\times100} : \frac{1}{3.474\times10^{20}}$$

Hence, n_{500} can be figured out, and it equals 5.98×10^{18} cm^{-3}. We also labeled it in Fig. 2-3

(green dashed line). It means the number of dopants activated at 500℃. Then, to estimate the numbers of defects, we calculated the difference between SIMS profile and n_{500}. The calculation is shown as below.

$$(1.2\times10^{19}-5.98\times10^{18})\times(100nm\times10^{-7})=6.02\times10^{13}cm^{-2}$$

Note this result is base on our assumption which states there is no defect in the case of 700℃. However, the dopants after annealing at 700℃ can't be activated completely in real. Therefore, $6.02\times10^{13}\ cm^{-2}$ is a "minimum" value, and it gives us the sense of the amount of defects under such process condition.

Following, we would discuss the leakage paths of reverse currents in lots of cases. Fig. 2-4 shows the box-shaped implantation region. The dashed line is the space charge edge which is a function of the voltage bias, and defects inside will contribute to a drift leakage current. It implies possible paths of leakage currents can be separated into two main parts – perimeter leakage current density (J_P) and area leakage current density (J_A). The former is almost dependent on surface defects, e.g. between Ge and SiO_2, in the space charge region, and the latter is dependent on bulk defects. Fig. 2-5 shows the electrical characteristics of the n^+-p junction activated at 500℃ for 30sec with various implanted area. Fig. 2-5(a) displays the original data, and it implies the sheet resistance can't be ignored due to the slightly decreasing forward current with the increasing dimension. To understand the paths of reverse leakage currents, original data in Fig. 2-5(a) is divided by ion-implanted area or ion-implanted perimeter, and the results are shown in Fig. 2-5(b) and Fig. 2-5(c), respectively. It can be understood from the total reverse leakage current shown as below.

$$I_R = J_A\times A + J_P\times P\,, \tag{2.4}$$

where I_R is the total leakage current, A is the implanted area, P is the perimeter of A. If I_R is divided by A or P, it will become Eq. (2.5) or Eq. (2.6), respectively.

$$\frac{I_R}{A}\equiv J^A = J_A + J_P\times\frac{P}{A} \tag{2.5}$$

$$\frac{I_R}{P} \equiv J^P = J_A \times \frac{A}{P} + J_P \tag{2.6}$$

Here we assumed J_A and J_P were unknown constants; the ratio of P and A were variable due to three dimensions on our mask. If J_A dominates the total leakage current, namely J_P can be ignored, Eq. (2.5) will result in the same value of J^A no matter which dimension is. Or, if J_P dominates, Eq. (2.6) will show J^P is a constant even through $\frac{A}{P}$ is a variable. By this analytic method, we can quickly figure out which component of leakage current (J_A or J_P) dominates more in quality.

Fig. 2-5(b) indicates there are different leakage currents with various dimensions, but Fig. 2-5(c) gives the opposed result qualitatively. It means that the "perimeter" leakage current is more significant than "area" component obviously. We also used Eq. (2.5) to extract J_A and J_P, and the result was shown in Fig. 2-5(d). The slope and intercept in y-axis relates to J_P and J_A, respectively. Fig. 2-6 also displays samples activated at 600℃ have a similar behavior to those activated at 500℃. On the other hand, it also exhibits that J_A is negative for these two cases, but actually it should be small and positive. Maybe this linear extrapolation method doesn't fit the real behaviors for 500℃ and 600℃ cases as it is close to the intercept of y-axis. But for the case of 700℃, it owns different characteristics in Fig. 2-7. It is obviously that the area leakage current dominates the leakage path, because Fig. 2-7(b) is more "convergent" than Fig. 2-7(c). Hence, the "area" current dominates the total leakage current. At last, the three activation conditions are also plotted together in Fig. 2-8. It reveals J_P can be reduced effectively in Fig. 2-8(b) and contributes to a lower leakage current.

Besides, we also found a smaller dimension would make perimeter current more important.

$$\frac{I_A}{I_P} \equiv \frac{J_A \times a^2}{J_P \times 4a} = \frac{J_A}{J_P} \times \frac{a}{4} \sim a \tag{2.7}$$

Hence, as we shrink the dimension, I_P will more dominate the off-state current. In other words, defects along the perimeter should be eliminated well.

2-3-2 The effect of capping SiO_2 before activation

Fig. 2-9(a) shows the effect of capping SiO_2 on electrical characteristics. Although the reverse currents are almost the same, the forward current is increased much for the sample capped SiO_2 before activation. Furthermore, when we treated the capped sample with a longer activation time till 90sec, the forward current kept the similar behavior, but it degraded the leakage current seriously. The degradation presents that excess of thermal budget may result in precipitates of phosphorous. Therefore, those defects in Ge will give a larger leakage component [12]. Fig. 2-9(b) exhibits the SIMS profiles, and an obvious difference between the samples with and without capping layer near the surface is shown. The phenomenon seems capping SiO_2 can suppress "out-diffusion" during activation due to a higher surface concentration, compared to samples without capping, even if it extends activation time till 90sec. It can be expected that a higher surface concentration should result in a lower sheet resistance. However, when we measured the sheet resistance, it indicated close values in Fig. 2-9(c). In Eq (2.1), R_s is related to the integration of the concentration profile. We attended to the SIMS profile again, and found the peak for the capped samples should have less contribution on the integration which was integrated from surface to junction depth. Accordingly, the improvement of those capped samples is not due to a smaller sheet resistance.

Another possibility of the improvement is that a lower contact resistance (R_c) may be achieved for samples capped SiO_2. Hence, we utilized the R_s data measured by the four-point probe system to reduce a variable and considered the equation shown as below.

$$\begin{aligned} R &= \frac{R_s \times d}{Z} + 2R_c \\ &= R_s \times 1.6 + 2R_c \end{aligned} \tag{2.8}$$

,where R is the total resistance from the measurement of current-voltage (I-V) characteristics by the structure illustrated in Fig. 2-10(a), d and Z are shown in the figure as well, R_s is sheet

resistance, and R_c is contact resistance. The characteristics of I-V are shown in Fig. 2-10(b), and R can be extracted at about 1volt due to the Schottky properties in small voltage bias. By Fig. 2-9(c) and Fig. 2-10(c) (circle symbols) we knew the values of R_s and R, respectively. Hence, R_c can be estimated from Eq. (2.8), and it is plotted together with R in Fig. 2-10(c). Because there are two contacts in our test structure, the total contact resistance is $2R_c$. From Fig. 2-10(c), $2R_c$ contributes a ratio more than fifty percents on total resistance obviously. In other words, the contact resistance dominates the total resistance. More important, it also reveals a smaller R_c can be achieved for the capped samples.

Besides, Fig. 2-11(a~ b) displays the electrical characteristics of the samples capped SiO_2 with various activation temperature ranging from 600℃ to 700℃. We found both the forward and reverse currents were improved with the increasing activation temperature. Comparing to these samples which are no capping layer during annealing in Fig. 2-11(c), the degradation of forward current is observed though it also improves the leakage current with increasing temperature. We contributed this difference to the effect of R_c again. To check it, the relation between R and R_c for some samples above is presented in Fig. 2-12(a), and the details of these conditions are shown in Table 2-1. Then, two things can be observed. First, it displays a similar result which shows $2R_c$ will dominate R no matter what the value of R_s is. Second, decreasing R_c with increasing activation temperature for capped samples may be assigned to their various surface concentrations which lead to different schottky barrier heights (φ_{Bn}). φ_{Bn} will reflect on the specific contact resistances [19]. Hence, the SIMS profiles of the capped samples after annealing at 600 and 700℃ for 30sec are shown in Fig. 2-13(a). We could find these capped samples can prevent dopant loss obviously. Besides, an increasing activation temperature will result in a more severe diffusion. Combining this two effects, more dopant will accumulate near the surface with a higher activation temperature. Finally, the tendency of a decreasing contact resistance with an increasing temperature can be understood for these capped samples. Similarly, because Fig. 2-13(b) exhibits a higher activation temperature

accompanies more significant dopant loss, an opposite relation between annealing temperature and contact resistance in Fig. 2-12 can be realized as well.

As we done in pre-section, it was also extracted J_A and J_P from the conditions in Fig. 2-11(a). We could find the area leakage current would dominate more with increasing activation temperature from Fig. 2-14 to Fig. 2-16. The fitting lines and extracted values are compared in Fig. 2-17(a) and Fig. 2-17(b), respectively. It indicates not only more completed activation leads to smaller values of J_A and J_P, but also an important thing: with the increasing annealing temperature, J_P is reduced about a factor of thirty more than J_A is. Hence, it proves that J_P should be eliminated well during activation to obtain good junction performances again. A similar phenomenon was also observed in some publications [20-21]. Besides, bulk defects due to implantation have been demonstrated that they can be totally activated after annealing at temperatures ranging from 500 to 600℃ [17,22]. It consists with our extracted J_A in Fig. 2-17(b) which exhibits J_A is almost the same from 600 to 700℃. Namely the bulk defects in our studies can be activated well at 600℃. Hence, a much higher annealing temperature we chosen till 700℃ is just for activating those defects along the perimeter of our implantation region. However, a directly physical proof should be checked out.

2-3-3 The effect of different implantation energies and activation times on the electrical characteristics of diodes

We have known some adequate process conditions, such as capping SiO_2 and activation at 700℃, for the formation of n^+-p junction on bulk Ge so far. In order to optimize better, some conditions of implantation energies and activation times were selected to study. In this section, all samples were capping SiO_2 before annealing at 700℃, and Table 2-2 shows the conditions we proceeded. Fig. 2-18(a~b) illustrate the I-V characteristics and sheet resistance of all conditions, respectively. Activation for 30sec or 60sec results in very similar I-V

performances, but it exhibits the same degradation on leakage currents for a longer activation time till 90sec no matter which implantation energy is chosen. This degradation may result from excess of thermal budget that will result in P precipitates we mentioned before. The precipitates should be distributed from surface to a depth less than 100nm due to the SIMS profile in Fig. 2-9(b) which shows a peak at this range [12]. Then, Fig. 2-18(b) gives us the brief picture. Because the precipitates are close to the Ge surface relatively to the junction depth, which is estimated over 400nm at least, a much larger "perimeter" leakage current will be introduced due to those precipitates in the space charge region. It can consist with Fig. 2-21 and Fig. 2-24, which show J_P will become larger after activation for 90sec. That may be why the reverse current degrades after higher thermal budget.

The sheet resistance demonstrated in Fig. 2-18(c) only relates to the implantation energy, but not relates to the activation time. Furthermore, there are smaller sheet resistances for the samples at implantation energy of 60keV than 30keV, and it also responds to the forward current slightly. We attributed this to a deeper junction for implantation energy of 60keV, and it might result in a smaller R_s due to Eq. (2.1). On the other hand, it shows the study about the paths of leakage currents from Fig. 2-19 to Fig. 2-24 again. Instead of activation for 90sec we mentioned above, it could be found the performances for activation time of 30sec and 60sec for both implantation energies were very similar. All of the four conditions exhibit "area" leakage current dominates the leak qualitatively. Of course, the condition of activation for 90sec is not suitable for our purposes of fabricating devices due to its increased leakage current. Hence, we only considered the conditions of annealing for 30sec and 60sec and plotted their figures (d) together in Fig. 2-25(a). J_A and J_P are extracted and illustrated in Fig. 2-25(b). Integrating the qualitative and quantitative results, it shows that these four conditions are almost undistinguishable.

At last we estimated the ideal leakage current and compared with our results. Considering the equations as below:

$$J = J_p + J_n = J_s \times \left[e^{\frac{qV}{kT}} - 1 \right] \tag{2.9}$$

$$J_s \equiv \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \tag{2.10}$$

, where J is the diffusion current density ideally, J_p (or J_n) are the minority hole (or electron) current density which diffuses from p-region to n-region (or n-region to p-region), and J_s is the saturation current density. In Eq. (2.10), p_{no} and n_{po} are the equilibrium hole density in the n-region and electron densities in the p-region, respectively; L and D are the minority carrier diffusion length and diffusion coefficient, and the indexes in Eq. (2.10) mean which the region is (n or p). We also used those relation, $p_{no} = \frac{n_i^2}{N_d}$, $n_{po} = \frac{n_i^2}{N_a}$, $D = \frac{kT}{q}\mu$, $L = \sqrt{D\tau}$, to substitute Eq. (2.10). Then we could calculate it as below.

$$\begin{aligned} J_s &= qn_i^2 \left[\frac{1}{N_d} \sqrt{\frac{\mu_p}{\tau_p} \times \frac{kT}{q}} + \frac{1}{N_a} \sqrt{\frac{\mu_n}{\tau_n} \times \frac{kT}{q}} \right] \\ &= (1.6 \times 10^{-19})(2.4 \times 10^{13})^2 \left[\frac{1}{10^{18}} \sqrt{\frac{1900}{8.6 \times 10^{-7}} \times 0.0259} + \frac{1}{2 \times 10^{15}} \sqrt{\frac{3900}{1.87 \times 10^{-5}} \times 0.0259} \right] \\ &\approx 1.07 \times 10^{-4} \quad (\mathrm{A/cm^2}) \end{aligned}$$

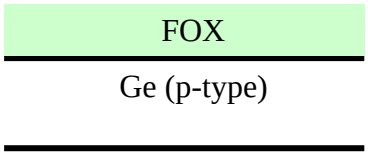
From Eq. (2.9), it hints the reverse diffusion current J_R should be equal: $-J_s$. Comparing our best performances shown in Fig. 2-17(a) to the value J_s we estimated above, the ratio of them is $\frac{J_s(ours)}{J_s(estimated)} \approx 2$. And ours diodes reach a ratio of $\frac{J(forward)}{J(reverse)}$ about $10^{4.7}$.

2-4 Summary

We have fabricated the n^+-p diodes on bulk Germanium successfully, and a reverse current about $2\times10^{-4}\,A/cm^2$ very close to our estimated ideal value about $1\times10^{-4}\,A/cm^2$ can be achieved. We also estimated the number of defects for samples annealing at 500℃. It gives an order of $10^{13}\,cm^{-2}$. Besides, the most important thing in our studies is the analysis of paths of the leakage current. No matter if capping SiO_2 before activation, we could find the total leakage current was dominated by the "perimeter" component for activation at 500 and 600℃. With an increasing temperature, it shows an interesting tendency which exhibits the area leakage current becomes more dominant than perimeter component till 700℃. Not only the qualitative analysis, we also extracted the values of J_A and J_P. It is demonstrated that the elimination of perimeter defects which lead to a large value of J_P is the target of activation. In other words, we should eliminate those defects along the perimeter of implantation region effectively. Besides, the capping effect on the I-V performances of diodes is investigated in our studies. It displays a smaller contact resistance will be obtained if a SiO_2 thin film is deposited before activation. In addition, samples with capping SiO_2 will get a decreasing contact resistance with an increasing activation temperature from 600 to 700℃. This behavior is opposite to samples without capping layer. The phenomenon can be attributed to their different surface concentrations which lead to various energy barrier heights. We also treated implantation energies of 30keV and 60keV, but similar performances were displayed. First, activation for 90sec displays a higher leakage current whatever the implantation energy is chosen. We applied this to the formation of P precipitates which are very close to the Ge surface. Hence, a large perimeter current occurs. Second, implantation energies of 30keV and 60keV with further activation for 30sec or 60sec present identically electrical performances. And a ratio of forward to reverse current about 5×10^4 at ±1 volt can be achieved.

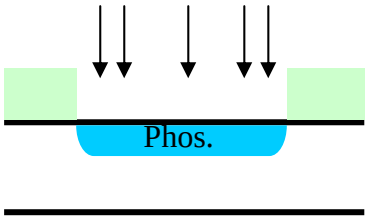
A. Wafer cleaning (HF:H_2O = 1:100)

Deposit Field Oxide by PECVD

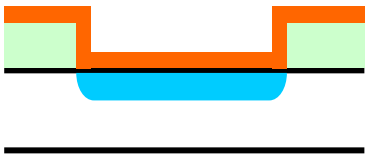


B. Define n^+-region (1^{st} mask)

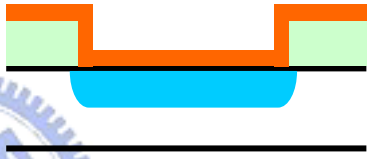
Implantation (Phos.)



C. Some samples are capped SiO_2. (PECVD)



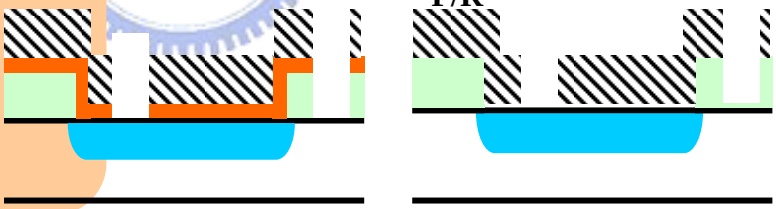
D. Dopant activation (500 ~ 700℃)



E. Define contact hole (2^{nd} mask)

Etching SiO_2 by BOE

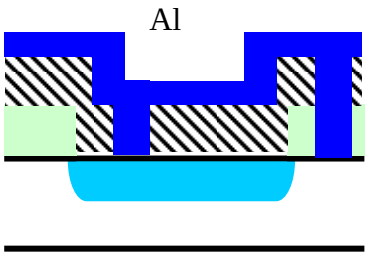
Without remove P/R



(Capped SiO_2) (Uncapped SiO_2)

F. Al deposition (thermal coater)

(Illustration by uncapped samples)



G. Lift-off to define Al pattern in ACE

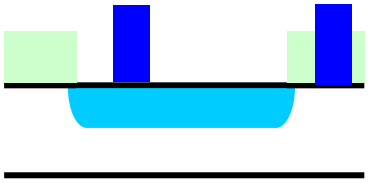
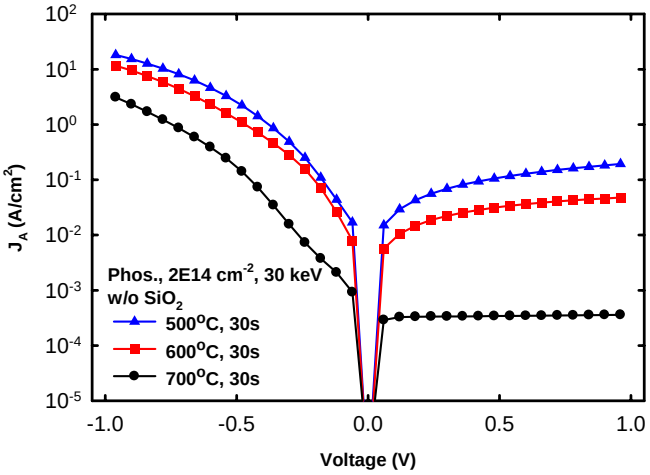
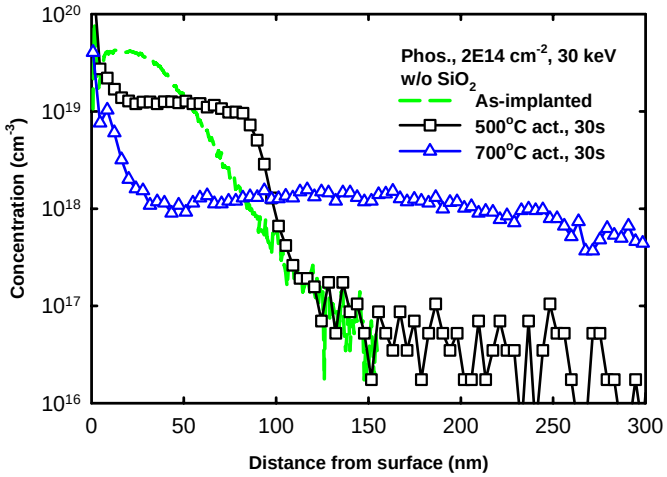


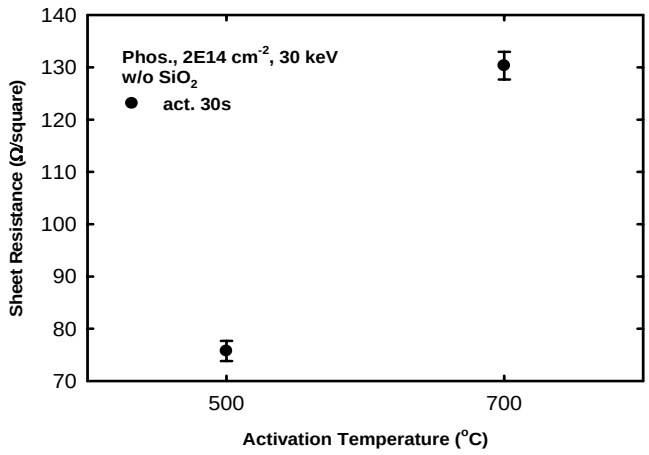
Fig. 2-1 n^+-p junction fabrication flow chart



(a)



(b)



(c)

Fig. 2-2 (a) The J_A-V performances of diodes activated at 500 to 700℃ for 30sec. (b) and (c) are the measurement of SIMS and R_s, respectively. Note the samples are not capped SiO_2 before annealing.

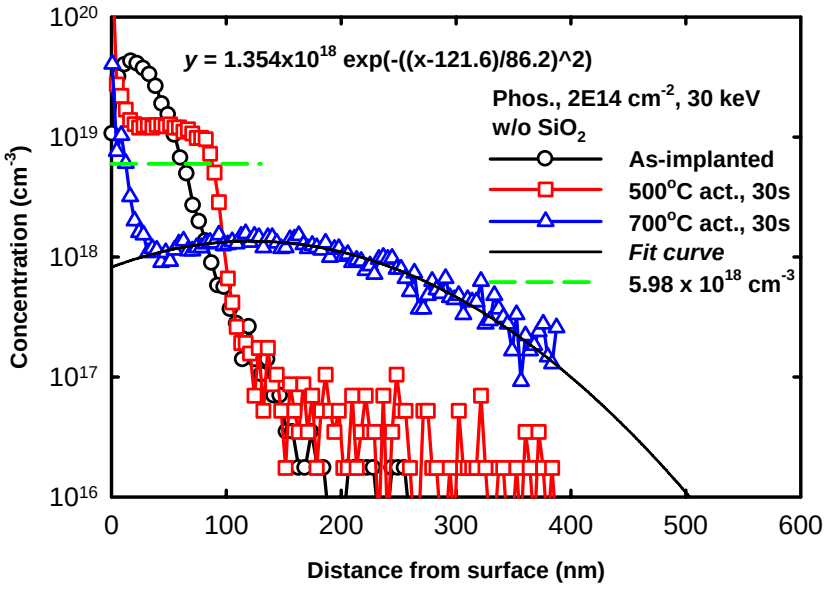


Fig. 2-3 It shows the fitting line of activation at 700℃ (solid curve) and an estimated activation level after annealing at 500℃ (green dashed line). Note the samples are not capped SiO_2 before annealing.

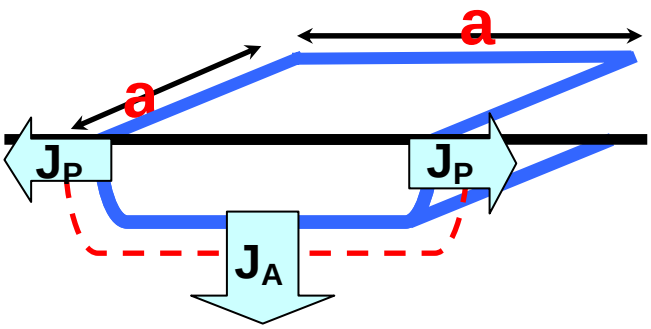
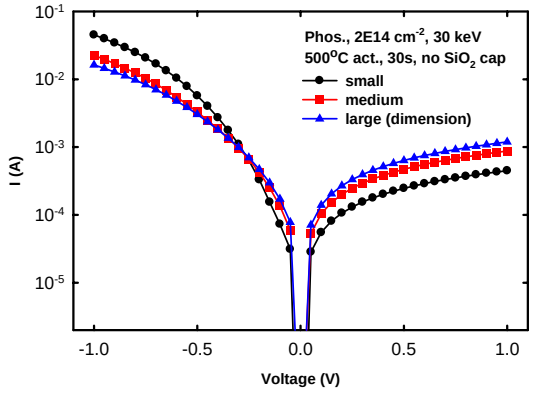
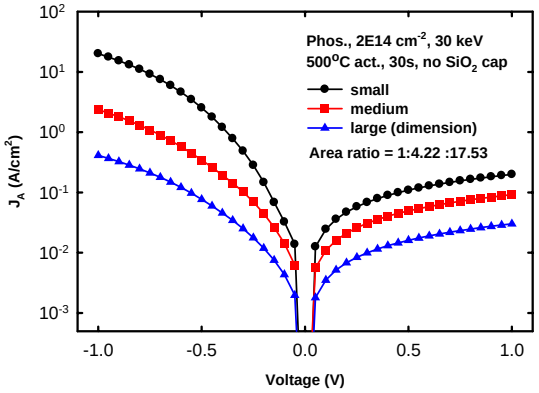


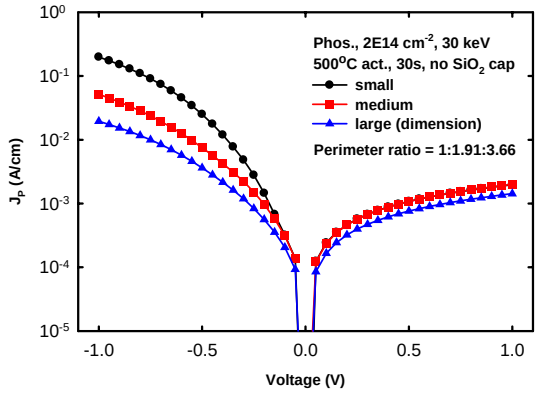
Fig. 2-4 This picture illustrates the paths of junction leakage currents. The box-shaped is the implantation region of Phosphorus with a perimeter of ***a****. The dashed line is the edge of space charge region, and defects inside will contribute to a drift leakage current. We separated the current into two main parts, J_A and J_P.*



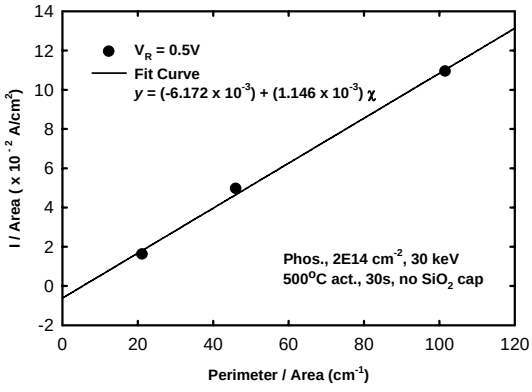
(a)



(b)



(c)



(d)

Fig. 2-5 (a) The I-V characteristics of junctions activated at 500℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "perimeter current" dominates the leakage current qualitatively. (d) It shows the extracted J_A and J_P quantitatively. Note the samples are not capped SiO_2 before annealing.

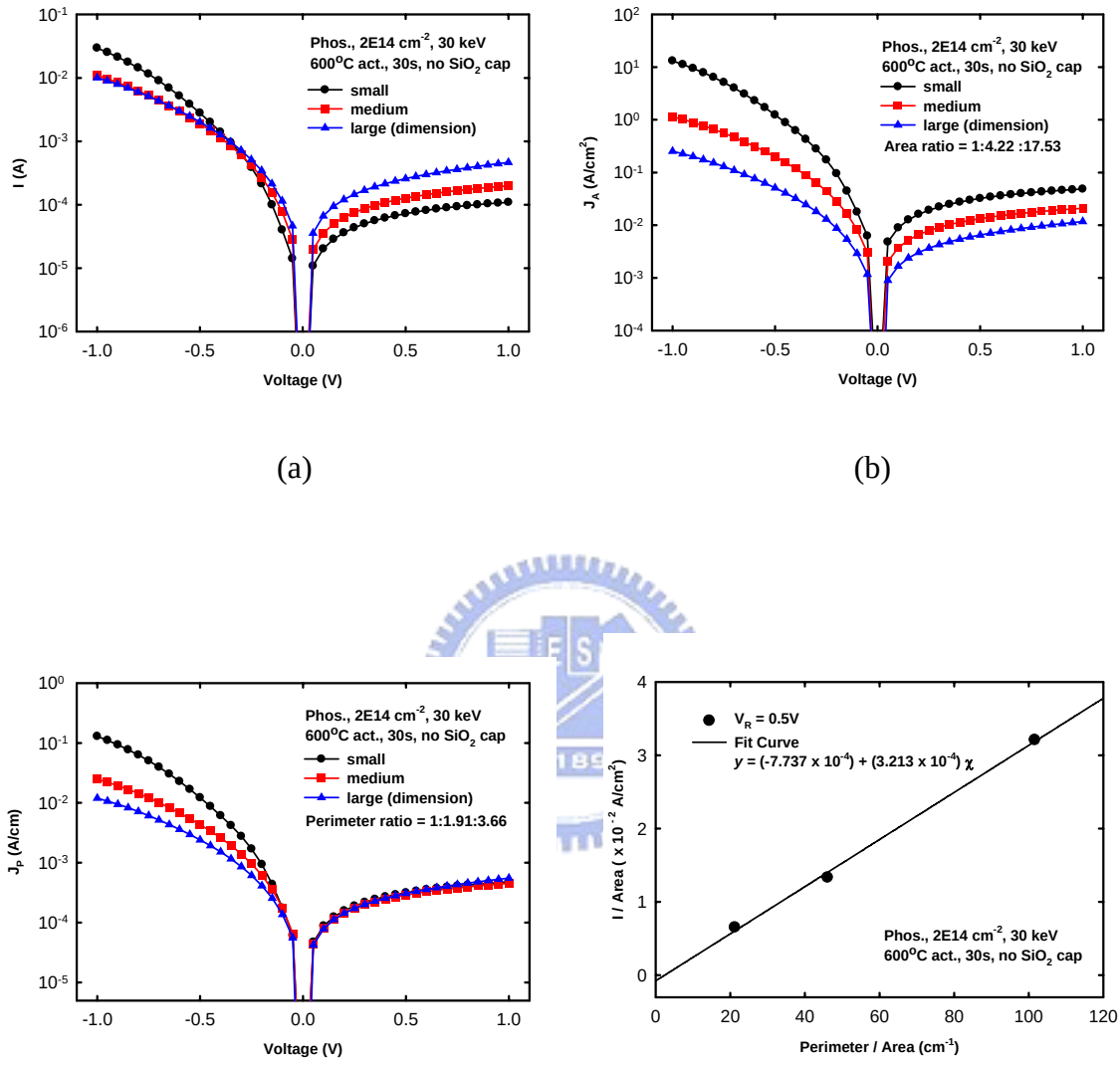
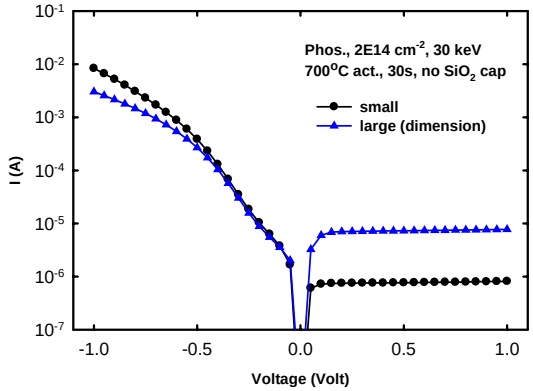
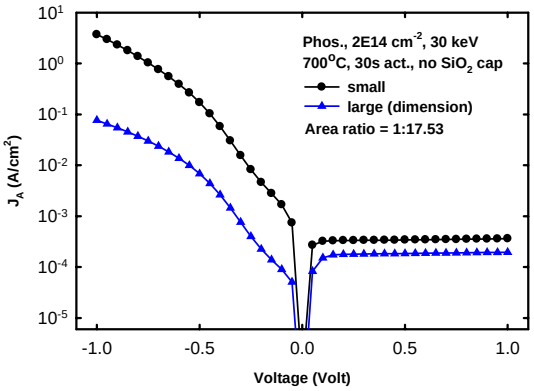


Fig. 2-6 (a) The I-V characteristics of junctions activated at 600℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "perimeter current" dominates the leakage current qualitatively. (d) It shows the extracted J_A and J_P quantitatively. Note the samples are not capped SiO_2 before annealing.



(a)



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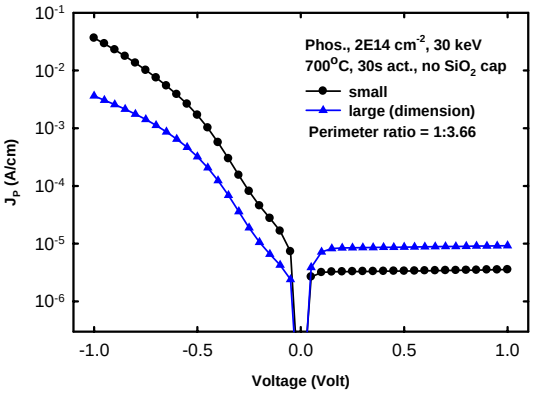
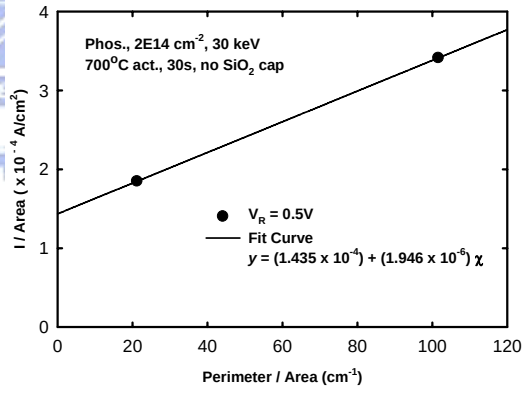
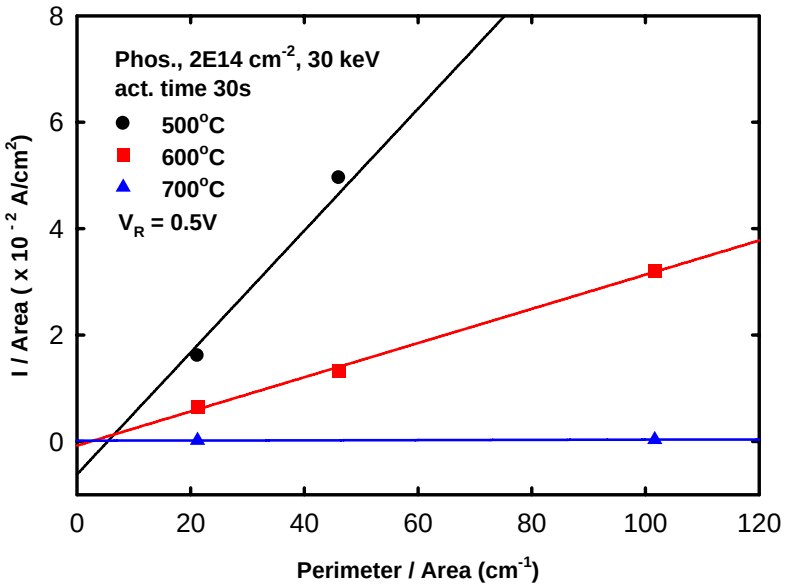


(c)

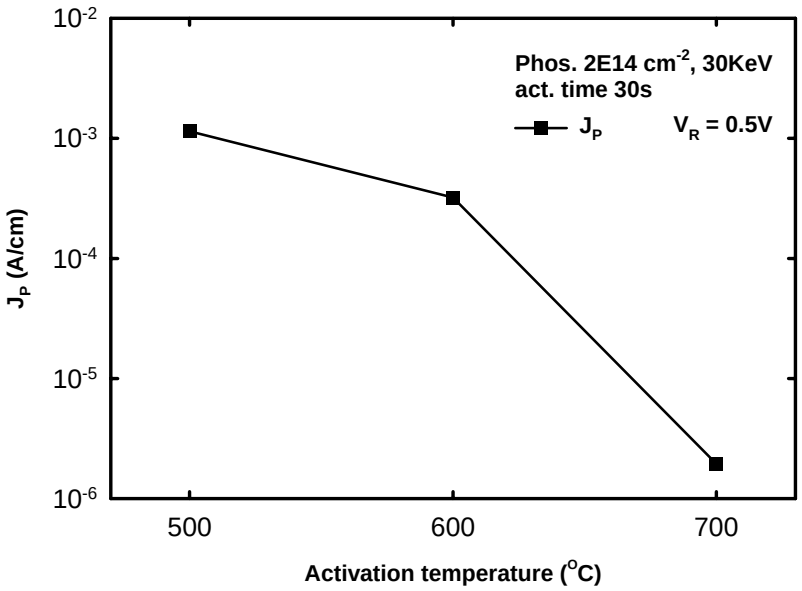


(d)

Fig. 2-7 (a) The I-V characteristics of junctions activated at 700℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates the leakage current qualitatively. (d) It shows the extracted J_A and J_P quantitatively. Note the samples are not capped SiO_2 before annealing.

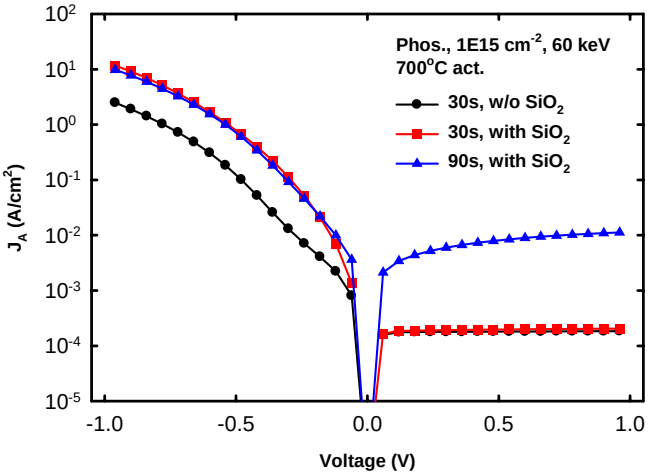


(a)

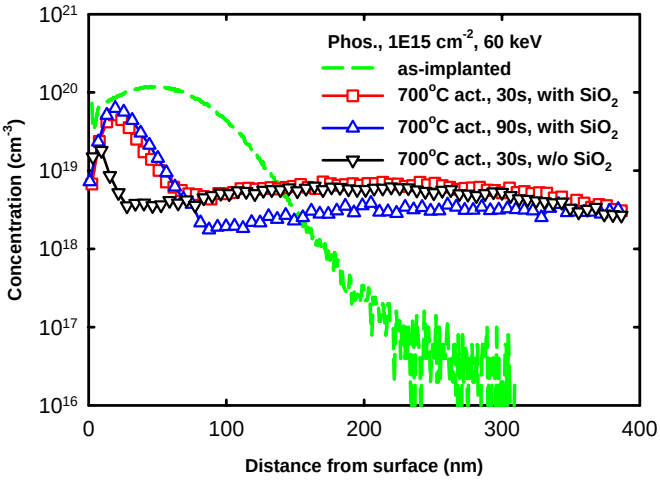


(b)

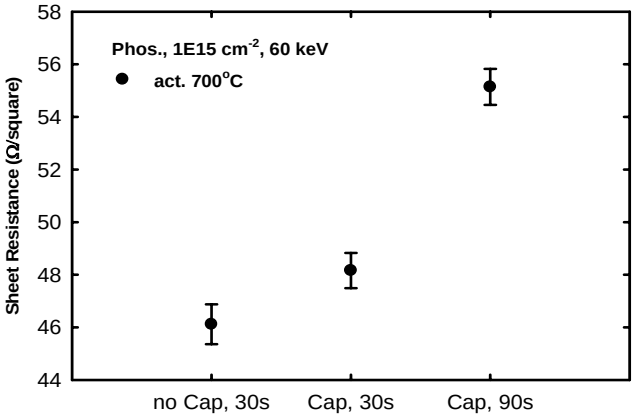
Fig. 2-8 (a) The comparison of the leakage current at various activation temperatures. It is plotted by combining Fig. 2-5(d), Fig. 2-6(d), and Fig. 2-7(d) together. (b) The extracted J_P from (a) decreases with the increasing activation temperature.



(a)

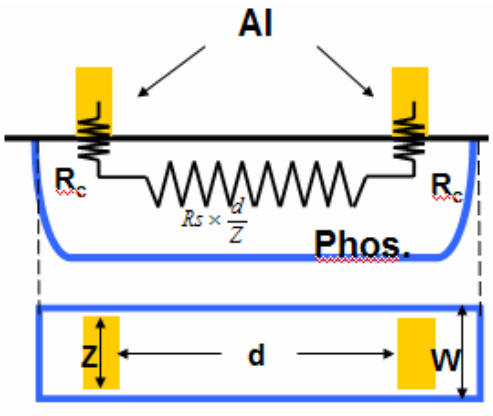


(b)

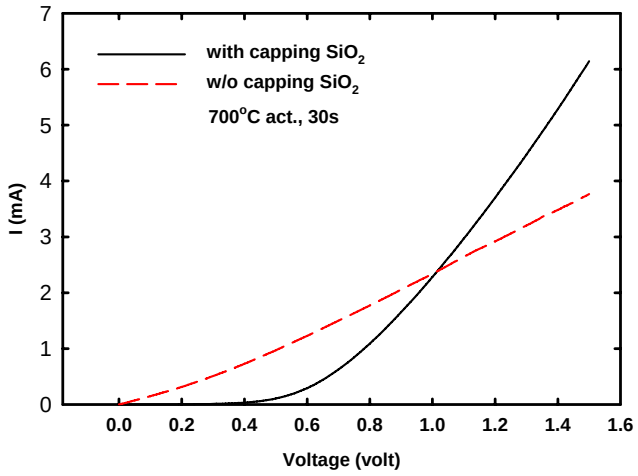


(c)

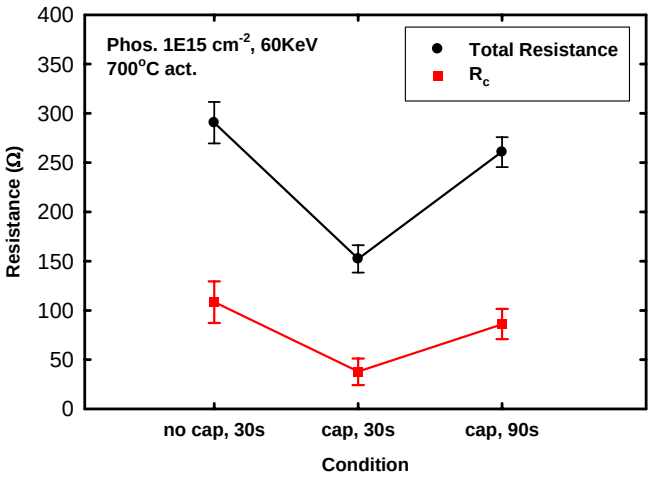
Fig. 2-9 (a) It exhibits the J_A-V performances of diodes activated with or without capping layer SiO_2. (b) and (c) are the measurement of SIMS and R_s, respectively.



(a)

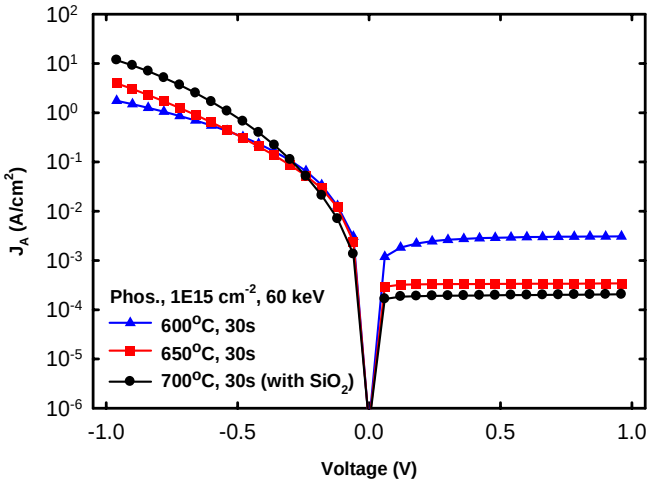


(b)

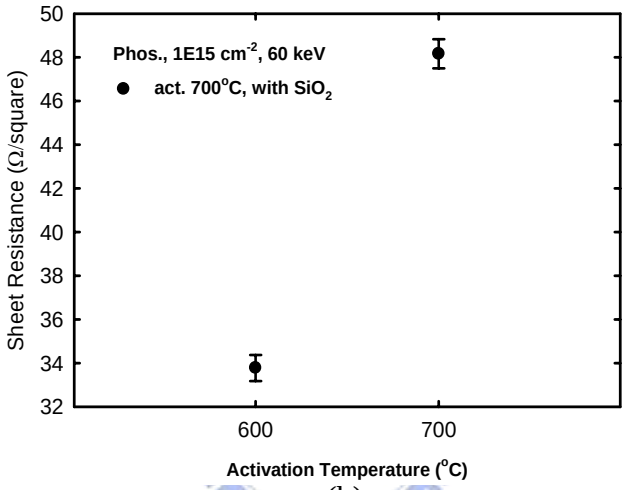


(c)

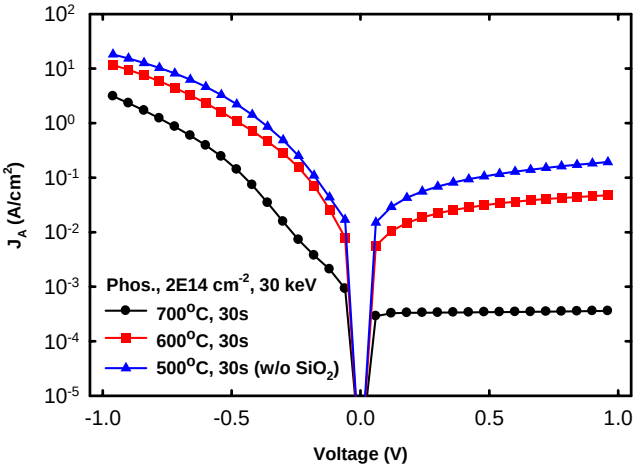
Fig. 2-10 (a) The test structure is utilized to extract the contact resistance. The upper and lower pictures are the profile and top view of this structure. (Z = 100 um, d = 160um) (b) The I-V characteristics of the test structure with or without capping layer. (c) The extracted total resistance from (b) and calculated R_c are plotted together.



(a)



(b)



(c)

Fig. 2-11 (a) The J_A-V performances of diodes activated at 600 to 700℃ for 30sec. Note the samples are capped SiO_2 before annealing. (b) It is the measurement of R_s. (c) The J_A-V performances of diodes activated at 500 to 700℃ for 30sec. Note the samples are not capped SiO_2 before annealing.

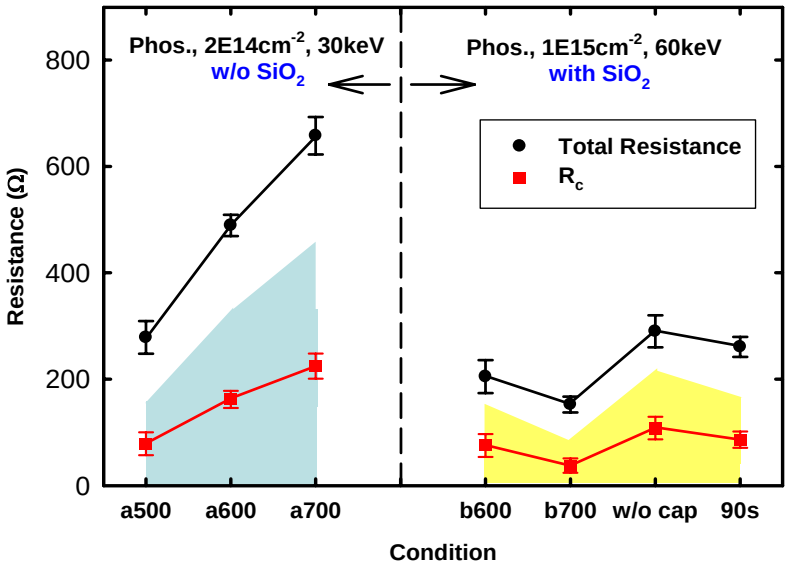
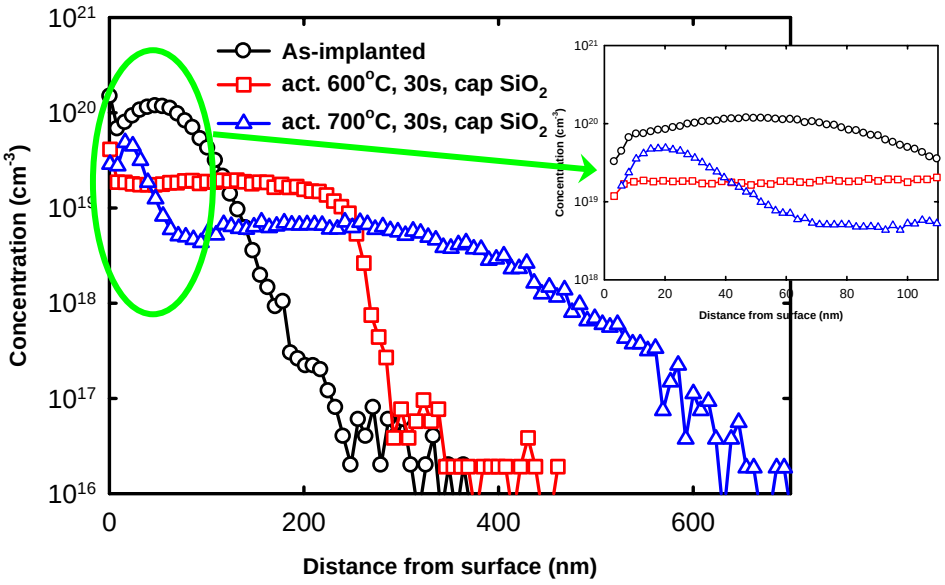


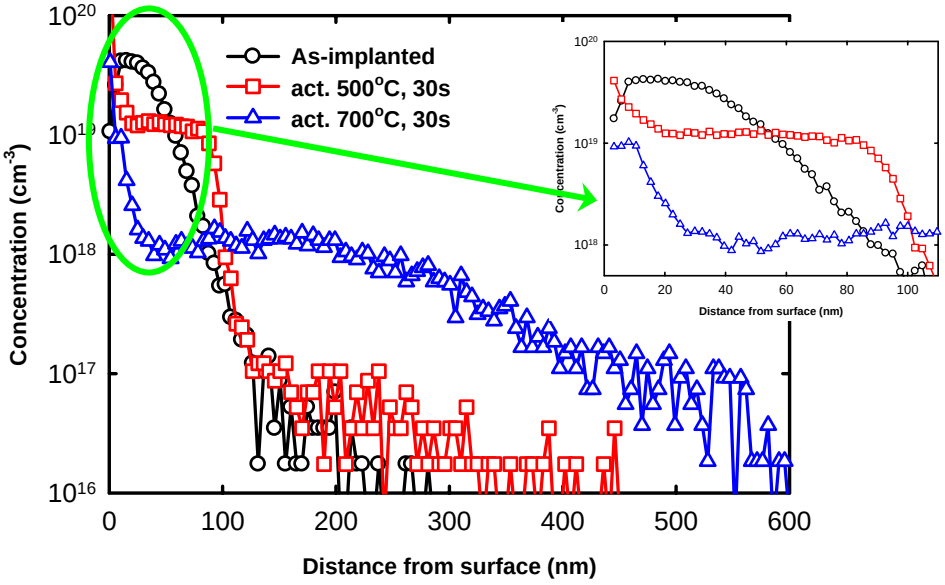
Fig. 2-12 The extracted total resistance and calculated contact resistance are plotted together. The details of those labels are shown in Table. 2-1.

condition	Implantation (cm^{-2}, eV)	Act. Temp.(℃)	Cap SiO_2
a500	2E14, 30K	500	X
a600	2E14, 30K	600	X
a700	2E14, 30K	700	X
b600	1E15, 60K	600	O
b700	1E15, 60K	700	O
w/o cap	1E15, 60K	700	X
b90s	1E15, 60K	700	O

Table 2-1 The details of those labels in Fig. 2-12.



(a)



(b)

Fig. 2-13 (a) and (b) are t*he profiles of SIMS for samples with and w/o capping SiO_2 before annealing, respectively. Samples in (a) are activated at 600 or 700℃ for 30sec. Samples in (b) are activated at 500 or 700℃ for 30sec.*

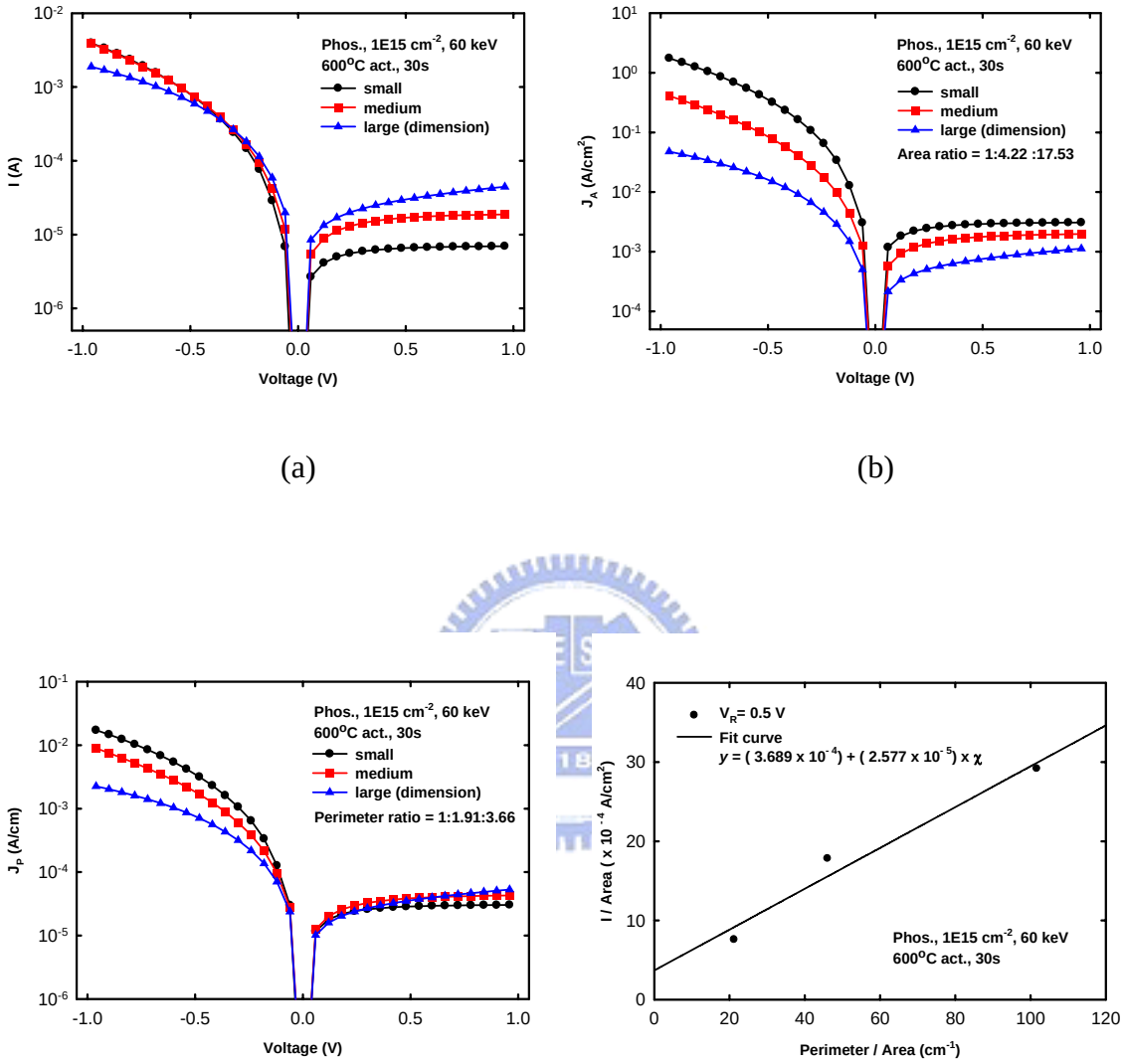


Fig. 2-14 (a) The I-V characteristics of junctions activated at 600℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "perimeter current" dominates the leakage current qualitatively. (d) It shows the extracted J_A and J_P quantitatively. Note the samples are capped SiO_2 before annealing.

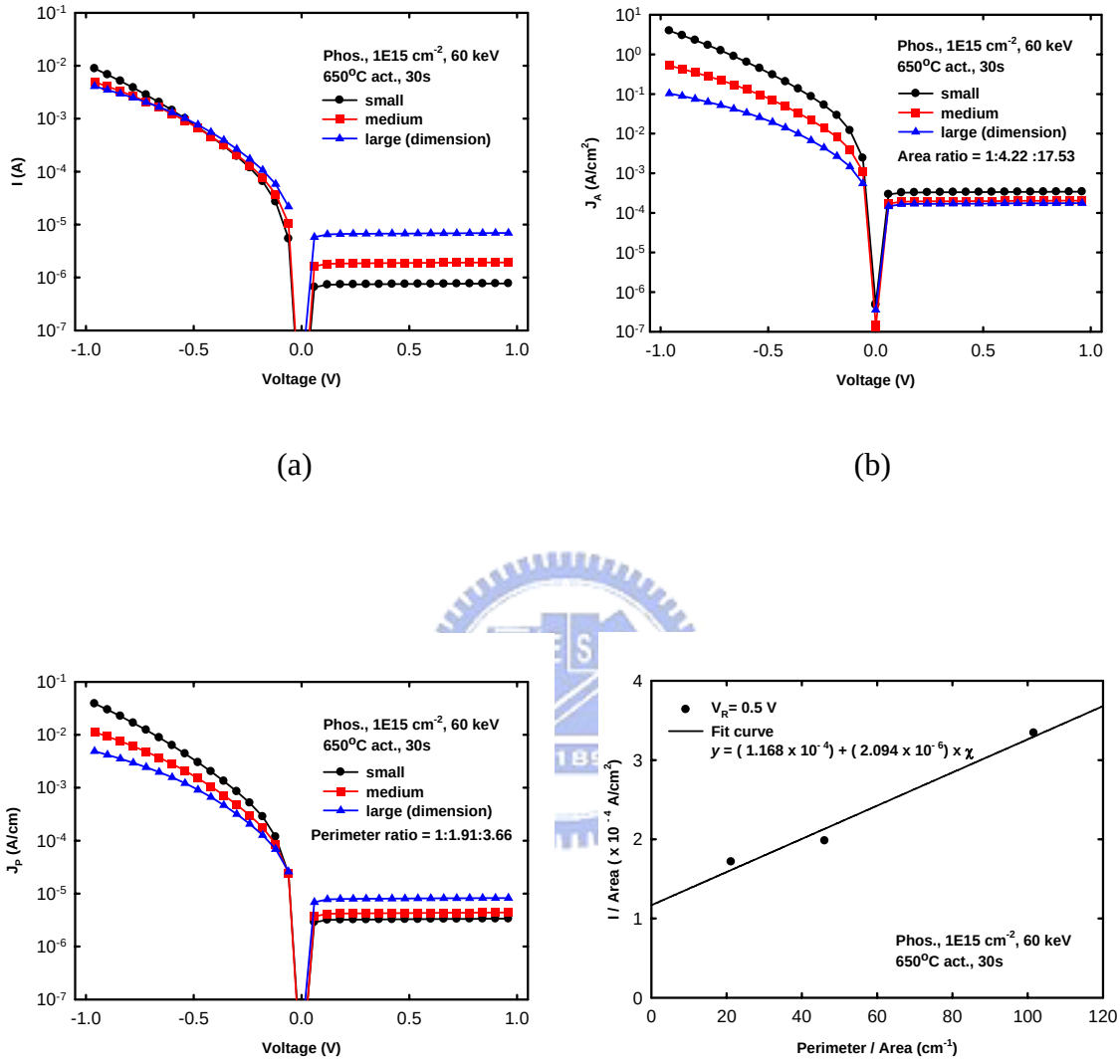


Fig. 2-15 (a) The I-V characteristics of junctions activated at 650℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates the leakage current qualitatively. (d) It shows the extracted J_A and J_P quantitatively. Note the samples are capped SiO_2 before annealing.

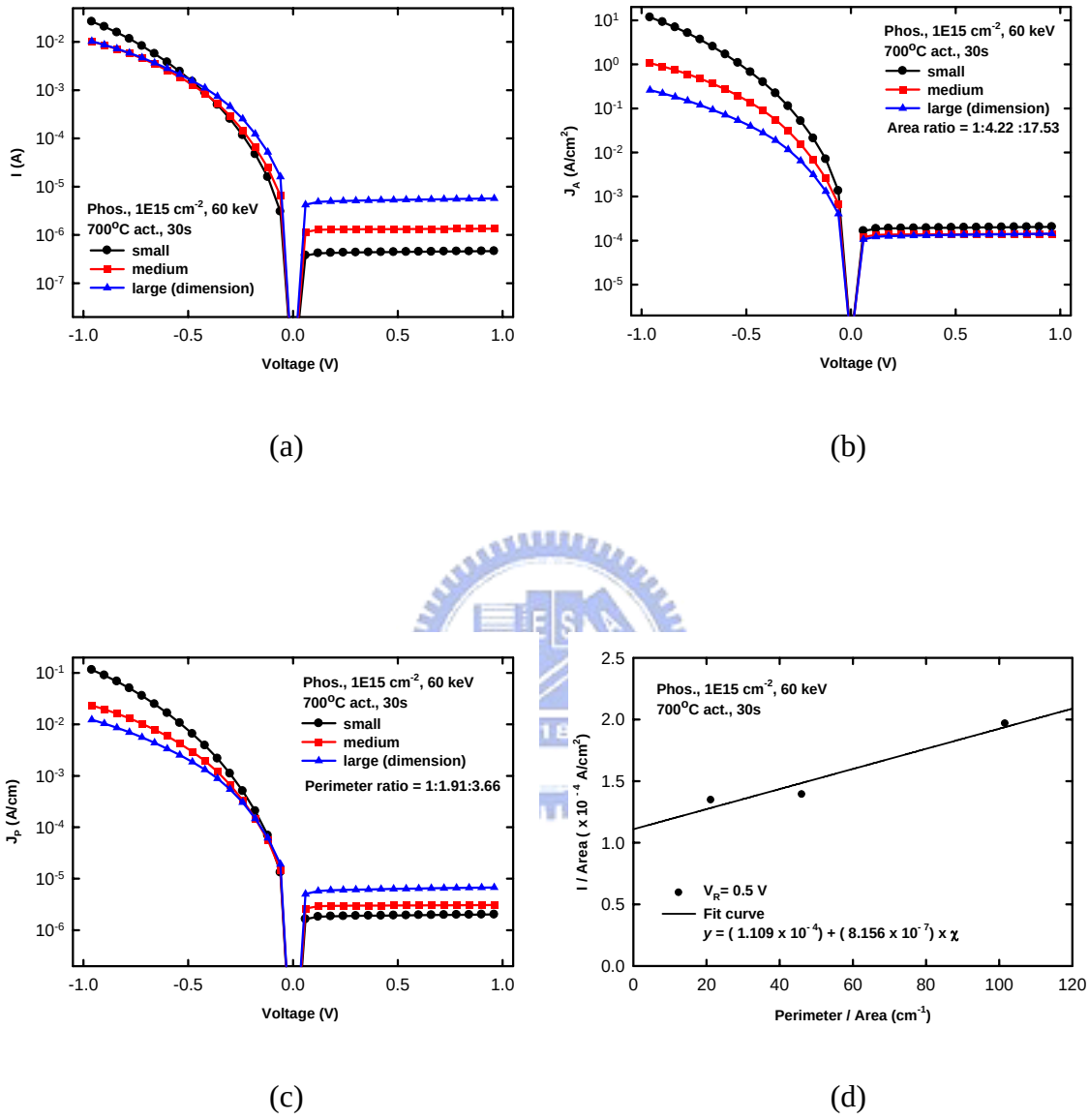
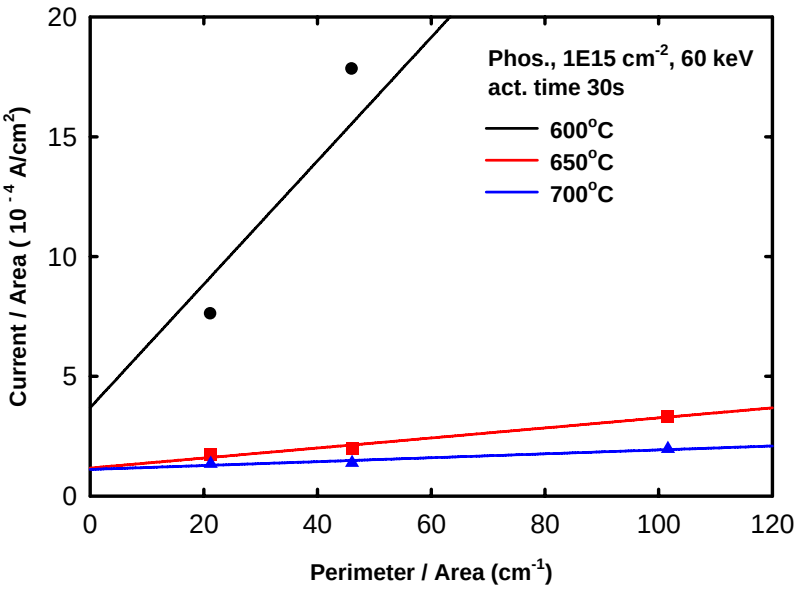
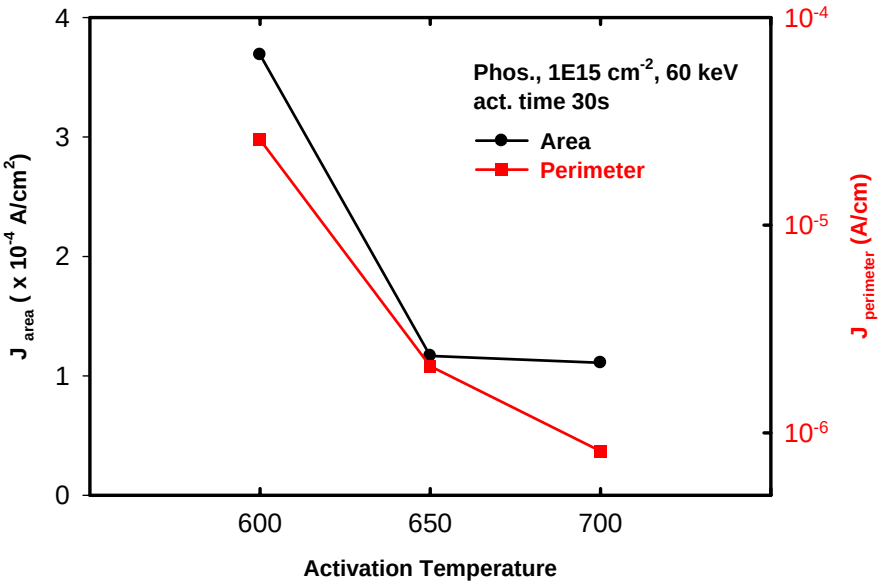


Fig. 2-16 (a) The I-V characteristics of junctions activated at 700℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates the leakage current qualitatively. (d) It shows the extracted J_A and J_P quantitatively. Note the samples are capped SiO_2 before annealing.



(a)



(b)

Fig. 2-17 (a) The comparison of the leakage current at various activation temperatures. It is plotted by combining Fig. 2-14(d), Fig. 2-15(d), and Fig. 2-16(d) together. (b) The extracted J_P and J_A from (a) decreases with the increasing activation temperature.

	(O)	(O)	(X)	(O)	(O)	(X)
Implant Energy (keV) (1E15cm^{-2})	30	30	30	60	60	60
Activation time (s) (700°C)	30	60	90	30	60	90

Table 2-2 The conditions of various implantation energy and activation time we chosen.

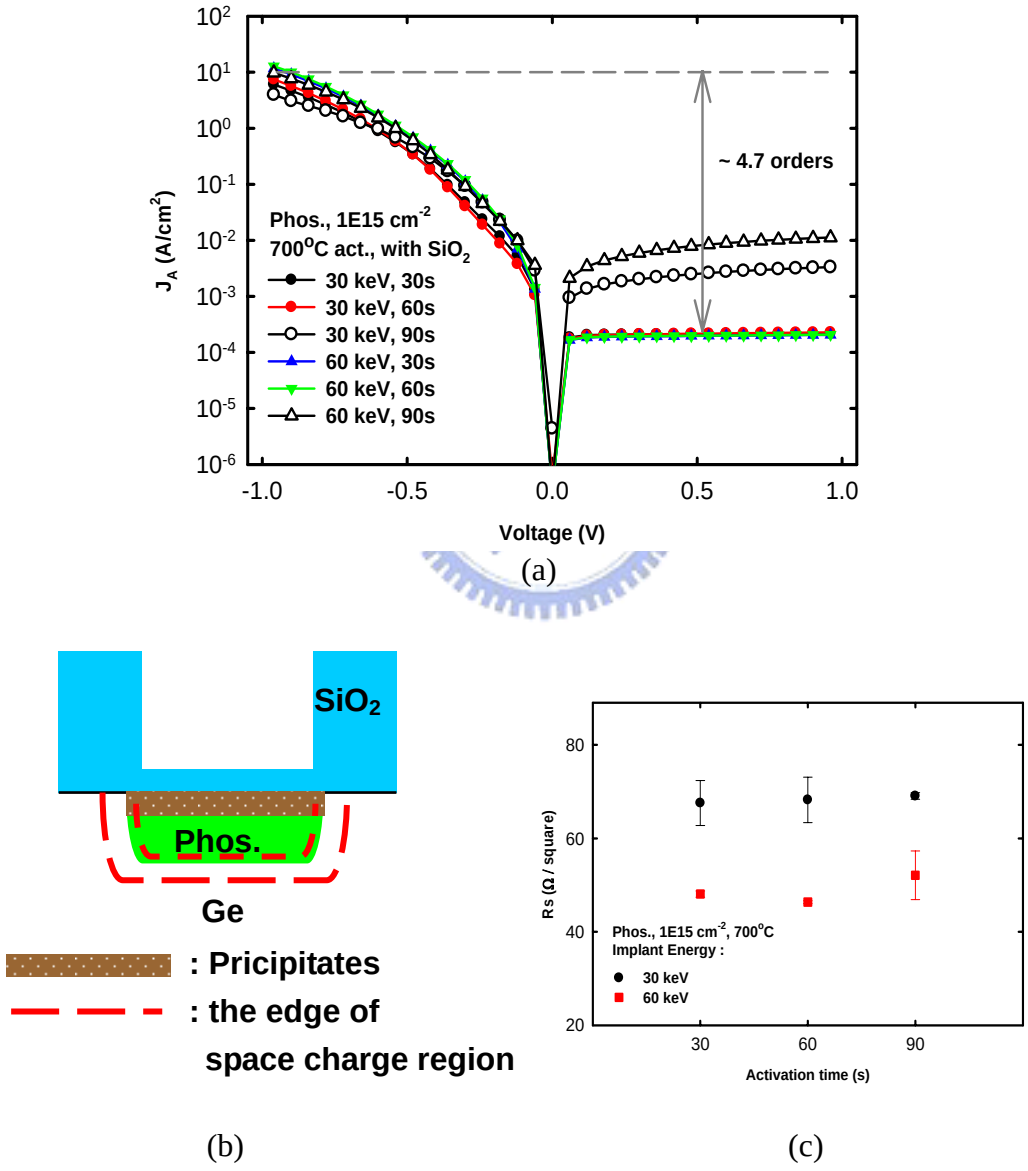
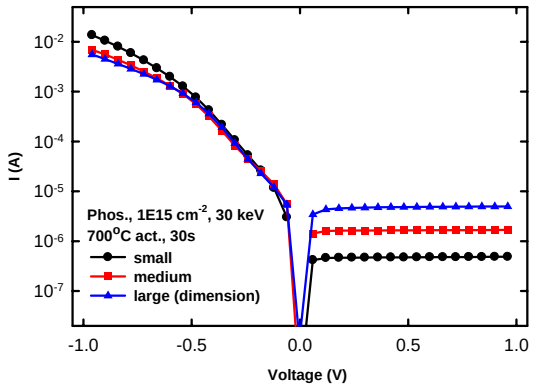
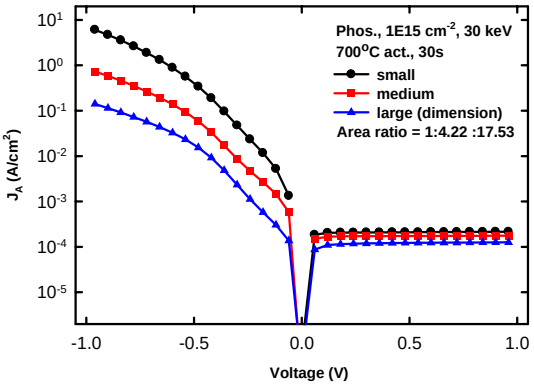


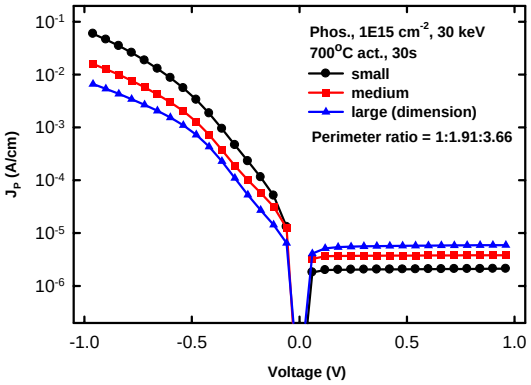
Fig. 2-18 (a) and (c) are the J_A-V characteristics and sheet resistance of six samples in Table. 2-2. (b) A picture shows "perimeter" leakage current induced by Phosphorus precipitates.



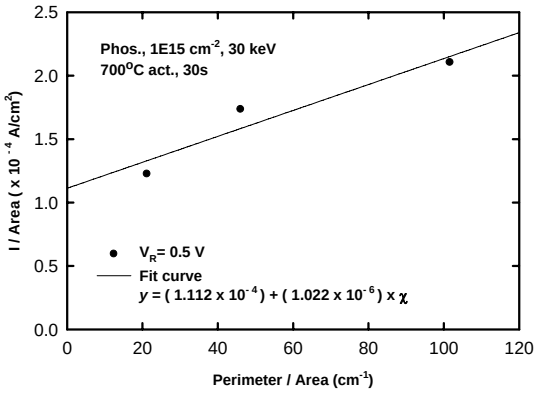
(a)



(b)

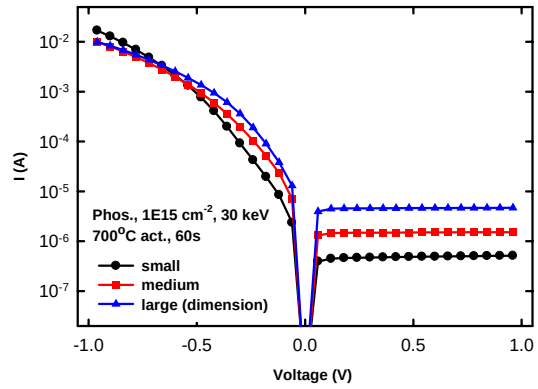


(c)

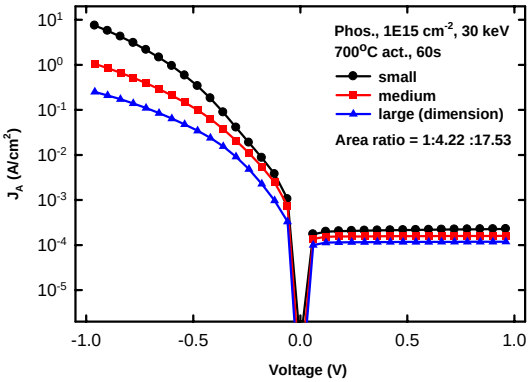


(d)

Fig. 2-19 (a) The I-V characteristics of junctions which were treated implantation energy of 30keV and activated at 700℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates the leakage current qualitatively. (d) It shows the fitting curve for extracting J_A and J_P quantitatively.



(a)



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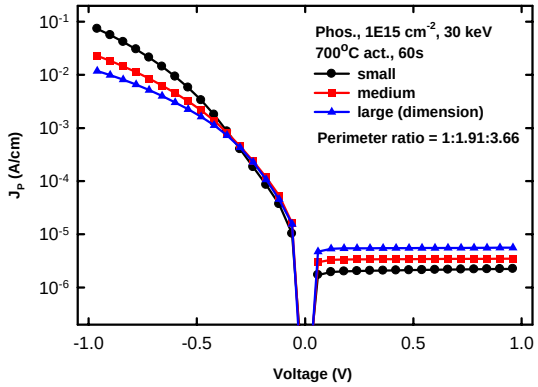
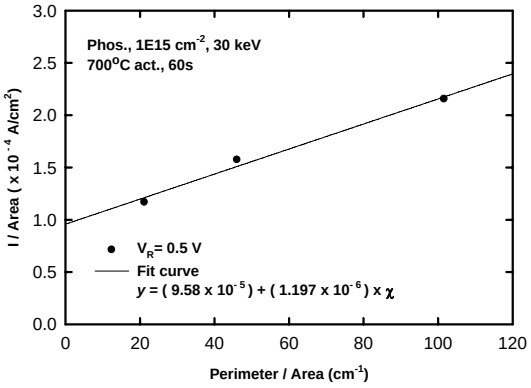


(c)



(d)

Fig. 2-20 (a) The I-V characteristics of junctions which were treated implantation energy of 30keV and activated at 700℃ for 60sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates the leakage current qualitatively. (d) It shows the fitting curve for extracting J_A and J_P quantitatively.

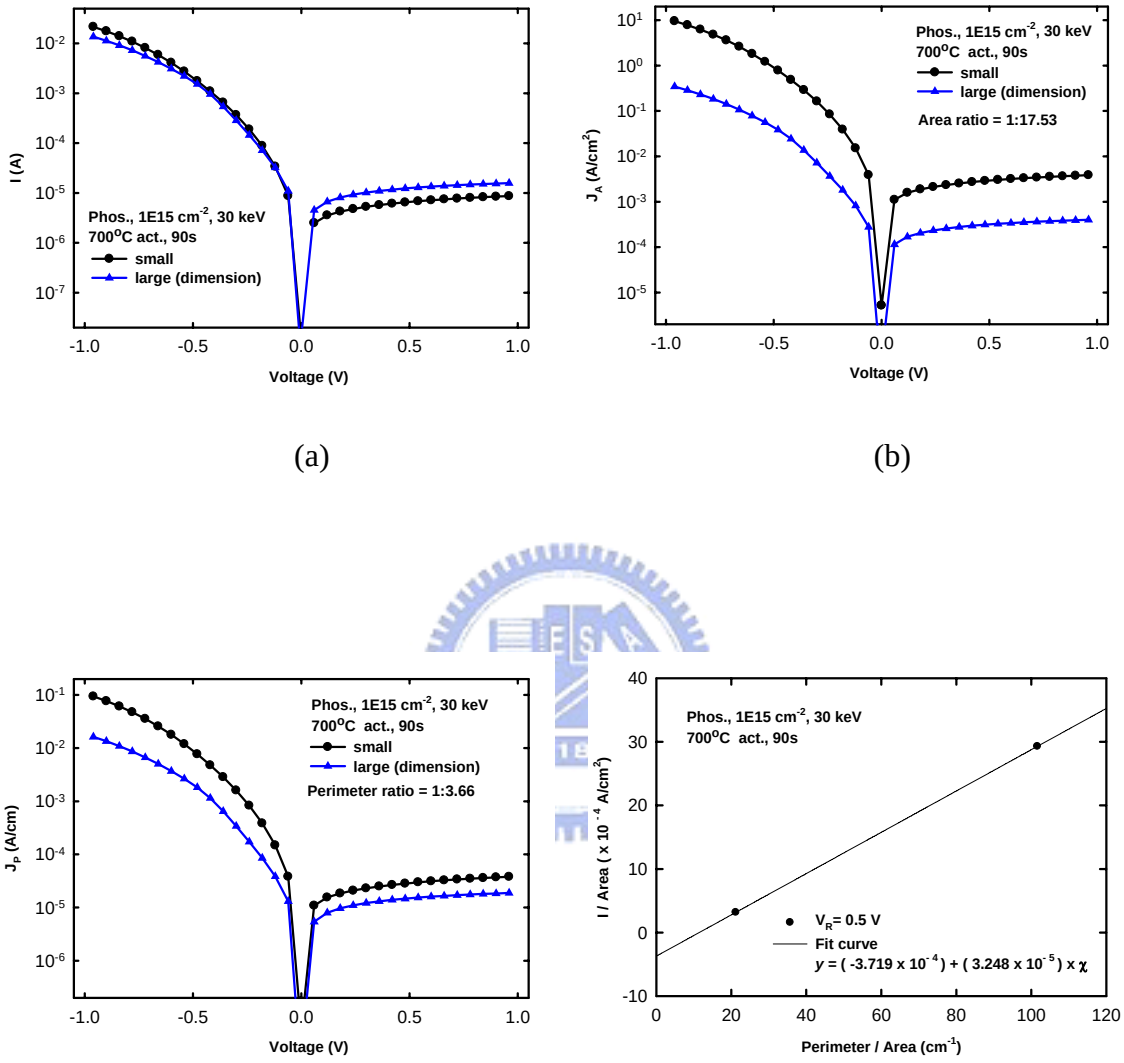


Fig. 2-21 (a) The I-V characteristics of junctions which were treated implantation energy of 30keV and activated at 700℃ for 90sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "perimeter current" dominates the leakage current qualitatively. (d) It shows the fitting curve for extracting J_A and J_P quantitatively.

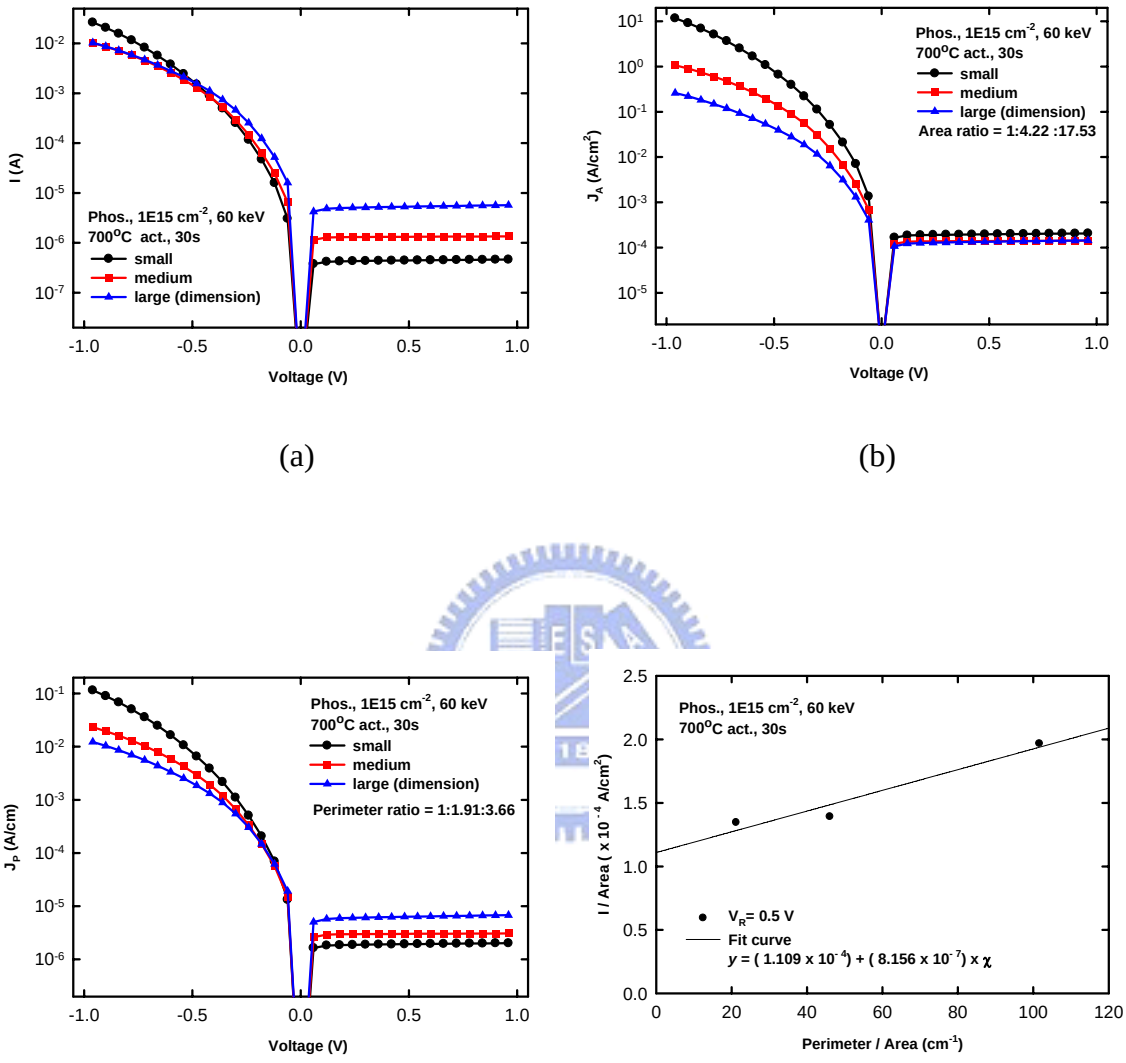


Fig. 2-22 (a) The I-V characteristics of junctions which were treated implantation energy of 60keV and activated at 700℃ for 30sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates the leakage current qualitatively. (d) It shows the fitting curve for extracting J_A and J_P quantitatively.

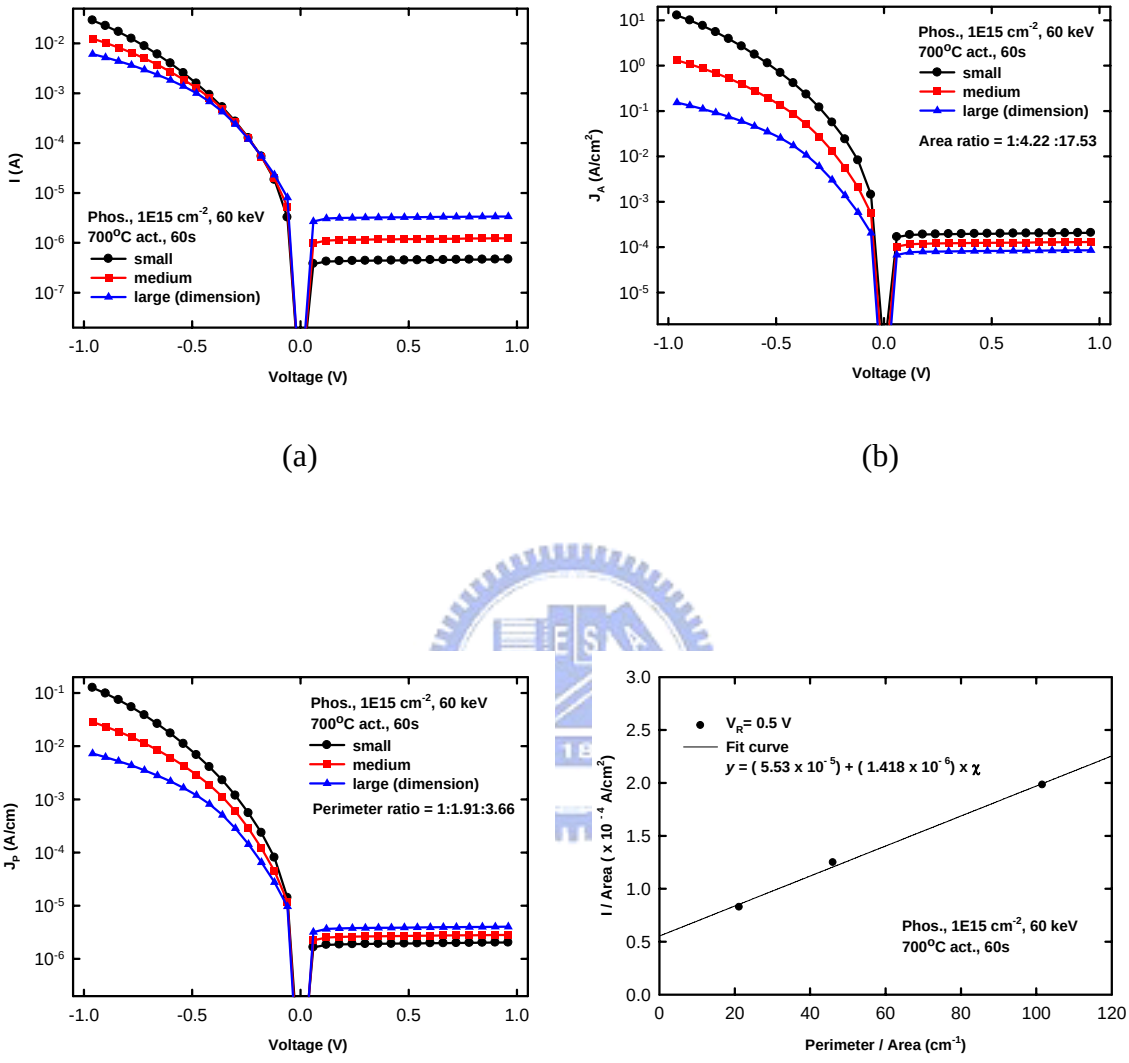
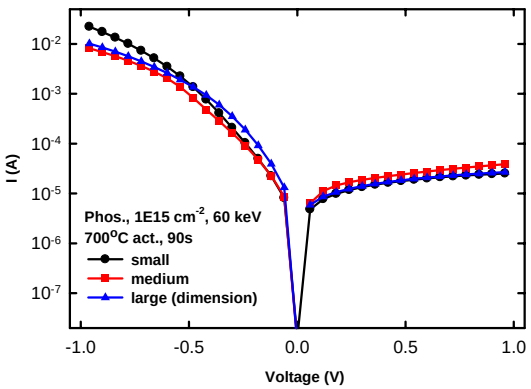
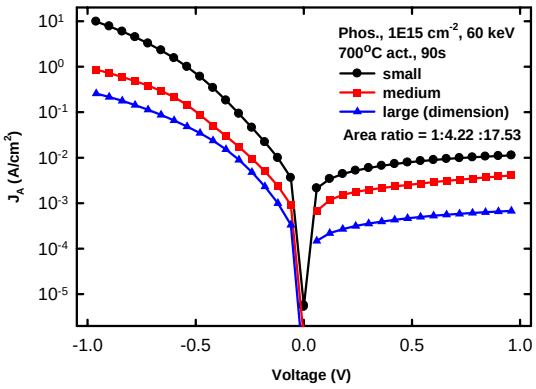


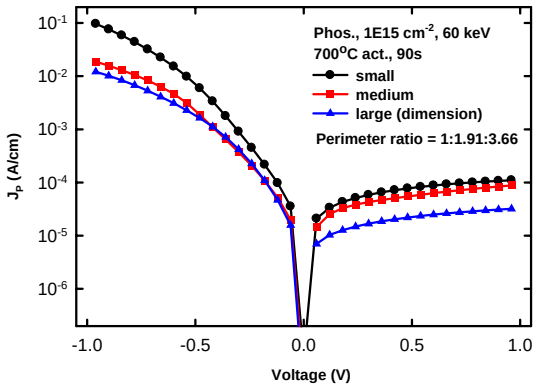
Fig. 2-23 (a) The I-V characteristics of junctions which were treated implantation energy of 60keV and activated at 700℃ for 60sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates the leakage current qualitatively. (d) It shows the fitting curve for extracting J_A and J_P quantitatively.



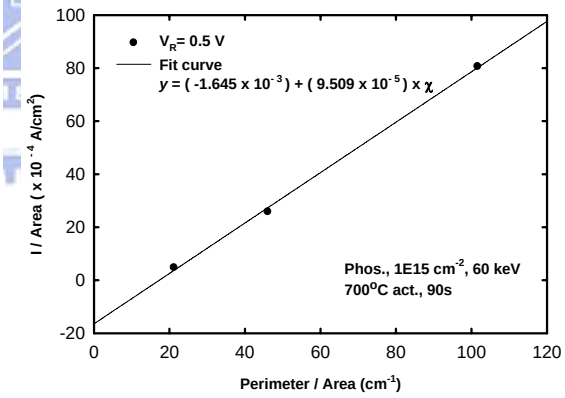
(a)



(b)

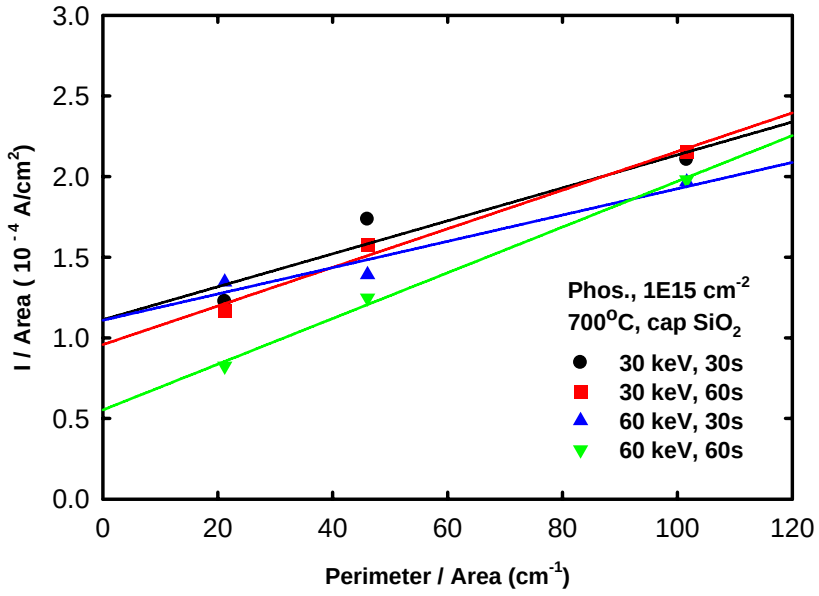


(c)

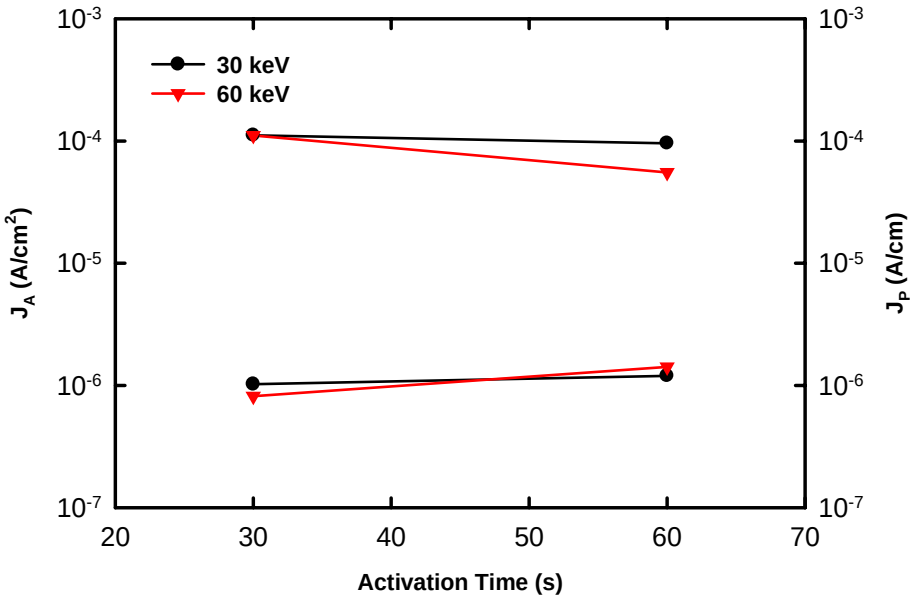


(d)

Fig. 2-24 (a) The I-V characteristics of junctions which were treated implantation energy of 60keV and activated at 700℃ for 90sec with various dimensions. (b) and (c) show the J_A-V and J_P-V characteristics, respectively. It hints the "area current" dominates more qualitatively. (d) It shows the fitting curve for extracting J_A and J_P quantitatively.



(a)



(b)

Fig. 2-25 The four samples in Table. 2-2 were treated implantation energy of 30keV or 60keV with further activation at 700℃ for 30sec or 60sec. (a) shows the fitting curve for extracting J_A and J_P quantitatively, and the extracted values are plotted in (b).

Chapter 3

The electrical performances of Germanium nMOSFETs with various conditions of source/drain junction formation

3-1 Introduction

In chapter 2, we have optimized the thermal process for the Ge n^+-p junction formation. Consequently, a reverse current of ca. 2 $\times 10^{-4}$ A/cm^2 from 0 to 1volt could be achieved with $\frac{J(forward)}{J(reverse)}$ ratio about 5 $\times$ 10^4. On the other hand, our group has studied the physical and electrical characteristics of the MOS structure (Pt / ALD Al_2O_3 / p-type Ge / Al) on bulk Ge and has attained adequate deposition condition of atomic layer deposition (ALD) system [23]. Therefore, we further integrated these correlative processes to form Ge nMOSFETs in this chapter. It indicates that implantation energy of 30keV or 60keV with further activation at 700 ℃ for 30s or 60s results in very similar and good electrical characteristics in section 2-3-3. Hence, we fabricated Ge nMOSFETs with these four conditions.

To realize our devices, we used a 4-mask process which was gate-last. Though electron mobility is much higher than hole mobility in Ge, we have mentioned that Ge nMOSFETs process would confront higher thermal budget than pMOSFETs because of the lower n-type dopant solubility. Hence, a worse gate stack for nMOSFETs, compared with pMOSFETs, may degrade the electrical performances due to more severely scattering mechanism such as surface roughness [24]. After the studies of above four conditions, we tried to reduce the thermal budget by decreasing activation temperature or activation time in section 3-3-2. In

this chapter, we investigated the electrical characteristics of Ge nMOSFETs, such as I_d-V_g and I_d-V_d, and further extracted sub-threshold swing (S.S), threshold voltage (Vth), source-drain series resistance (R_{SD}), and dopant in-diffusion length (ΔL), etc. Finally, we tried to figure out the physical meaning between those extracted parameters and conditions as possible as we could.

3-2 Experimental Procedures

In our nMOSFETs study, p-type (Gallium (Ga), concentration ~ 2×10^{15} /cm^3) Ge substrates were prepared. After broking a new wafer into adequate size, we cleaned them in diluted HF solution (HF:H_2O = 1:100) and deionized (D.I.) water alternately with several cycles. Then we treated them by a HF dip and N_2 drying in order to form an H-bond passivation layer on Ge surface. Furthermore, we deposited SiO_2 as field oxide and hard mask for following implantation by using a Plasma Enhanced Chemical Vapor Deposition (PECVD) system. Then we defined the implantation region for n-type dopant – Phosphorous (P) – by Mask 1 and etched SiO_2 by Buffer Oxide Etchant (BOE). Next, P was implanted into these samples with dose 1×10^{15} /cm^2 at 30 or 60 keV. Subsequently, samples were deposited 500 Å-thick SiO_2 by PECVD system and treated by a rapid thermal annealing (RTA) system in N_2 ambient at 650 or 700°C for various activation time ranging from 5sec to 60sec. Then we used Mask 2 to define the active region and etched SiO_2 till Ge surface was exposed by BOE. After remove the photoresist (P/R), we treated these samples by a HF dip (HF:H_2O = 1:30) for a few seconds to avoid the native oxide formation as possible as we could. Then we put these samples into the atomic-layer-deposition system (ALD) in Instrument Technology Research Center (ITRC) as fast as we could and deposited Al_2O_3 thin film. In ALD system, Al_2O_3 was achieved by pulsing alternative Tri-methyl- aluminum (TMA, or $Al(CH_3)_3$) and H_2O as the metal and oxidant precursors, respectively, into the reactor for 1sec every precursor at a constant pressure about 10 torr; an N_2 purge for 10sec was also treated after each precursor reacting for 1sec in order to remove residual precursors. The main recipe of ALD thin film as gate dielectric was reaction for 100 cycles at 170°C and it would have a thickness about 110Å. After the deposition of Al_2O_3, we continually etched the contact hole by Mask 3, and deposited Al by thermal coater as soon as possible. Finally, samples were defined the Al

pattern as electrodes by Mask 4. The overall fabrication processes of MOSFET were illustrated in Fig. 3-1 with a brief way. At last, we measured the characteristics of current-voltage (I-V) and capacitor-voltage (C-V) by HP 4156 system and HP4284, respectively.

3-3 Results and Discussion

3-3-1 Electrical characteristics of Ge nMOSFETs with various implantation and activation conditions

After optimizing the thermal process in chapter 2, we fabricated nMOSFETs under these four conditions, which were implantation energy of 30keV or 60keV with further annealing for 30sec or 60sec. Fig. 3-2(a~b) show the I_d-V_g and G_m-V_g performances, respectively. I_d-V_g exhibits all samples have close off-state currents, but an obvious difference of their on-state currents can be seen, and G_m-V_g also has a similar phenomenon. We attributed this to the effect of series resistance from source to drain. Fig. 3-2(c) also displays their I_d-V_d characteristics together. We could find that the well-known "linear region" here was not linear obviously. It hints somewhere in the current path, namely from source to drain, gives a high series resistance which effects the performance again. Furthermore, series resistances of these four conditions can be compared qualitatively by the degree of "rising" drain current in the linear region, such as V_d = 0.5 volt. Accordingly, the resistance for sample marked (30keV, 30sec) seems lowest; resistances of other samples marked (60keV, 30sec), (60keV 60sec), and (30keV, 60sec) are arranged from low to high in order. The tendency consists with I_d-V_g and G_m-V_g performances. On the other hand, it seems that a longer activation time will degrade drain current no matter which implantation energy is. Fig. 3-3 shows the extraction of source-drain series resistance (R_{SD}) and dopant in-diffusion length ($\triangle L$), and Fig. 3-4(a) displays the result. We could find a larger $\triangle L$ would accompany a larger R_{SD} with a longer activation time actually.

To realize above phenomenon, R_{SD} can be divided into several parts which are contact resistance (R_c) between Ge and Al, sheet resistance (R_{sh}) in implanted region, spreading resistance (R_{sp}), and accumulation resistance (R_{acc}) which is due to doping gradient [19,25].

The four resistances are also shown in Fig. 3-4(d). Refer to R_c and R_{sh}, we have extracted them for some cases in section 2-3-2. Fig. 2-12 shows those capped samples own the total resistance about 200Ω, and this can be as an estimated value of the sum of $2R_c$ and $2R_{sh}$ (2 is due to source and drain.) in our nMOSFETs study. Although Fig. 2-10(a) and Fig. 3-4(d) exhibit different structures, we believed they had close values of R_c and R_{sh} due to their dimensions. Hence, 200Ω compares with our extracted values of R_{SD} which is over 800Ω at least, it hints other two resistances, namely R_{acc} or R_{sp}, will dominate the R_{SD}. Besides, higher thermal budget will lead to more severe dopant diffusion. This makes the dopant concentration near the junction less gradient and increases the overlap region between gate and S/D. Accordingly, R_{acc} will become larger with higher thermal budget. In other words, R_{acc} can be assigned to the behaviors of ΔL and R_{SD} with activation time in Fig. 3-4(a).

Besides, a relatively more serious drain-induced barrier lowering (DIBL) effect on Germanium than on Silicon will be expected by charge-sharing model due to its larger dielectric constant. It can be considered the equation shown as below [19].

$$\Delta V_T = -\frac{qN_a W_m r_j}{C_o L}\left[\sqrt{1+\frac{2W_m}{r_j}}-1\right] \sim -W_m\left[\sqrt{1+\frac{2W_m}{r_j}}-1\right], \; W_m \sim \varepsilon^{\frac{1}{2}} \qquad (3.1)$$

, where ΔV_T is the difference of threshold voltage as we consider the charge-sharing model (or say, DIBL effect), W_m is the depletion width of the S/D junction, and ε is the dielectric constant of the bulk material (16 for Ge, and 11.9 for Si). The charge-sharing model also illustrates in Fig. 3-4(d), and the red dashed line is the depletion edge. In our study, it was actually observed the DIBL effect between V_d = 0.6V and 2.1V, and plotted the result in Fig. 3-4(b) with the ΔL we extracted above. A strong relation between DIBL and ΔL can be seen obviously, and it may be explained as following. A larger ΔL will introduce a smaller effective channel length (L_{eff} = L_{mask} - ΔL), and it may contribute more significant DIBL effect due to Eq. (3.1) which states L (L_{eff}) is inversely proportional to ΔV_T. Furthermore, a larger ΔV_T (DIBL effect) will lead to a smaller V_{th} under the same voltage bias. To verify it,

V_{th} for channel length 5 μm is plotted with observed DIBL for channel length 4 μm together in Fig. 3-4(c), and it indicates the results we expected. Besides, the relation between V_{th} and ΔL are also shown in Fig. 3-5(a); Fig. 3-5(b) and (c) display V_{th} and DIBL with various channel length, respectively.

On the other hand, we plotted the fitting lines in Fig. 3-3 for $V_g - V_{th} = 5V$ together in Fig. 3-6, we could find that a longer activation time led to a higher "channel resistance" due to its larger slope. Maybe the reason is that more thermal budgets will degrade the channel performance, such as increased scattering effect between Ge and Al_2O_3. We also used single-frequency method to extract the interfacial density of state (D_{it}) at 100K Hz, and found activation for 60sec had a slightly higher D_{it} about $5.24\times10^{13}\ eV^{-1}cm^{-2}$ than 30sec did. To compare further electrical performances, the sub-threshold swing (S.S.) and on-off ratio are also extracted and exhibits in Fig. 3-7(a). At last, we concluded the sample marked (30keV, 30sec) has the best electrical characteristics by above analysis, and plotted its C-V, I_d-V_g, and I_d-V_d in Fig. 3-7(b ~d).

3-3-2 The effect of reducing thermal budget during activation on electrical characteristics of the Ge nMOSFETs

Although we have investigated that the sample which was treated implantation energy 30keV and activated at 700℃ for 30sec owned the best result from pre-section conditions, it still revealed an obvious dopant in-diffusion length (ΔL). In order to improve this, we tried to reduce the thermal budget, because the experience of pre-work told us that ΔL would larger with an increasing activation time. Hence, reducing activation time and decreasing activation temperature are taken into account. Accordingly, (650℃, 30sec), (700℃, 5sec), (700℃, 15sec), and (700℃, 30sec) are chosen. The label stands for activation temperature and time. Fig. 3-9(a) shows the I_d-V_g and G_m-V_g of some conditions we chosen. The sample activated at

650℃, compared to 700℃, exhibits an unacceptable degradation on both on- and off-state currents. However, we found similar off-state currents for samples activated at 700℃ for 5, 15, and 30sec could be seen. It may hint the temperature is more dominate than time during annealing. In addition, it also reflects the series resistance form source to drain due to different drain currents. Fig. 3-9(b) displays the characteristics of source current (I_s-V_g) which was measured together with drain current simultaneously. I_s is equal to I_d as we expected, but off-state current is much lower than I_d. It is relative to our mask which is for gate-lasted process, and in order to make sure a "total" overlap between gate and channel, the layout of gate is extended behind each edge of the channel till 10 μm, namely gate stack and S/D are overlap 20 μm. Hence, an unavoidable effect of gate-induced drain leakage (GIDL) will occur. That's why off-state current in Fig. 3-9(a) and (b) are different. Of course, the increasing body current (I_B) was also found due to GIDL effect (not shown). Fig. 3-9(c) displays I_d-V_d for these four conditions, and a significant difference is observed in the saturation region. Regardless of the condition for 650℃, it was found decreasing saturation current was accompanied with decreasing activation time. The degraded trend is similar to the behavior of I_d-V_g. Fig. 3-10 presents the I_d-V_g and I_s-V_g individually for the four conditions above, and I_d-V_d characteristics are shown in Fig. 3-11 as well.

It was also extracted R_{SD} and ΔL as pre-section we done and was shown in Fig. 3-12. Additionally, the controlled sample labeled (700℃, 30s) owns a lower R_{SD} than the same condition in pre-section. This is attributed to some errors in our fabrication process, especially in coating Al process. However, this shouldn't affect the quantitative comparison in both sections respectively. And the result was integrated together in Fig. 3-13(a). It shows lower ΔL can be achieved by decreasing activated time due to less dopant diffusion. Unfortunately, it introduces a higher R_{SD} with less thermal budget. To double check the junction leakage performances for samples activated at 700℃ for 5sec to 60sec was investigated, and illustrated in Fig. 3-14. It displays an unobvious difference in junction leakage current, and

means all sample have similar activation level. Hence, the concentration near their space charge region should be the same. Hence, we attributed the various R_{SD} to the different concentration profiles of “bulk” S/D or the region near metal contacts for these four samples. This may lead to different contact resistance, sheet resistance, spreading resistance, or accumulation resistance we mentioned before.

Besides, Fig. 3-13(b) exhibits the channel resistance of these four thermal conditions by their slopes. The sample marked (650℃, 30sec) is less gradient than others activated at 700℃ for ranging from 5sec to 30sec. It suggests the activation temperature will effect on the interfacial quality more severely. However, another interesting thing is the slopes are almost the same for other samples which is activated for 5sec, 15sec, and 30sec. It implies the interfacial quality may not so sensitive to activation time, at least in the range 5 to 30sec at 700℃ Fig. 3-15 shows the comparison of swing, and on-off ratio and Fig. 3-16 exhibits the C-V (and G-V) characteristics. As far as our discussion, implantation for 30keV and annealing at 700℃ for 30sec have the most superior behaviors than other conditions, including activation time, annealing temperature, and even implantation energy.

3-4 Summary

We have optimized the n^+-p junction formation on bulk Germanium and obtained four process conditions which have similar electrical characteristics. The four conditions are implantation energy of 30keV or 60keV with further activation at 700℃ for 30sec or 60sec. Hence, we utilized them to fabricate Ge nMOSFETs. It was found that activation time seemed to effect on the dopant concentration of source and drain for both implantation energies. This would result in different R_{SD} and further total series resistance from source to drain. Because there were almost four parts in R_{SD}, we used some data to estimate the main reason was R_{acc} which was dependent on concentration and the overlap between gate stack and S/D. Besides, strong relations between ΔL, V_{th}, and DIBL are also observed. Although the sample with implant energy of 30keV and further activated at 700℃ for 30sec has the better electrical performances, a large ΔL is still observed. To improve this, we reduced the thermal budget during activation. However, either reducing activation time or decreasing activation temperature leads to a larger R_{SD}, even if they own a lower ΔL. We also attributed this to the redistribution of doping concentration in the source and drain after annealing. Finally, we believed implantation for 30keV and annealing at 700℃ for 30sec have the most superior behaviors than other conditions, including activation time, annealing temperature, and even implantation energy. In order to improve the high R_{SD}, we considered the FGA process in next chapter.

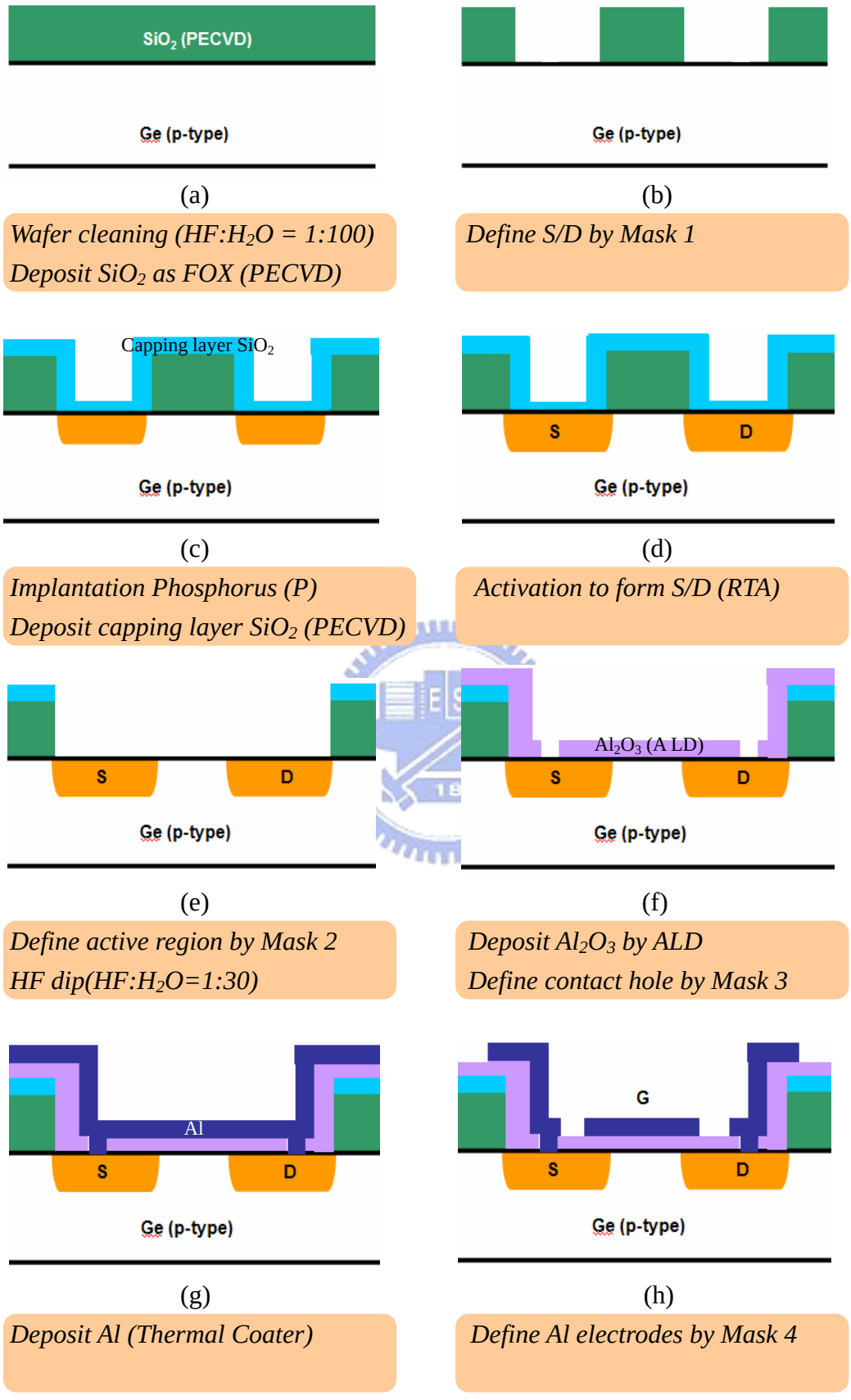
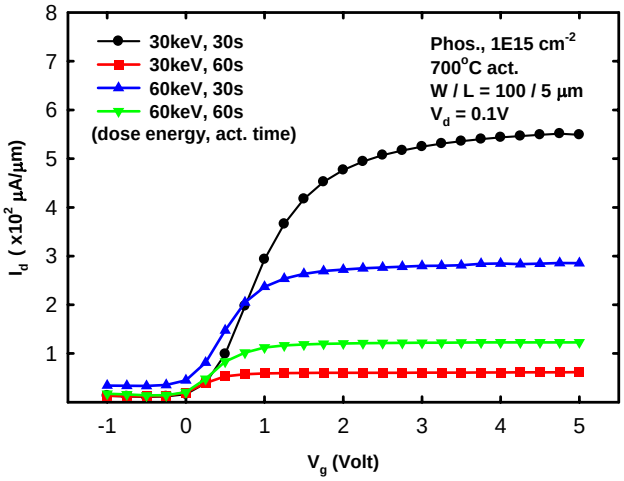
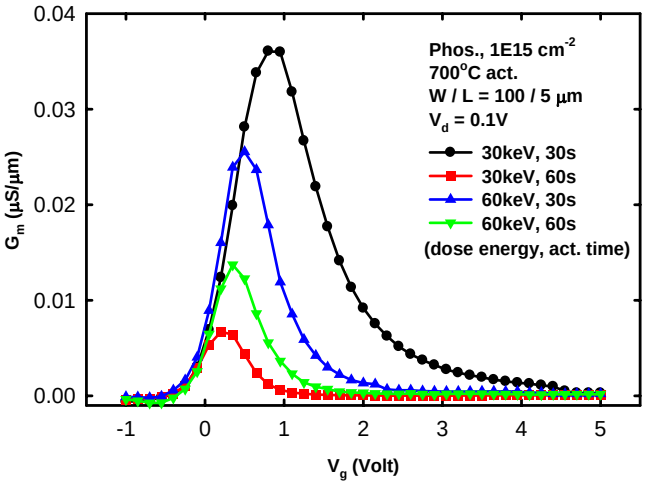


Fig. 3-1 Ge nMOSFETs fabrication flow chart



(a)



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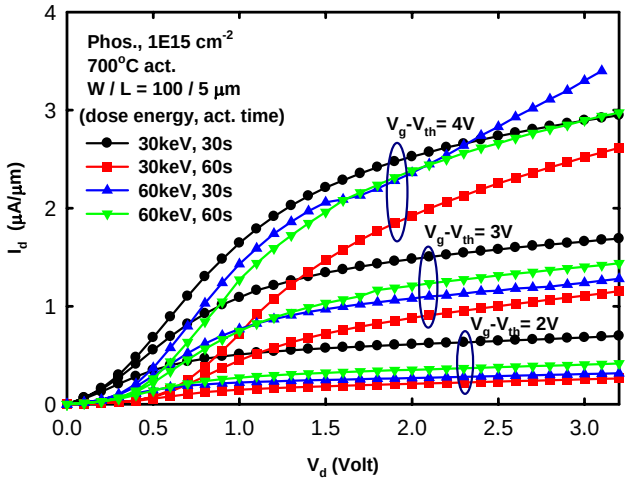
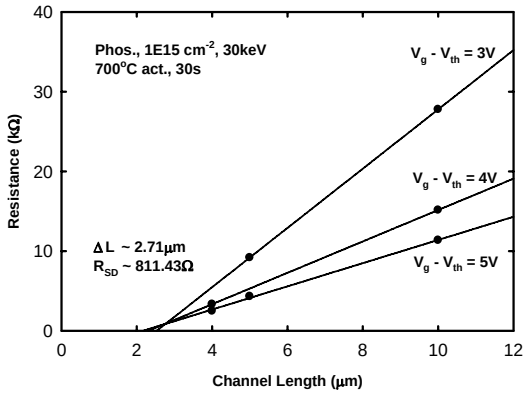
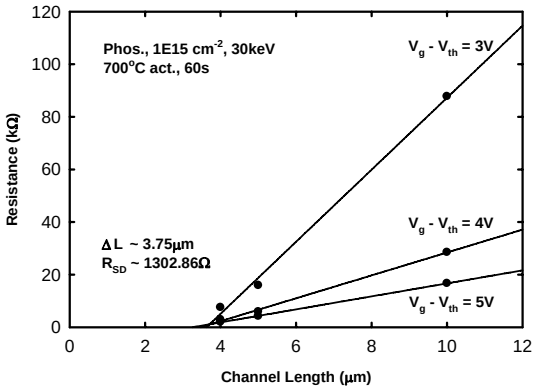


(c)

Fig. 3-2 It shows the (a) I_d-V_g, (b) G_m-V_g, and (c) I_d-V_d performances under implantation energy of 30 or 60keV with further activation at 700℃ for 30 or 60sec.



(a)



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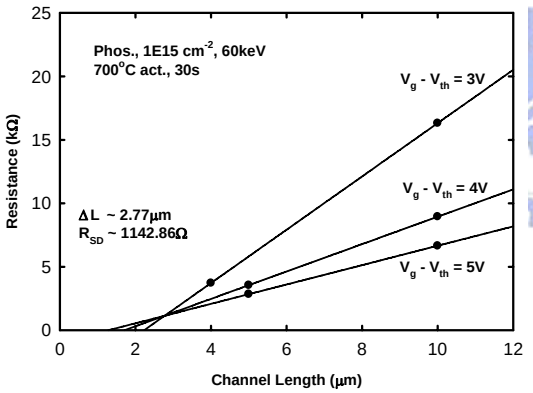
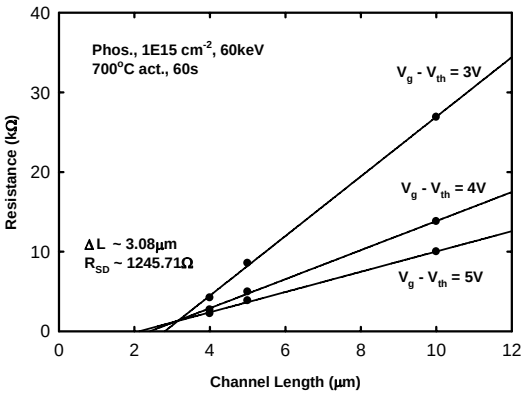
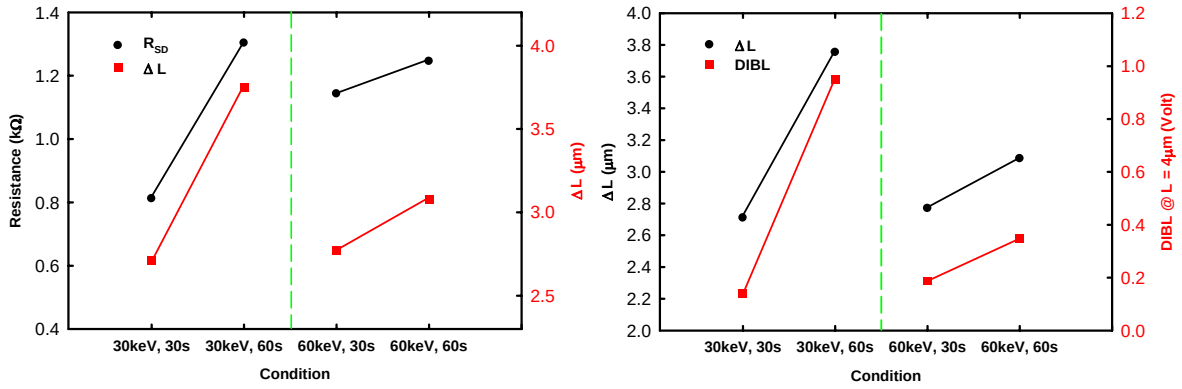


(c)



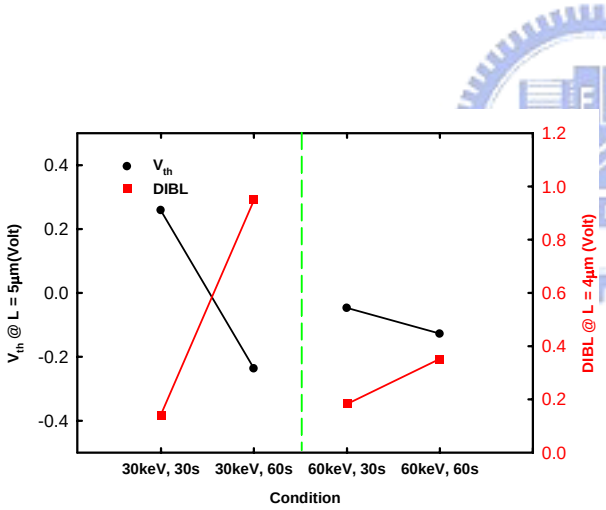
(d)

Fig. 3-3 The R_m-L_g fitting curves for extraction of R_{SD} and $\triangle L$. (a), (b), (c), and (d) are (30keV, 30sec), (30keV, 60sec), (60keV, 30sec), and (60keV, 60sec), respectively. The label (#keV, #sec) stands for the implantation energy and activation time at 700 ℃.



(a)

(b)



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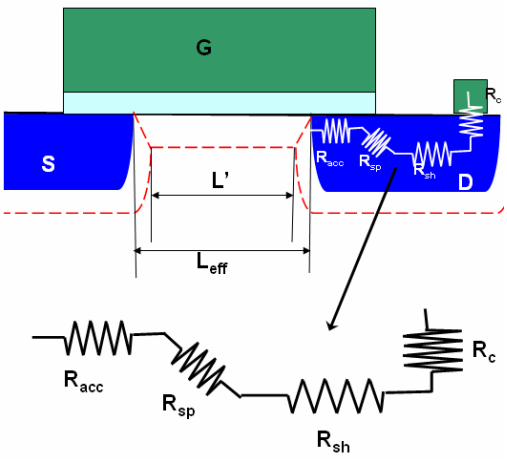
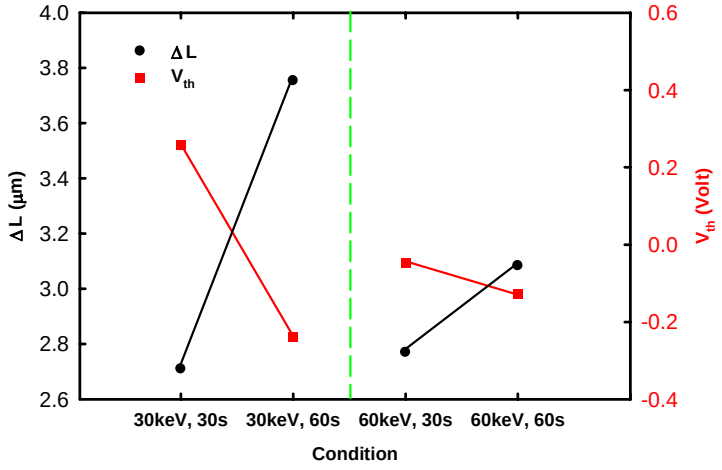
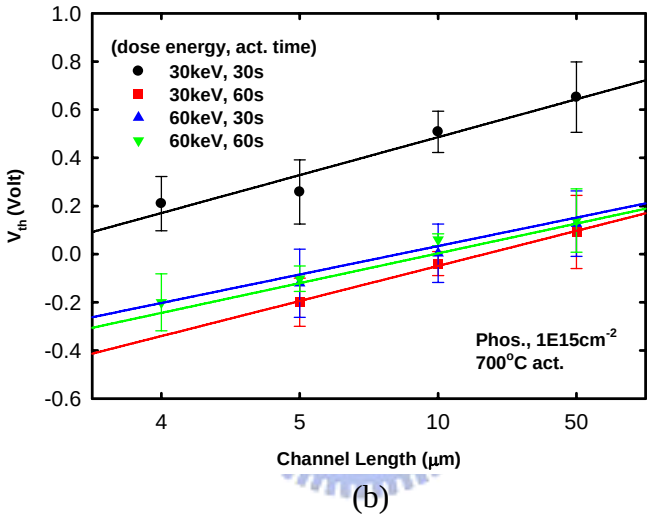


(d)

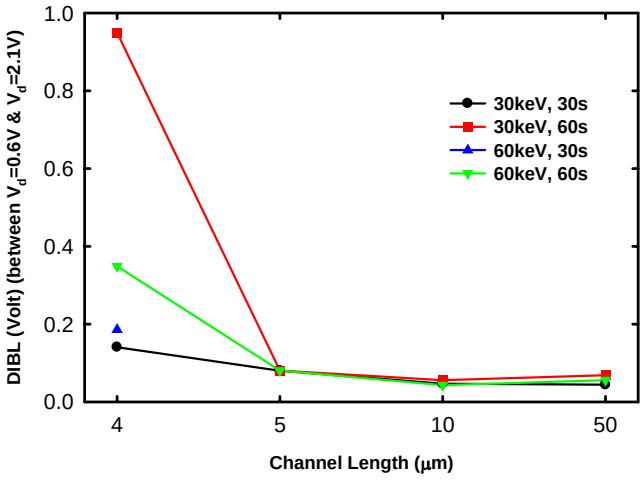
Fig. 3-4 The extracted values of (a) R_{SD} and △L (b)△L and DIBL (c) V_{th} and DIBL are plotted. DIBL is extracted for channel length 4㎛. (d) A picture presents R_{SD} has four parts: R_{acc}, R_{sp}, R_{sh}, and R_c. It also shows the DIBL effect due to charge sharing model. The red dashed line is the edge of depletion region.



(a)



(b)



(c)

Fig. 3-5 The extracted values of (a) V_{th} and $\triangle L$ (b) V_{th} (c) DIBL are plotted.

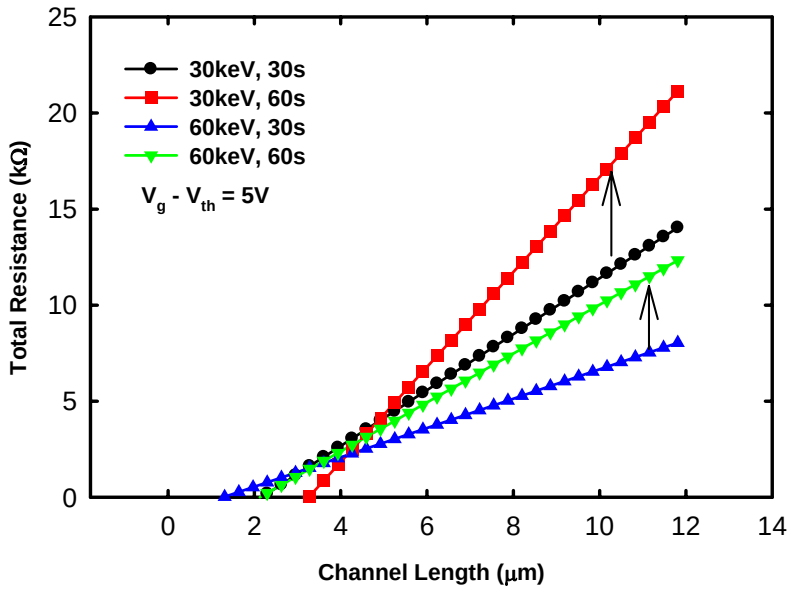


Fig. 3-6 It is plotted the fitting lines for V_g-V_{th}=5V in Fig. 3-3 together.

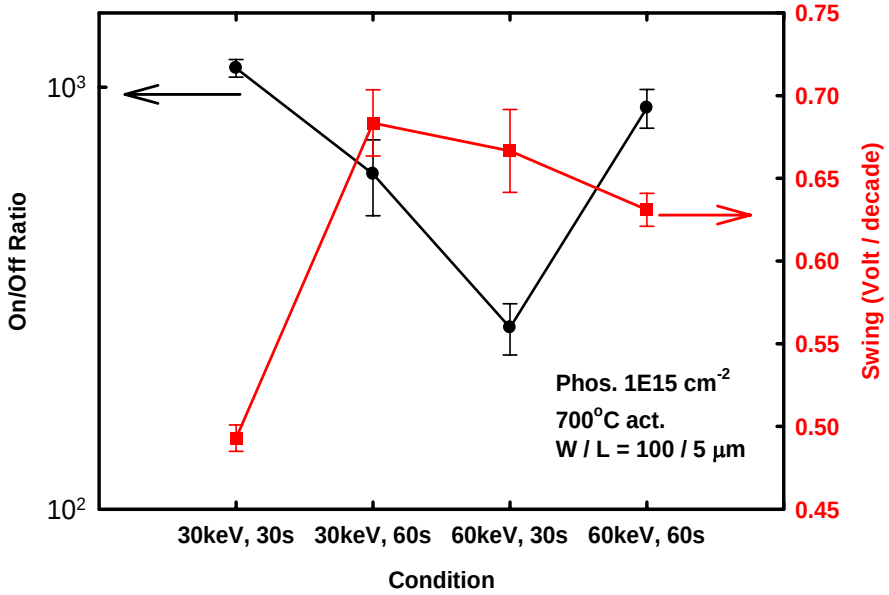
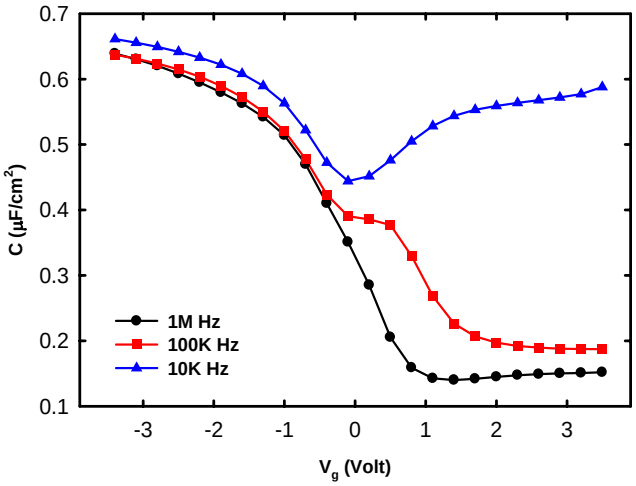
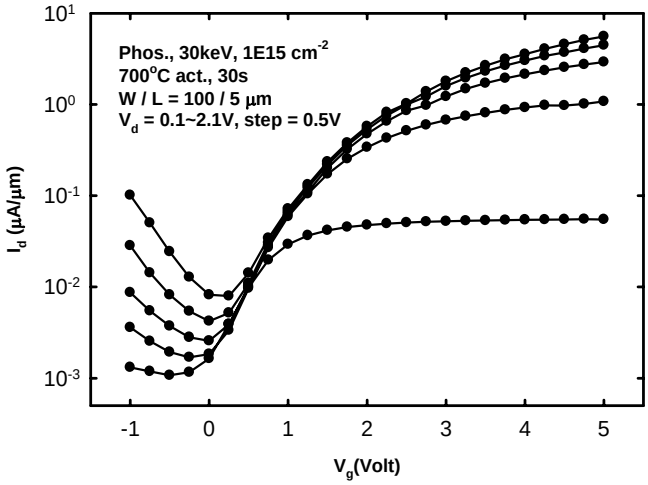


Fig. 3-7 The extracted sub-threshold swing (S.S.) and on-off ratio for these four conditions which are implantation energy of 30keV or 60keV with further activation at 700℃ for 30sec or 60sec.



(a)



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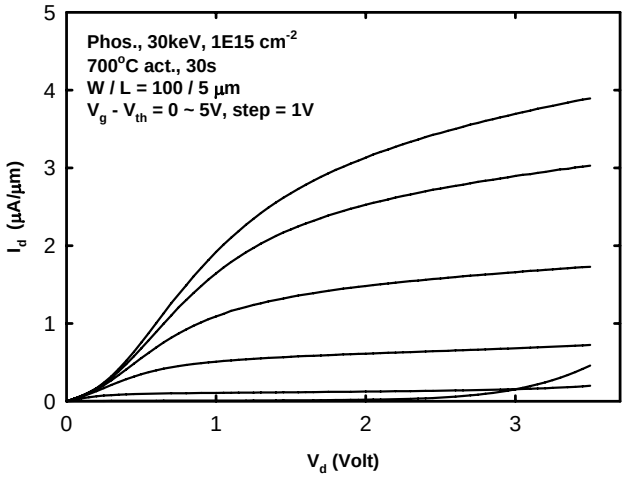
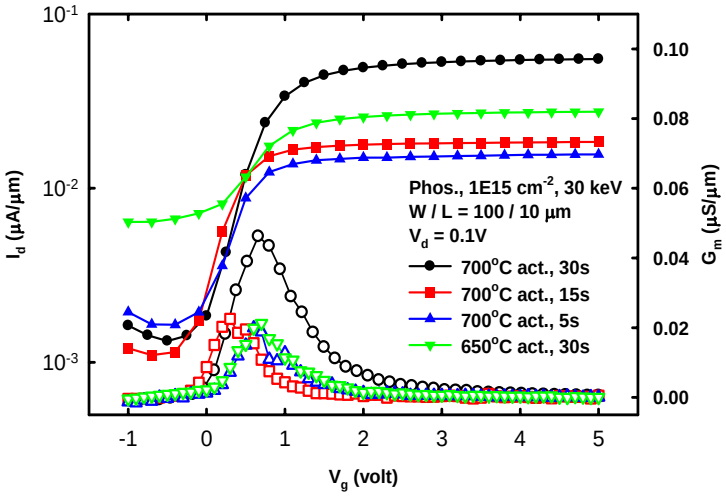
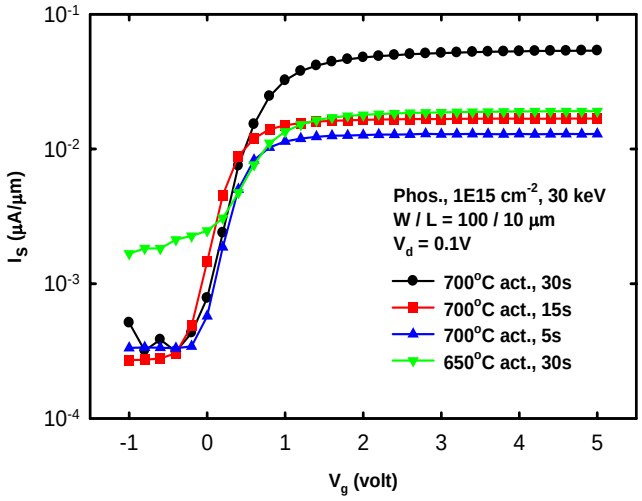


(c)

Fig. 3-8 The (a) C-V (b) I_d-V_g, and (c) I_d-V_d performances after annealing at 700℃ for 30sec. The S/D is implanted Phos. for 30keV.



(a)



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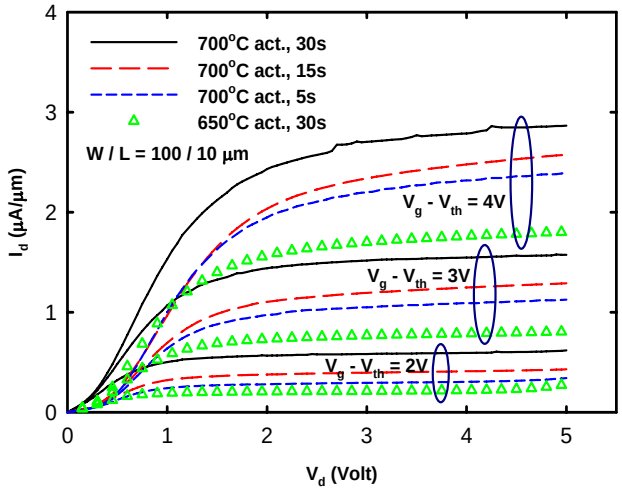
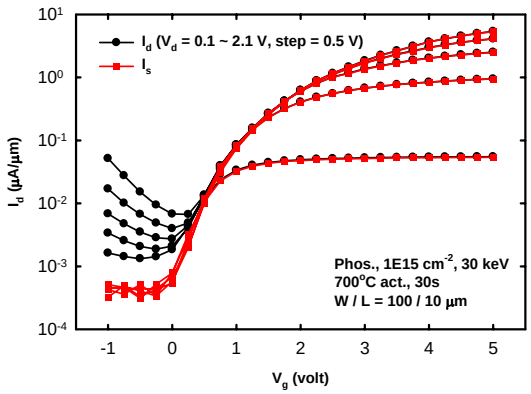
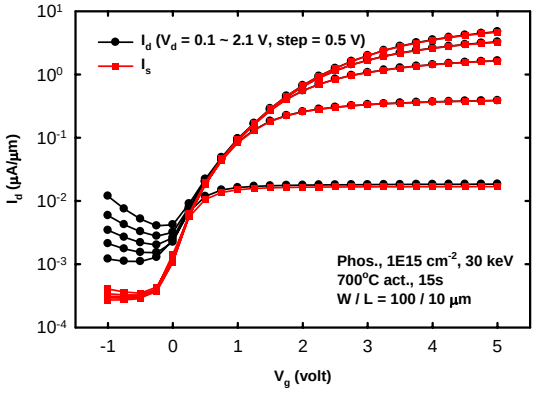


(c)

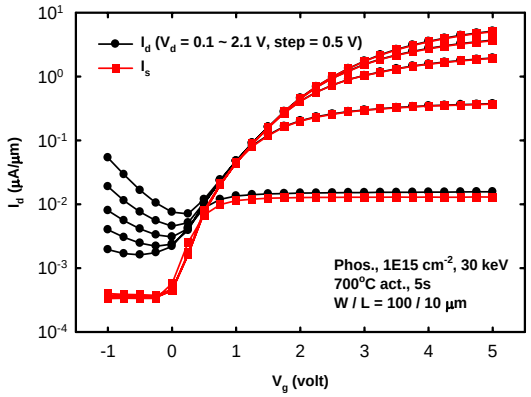
Fig. 3-9 The (a) I_d-V_g, (b) I_s-V_g at V_d=0.1V, and (c) I_d-V_d performances for four annealing conditions are shown together. The G_m-V_g also plotted in (a). These four conditions are annealing at 650 or 700℃ for 5, 15, or 30sec.



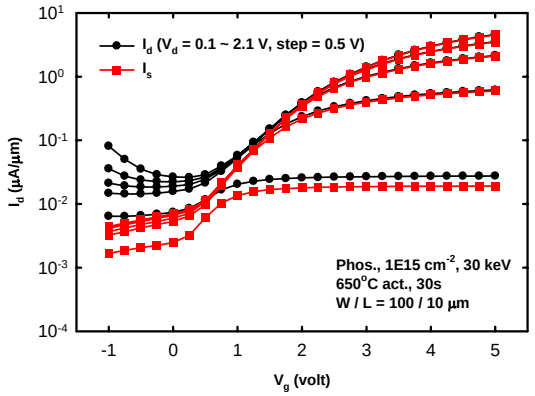
(a)



(b)



(c)



(d)

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Fig. 3-10 The I_d-V_g and I_s-V_g characteristics of four activation conditions we chosen These conditions are activation at 650 or 700℃ for 5, 10, or 30sec.

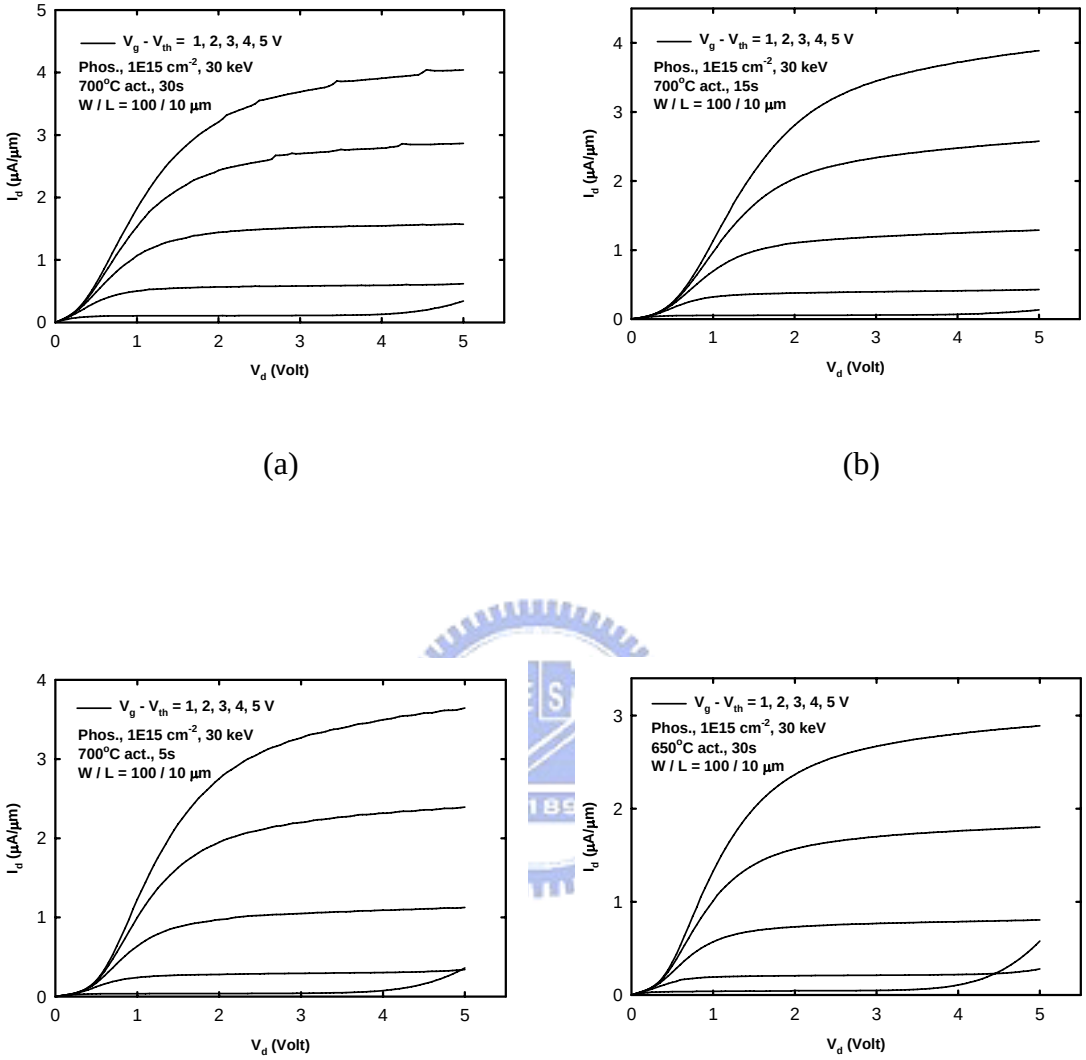


Fig. 3-11 The I_d-V_d characteristics of four activation conditions we chosen. These conditions are activation at 650 or 700℃ for 5, 10, or 30sec.

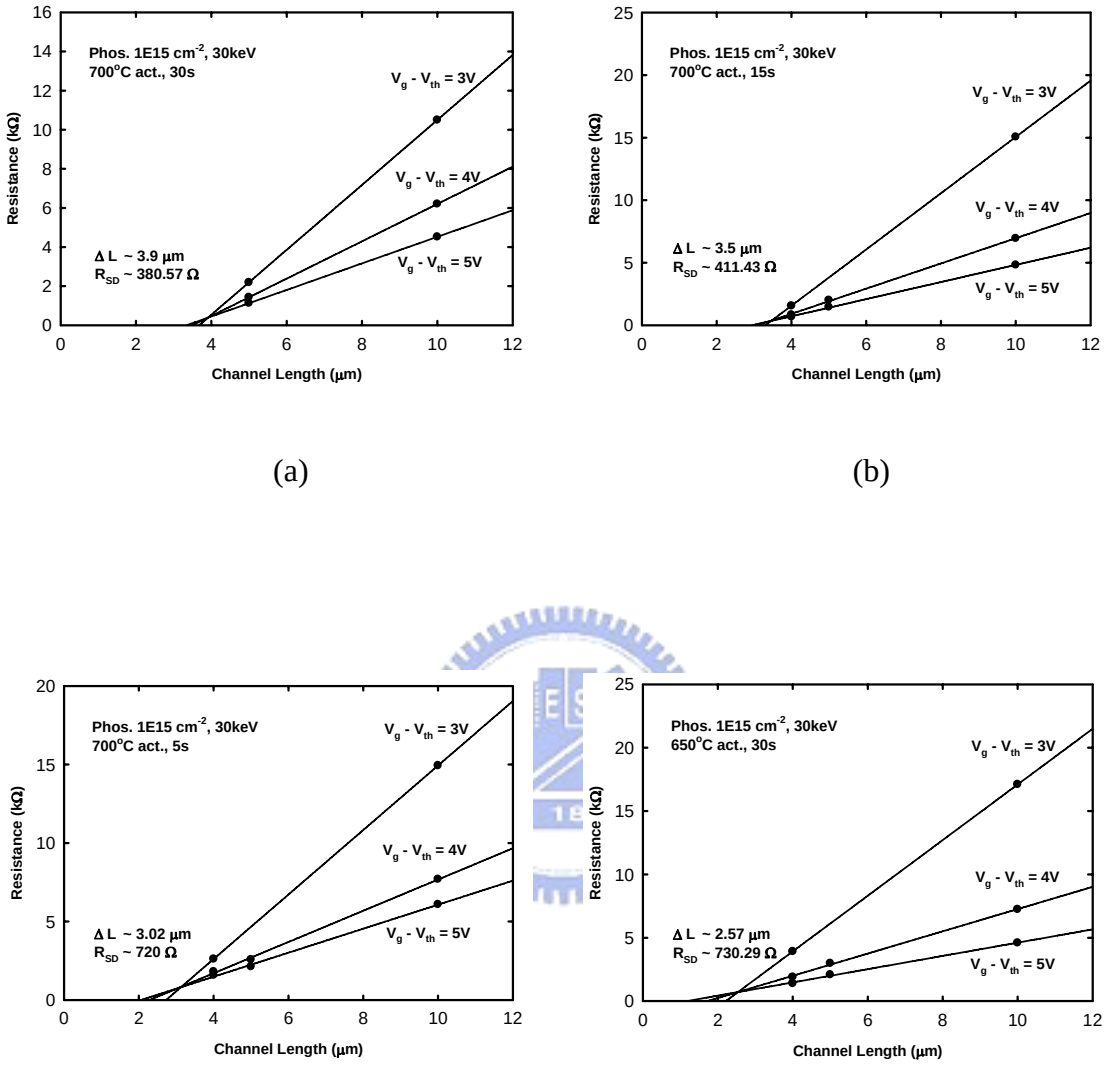
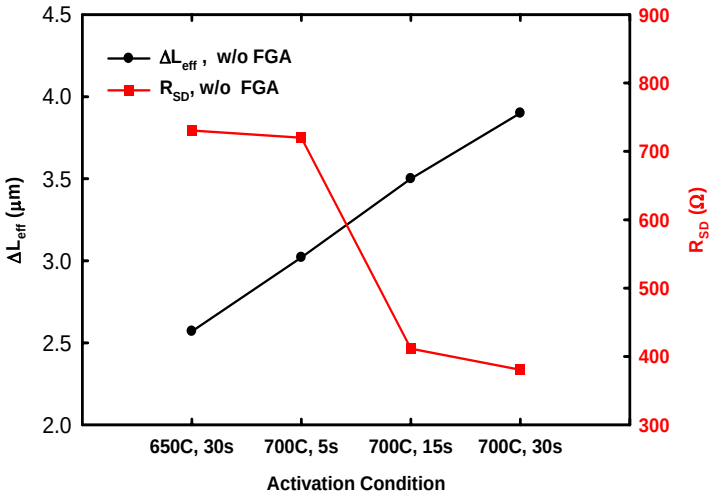
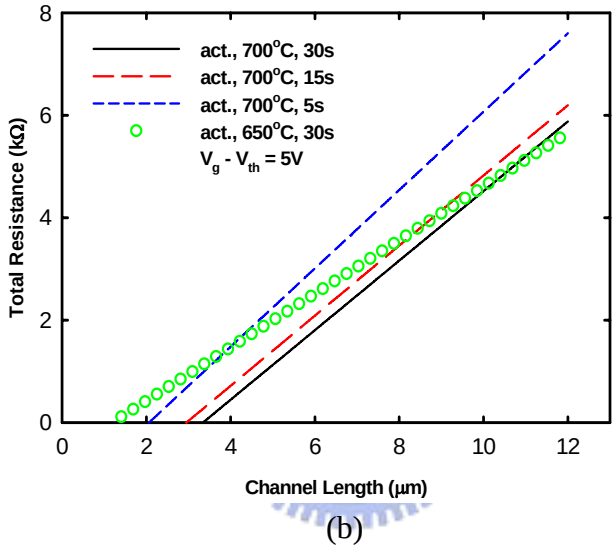


Fig. 3-12 The R_m-L_g fitting curves for extraction of R_{SD} and △L. (a), (b), (c), and (d) are (700℃, 30sec), (700℃, 15sec), (700℃, 5sec), and (650℃, 30sec), respectively. The label (#℃, #sec) stands for the activation temperature and time.



(a)



(b)

Fig. 3-13 (a)The extracted R_{SD} and ΔL from Fig. 3-12. (b) It is plotted the fitting lines for V_g-V_{th}=5V in Fig. 3-12 together.

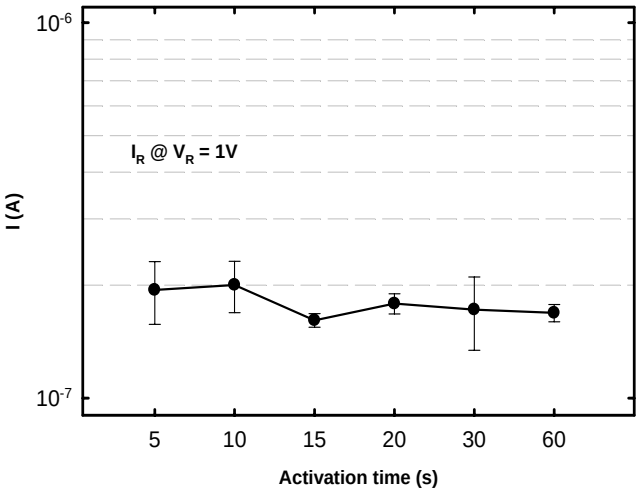
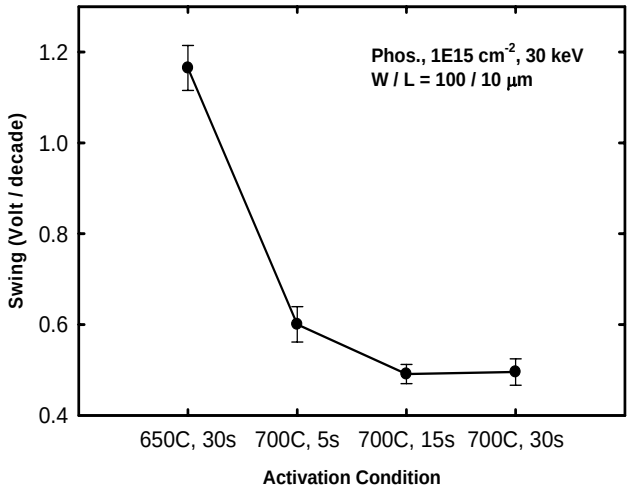
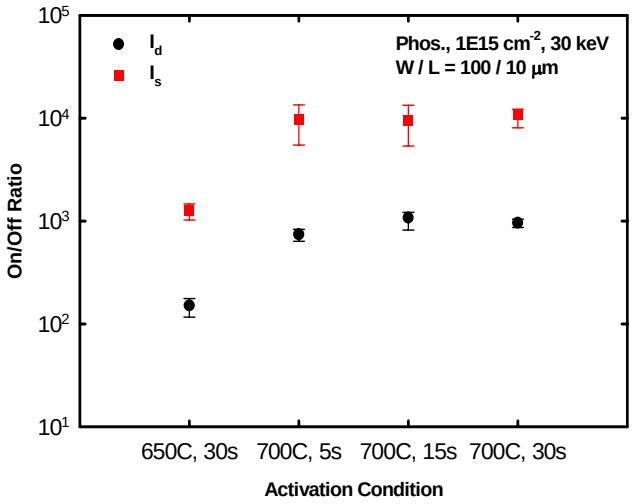


Fig. 3-14 The leakage current of samples activated at 700℃ for 5 to 60sec at V_R=1V.



(a)



(b)

Fig. 3-15 The extracted sub-threshold swing (S.S.) and on-off ratio for these four conditions which are activated at 650 or 700℃ for 5, 15, or 30sec. On-off ratio is also extracted from source current.

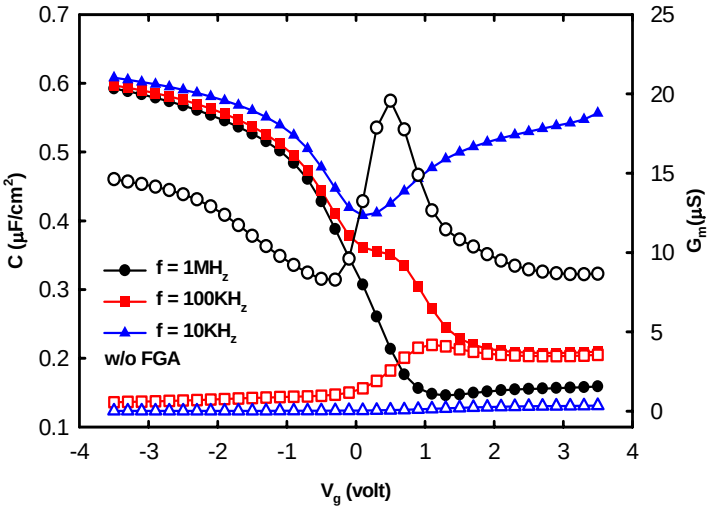


Fig. 3-16 The C-V (and G_m-V) performances after annealing at 700℃ for 30sec.

Chapter 4
nMOSFETs on bulk Ge with forming gas annealing (FGA)

4-1 Introduction

In order to better the issue of high R_{SD} in pre-chapter, we considered a forming gas annealing (FGA) process. The FGA process is very popular in CMOS industry. It is usually used to repair the dangling bonds, which exist in the interface between gate oxide and channel, by H-bond. Hence, a higher quality interface will eliminate some trapping and scattering mechanisms, such as coulomb-force-induced scattering, etc. Finally, it will improve the off-state current, carrier mobility and further saturation current [26-29]. Besides, it also utilized for the silicidation or germanide to reduce the specific contact resistance between semiconductor and metal electrodes [30].

In this chapter, we also used the same masks to form our devices and treated samples with FGA at last. Because FGA process was arranged just after the formation of Al electrodes, we could expect the improvements in both interfacial density of states and S/D resistance. We also extracted sub-threshold swing (S.S), threshold voltage (Vth), source/drain series resistance (R_{SD}), and dopant in-diffusion length (ΔL), etc. Finally, we tried to figure out the physical meaning between those extracted parameters and conditions as possible as we could.

4-2 Experimental Procedures

In our nMOSFETs study, p-type (Gallium (Ga), concentration ~ 2×10^{15} /cm^3) Ge substrates were prepared. After broking a new wafer into adequate size, we cleaned them in diluted HF solution (HF:H_2O = 1:100) and deionized (D.I.) water alternately with several cycles. Then we treated them by a HF dip and N_2 drying in order to form an H-bond passivation layer on Ge surface. Furthermore, we deposited SiO_2 as field oxide and hard mask for following implantation by using a Plasma Enhanced Chemical Vapor Deposition (PECVD) system. Then we defined the implantation region for n-type dopant – Phosphorous (P) – by Mask 1 and etched SiO_2 by Buffer Oxide Etchant (BOE). Next, P was implanted into these samples with dose 1×10^{15} /cm^2 at 30keV. Subsequently, samples were deposited 500 Å-thick SiO_2 by PECVD system and treated by a rapid thermal annealing (RTA) system in N_2 ambient at 650℃ for 30sec or at 700℃ for ranging from 5sec to 30sec. Then we used Mask 2 to define the active region and etched SiO_2 till Ge surface was exposed by BOE. After remove the photoresist (P/R), we treated these samples by a HF dip (HF:H_2O = 1:30) for a few seconds to avoid the native oxide formation as possible as we could. Then we put these samples into the atomic-layer-deposition system (ALD) in Instrument Technology Research Center (ITRC) as fast as we could and deposited Al_2O_3 thin film. In ALD system, Al_2O_3 was achieved by pulsing alternative Tri-methyl- aluminum (TMA, or $Al(CH_3)_3$) and H_2O as the metal and oxidant precursors, respectively, into the reactor for 1sec every precursor at a constant pressure about 10 torr; an N_2 purge for 10sec was also treated after each precursor reacting for 1sec in order to remove residual precursors. The main recipe of ALD thin film as gate dielectric was reaction for 100 cycles at 170℃ and it would have a thickness about 110Å. After the deposition of Al_2O_3, we continually etched the contact hole by Mask 3, and deposited Al by thermal coater as soon as possible. Then samples were defined the Al pattern

as electrodes by Mask 4. Finally, we used forming gas annealing (FGA) for sintering in N_2 ambient with 5% H_2 at 300℃ and 400℃ for 30min and 20 min, respectively. The overall fabrication processes of MOSFET were illustrated in Fig. 4-1 with a brief way. At last, we measured the characteristics of current-voltage (I-V) and capacitor-voltage (C-V) by HP 4156 system and HP4284, respectively.

4-3 Results and Discussion

4-3-1 Electrical characteristics of the Ge nMOSFETs after forming gas annealing (FGA)

In chapter 3, we have fabricated nMOSFETs and investigated the effect of some activation parameters on electrical performances. Although the conditions of implantation energy of 30keV and annealing at 700℃ for 30sec contribute a better result relatively, the excess S/D resistance is still a drawback. To improve this, we took forming gas annealing (FGA) into account. Fig. 4-2 shows the I_d-V_g performances of the samples with or without FGA processes at 300℃ for 30min. Obviously currents in the linear region is improved about one order for all samples, and transconductance (G_m) also becomes larger by a factor of tens (not shown). It also displays the electrical performances of I_d-V_d in Fig. 4-3. We could find all samples presented much improvement on saturation current about a factor of six, and currents in the linear region became more "linear" than samples without FGA as our expectation. Above improvement could be attributed to the achievement of a lower resistance in the current path from source to drain. However, the significant and obvious degradation on off-state current which is due to junction leakage current could be seen in Fig. 4-2 as well. In addition, the samples which are activated at 650℃ and 700℃ for 30sec and 5sec, respectively, present more obvious junction leakage than others due to an increasing drain current even under $V_g = V_{th}$ in Fig. 4-3. The degradation of leakage current is very interesting because it is found the same FGA process on Ge pMOSFETs in our other study can much improve the electrical characteristics, such as leakage current and swing.

Fig. 4-4 shows the work of extracting R_{SD} and ΔL as we done before. The results are displayed in Fig. 4-5(a~ b). The extracted values of R_{SD} are much lower than fresh samples about a factor of four. We have mentioned there are four parts in R_{SD}, and some ideas are taken into account as following. First, FGA processes may let the interface between Ge and Al

has alloy-like phase and further reduce R_c. Second, the FGA processes should lead to P redistribution, and it will effect on R_{acc} , R_{sh}, or R_{sp}. However, the exact reason should be further verified.

Besides, the values of degraded sub-threshold swing (S.S.) and on-off current ratio compared with the samples without FGA are also shown in Fig. 4-5(b~ c). Although the sample activated at 700℃ for 30sec with FGA at 300℃ for 30min still has better performance, it also degrades on-off ratio about one order and swing about 200mV/decade. In addition, we also investigated FGA at a higher temperature – 400℃ for 20min, and the result was illustrated in Fig. 4-6. It indicates a more serious degradation on junction leakage current can be observed than the case at 300℃ for 30min. To double check the junction performances, we used the masks of nMOSFETs process to fabricate the diode which was implanted with 1×15 cm^{-2} for 30keV and activated at 700℃ for various time ranging from 5sec to 60sec. Some samples are treated FGA for 300℃ and 400℃. The sample activated for 30sec was chosen to present the I-V performance and plotted in Fig. 4-7(a). After FGA, the forward characteristic is improved; however, it also shows the degradation on leakage current. Especially for FGA at 400℃, it is obviously that the junction is “destroyed” from the symmetrically electrical performance. The leakage currents at 1volt for various activation times are shown in Fig. 4-7(b). It indicates reverse current increases with an increasing temperature during FGA again no matter which activation time is.

4-3-2 The interface quality and reliability of gate dielectric Al_2O_3

Forming gas annealing not only reduces the contact resistance, but also recovers the interfacial density of states (D_{it}) in the channel region. The D_{it} will charge or discharge and further degrades the mobility by scattering. Fig. 4-8(a) and (b) reveal the capacitance-voltage (C-V) characteristics of the sample labeled (30keV, 700℃, 30sec) with and without FGA at 300℃, respectively. It shows the electrical behavior of C-V has more frequency disturbance and less gradient slope at the flat band voltage before FGA. Besides, we used the single frequency method to estimate the D_{it} about 4.67×10^{12} $cm^{-2}eV^{-1}$ and 1.98×10^{12} $cm^{-2}eV^{-1}$ at 1MHz for without and with FGA, respectively. On the other hand, Fig. 4-8(c) indicates that each sample with FGA will lead to an obviously lower slope, namely a lower channel resistance. This can consist with D_{it}, because a lower D_{it} will lead to less carrier scattering. Accordingly, less scattering will improve the mobility. Fig. 4-8(d) presents the best mobility of our work (with FGA at 300℃ for 30min) compared with some recent publications, and it leaves much to be desired.

We have known the fact that FGA can improve D_{it}, but it also degrades the junction as well. Considering the nMOSFETs fabrication we followed, it's a gate-last process which will damage the interface of Ge before depositing Al_2O_3 due to the step which is etching the dummy gate (Fig. 4-1(e)). Maybe a gate-first process with a following FGA for optimizing the gate stack, and utilizing the laser annealing method to activate dopant in S/D without damage gate stack will improve the electrical characteristics above [24].

Finally, Fig. 4-9 and Fig. 4-10 show the electrical degradation after positive gate bias stress (or say PBTI) for samples without and with FGA, respectively. And the extractions of degradation parameters, which are I_d degradation, $\triangle V_{th}$, and swing, are shown in Fig. 4-11. It exhibits though FGA will improve the interface but also degrade the high-K film. The exact cause should be further investigated.

4-4 Summary

In this chapter, the source/drain resistance could be much improved after forming gas annealing at 300℃ for 30min. Although we still had no direct evidence, we attributed this to the formation of alloy-like phase between Ge and Al or the redistribution of P dopant concentration after the thermal budget of FGA. Furthermore, the channel resistance could be reduced much as well. This part consisted with the values of D_{it} we extracted before and after FGA. We believed that FGA repaired the interface density of states, and it would lead to a lower resistance due to less scattering which is dependent on D_{it}. However, much degradation was observed on junction leakage current after FGA. The exact reason should be verified further. Besides, an interesting thing was also found that a worse reliability by PBTI measurement could be seen after FGA, though it owned a better interface between channel and gate dielectric Al_2O_3. This part is also necessary to verify. Finally, the extracted mobility was compared with some recent publications.

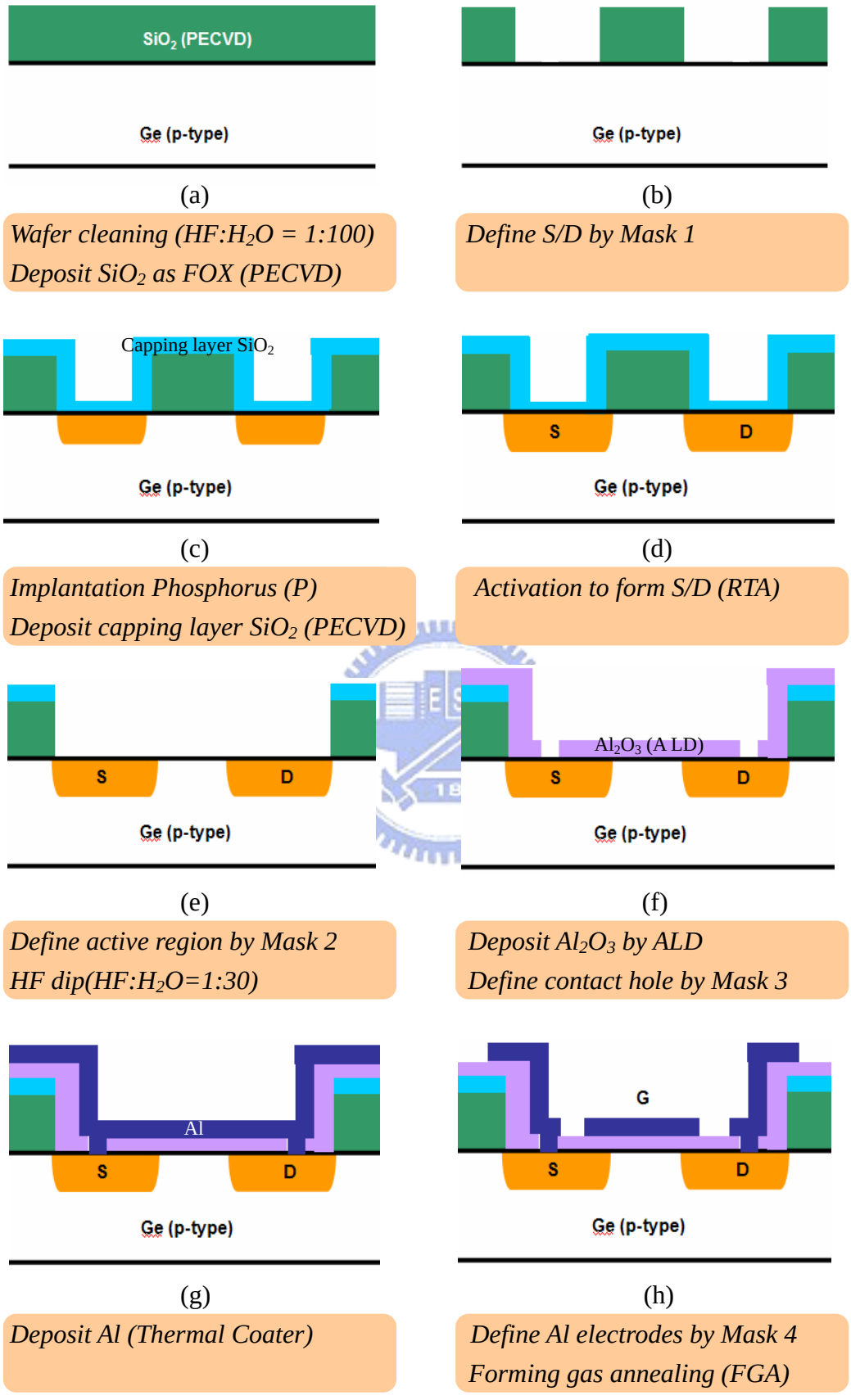


Fig. 4-1 Ge nMOSFETs fabrication with forming gas annealing at last flow chart

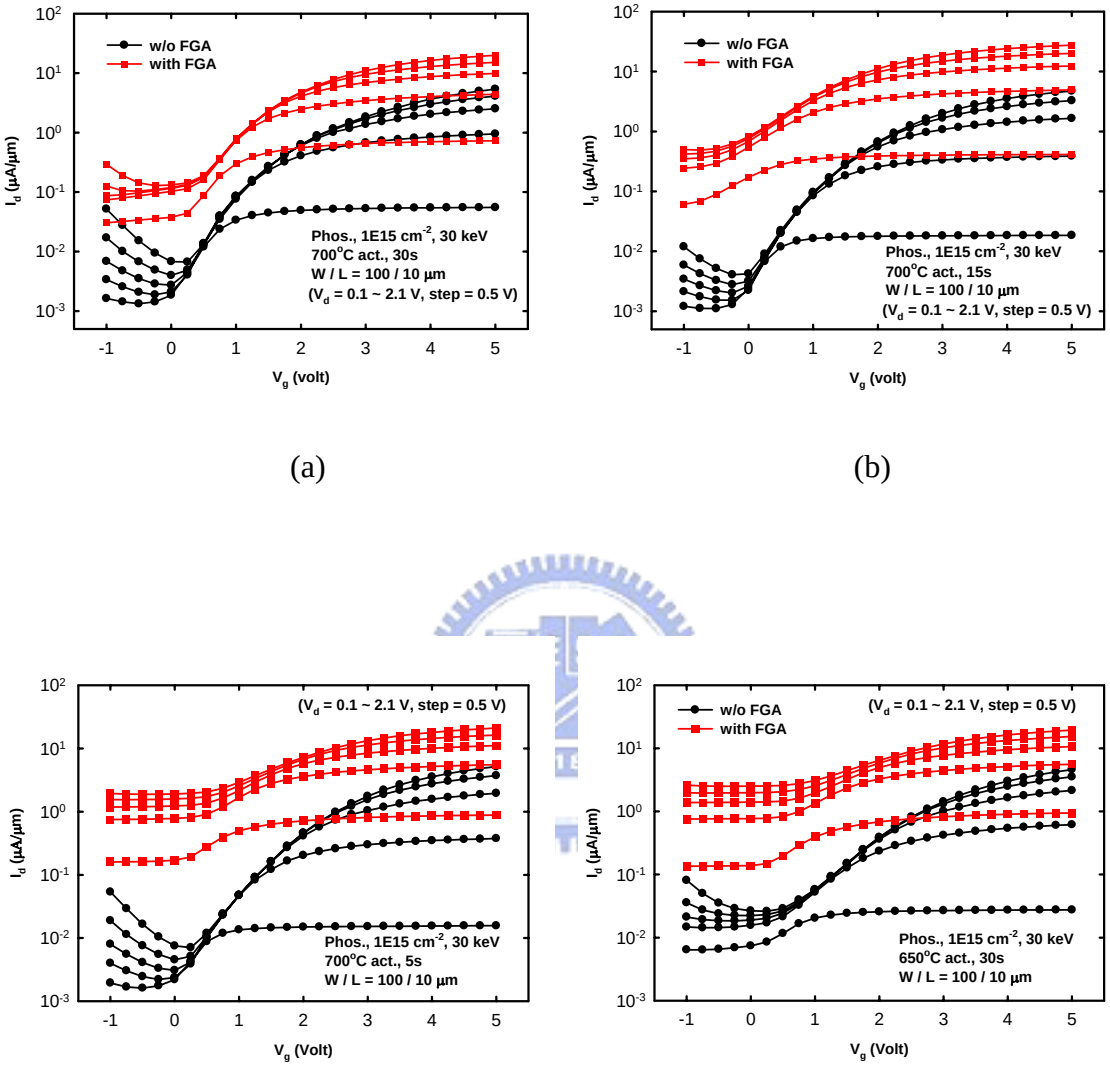


Fig. 4-2 The I_d-V_g curves of samples with and w/o FGA at 300 ℃ for 30min. (a), (b), (c), and (d) are (700 ℃, 30sec), (700 ℃, 15sec), (700 ℃, 5sec), and (650 ℃, 30sec), respectively. The label (# ℃, #sec) stands for the activation temperature and time.

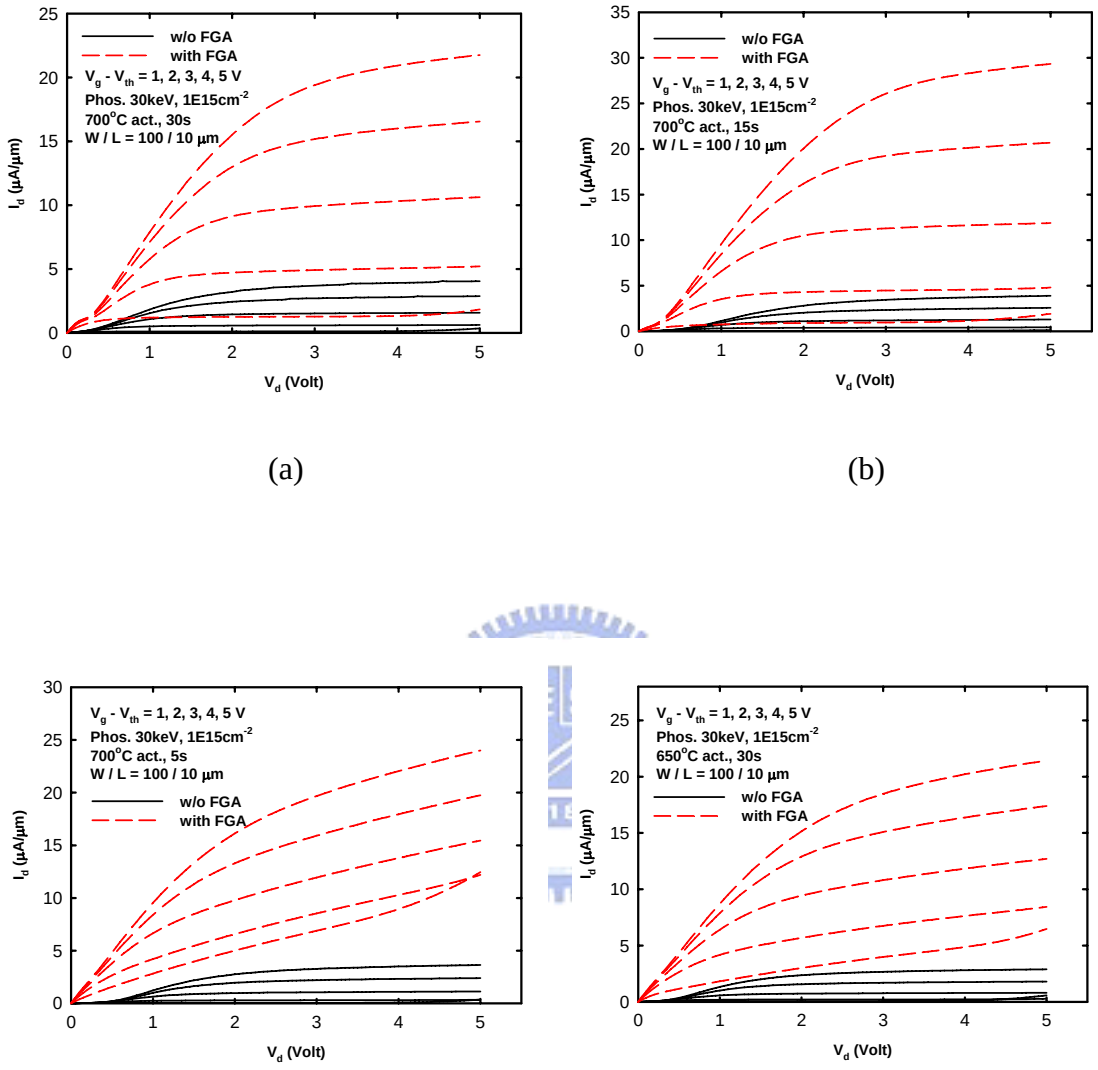


Fig. 4-3 The I_d-V_d curves of samples with and w/o FGA at 300 ℃ for 30min. (a), (b), (c), and (d) are (700 ℃, 30sec), (700 ℃, 15sec), (700 ℃, 5sec), and (650 ℃, 30sec), respectively. The label (# ℃, #sec) stands for the activation temperature and time.

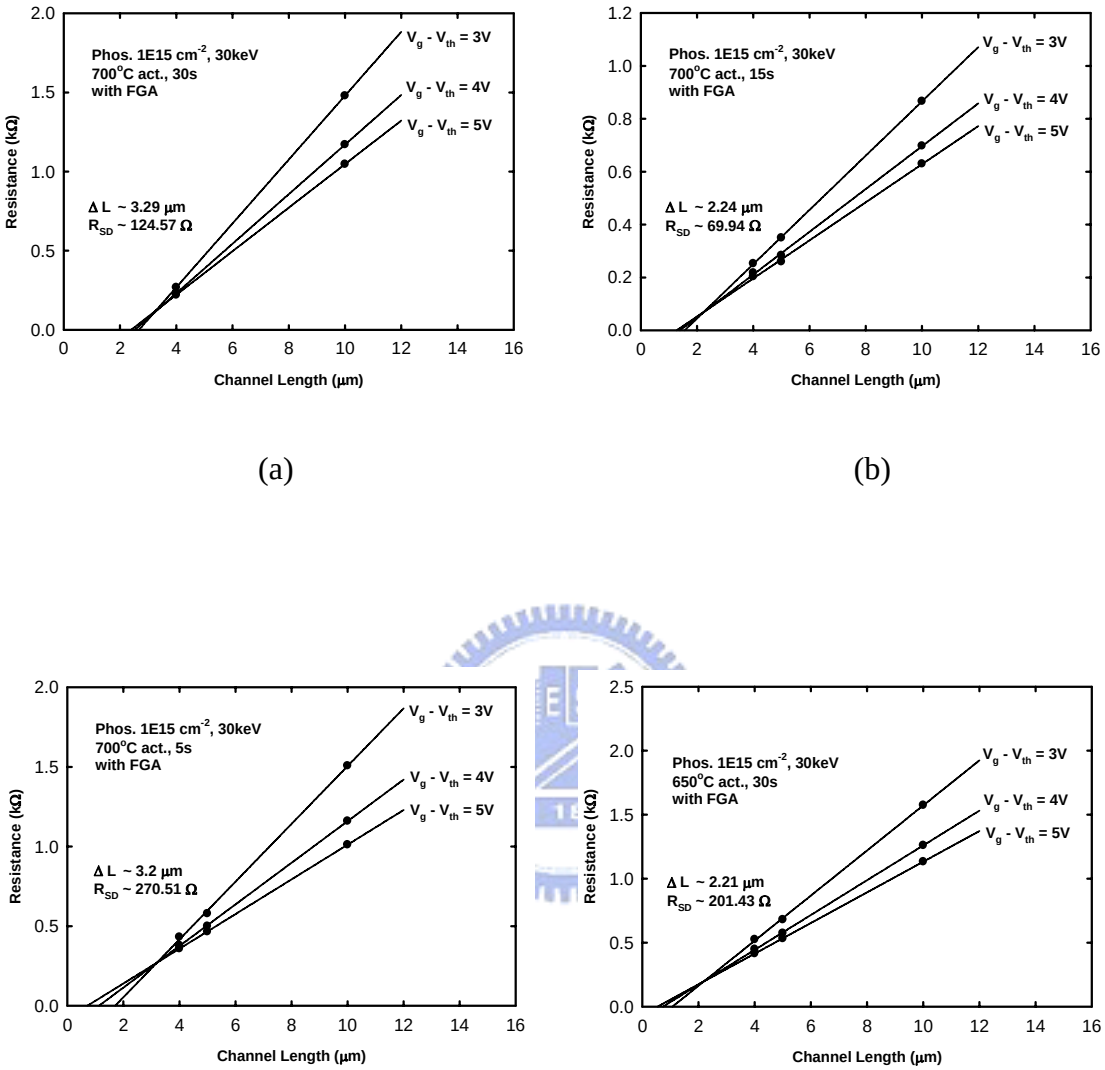
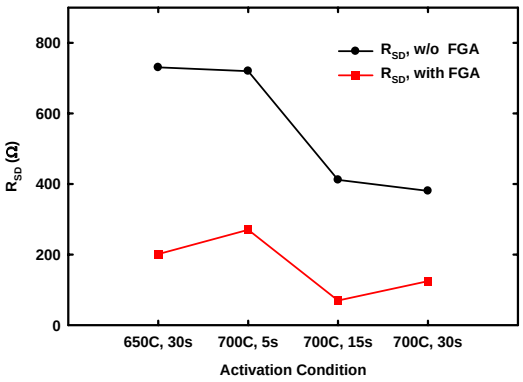
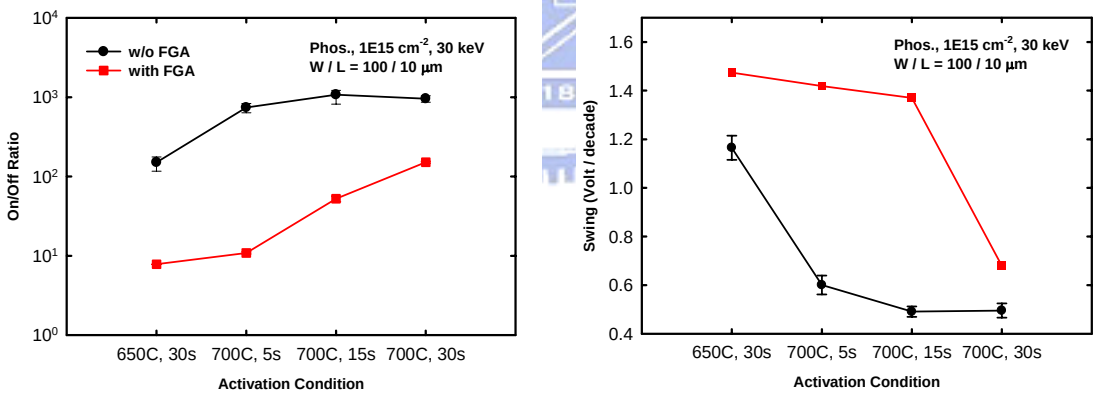


Fig. 4-4 The R_m-L_g fitting curves for extraction of R_{SD} and $\triangle L$. (a), (b), (c), and (d) are (700℃, 30sec), (700℃, 15sec), (700℃, 5sec), and (650℃, 30sec), respectively. The label (#℃, #sec) stands for the activation temperature and time.

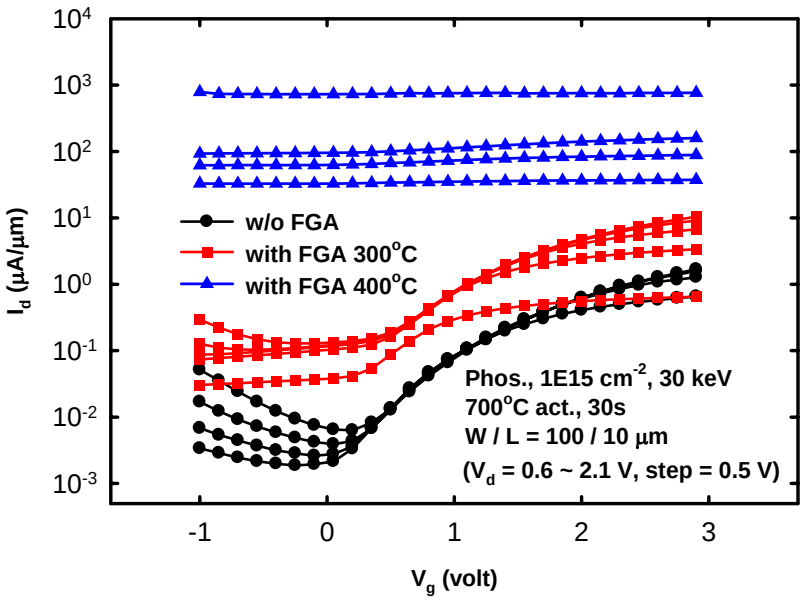


(a)

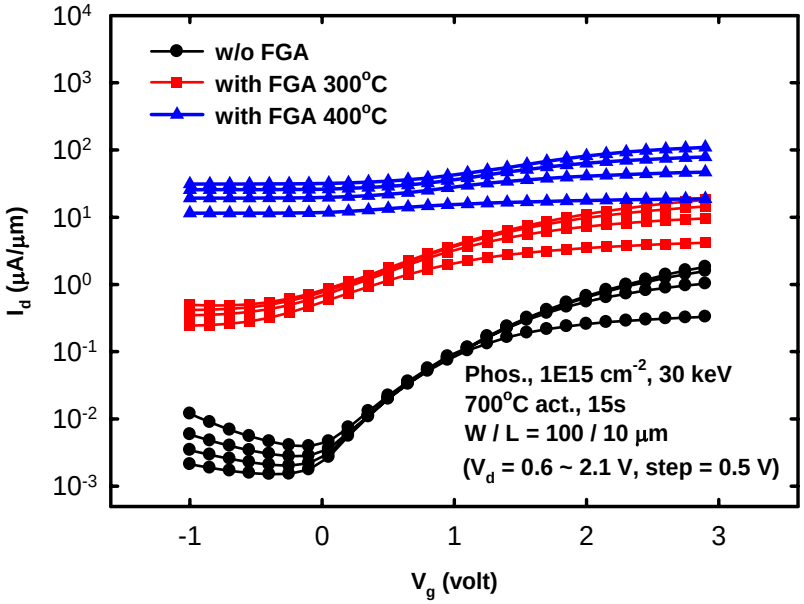


(c) (d)

Fig. 4-5 (a) shows the extracted R_{SD} from Fig. 4-4. (b) and (c) reveal extracted on-off ratio and swing, respectively. They are compared with samples without FGA. The label (# ℃, #sec) stands for the activation temperature and time.

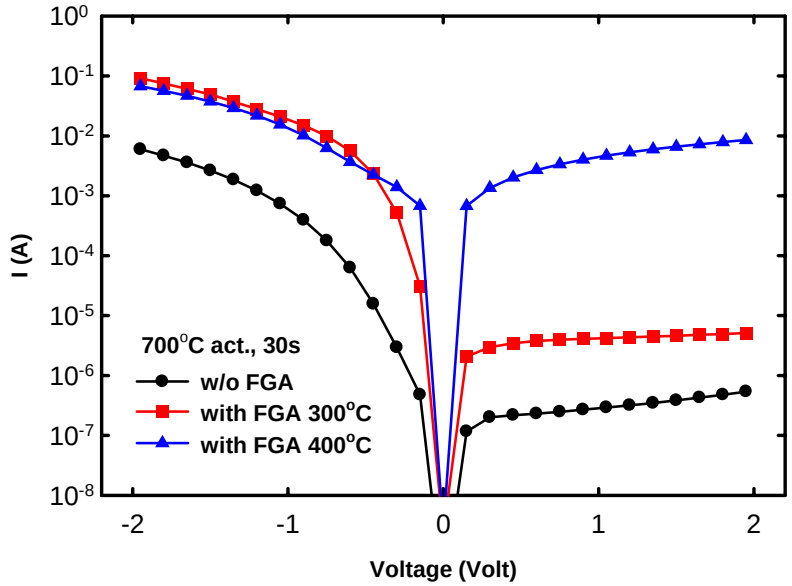


(a)

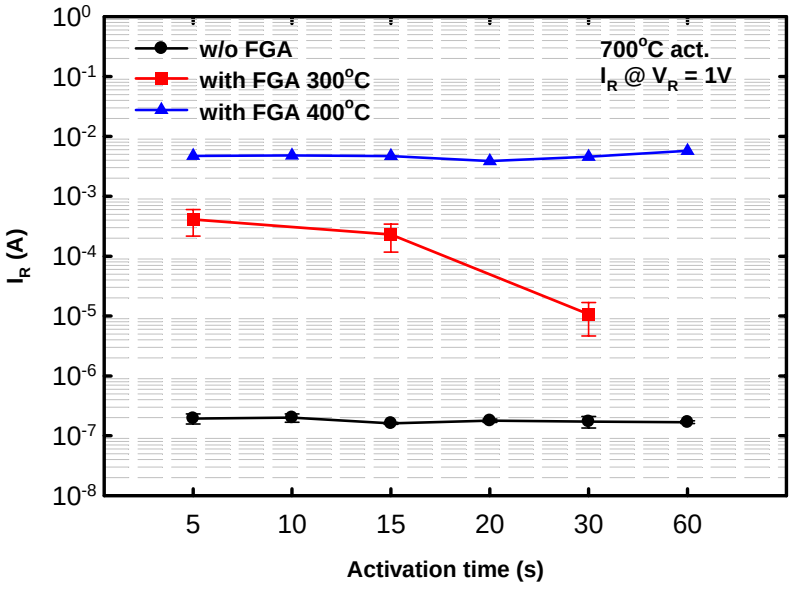


(b)

Fig. 4-6 (a) and (b) are for samples activated at 700℃ for 30sec and 15sec, respectively. They show the I_d-V_g characteristics with no FGA, FGA at 300℃, and 400℃.

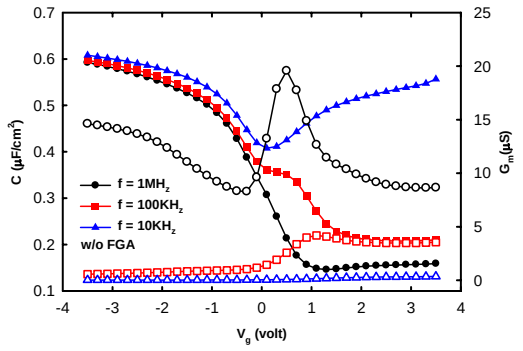


(a)

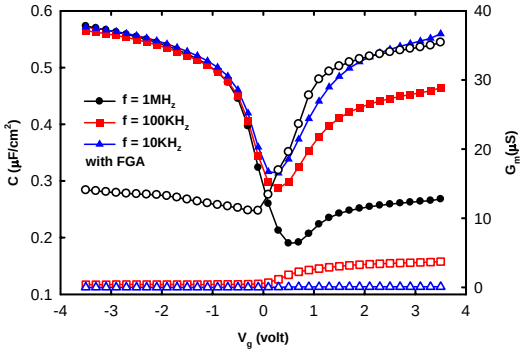


(b)

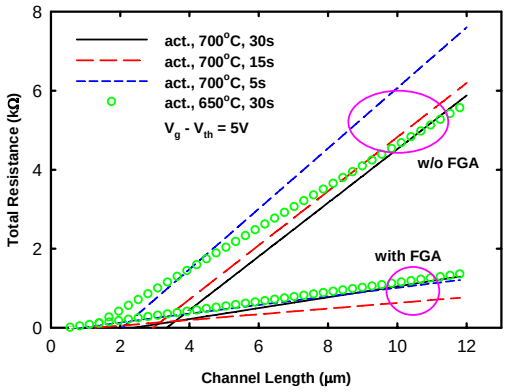
Fig. 4-7 (a) The I-V characteristics of n^+-p junction which activated at 700℃ for 30sec with no FGA, FGA 300℃, or FGA 400℃. (b) The reverse current at 1volt for some activation time ranging from 5sec to 60sec with no FGA, FGA 300℃, or FGA 400℃.



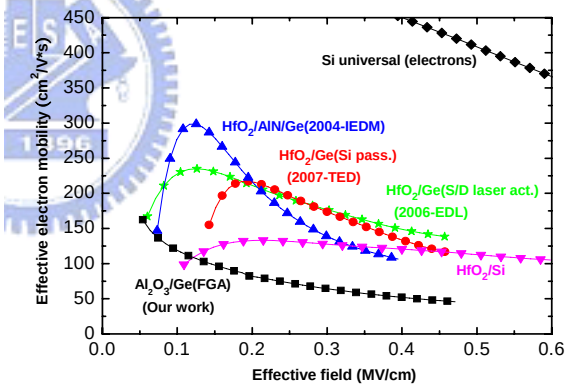
(a)



(b)

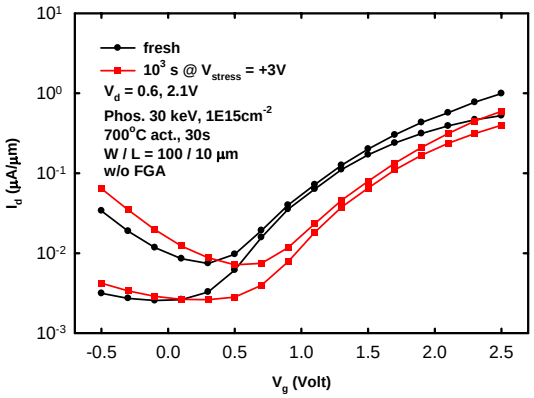


(c)

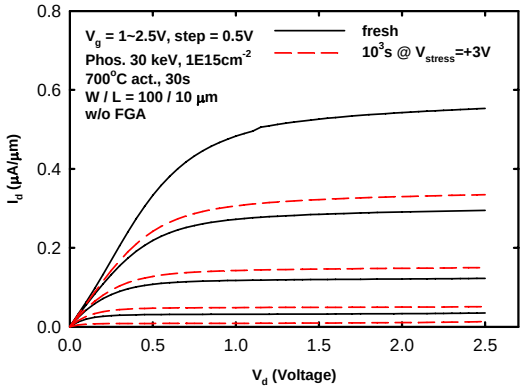


(d)

Fig. 4-8 (a) and (b) are the C-V (and G-V) characteristics of samples, whose structure is Al/Al_2O_3/p-type Ge, w/o and with FGA at 300℃, respectively. The solid and hollow patterns are for C and G, respectively. (c) It is plotted the fitting lines for V_g-V_{th}=5V for samples with and w/o FGA. (d) The extracted mobility compares with some publications.



(a)



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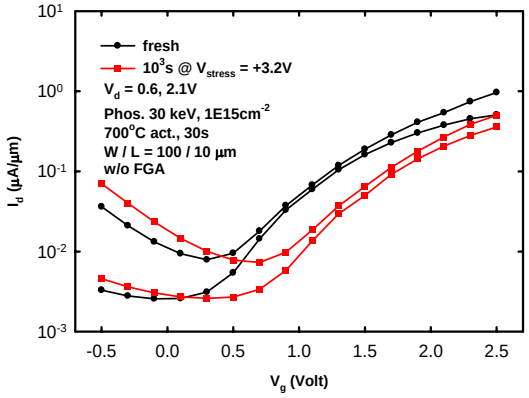
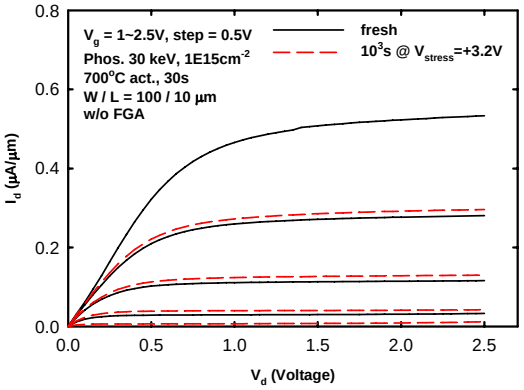


(c)



(d)

Fig. 4-9 (a)(b) and (c)(d) show the I_d-V_g and I_d-V_d characteristics before and after PBTI at V_{stress}=3V and 3.2V for 1000sec, respectively. The sample is chosen the one which is activated at 700℃ for 30sec without further FGA.

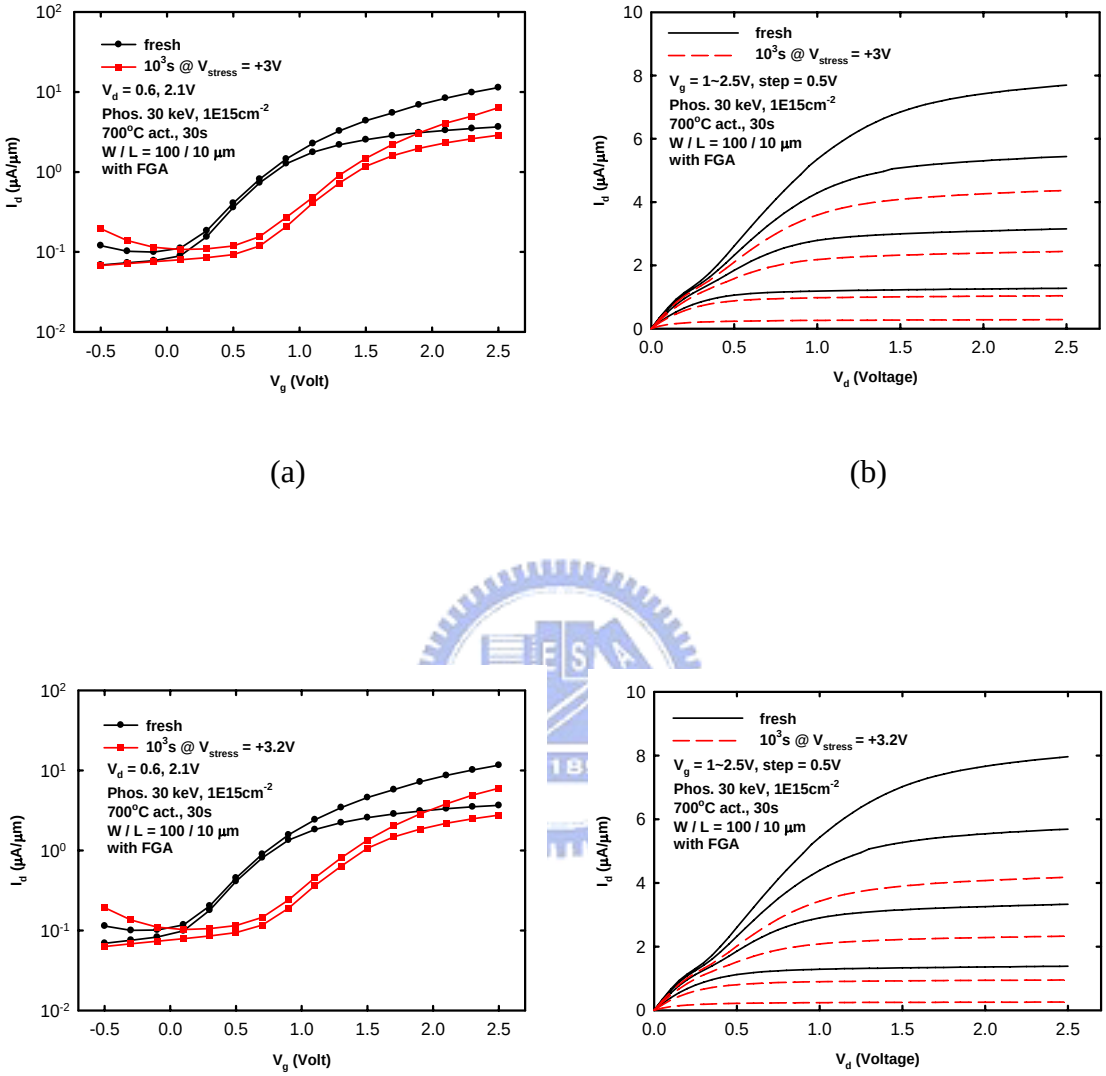
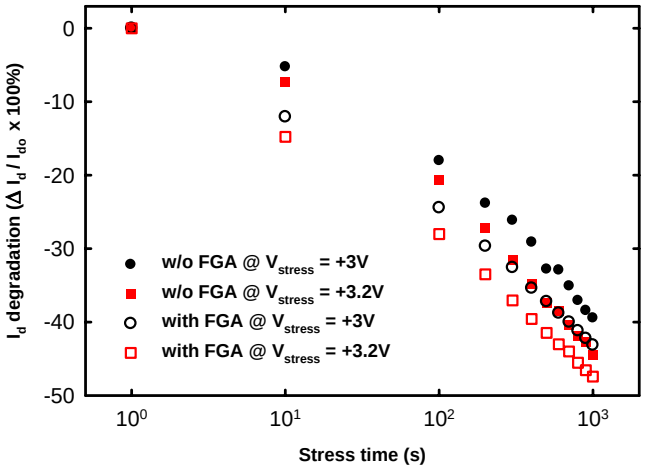
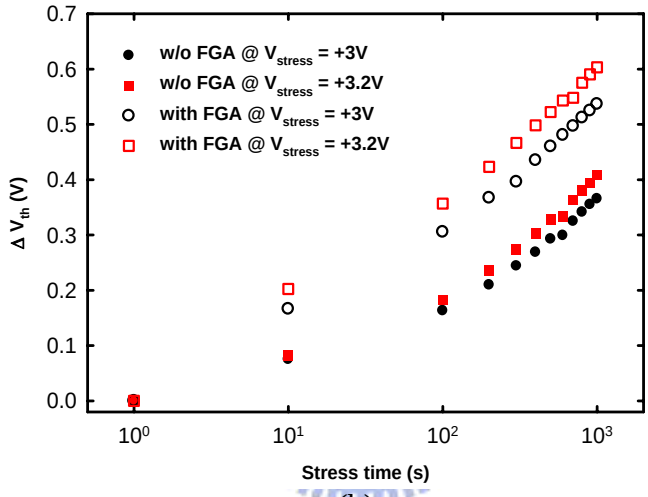


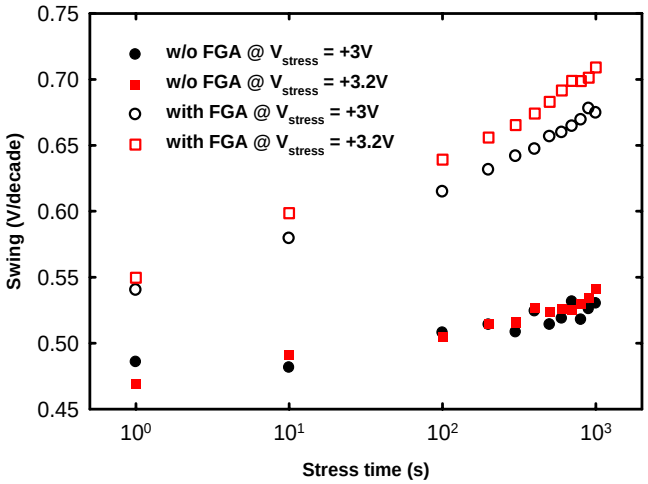
Fig. 4-10 (a)(b)and (c)(d) show the I_d-V_g and I_d-V_d characteristics before and after PBTI at V_{stress}=3V and 3.2V for 1000sec, respectively. The sample is chosen the one which is activated at 700℃ for 30sec with further FGA at 300℃ for 30min.



(a)



(b)



(c)

Fig. 4-11 It shows the degraded performances of (a) I_d, (b) $\triangle V_{th}$, and (c) swing by PBTI measurement. V_{stress} = 3V and 3.2V.

Chapter 5

Conclusions and Suggestions for Future Work

5-1 Conclusions

We had succeeded in optimizing the annealing conditions for the formation of n^+-p junctions on bulk Germanium. A reverse current about 2×10^{-4} A/cm^2 very close to our estimated ideal value about 1×10^{-4} A/cm^2 could be achieved. Moreover, the most important thing in our diode studies was the analysis of paths of the leakage current. We could find that no matter if capping SiO_2 before activation, the total leakage current was dominated by the "perimeter" component for activation at 500 and 600℃. With an increasing temperature more than 600℃, it shown the area leakage current became more dominant than perimeter component till 700℃. It meant the elimination of perimeter defects which led to a large value of J_P was the target of activation. Unfortunately, J_P was also inversely proportional to the square root of the area of implantation region. Hence, how to remove those perimeter defects should be the first aim. During our n^+-p junction studies, we also found a smaller contact resistance between Al and Ge would be obtained if a SiO_2 thin film was deposited before activation. In addition, samples with capping SiO_2 would get a decreasing contact resistance with an increasing activation temperature from 600 to 700℃. This behavior was opposite to samples without capping layer. The phenomenon could be attributed to their different surface concentrations which led to various energy barrier heights. Finally, a ratio of forward to reverse current about 5×10^4 at ±1 volt could be achieved.

In chapter 3, by utilizing the results of optimization of the activation processes, we subsequently fabricated Ge nMOSFETs with Al_2O_3 as our high-k gate dielectric and further

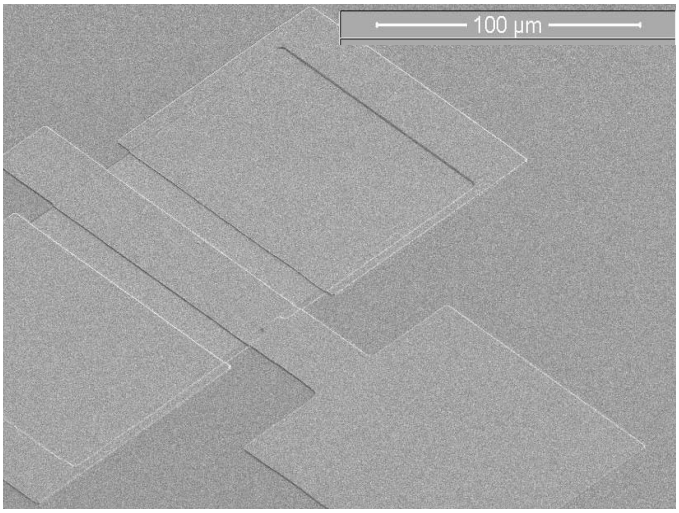
investigated their electrical performances. Not only I_d-V_g, I_d-V_d, and C-V performances, but also some electrical parameters, such as source-drain resistance, dopant in-diffusion length, and sub-threshold swing, were extracted to realize the device characteristics. Although we could achieve on-off ratios about 10^3 and 10^4 for drain and source currents, respectively, a severe source-drain resistance was also observed.

In chapter 4, we considered the forming gas annealing (FGA) process to improve the drawback. Some parameters were also extracted to compare together before and after FGA. It actually demonstrated not only source-drain resistance but also channel resistance could be much improved. Unfortunately, the junction leakage current became out of control and much degraded the electrical performances on our Ge nMOSFETs. The exact cause should be investigated by some further physical analysis.

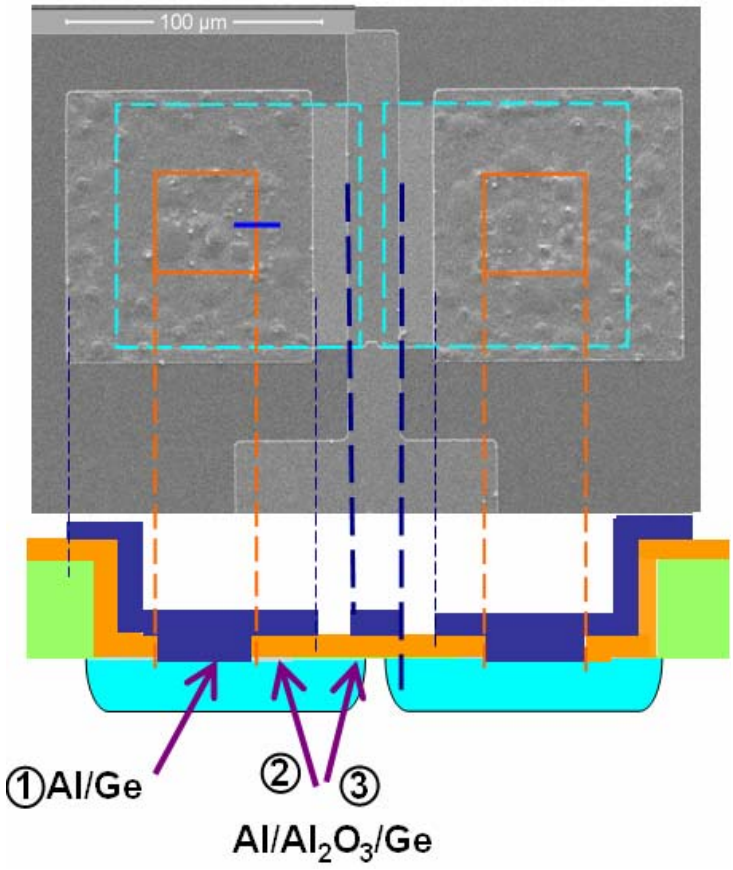
5-2 Suggestions for Future Work

In our diode studies, we demonstrated that the perimeter defects could be activated better with a higher annealing temperature. In other words, it seemed that there would be less interfacial density of states between Ge and field oxide SiO_2 as our activation temperature was higher. However, this part was only investigated from electrical analysis. It might be consisted with further physical studies such as TEM. Besides, we could also study the I-V characteristics of our n^+-p junctions under different operation temperatures.

In our Ge nMOSFETs studies, the most interesting thing was the degradation of S/D junctions. An initially physical analysis was shown in Fig. 5-1 and Fig. 5-2 which shown the top view and cross section by scanning electron microscope (SEM), respectively. Fig. 5-1(a) and Fig. 5-1(b) were the top view of our nMOSFET before and after FGA, respectively. An obviously difference was that the metal Al for S/D contacts had severe roughness after FGA. However, the metal Al for the gate was still smooth. Hence, it suggested that the roughness was not due to Al itself such as its low melting point. Considering Fig. 5-1(b), it also exhibited the cross section of our device. We attended to three locations which were labeled ①, ②, and ③. ① was the interface between Al and Ge; ②, and ③ were the $Al/Al_2O_3/Ge$ structure located at S/D and gate, respectively. By comparing the three locations, it seemed that the roughness was related to the direct contact of Al and n-type Ge. Then, two possible causes could be considered. One was Ge or P might out-diffuse, and another was Al might interact with Ge or P during FGA. Besides, comparing ② with ③, it also hinted Al_2O_3 was like a “barrier”. Hence, only S/D pads were roughness. In addition, we also tried to observe both the cross section of ① and ② before and after FGA in Fig. 5-2. However, Fig. 5-2 presented all interfaces of Ge were no obvious roughness compared with the top view of Al pads shown in Fig. 5-1. The exact cause should be further investigated.

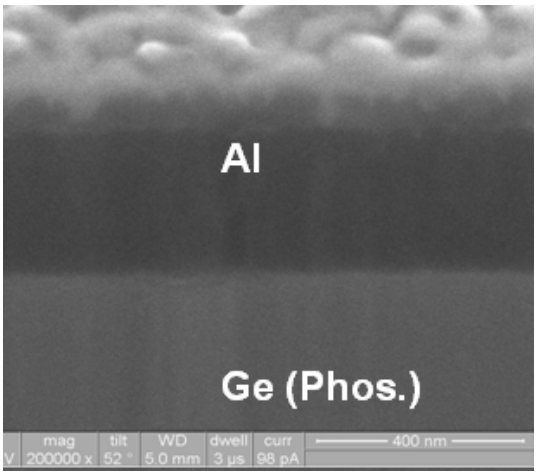


(a)

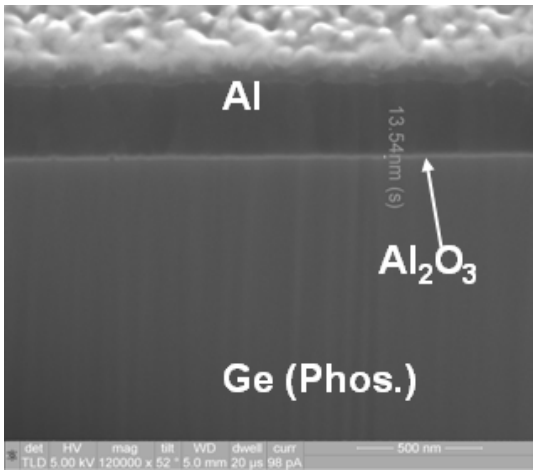


(b)

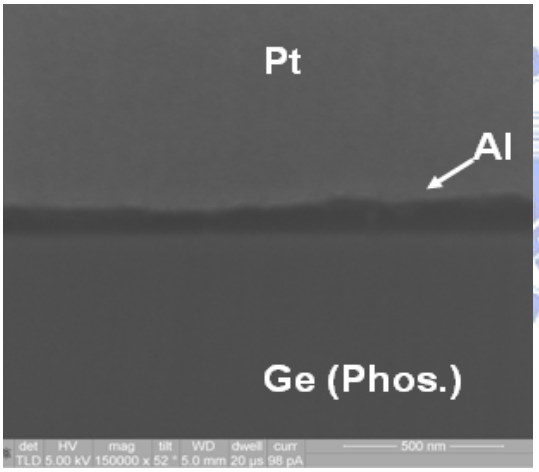
Fig. 5-1 (a) and (b) show the top view of our nMOSFET before and after FGA, respectively. Moreover, Fig. 5-1(b) also exhibits a brief picture for our device cross section corresponding to the real top view.



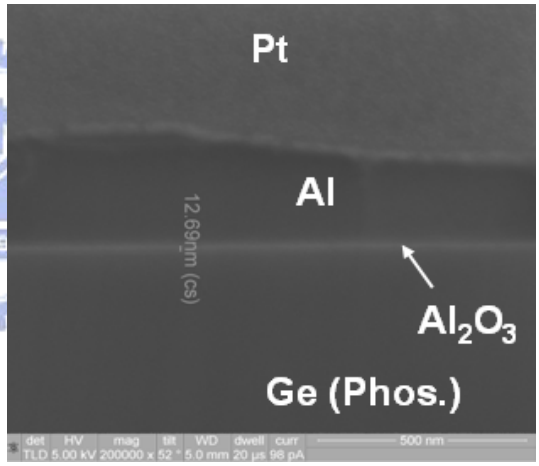
(a)



(b)



(c)



(d)

Fig. 5-2 (a),(b) and (c),(d) are the samples w/o and with FGA, respectively. (a) and (c) are corresponding to the location labeled ① in Fig.5-1(b). (b) and (d) are corresponding to the location labeled ② in Fig.5-1(b).

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於鍺基板製作n^+-p型二極體及n型金氧半場效電晶體之電性研究

(*Electrical characteristics of n^+-p junction and nMOSFETs on bulk Germanium*)