國立交通大學

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博士論文

雙重電漿處理技術應用於具高介電常數閘極絕緣層的金屬-絕緣層-半導體電容及低溫多晶矽薄膜電晶體之特性研究

Investigation of Dual Plasma Treatment Technology on MIS Capacitor and Low Temperature Polycrystalline Silicon Thin Film Transistor with High-κ Gate Dielectric

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中文摘要

閘極長度及閘極氧化層的快速微縮會產生過大的閘極穿隧漏電流及元件可靠度的問題，使用高介電常數材料取代傳統閘極二氧化矽可以有效解決此問題，高介電質材料可以在較大的物理厚度下仍然維持較低的等效氧化層厚度，進而降低閘極的穿隧漏電流並且維持較好的元件特性。在過去有許多論文曾經用電漿氮化或電漿氟化處理對高介電常數材料薄膜使其達到較佳的特性，電漿氮化及電漿氟化對於提升元件特性各有其優點，在本篇論文中，我們提出雙重電漿處理的方式，結合沉積高介電薄膜前的電漿氟化處理及沉積後高介電薄膜後的電漿氮化處理二種優點，並將此技術應用在具高介電材料的金屬-絕緣層-半導體電容及低溫多晶矽薄膜電晶體結構上，以期結合兩種電漿處理之優點以更進一步提升元件的電特性及可靠度。

首先，我們將雙重電漿處理技術應用具二氧化鉿的金屬-絕緣層-半導體電容結構上，並探討其電特性及可靠度，並且分析其電流傳導機制。根據結果顯示，經過雙重電漿處理的樣品均有顯著的改善，包括電容密度的提升、漏電的降低、

遲滯現象的改善，雙重電漿處理可以有效消除介電質薄膜中的缺陷、消除表面狀態的數目、提升元件可靠度。另外，經雙重電漿處理後之二氧化鉿電容器，其漏電流機制主要是由三種漏電機制所主導，分別是蕭基發射(Schottky emission)主導中低電場，弗崙克爾-普爾發射(Frenkel-Poole emission)主導於中高電場以及福勒-諾德海姆穿隧(Fowler-Nordheim tunneling)主導於高電場。

其次，我們也將雙重電漿技術應用在具氧化鉿鋁之金屬-絕緣層-半導體電容結構上，根據實驗結果，雙重電漿處理一樣可以有效提升其電特性及可靠度，改善介面品質，增加其崩潰電壓。

最後，我們將電漿處理技術應用在多晶矽薄膜電晶體上，希望藉由雙重電漿電漿處理可以鈍化二氧化鉿高介電常數材料內的氧空缺與基板的表面缺陷，亦可修補多晶矽薄膜通道的缺陷，結果顯示，經過雙重電漿處理的樣品，臨界電壓(V_{th})、次臨界擺幅(S.S.)、轉導(G_m)、載子遷移率(μ_{eff})都可以很有效的改善，表面狀態數目(D_{it})及多晶矽中的缺陷密度(N_{trap})也有效的降低。另外經由低頻雜訊(1/f noise or flicker noise)的量測可發現經過雙重電漿處理過的元件其表現出來的雜訊較低，表示其介面及通道缺陷可以有效被修補。藉由可靠度的分析，包括給予閘極正偏壓應力(PBS)、閘極負偏壓應力(NBS)、閘極正偏壓高溫應力(PBTI)、熱載子應力(HCS)可觀察到介面層之陷阱能態密度(ΔN_{it})及氧化層缺面密度(ΔN_{ot})。結果顯示，經過雙重電漿處理過的樣品表現出較佳的元件電特性、較強的應力抵抗能力並提升元件的可靠度。

Investigation of Dual Plasma Treatment Technology on MIS Capacitor and Low Temperature Polycrystalline Silicon Thin Film Transistor with High-κ Gate Dielectric

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Abstract

The aggressive shrinking of the gate length and gate dielectric thickness accompanies excessive leakage current and reliability problems. To solve these problems, a major solution is to replace the traditional SiO_2 or SiON by High-dielectric-constant (high-κ) material. The improvement in the electrical characteristics of HfO_2 thin film with plasma nitridation process or plasma fluorination process has also been examined. In this dissertation, dual plasma treatment, CF_4 pre-treatment and nitrogen post-treatment, was performed on HfO_2 MIS capacitor and low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs).

First, dual plasma, CF_4 pre-treatment and nitrogen post-treatment, treatments were performed on HfO_2 MIS capacitor. We examine electrical characteristics,

reliability properties and current conduction mechanisms of HfO_2 MIS capacitor. According to the this study, HfO_2 gate dielectric properties including capacitance density, gate leakage current density, and hysteresis could be improved by dual plasma treatment. The dominant current conduction mechanism in HfO_2 layer was Schottky emission type in the region of low to medium electric fields; Frenkel-Poole (F-P) emission operated in the region of medium to high fields; Fowler-Nordheim (F-N) tunneling was dominant at high fields. Dual plasma treatment was effective in improving interface quality, eliminating shallow trap levels, and enhancing reliability properties.

Secondly, in order to improve the reliability and thermal stability of the HfO_2 dielectrics. Al could be added to HfO_2 forming $HfAlO_x$ to increase the crystallization temperature. Similarly, we use dual plasma treatment to examine interface quality and reliability properties of $HfAlO_x$ MIS capacitor. Based on our results, the electrical characteristics including C-V, I-V, hysteresis, frequency dispersion, and CVS characteristics of HfAlOx gate dielectrics could be great improved by dual plasma treatment.

Finally, the dual plasma treatment is successfully utilized on the LTPS-TFTs. The improvement of electrical characteristics has been studied, including the hysteresis and the I-V characteristics. The device parameters, such as V_{th}, S.S., G_m, μ_{eff}, D_{it}, and N_{trap} are extracted to verify the improvement effect. It shows that the sample with dual plasma treatment have better electrical characteristics. Also, according to the $1/f$ noise (flicker noise) measurement, dual plasma treatment could effectively reduce the grain-boundary trap-state densities at the channel and the oxide traps at the oxide/poly-Si interface. Furthermore, the reliability properties and mechanisms of high performance HfO_2 gate dielectric LTPS-TFT with dual plasma treatment are

investigated, including positive bias stress (PBS), negative bias stress (NBS), positive bias temperature instability (PBTI), and hot carrier stress (HCS). Also, in order to indicate the damage region induced by HCS, the output characteristics of the normal mode and reverse mode (S/D reverse) of the sample after HCS. In conclusion, TFT with dual plasma treatment has better stress immunity than the sample without treatment.

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Contents

Table Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 1

Introduction

1.1 Background

The complementary metal oxide semiconductor (CMOS) field effect transistor (FET) plays the important role in modern electronic industry. In order to have greater integrated circuit functionality, lower power consumption, higher performance, and lower cost, the demand of the industry requires the higher density of transistors on the wafer, which means the feature size of the transistor need to become smaller. In 1965, Gordon E. Moore proposed the "Moore's law" to predict the number of devices increases doubled per wafer every year [1], and he revised the projection of law from every year to every two year in 1975 [2].

The drive current associated with metal oxide semiconductor (MOS) field effect transistor (FET) could be written as

$$I_D = \frac{W}{L}\mu C_{inv}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \quad , \tag{1}$$

where W and L are the width and channel length of the transistor channel respectively, μ is the channel carrier mobility, C_{inv} is the capacitance density associated with the gate dielectric when the transistor is inverted, V_G is the voltage applied on transistor's gate, V_T is the threshold voltage, V_D is the applied voltage on drain terminal of the transistor. At first, the drain current (I_D) increases linearly with the drain voltage (V_D)

and finally saturates to maximum at $V_D=V_G-V_T$, leading to

$$I_{D,sat} = \frac{W}{L}\mu C_{inv}\frac{(V_G - V_T)^2}{2} \quad . \tag{2}$$

According to eq. (2), there are some ways to improve the performance, including increase the term (V_G-V_T), reduce the channel length (L), and increase the channel width (W) and the gate dielectric capacitance (C_{inv}).

In terms of the increase (V_G-V_T), it is limited in a range because of reliability and room temperature operation constraints [3]. Too large V_G will create undesirable high electric field across the gate dielectric, inducing the high leakage current, high power consumption, and reliability problems. Moreover, V_T could not easily be reduced below 200 mV. Because kT is approximate 25mV at room temperature, the specific temperature would adversely affect the V_T value, causing statistical fluctuation in thermal energy.

Even through the shrinkage of the channel length (L) could achieve density, speed, and power improvements, the scaling cannot go on forever. The continue shortening of the channel length will not only increase the fabrication complexity but also cause the undesirable physical phenomena, which called short-channel effect [4]. There are five different effects of short channel in MOSFET, such as drain-induced barrier lowering (DIBL) or punch-through, velocity saturation, channel length modulation, source-drain series resistance, and MOSFET breakdown [5]-[8].

An FET is a capacitance-operated device; in other words, the source-drain current of the FET depends on the gate capacitance C_{ox}. The C_{ox} which ignored depletion effects and quantum mechanism for silicon substrate [9] could be written

$$C_{ox} = \frac{\varepsilon_0 \kappa A}{t}, \tag{3}$$

where ε_0 is the permittivity of free space (8.85×10^{-14} F/cm), κ is the dielectric constant (relative permittivity) of the material, t is thickness of the gate oxide dielectric and A is the area of the capacitor. Based on eq. (3), the gate capacitance could be increased by decreasing the thickness of the gate oxide. However, the aggressive shrinking of the gate length and gate dielectric thickness accompanies excessive leakage current and reliability problems. Fig. 1-1 shows the prediction of the gate oxide (SiO_2) thickness for feature technology node. According to the prediction, the gate oxide would be so thin that would be 1.3 nm in 2012, which only consists of three atomic layers [10]. Fig. 1-2 shows the gate leakage current with different oxide thickness. The direct tunneling leakage current from the quantized inversion layer increase exponentially with decreasing oxide thickness [11]. The leakage current becomes problematic when oxide thickness below 20 Å. To solve these problems, a major solution is to replace the traditional SiO_2 or SiON by other higher dielectric constant material.

1.2 High-κ gate dielectric

1.2.1 Advantages of high-κ gate dielectric

In terms of the electrical design of the device, it is convenient to define an electrical thickness of the high-κ gate dielectric. According to eq. (3), the capacitance could be expressed in terms of t_{eq} (equivalent oxide thickness (EOT)) and 3.9 (dielectric constant of SiO_2).

$$t_{eq} = EOT = \left(\frac{3.9}{\kappa_{high-\kappa}}\right) t_{high-\kappa}. \quad (4)$$

The term t_{eq} represents the theoretical thickness of SiO_2 that was required to achieve the same capacitance density as the dielectric. Using high dielectric constant material for gate dielectric could have larger physical thickness and maintain smaller equivalent oxide thickness (EOT), as shown in Fig. 1-3. The direct tunneling current would be decreased due to larger physical thickness. Compared to the high performance microprocessor market, transistors with lower (about 10^{-3} A/cm^2) leakage currents would be required for the rapidly growing market of low-power applications. Fig. 1-4 shows the gate current density and the standby power consumption as a function of gate voltage. Compared to 15 Å oxide, the high-κ gate dielectric with same EOT shows the great reduction of the gate leakage and power consumption. As a result, the gate dielectric with higher permittivity than oxide is required for low power device. In short, high-dielectric-constant (high-κ) thin films have been considered as suitable gate dielectric for modern CMOS technology.

1.2.2 Choice of the high-κ gate dielectric

To minimize the direct tunneling current, the ultrathin silicon oxynitride (SiON) is a solution to replace silicon oxide (SiO_2) when conventional oxide cannot be scaled down. Several researches focus on applying different methods to optimize the quality of ultrathin oxynitride to substitute conventional oxide since 1990 [12]-[15]. It has been reported that oxynitride has ability to prevent boron diffusion from gate electrode to substrate in pMOSFETs [16, 17], suppress the hot-carrier degradation and enhance electron mobility in nMOSFETs [18, 19], and reduce the equivalent oxide thickness or leakage current [20, 21]. The dielectric permittivity (κ) of oxynitride depends on its content of nitrogen. Unfortunately, the oxynitride only extends the gate dielectric two or three (90-40nm) generations because the κ value is not higher enough. As a result, high-κ material becomes a candidate to replace conventional

oxide and oxynitride. The principle of choosing the high-κ material is described as follows [22]:

(a) The κ value must be high enough.

Table 1-1 shows the main high-κ gate dielectric materials with their parameters: ε is the permittivity, Eg is the band gap, CBO is the conduction band offset, and VBO is the valence band offset [23]. Fig. 1-5 depicts the relation between the κ value and the dielectric band gap [24]. It can be seen that the κ value tends to vary inversely with the band gap. The first requirement is the κ value should be over 12. There are numerous dielectrics with extremely large κ value, but with unsuitable low band gap. Furthermore, a very large κ is undesirable in CMOS design due to undesirable fringing fields at the source and drain electrode [25]. Consequently, the dielectric, such as HfO_2, ZrO_2, and La_2O_3, with κ value within 25-30 is preferable in CMOS technology.

(b) High-κ dielectric should be thermodynamically stable with Si channel.

There usually have extensive inter-diffusion effects or chemical reactions when direct growing high-κ gate dielectric on silicon substrate, resulting in the properties degradation of the gate dielectric, the underlying silicon, or both [26]. The required property of the dielectrics is that it must not react with Si forming either SiO_2 or silicide according to the unbalanced reactions

$$MO_2 + Si \rightarrow M + SiO_2, \tag{5}$$

$$MO_2 + 2Si \rightarrow MSi + SiO_2. \tag{6}$$

This reason is that forming SiO_2 layer would increase the EOT and negate the effect of using high-κ gate dielectric, whereas forming silicide (eq. (6)) would short out the

field effect.

It could be used a ternary phase diagram with tie lines to represent the stability of a gate dielectric in contact with Si, as shown in Fig. 1-6. Tie lines which connect two compositions represent that they could be with each other in equilibrium [22]. As shown in Fig. 1-6(a) and Fig. 1-6(b), MO_x could not directly connect to Si unless via the SiO_2, for example Ta_2O_5 or TiO_2. On the other hand, metal oxide dominant type shown in Fig. 1-6(c) has a tie line between MO_x and Si, which means that high-κ metal oxides could direct connect to Si, such as ZrO_2. In short, it should be focus on metal oxide dominant type for choosing high-κ materials, like ZrO_2, HfO_2, Al_2O_3, Y_2O_3, La_2O_3, Sc_2O_3 and some lanthanides such as Pr_2O_3, Gd_2O_3 and Lu_2O_3.

(c) Higher energy band gap and conduction band offset with Si should over 1 eV.

The high-κ material should act as a gate insulator in MOS structure. In that case, it requires that the potential barrier at each band must be over 1 eV so that could inhibit conduction by the Schottky emission of electrons or holes into the oxide band [24], as shown schematically in Fig. 1-7. Fig. 1-8 depicts the calculated conduction band and valence band offsets of various oxide on Si. In general, the conduction band offset is usually smaller than the valence band offset; therefore, the limits of the choice on high-κ material should with band gap over 5 eV. The high-κ material such as ZrO_2, HfO_2, Al_2O_3, Y_2O_3, La_2O_3 and various lanthanides and their silicates and aluminates could satisfy this criterion.

(d) Interface quality

The oxide is directly contact with Si channel, while the carriers in the channel flow within angstroms of the Si-oxide interface. Therefore, the interface must be the highest electrical quality; in other words, the interface should have less roughness and

absence of interface defects.

(e) Defects

Defects in the dielectric are the electronic states in the band gap of the oxide, which are usually generated by oxygen vacancies or impurities. There are some reasons that defects are undesirable and should be greatly reduced. First, charge trapped in the defects states in the oxide band gap and would change with time, resulting in the threshold voltage shift and instability of operation voltage. Second, the trapped charge in the defect would induce carrier scattering within the channel, leading to carrier mobility degradation. Third, defects cause the electrical reliability problems of the devices, such as hysteresis, breakdown, hot-carrier stress (HCS), stress-induced leakage current (SILC), time dependent dielectric breakdown (TDDB), positive bias temperature instability (PBTI), and negative bias temperature instability (NBTI).

1.2.3 Hf-based high-κ gate dielectric

In order to replace conventional SiO_2 as a gate dielectric thin film, high-κ materials have been investigated, such as ZrO_2 [27-29], HfO_2 [30-32], Ta_2O_5 [33], TiO_2 [34-36], Y_2O_3 [37-39], Al_2O_3 [40, 41], La_2O_3 [42]. Ta_2O_5 and TiO_2 have too low conduction band offset with Si, thus the leakage current is sensitive to temperature. Al_2O_3 has the disadvantage of a rather low κ value, whereas Y_2O_3 has not only lower κ value than HfO_2 but also poor thermal stability due to heavily reactive with Si. La_2O_3 has a slightly higher κ than HfO_2, it is hygroscopic though. Although ZrO_2 and HfO_2 are both generally believed to be two good materials for high-κ gate dielectric, it was found that ZrO_2 was slightly reactive with Si forming the silicide $ZrSi_2$ [22]. For this reason, HfO_2 was presently the preferred high-κ gate dielectric over ZrO_2.

In short, HfO_2 is a promising gate dielectric layer because it has high dielectric constant (κ ~ 25), relatively large band gap (Eg ~ 5.7 eV), large conduction band offset with Si (~1.5 eV), and stable contact with Si.

1.3 Current conduction mechanisms

The current conduction mechanisms in Hf-based gate dielectrics should be identified. They are generally attributed to Schottky emission (SE), Frenkel-Poole (F-P) emission, and Fowler-Nordheim (F-N) tunneling. Each current transport mechanisms will be introduced in the following.

1.3.1 Schottky emission (SE)

Electrons get enough thermal energy to overcome the potential barrier of the dielectric and transport to the anode, called Schottky emission or thermionic emission. The charge transport process of S.E is shown in Fig. 1-9. The standard Schottky emission could be expressed as

$$J_{SE} = A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right], \qquad A^* = 120\frac{m^*}{m_0}\ \left(\frac{A}{cm^2K^2}\right), \tag{7}$$

where J_{SE} is the current density, A^* is the effective Richardson constant, E is the electric field, T is the absolute temperature, q is the electron charge, $q\phi_B$ is the Schottky barrier height, k is Boltzmann's constant, ε_0 is the permittivity of free space, ε_r is the dynamic dielectric constant, m^* is the electron effective mass, and m_0 is the free electron mass.

1.3.2 Frenkel-Poole (F-P) emission

When gate under negative bias, electrons will inject from gate into the dielectric layer and will be trapped into shallow trap levels. Thereafter, the electrons transported through the dielectric layer by hopping between these trap levels, leading to leakage current, called Frenkel-Poole (F-P) emission. The charge transport process of F-P is shown in Fig. 1-10. The standard F-P emission could be expressed as

$$J_{FP} = C_t E \exp\left[\frac{-q\left(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right], \quad (8)$$

where J_{FP} is the current density, E is effective electric field, C_t is a constant proportional to the density of bulk oxide traps, $q\phi_t$ is the trap energy in oxide, and other parameters are as defined earlier. For the standard Frenkel-Poole emission, a plot of $\ln(J_{FP}/E)$ versus $E^{1/2}$ should be linear. It was found that F-P emission is the dominate conduction mechanism in the region of medium to high electric fields

1.3.3 Fowler-Nordheim (F-N) tunneling

In higher electric field, the Fowler-Nordheim (F-N) tunneling dominated the conduction mechanism. The injection of electrons from the gate entered the conduction band of HfO_2 by tunneling through a triangular potential barrier. The charge transport process of F-N is shown in Fig. 1-11. The standard F-N emission could be expressed as

$$J_{FN} = AE^2 \exp\left[\frac{-8\pi\sqrt{2m^*}\left(q\phi_f\right)^{3/2}}{3qhE}\right], \quad (4)$$

where J_{FN} is the current density, h is the Plunk's constant, m^* is the electron effective mass in oxide, and $q\phi_f$ is the potential barrier height.

1.4 Motivation

The rapid progress of complementary metal oxide semiconductor (CMOS) integrated circuit technology has met several serious technological challenges over the past few years. According to the prediction of the International Technology Roadmap for Semiconductor (ITRS), the conventional gate dielectric layer will reach its physical limits. Gate dielectric scaling of CMOS will increase the speed and the packing density of modern circuits. However, the aggressive shrinking of the gate length and gate dielectric thickness accompanies excessive leakage current and reliability problems. To solve these problems, a major solution is to replace the traditional SiO2 or SiON by other higher dielectric constant material. Using high dielectric constant material for gate dielectric could have larger physical thickness and maintain smaller equivalent oxide thickness (EOT). As a result, high-dielectric-constant (high-κ) thin films have been considered as suitable gate dielectric for modern CMOS technology. There are various high-κ thin film has been investigated. Among these high-κ materials, HfO_2 is considered as the most promising candidate because of high dielectric constant (~25), wide band gap (~5.7 eV), and large band offset with Si conduction band (~1.5 eV). Nevertheless, there are still some issues which need to be considered, such as the reliability and thermal stability of the dielectrics.

1.4.1 Plasma nitridation

It has been reported that nitrogen incorporated into HfO_2 gate dielectrics has beneficial effect on performance [43]. As reported in previous study, nitrogen incorporation can suppress crystallization during high temperature treatment, reduce

dopant penetration, increase dielectric constant, and reduce leakage current by about 3-4 orders of magnitude [44]. Umezawa et al [45] noted that nitrogen could deactivate the oxygen vacancy related states within HfO_2 band gap. The absence of gap states leads to the removal of electron leakage path. Fig. 1-12 illustrates the leakage reduction mechanism of the nitrogen incorporated in HfO_2 thin film. When two nitrogen (N) atoms are located nsearby the oxygen vacancy (V_o), two electrons which trapped at the Vo level are transferred to N atoms. As shown in Fig. 1-12(b), the relaxation of Hf atoms causes the elimination of V_o level state, resulting to the removal of electron path in the band gap.

1.4.2 Plasma fluorination

In recently years, the formation of an interfacial layer (IL) at HfO_2/Si interface during the growth of dielectric thin film and post processing appears to be a critical issue. Because of low dielectric constant of IL, IL limits the reduction of the effective oxide thickness (EOT). The quality of interfacial layer (IL) becomes more and more important due to gate dielectric scaling. Wang et al noted that the applied electric field would be largely distributed at low-κ layer in high-κ/low-κ stack layer; as a result, the first breakdown happened in the low-κ layer [46].

$$\frac{E_{low-\kappa}}{E_{high-\kappa}} = \frac{\kappa_{high-\kappa}}{\kappa_{low-\kappa}}. \tag{5}$$

Fluorine incorporation also has some improvement on electrical characteristics [47, 48]. Fluorine incorporated into dielectric layer could improve IL quality because of stronger bonding energy of Si-F bonds (5.73 eV) compared to Si-H bonds (3.18eV) [49]. Furthermore, IL at HfO_2/Si interface could be suppressed by CF_4 pre-treatment [50]. The hysteresis also could be suppressed by fluorine, which could be explained

by inner-interface model as shown in Fig. 1-13 and Fig. 1-14.

1.4.2 Dual plasma treatment

There have been many studies using fluorine plasma treatment or nitrogen plasma treatment to improve the performance of the device. In this thesis, we proposed to combine two kinds of plasma treatment (CF_4 pre-treatment and nitrogen post-treatment) in order to further improve the electrical characteristics and strength the reliability characteristics of Hf-based MIS capacitor and Low-Temperature Polycrystalline-Silicon (LTPS) Thin-Film Transistor (TFT).

This method that combined CF_4 pre-treatment and nitrogen post-treatment is called dual plasma treatment. The purpose of dual plasma treatment is to combine the advantages of two kinds of plasma treatment. We intended to employ CF_4 plasma pre-treatment in order to eliminate the low dielectric constant interfacial layer and improved the quality of silicon substrate surface. Moreover, we used the NH_3 and N_2 plasma post-treatment to reduce oxygen vacancies, increase the permittivity, and increase the crystallization temperature of Hf-based device.

1.5 Organization of the dissertation

In this dissertation, we concentrate our effort to examine the effect of dual plasma treatment (CF_4 pre-treatment and nitrogen post-treatment) on the electrical characteristics and the reliability of the Hf-based device. There are five chapters in this dissertation, and the content of each chapter are described as following.

In chapter 1, we introduce the general background of the high-κ materials,

including the principle of choosing high-κ materials, and the most candidate high-κ material. Then, we describe the current conduction mechanisms in high-κ dielectric, such as Schottky emission (SE), Frenkel-Poole (F-P) emission, and Fowler-Nordheim (F-N) tunneling. The motivation that new method called dual plasma treatment is launched to combine the advantages of two kinds of plasma treatment (CF_4 pre-treatment and nitrogen post-treatment).

In chapter 2, we propose to combine two kinds of plasma treatment (denoted as dual plasma treatment), CF_4 pre-treatment and nitrogen post-treatment, in order to achieve further improvement. We have examined the reliability properties and the current conduction mechanism of HfO_2 MIS capacitor structure. First of all, the capacitance-voltage (C-V) characteristics and current-voltage (J-V) characteristics will be briefly described. Second, the frequency dispersion and constant voltage stress (CVS) characteristics of the samples will be analyzed to estimate the improvement. Finally, current conduction mechanisms, such as Schottky emission, Frenkel-Poole (F-P) emission, and Fowler-Nordheim (F-N) tunneling will be discussed. Schottky barrier height, F-P barrier height, and F-N barrier height will be extracted.

In chapter 3, Al/Ti/ $HfAlO_x$/Si MIS capacitor structure would be fabricated. We propose to combine CF_4 pre-treatment and N_2 post-treatment (denoted as dual plasma treatment) to examine interface quality and reliability properties of $HfAlO_x$ MIS capacitor.

In chapter 4, according to chapter 2 and chapter 3, we have demonstrated the dual plasma treatment on MIS capacitor with high-κ gate dielectric. In this chapter, dual plasma treatment (CF_4 pre-treatment and N_2 post-treatment) will be utilized on LTPS TFTs to reduce defects in poly-Si channel and HfO_2 gate dielectric. The

electrical improvement would be studied, including the hysteresis and the I-V characteristics. The device parameters, such as Vth, S.S., G_m, μ_{eff}, D_{it}, and N_{trap} are extracted to study the improvement effect. Furthermore, the reliability properties and mechanisms of high performance HfO_2 gate dielectric LTPS-TFT with dual plasma treatment are investigated, including PBS, NBS, HCS.

Finally, in chapter 5, the summarizations of experimental results in this dissertation and future recommendations are described.

Table 1-1 Main high-κ gate dielectric materials with their parameters: ε is the permittivity, Eg is the band gap, CBO is the conduction band offset, and VBO is the valence band offset [23].

Material	ϵ	E_g (eV)	CBO (eV)	VBO (eV)
SiO_2	3.9	9.0	3.2	4.7
Si_3N_4	7	5.3	2.4	1.8
Al_2O_3	9	8.8	2.8	4.9
La_2O_3	30	6.0	2.3	2.6
Y_2O_3	15	6.0	2.3	2.6
ZrO_2	25	5.8	1.5	3.2
Ta_2O_5	22	4.4	0.35	2.95
HfO_2	25	5.8	1.4	3.3
$HfSiO_4$	11	6.5	1.8	3.6
TiO_2	80	3.5	0	2.4
a-$LaAlO_3$	30	5.6	1.8	2.7
$SrTiO_3$	2000	3.2	0	2.1

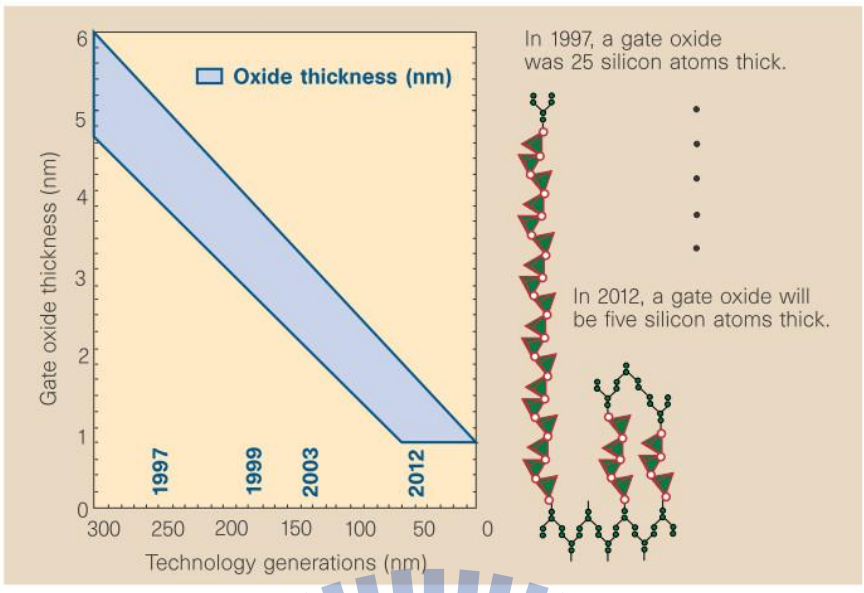

Fig. 1-1 International Technology Roadmap for Semiconductors (ITRS). Predictions of the gate oxide (SiO2) thickness for future technology generations, which were defined by the critical device size [10].

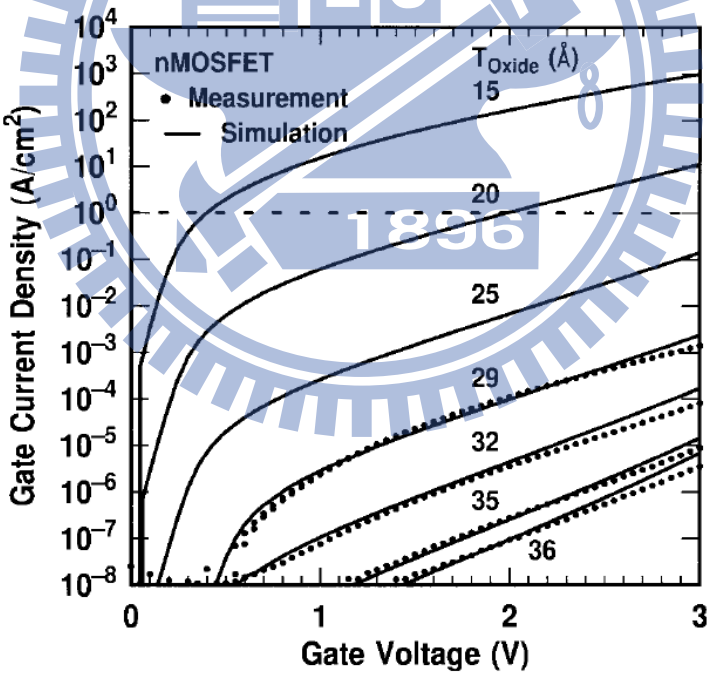

Fig. 1-2 The direct tunneling gate current vs. gate voltage with different gate oxide thickness [11].

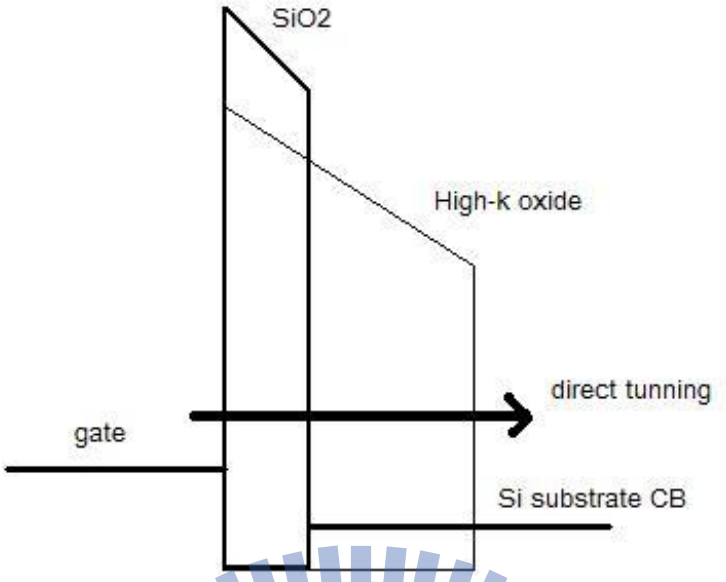

Fig. 1-3 Schematic of direct tunneling through a SiO_2 and the thicker high-k gate dielectric layer.

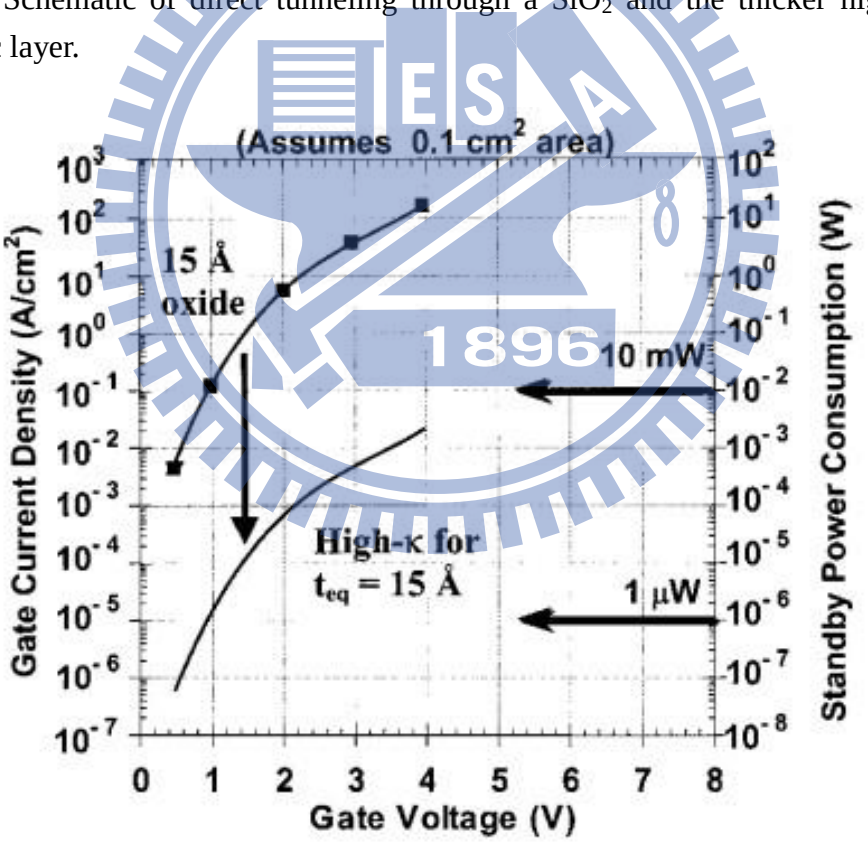

Fig. 1-4 Power consumption and gate leakage current density for a chip which has a 15 Å thick SiO_2 gate dielectric compared to the potential reduction in leakage current by an alternate gate dielectric exhibiting the same EOT. Total gate area of 0.1 cm^2 [3].

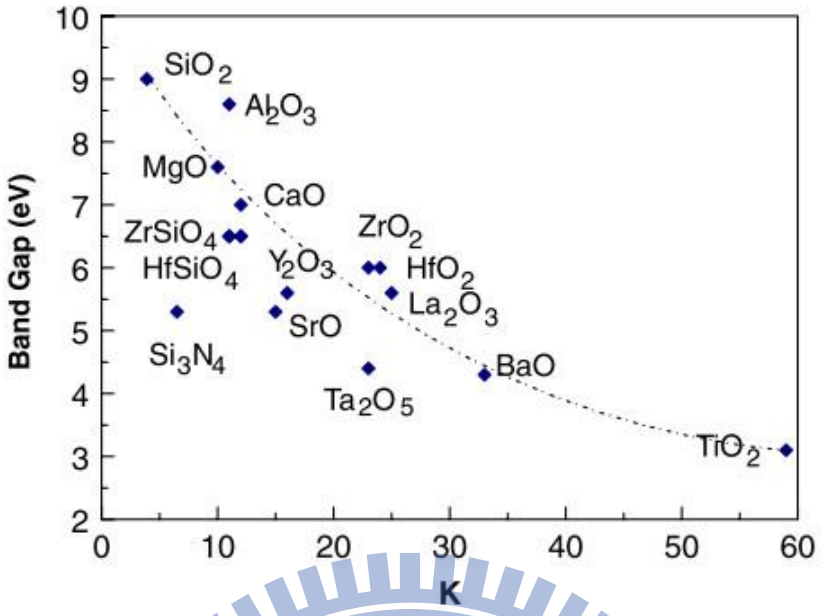

Fig. 1-5 Dielectric constant versus band gap for candidate high-κ materials [24].

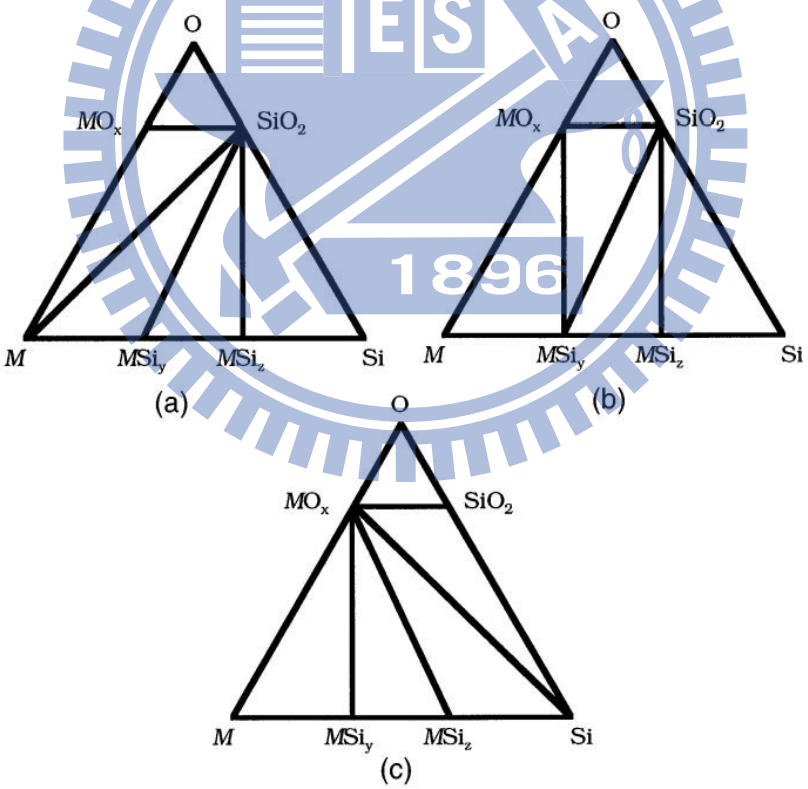

Fig. 1-6 Three types of M (metal)-Si-O phase diagrams at fixed temperature and pressure: (a) SiO_2 dominant, (b) No phase dominant, and (c) Metal oxide dominant [26].

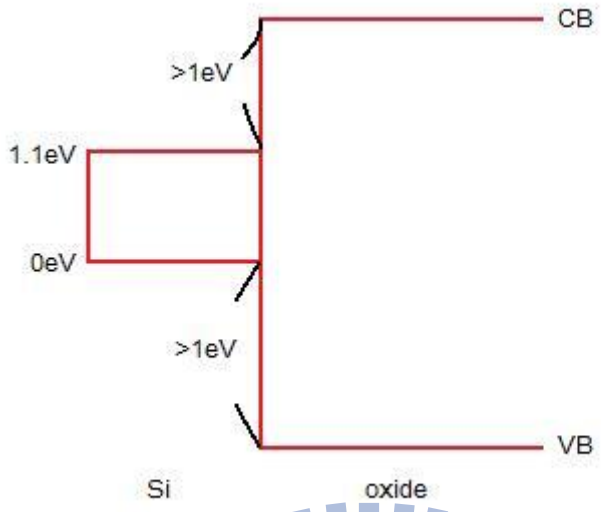

Fig. 1-7 The relation of band offsets with carrier injection of electrons and holes in gate oxide band states.

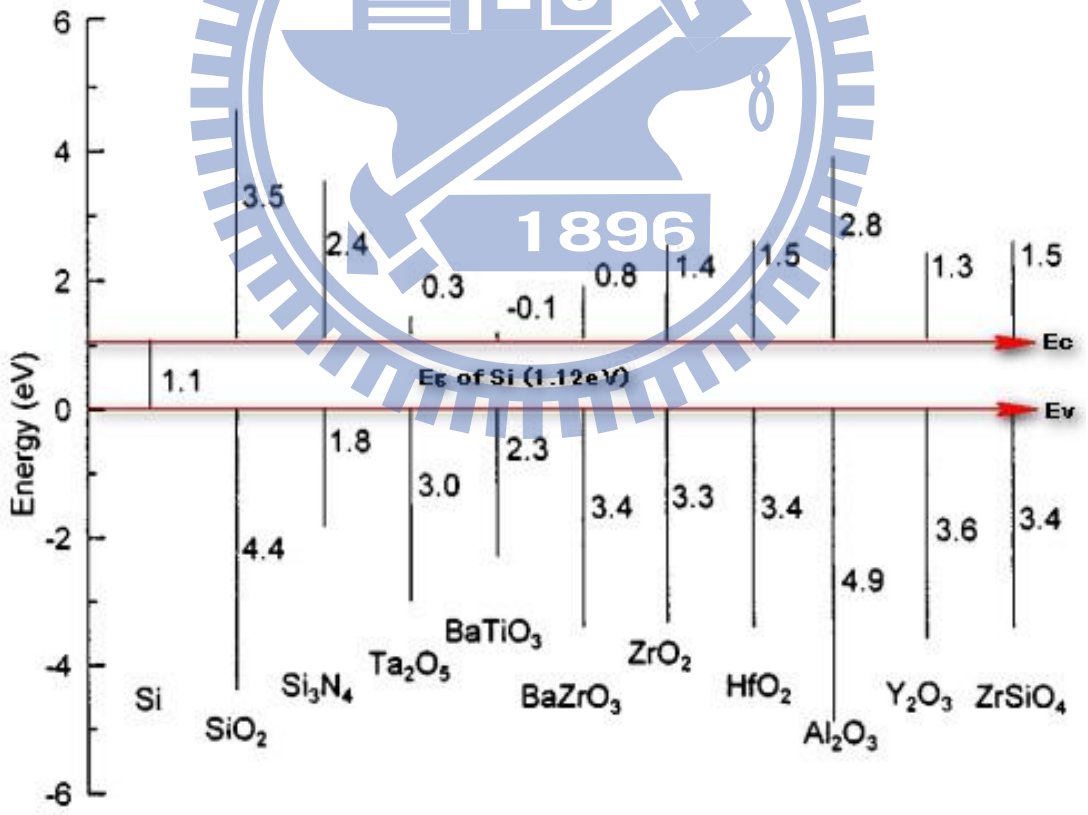

Fig. 1-8 The band alignments of typical high-k gate dielectrics [24].

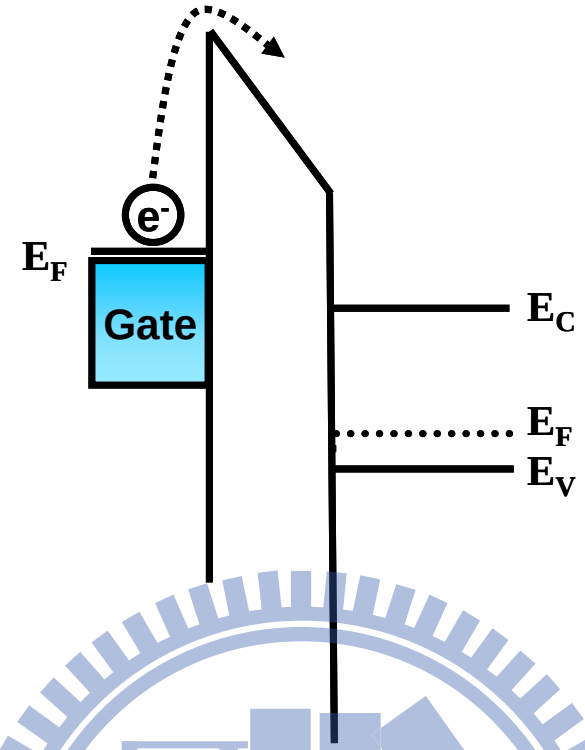

Fig. 1-9 Energy band diagram of Schottky emission current conduction mechanism.

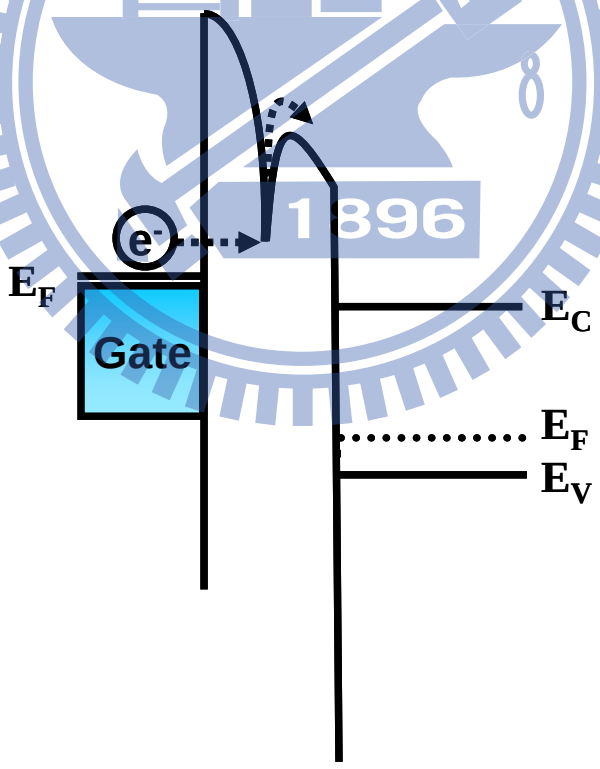

Fig. 1-10 Energy band diagram of Frenkel-Poole emission current conduction mechanism.

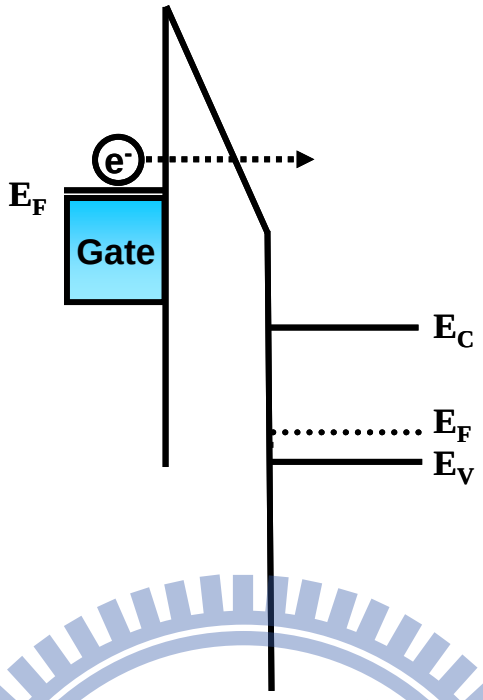

Fig. 1-11 Energy band diagram of Fowler-Nordheim tunneling current conduction mechanism.

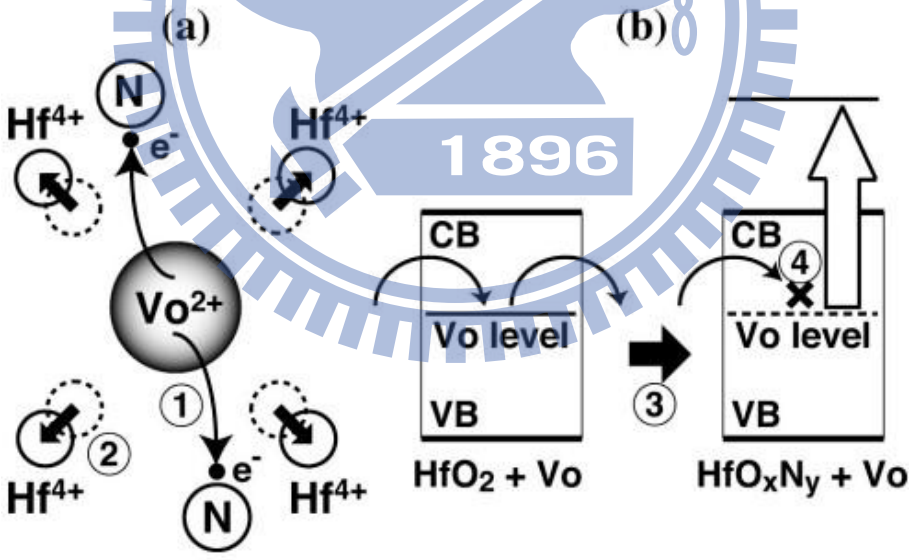

Fig. 1-12 Schematic illustration of N incorporation effects :

(a) N-induced atomistic relaxation around Vo: ① Electron transfer from Vo to N atoms,② Outward movement of Hf4+ ions due to the increase in Hf4+- Hf4+ Coulomb repulsion, (b) N-induced elimination of leakage paths: ③ Vo level elevation due to the decrease in attractive Coulomb interaction fromHf4+ ions around Vo,④ removal of leakage paths due to the elimination of a Vo level [45]

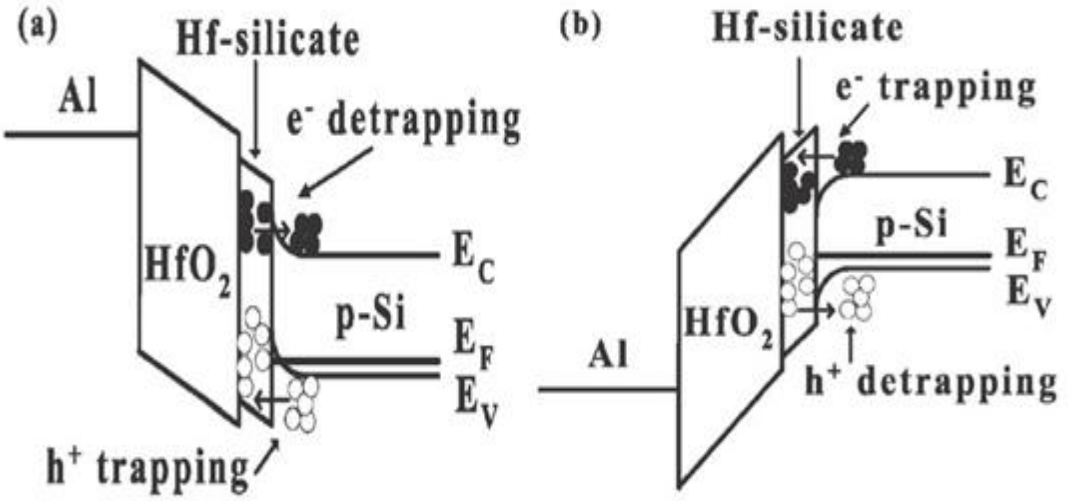

Fig. 1-13 Inner-interface trapping model of HfO_2 for sweeping voltage from (a) accumulation to (b) inversion [48].

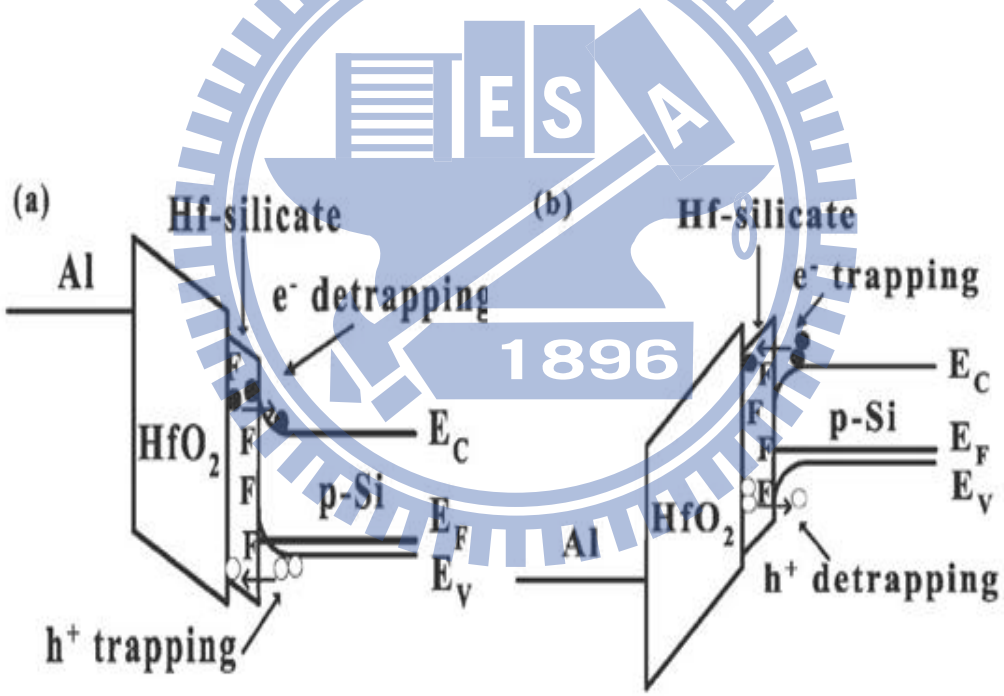

Fig. 1-14 Inner-interface trapping model of HfO_2 after CF_4 plasma treatment for sweeping voltage from (a) accumulation to (b) inversion [48].

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Chapter 2

Electrical Characteristics, Reliability Properties and Current Conduction Mechanisms of HfO_2 MIS Capacitor with Dual Plasma Treatment

2.1 Introduction

The rapid progress of complementary metal oxide semiconductor (CMOS) integrated circuit technology has met several serious technological challenges over the past few years. According to the prediction of the International Technology Roadmap for Semiconductor (ITRS), the conventional gate dielectric layer will reach its physical limits [1]. Gate dielectric scaling of CMOS will increase the speed and the packing density of modern circuits. However, the aggressive shrinking of the gate length and gate dielectric thickness accompanies excessive leakage current and reliability problems. To solve these problems, a major solution is to replace the traditional SiO_2 or SiON by other higher dielectric constant material. Using high dielectric constant material for gate dielectric could have larger physical thickness and maintain smaller equivalent oxide thickness (EOT). As a result, high-dielectric-constant (high-κ) thin films have been considered as suitable gate dielectric for modern CMOS technology. There are various high-κ thin film has been investigated [2-4]. Among these high-κ materials, HfO_2 is considered as the most

promising candidate because of high dielectric constant (~25), wide band gap (~5.7 eV), and large band offset with Si conduction band (~1.5 eV) [2, 5]. Nevertheless, there are still some issues which need to be considered, such as the reliability and thermal stability of the dielectrics [6, 7].

It has been reported that nitrogen incorporated into HfO_2 gate dielectrics has beneficial effect on performance [8]. Nitrogen could be incorporated into dielectric layer by ICP plasma nitridation process at lower temperature [9, 10]. As reported in previous study: nitrogen incorporation can suppress crystallization during high temperature treatment, reduce dopant penetration, increase dielectric constant, and reduce leakage current by about 3-4 orders of magnitude [11, 12]. Umezawa et al [13] noted that nitrogen could deactivate the oxygen vacancy related states within HfO_2 band gap. The absence of gap states leads to the removal of electron leakage path.

In addition, the incorporation of fluorine in HfO_2 gate dielectrics also has been reported to be beneficial for electrical and reliability performance [14-16]. The quality of interfacial layer (IL) becomes more and more important due to gate dielectric scaling. Wong et al [17] noted that the applied electric field would be largely distributed in the low-κ region for high-κ/low-κ stack layer because of Gauss's law. The first breakdown happened in the low-κ layer [17]. Recently, several studies have used fluorine incorporation to improve IL quality at HfO_2/Si interface because Si-F bond (5.73 eV) is stronger than Si-H bond (3.18eV) [18, 19]. Moreover, pre-CF_4 plasma treatment has been shown to effectively suppress the IL formation [20].

In this study, we propose to combine two kinds of plasma treatment (denoted as dual plasma treatment), CF_4 pre-treatment and nitrogen post-treatment, in order to achieve further improvement. We have examined the reliability properties and the

current conduction mechanism of HfO_2 MIS capacitor structure. First of all, the capacitance-voltage (C-V) characteristics and current-voltage (J-V) characteristics will be briefly described. Second, the frequency dispersion and constant voltage stress (CVS) characteristics of the samples will be analyzed to estimate the improvement. Finally, current conduction mechanisms, such as Schottky emission, Frenkel-Poole (F-P) emission, and Fowler-Nordheim (F-N) tunneling will be discussed. Schottky barrier height, F-P barrier height, and F-N barrier height will be extracted.

2.2 Experimental

2.2.1 MIS capacitor fabrication

After standard RCA cleaning, the samples were treated in CF_4 plasma (denoted as CF_4 pre-treatment) for various times. The substrate temperature in a plasma enhanced chemical vapor deposition (PECVD) system was set at 300 ^oC. The process pressure and the CF_4 flow rate were 500 mTorr and 100 sccm, respectively. The RF power was set at 20 W and the exposure times were varied in the range of 10-40 sec. After CF_4 pre-treatment, HfO_2 thin film was deposited on the samples by the metal organic chemical vapor deposition (MOCVD) system. Then post deposition annealing (PDA) was performed at 600 ^oC for 30 sec in a rapid temperature annealing (RTA) system. After PDA, samples were nitrided in nitrogen plasma (denoted as nitrogen post-treatment) by PECVD. The flow rate of nitrogen gas, which is N_2 or NH_3, was set at 100 sccm. Post nitridation annealing (PNA) was performed with RTA equipment at 600 ^oC for 30 sec in order to reduce plasma damage. Thereafter, 40 nm-Ti films and 400 nm Al films were deposited by e-beam evaporation system. The top electrodes

were defined lithographically and etched to define a gate area of 5000 μm^2. Finally, backside Al electrodes were deposited by the thermal evaporation to form the Ohmic contact.

2.2.2 Single plasma treatment and dual plasma treatment

In this study, there are two different kinds of experiment of plasma treatment. First, for single nitrogen post-treatment, samples were nitrided in nitrogen plasma (N_2 or NH_3) by PECVD system after HfO_2 deposition and PDA. The purpose of the first experiment is that the best condition of nitrogen post-treatment will be used in dual plasma treatment experiment. Second, for dual plasma treatment, CF_4 pre-treatment with different durations and nitrogen post-treatment were combined in Al/Ti/HfO_2/Si capacitors. The key process flow of two experiments in this work is schematically shown in Fig. 2-1(a) single nitrogen post-treatment and Fig. 2-1(b) dual plasma treatment (CF4 pre-treatment and nitrogen post-treatment).

2.2.3 The MIS capacitor measurement

The capacitance-voltage (C-V) and current-voltage (I-V) characteristics of MIS structure were measured by using a C-V measurement (Hewlett-Packard 4284) and Hewlett-Packard 4156C semiconductor parameter analyzer, respectively. The condition of frequency dispersion measurement was set as from 1 kHz to 100 kHz. The stress condition of CVS measurement was set as a constant voltage -3V for 0 to 500 sec. Furthermore, the I-V characteristics were measured at elevated temperatures from 25 to 125 ^oC, 25 ^oC per step, in order to analyze current conduction mechanisms.

2.3 Electrical characteristics of single plasma treatment

2.3.1 C-V and J-V Characteristics

Fig. 2-2 shows the C-V and I-V characteristics of the HfO_2 thin films with N_2 post-treatment for different process durations. The sample treated in N_2 plasma for 120 sec perform the maximum capacitance density among these samples. The leakage current density is suppressed for the sample treated in N_2 plasma for 120 sec. The capacitance is degraded and the leakage current is increased while the samples treated longer than 120 sec, owing to plasma damage. It can be observed that the sample treated in N_2 plasma for 120 sec with RF power 50W performs the best performance. Similarly, the sample treated in NH_3 plasma with RF power 40W for 120 sec displays the best C-V and I-V characteristics than other samples, as shown in Fig. 2-3. These two conditions will be chosen for dual plasma treatment.

In order to combine two kinds of plasma, the samples treated in CF_4 plasma (denoted as CF_4 pre-treatment) for different durations and N_2 or NH_3 plasma (denoted as nitrogen post-treatment) for 120 sec is examined.

2.4 Electrical characteristics of dual plasma treatment

2.4.1 C-V and J-V characteristics

Fig. 2-4 shows the C-V characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and N_2 plasma for 120 sec. The frequency used in the high frequency C-V measurement was set at 50 kHz. The sample was treated only in N_2 plasma for 120 sec (RF power = 50 W) shows much higher capacitance

density than the sample with no treatment. The higher capacitance could be attributed to the PDA process [21-23] and the nitrogen incorporation in the HfO_2 thin film. The nitrogen incorporation could enhance the electronic polarization as well as the ionic polarization, which result in the increase of dielectric constant [12, 24]. On the other hand, the capacitance density and interface characteristics show further improvement with the combination of CF_4 pre-treatment for 10 sec and N_2 post-treatment for 120 sec. With CF_4 pre-treatment, fluorine atoms would pile up at the HfO_2/Si interface, improve the quality of interface [19], and suppress the IL formation [20]. Besides, for CF_4 pre-treatment times longer than 10 sec, the plasma damage caused the degradation of HfO_2/Si interface and the degradation of capacitance density.

Fig. 2-5 shows the J-V characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and N_2 plasma for 120 sec. Compared with the sample with no treatment, the gate leakage current decreased by about 4 orders of magnitude for the sample with CF_4 pre-treatment for 10 sec and N_2 post-treatment for 120 sec. The reduction of the gate leakage could be attributed to defect passivation. Oxygen vacancy related states and interface states could be passivated by nitrogen and fluorine atoms [13, 16]. On the other hand, for CF_4 pre-treatment times longer than 10 sec, the plasma damage caused the degradation of interface and the increase of gate leakage current. The best condition of dual plasma treatment is as follows: CF_4 pre-treatment (time=10s, RF Power=20W) and N_2 post-treatment (time=120s, RF Power=50W). The gate leakage of the sample with best condition is 1.05×10^{-5} A/cm^2 at V_g = -1.5 V. Table 2-1 illustrates the basic electrical characteristics.

In Fig. 2-6 and Fig. 2-7, the C-V and the J-V characteristics of the HfO_2 gate dielectrics, treated in CF_4 plasma for different process durations and NH_3 plasma for 120 sec, are presented. The RF power of NH_3 post-treatment was set at 40 W. As

mentioned before, the reason of the improvement in the NH_3 plasma nitridation process could be the same as the one in the N_2 plasma nitridation process. From the similar analysis, the best condition of dual plasma treatment is as follows: CF_4 pre-treatment (time=10s, RF Power=20W) and NH_3 post-treatment (time=120s, RF Power=40W). The gate leakage of the sample with best condition is 1.62×10^{-5} A/cm^2 at V_g = -1.5 V. In summary, C-V and I-V Characteristics could be further improved by dual plasma treatment. Table 2-2 illustrates the basic electrical characteristics.

2.4.2 Hysteresis

Fig. 2-8 demonstrates the hysteresis characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and N_2 plasma for 120 sec. Hysteresis measurement was measured from accumulation to inversion (-2 V to 1 V) and backward form inversion to accumulation (1V to -2 V) by sweeping the voltage. Because positive and negative carrier might be trapped at the inner interface during voltage sweeping [19], the hysteresis phenomenon could be observed for all the samples. Although single N_2 plasma treatment could improve the hysteresis characteristic, the hysteresis characteristic could be further improved by dual plasma treatment (CF_4 pre-treatment for 10 sec and N_2 post-treatment for 120 sec). The C-V curve shift of the sample treated by the combination of CF_4 pre-treatment for 10 sec and N_2 post-treatment for 120 sec is about 14 mV, which is smaller than the fresh sample (27 mV) and the sample with N_2 plasma treatment (17 mV). Moreover, the fresh sample shows a hump in the depletion region of the C-V characteristics, due to higher D_{it} at the interface [38]. After dual plasma treatment (CF_4 pre-treatment for 10 sec and N_2 post-treatment for 120 sec), the hump could be effectively eliminated. It can be speculated that interface quality could be enhanced by dual plasma treatment. On the other hand, the hump and hysteresis became worst while CF_4 pre-treatment

time is longer than 10 sec due to plasma damage at the HfO_2/Si interface. Similarly, the sample treated by the combination of CF_4 pre-treatment for 10 sec and NH_3 post-treatment for 120 sec shows the best hysteresis and interface characteristics than other samples, as shown in Fig. 2-9.

2.4.3 Frequency dispersion characteristics

The C-V characteristics of the HfO_2 thin films, treated with CF_4 plasma for different process durations and N_2 plasma for 120 sec, have been measured as a function of frequency as shown in Fig. 2-10 to Fig. 2-15. The measurements were made in the frequency range of 1-100 kHz (1, 10, and 100 kHz). Frequency dispersion could be observed because of the response of trap charges to signal frequency. At low frequencies, interface traps generated the additional capacitance because some of traps could follow the change of gate voltage [25]. The frequency dispersion in the accumulation region and the hump in the depletion region are significant for the sample with no treatment. The sample treated by N_2 plasma showed relatively smaller frequency dispersion and smaller hump than the sample with no treatment. On the other hand, it was obvious that the sample treated by CF_4 pre-treatment for 10 sec and N_2 post-treatment for 120 sec exhibited nearly no dispersion in the accumulation region and nearly no hump in the depletion because interface states could be improved effectively [25-28] by dual plasma treatment. However, the frequency dispersion and the hump became severe again when the CF_4 pre-treatment time is longer than 10 sec owing to plasma damage at interface.

Fig. 2-16 to Fig. 2-20 display the C-V frequency dependence of the HfO_2 thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 120 sec. The sample treated by CF_4 pre-treatment for 10 sec and NH_3 post-treatment for

120 sec exhibited nearly no dispersion and nearly no hump during C-V measurement. This indicated that dual plasma treatment could effectively eliminate interface states and greatly enhance IL quality than single plasma treatment.

2.4.4 Constant voltage stress characteristics

In order to study the trapping properties of the Al/Ti/HfO_2/Si MIS capacitors, the constant voltage stress (CVS) was applied on the gate electrode, leading to the stress induced flat-band voltage shift. The stress voltage was set at -3 V. The stress times were made in a range from 0 to 500 sec. As shown in Fig. 2-21 to Fig. 2-27, all the C-V curves shift to left as stress time increase indicated that there were positive charges trapped in the high-κ dielectric layer. Trapping of positive charges could be explained by Anode hole injection model [29]. At higher electrical field, electrons might tunnel through a triangular potential barrier of the gate dielectric film by the mechanism of Fowler-Nordheim (F-N) tunneling and arrive at the anode terminal, resulting in the generation of electron-hole pairs, as shown in Fig. 2-28 [18].

During constant negative bias stress at a fixed gate voltage, the injected electrons traveled through dielectric and arrived at the interface. These electrons gained energy to liberate the hydrogen at the interface, leading to the generation of Si dangling bond and released hydrogen atom. These dangling bonds were interface defects, which usually called the p_b centers. The liberated hydrogen diffused into the dielectric through the oxide field, trapped in the dielectric, leading to the creation of positively charged centers [30, 31].

$$Si_3 \equiv SiH + e^- \rightarrow Si_3 \equiv Si\cdot + H + e^- . \quad (1)$$

Compared to Fig. 2-22 and Fig. 2-23, the C-V curves had smaller V_{fb} shift and less distortion for samples with dual plasma treatment, indicating that samples with

dual plasma treatment had less interface trap charges generated at the dielectric/Si interface and had better reliability properties than samples with single plasma treatment.

2.5 Current conduction of Al/Ti/HfO_2/Si MIS capacitors

In order to understand the current conduction mechanism, three kinds of conduction mechanisms were be analyzed, including Schottky emission (SE), Frenkel-Poole (F-P) emission, and Fowler-Nordheim (F-N) tunneling. The leakage current was measured from 298 K to 398 K (25 K per step) because to analyze S.E. and F-P emission needs the time dependence of the leakage current.

2.5.1 Schottky emission (S.E.)

Fig. 2-29 to Fig. 2-39 depicts the J-E plots for all the samples from 298 K to 398 K (25 K per step). The electric field E is an "effective" electric field (E = V/CET), while capacitance effective thickness (CET) is extracted from the capacitance density in the accumulation region [32]. The standard Schottky emission could be expressed as

$$J_{SE} = A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right], \qquad A^* = 120\frac{m^*}{m_0}\ \left(\frac{A}{cm^2K^2}\right), \qquad (2)$$

where J_{SE} is the current density, A^* is the effective Richardson constant, E is the effective electric field, T is the absolute temperature, q is the electron charge, $q\phi_B$ is the Schottky barrier height, k is Boltzmann's constant, ε_0 is the permittivity of free space, ε_r is the dynamic dielectric constant, m^* is the electron effective mass in HfO_2,

m_0 is the free electron mass. The electron effective mass is 0.1 m_0 [33, 34].

For the standard Schottky emission, a plot of $\ln(J/T^2)$ versus $E^{1/2}$ should be a straight line, as shown in Fig. 2-40 to Fig. 2-50. The slope of standard plot could obtain dynamic dielectric constant (ε_r), which is agreed with previous study [35] pretty well. It was found that Schottky emission is the dominate conduction mechanism in the region of low to medium electric fields (1.7 - 3.0 MV/cm) [36]. Eq. (3) expressed the intercept of the Schottky emission plot with the vertical axis. The barrier height could be extracted from Eq. (3).

$$Intercept = \ln(A^*) - \frac{q\phi_B}{kT}, \qquad A^* = 120\frac{m^*}{m_0}\left(\frac{A}{cm^2K^2}\right). \tag{3}$$

Because of effective electric field (E = V/CET), the extracted barrier heights in this study are effective barrier heights. The band diagram of Al/Ti/HfO2/Si MIS capacitor for S.E. is shown in Fig. 2-51. The extracted Schottky barrier heights ($q\phi_B$) for the samples with no treatment, single plasma treatment, and dual plasma treatment are listed in Table 2-3. The barrier heights for the sample without treatment is 1.01±0.04 eV. It is clear that the samples had larger barrier height than other samples after CF_4 pre-treatment for 10 sec and nitrogen post-treatment for 120 sec.

In short, dual plasma treatment could effectively increase the Schottky barrier height, which could effectively decrease the gate leakage current in the region of low to medium electric fields (1.7 - 3.0 MV/cm) at higher temperature.

2.5.2 Frenkel-Poole (F-P) emission

When gate under negative bias, electrons will inject from gate into HfO_2 dielectric layer and will be trapped into shallow trap levels. Thereafter, the electrons

transported through the dielectric layer by hopping between these trap levels, leading to leakage current, called Frenkel-Poole (F-P) emission. The standard F-P emission could be expressed as [35]

$$J_{FP} = C_t E \exp\left[\frac{-q\left(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right], \quad (4)$$

where J_{FP} is the current density, E is effective electric field, C_t is a constant proportional to the density of bulk oxide traps, $q\phi_t$ is the trap energy in HfO_2, and other parameters are as defined earlier.

For the standard Frenkel-Poole emission, a plot of $\ln(J_{FP}/E)$ versus $E^{1/2}$ should be linear, as shown in Fig. 2-52 to Fig. 2-62. It was found that F-P emission is the dominate conduction mechanism in the region of medium to high electric fields (4.0 - 6.0 MV/cm). Then, a plot of $\ln(J_{FP}/E)$ versus 1/T at various electric fields were illustrated in order to extract $q\phi_t$, as shown in Fig. 2-63 to Fig. 2-73. These trap levels ($q\phi_t$) are a function of the square root of the electric field. The intercepts with vertical axis shows the trap levels without barrier lowing induced by image force. The trap energy in dielectric layer could be extracted form good F-P fitting, as shown in Fig. 2-74.

Table 2-4 lists the trap energy levels of the samples with no treatment, single plasma treatment, and dual plasma treatment. The extracted trap levels for the sample with and without N_2 post-treatment were 1.12 eV and 0.72 eV, respectively. In contrast, the trap level for the sample treated by CF_4 pre-treatment for 10 sec and N_2 post-treatment for 120 sec was 1.14 eV. The deeper trap level means that most of shallow trap levels in HfO_2 thin film can be eliminated [32] by using dual plasma

treatment. The elimination of shallow trap levels resulted in the reduction of F-P conduction current. Similarly, the sample treated in CF_4 pre-treatment for 10 sec and NH_3 post-treatment for 120 sec also exhibited larger trap levels than other samples. In short, dual plasma treatment could eliminate the shallow trap levels and greatly reduce the gate leakage current. The band diagram is depicted in Fig. 2-75.

2.5.2 Fowler-Nordheim (F-N) Tunneling

In higher electric field, the Fowler-Nordheim (F-N) tunneling dominated the conduction mechanism [36]. The standard F-P emission could be expressed as

$$J_{FN} = AE^2 \exp\left[\frac{-8\pi\sqrt{2m^*}(q\phi_f)^{3/2}}{3qhE}\right], \quad (5)$$

where J_{FN} is the current density, h is the Plunk's constant, $q\phi_f$ is the potential barrier height, m^* is the electron effective mass in HfO_2, and the other notations were as same as mentioned before. The electron effective mass here is 0.1 m_0 [33, 34]. If the leakage current is dominated by the F-N mechanism, a plot of $\ln(J/E^2)$ versus 1/E should be linear. Linear characteristic could be observed at high electric field (> 7 MV/cm), as shown in Fig. 2-76. The slope of each curve in Fig. 2-76 and Eq. (6) could obtain the F-N barrier height, which were listed in Table 2-5

$$\phi_f = \left(\frac{9h^2}{128\pi^2 m^* q}\right) * (slope)^{2/3}. \quad (6)$$

Table 2-5 listed the F-N barrier height of the samples with no treatment, single plasma treatment, and dual plasma treatment. It could be observed that samples treated in CF_4 pre-treatment for 10 sec and nitrogen post-treatment for 120sec had larger value than other samples. The injection of electrons from the gate entered the

conduction band of HfO_2 by tunneling through a triangular potential barrier, as shown in Fig. 2-77. The injected electrons interacted with lattice or transferred its energy at anode [37], which resulted in the degradation of the dielectric layer. As a result, the sample with proper dual plasma treatment had bigger F-N barrier height and better reliability properties.

2.6 Conclusion

In conclusion, the reliability properties and current conduction mechanisms of HfO_2 gate dielectric films as a function of dual plasma treatment (the combination of CF_4 pre-treatment and nitrogen post-treatment) have been investigated. First, the best conditions which decided form C-V and J-V characteristics were the samples treated by CF_4 plasma for 10 sec and N_2 (NH_3) plasma for 120 sec. According to the current conduction analysis, the dominant current conduction mechanism was Schottky emission type in the region of low to medium electric fields (1.7 – 3.0 MV/cm); Frenkel-Poole (F-P) emission operated in the region of medium to high fields (4.0 – 6.0 MV/cm); Fowler-Nordheim (F-N) tunneling was dominant at high fields (> 7 MV/cm). Fig. 2-78 shows the summary of the three current conduction mechanisms in different ranges of applied gate voltage. Dual plasma treatment was effective in improving interface quality, eliminating shallow trap levels, and enhancing reliability properties. In summary, the effect of dual plasma treatment could be better than single plasma treatment and dual plasma treatment would be an effective technology to improve the reliability of HfO_2 thin films.

Table 2-1 illustrates the basic electrical characteristics of the sample for dual plasma treatment (CF_4 pre-treatment and N_2 post-treatment).

Samples	**Fresh**	**N_2(120s)**	**CF_4(10s)+ N_2(120s)**	**CF_4(20s)+ N_2(120s)**	**CF_4(30s)+ N_2(120s)**	**CF_4(40s)+ N_2(120s)**
C(μF/cm^2)	0.78	1.12	1.21	1.11	0.98	0.95
Improve percentage (%)		44	55.71	42.53	26.15	23.07
CET (nm)	4.44	3.08	2.85	3.11	3.51	3.61
J(A/cm^2)	4.72E-01	9.10E-06	1.05E-05	5.61E-05	9.84E-05	3.24E-04
Hysteresis (mV)	26.90	17.00	14.41	20.44	23.64	25.99

Table 2-2 illustrates the basic electrical characteristics of the sample for dual plasma treatment (CF_4 pre-treatment and NH_3 post-treatment).

Samples	**Fresh**	**NH_3(120s)**	**CF_4(10s)+ NH_3 (120s)**	**CF_4(20s)+ NH_3 (120s)**	**CF_4(30s)+ NH_3 (120s)**	**CF_4(40s)+ NH_3 (120s)**
C(μF/cm^2)	0.78	1.12	1.26	1.16	1.08	1.05
Improve percentage (%)		44.12	61.60	49.30	38.88	34.33
CET (nm)	4.44	3.08	2.75	2.97	3.20	3.30
J(A/cm^2)	4.72E-01	1.03E-4	1.62E-05	1.08E-04	2.05E-03	2.84E-03
Hysteresis (mV)	26.90	15.53	14.41	21.23	27.60	23.11

Table 2-3 Schottky Barrier Height Extracted for The Samples with No Treatment, Single Plasma Treatment, and Dual Plasma Treatment.

Barrier height	**Fresh**	**N_2(120s)**	**CF_4(10s)+ N_2(120s)**	**CF_4(20s)+ N_2(120s)**	**CF_4(30s)+ N_2(120s)**	**CF_4(40s)+ N_2(120s)**
$q\phi_B(eV)$	1.01±0.04	1.23±0.09	1.32±0.1	1.19±0.09	1.14±0.08	1.13±0.08
Barrier height	**Fresh**	**NH_3(120s)**	**CF_4(10s)+ NH_3 (120s)**	**CF_4(20s)+ NH_3 (120s)**	**CF_4(30s)+ NH_3 (120s)**	**CF_4(40s)+ NH_3 (120s)**
$q\phi_B(eV)$	1.01±0.04	1.21±0.04	1.32±0.07	1.21±0.07	1.13±0.05	1.15±0.04

Table 2-4 F-P Trapping Level Extracted for The Samples with No Treatment, Single Plasma Treatment, and Dual Plasma Treatment.

Barrier height	**Fresh**	**N_2(120s)**	**CF_4(10s)+ N_2(120s)**	**CF_4(20s)+ N_2(120s)**	**CF_4(30s)+ N_2(120s)**	**CF_4(40s)+ N_2(120s)**
$q\phi_t(eV)$	0.72	1.12	1.14	0.91	0.80	0.83
Barrier height	**Fresh**	**NH_3(120s)**	**CF_4(10s)+ NH_3 (120s)**	**CF_4(20s)+ NH_3 (120s)**	**CF_4(30s)+ NH_3 (120s)**	**CF_4(40s)+ NH_3 (120s)**
$q\phi_t(eV)$	0.72	0.82	1.10	0.80	0.72	0.74

Table 2-5 F-N Barrier Height Extracted for The Samples with No Treatment, Single Plasma Treatment, and Dual Plasma Treatment

Barrier height	**Fresh**	**N_2(120s)**	**CF_4(10s)+ N_2(120s)**	**CF_4(20s)+ N_2(120s)**	**CF_4(30s)+ N_2(120s)**	**CF_4(40s)+ N_2(120s)**
$q\phi_f(eV)$	1.78	1.86	2.01	1.85	1.71	1.66
Barrier height	**Fresh**	**NH_3(120s)**	**CF_4(10s)+ NH_3 (120s)**	**CF_4(20s)+ NH_3 (120s)**	**CF_4(30s)+ NH_3 (120s)**	**CF_4(40s)+ NH_3 (120s)**
$q\phi_f(eV)$	1.78	1.86	1.92	1.83	1.80	1.76

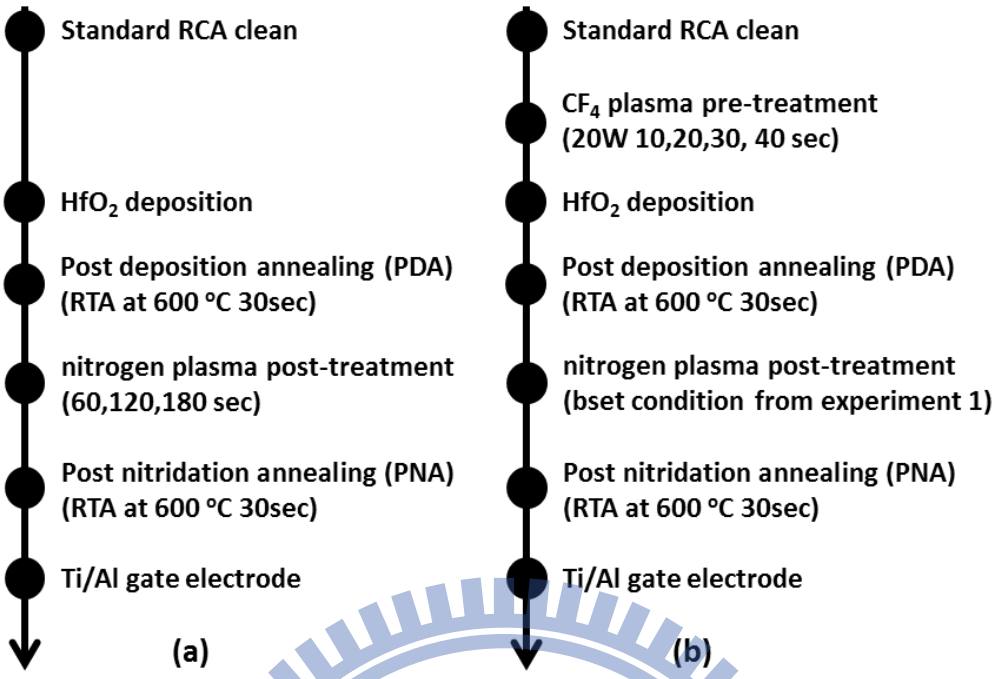

Fig. 2-1 Schematic of key process flow of two experiments in this study (a) single nitrogen post-treatment and (b) dual plasma treatment (CF4 pre-treatment and nitrogen post-treatment).

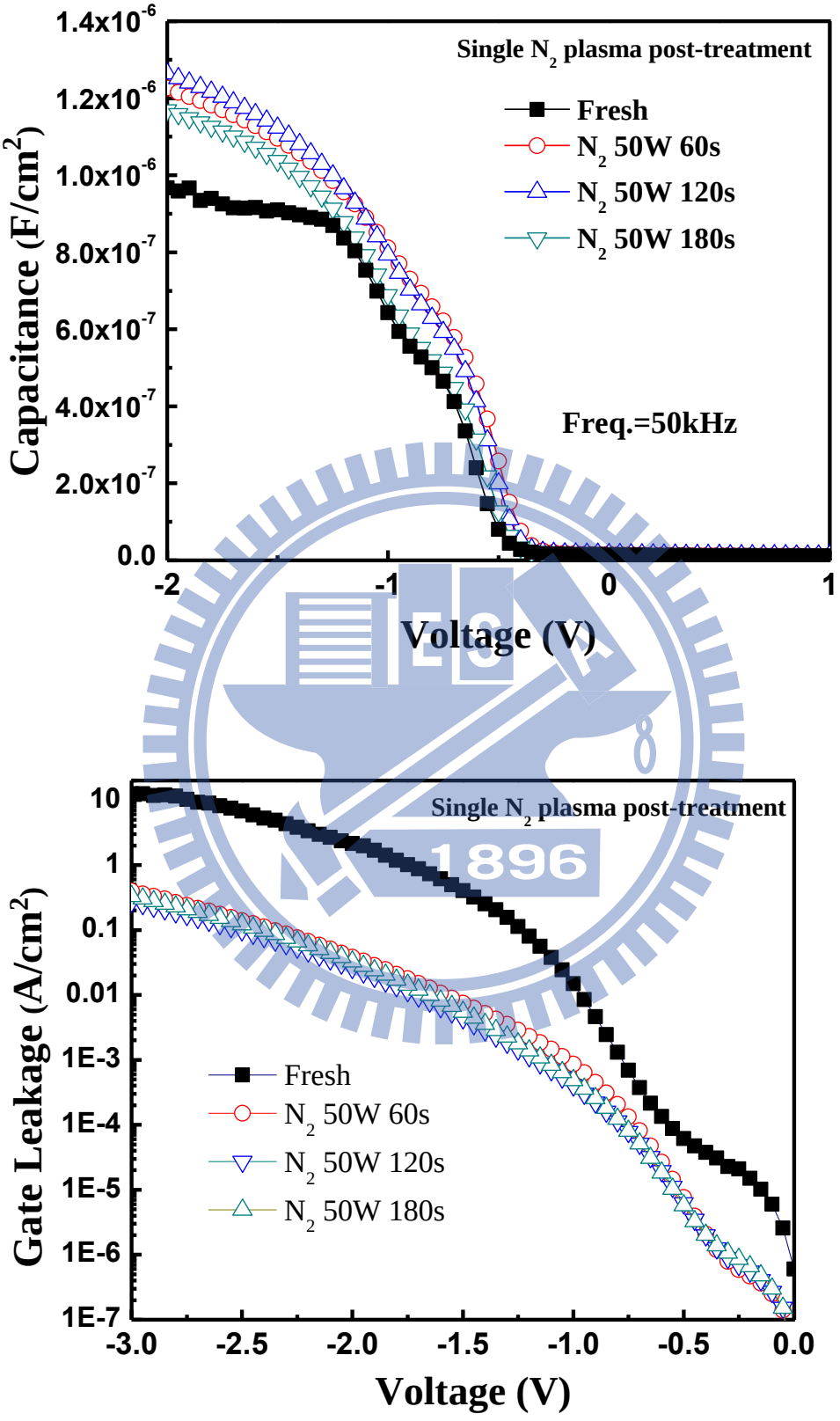

Fig. 2-2 The C-V and I-V characteristics of the HfO_2 thin films with N_2 post-treatment for different process durations.

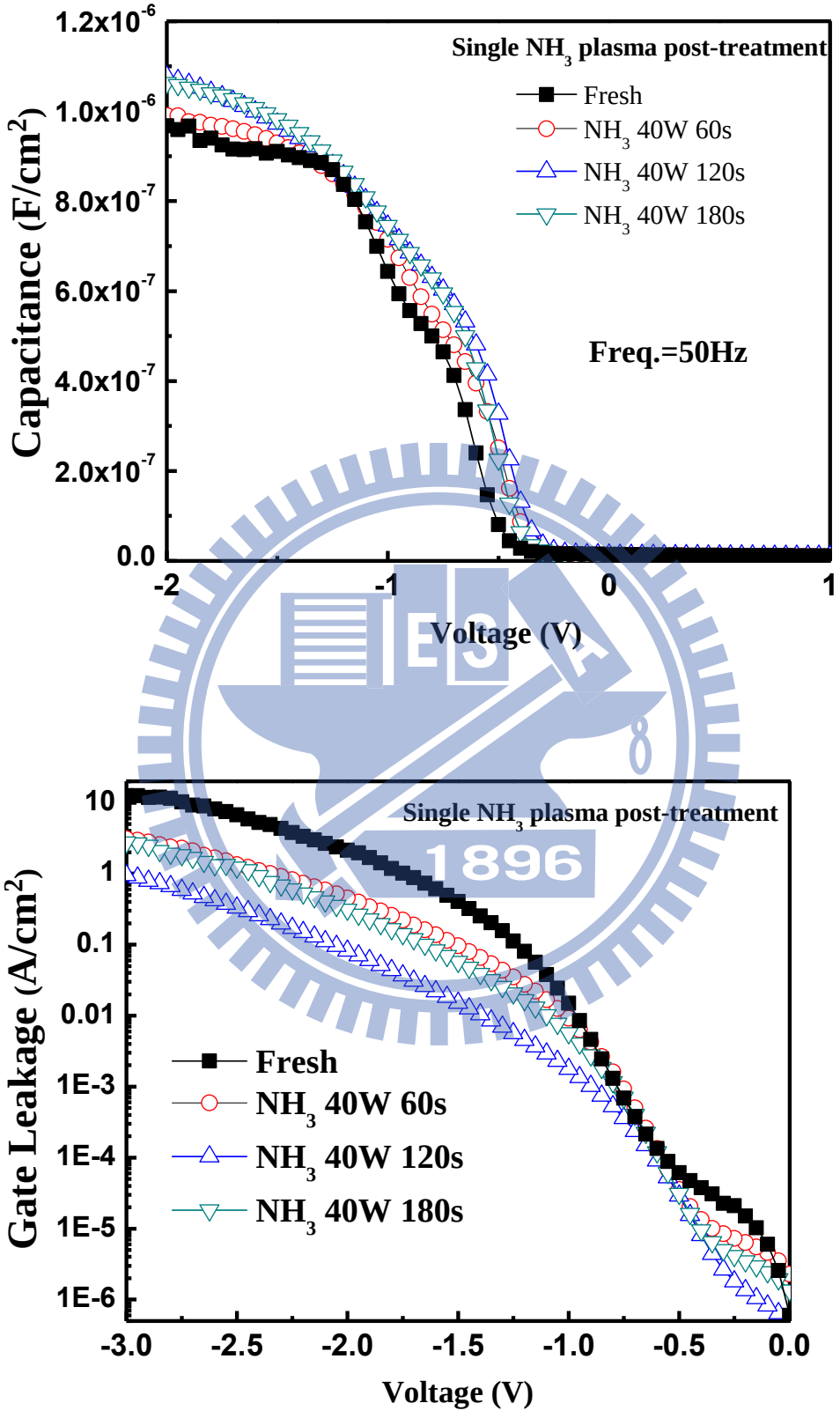

Fig. 2-3 The C-V and I-V characteristics of the HfO_2 thin films with NH_3 post-treatment for different process durations.

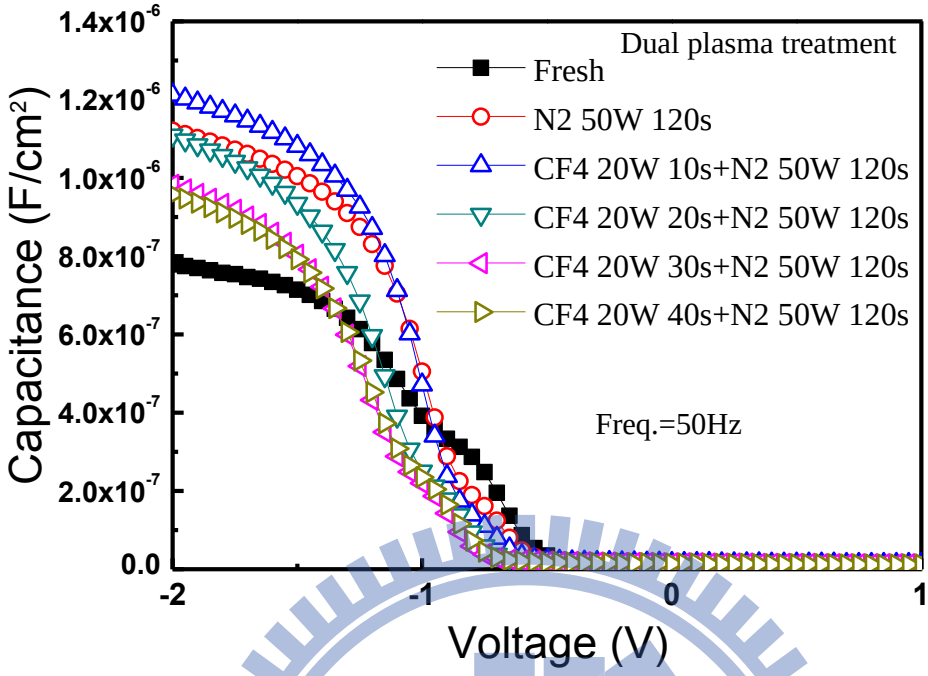

Fig. 2-4 The C-V characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and N_2 plasma for 120 sec.

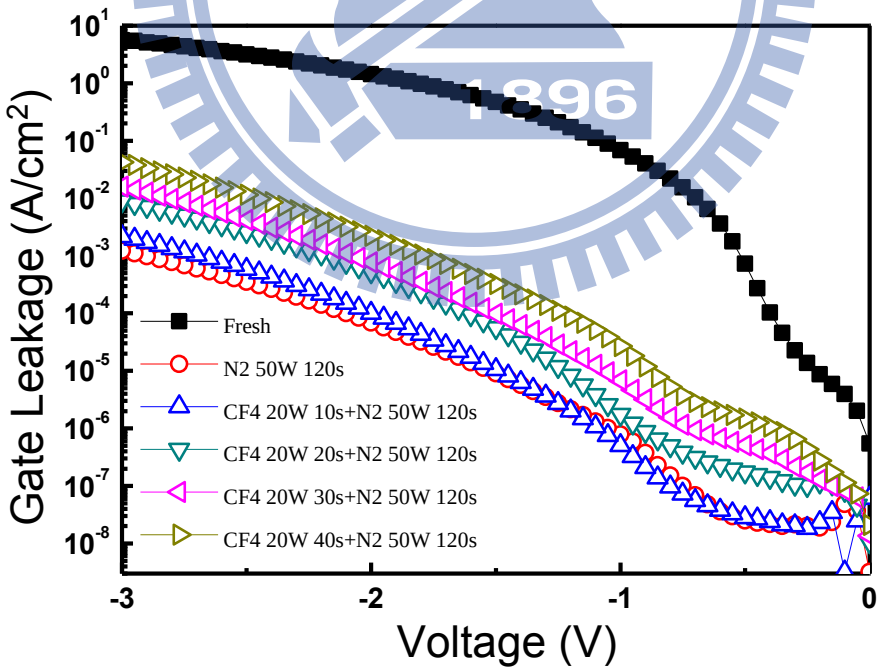

Fig. 2-5 The J-V characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and N_2 plasma for 120 sec.

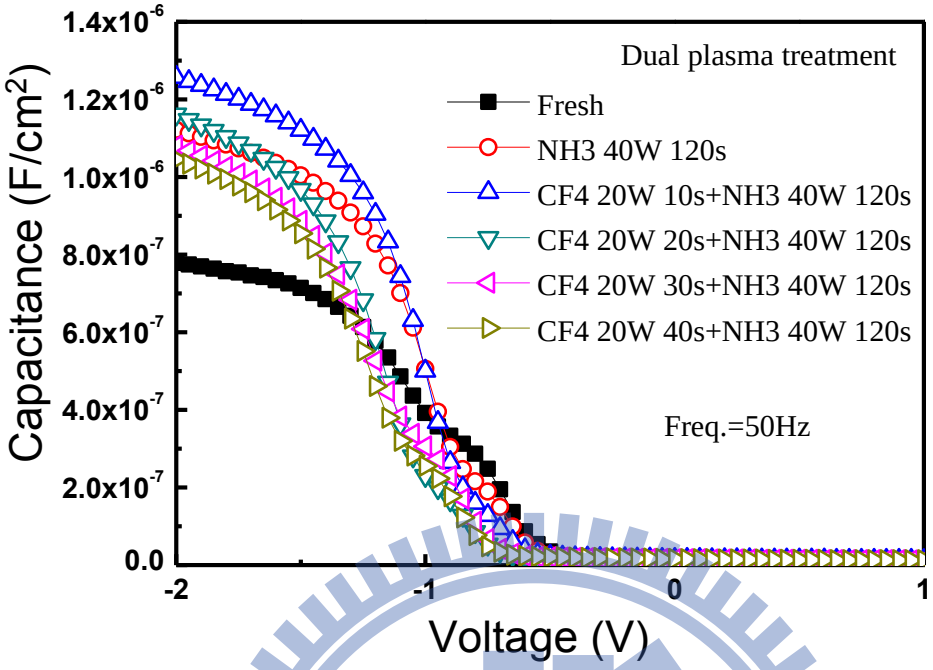

Fig. 2-6 The C-V characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 120 sec.

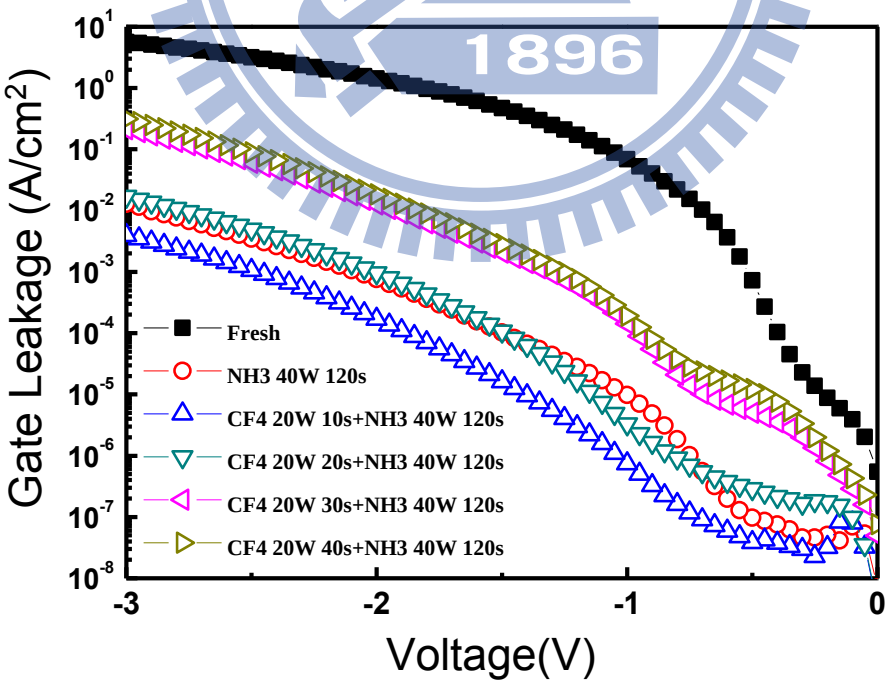

Fig. 2-7 The J-V characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 120 sec.

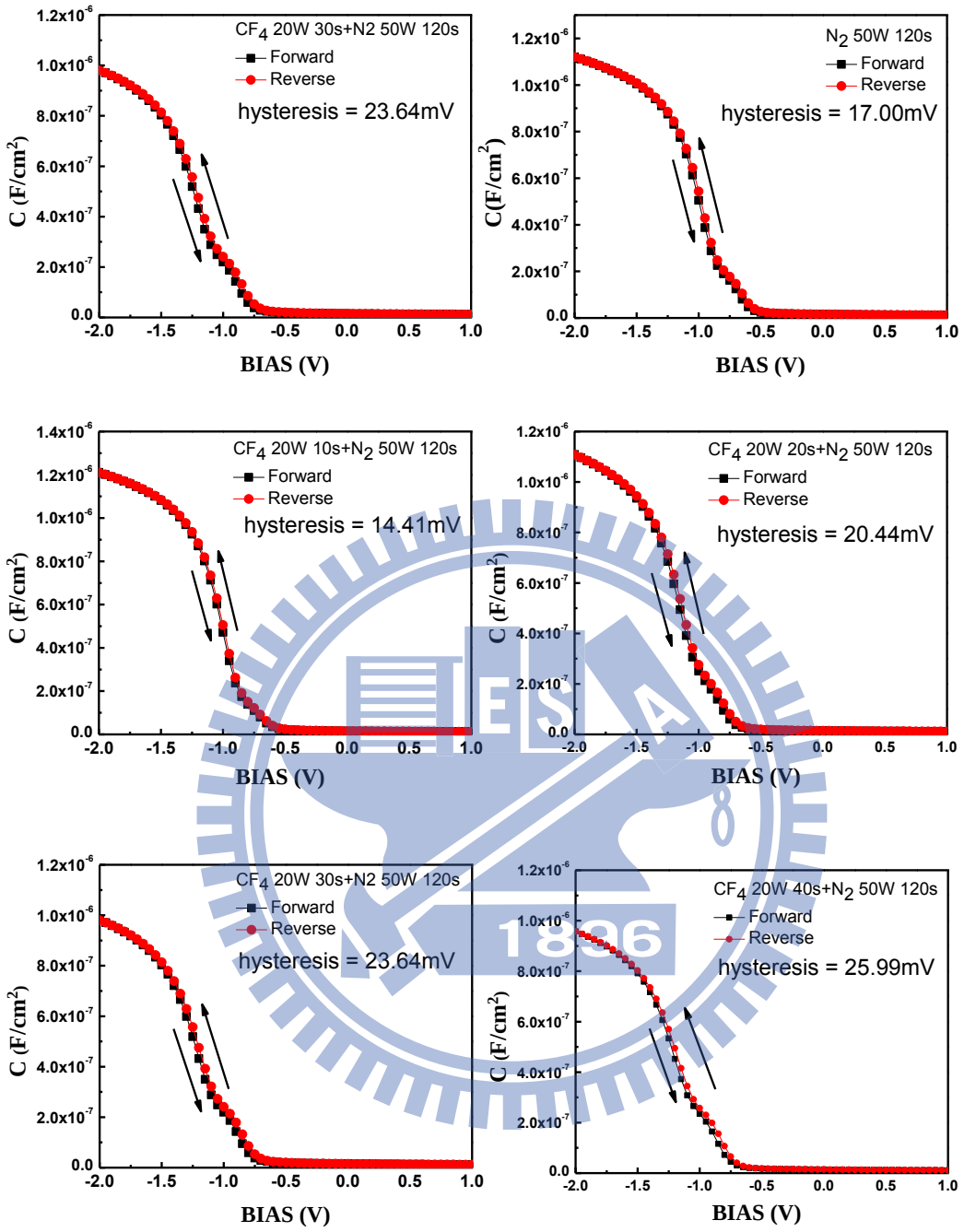

Fig. 2-8 The hysteresis characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and N_2 plasma for 120 sec.

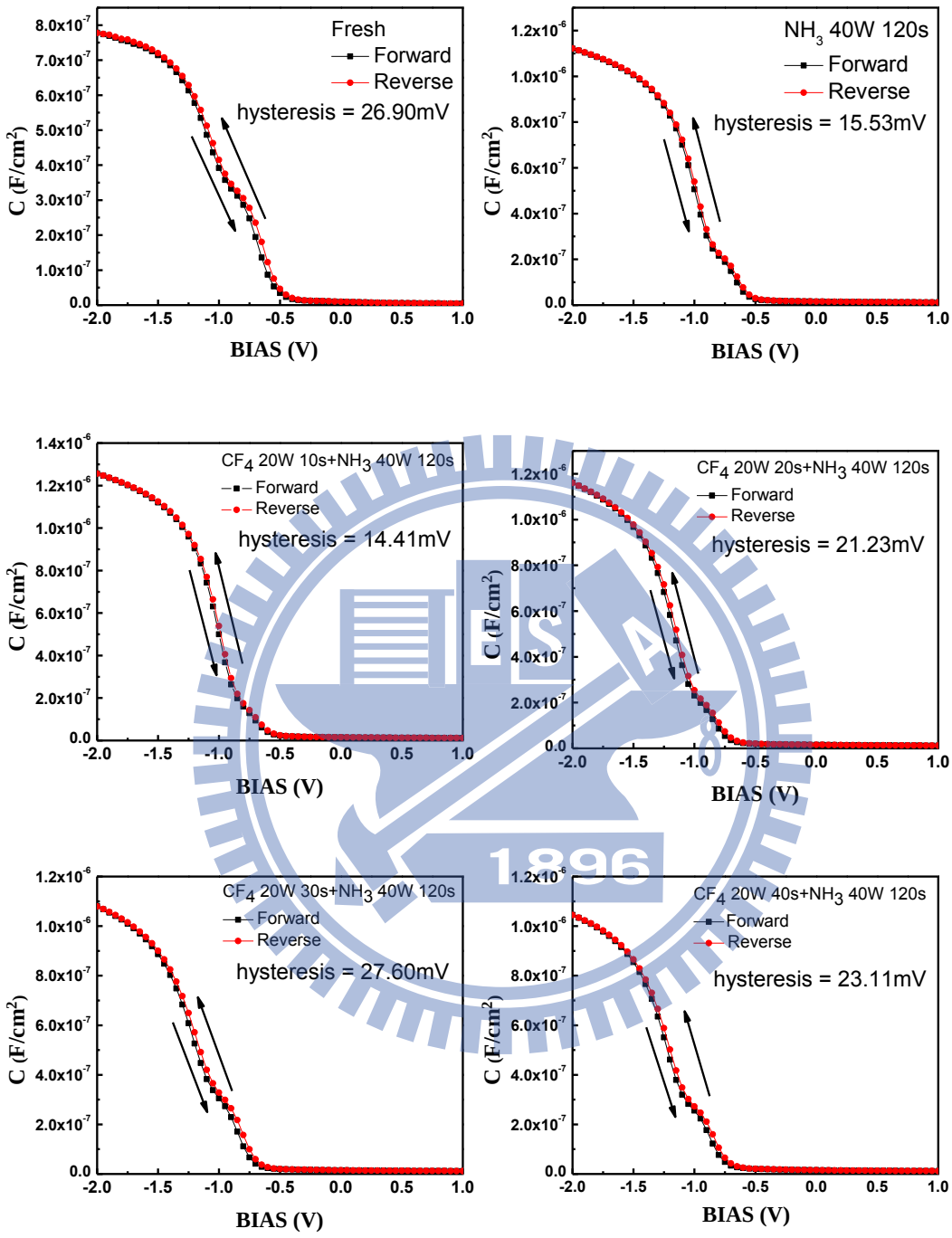

Fig. 2-9 The hysteresis characteristics of the HfO_2 thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 120 sec.

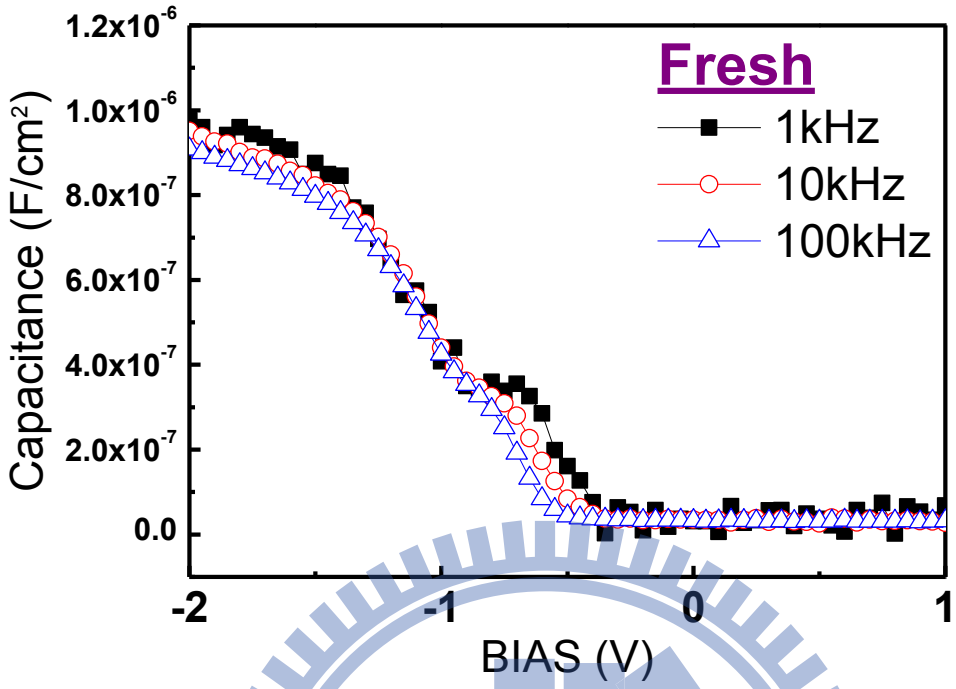

Fig. 2-10 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors for fresh sample.

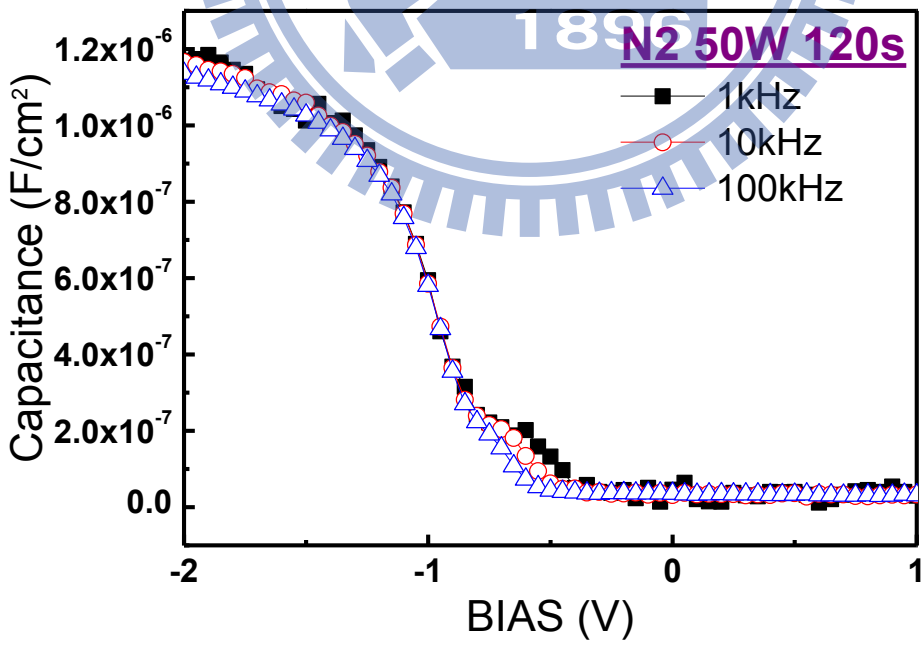

Fig. 2-11 frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in N_2 120 sec.

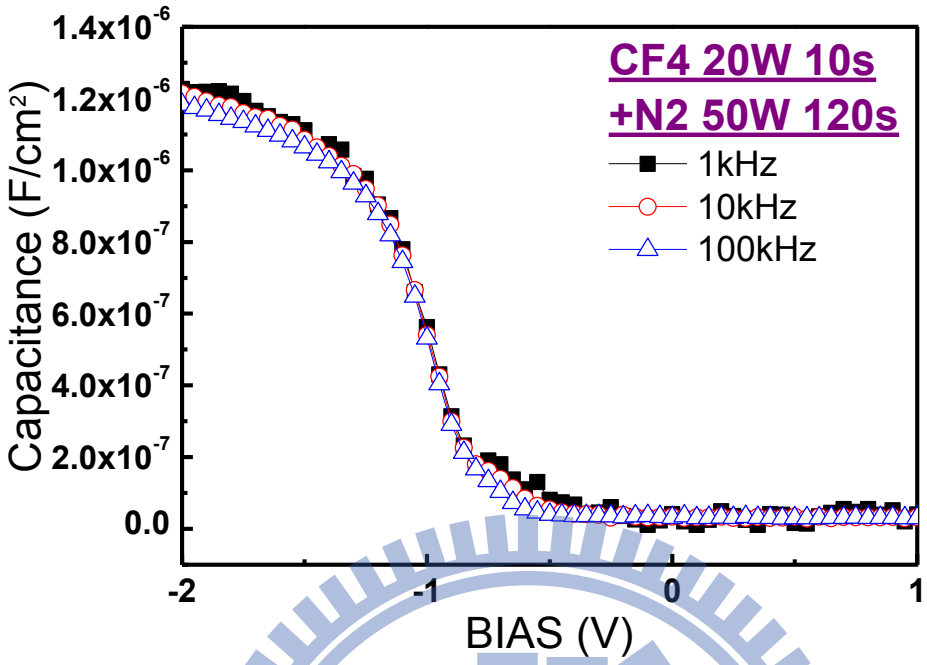

Fig. 2-12 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 10 sec + N_2 120 sec.

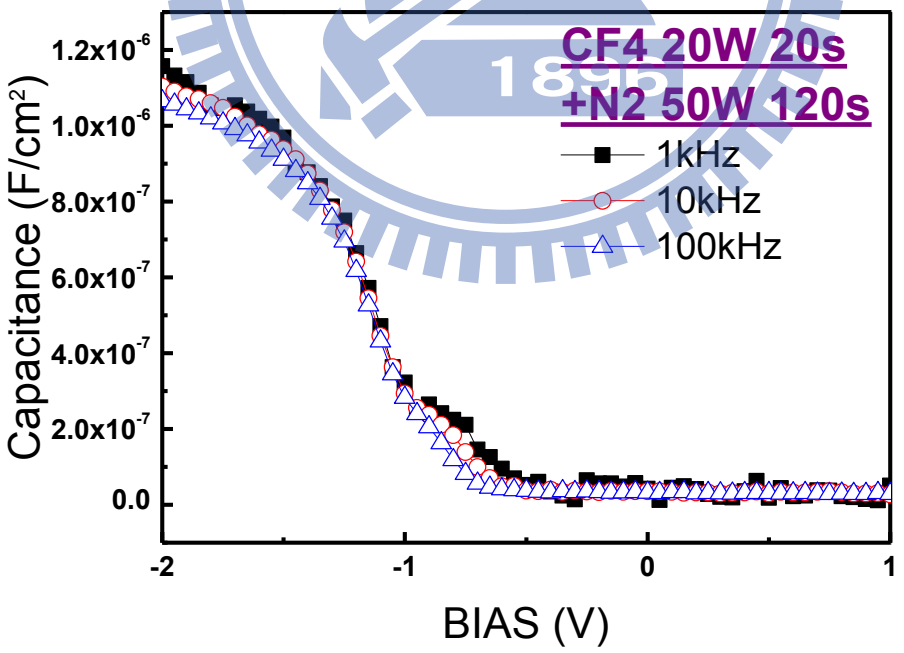

Fig. 2-13 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 20 sec + N_2 120 sec.

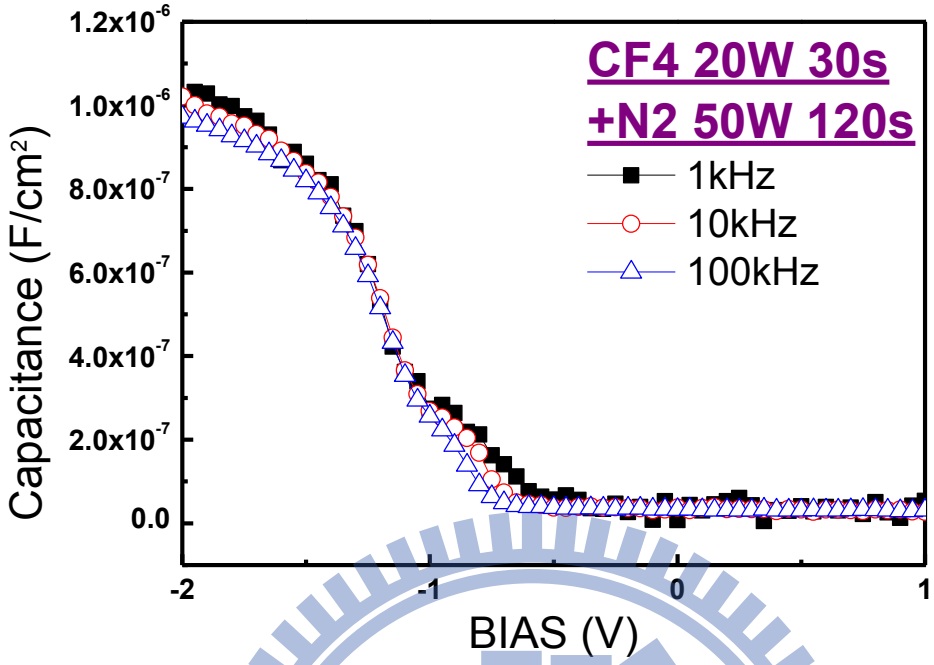

Fig. 2-14 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 30 sec + N_2 120 sec.

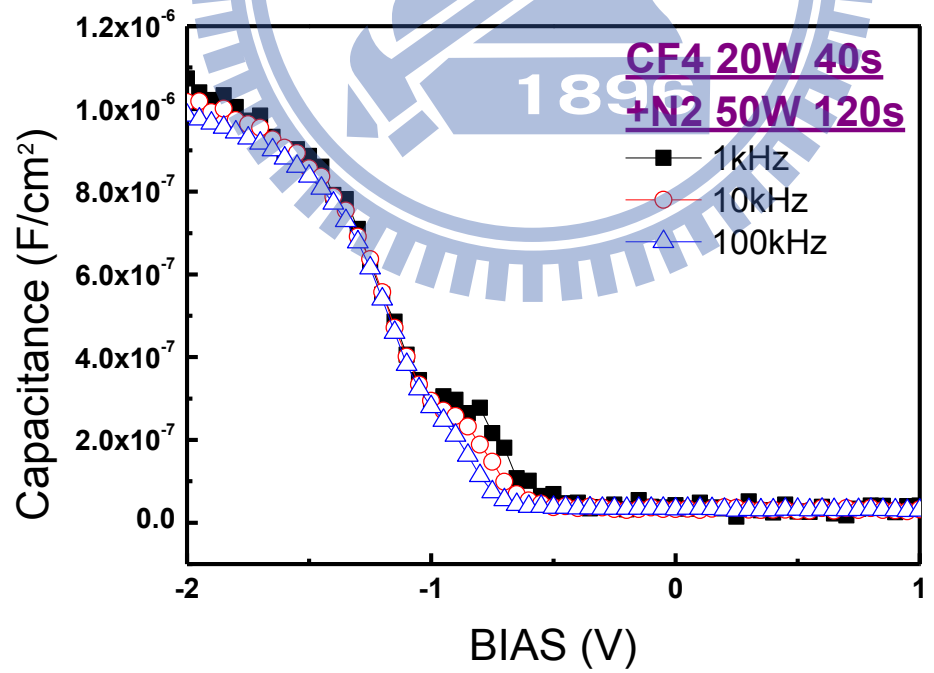

Fig. 2-15 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors for treated in CF_4 40 sec + N_2 120 sec.

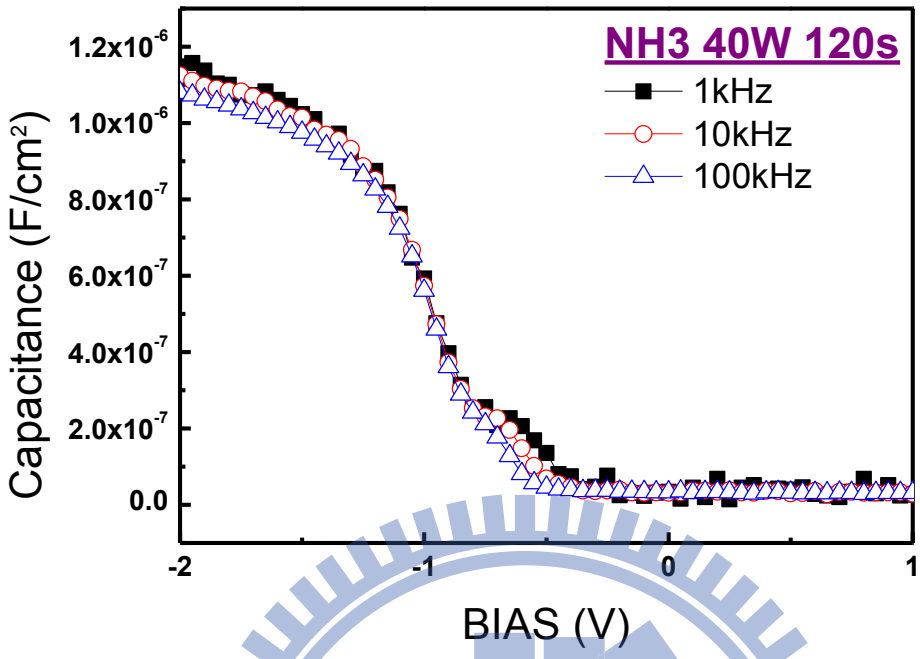

Fig. 2-16 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in NH_3 120 sec.

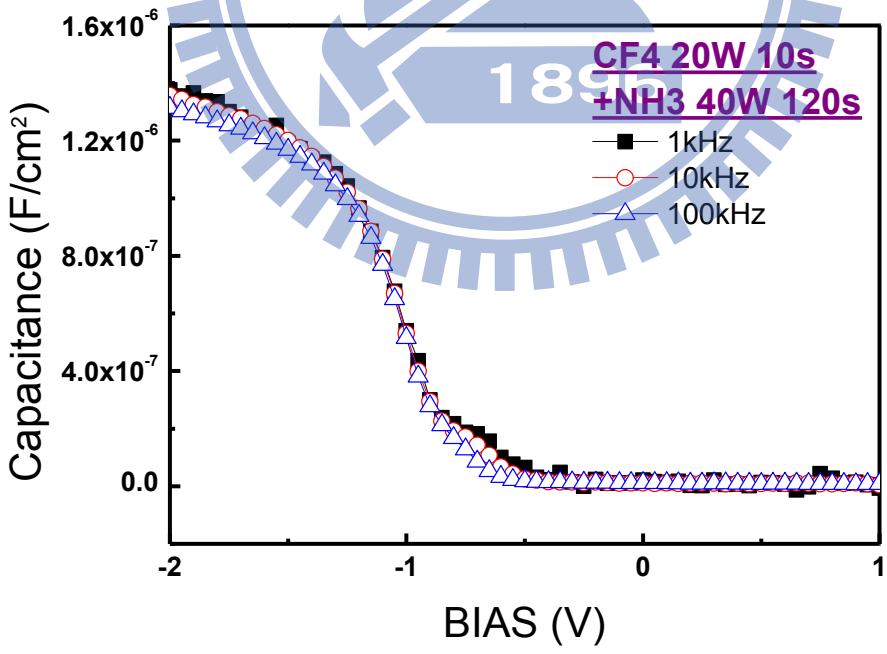

Fig. 2-17 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 10 sec + NH_3 120 sec.

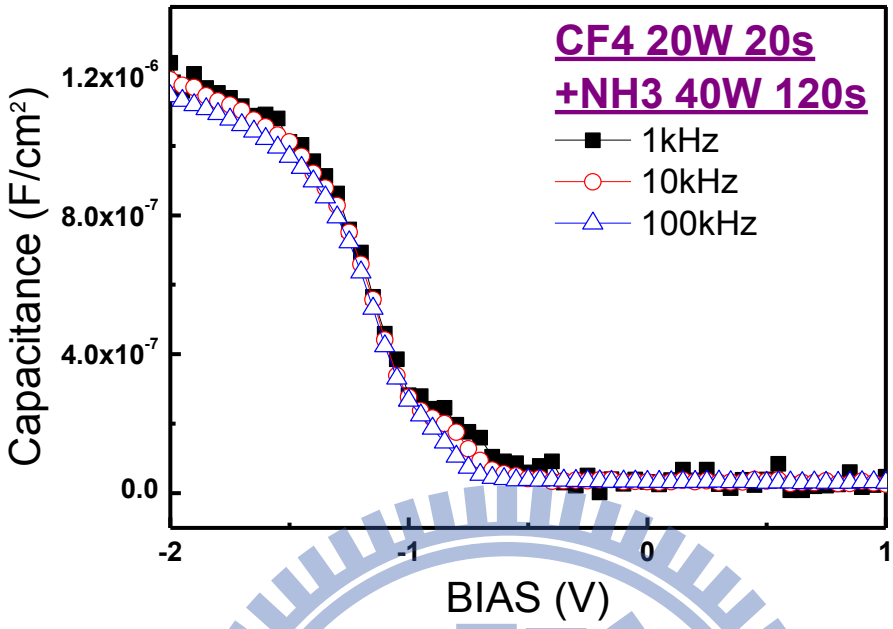

Fig. 2-18 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 20 sec + NH_3 120 sec.

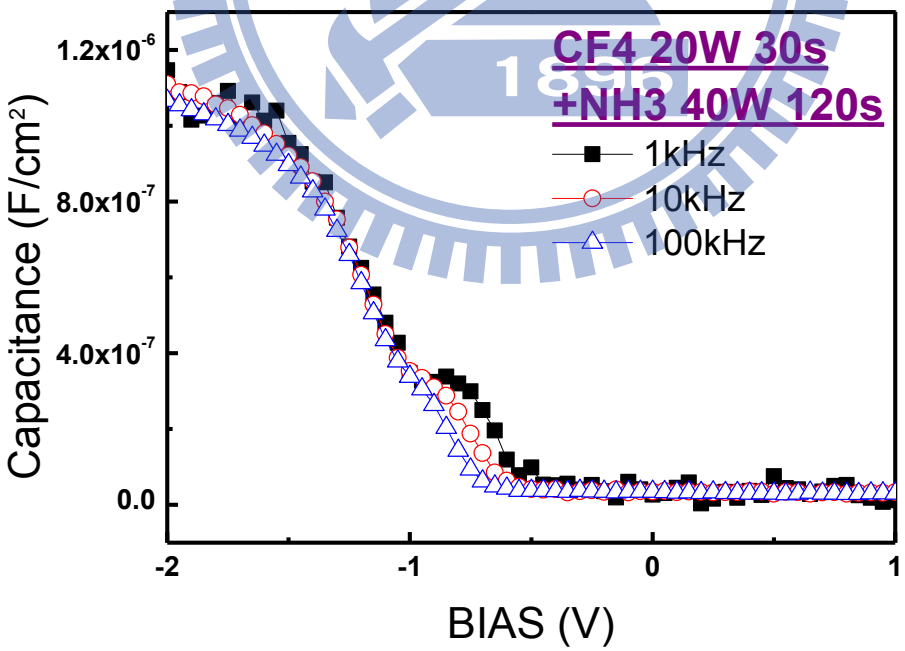

Fig. 2-19 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 30 sec + NH_3 120 sec.

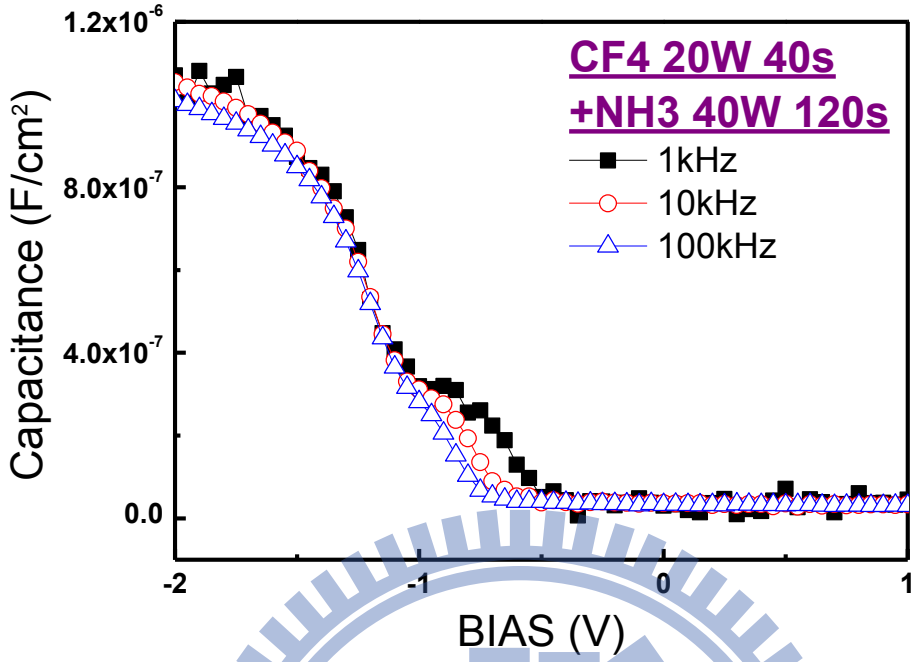

Fig. 2-20 Frequency dependence of C-V curve for the Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 40 sec + NH_3 120 sec.

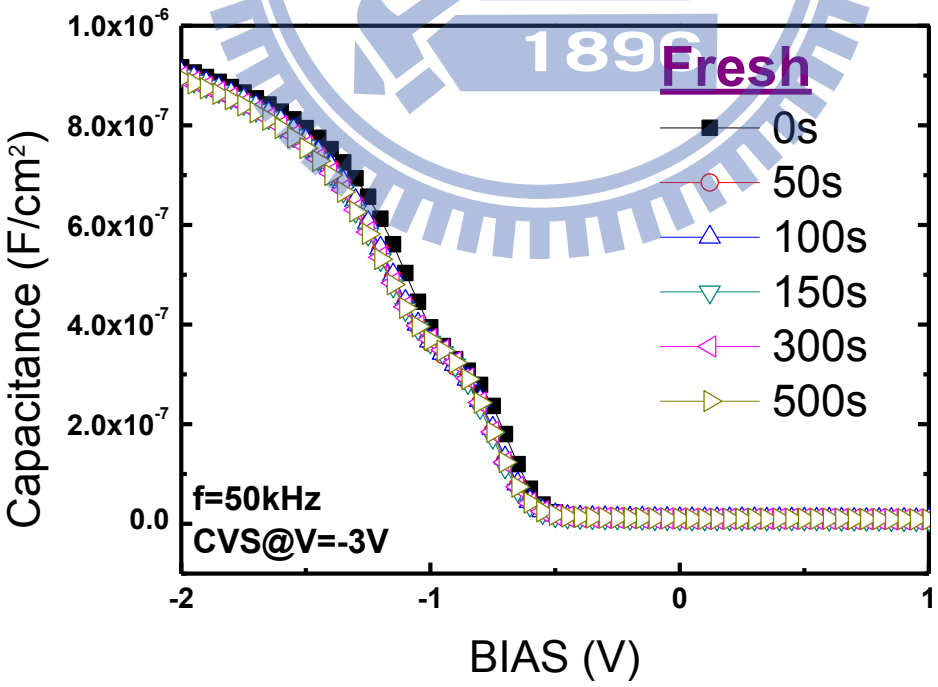

Fig. 2-21 C-V curves of Al/Ti/HfO_2/Si MIS capacitors for Fresh sample before and after CVS condition. The stress voltage is -3 V.

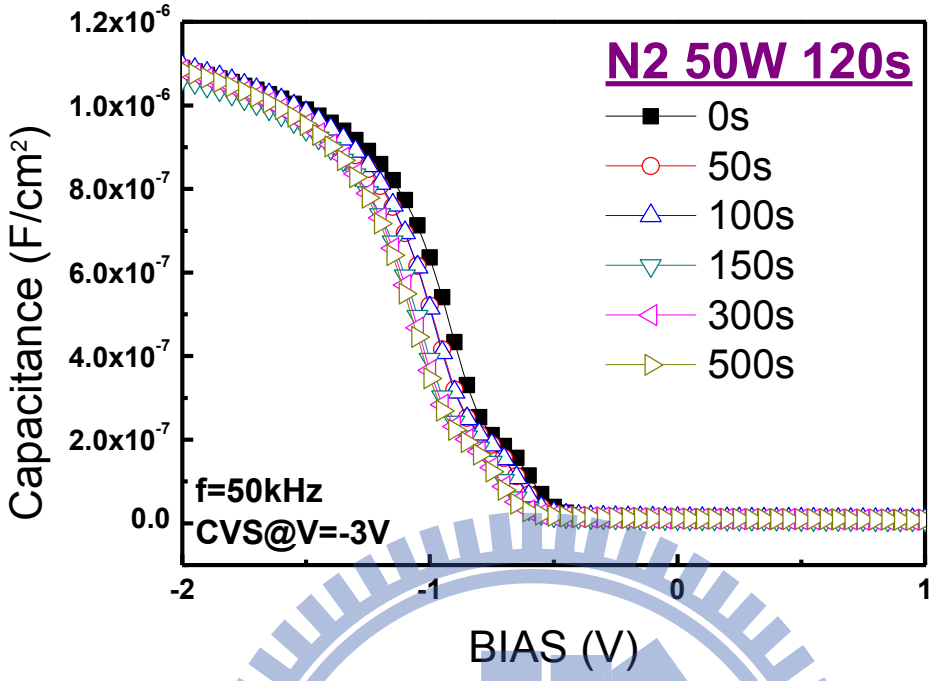

Fig. 2-22 C-V curves of Al/Ti/HfO_2/Si MIS capacitors treated in N_2 120 sec before and after CVS condition. The stress voltage is -3 V.

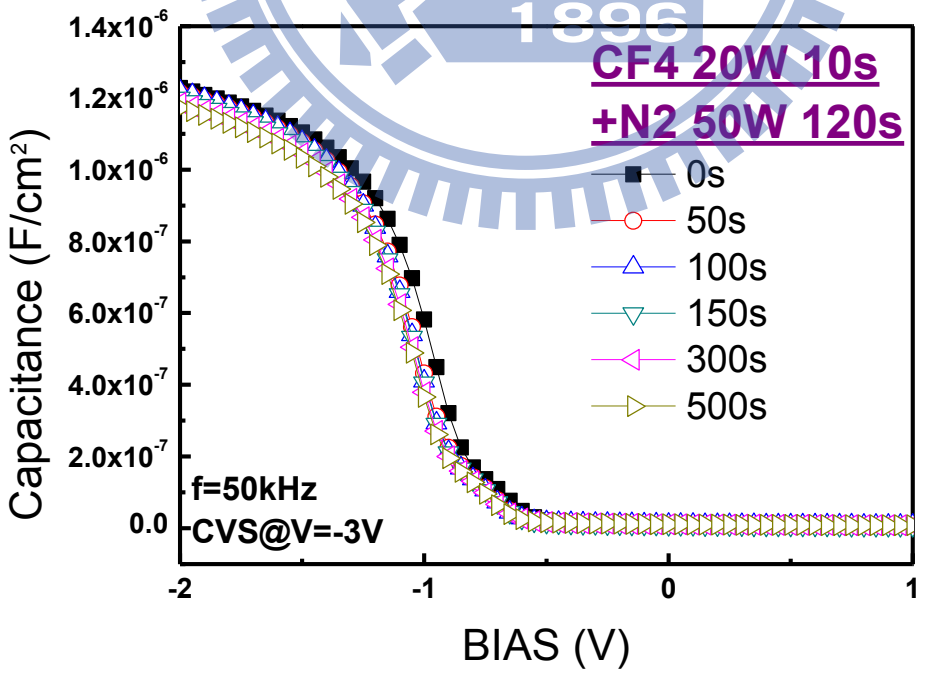

Fig. 2-23 C-V curves of Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 10 sec + N_2 120 sec before and after CVS condition. The stress voltage is -3 V.

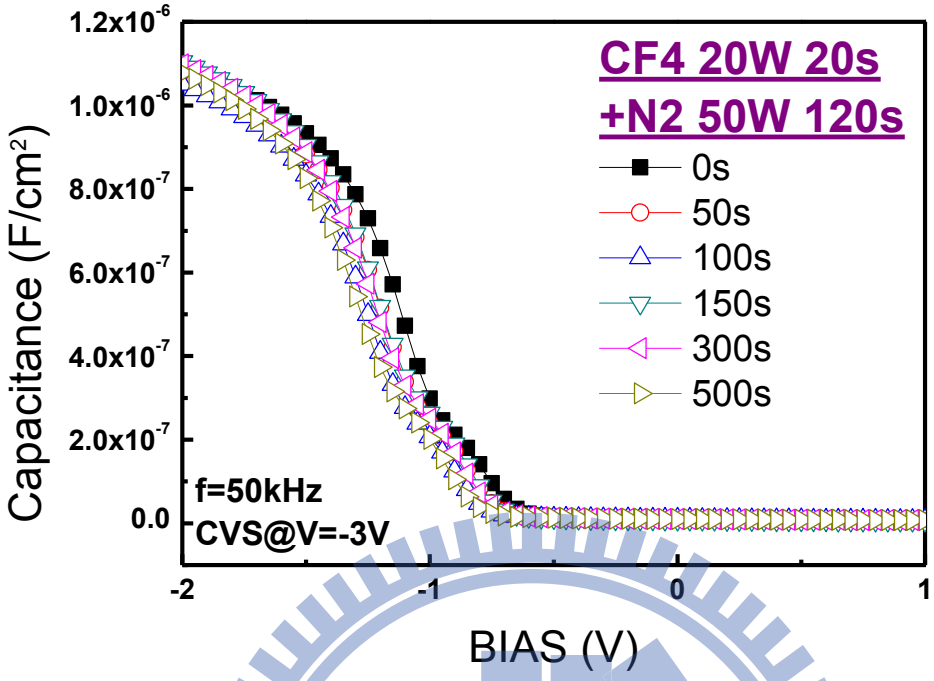

Fig. 2-24 C-V curves of Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 20 sec + N_2 120 sec before and after CVS condition. The stress voltage is -3 V.

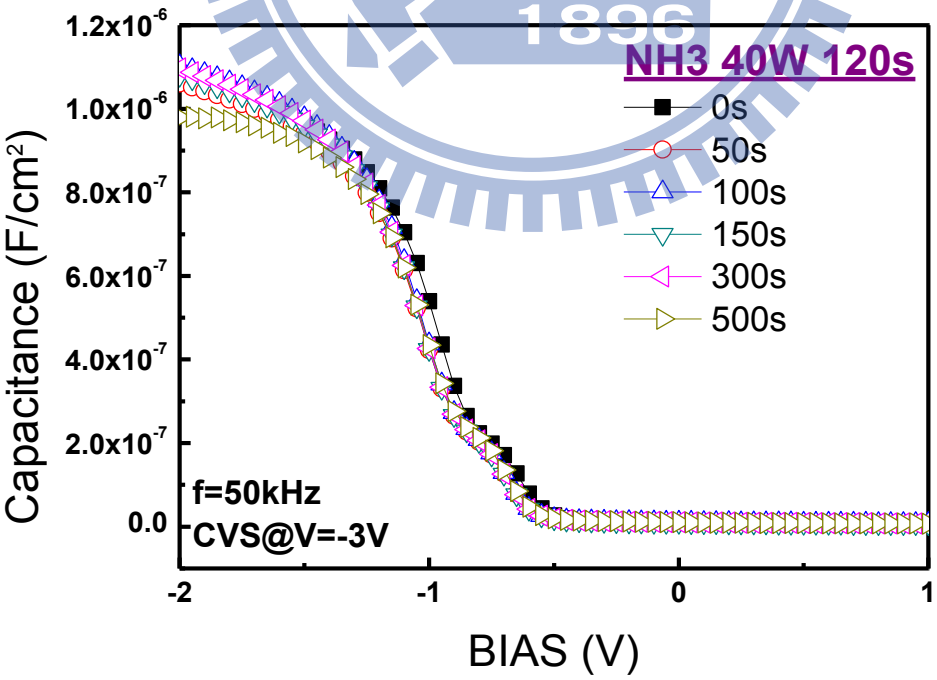

Fig. 2-25 C-V curves of Al/Ti/HfO_2/Si MIS capacitors treated in NH_3 120 sec before and after CVS condition. The stress voltage is -3 V.

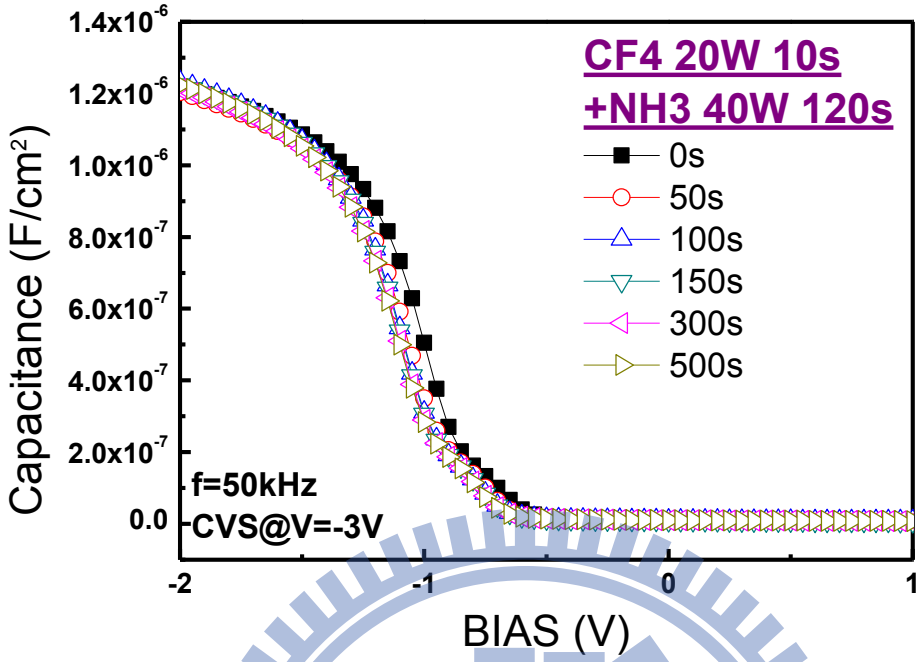

Fig. 2-26 C-V curves of Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 10 sec + NH_3 120 sec before and after CVS condition. The stress voltage is -3 V.

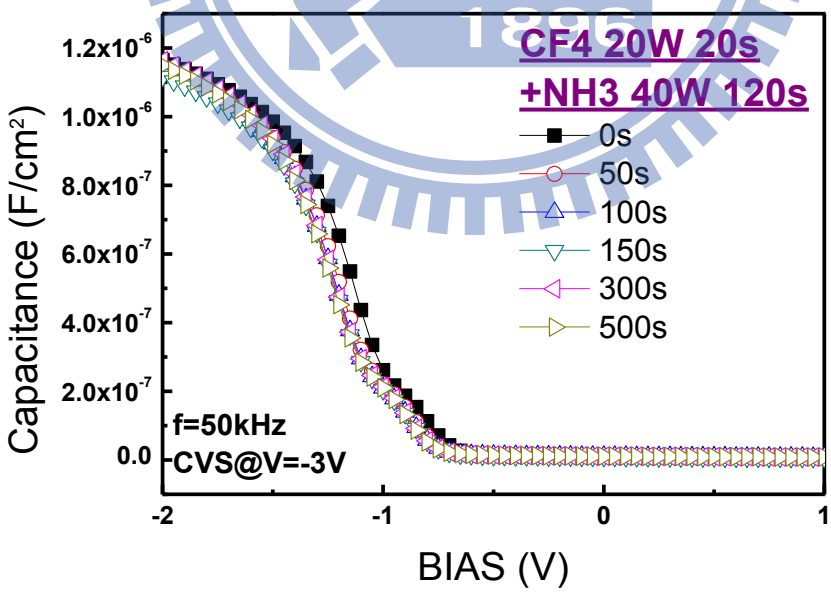

Fig. 2-27 C-V curves of Al/Ti/HfO_2/Si MIS capacitors treated in CF_4 20 sec + NH_3 120 sec before and after CVS condition. The stress voltage is -3 V.

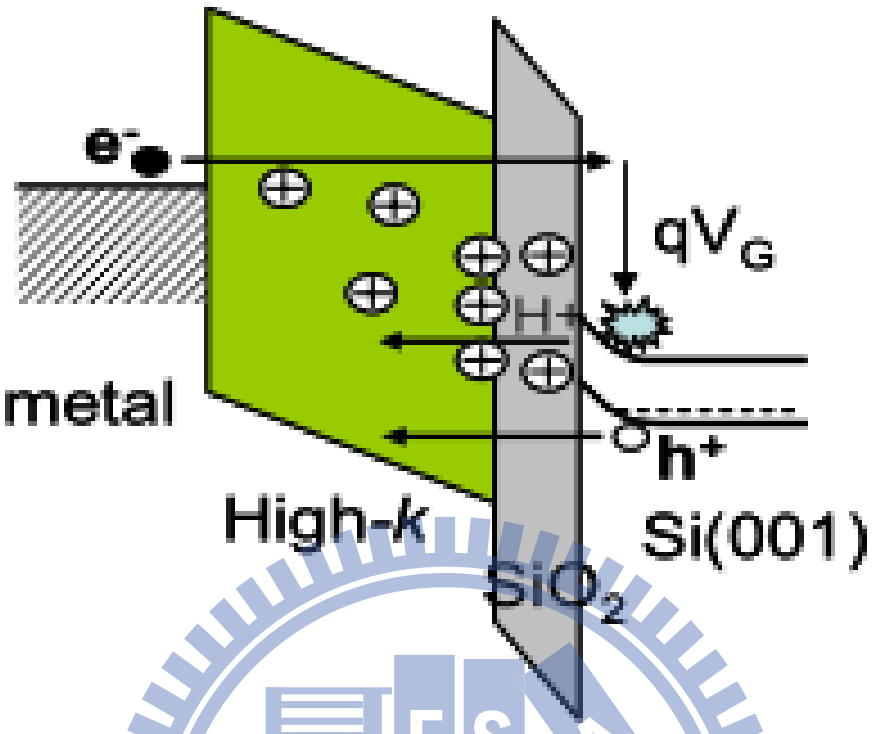

Fig. 2-28 Schematic of the band diagram of HfO_2 gate stake structure under constant negative voltage stress [18].

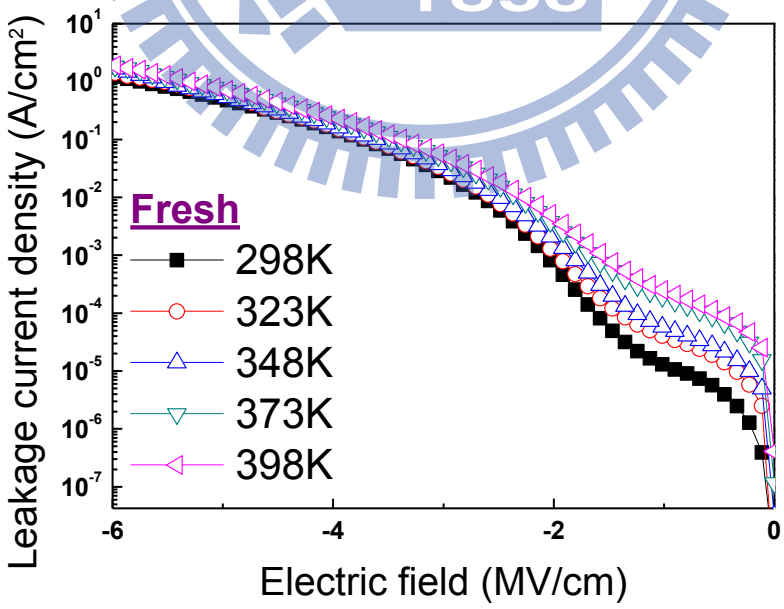

Fig. 2-29 The J-E curves plots for the sample without treatment at different temperatures from 298 K to 398 K.

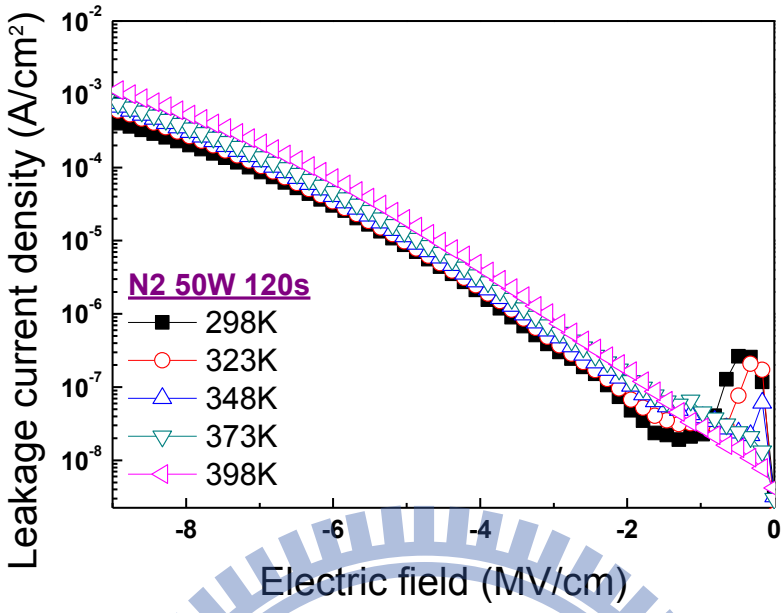

Fig. 2-30 The J-E curves plots for the sample treated in N_2 120 sec at different temperatures from 298 K to 398 K.

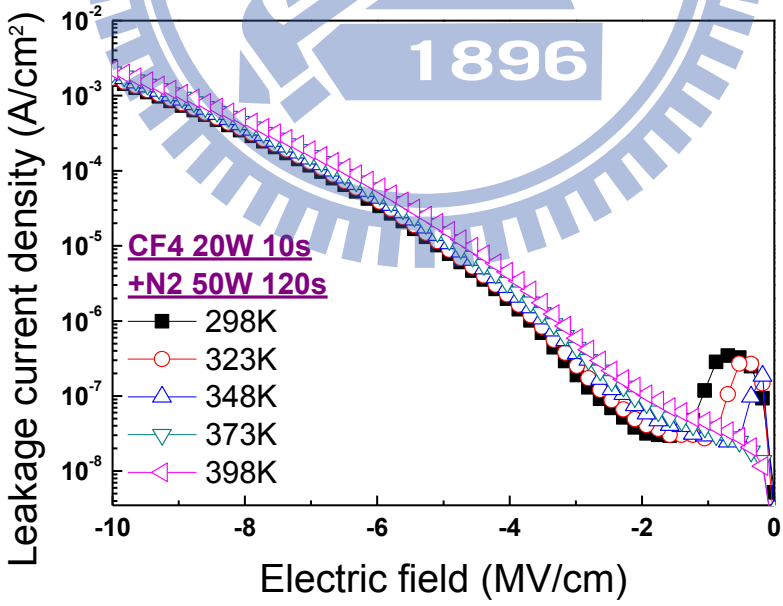

Fig. 2-31 The J-E curves plots for the sample treated in CF_4 10 sec + N_2 120 sec at different temperatures from 298 K to 398 K.

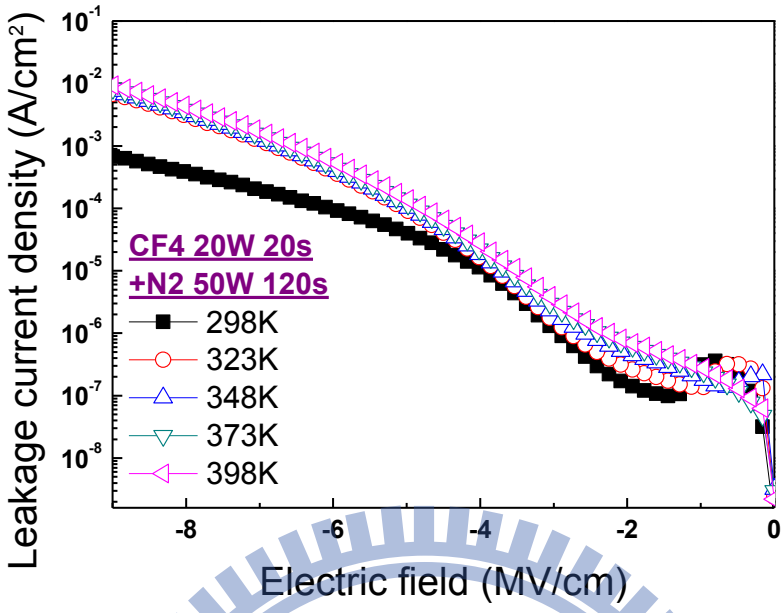

Fig. 2-32 The J-E curves plots for the sample treated in CF_4 20 sec + N_2 120 sec at different temperatures from 298 K to 398 K.

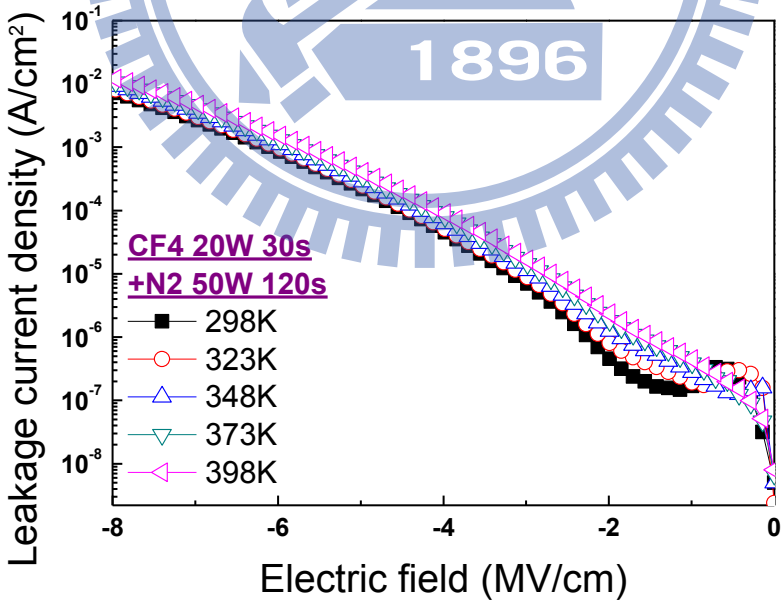

Fig. 2-33 The J-E curves plots for the sample treated in CF_4 30 sec + N_2 120 sec at different temperatures from 298 K to 398 K.

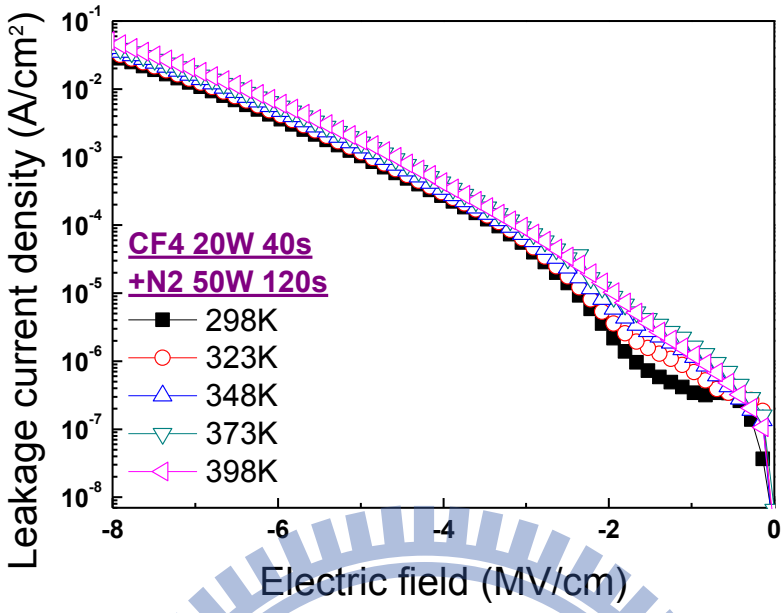

Fig. 2-34 The J-E curves plots for the sample treated in CF_4 40 sec + N_2 120 sec at different temperatures from 298 K to 398 K.

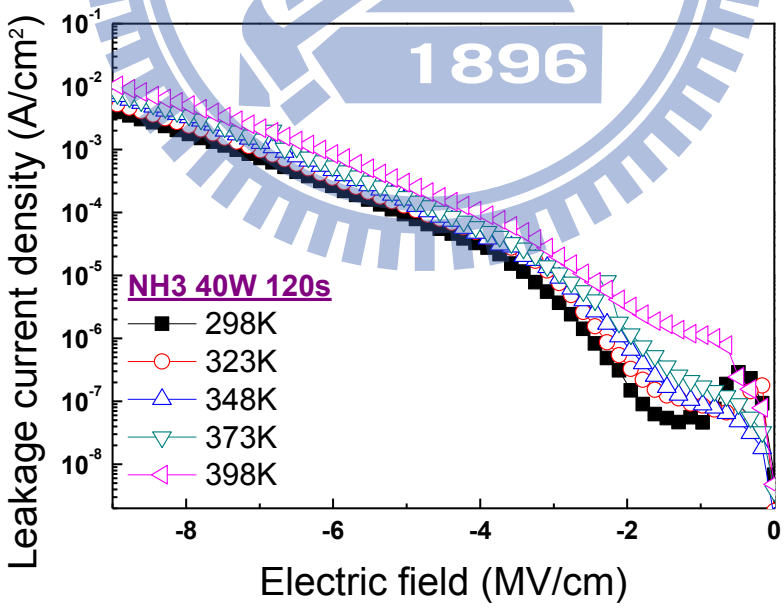

Fig. 2-35 The J-E curves plots for the sample treated in NH_3 120 sec at different temperatures from 298 K to 398 K.

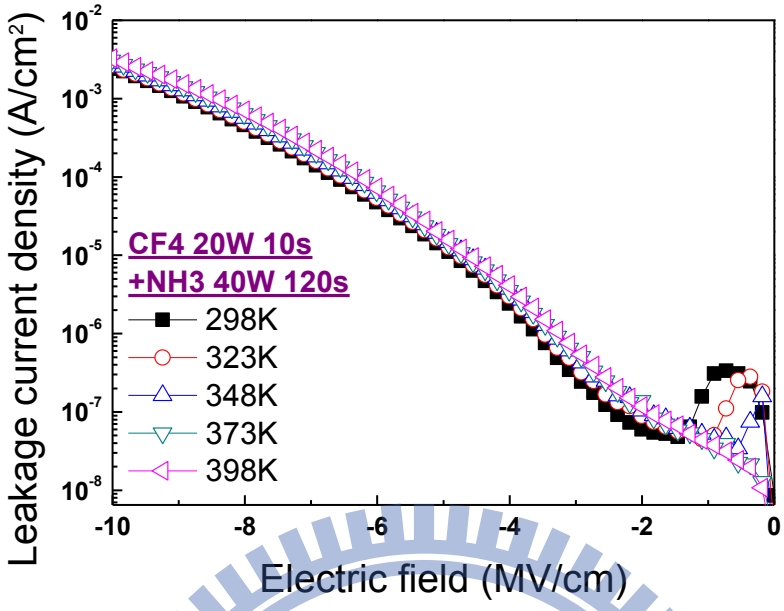

Fig. 2-36 The J-E curves plots for the sample treated in CF_4 10 sec + NH_3 120 sec at different temperatures from 298 K to 398 K.

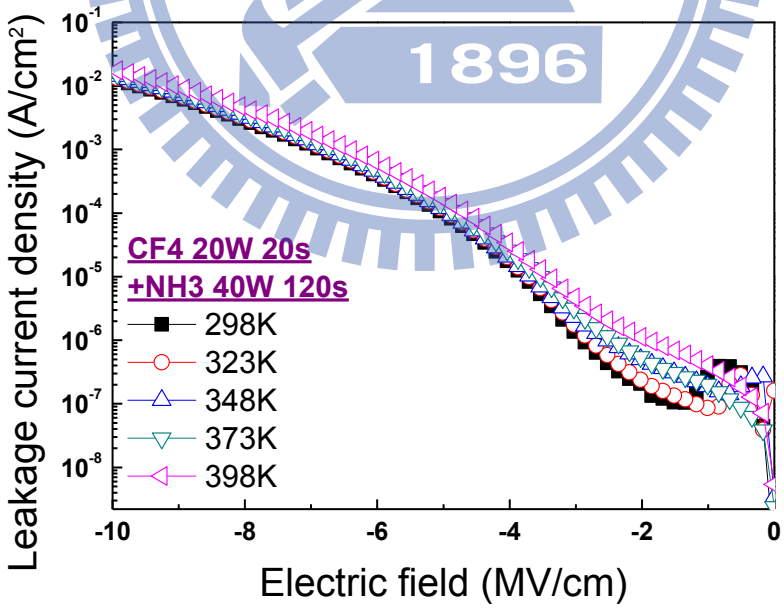

Fig. 2-37 The J-E curves plots for the sample treated in CF_4 20 sec + NH_3 120 sec at different temperatures from 298 K to 398 K.

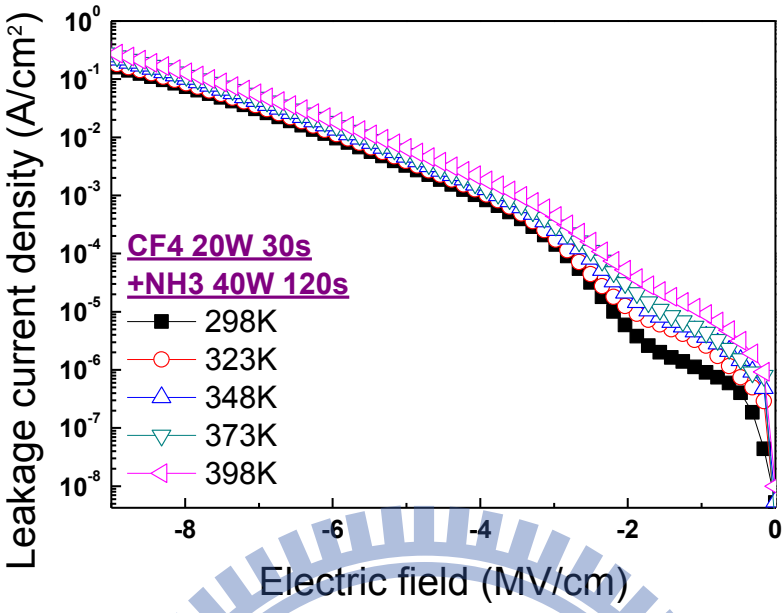

Fig. 2-38 The J-E curves plots for the sample treated in CF_4 30 sec + NH_3 120 sec at different temperatures from 298 K to 398 K.

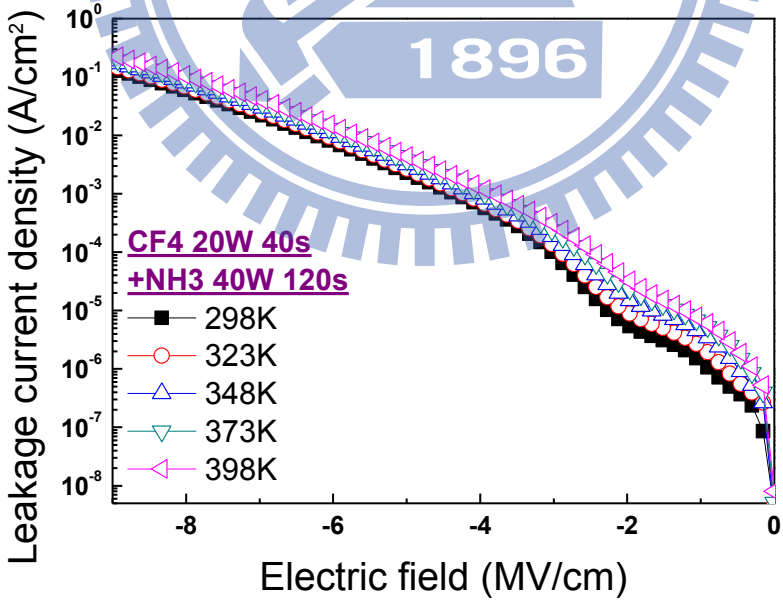

Fig. 2-39 The J-E curves plots for the sample treated in CF_4 40 sec + NH_3 120 sec at different temperatures from 298 K to 398 K.

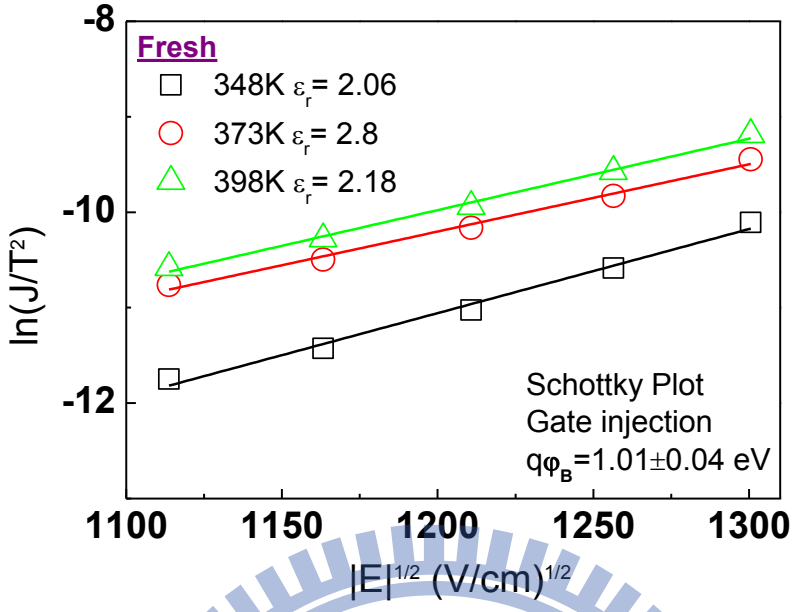

Fig. 2-40 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with no treatment at different temperatures (348K, 373K, and 398K).

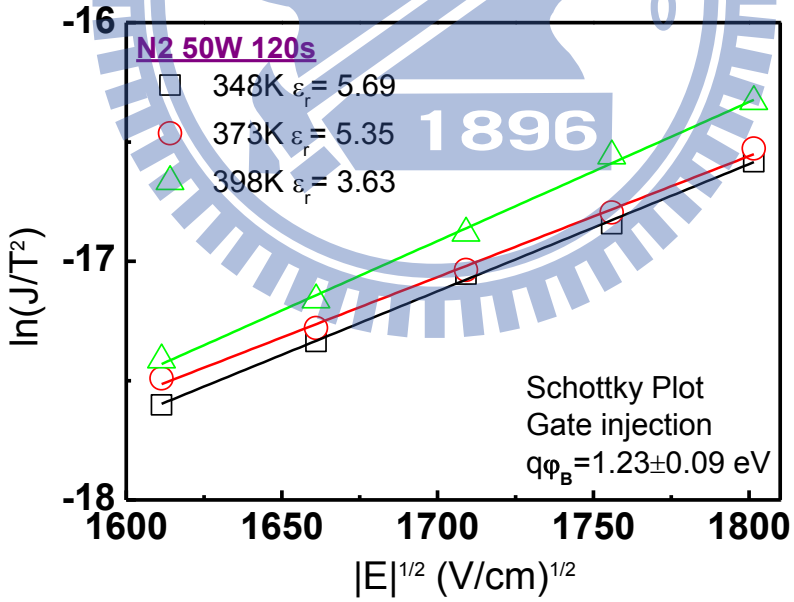

Fig. 2-41 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with N_2 120 sec at different temperatures (348K, 373K, and 398K).

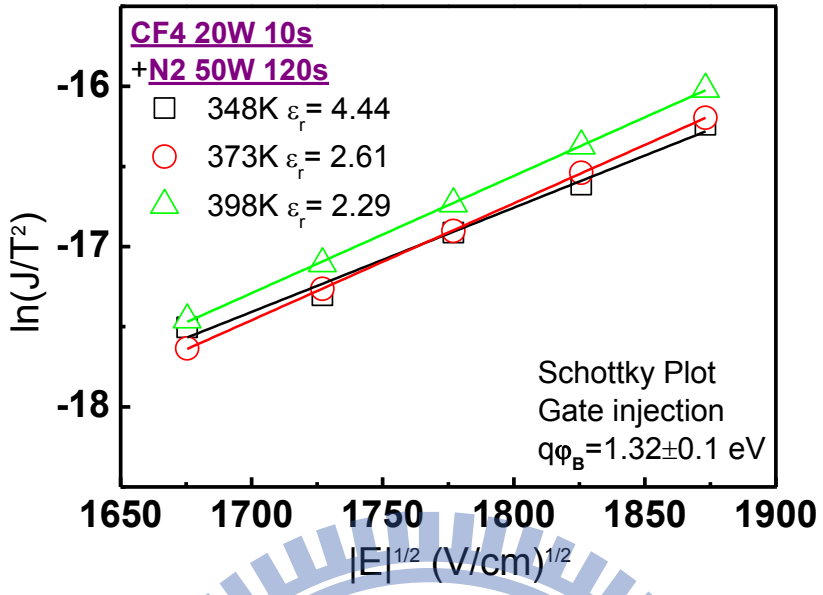

Fig. 2-42 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 10 sec + N_2 120 sec at different temperatures (348K, 373K, and 398K).

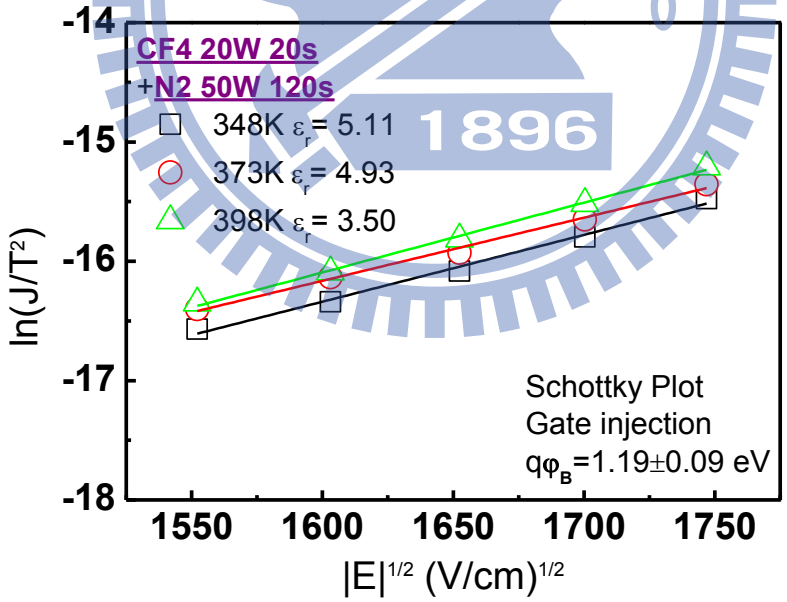

Fig. 2-43 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 20 sec + N_2 120 sec at different temperatures (348K, 373K, and 398K).

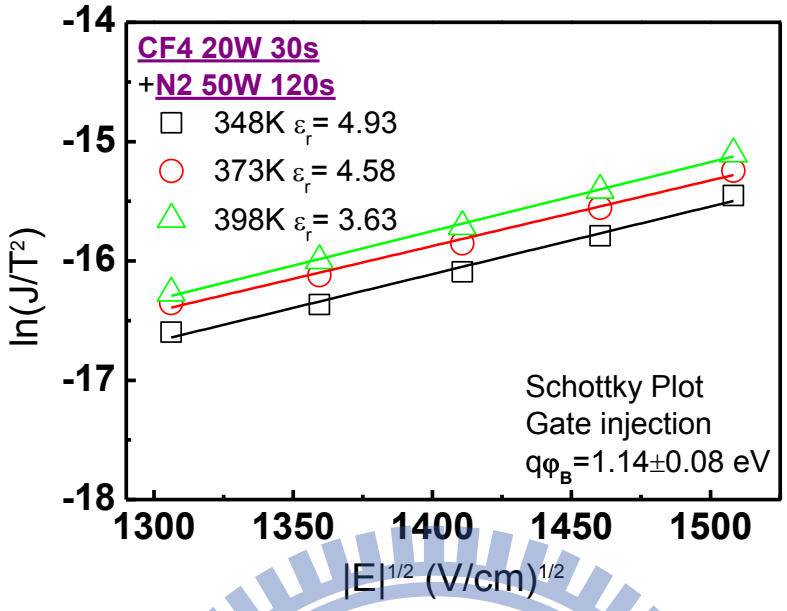

Fig. 2-44 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 30 sec + N_2 120 sec at different temperatures (348K, 373K, and 398K).

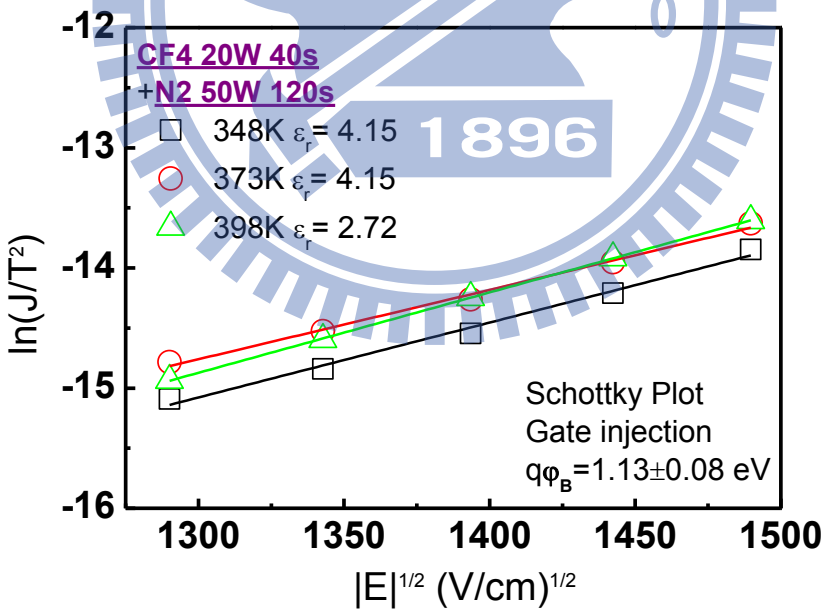

Fig. 2-45 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 40 sec + N_2 120 sec at different temperatures (348K, 373K, and 398K).

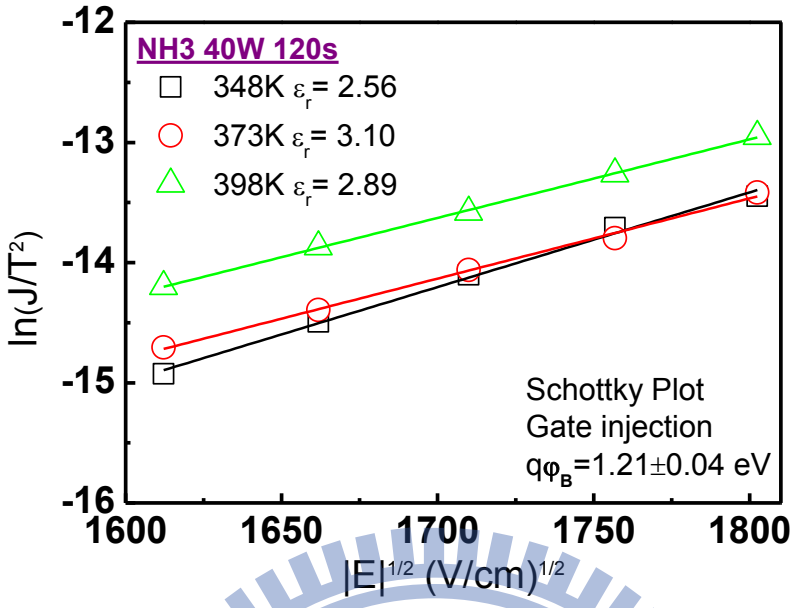

Fig. 2-46 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with NH_3 120 sec at different temperatures (348K, 373K, and 398K).

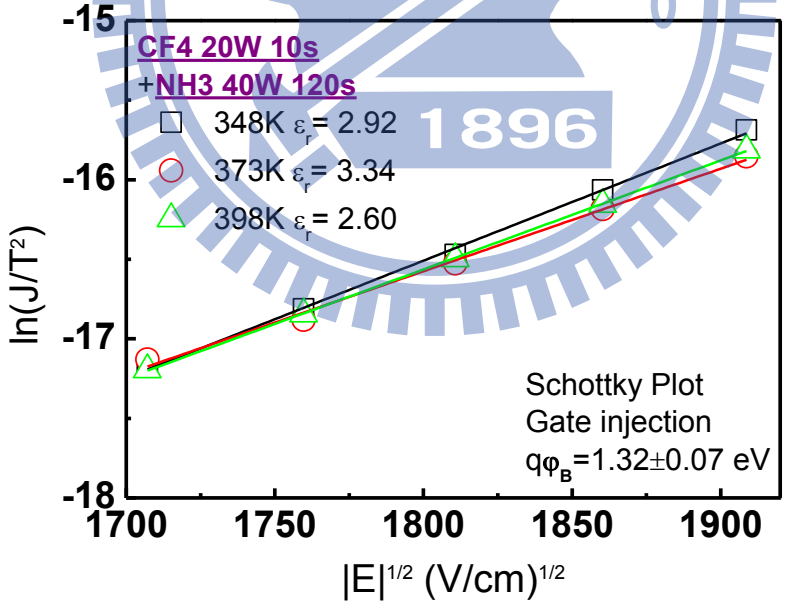

Fig. 2-47 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 10 sec + NH_3 120 sec at different temperatures (348K, 373K, and 398K).

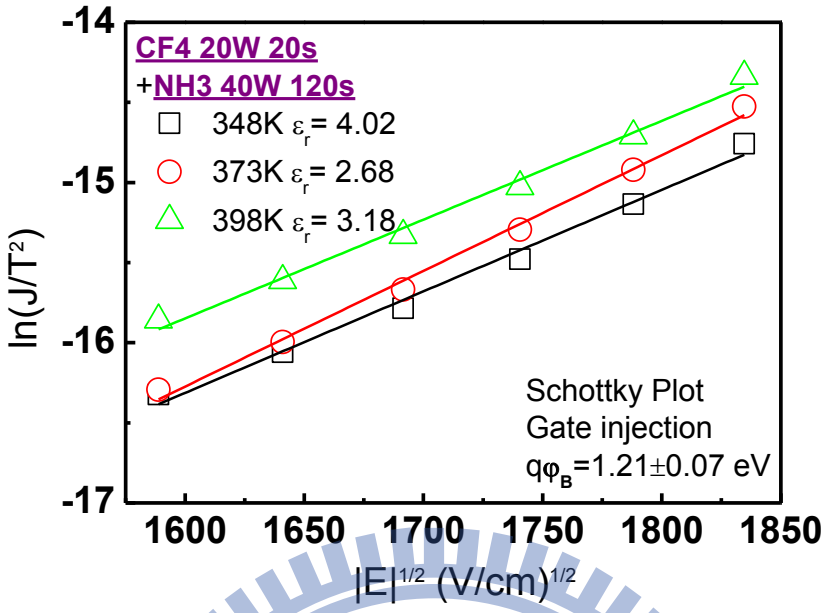

Fig. 2-48 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 20 sec + NH_3 120 sec at different temperatures (348K, 373K, and 398K).

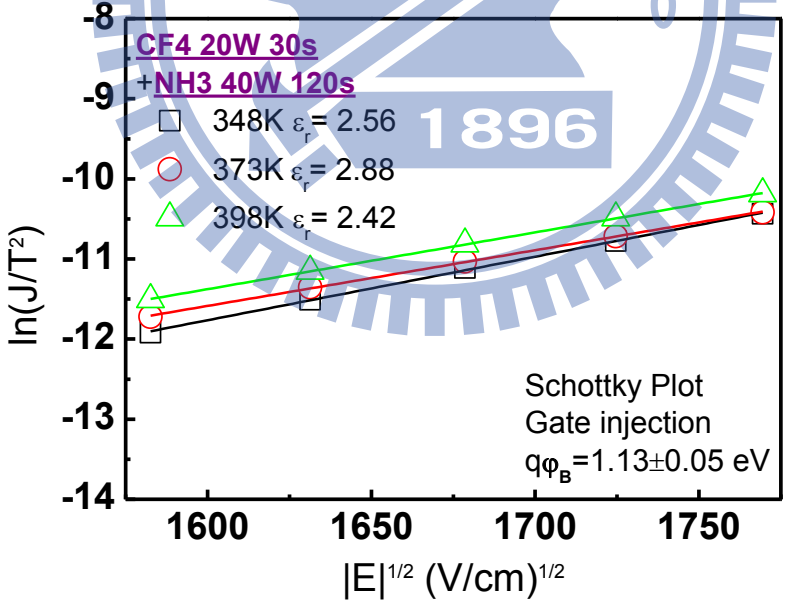

Fig. 2-49 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 30 sec + NH_3 120 sec at different temperatures (348K, 373K, and 398K).

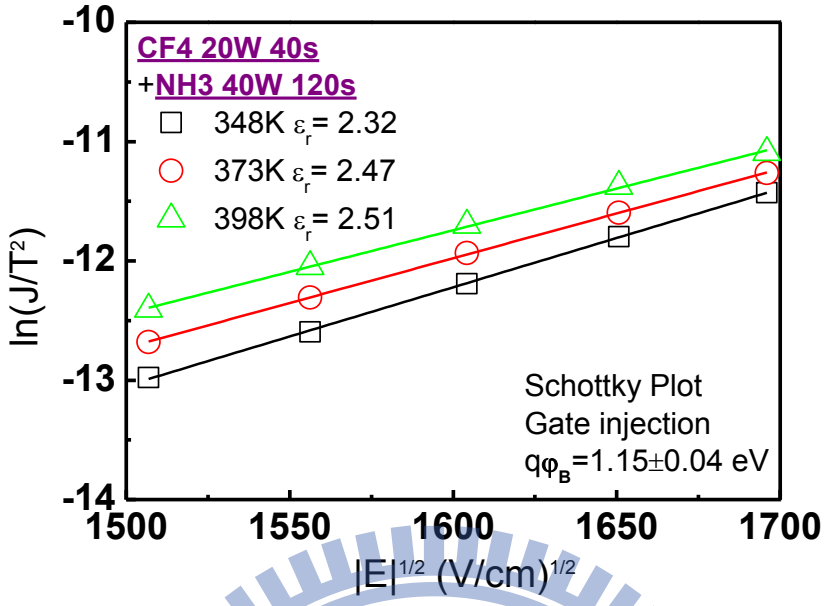

Fig. 2-50 Schottky emission plots, $\ln(J/T^2)$ versus $E^{1/2}$, for the HfO_2 thin film with CF_4 40 sec + NH_3 120 sec at different temperatures (348K, 373K, and 398K).

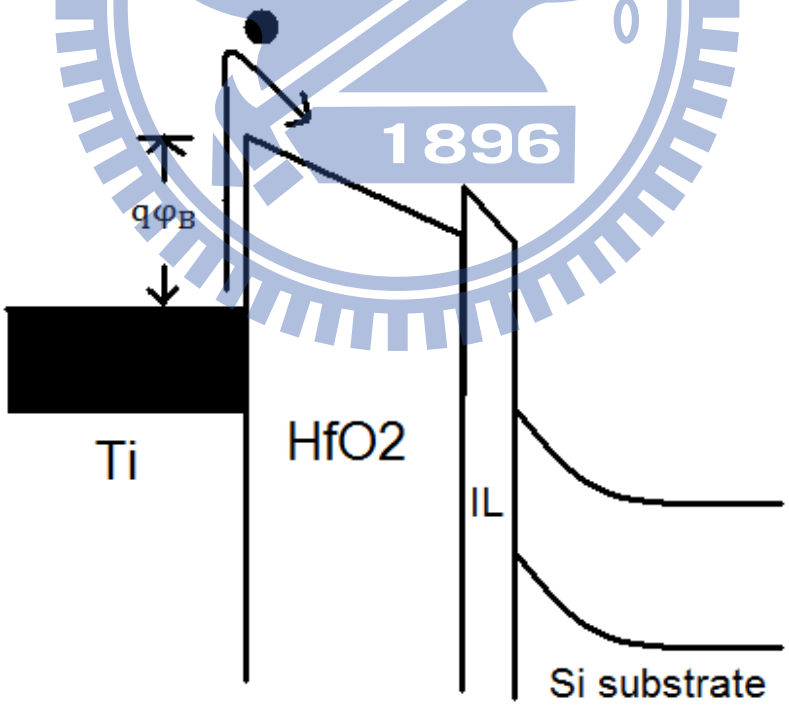

Fig. 2-51 The band diagram of Al/Ti/HfO2/Si MIS capacitors for the Schottky emission under gate injection. qφB is the Schottky barrier height.

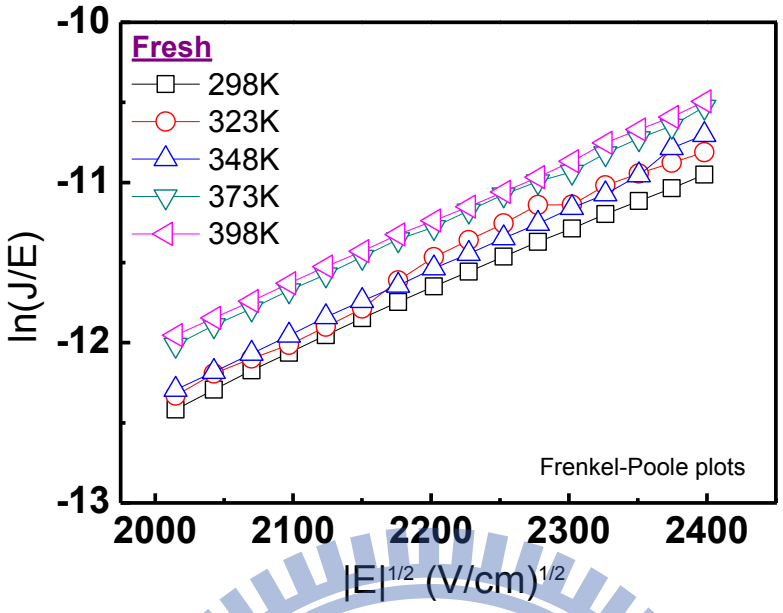

Fig. 2-52 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with no treatment at different temperatures (298 - 398 K).

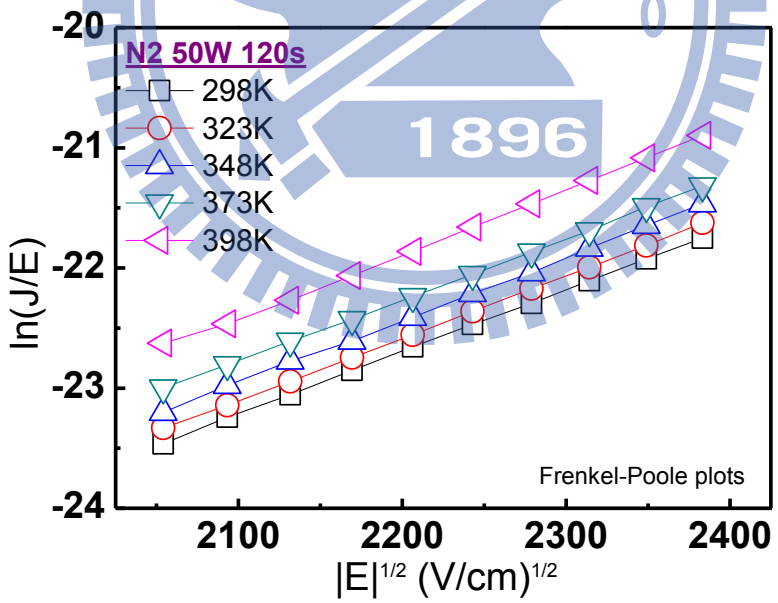

Fig. 2-53 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with N_2 120 sec at different temperatures (298 - 398 K).

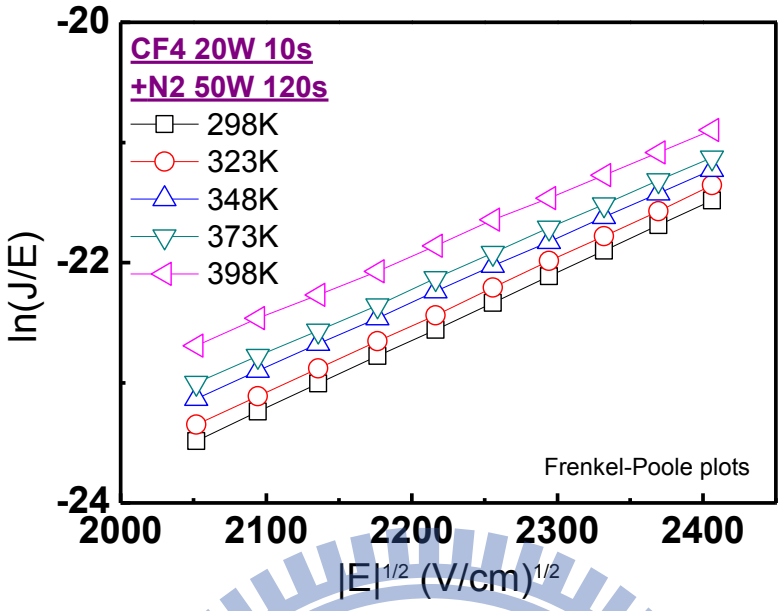

Fig. 2-54 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 10 sec + N_2 120 sec at different temperatures (298 - 398 K).

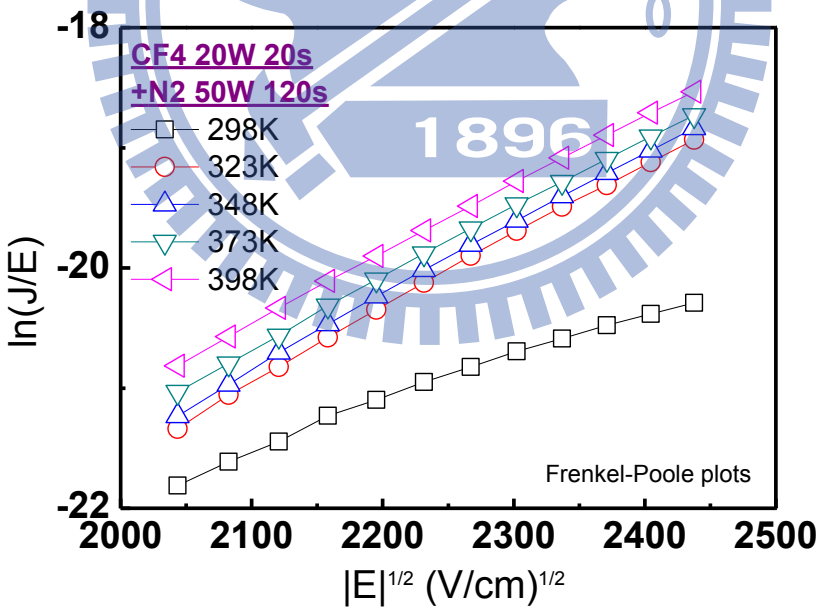

Fig. 2-55 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 20 sec + N_2 120 sec at different temperatures (298 - 398 K).

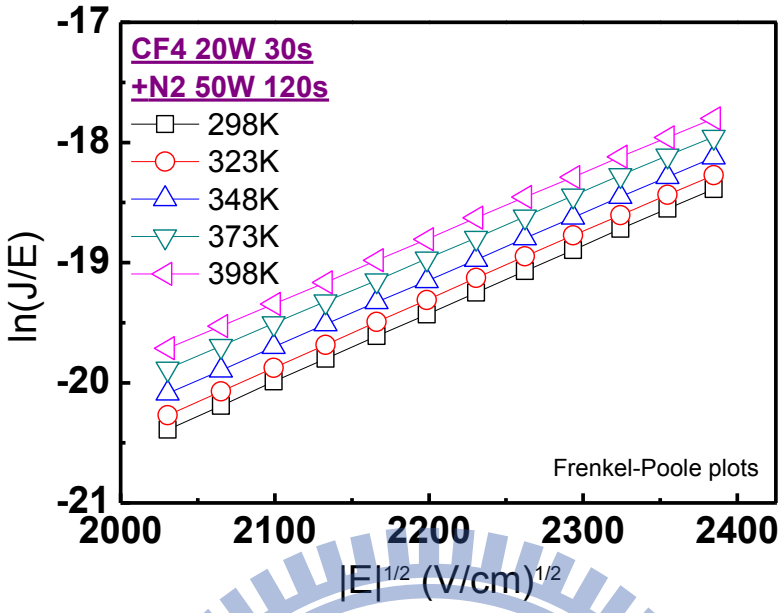

Fig. 2-56 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 30 sec + N_2 120 sec at different temperatures (298 - 398 K).

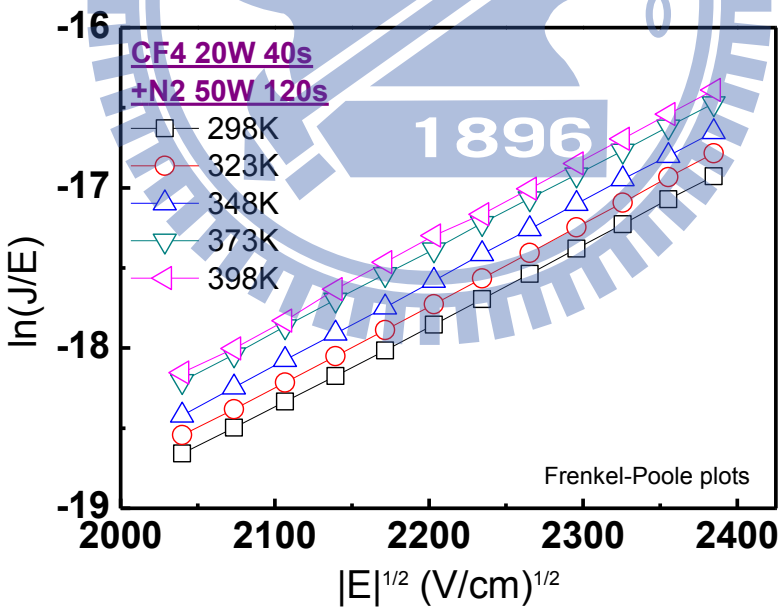

Fig. 2-57 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 40 sec + N_2 120 sec at different temperatures (298 - 398 K).

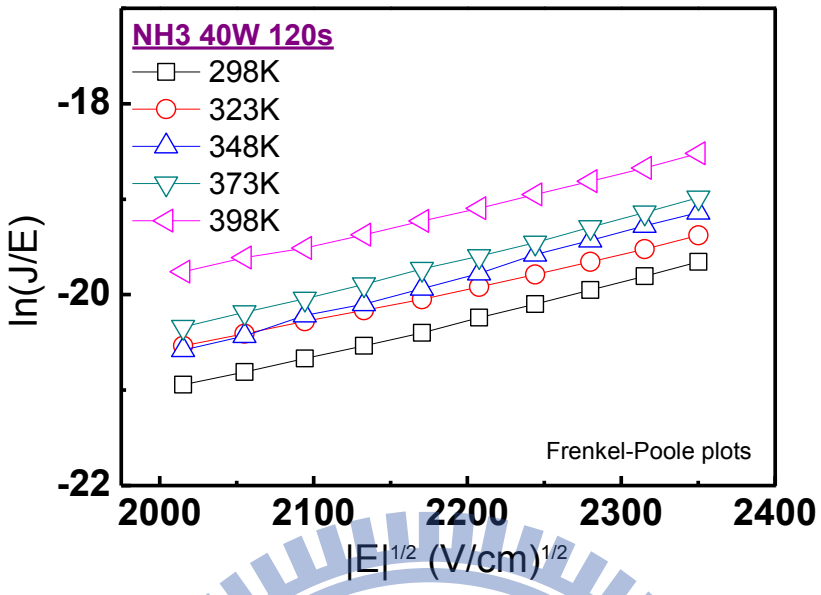

Fig. 2-58 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with NH_3 120 sec at different temperatures (298 - 398 K).

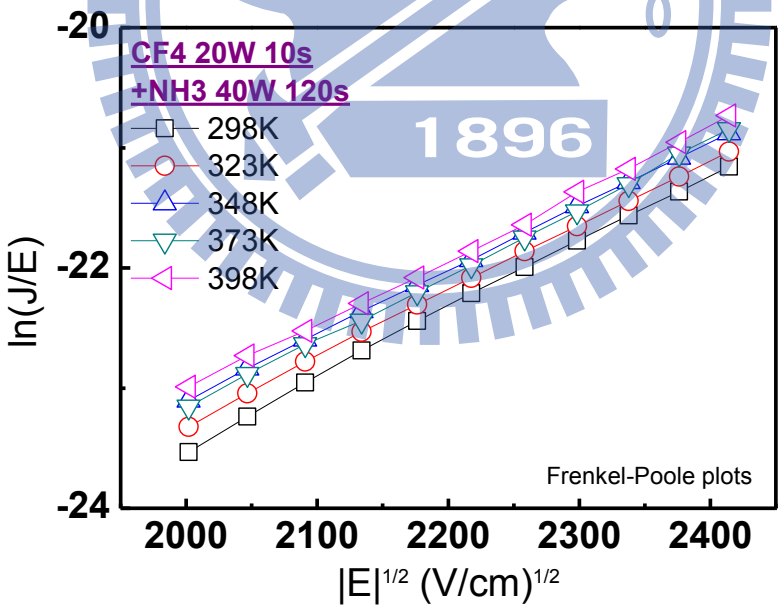

Fig. 2-59 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 10 sec + NH_3 120 sec at different temperatures (298 - 398 K).

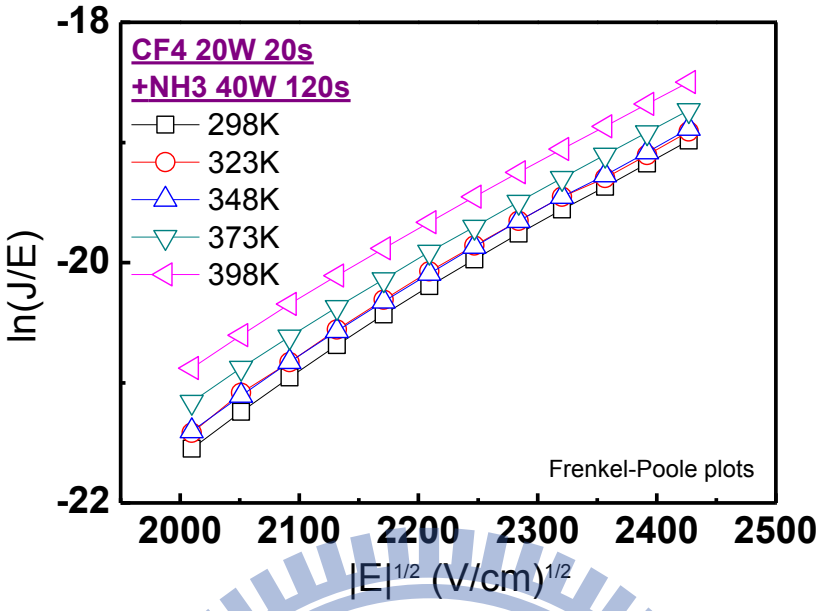

Fig. 2-60 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 20 sec + NH_3 120 sec at different temperatures (298 - 398 K).

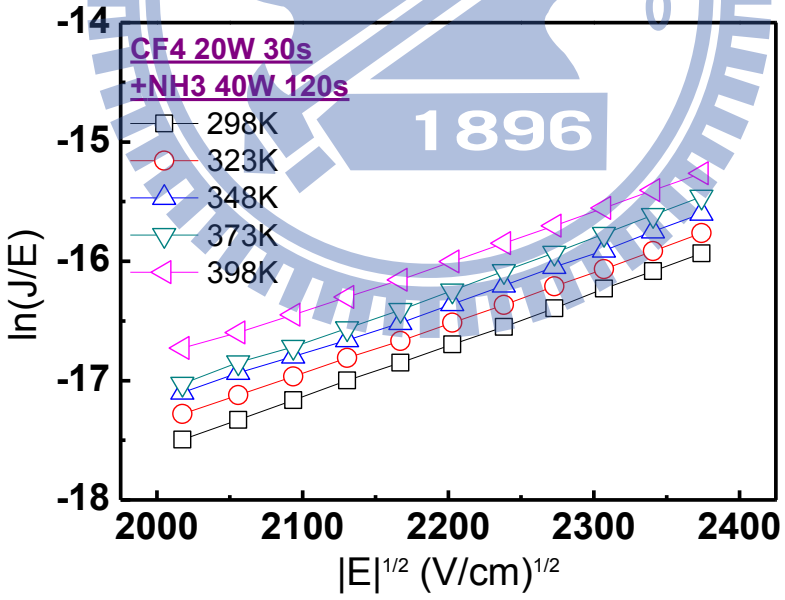

Fig. 2-61 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 30 sec + NH_3 120 sec at different temperatures (298 - 398 K).

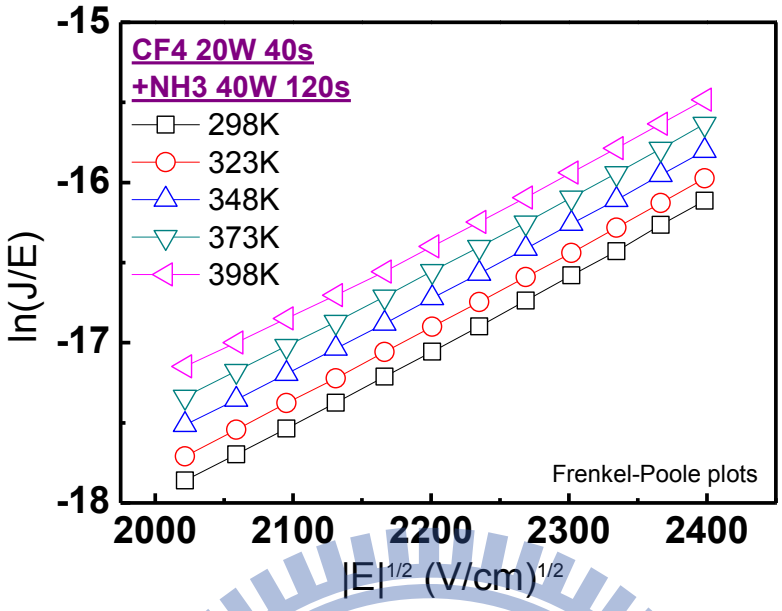

Fig. 2-62 Frenkel-Poole emission plots, ln(J/E) versus $E^{1/2}$, for the HfO_2 thin film with CF_4 40 sec + NH_3 120 sec at different temperatures (298 - 398 K).

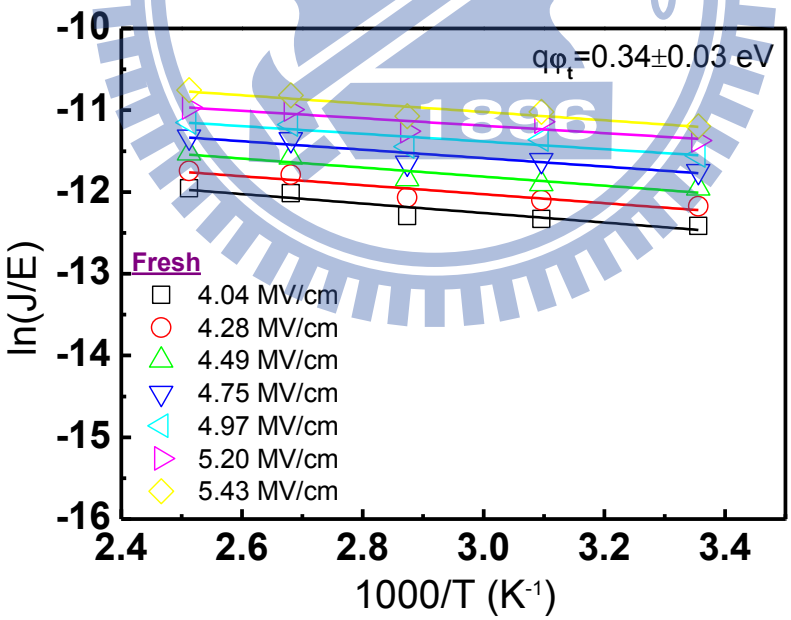

Fig. 2-63 Plots of $\ln(J_{FP}/E)$ versus 1/T at various electric fields for Fresh sample. qφt is the trap energy level in HfO_2.

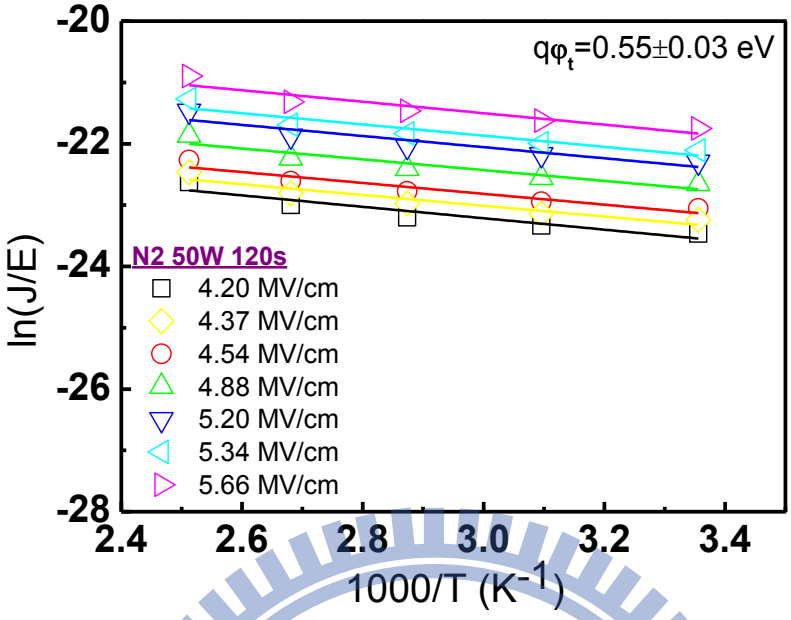

Fig. 2-64 Plots of ln(J_{FP}/E) versus 1/T at various electric fields for the sample treated in N_2 120 sec. qφt is the trap energy level in HfO_2.

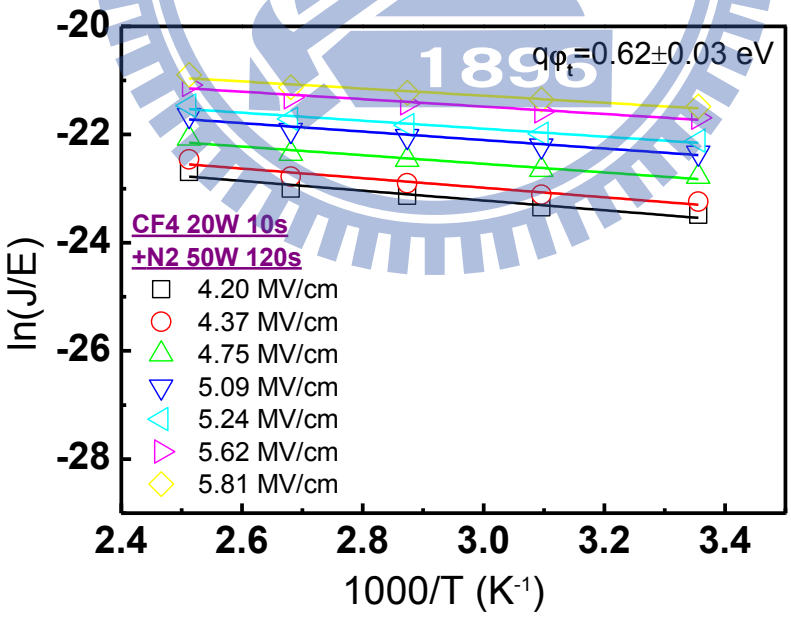

Fig. 2-65 Plots of ln(J_{FP}/E) versus 1/T at various electric fields for the sample treated in CF_4 10 sec + N_2 120 sec. qφt is the trap energy level in HfO_2.

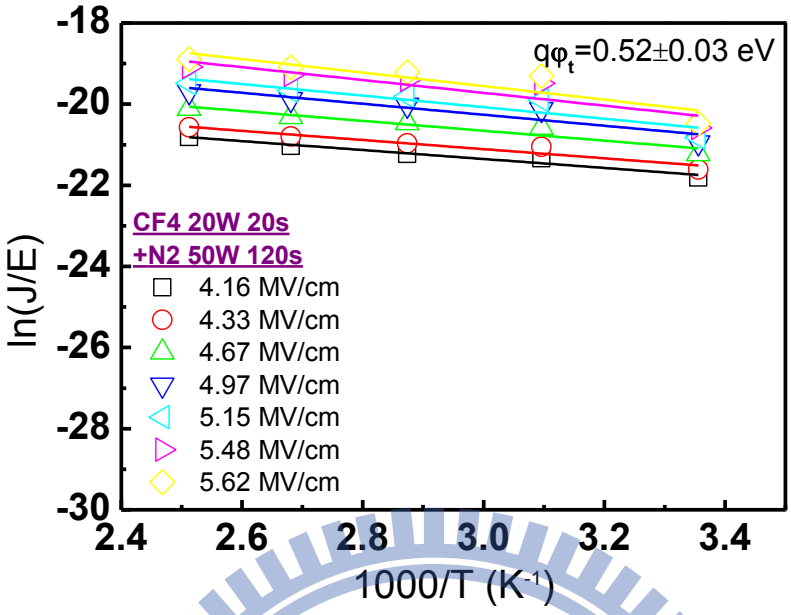

Fig. 2-66 Plots of $\ln(J_{FP}/E)$ versus 1/T at various electric fields for the sample treated in CF_4 20 sec + N_2 120 sec. qφt is the trap energy level in HfO_2.

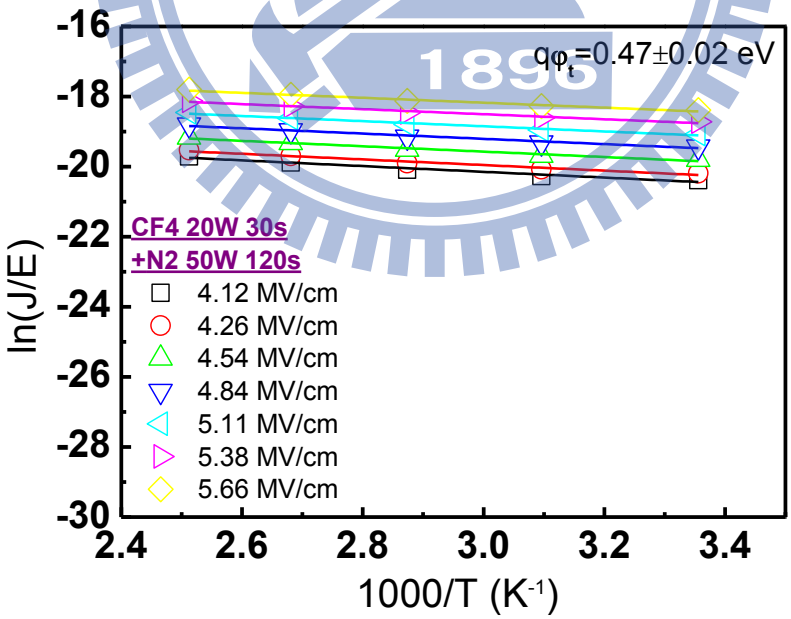

Fig. 2-67 Plots of $\ln(J_{FP}/E)$ versus 1/T at various electric fields for the sample treated in CF_4 30 sec + N_2 120 sec. qφt is the trap energy level in HfO_2.

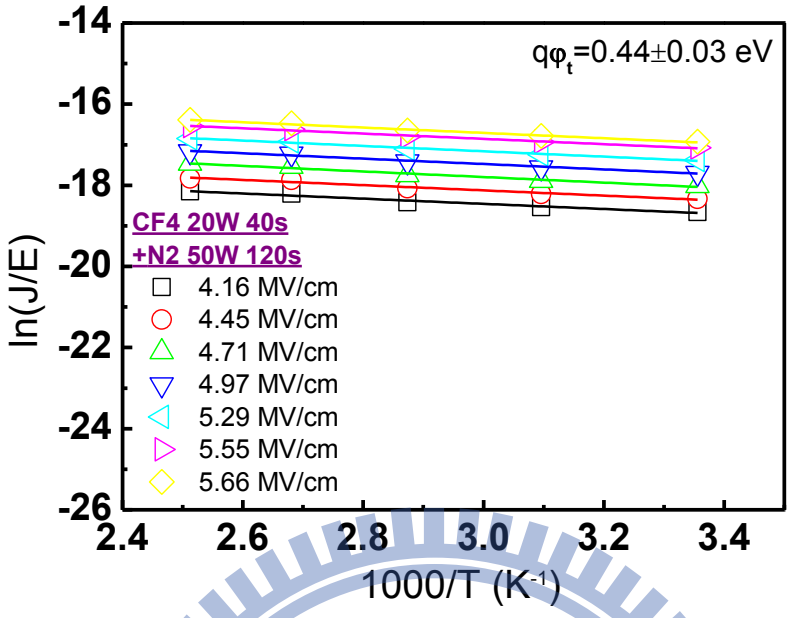

Fig. 2-68 Plots of $\ln(J_{FP}/E)$ versus 1/T at various electric fields for the sample treated in CF_4 40 sec + N_2 120 sec. qφt is the trap energy level in HfO_2.

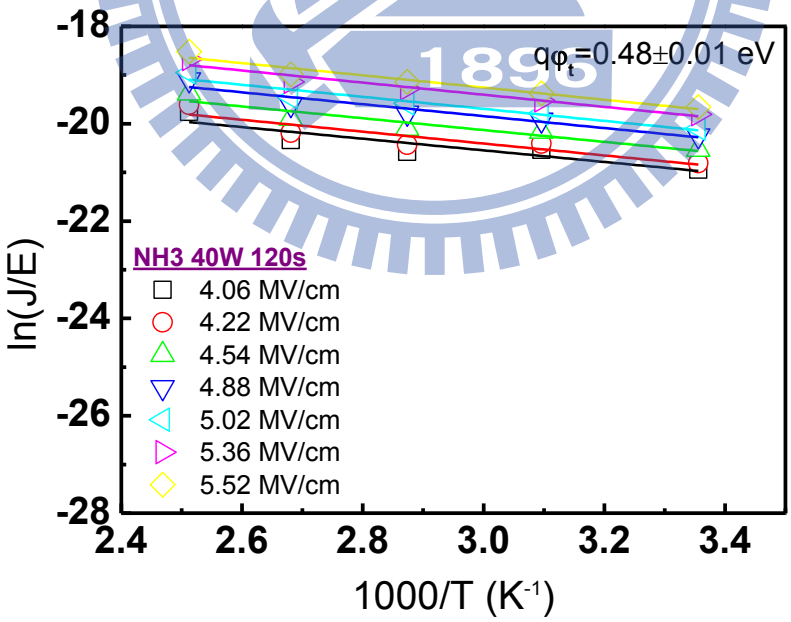

Fig. 2-69 Plots of $\ln(J_{FP}/E)$ versus 1/T at various electric fields for the sample treated in NH_3 120 sec. qφt is the trap energy level in HfO_2.

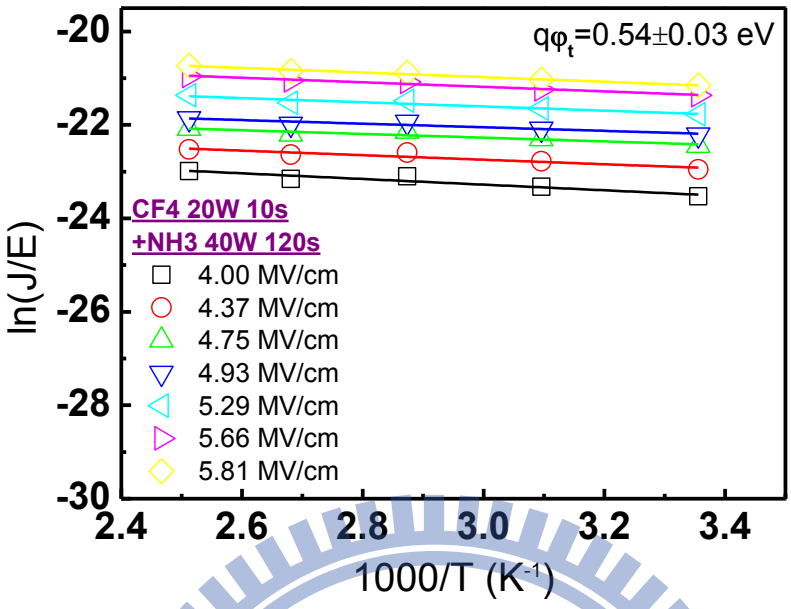

Fig. 2-70 Plots of ln(J_{FP}/E) versus 1/T at various electric fields for the sample treated in CF_4 10 sec + NH_3 120 sec. qφt is the trap energy level in HfO_2.

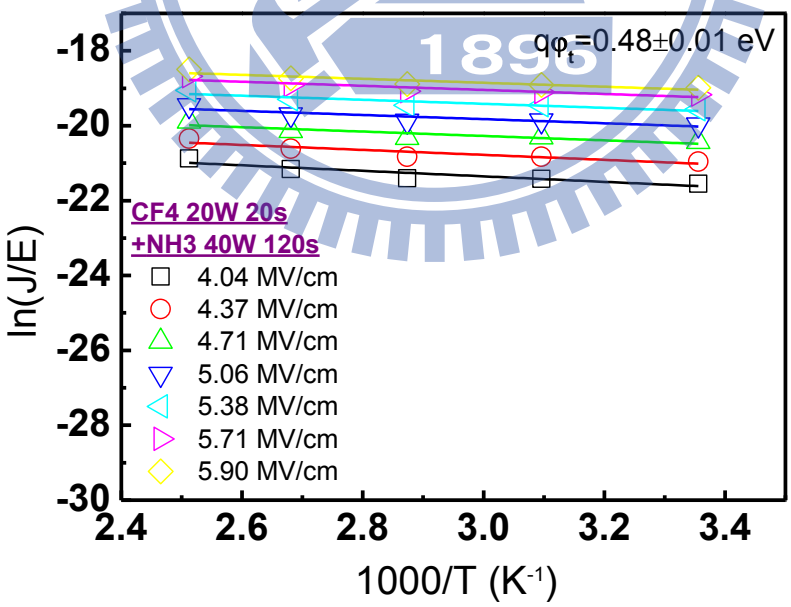

Fig. 2-71 Plots of ln(J_{FP}/E) versus 1/T at various electric fields for the sample treated in CF_4 20 sec + NH_3 120 sec. qφt is the trap energy level in HfO_2.

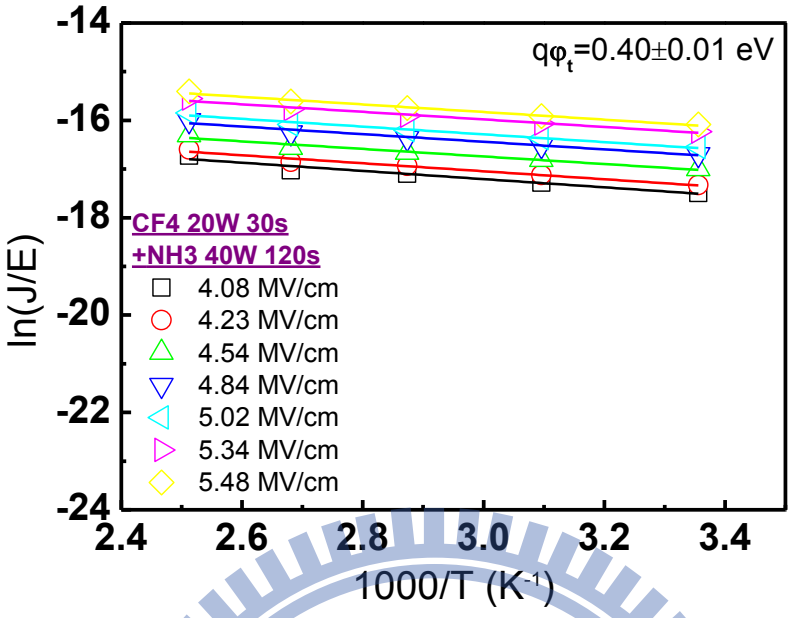

Fig. 2-72 Plots of ln(J_{FP}/E) versus 1/T at various electric fields for the sample treated in CF_4 30 sec + NH_3 120 sec. qφt is the trap energy level in HfO_2.

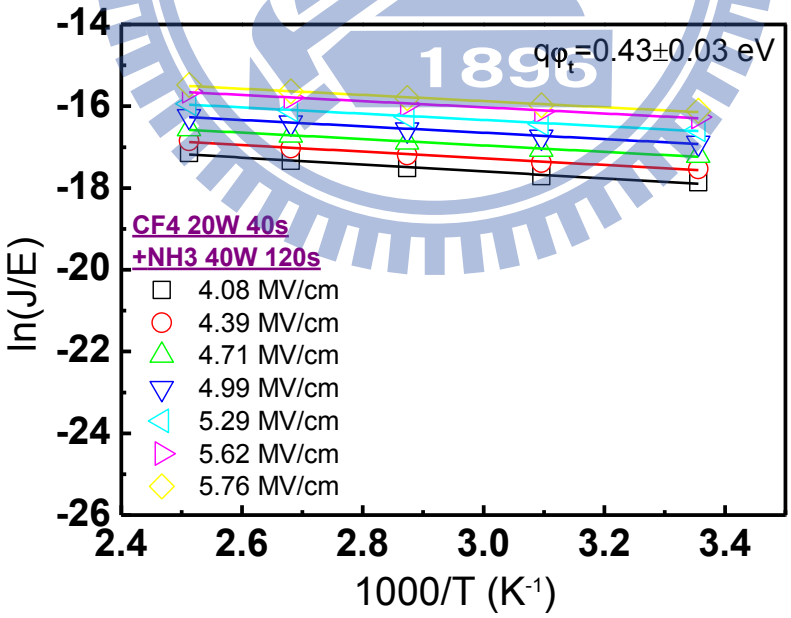

Fig. 2-73 Plots of ln(J_{FP}/E) versus 1/T at various electric fields for the sample treated in CF_4 40 sec + NH_3 120 sec. qφt is the trap energy level in HfO_2.

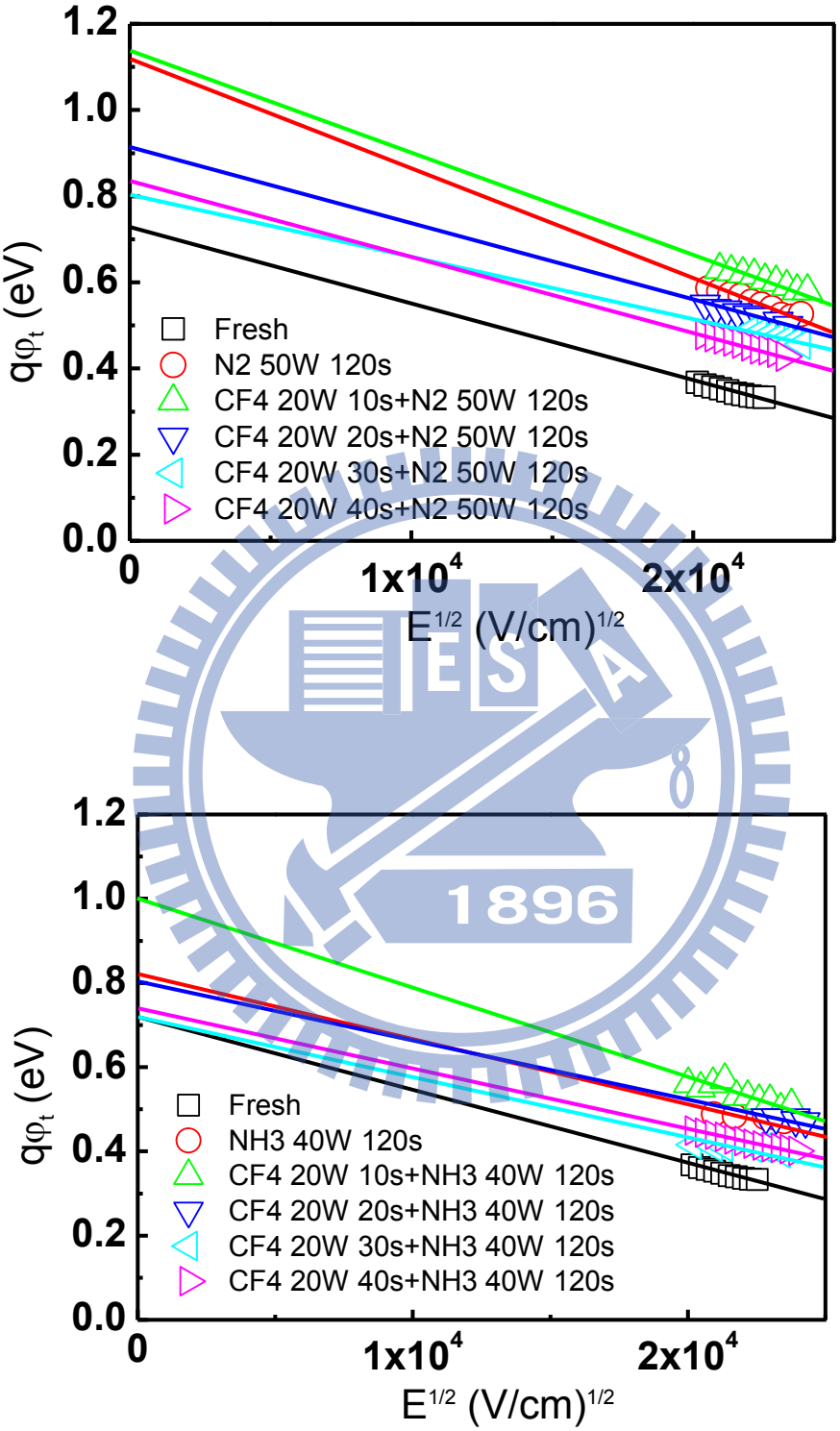

Fig. 2-74 Trapping energy levels extracted from F-P fitting for the samples with dual plasma treatment (a) CF_4 plasma and N_2 plasma (b) CF_4 plasma and NH_3 plasma.

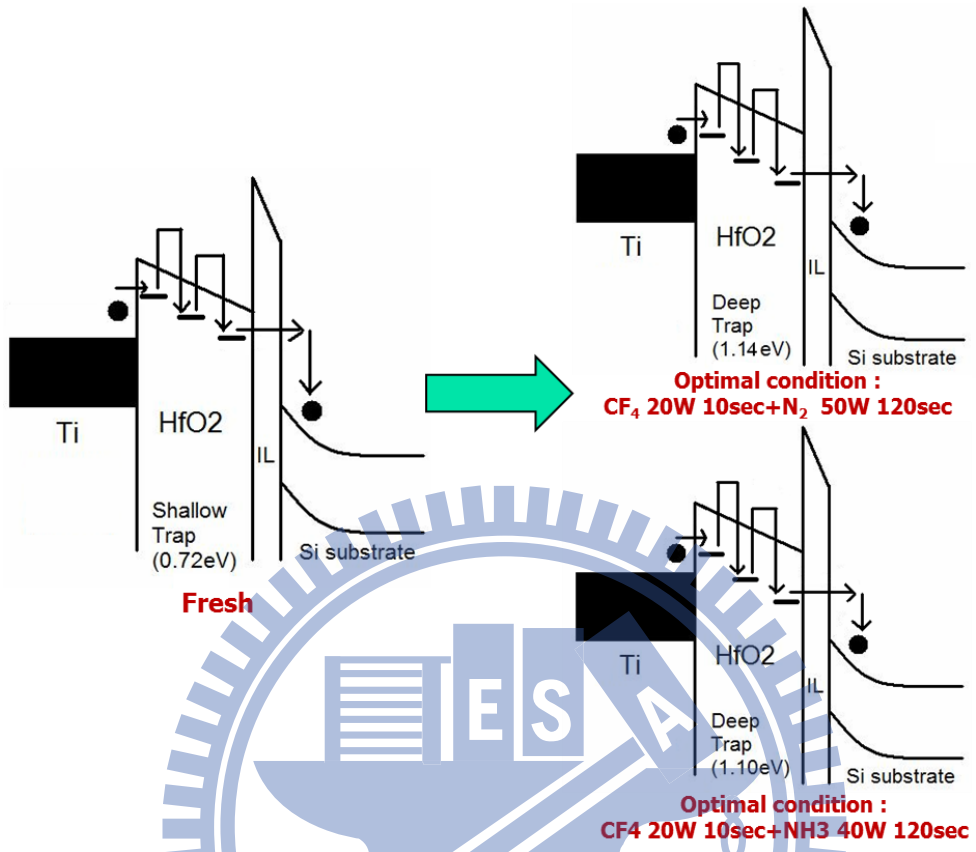

Fig. 2-75 Schematic of the band diagram of Al/Ti/HfO2/Si MIS capacitors before and after dual plasma treatment for the Frenkel Poole emission under gate injection.

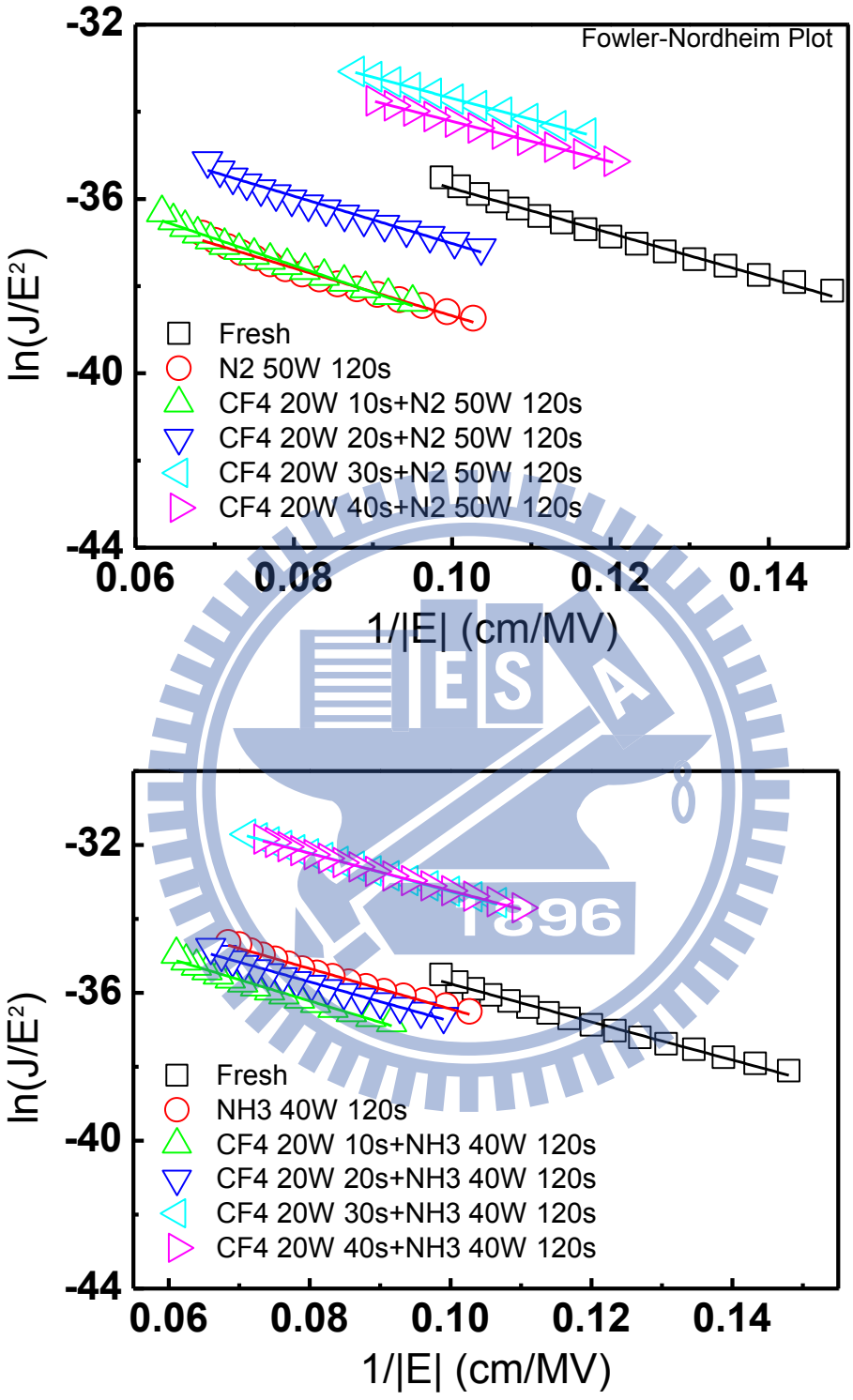

Fig. 2-76 F-N tunneling characteristic, $\ln(J/E^2)$ vs. 1/E, for the samples with dual plasma treatment (a) CF_4 plasma and N_2 plasma (b) CF_4 plasma and NH_3 plasma

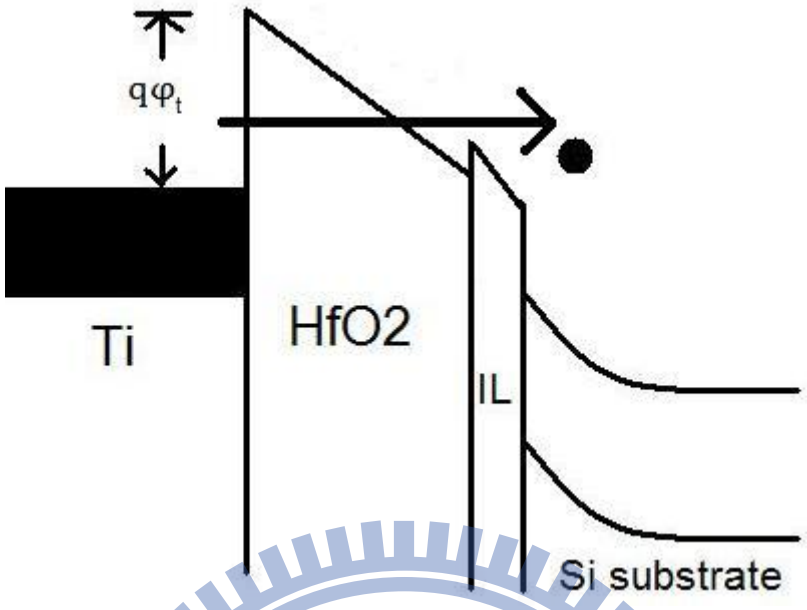

Fig. 2-77 The band diagram of Al/Ti/HfO2/Si MIS capacitors for Fowler-Nordheim tunneling under gate injection. qφt is the FN potential barrier height.

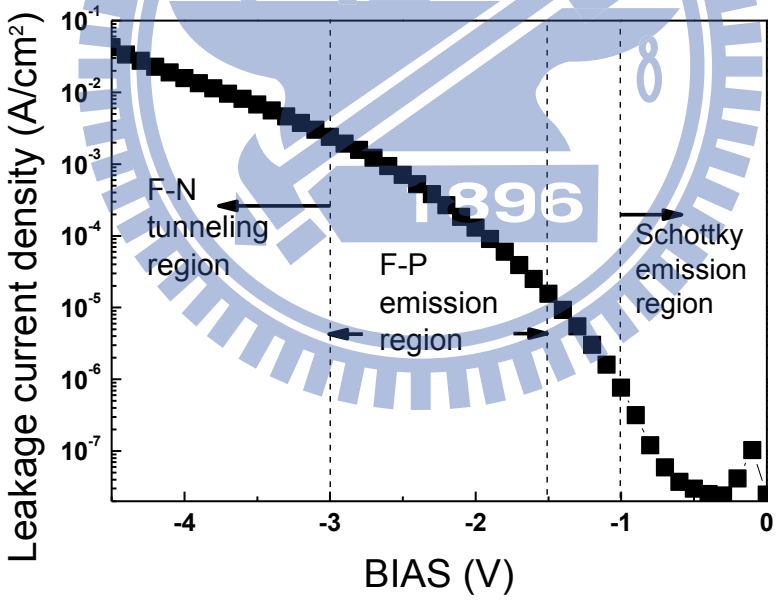

Fig. 2-78 The summary of the three current conduction mechanisms in different ranges of applied gate voltage.

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Chapter 3

Improvement on Interface Quality and Reliability Properties of $HfAlO_x$ MIS Capacitor with Dual Plasma Treatment

3.1 Introduction

For increasing the speed and pack density of integrated circuits, the physical thickness of the gate oxide becomes thinner as the dimension of complementary metal-oxide-semiconductor (CMOS) structure is continue scaling down. However, gate leakage current due to direct tunneling of electron through gate dielectric becomes too high when SiO_2 is too thin. Excessive off-state leakage current would lead to intolerable power consumption and over heat of the devices. In order to solve these issues, replacing conventional SiO_2 to a higher dielectric constant (high-k) dielectric layer can has higher physical thickness and maintains relatively low equivalent oxide thickness (EOT) [1]. In this decade, high-k materials have been vastly investigated, including HfO_2, ZrO_2, TiO_2, La_2O_3, Ta_2O_5, Al_2O_3, and $SrTiO_3$ [2-4]. Because of high dielectric constant (k ~ 25), relatively large band gap (Eg ~ 5.7 eV), large conduction band offset with Si (~1.5 eV), and stable contact with Si [5], HfO_2 becomes the most popular candidate dielectric. However, the crystallization temperature of HfO_2 is quite low, which will induce large leakage current and lateral

non-uniformity associated with grain boundaries after post thermal processes. It has been reported that adding Al into HfO_2 to form Hf-aluminates could increase the crystallization temperature [6]. When $HfAlO_x$ film is grown on Si substrate, the formation of interfacial layer (IL) at $HfAlO_x$/Si interface is inevitable. IL limits the reduction of the effective oxide thickness (EOT) due to low dielectric constant of IL [7-8].

Recently, it has been reported that nitrogen incorporated into high-k dielectric layer can increase thermal stability and increase dielectric constant [9-11]. Nitrogen atoms could eliminate the oxygen vacancy related states in HfO_2 band gap [12], which could suppress the leakage current about 3-4 order of magnitude [13-14]. On the other hand, fluorine incorporated in high-k gate stack has been used for many years [15-16]. The weak Si-O and Si-H bonds will be replaced by Si-F bonds at the interface, which could improve IL quality and dielectric reliability [17-18]. Moreover, CF_4 pre-treatment could suppress IL formation at interface [19].

In this work, Al/Ti/ $HfAlO_x$/Si MIS capacitor structure would be fabricated. We propose to combine CF_4 pre-treatment and N_2 post-treatment (denoted as dual plasma treatment) to examine interface quality and reliability properties of $HfAlO_x$ MIS capacitor.

3.2 Experimental

In this study, Al/Ti/$HfAlO_x$/Si gate stack were be fabricated. The silicon wafers were p-type (100) with the resistivity of 1-10 Ω-cm. A standard RCA clean was performed on all samples at first. $HfAlO_x$ layer was deposited by a MOCVD system

at 500 ^{o}C. The post-deposition annealing (PDA) or the post-nitridation annealing (PNA) was performed at 600 ^{o}C for 30 sec by a RTA system. A 40 nm Ti film was deposited by dual e-gun evaporation system, while a 400 nm Al film was thermally evaporated. Then, 5000 μm^2 of top gate electrodes were defined by lithography.

The experiment of plasma treatment in this study contained two parts. The first part was single nitrogen plasma post-treatment. After $HfAlO_x$ thin film deposition and PDA, samples were prepared in nitrogen plasma by PECVD system. The RF power was set at 50W and the times were in the range of 30-300 sec (30, 90, 150, and 300 sec). Then, post nitridation annealing (PNA) was performed in order to reduce plasma damage after N_2 plasma post-treatment.

The second part of this study was dual plasma treatment, which was the combination of CF_4 pre-treatment and nitrogen post-treatment in Al/Ti/$HfAlO_x$/Si MIS capacitors. After standard RCA cleaning, CF_4 pre-treatment was performed on the samples by PECVD. The RF power was set at 20W and the exposure times were in the range of 10-40 sec, 10 sec per step (10, 20, 30, and 40 sec). After CF_4 pre-treatment, $HfAlO_x$ layer deposition and PDA were performed. Then nitrogen post-treatment whose best condition was obtained from the first experiment earlier was used on the samples. Finally, MIS capacitors were formed after PNA and gate electrode formation. The process flow of two experiments is schematically shown in Fig. 3-1. The capacitance-voltage (C-V) characteristics were measured by C-V measurement (HP 4284) and the current-voltage (I-V) characteristics of were measured by a semiconductor parameter analyzer (HP 4156C).

3.3 Electrical characteristics of single plasma treatment

3.3.1 C-V and J-V Characteristics

Fig. 3-2 presents the C-V characteristics of the $HfAlO_x$ thin films with N_2 post-treatment for different process durations. The measurement frequency was set as 50 kHz. The capacitors treated in N_2 plasma for 90 sec show larger capacitance than other samples. Nitrogen incorporated into the dielectric layer could enhance the ionic polarization as well as the dielectric constant; as a result, the capacitance could be increased [14]. Besides, the capacitance of the samples treated for 150 sec and 300 sec is degraded due to plasma damage. Fig. 3-3 shows the I-V characteristics of the $HfAlO_x$ thin films with N_2 post-treatment for different process durations. It can be observed that the gate leakage current is restrained for the sample with N_2 plasma treatment for 90 sec, owing to defect passivation. Likewise, when the nitridation process time is longer than 90 sec, the current density becomes higher because of plasma damage.

In short, it can be seen that the best condition of the N_2 plasma nitridation is as following: N_2 post-treatment for 90 sec with the RF power 50W. Similarly, it also can be found that the best condition of the NH_3 plasma nitridation is as following: NH_3 post-treatment for 90 sec with the RF power 40W, according to Fig. 3-4 and Fig. 3-5. In order to examine the effect of dual plasma treatment on HfAlOx thin films, the samples were treated in CF4 plasma pre-treatment for different durations and N_2 (NH_3) plasma post-treatment for 90 sec.

3.4 Electrical characteristics of dual plasma treatment

3.4.1 C-V and J-V characteristics

Fig. 3-6 shows the C-V characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec. It could be observed that sample treated by single N_2 plasma treatment for 90 sec displays higher capacitance density than fresh sample, which is owing to the enhancement of ionic polarization [14]. On the other hand, the sample treated by CF_4 pre-treatment for 10 sec (RF power = 20 W) and N_2 post-treatment for 90 sec (RF power = 50 W) has further improvement than the sample only treated by N_2 post-treatment. The capacitance density has 42.5 % higher than the fresh sample after dual plasma treatment. Furthermore, the sample treated by dual plasma (CF_4 plasma for 10 sec and N_2 plasma for 90 sec) exhibits much sharp of C-V curve; as a result, the interface quality has been apparently improved by dual plasma treatment. However, while the CF_4 pre-treatment time is longer than 10 sec, the capacitance density and the slope of C-V cure become worse because of CF_4 plasma damage at the $HfAlO_x$/Si interface.

Fig. 3-7 displays the J-V characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec. The gate leakage current density is suppressed by 3 orders of magnitude for the sample treated by dual plasma treatment (CF_4 plasma for 10 sec and N_2 plasma for 90 sec), compared to the fresh sample. The suppress of the leakage current is ascribed to defect passivation by nitrogen atom and fluorine atom [12, 15] because the leakage path form defect states within $HfAlO_x$ band gap has been cut off. Similarly, the plasma damage become serious as the CF_4 pre-treatment time is longer than 10 sec; consequently, the gate leakage increased.

In Fig. 3-8 and Fig. 3-9, the C-V and the J-V characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 90 sec are presented. The basic electrical characteristics for dual plasma treatment on $HfAlO_x$ MIS capacitor are shown in Table 3-1 and Table 3-2.

3.4.2 Hysteresis

Fig. 3-10 displays the hysteresis characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec. Hysteresis characteristics was measured from negative to positive voltage (accumulation to inversion) and then swept back form positive to negative voltage (inversion to accumulation). The hysteresis phenomenon of the C-V curve could be explained by the inner-interface trapping model that the positive and negative carriers might be trapped at the inner interface [16]. The defect states are called slow trapping sites [20]; consequently, the C-V curve shift would be smaller as the number of defects becomes lower. The hysteresis phenomenon could be observed for all the samples. The shift of C-V curve for the fresh sample is 65.2 mV, whereas the C-V curve shift of the sample treated by N_2 plasma for 90 sec is 27.6 mV. Even through the single N_2 post-treatment could improve the hysteresis characteristic, dual plasma treatment (CF_4 pre-treatment for 10 sec and N_2 post-treatment for 90 sec) is observed that could further improve the hysteresis phenomenon. The hysteresis phenomenon of the sample treated by dual plasma is retrained to 10.1 mV, which is the smallest among all samples. In addition, it can be seen that there is a hump in the depletion region of C-V curve for the fresh sample, owing to higher D_{it} at the interface [21]. The hump could be greatly reduced for the sample treated by dual plasma treatment (CF_4 pre-treatment for 10 sec and N_2 post-treatment for 90 sec). The factor of improvement might be from the reduction of the interface states, therefore the interface quality could be enhanced by dual plasma

treatment. On the other hand, while CF_4 pre-treatment time is longer than 10 sec, the hump and hysteresis became worst because of plasma damage at the $HfAlO_x$/Si interface.

Fig. 3-11 displays the hysteresis characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 90 sec. Form the similar analysis, it could be observed that the smallest hysteresis characteristics (8.8 mV) and nearly no hump in the C-V curve for the sample treated in CF_4 pre-treatment for 10 sec and NH_3 post-treatment for 90 sec. The interface states can be great improved by dual plasma treatment. The data of the hysteresis for all the samples are also shown in Table 3-1 and Table 3-2.

3.4.3 Breakdown voltage

Fig. 3-12 presents the breakdown characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 (NH_3) plasma for 90 sec. Although the sample treated by single N_2 (NH_3) plasma shows lower gate leakage current than fresh sample, the leakage is suppressed mostly for the sample with dual plasma treatment (CF_4 pre-treatment for 10 sec and N_2 (NH_3) post-treatment for 90 sec). The reduction of gate leakage current is the result of defect passivation. Nitrogen and fluorine atoms could reduce the oxygen vacancy related states and interface states within $HfAlO_x$ band gap. Nevertheless, while CF_4 pre-treatment is longer than 10 sec, the non-ideal effect that gate leakage increased. The reason for this phenomenon might be attributed to plasma damage at the interface. These results consisted with the breakdown voltage behaviors and distribution, as shown in Fig. 3-13. It has been reported that the first breakdown happened in the low-k layer because the applied electric field would be largely distributed in the low-k region for high-k/low-k gate

stack [22]. In other words, interfacial layer (IL) represented the low-k layer and would cause the reliability problems. As shown in Fig. 3-13, the sample treated by dual plasma treatment (CF_4 pre-treatment for 10 sec and N_2 (NH_3) post-treatment for 90 sec) shows the largest breakdown voltage because of the great improvement on interface quality. In short, the best condition of dual plasma treatment is CF_4 pre-treatment in 10 sec with RF power 20W and N_2 (NH_3) post-treatment in 90 sec. The breakdown voltage of all the samples is illustrated in Table 3-1 and Table 3-2.

3.4.4 Frequency dispersion characteristics

The C-V characteristics of the $HfAlO_x$ thin films with CF_4 plasma for different process durations and N_2 plasma for 90 sec measured under different frequencies were compared in Fig. 3-14. The range of measurement frequency was set form 1 kHz to 100 kHz. It could be noticed that the strong frequency dispersion in the accumulation region and the hump in the depletion region in the C-V curve for the fresh sample. The effect of frequency dispersion is attributed to the response of charges to signal frequency [23]. Because some of the traps could follow the change of the applied gate voltage, the additional capacitance would be generated [23]. Compared to the fresh sample, the sample treated by N_2 plasma showed relatively smaller frequency dispersion and smaller hump. Besides, it could be observed that the sample with dual plasma treatment (CF_4 pre-treatment for 10 sec and N_2 post-treatment for 90 sec) shows nearly no dispersion in the accumulation region and nearly no hump in the depletion region, which is independent of frequency. The reason of the improvement could be ascribed to that dual plasma treatment could effectively improve the interface quality [23-26]. However, while CF_4 pre-treatment time is longer than 10 sec, the frequency dispersion and the hump became worst again because of plasma damage at the interface

Fig. 3-15 depicts the C-V characteristics of the $HfAlO_x$ thin films with CF_4 plasma for different process durations and NH_3 plasma for 90 sec measured under different frequencies. Similarly, the sample with dual plasma treatment (CF_4 pre-treatment for 10 sec and NH_3 post-treatment for 90 sec) shows nearly no dispersion in the accumulation region and nearly no hump in the depletion region, which is attributed to the improvement of the interface quality.

3.4.5 Constant voltage stress characteristics

The C-V curves before and after CVS testing of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec are shown in Fig. 3-16. The stress voltage was set as -3 V and the tress time was set in a range from 0 to 700 sec. It could be observed that all the C-V curves shift to left when stress time increase indicating that the generation of positive charges are trapped in the dielectric layer, which could be explained by Anode hole injection model [27]. The injected electrons traveled from the gate through the dielectric layer and arrived at the interface when constant negative bias stress, resulting in the de-passivation of $Si_3{\equiv}SiH$ centers and creating the $Si_3{\equiv}Si$-dangling bonds at the interface (so called P_{b0} centers) [28]. The released hydrogen transported through the dielectric field by electric field and trapped in the dielectric; as a consequence, it may create the positively charged centers [29]. On the other hand, the C-V curve of fresh sample exhibited hump after constant voltage stress, owing to the creation of interface defects. Compared to other samples, it is worth mentioning that the C-V curves had smaller V_{fb} shift and less distortion for samples with CF_4 pre-treatment for 10sec and N_2 post-treatment for 90sec because less interface trap charges generated at the $HfAlO_x$/Si interface. On the other hand, the similar phenomenon also could be observed for the sample treated in CF_4 pre-treatment and NH_3 post-treatment for

90sec, which is shown in Fig. 3-17.

3.5 Current conduction of Al/Ti/HfO_2/Si MIS capacitors

In order to understand the current conduction mechanism, three kinds of conduction mechanisms were be analyzed, including Schottky emission (S.E.), Frenkel-Poole (F-P) emission, and Fowler-Nordheim (F-N) tunneling. The leakage current was measured from 298 K to 398 K (25 K per step) because to analyze S.E. and F-P emission needs the time dependence of the leakage current.

3.5.1 Schottky emission (S.E.)

The standard Schottky emission could be expressed as

$$J_{SE} = A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right], \qquad A^* = 120\frac{m^*}{m_0}\left(\frac{A}{cm^2K^2}\right), \tag{1}$$

where J_{SE} is the current density, A^* is the effective Richardson constant, E is the effective electric field, T is the absolute temperature, q is the electron charge, $q\phi_B$ is the Schottky barrier height, k is Boltzmann's constant, ε_0 is the permittivity of free space, ε_r is the dynamic dielectric constant, m^* is the electron effective mass in HfO_2, m_0 is the free electron mass. The electron effective mass is 0.1 m_0.

A plot of $\ln(J/T^2)$ versus $E^{1/2}$ should be a straight line, as shown in Fig. 3-18. Eq. (2) expressed the intercept of the Schottky emission plot with the vertical axis. The barrier height could be extracted from Eq. (2). The Schottky barrier height of all the samples is shown in Table 3-3. It is clear that the $HfAlO_x$ samples had larger barrier height than other samples after CF_4 pre-treatment for 10 sec and nitrogen

post-treatment for 90 sec.

$$Intercept = \ln\left(A^*\right) - \frac{q\phi_B}{kT}, \qquad A^* = 120\frac{m^*}{m_0}\ \left(\frac{A}{cm^2K^2}\right). \tag{2}$$

3.5.2 Frenkel-Poole (F-P) emission

When gate under negative bias, electrons will inject from gate into HfO_2 dielectric layer and will be trapped into shallow trap levels. Thereafter, the electrons transported through the dielectric layer by hopping between these trap levels, leading to leakage current, called Frenkel-Poole (F-P) emission. The standard F-P emission could be expressed as [35]

$$J_{FP} = C_t E \exp\left[\frac{-q\left(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right], \tag{3}$$

where J_{FP} is the current density, E is effective electric field, C_t is a constant proportional to the density of bulk oxide traps, $q\phi_t$ is the trap energy in $HfAlO_x$. The trap energy in dielectric layer could be extracted form good F-P fitting, as shown in Fig. 3-19. The extracted trap levels are illustrated in Table 3-4.

The extracted trap levels for the sample with and without N_2 post-treatment were 1.27 eV and 0.92 eV, respectively. In contrast, the trap level for the sample treated by CF_4 pre-treatment for 10 sec and N_2 post-treatment for 90 sec was 1.49 eV. The deeper trap level means that most of shallow trap levels in HfO_2 thin film can be eliminated by using dual plasma treatment. The elimination of shallow trap levels resulted in the reduction of F-P conduction current. Similarly, the sample treated in CF_4 pre-treatment for 10 sec and NH_3 post-treatment for 90 sec also exhibited larger trap levels than other samples. In short, dual plasma treatment could eliminate the

shallow trap levels and greatly reduce the gate leakage current.

3.5.2 Fowler-Nordheim (F-N) Tunneling

In higher electric field, the Fowler-Nordheim (F-N) tunneling dominated the conduction mechanism. The standard F-P emission could be expressed as

$$J_{FN} = AE^2 \exp\left[\frac{-8\pi\sqrt{2m^*}(q\phi_f)^{3/2}}{3qhE}\right], \quad (4)$$

where J_{FN} is the current density, h is the Plunk's constant, $q\phi_f$ is the potential barrier height, m^* is the electron effective mass in HfO_2, and the other notations were as same as mentioned before. The electron effective mass here is 0.1 m_0. If the leakage current is dominated by the F-N mechanism, a plot of $\ln(J/E^2)$ versus 1/E should be linear. Linear characteristic could be observed at high electric field, as shown in Fig. 3-20. The slope of each curve in Fig. 3-20 and Eq. (5) could obtain the F-N barrier height, which were listed in Table 3-5.

$$\phi_f = \left(\frac{9h^2}{128\pi^2 m^* q}\right) * (slope)^{2/3}. \quad (5)$$

Table 3-5 listed the F-N barrier height of the samples with no treatment, single plasma treatment, and dual plasma treatment. It could be observed that samples treated in CF_4 pre-treatment for 10 sec and nitrogen post-treatment for 90sec had larger value than other samples. The injection of electrons from the gate entered the conduction band of $HfAlO_x$ by tunneling through a triangular potential barrier. The injected electrons interacted with lattice or transferred its energy at anode, which resulted in the degradation of the dielectric layer. As a result, the sample with proper dual plasma treatment had bigger F-N barrier height and better reliability properties.

3.6 Conclusion

The interface quality and reliability properties of $HfAlO_x$ gate dielectric with dual plasma have been verified. Based on above results, the electrical characteristics including C-V, I-V, hysteresis, frequency dispersion, and CVS characteristics of HfAlOx gate dielectrics could be great improved by dual plasma treatment. According to our study, the best condition is CF_4 pre-treatment for 10 sec and N_2 (NH_3) post-treatment for 90 sec time. According to the current conduction analysis, the dominant current conduction mechanism was Schottky emission type in the region of low to medium electric fields; Frenkel-Poole (F-P) emission operated in the region of medium to high fields; Fowler-Nordheim (F-N) tunneling was dominant at high fields. In conclusion, dual plasma treatment could improve interface quality and enhance reliability properties of $HfAlO_x$ thin films.

Table 3-1 illustrates the basic electrical characteristics of the $HfAlO_x$ sample for dual plasma treatment (CF_4 pre-treatment and N_2 post-treatment).

Samples	**Fresh**	**N_2(120s)**	**CF_4(10s)+ N_2(120s)**	**CF_4(20s)+ N_2(120s)**	**CF_4(30s)+ N_2(120s)**	**CF_4(40s)+ N_2(120s)**
C(μF/cm^2)	0.86	1.16	1.23	1.05	0.88	0.84
Improve percentage (%)		34.41	42.53	21.67	3.01	-2.78
CET (nm)	3.68	2.97	2.82	3.30	3.88	4.12
J(A/cm^2)	9.47E-3	3.57E-4	5.96E-6	3.92E-5	4.10E-4	5.15E-4
Hysteresis (mV)	65.2	27.6	10.1	46.4	79	101.5
-V_{bd}	~4.3	~4.9	~6.6	~5.8	~5.1	~4.6

Table 3-2 illustrates the basic electrical characteristics of the $HfAlO_x$ sample for dual plasma treatment (CF_4 pre-treatment and NH_3 post-treatment).

Samples	**Fresh**	**NH_3(120s)**	**CF_4(10s)+ NH_3 (120s)**	**CF_4(20s)+ NH_3 (120s)**	**CF_4(30s)+ NH_3 (120s)**	**CF_4(40s)+ NH_3 (120s)**
C(μF/cm^2)	0.94	1.2	1.3	0.97	0.81	0.61
Improve percentage (%)		27.93	37.53	3.2	-13.97	-34.65
CET (nm)	3.68	2.88	2.68	3.57	4.28	5.63
J(A/cm^2)	9.47E-3	2.39E-4	1.1E-5	1.23E-5	3.1E-4	3.48E-4
Hysteresis (mV)	52.7	33.8	8.8	50.1	90.3	146.7
-V_{bd}	~6	~6.9	~8.1	~7.6	~7.1	~6.5

Table 3-3 Schottky Barrier Height Extracted for The $HfAlO_x$ Samples with No Treatment, Single Plasma Treatment, and Dual Plasma Treatment.

Barrier height	**Fresh**	**N_2(90s)**	**CF_4(10s)+ N_2(90s)**	**CF_4(20s)+ N_2(90s)**
$q\phi_B(eV)$	1.07±0.06	1.21±0.04	1.29±0.04	1.18±0.05
Barrier height	**Fresh**	**NH_3(90s)**	**CF_4(10s)+ NH_3 (90s)**	**CF_4(20s)+ NH_3 (90s)**
$q\phi_B(eV)$	1.07±0.06	1.22±0.07	1.33±0.06	1.19±0.03

Table 3-4 F-P Trapping Level Extracted for The $HfAlO_x$ Samples with No Treatment, Single Plasma Treatment, and Dual Plasma Treatment.

Barrier height	**Fresh**	**N_2(90s)**	**CF_4(10s)+ N_2(90s)**	**CF_4(20s)+ N_2(90s)**
$q\phi_t(eV)$	0.92	1.27	1.49	1.16
Barrier height	**Fresh**	**NH_3(90s)**	**CF_4(10s)+ NH_3 (90s)**	**CF_4(20s)+ NH_3 (90s)**
$q\phi_t(eV)$	0.92	1.18	1.46	1.33

Table 3-5 F-N Barrier Height Extracted for The $HfAlO_x$ Samples with No Treatment, Single Plasma Treatment, and Dual Plasma Treatment

Barrier height	**Fresh**	**N_2(90s)**	**CF_4(10s)+ N_2(90s)**	**CF_4(20s)+ N_2(90s)**	**CF_4(30s)+ N_2(90s)**	**CF_4(40s)+ N_2(90s)**
slope	5.18E9	8.03E9	1.42E10	1.02E10	1.00E10	7.11E9
$q\phi_f(eV)$	1.8	2.39	3.47	2.81	2.77	2.21
Barrier height	**Fresh**	**NH_3(90s)**	**CF_4(10s)+ NH_3 (90s)**	**CF_4(20s)+ NH_3 (90s)**	**CF_4(30s)+ NH_3 (90s)**	**CF_4(40s)+ NH_3 (90s)**
slope	5.18E9	6.28E9	1.15E10	8.65E9	5.04E9	2.68E9
$q\phi_f(eV)$	1.8	2.04	3.05	2.52	1.76	1.16

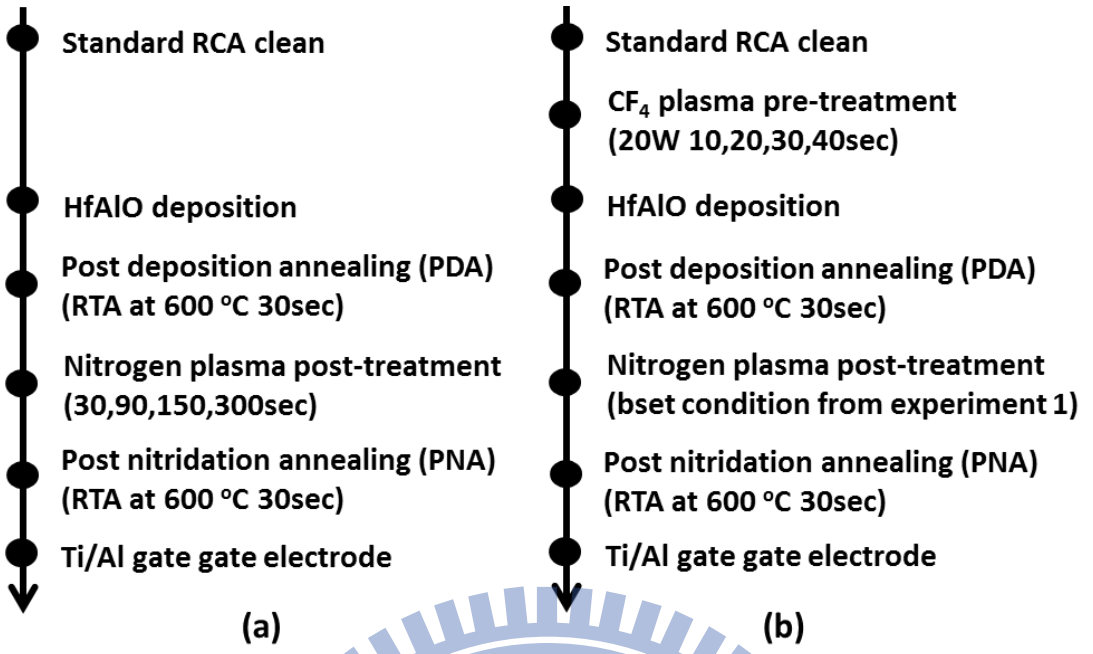

Fig. 3-1 Key process flows of two experiments in this work for (a) single nitrogen post-treatment and (b) dual plasma treatment (CF_4 pre-treatment and nitrogen post-treatment)

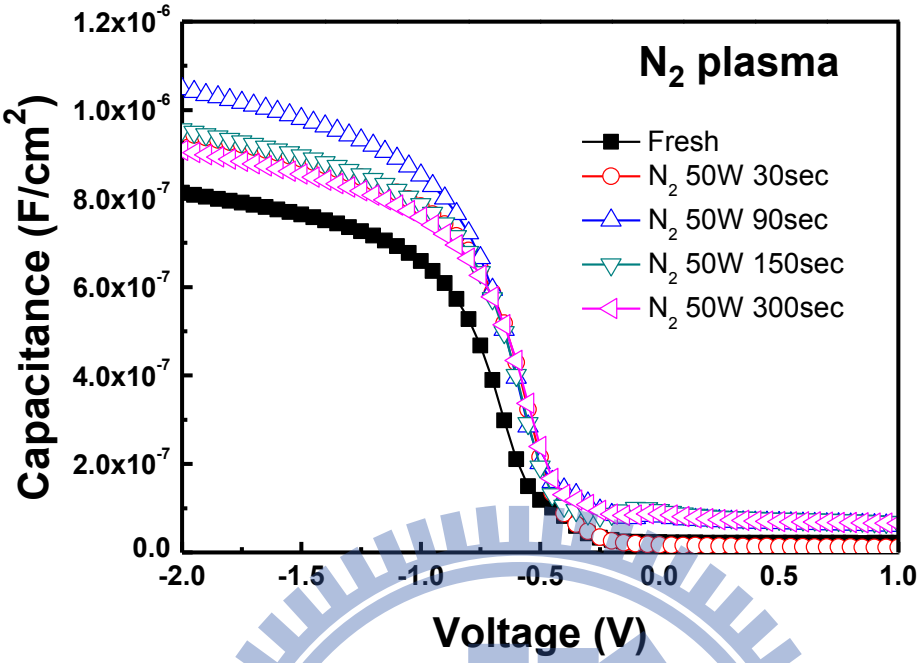

Fig. 3-2 The C-V characteristics of the $HfAlO_x$ thin films with N_2 post-treatment for different process durations.

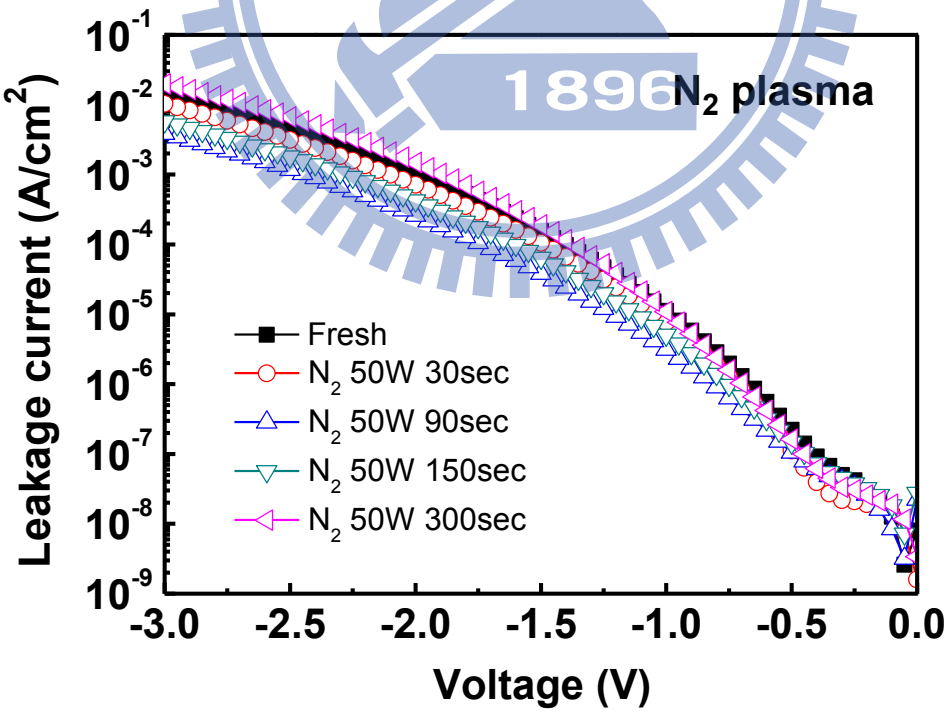

Fig. 3-3 The I-V characteristics of the $HfAlO_x$ thin films with N_2 post-treatment for different process durations.

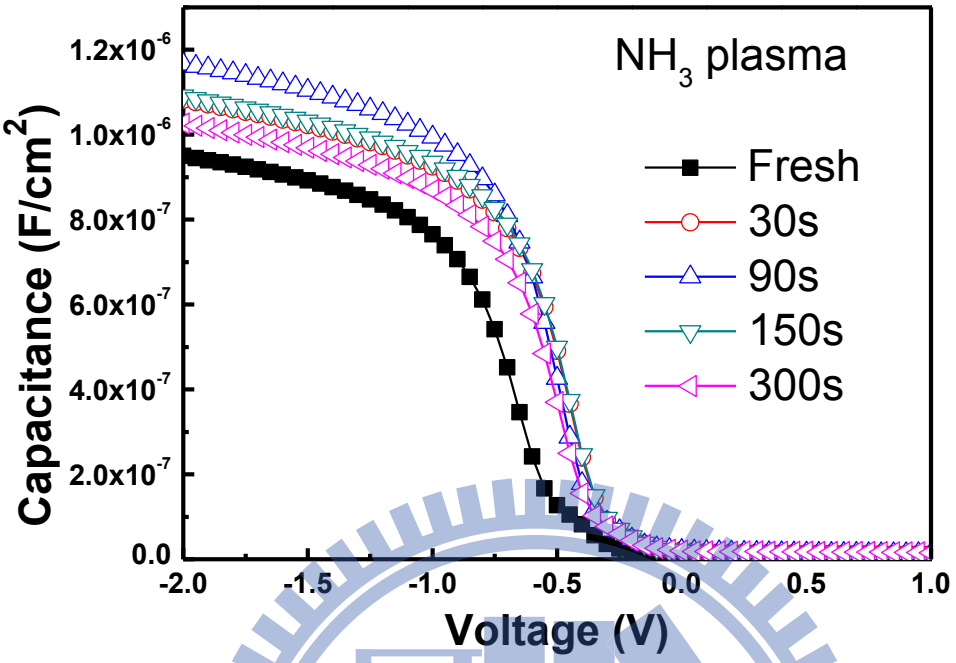

Fig. 3-4 The C-V characteristics of the $HfAlO_x$ thin films with NH_3 post-treatment for different process durations.

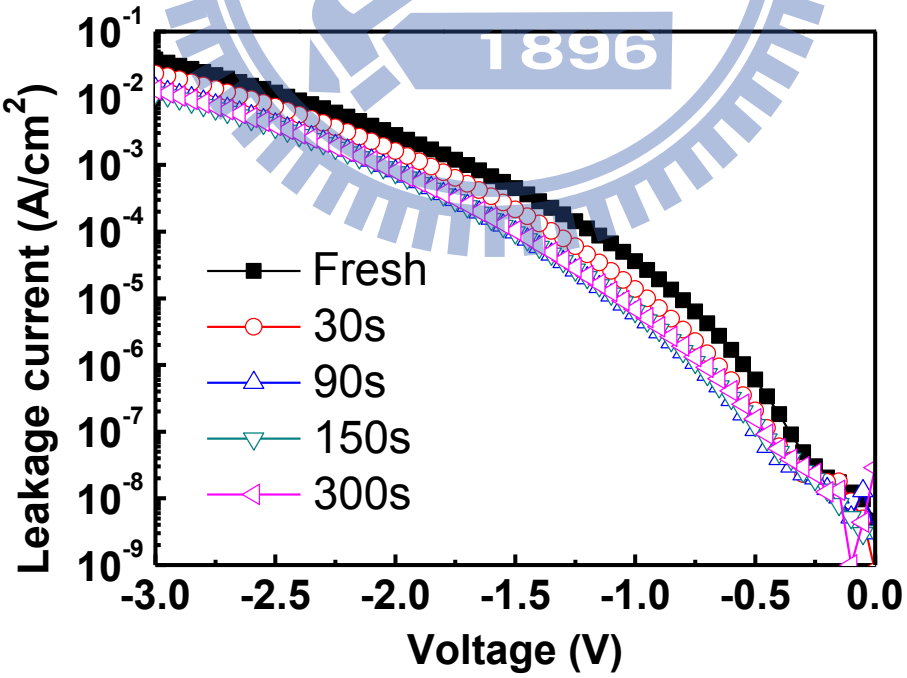

Fig. 3-5 The I-V characteristics of the $HfAlO_x$ thin films with NH_3 post-treatment for different process durations.

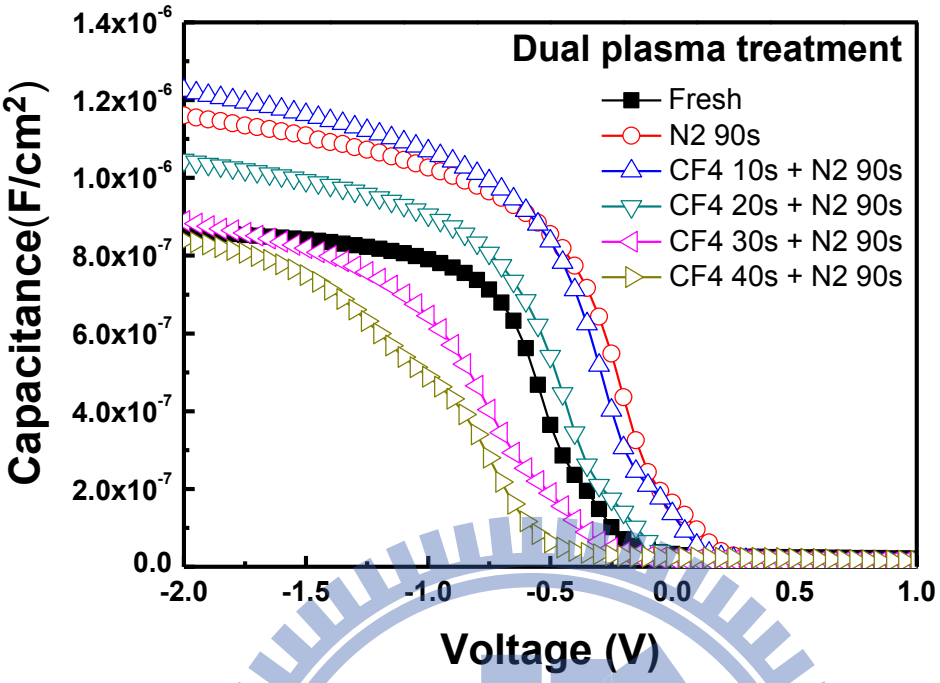

Fig. 3-6 The C-V characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec.

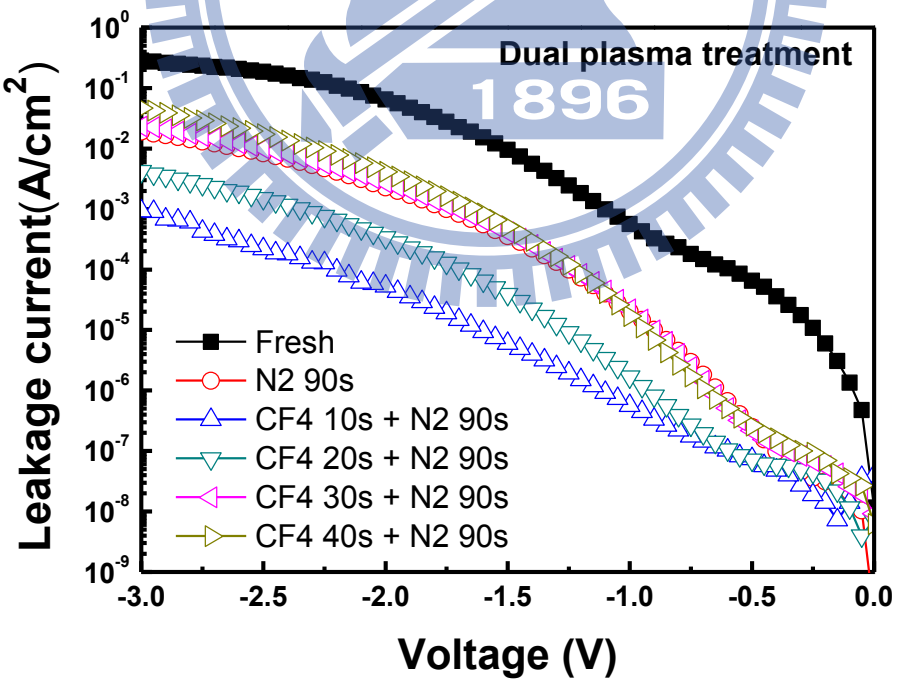

Fig. 3-7 The J-V characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec.

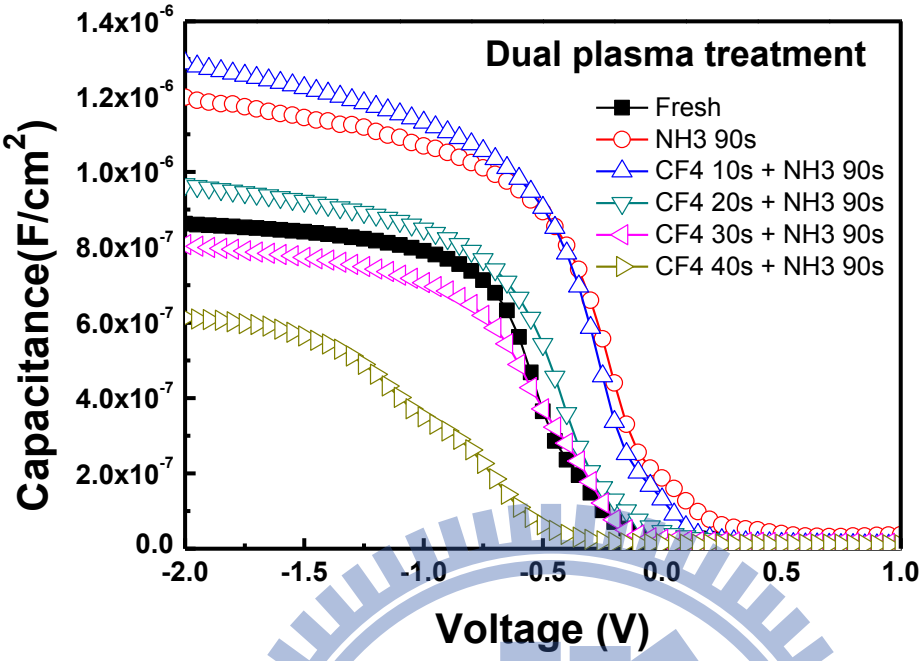

Fig. 3-8 The C-V characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 90 sec.

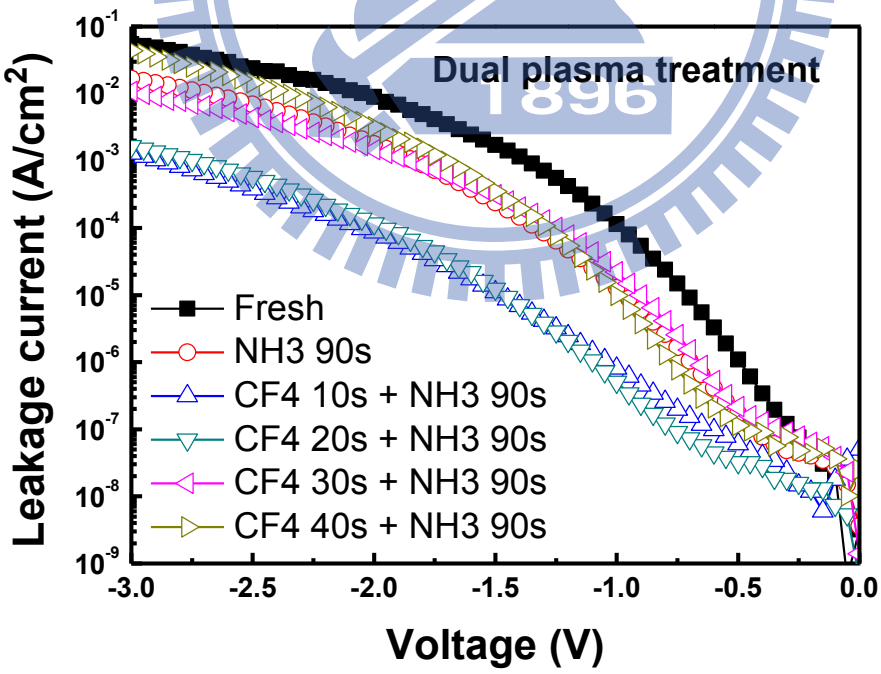

Fig. 3-9 The J-V characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 90 sec.

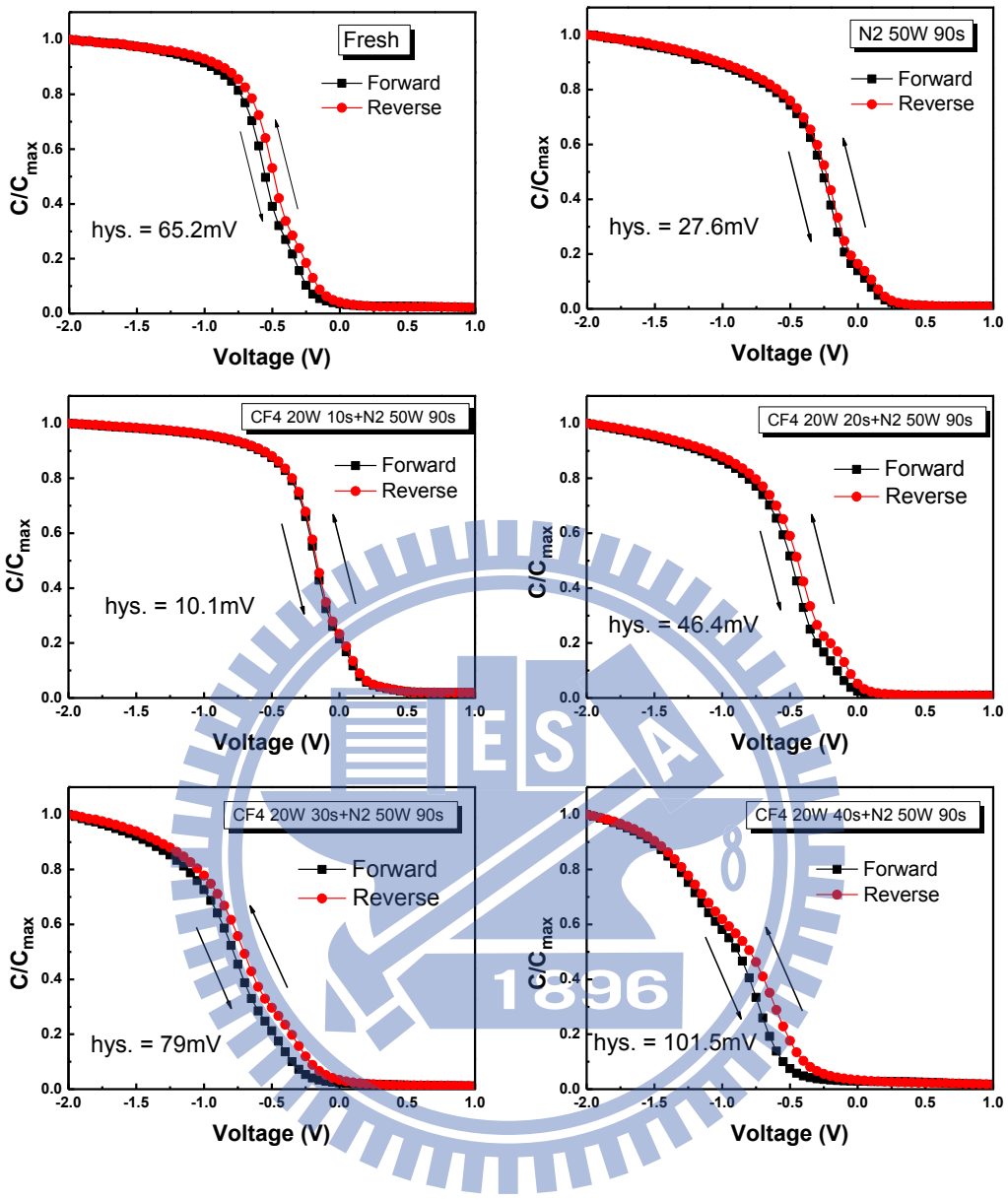

Fig. 3-10 The hysteresis characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec.

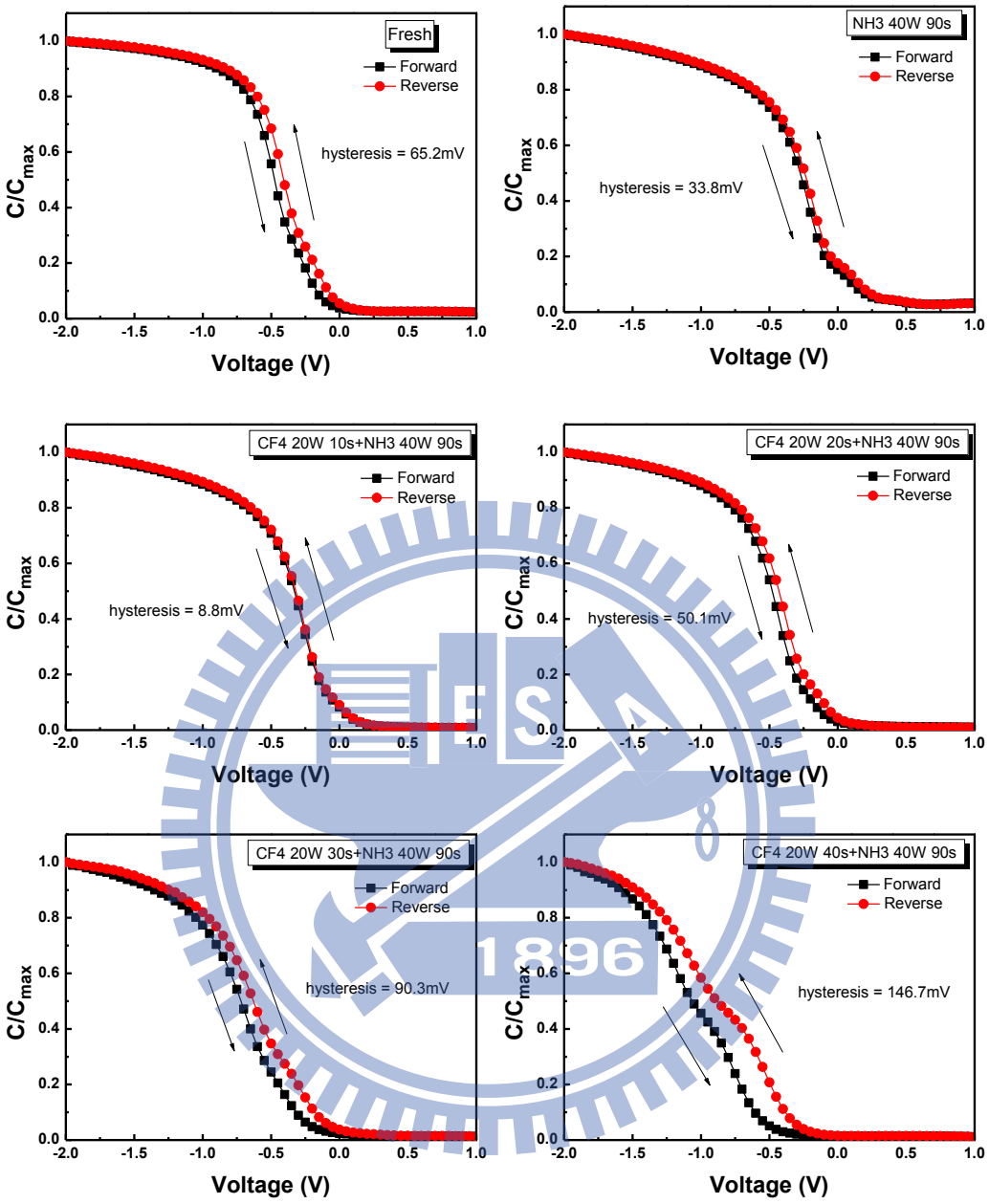

Fig. 3-11 The hysteresis characteristics of the $HfAlO_x$ thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 90 sec.

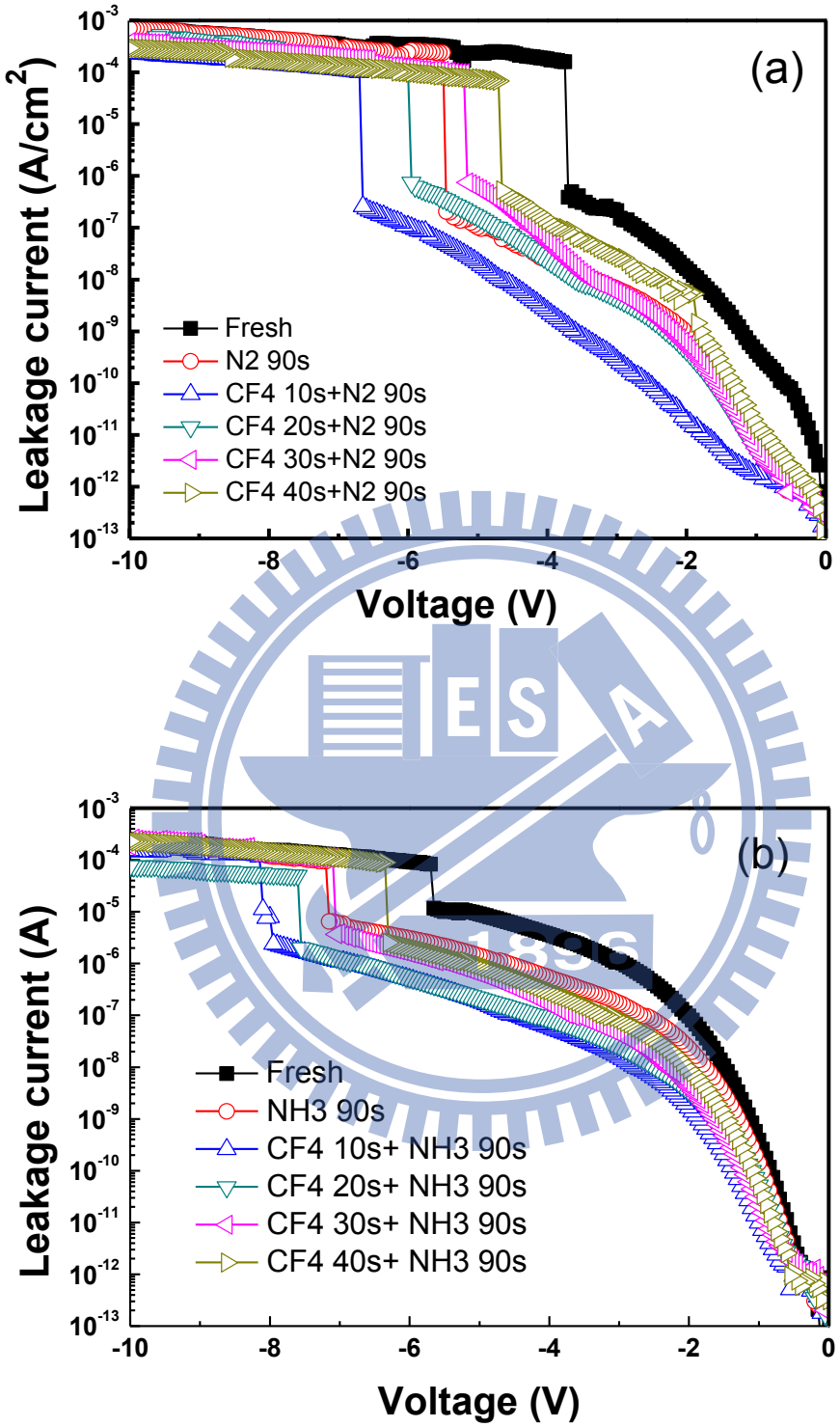

Fig. 3-12 Breakdown behavior of $HfAlO_x$ MIS capacitor treated in (a) CF_4 and N_2 plasma treatment, and (b) CF_4 and N_2 plasma treatment.

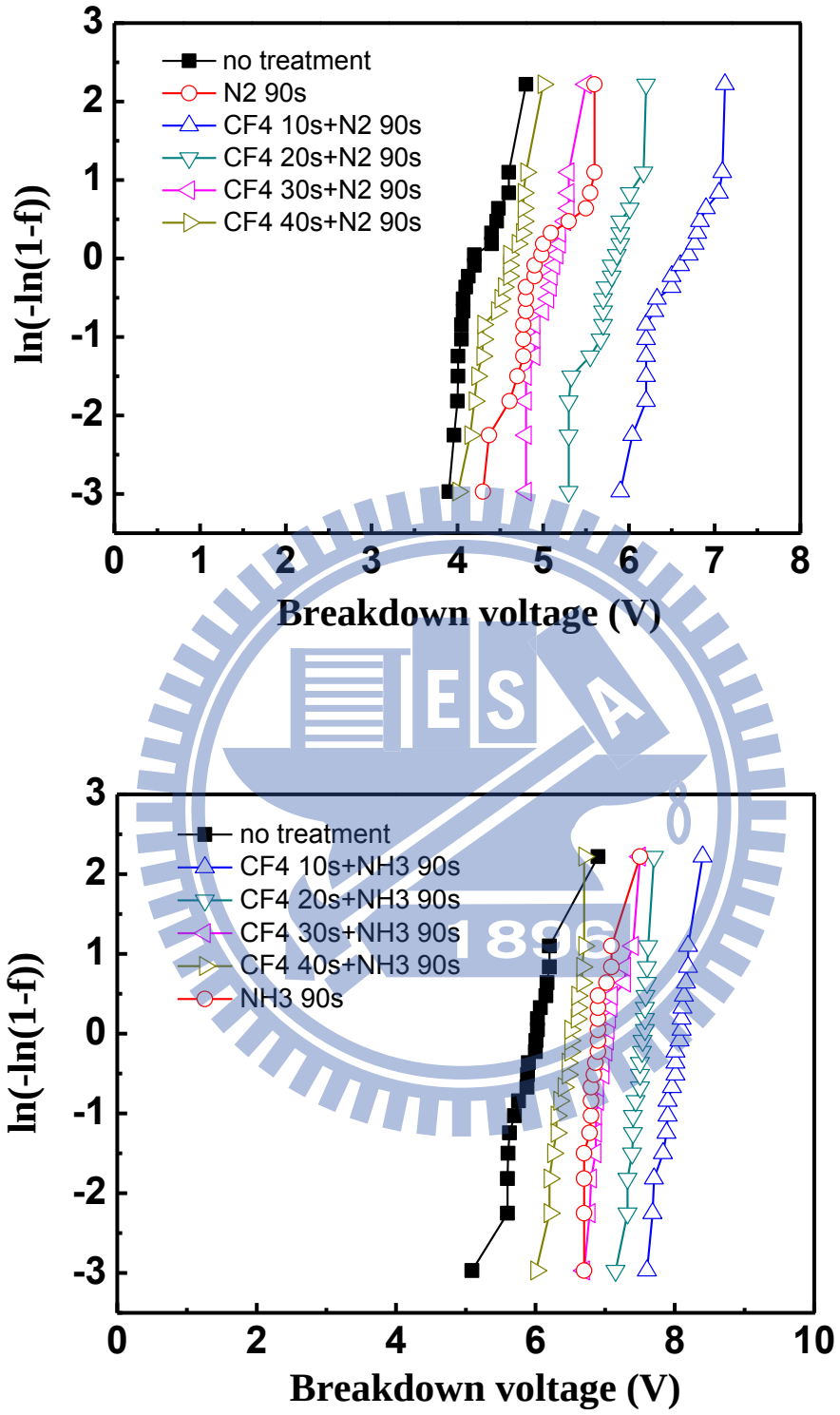

Fig. 3-13 The Weibull plot of the breakdown voltage $HfAlO_x$ MIS capacitor treated in (a) CF_4 and N_2 plasma treatment, and (b) CF_4 and N_2 plasma treatment.

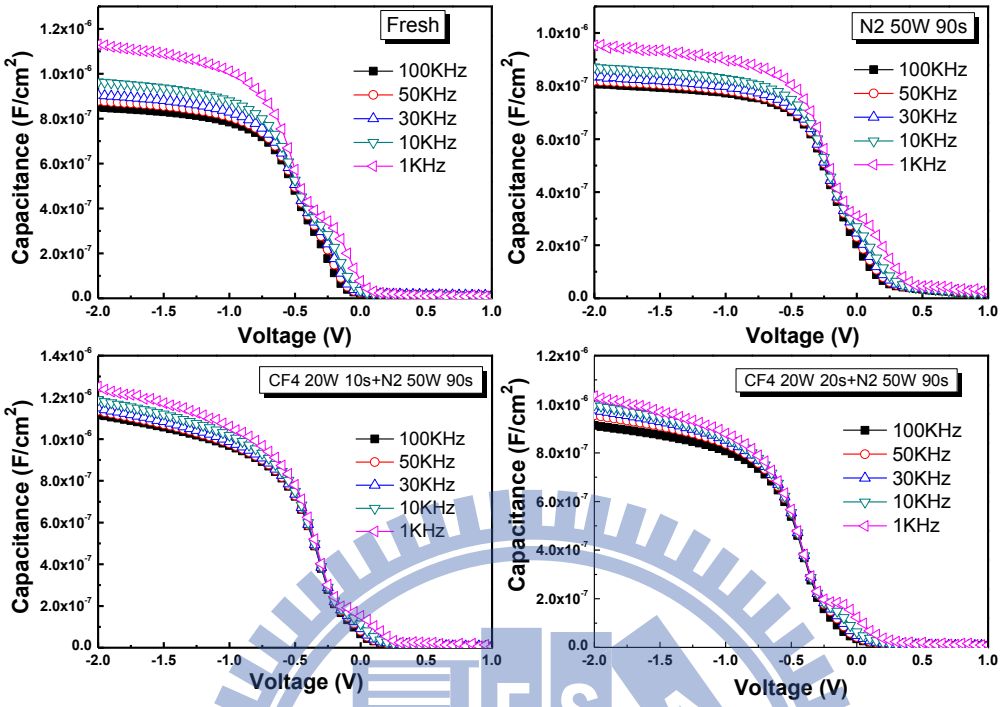

Fig. 3-14 C-V frequency dispersion characteristics of the HfAlOx thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec.

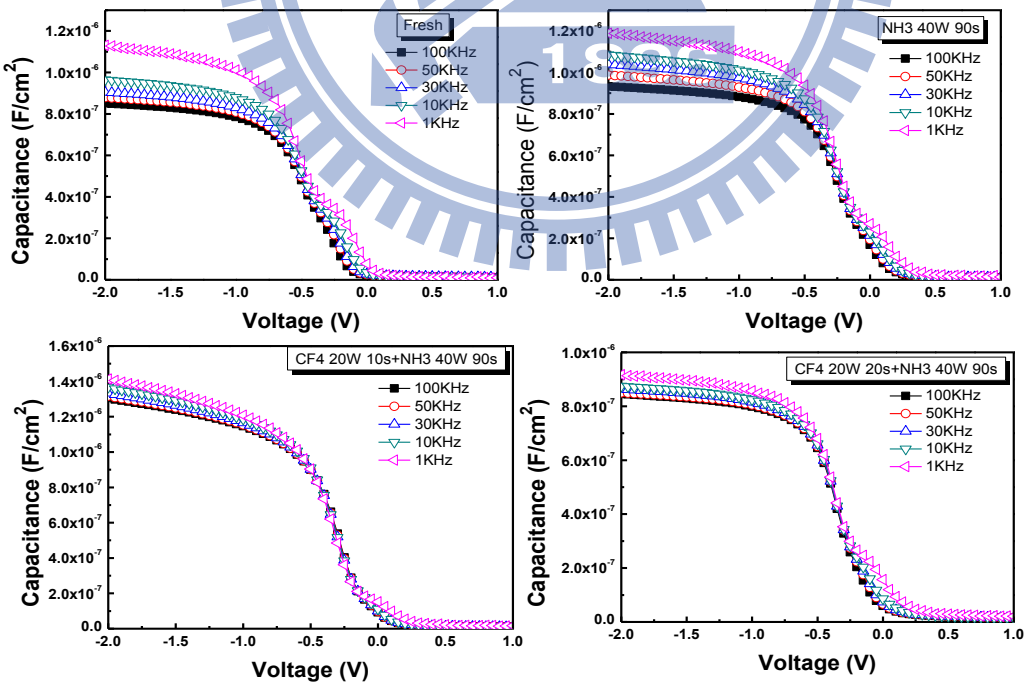

Fig. 3-15 C-V frequency dispersion characteristics of the HfAlOx thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 90 sec.

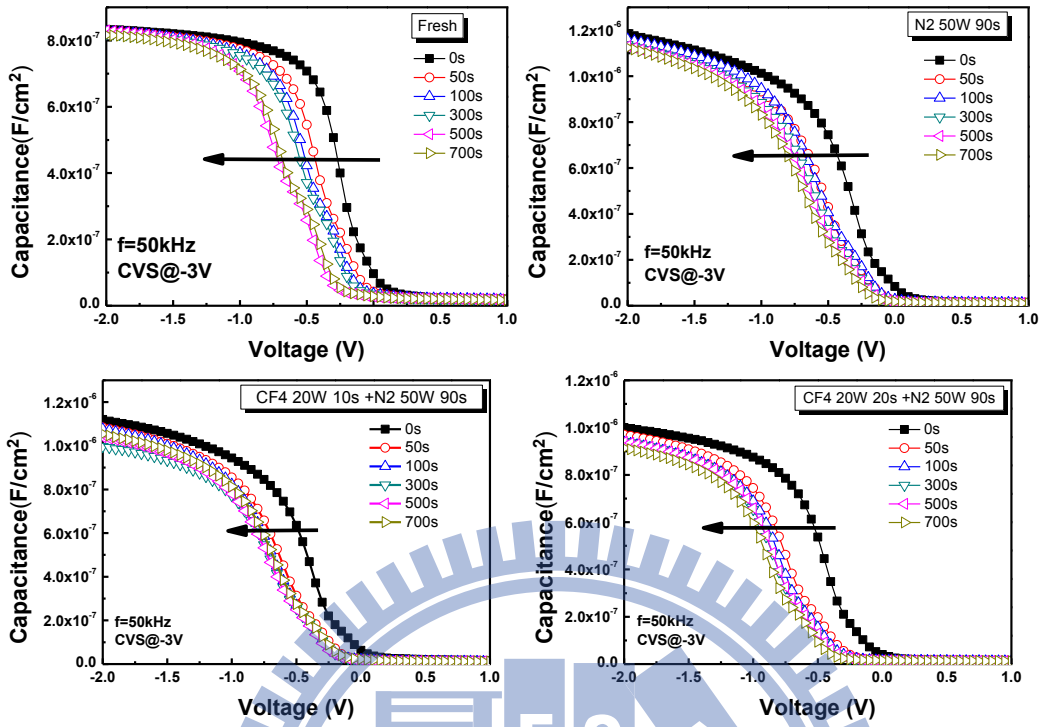

Fig. 3-16 The C-V curves before and after CVS characteristics of the HfAlOx thin films treated in CF_4 plasma for different process durations and N_2 plasma for 90 sec.

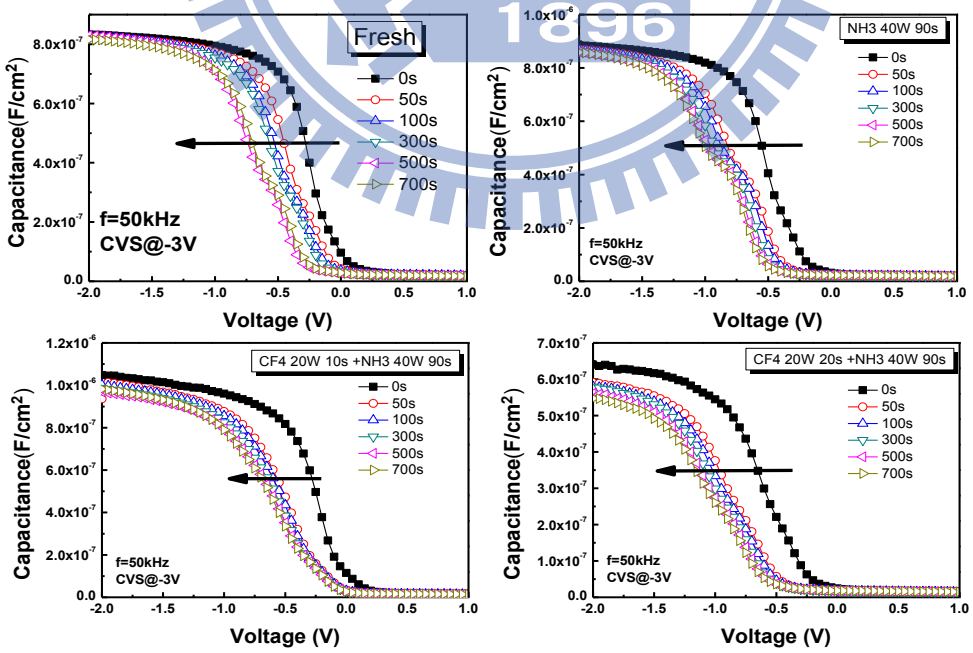

Fig. 3-17 The C-V curves before and after CVS characteristics of the HfAlOx thin films treated in CF_4 plasma for different process durations and NH_3 plasma for 90 sec.

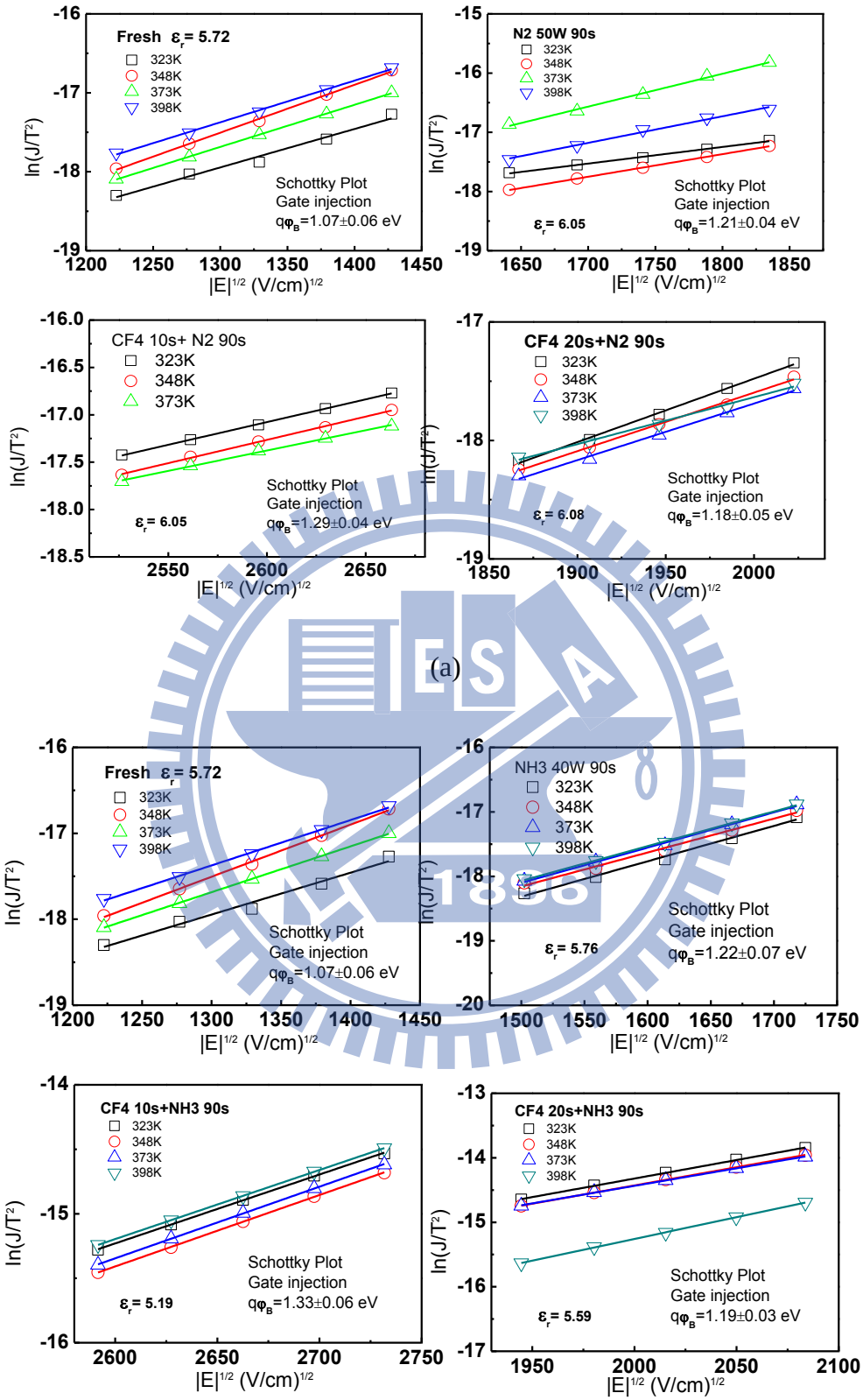

Fig. 3-18 Schottky emission plots, ln(J/T2) versus E1/2, for the HfAlOx thin film with (a) CF_4 plasma + N_2 plasma (b) CF4 plasma + NH3 plasma at different temperatures

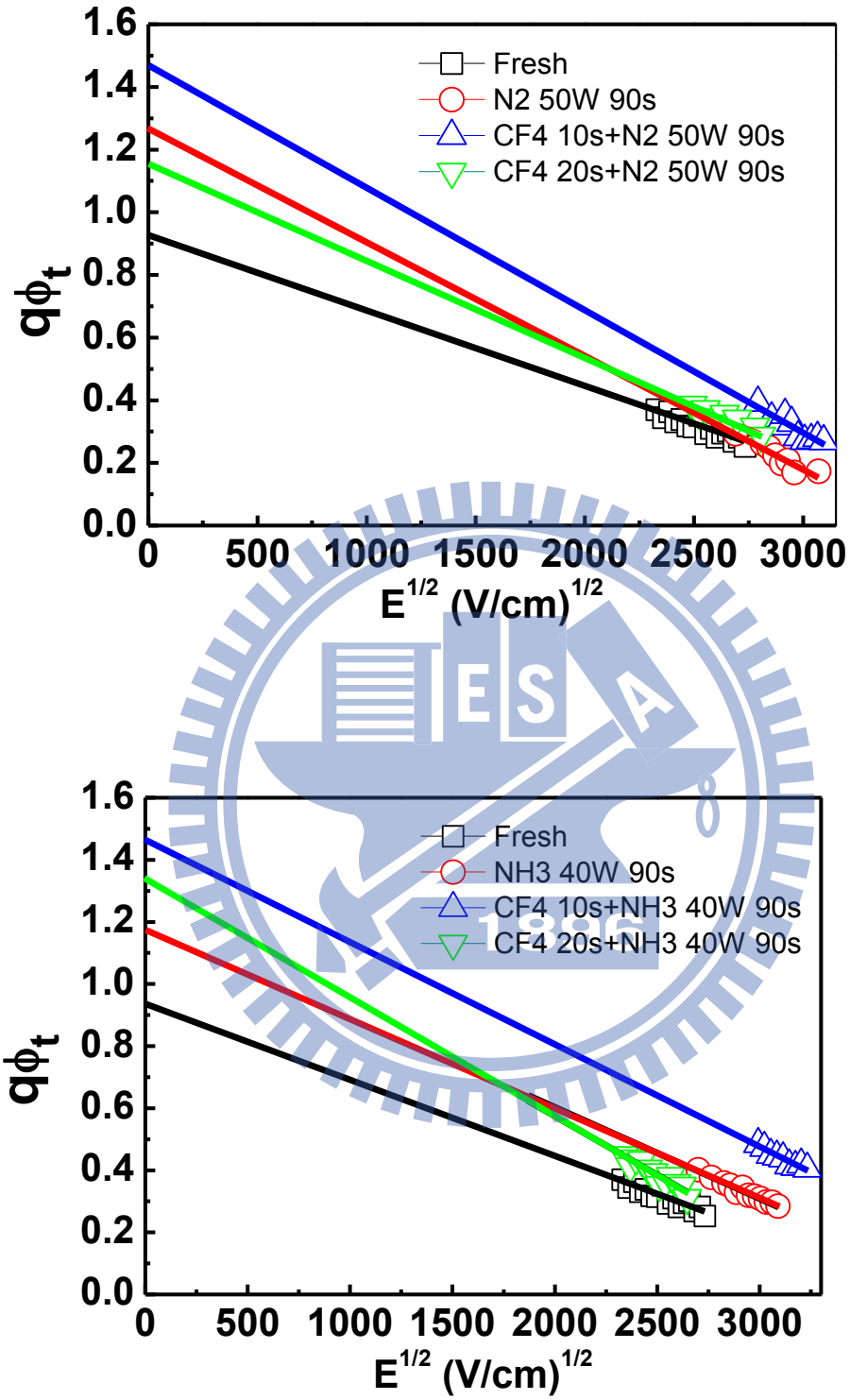

Fig. 3-19 Trapping energy levels extracted from F-P fitting for the $HfAlO_x$ samples with dual plasma treatment (a) CF_4 plasma and N_2 plasma (b) CF_4 plasma and NH_3 plasma.

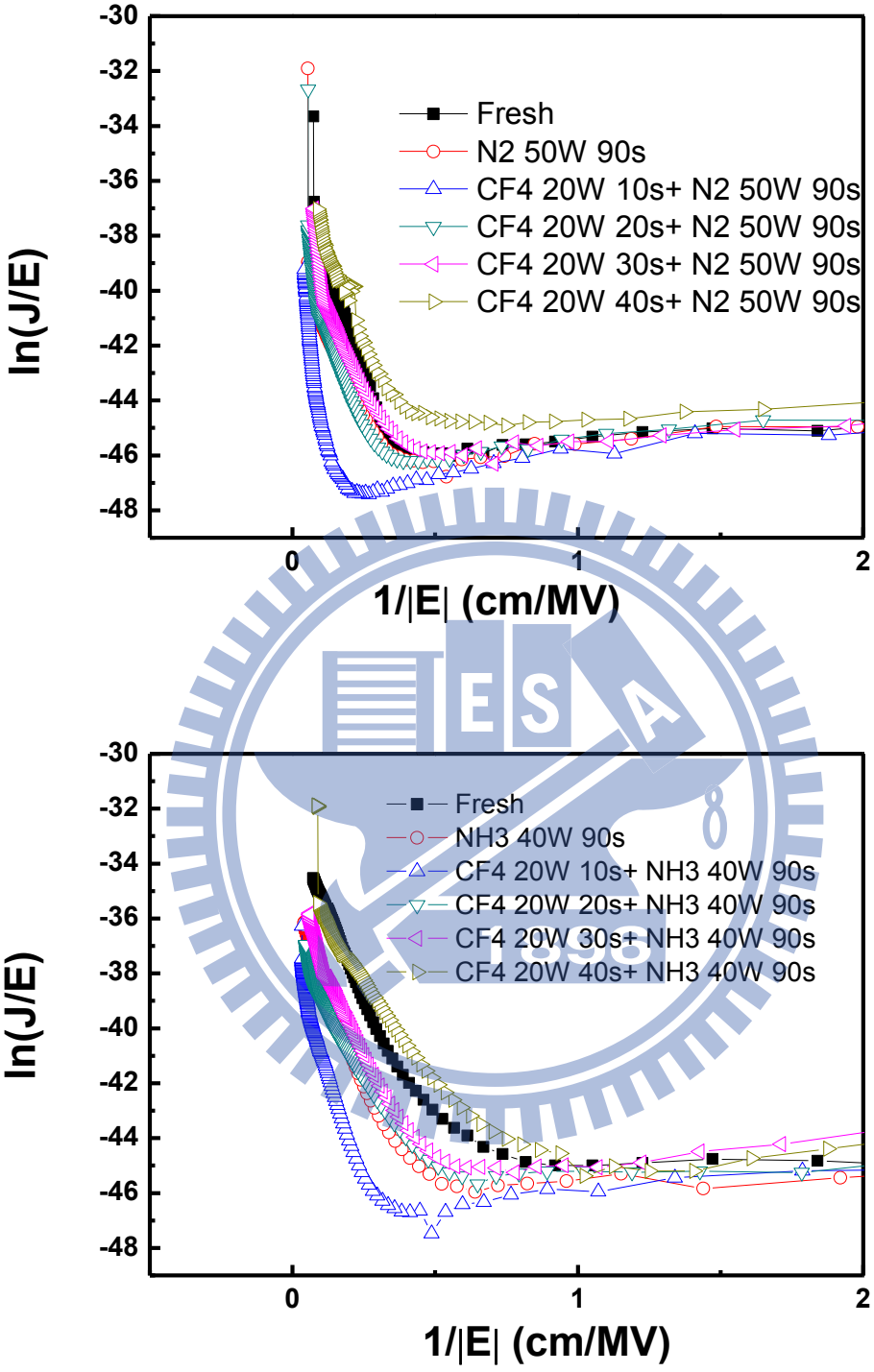

Fig. 3-20 F-N tunneling characteristic, $\ln(J/E^2)$ vs. 1/E, for the $HfAlO_x$ samples with dual plasma treatment (a) CF_4 plasma and N_2 plasma (b) CF_4 plasma and NH_3 plasma

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Chapter 4

Investigation of Dual Plasma Treatment on Low Temperature Polycrystalline Silicon Thin Film Transistor with HfO_2 High-κ Gate Dielectric

4.1 Introduction

4.1.1 Background of silicon channel thin-film transistor

Polycrystalline silicon thin-film transistors (TFTs) have been widely investigated in fields such as large-area electronic applications, including linear image sensors and active-matrix liquid crystal displays (AMLCDs) [1-3]. The major application of poly-Si TFTs in AMLCDs is the peripheral driving circuits and the pixel switching elements on the same glass substrate to realize system-on-panel technology [4]. Nevertheless, developing high performance and high reliability poly-Si TFTs are difficult for both peripheral driving circuits and the pixel switching elements. Pixel switching elements required TFTs to operate at higher voltages as well as low gate leakage currents to drive the liquid crystal; on the other hand, peripheral driving circuits needs TFTs with good electrical characteristics, such as low operation voltage, low sub-threshold swing, high driving current, and low gate leakage current.

The liquid crystal of LCD can have different polarization which can make the

incident white light revel different colors. The switch device, which controls the polarization of the liquid crystal, is required to make the liquid crystal be a display monitor. At first, amorphous-Si TFTs are generally chosen to be the switch device in LCD industry. However, the driving currents of a-Si TFTs are too low. The low driving current is attributed to low conductive of a-Si, which is corresponding to low field effect mobility (~1 cm^2/V-s). High driving current of switch device is needed to drive the pixels and enhance the respond time of liquid crystal in developing the large size display panel. In that case, low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been employed to instead the a-Si TFTs due to higher field effect carrier mobility (μ_{eff}). The field effect mobility in poly-Si is higher than in a-Si about 1~2 orders [10]. In addition to the switch device, the functional electronic circuits of LCD are integrated on the panel to achieve system-on-panel (SOP). High performance TFTs including low gate leakage current, low sub-threshold swing, high driving currents, and low threshold voltage are necessary to achieve high performance circuits. In summary, the improvement of LTPS TFTs on large area glass substrate becomes a significant issue in AMLCD technology.

Because the LTPS TFTs is usually fabricated on glass substrate, the low temperature process is necessary due to the melting point of the glass panel. The solid phase crystallization (SPC) process is widely used to recrystallize the a-Si because of its good grain size uniformity and low production cost [11]; besides, SPC process usually with the maximum process temperature at 600 ^oC for low temperature purpose.

Even though the TFT structure is similar with silicon-on-insulator (SOI) device, there are still different between two devices. The different between the TFT and the SOI device is the crystal phase of the silicon channel thin film; that is, amorphous or

polycrystalline silicon thin film is refer to TFT and single crystalline silicon thin film is refer to SOI device. SOI device exhibits ultra-high performance in VLSI technology due to higher carrier mobility and the suppression of short channel effect. In recent year, TFTs have much attention for the application of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) in the back-end fabrication process of VLSI technology [12-13] because the purpose of three dimension integration of integrates circuit.

4.1.2 LTPS TFTs with high-κ gate dielectric

In order to improve the electrical performance of the LTPS TFTs, having thinner gate oxide thickness can increase the gate capacitance density and enhance the driving current. However, the gate leakage current is unacceptable if the gate oxide becomes thinner, which will significantly degrade the electrical characteristics of LTPS TFTs [14]. In order to replace conventional SiO_2 as a gate dielectric thin film, high-κ materials have been investigated, such as HfO_2, ZrO_2, TiO_2, La_2O_3, Ta_2O_5, Al_2O_3, and $SrTiO_3$ [15-17]. Among all these high-κ materials, HfO_2 is a promising gate dielectric layer because it has high dielectric constant (κ ~ 25), relatively large band gap (Eg ~ 5.7 eV), large conduction band offset with Si (~1.5 eV), and stable contact with Si [18].

4.1.3 LTPS TFTs with plasma treatment

There are many defects in at the grain boundary of the polycrystalline silicon thin film, causing the performance degradation of the LTPS TFTs [19]. It has been reported that poly-Si TFTs with high-κ gate dielectric would suffer from a more undesirable gate-induced drain leakage (GIDL) [20] because such high gate capacitance density would contributed to a high electric field at the gate-to-drain

overlap, resulting in high field emission via the trap states at the grain boundaries. There are various techniques to improve the performance and reduce the trap states, including hydrogen plasma treatment or fluorine ion implantation into poly-Si [21-24]. According to chapter 2 and chapter 3, we have demonstrated the dual plasma treatment on MIS capacitor with high-κ gate dielectric. In this study, dual plasma treatment (CF_4 pre-treatment and N_2 post-treatment) will be utilized on LTPS TFTs to reduce defects in poly-Si channel and HfO_2 gate dielectric.

4.2 Experimental

Fig. 4-1 shows the Schematic of process flow of high-κ HfO_2 gate dielectric LTPS TFT structure with dual plasma treatment. After standard RCA cleaning, 500 nm buried thermal oxide layer was capped on the silicon substrate. A 50 nm un-doped amorphous (a-Si) film was deposited on buried oxide by using low pressure chemical vapor deposition (LPCVD) system. In order to recrystallize the a-Si to poly-Si, solid phase crystallization (SPC) process was used at 600 ℃ for 24-h in a N_2 ambient. Then, 500-nm oxide as device isolation layer was deposited by plasma enhanced chemical vapor deposition (PECVD) system at 300 ^{o}C, as shown in Fig. 4-1(a). The device active region was patterned and S/D region was etched by BOE solution. After the S/D was implanted with phosphorus ($20\ \text{keV at}\ 5\times10^{15}\text{cm}^{-2}$), the S/D was activated at 600℃ for 24 hours annealing in N_2 ambient, as shown in Fig. 4-1(b). After active region patterning, CF_4 plasma pre-deposition treatment was performed on poly-Si by PECVD system at 300 ℃ with power 20 W and the flow-rate was 100 sccm while the pressure is 500 mTorr, as shown in Fig. 4-1(c). Then, high-κ HfO_2

gate dielectric was deposited by electron-beam evaporation system at room temperature. After post deposition annealing in O_2 ambient by furnace to improve gate oxide quality, N_2 plasma post-deposition treatment was performed at 300℃. The RF power was 30W and a flow-rate was 100 sccm at a pressure 500 mTorr, as shown in Fig. 4-1(d). Post nitridation annealing (PNA) was performed with RTA equipment at 600 ^{o}C for 30 sec in order to reduce plasma damage. Thereafter, 500 nm Al films were deposited by thermal coater system after contact hole patterning. Finally, the gate and S/D electrodes were defined lithographically as illustrated in Fig. 4-1(e).

4.3 Electrical characteristics of LTPS TFTs

4.3.1 Transfer characteristics I_{DS}-V_{GS}

Fig. 4-2 shows the transfer characteristics I_{DS}-V_{GS} of the HfO_2 LTPS-TFTs with and without dual plasma treatment at V_d = 0.1V and V_d = 1V. The channel width (W) and the channel length (L) are 100μm and 10μm, respectively. The device parameter such as the threshold voltage (V_{th}), field effect mobility (μ_{eff}), subthreshold swing (S.S.), and on-off current ratio (I_{on}/I_{off}) are extracted at V_d = 0.1V. The threshold voltage is defined by the constant current method as the gate voltage when the drain current reach 100nA × (W/L) at V_d = 0.1V. The on-off current ratio is defined as the ratio of the maximum driving current to the minimum leakage current at V_d = 0.1V. The field effect mobility (μ_{eff}) is extracted from the maximum transconductance at V_d = 0.1V. Table 4-1 illustrates the device parameters for HfO_2 LTPS-TFTs with and without dual plasma treatment. It could be observed that the sample with dual plasma treatment displays better performance than the sample without treatment. The

minimum leakage current (I_{off}) is reduced from 58 to 5.02 pA, whereas the subthreshold swing (S.S.) is improved from 0.27 to 0.21 V/dec. The grain defects and interface states affect the I_{off} and S.S. [25]; in other word, the improvement on I_{off} and S.S. is attributed to the reduction of the grain defects and interface states. The interface trap state density (D_{it}) near the HfO_2/poly-Si interface could be evaluated from subthreshold swing (S.S.) by neglecting the depletion capacitance in the channel layer [26], as shown in eq. 1.

$$D_{it} = \left[\left(\frac{S.S.}{\ln 10}\right)\left(\frac{q}{KT}\right) - 1\right]\left(\frac{C_{OX}}{q}\right). \quad (1)$$

Based on the calculation, the effective interface state for the fresh sample is 7.83×10^{12} cm^{-2}, while the sample with dual plasma treatment is 5.59×10^{12} cm^{-2}. It indicates that the D_{it} have 28.6% reduction because of dual plasma treatment. Fig. 4-3 displays the hysteresis characteristics for the sample with and without dual plasma treatment. It could be seen that the sample with dual plasma treatment has smaller V_{FB} shift than the fresh sample, indicating the interface states could be efficiently decreased by dual plasma treatment. Fig. 4-4 shows the transconductance (G_m) of the HfO_2 LTPS-TFTs. The sample with dual plasma treatment shows the better transconductance than the sample without treatment. The improvement might be attributed to that dual plasma treatment could reduce the interface state at the HfO_2/poly-Si interface and reduce the defect in the high-κ gate dielectric. In addition, nitrogen in the high-κ gate dielectric could increase the permittivity, resulting in the enhancement of driving current. Fig. 4-5 depicts the plots of the $\ln[I_D/(V_G-V_{FB})^2]$ versus $1/(V_G-V_{FB})^2$ curves at V_D=1V. The V_{FB} is defined the gate voltage at the minimum drain current, which is at the current transfer characteristic. The grain-boundary trap-state densities (N_{trap}) with and without dual plasma treatment

were also estimated by Levinson and Proano method [27-28]. The grain-boundary trap-state densities (N_{trap}) are the function of the square root of the slope, which could be express as

$$N_{trap} = \frac{C_{ox}}{q}\sqrt{|Slope|}\,. \quad (2)$$

Based on the calculation, the N_{trap} of the sample without treatment is 7.87×10^{12} cm^{-2}; in contrast, the N_{trap} of the sample with dual plasma treatment is 6.35×10^{12} cm^{-2}. It indicates an improvement about 19.3% on the grain-boundary trap-state densities, which imply that dual plasma treatment could terminate the grain boundary defects in poly-Si channel thin film. The key device parameters of the HfO_2 LTPS-TFTs are listed in Table 4-1.

In brief, the sample treated in dual plasma treatment shows the better performance than the control sample, such as lower threshold voltage (1.14 V), better subthreshold swing (0.21 V/dec.), higher transconductance (11.2 μS) and field effect mobility (31.28 cm^2/V-s), and higher On-off current ratio (3.74×10^6). Furthermore, dual plasma treatment could greatly reduce the Interface trap state density and grain-boundary trap-state densities for 28.6% and 19.3%, respectively.

4.3.2 Active energy (E_a)

Fig. 4-6 shows the active energy (E_a) versus gate voltage of HfO_2 LTPS TFTs with and without dual plasma treatment. In order to extract Ea, I_D-V_G characteristics were measured for varying temperature from 25 to 125 ^oC. The value of E_a indicates the barrier of the grain boundary when carrier transport within the poly-Si channel; that is, the higher E_a in the off-state represents the higher carrier transport barrier of the grain boundary [29]. Compared to the sample without treatment, the sample with

dual plasma treatment shows the lower off-state current due to higher activation energy, whereas it shows higher driving current due to its lower activation energy. Fluorine atoms can passivate the trap states, resulting decrease the barrier height for the carrier's transport when the device is turned on and increase the barrier height for the carrier's transport when the device is turned off.

4.3.3 Output characteristics I_{DS}-V_{DS}

Fig. 4-7 depicts the I_D-V_D curve of HfO_2 LTPS-TFTs with and without dual plasma treatment. The high-κ HfO_2 LTPS-TFTs with dual plasma treatment represents higher driving current than no treatment at different gate voltage, due to the higher mobility and smaller threshold voltage. In contrast to the LTPS-TFTs without treatment, the driving currents of HfO_2 LTPS-TFTs with dual plasma treatment increase 28%, 99%, 45%, 36%, and 34% at V_{DS} = 5 V with V_{GS} = 1, 2, 3, 4, and 5 V, respectively.

4.3.4 Flicker noise (1/*f* noise)

Fig. 4-8 illustrates the normalized drain current noise spectral density (S_{ID}/I_{ds}^2) curves of the HfO_2 LTPS TFTs with and without dual plasma treatment at V_{DS}=0.1V and V_G-V_T=1V. The drain voltage was fixed at 0.1V to ensure operation in the linear region. S_{ID} is generally used as index of noise because measurement of current fluctuation is easier than measurement of voltage fluctuation. After the normalization of the drain current (S_{ID}/I_{ds}^2), it can be examined the number fluctuation or the mobility fluctuation without considering the current level. It has been reported that low frequency noise (also called 1/*f* noise or flicker noise) could be related to fluctuations of the grain boundary potential barrier height at the grain boundaries and the oxide traps at the oxide/poly-Si interface for the poly-Si TFTs [30-31]. It could be

observed that the flicker noise could be vastly improved for the sample with dual plasma treatment. The great improvement is attributed to that dual plasma treatment could effectively reduce the grain-boundary trap-state densities at the channel and the oxide traps at the oxide/poly-Si interface.

4.4 Reliability characteristics of LTPS TFTs

4.4.1 Negative bias stress (NBS) and positive bias stress (PBS)

The reliability of HfO_2 LTPS TFT is an important issue. Fig. 4-9 shows the I_D-V_G characteristic of HfO_2 LTPS-TFT with dual plasma treatment before and after negative bias stress (NBS) and positive bias stress (PBS). The stress conditions are V_G = -5V, -3.86V, and 6.14V with $V_D = V_S = 0V$ for 1500 s at T = 25°C. The stress V_G =-3.86 and 6.14 V represent $V_G - V_{th}$ = -5 and 5V, respectively. The flat-band voltage (V_{FB}) is defined as the gate voltage which reaches the minimum drain current [27]. The V_{FB} seems to shift different direction after NBS and PBS, indicating different polarity trap charges produced by NBS and PBS. The negative V_{FB} shift after NBS represents positive fixed oxide charges are produced, whereas the positive V_{FB} shift after NBS represents positive fixed oxide charges are produced. It is consist with the gate leakage characteristics as shown in Fig. 4-10. After NBS, positive fixed oxide charges which trapped into the oxide band gap will decrease the electrical potential of the oxide and increase the probability of electron tunneling, leading to an increase of gate leakage. Besides, negative fixed oxide charges which trapped into the oxide band gap after PBS will increase the electrical potential of the oxide and decrease the probability of electron tunneling, leading to a decrease of gate leakage. The band

diagrams are schematically shown in Fig. 4-11. Fig. 4-12 shows the subthreshold swing (S.S.) and the transconductance (G_m) of the HfO_2 LTPS-TFT with and without dual plasma treatment before and after NBS and PBS. It can be seen that either after NBS or after PBS will degrade the subthreshold swing and transconductance. Compared to the sample with PBS, the sample with NBS shows more aggressive degradation of subthreshold swing and transconductance. Fig. 4-13 and Fig. 4-14 show the transconductance and the subthreshold swing respectively for the sample with and without dual plasma treatment. Compared to the sample without treatment, it can be observed that the sample with dual plasma treatment has better improvement on transconductance and the subthreshold swing, which is owing to defect passivation.

4.4.2 PBS with different times

Fig. 4-15 shows the I_D versus V_G curves of the sample with dual plasma treatment under PBS for different durations. It can be observed that the little negative threshold voltage shift (ΔV_{th}) at the beginning of stress (10s), which might be attributed to the positive oxide charge buildup (ΔN_{ot}). After 10s, ΔV_{th} is positive and continuously increase with time. On the other hand, Fig. 4-16 shows the I_D versus V_G curves of the sample without dual plasma treatment under PBS for different durations. ΔV_{th} is positive and continuously increase with time. Besides, the slope of I-V curve becomes smaller as the stress time goes on, indicating the obvious degradation of shbthreshold swing. Fig. 4-17 shows the time evolutions of ΔV_{th} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBI stress at V_G-V_{TH} = 5V. ΔV_{th} with stress time is approximately follows a logarithmic dependence on times: V_{th}~alogt with a~0.6 for without treatment sample and a~0.46 for dual plasma treatment sample. It can be seen that the sample with dual plasma treatment shows a

smaller threshold voltage shift than the without treatment sample. Furthermore, the increase of threshold voltage shift ΔV_{th} for n-type HfO_2 LTPS-TFT with dual plasma treatment is slower than without treatment, indicating that the dangling bond between HfO_2/poly-Si is repaired by fluorine atoms.

ΔV_{th} is commonly ascribed to interface trap generation (ΔN_{it}) and oxide charge buildup (ΔN_{ot}). Positive ΔN_{ot} causes negative ΔV_{th} and vice versa. ΔN_{it} cause negative ΔV_{th} in pMOSFET and cause positive ΔV_{th} in nMOSFET because different type of interface states will influence ΔV_{th} when pMOSFET or nMOSFET operate at inversion. The interface states are regarded as acceptor-like in the upper half and donor-like in the lower half of the band gap, as shown in Fig. 4-18 [32]. In order to examine the threshold voltage shift (ΔV_{th}) behaviors as shown in Fig. 4-17, ΔN_{it} and ΔN_{ot} will be examined.

When sample under PBS, interface states are substantially generated. The Si-H bonds would be dissociated by inversion electrons in the channel, resulting in Si dangling bonds (Si≡Si·) as follows [33]

$$Si_3 \equiv Si - H + e^- \leftrightarrow Si_3 \equiv Si\bullet + X_{interface}, \quad (3)$$

$$X_{interface} \xleftrightarrow{(diffusion)} X^-_{bulk}, \quad (4)$$

where $X_{interface}$ is H-related released species. According to eq. (4), $X_{interface}$ could diffuse into the HfO_2 gate dielectrics and could be captured to build up the negative oxide charge (ΔN_{ot}), which could result in negative threshold voltage shift (ΔV_{th}).

Fig. 4-19 depicts the time evolutions of ΔN_{it} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBI stress at V_G-V_{TH} ~ 5V. The sample without treatment shows larger ΔN_{it} than the sample with dual plasma treatment, indicating

that dual plasma treatment improves the interface between HfO_2/poly-Si. Based on the conventional diffusion-reaction (D-R) model [34-35], ΔN_{it} created by above kinetics (eq. (3) and eq. (4)) approximately follows a power law related to time. The exponent near 0.25 represents the released species are neutral, whereas the exponent near 0.5 represents the released species are charged. After curve fitting, Fig. 4-19 shows the exponent of ΔN_{it} is ~0.26 for the sample without treatment, indicating the H-related released species are neutral. On the other hand, the exponent of ΔN_{it} is ~0.6 for the sample with dual plasma treatment, indicating the H-related released species might be negatively charged (X_{bulk}^{-}). In addition to X_{bulk}^{-}, electron, tunneling from channel and trapped in the oxide, would contribute the negative ΔN_{ot}, leading to the positive ΔV_{th} after PBS. Based on above discussion, the positive ΔV_{th} of the sample with dual plasma treatment might be attributed to ΔN_{ot}; on the other hand, ΔN_{it} might dominate the positive ΔV_{th} of the sample without plasma treatment.

Fig. 4-20 depicts the variations of the drive current under PBS. The degradation of the drive current might be attributed to oxide trapped charges and interface trap states induced mobility degradation. The sample with dual plasma treatment performs the smaller ΔI_{DS} than the control sample, which is owing to the substitution for the Si-F bonds to dangling bonds or weak Si-H bonds. On the other hand, nitrogen atoms could repair the defects in the HfO_2 bulk.

4.4.3 Positive bias temperature instability (PBTI)

Fig. 4-21 and Fig. 4-22 respectively show the I_D versus V_G curves of the sample with and without dual plasma treatment under PBTI for different durations (0 to 1000 sec.) with V_G-V_{TH} = 5V at T=100 ^oC. Similar degradation behavior such as subthreshold swing (S.S.), transconductance (G_m), and threshold voltage shift (ΔV_{th})

could be observed. However, PBTI shows much aggressive degradation behavior than PBS which described earlier. Fig. 4-23 shows the time evolutions of ΔV_{th} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBTI stress with V_G-V_{TH} = 5V at T=100 ^oC. Positive ΔV_{th} represents that negative charges trapped in the oxide. ΔV_{th} with stress time is approximately follows a logarithmic dependence on times: V_{th}~alogt with a~0.77 for without treatment sample and a~0.8 for dual plasma treatment sample. It can be seen that the sample with dual plasma treatment shows a smaller threshold voltage shift than the without treatment sample. Fig. 4-24 shows the time evolutions of ΔN_{it} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBTI stress with V_G-V_{TH} = 5V at T=100 ^oC. The sample without treatment shows larger ΔN_{it} than the sample with dual plasma treatment, indicating that dual plasma treatment improves the interface between HfO_2/poly-Si. The exponent of ΔN_{it} is ~0.45 for the sample without treatment; On the other hand, the ΔN_{it} is ~0.23 for the sample with dual plasma treatment.

In addition, the drain leakage currents (I_{min}) increase with times for the sample without treatment, as shown in Fig. 4-22. The drain leakage currents (I_{min}) could be contributed to two reasons: the gate leakage current and junction leakage current of drain side [36]. The gate leakage is too low to contribute the drain leakage, as shown in Fig. 4-25 and Fig. 4-26. Consequently, the drain leakage currents (I_{min}) could be attributed to the junction leakage of the drain side near the surface. During positive stress, the electron would be accelerated and move to HfO_2/poly-Si interface, colliding the weak bond of the grain boundary and damaging the interfacial layer (IL). The trap states would increase, which result in the degradation of subthreshold swing (S.S.), transconductance (G_m), and drain leakage currents (I_{min}) [37]. On the other hand, the sample with dual plasma treatment shows better immunity of drain leakage

currents (I_{min}) degradation because the grain boundaries could be passivated by fluorine atoms forming strong Si-F bonds as shown in Fig. 4-21.

4.4.4 Hot carrier stress (HCS)

In order to study the hot carrier stress (HCS) on poly-Si TFT, different drain bias (5-20 V, 5 V per step) with V_G-V_T=5V was applied on the sample, as shown in Fig. 4-27 and Fig. 4-28. Unlike traditional MOSFETs theory, electrical parameters of polysilicon TFTs including threshold voltage (V_{th}), maximum transconductance (G_m), and subthreshold swing (S.S.) could depend on grain, grain boundaries, and interface states [38]. Table 4-2 summarizes some electrical parameters and corresponding possible degradation causes for HfO_2 LTPS-TFTs under HCS. Table 4-3 to Table 4-5 show all electrical parameters degradation under Hot Carrier Stress (HCS) 1000s 1000s with V_{GS}-V_{th}=5V and drain bias 5V, 10V, and 15V respectively.

It can be observed that electrical characteristics of HfO_2 LTPS-TFT degrade severely when drain voltage is applied over 10V, indicating that the impact-ionization effect of Hot Carrier Stress (HCS) is appearing [39], such as as I_{on}, S.S. and G_m shown in Fig. 4-27 and Fig. 4-28. Threshold voltage shift (ΔV_{th}) during hot-carrier stress might be attributed to two degradation mechanism: hot carrier injection into the gate oxide (ΔN_{ot}) and deep grain-boundary trap generation (ΔN_{trap}) [38]. The positive ΔV_{th} appears after HCS and become aggressively when drain voltage is applied over 10V. As shown in Table 4-3 to Table 4-5, the sample with dual plasma treatment shows the best HCS immunity than control sample. Dual plasma treatment not only suppress the Interface states generation (ΔN_{it}) and tail states in the grain boundary but also improves the bulk HfO_2 oxide trap, leading to decrease the possibility of impact ionization and reduce the hot electron injecting into gate oxide.

In order to identify the damage region induced by HCS, the output characteristics of the normal mode and reverse mode (S/D reverse) of the sample after HCS 1000s with V_{GS}-V_{th}=5V and drain bias 15V are shown in Fig. 4-29. Fig. 4-29(a) shows the characteristics of the normal mode. It can be found the curves are crowed at low drain voltage, representing a resistive region which damaged by HCS. Moreover, there is no saturation region at higher drain voltage, so called kink effect, which is attributed to high density of hot-carrier induced traps. Fig. 4-29(b) displays the characteristics of the reverse mode, which mean the interchange of the source and drain. It is obvious that the drain current is much lower than normal mode. This phenomenon is attributed to the existence of the damaged region near the source end in the reverse mode operation and a larger drain voltage drop across the damaged region. As a result, HCS induced damage region is located near the drain side.

4.5 Physical analysis

Fig. 4-30 depicts the Hf 4f ESCA spectra of the sample without treatment. It could be seen that two distinct peaks of Hf-O bonding at 16.63 and 18.29 eV. After fluorine plasma pretreatment, the Hf 4f peak of the ESCA spectra would shift to higher binding eanrgy as shown in Fig. 4-31, indicating that the presence of H-F bonds in HfO_2. Fig. 4-32 shows the F 1s ESCA spectra of the sample treated by CF4 pretreatment.

4.6 Conclusion

In this chapter, the dual plasma treatment is successfully utilized on the LTPS-TFTs. The electrical improvement has been studied, including the hysteresis and the I-V characteristics. The device parameters, such as Vth, S.S., G_m, μ_{eff}, D_{it}, and N_{trap} are extracted to study the improvement effect. It shows that the dual plasma sample have better electrical characteristics. Also, according to the 1/*f* noise or flicker noise measurement, dual plasma treatment could effectively reduce the grain-boundary trap-state densities at the channel and the oxide traps at the oxide/poly-Si interface.

Furthermore, the reliability properties and mechanisms of high performance HfO_2 gate dielectric LTPS-TFT with dual plasma treatment are investigated, including PBS, NBS, PBTI, and HCS. Also, the damage region induced by HCS is distinguished by the normal mode and reverse mode (S/D reverse) operation. In conclusion, the sample with dual plasma treatment has better stress immunity than the sample without treatment.

Table 4-1 Device parameters for HfO_2 LTPS-TFTs with and without dual plasma treatment.

	Without treatment	Dual plasma treatment
Threshold voltage, V_{th} (V)	1.37	1.14
Subthreshold swing, S.S. (V/dec.)	0.27	0.21
Transconductance, G_m (μS)	8.19	11.20
Field effect mobility, μ_{eff} (cm^2/V-s)	22.93	31.28
Maximum driving current, I_{on} (μA)	14	18.8
Minimum leakage current, I_{off} (pA)	58	5.02
On-off current ratio (I_{on}/I_{off})	2.42×10^5	3.74×10^6
Interface trap state density (D_{it})	7.83×10^{12}	5.59×10^{12}
Grain boundary trap state density (N_{trap})	7.87×10^{12}	6.35×10^{12}

Table 4-2 Electrical parameters and corresponding possible degradation causes for HfO_2 LTPS-TFTs under HCS [36].

Electrical parameters after stressing	**Mainly depending on**
Δg_{mmax}	❑ interface state generation ❑ state generation in the grain boundaries (tail states)
ΔV_{ON}	❑ charges injected into the gate oxide ❑ interface state generation (deep states) ❑ state generation in the grain boundaries (deep states)
ΔS (subthreshold swing)	❑ intra-grain defect density generation (bulk states) ❑ interface state generation (deep states)

Table 4-3 Electrical parameters degradation under Hot Carrier Stress (HCS) 1000s with V_{GS}-V_{th}=5V and drain bias 5V

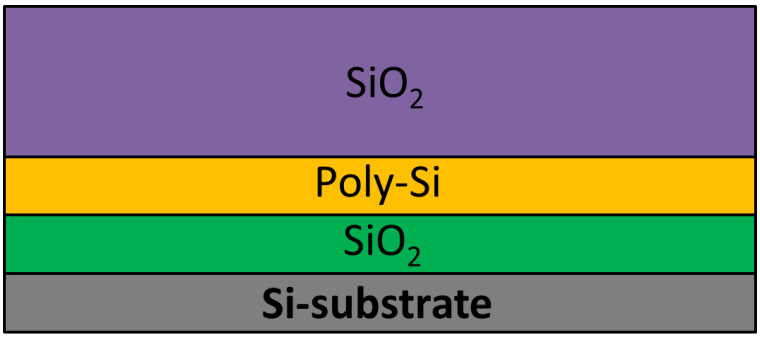
	ΔI_{on} (%)	ΔG_m(%)	ΔS.S. (%)	ΔN_{it}(%)	ΔV_t(V)	ΔN_{trap}(%)
Dual plasma treatment	4.3%	2.7%	33.2%	50.9%	0.578	57.2%
Without treatment	13.3%	4.8%	81.9%	105%	1.08	167%

Table 4-4 Electrical parameters degradation under Hot Carrier Stress (HCS) 1000s with V_{GS}-V_{th}=5V and drain bias 10V

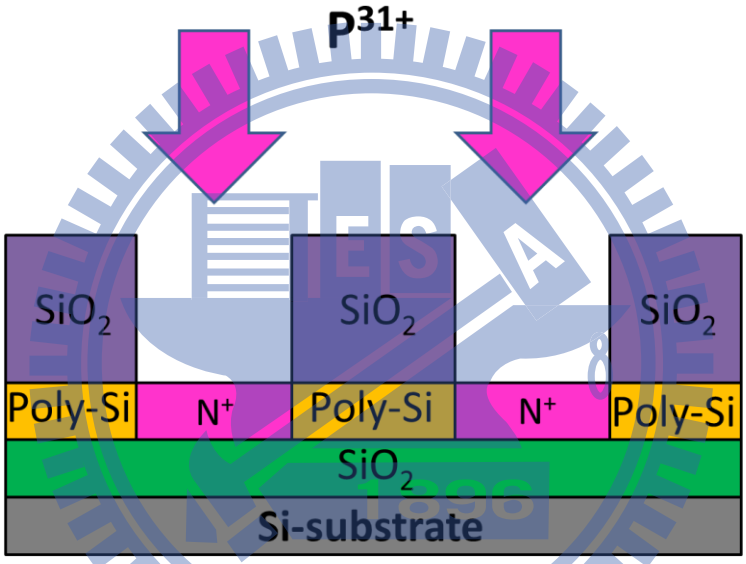
	ΔI_{on} (%)	ΔG_m(%)	ΔS.S. (%)	ΔN_{it}(%)	ΔV_t(V)	ΔN_{trap}(%)
Dual plasma treatment	5%	3.2%	40.7%	62.3%	0.572	57.4%
Without treatment	10%	7.4%	82.2%	106%	1.00	174%

Table 4-5 Electrical parameters degradation under Hot Carrier Stress (HCS) 1000s with V_{GS}-V_{th}=5V and drain bias 15V

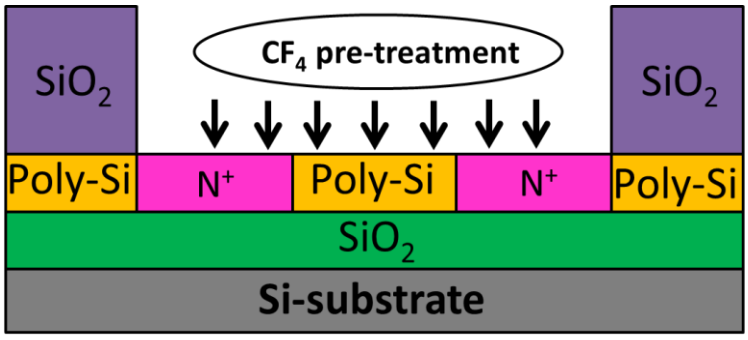
	ΔI_{on} (%)	ΔG_m(%)	ΔS.S. (%)	ΔN_{it}(%)	ΔV_t(V)	ΔN_{trap}(%)
Dual plasma treatment	72%	82.2%	61.1%	93.7%	1.28	112%
Without treatment	96.6%	95.0%	119%	153%	3.10	229%


SiO2
Poly-Si
SiO2
Si-substrate

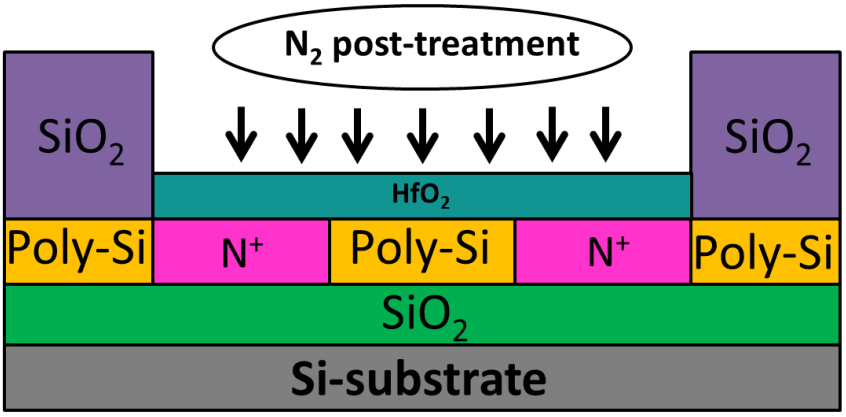
(a)


P31+
SiO2
SiO2
SiO2
Poly-Si
N+
Poly-Si
N+
Poly-Si
SiO2
Si-substrate

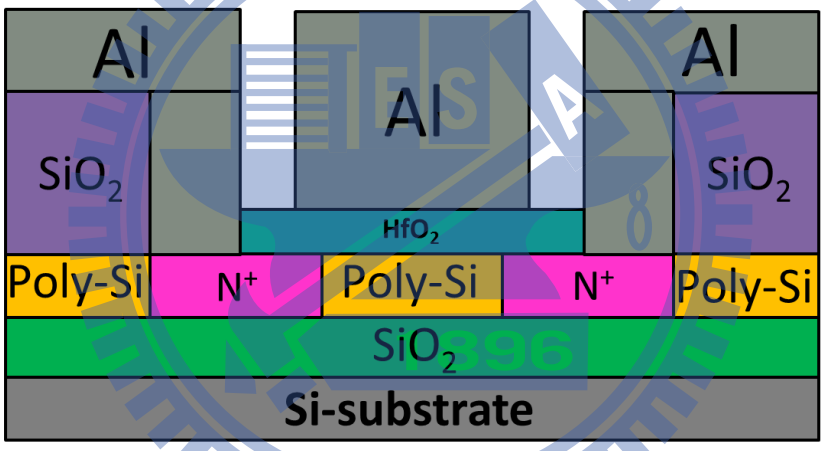
(b)


SiO2
CF4 pre-treatment
SiO2
Poly-Si
N+
Poly-Si
N+
Poly-Si
SiO2
Si-substrate

(c)



(d)



(e)

Fig. 4-1 Schematic of process flow of high-κ HfO_2 gate dielectric LTPS TFT structure with dual plasma treatment.

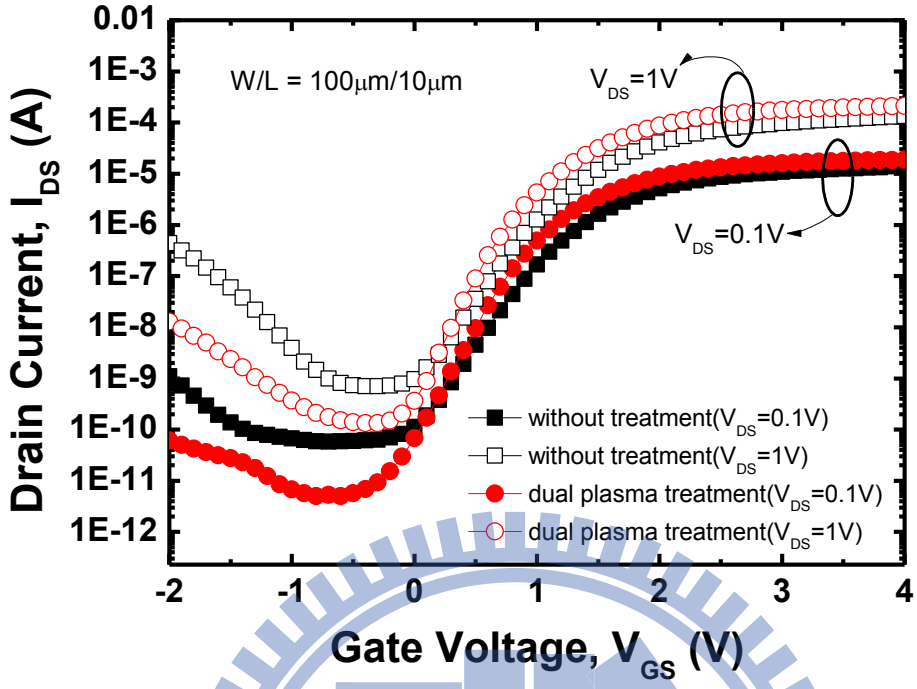


Fig. 4-2 The transfer characteristics I_{DS}-V_{GS} of the HfO_2 LTPS-TFTs with and without dual plasma treatment at V_d=0.1V and V_d=1V.

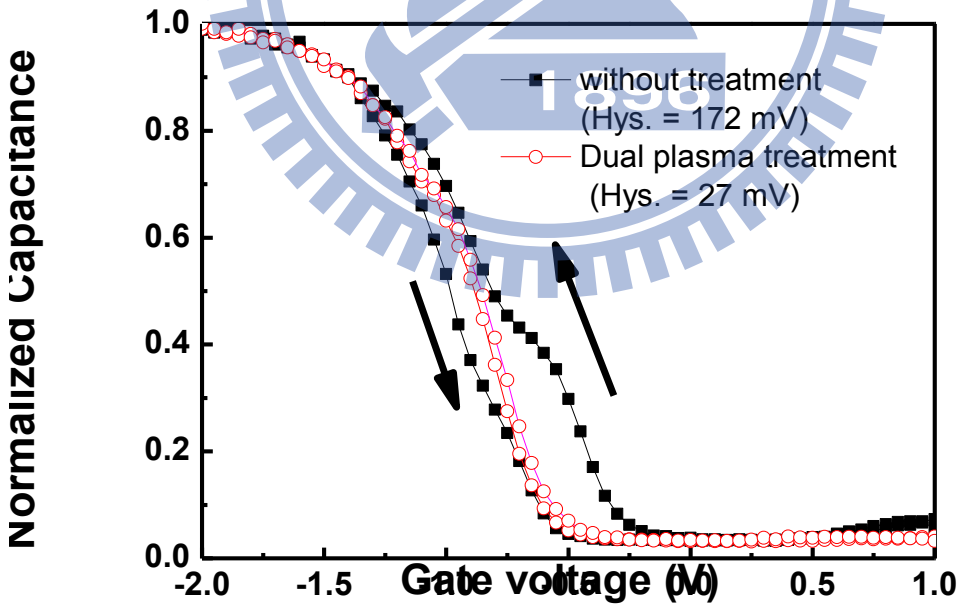


Fig. 4-3 The C-V curve of the HfO_2 MIS capacitor with and without dual plasma treatment.

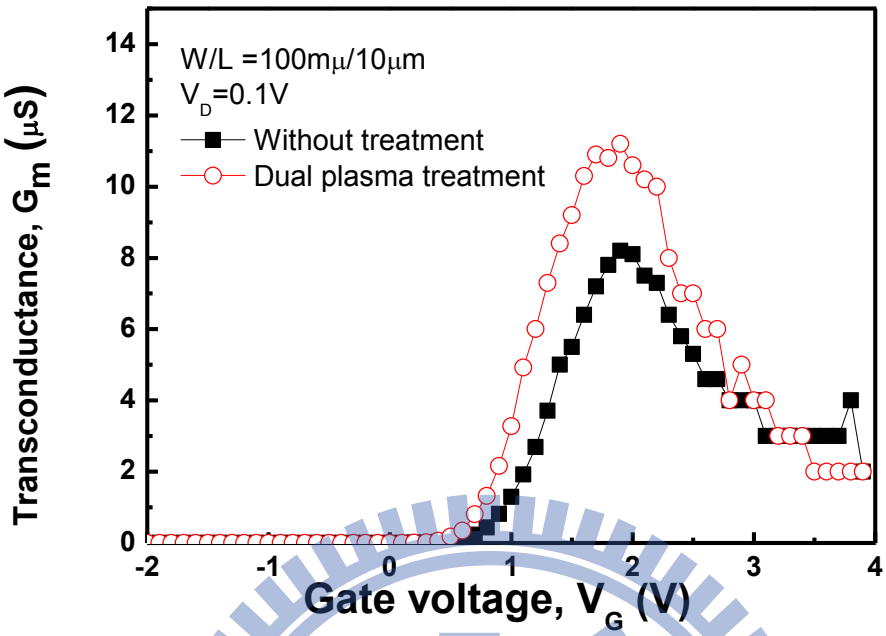


Fig. 4-4 The transconductance (G_m) of the LTPS-TFTs with dual plasma treatment measured at V_d=0.1V.

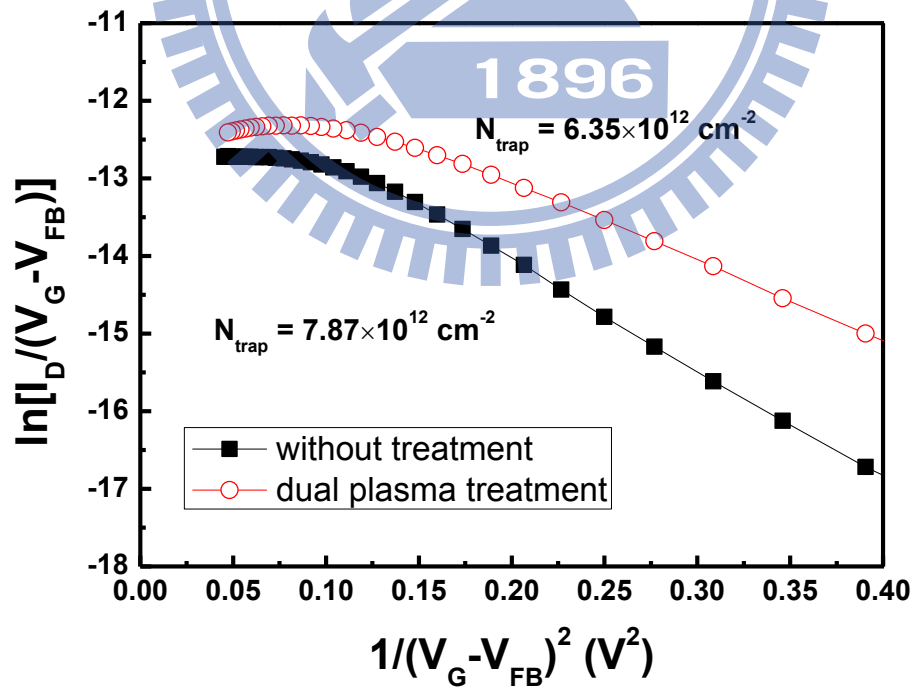


Fig. 4-5 The plots of the $\ln[I_D/(V_G-V_{FB})^2]$ versus $1/(V_G-V_{FB})^2$ curves at V_D=1V.

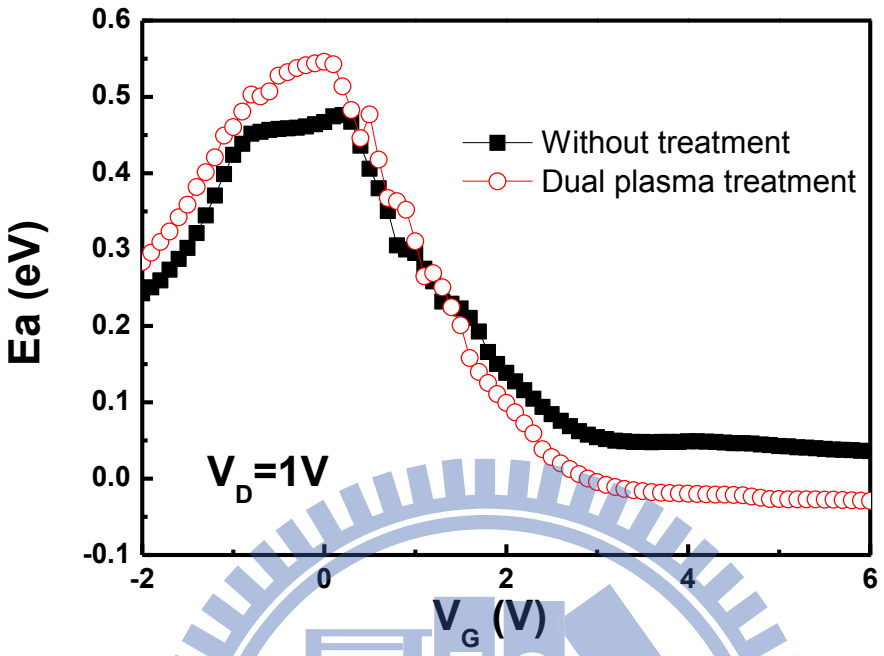


Fig. 4-6 Active energy (Ea) versus gate voltage of HfO_2 LTPS TFTs with and without dual plasma treatment.

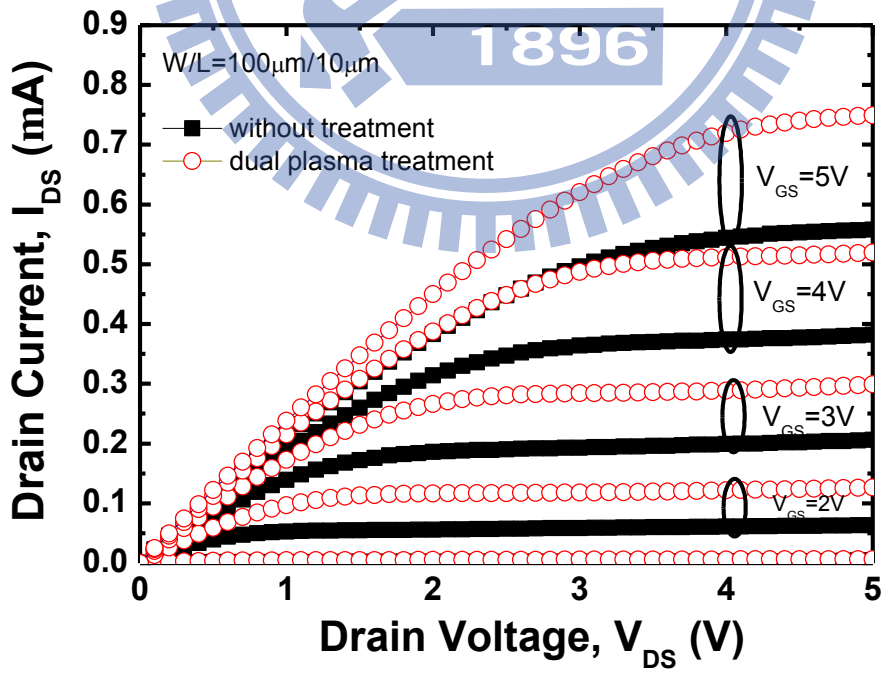


Fig. 4-7 The output characteristics (I_D-V_G) of HfO_2 LTPS TFTs with and without dual plasma treatment.

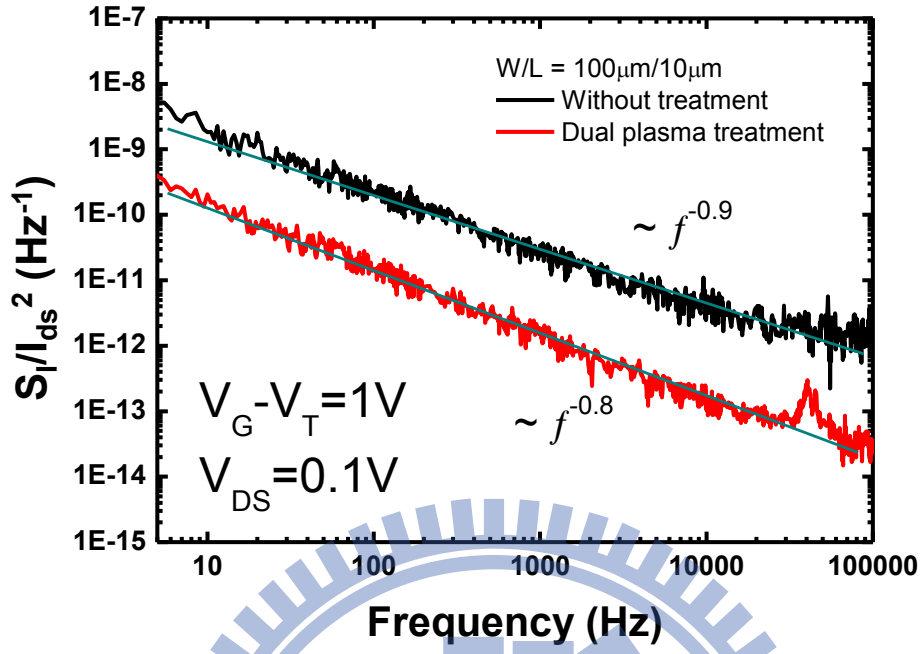


Fig. 4-8 S_{ID}/I_{ds}^2 of the HfO_2 LTPS TFTs with and without dual plasma treatment at V_{DS}=0.1V and V_G-V_T=1V.

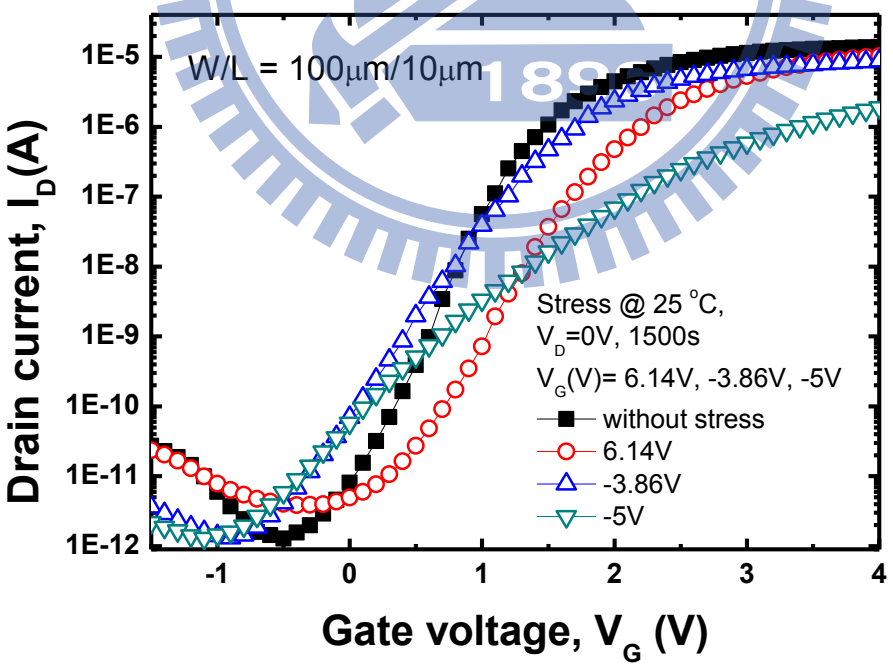


Fig. 4-9 The I_D-V_G characteristic of HfO_2 LTPS-TFT with dual plasma treatment before and after negative bias stress (NBS) and positive bias stress (PBS) with V_G = -5V, -3.86V, 0V, 6.14V and V_D = V_S = 0V for 1500 s at T = 25℃.

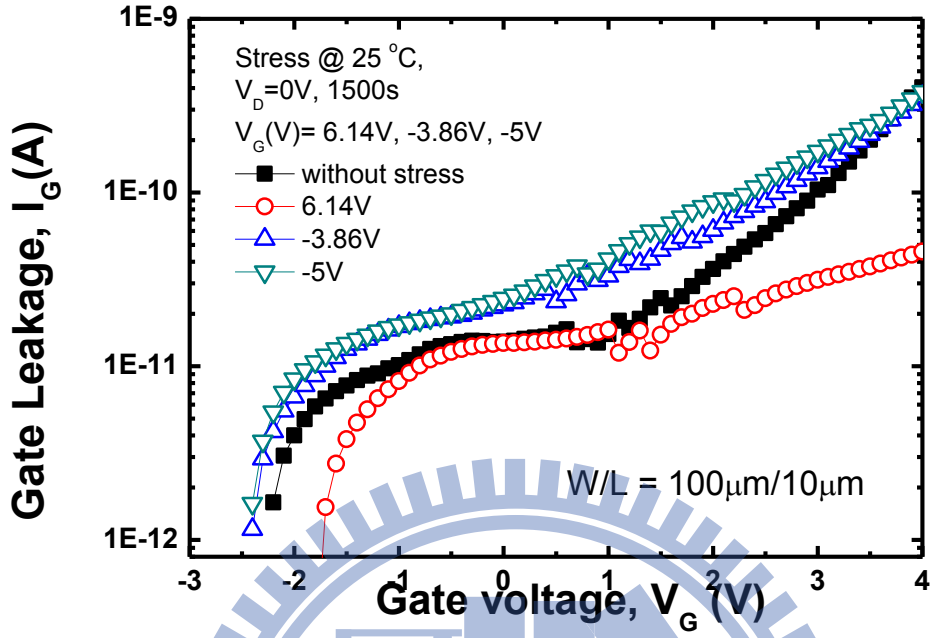


Fig. 4-10 The I_G-V_G characteristic of HfO_2 LTPS-TFT with dual plasma treatment before and after negative bias stress (NBS) and positive bias stress (PBS) with V_G = -5V, -3.86V, 0V, 6.14V and V_D = V_S = 0V for 1500 s at T = 25°C.

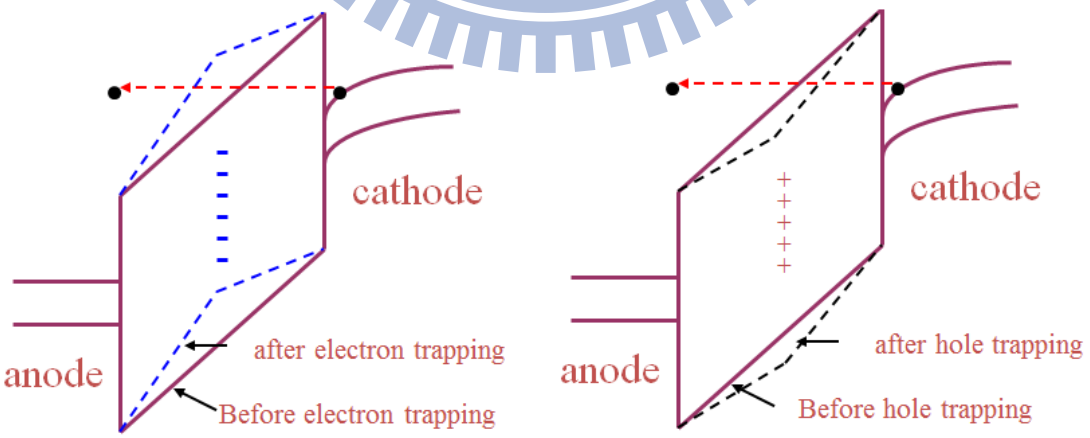


Fig. 4-11 The band diagram of the oxide after PBS and NBS.

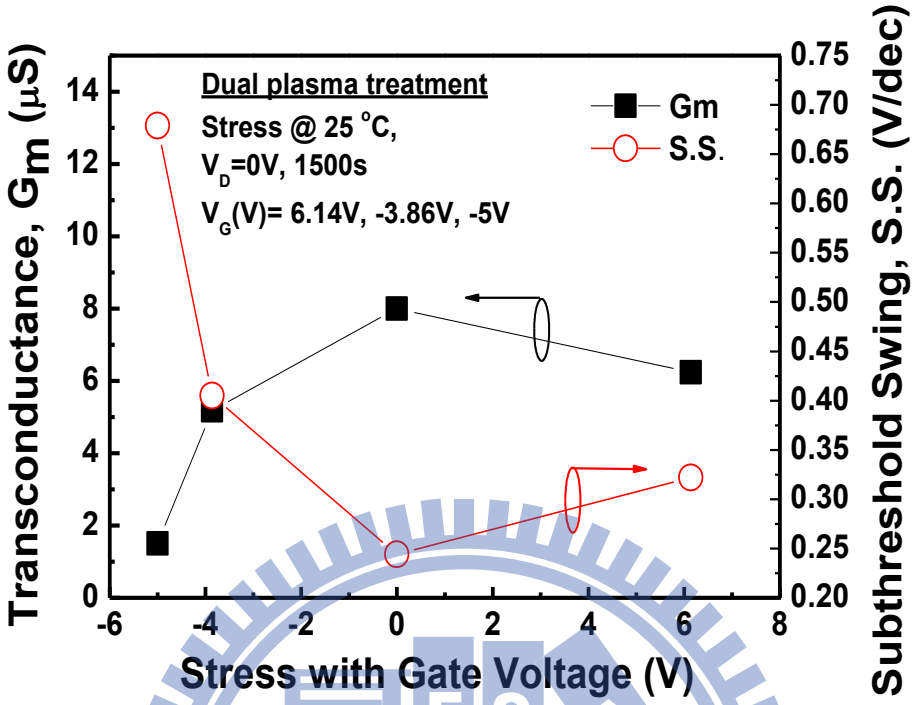


Fig. 4-12 Subthreshold swing S.S. and the transconductance G_m of the HfO_2 LTPS-TFT with dual plasma treatment before and after NBS and PBS.

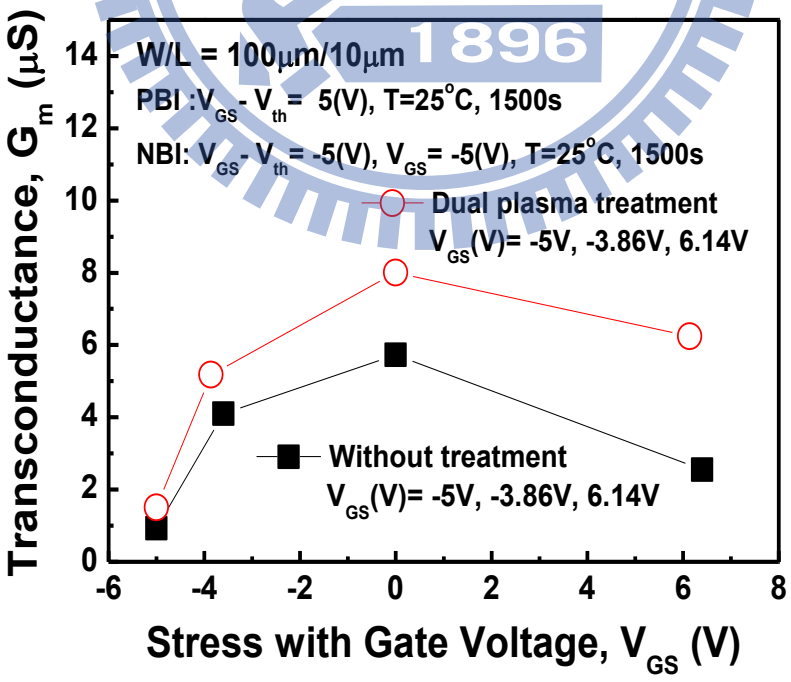


Fig. 4-13 The transconductance (G_m) of the HfO_2 LTPS-TFT with and without dual plasma treatment before and after NBS and PBS.

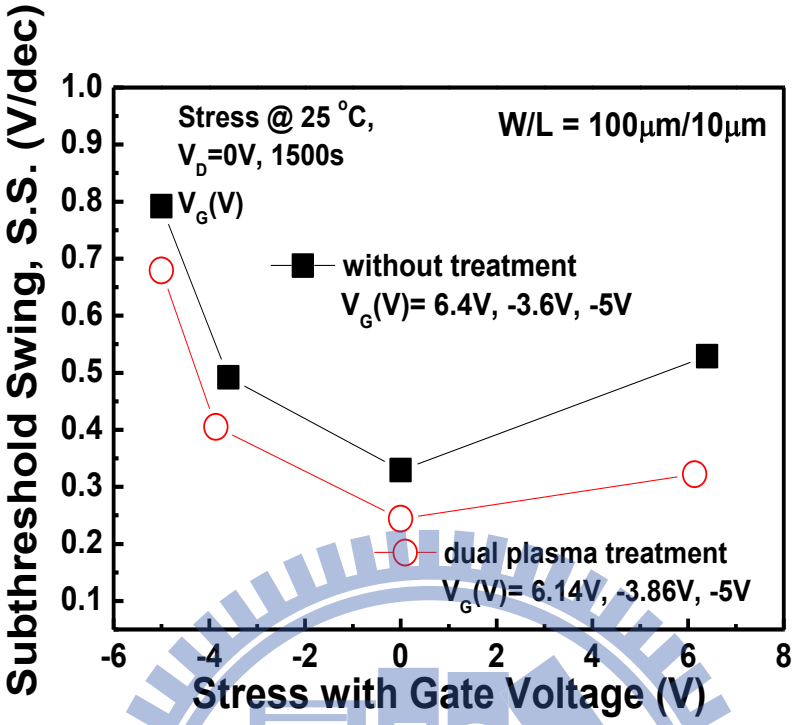


Fig. 4-14 The subthreshold swing (S.S.) of the HfO_2 LTPS-TFT with and without dual plasma treatment before and after NBS and PBS.

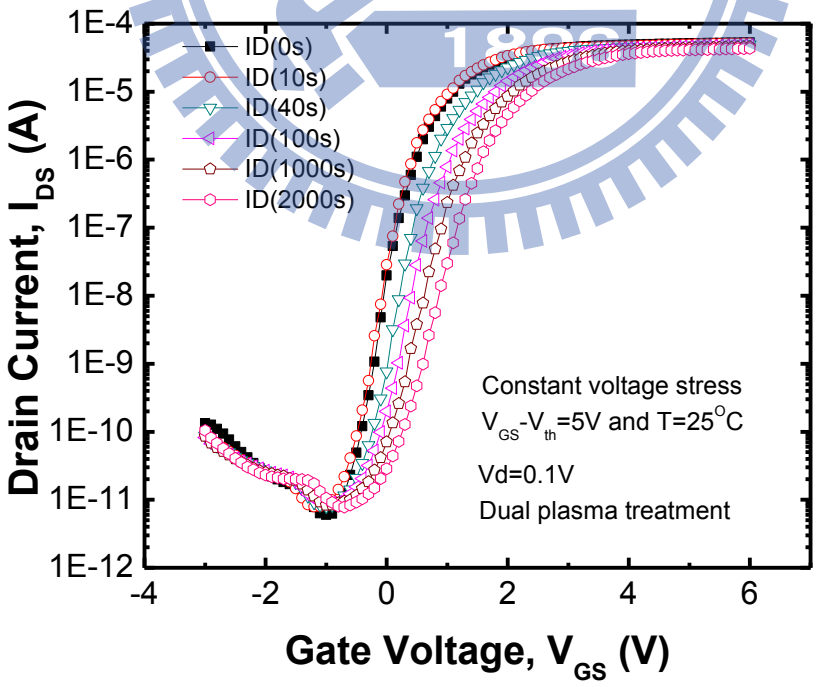


Fig. 4-15 The I_D versus V_G curves with stress time of n-type HfO_2 LTPS-TFT with dual plasma treatment under PBI stress with V_G-V_{TH} ~ 5V at T=25°C.

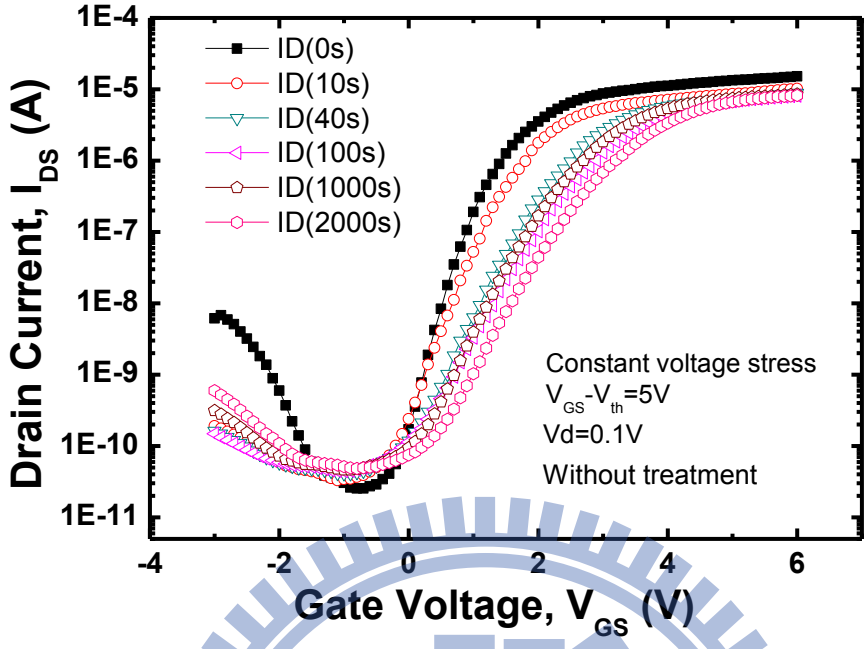


Fig. 4-16 The I_D versus V_G curves with stress time of n-type HfO_2 LTPS-TFT without plasma treatment under PBI stress with V_G-V_{TH} ~ 5V at T=25°C.

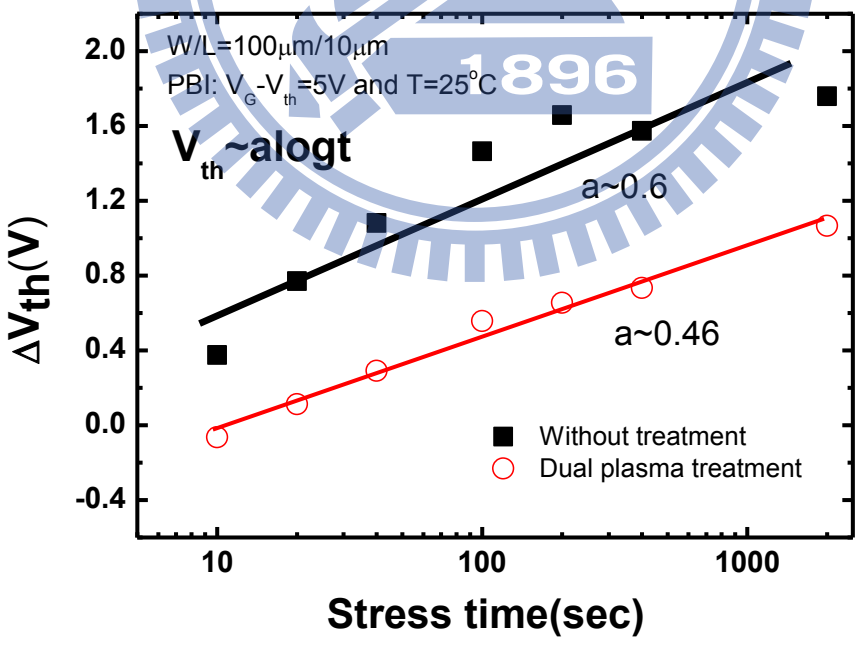


Fig. 4-17 Time evolutions of ΔV_{th} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBI stress at V_G-V_{TH} ~ 5V.

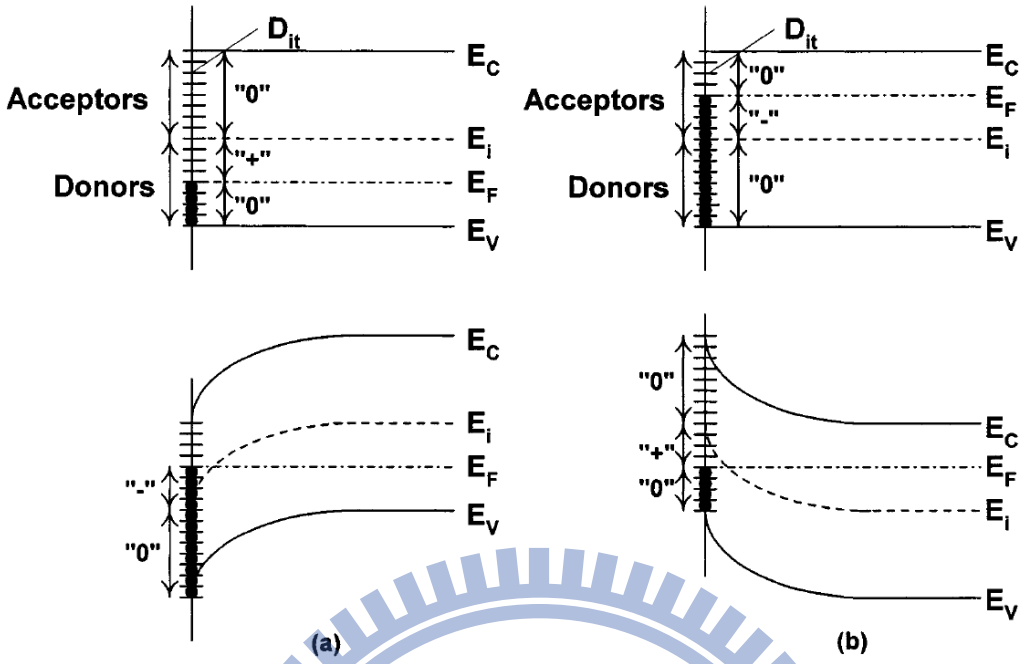


Fig. 4-18 Band diagrams of the Si substrate showing the occupation of interface states and different charge polarities when operating at inversion. (a) P-type substrate with positive interface charge at flatband and negative interface trap charge at inversion. (b) N-type substrate with negative interface charge at flatband and positive interface trap charge at inversion [32].

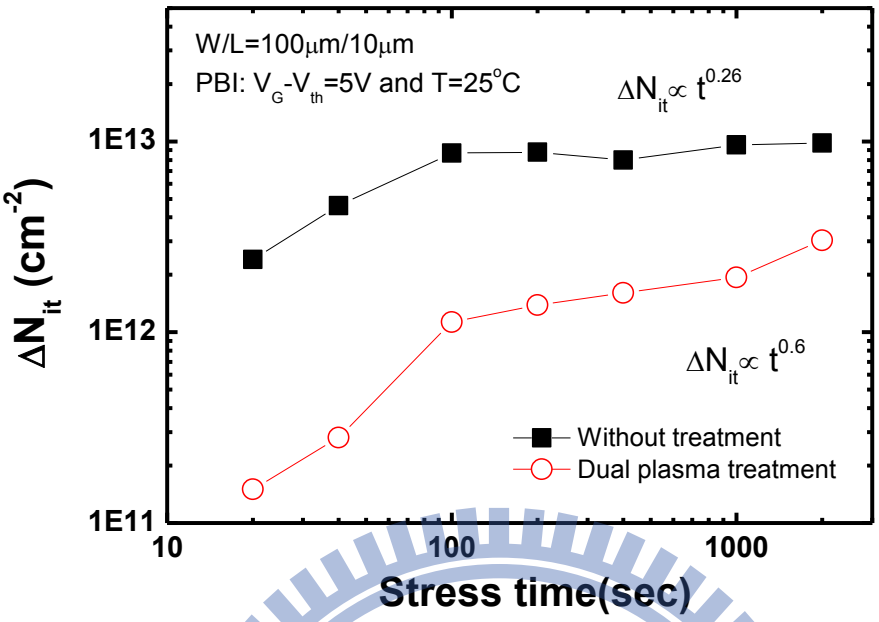


Fig. 4-19 Time evolutions of ΔN_{it} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBI stress at V_G-V_{TH} ~ 5V.

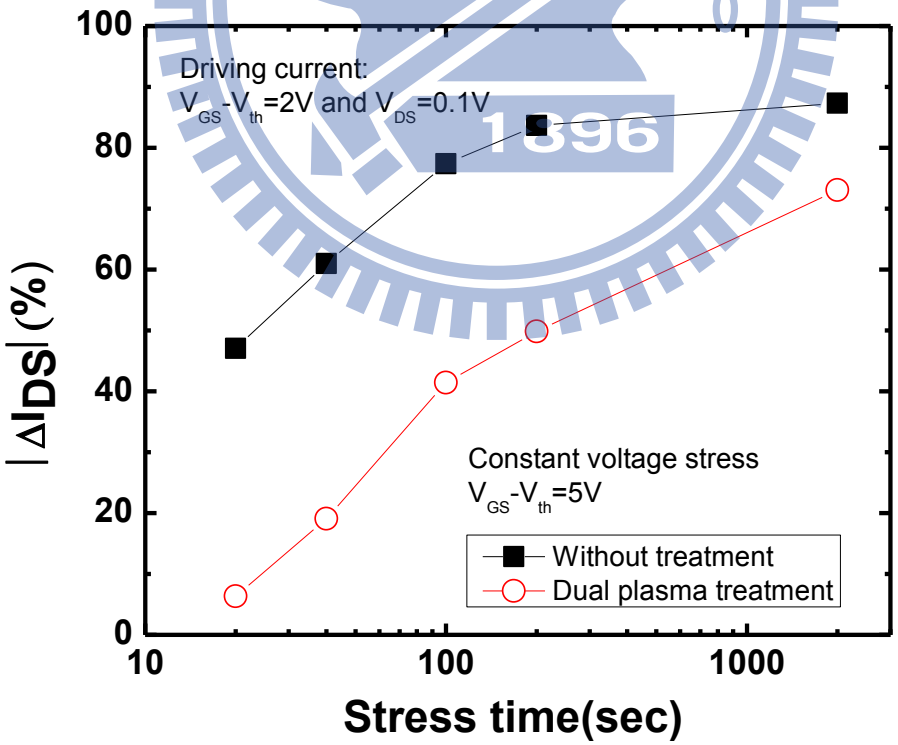


Fig. 4-20 The variations percentage of the drive current (ΔI_{DS}) under PBI stress.

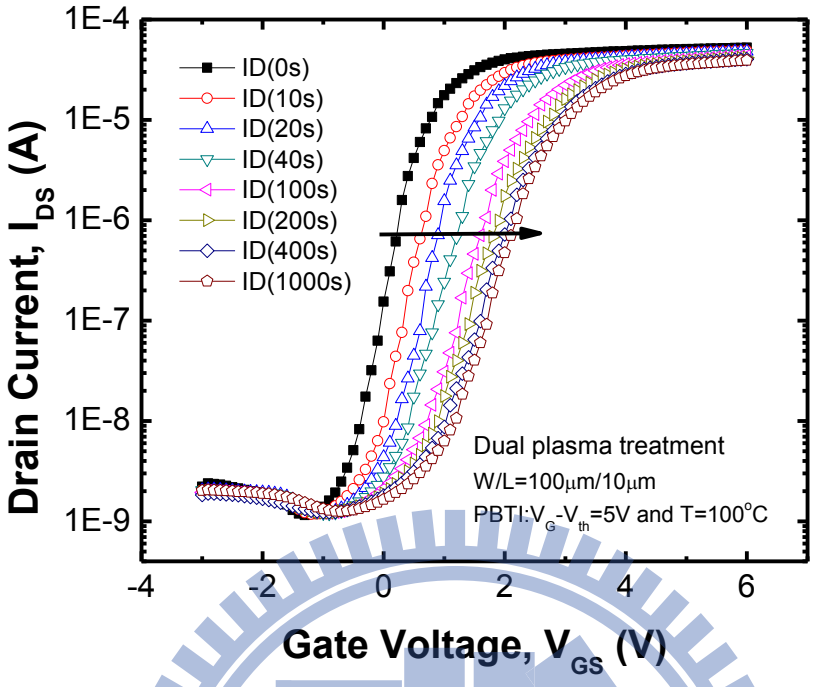


Fig. 4-21 The I_D versus V_G curves with stress time of n-type HfO_2 LTPS-TFT with plasma treatment under PBTI stress with V_G-V_{TH} ~ 5V at T=100°C.

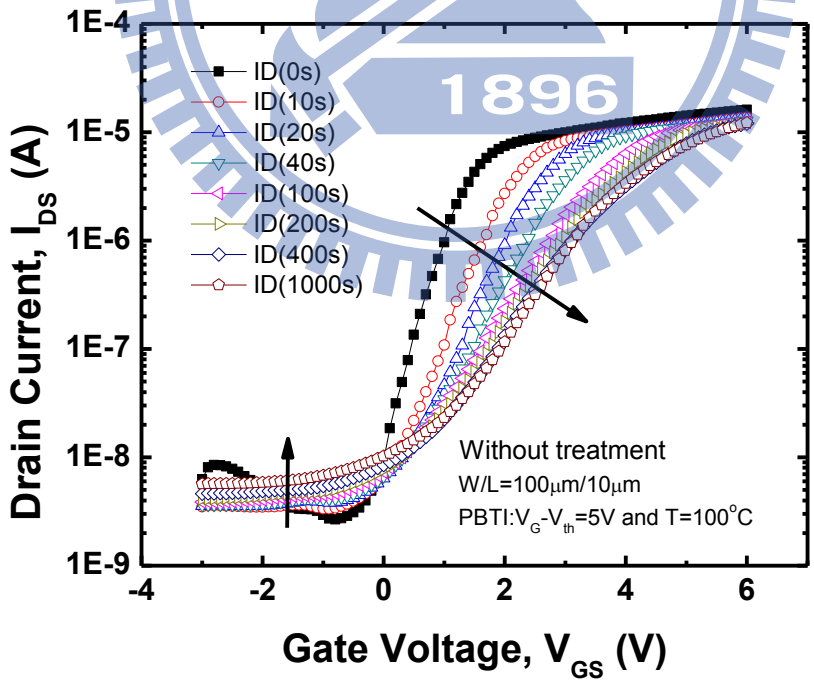


Fig. 4-22 The I_D versus V_G curves with stress time of n-type HfO_2 LTPS-TFT without dual plasma treatment under PBTI stress with V_G-V_{TH} ~ 5V at T=100°C.

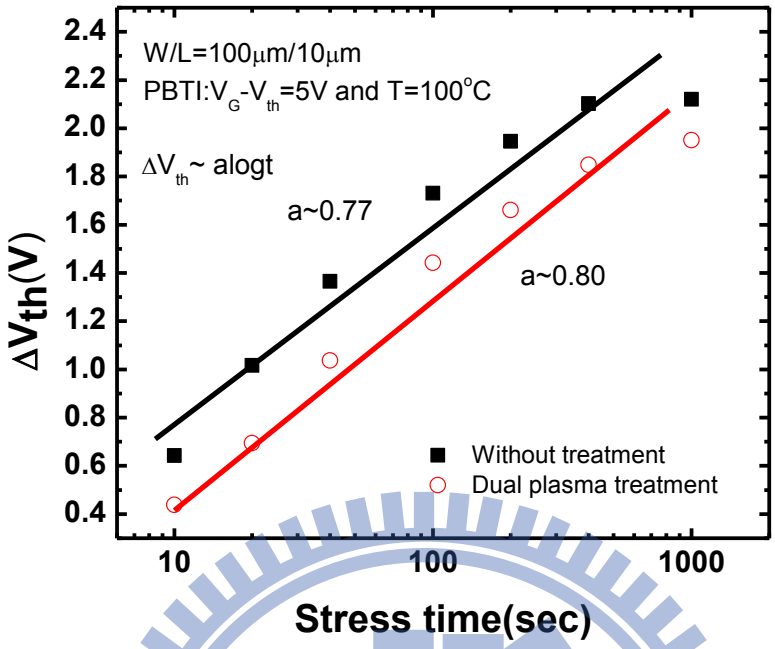


Fig. 4-23 Time evolutions of ΔV_{th} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBTI stress with V_G-V_{TH} ~ 5V at T=100°C

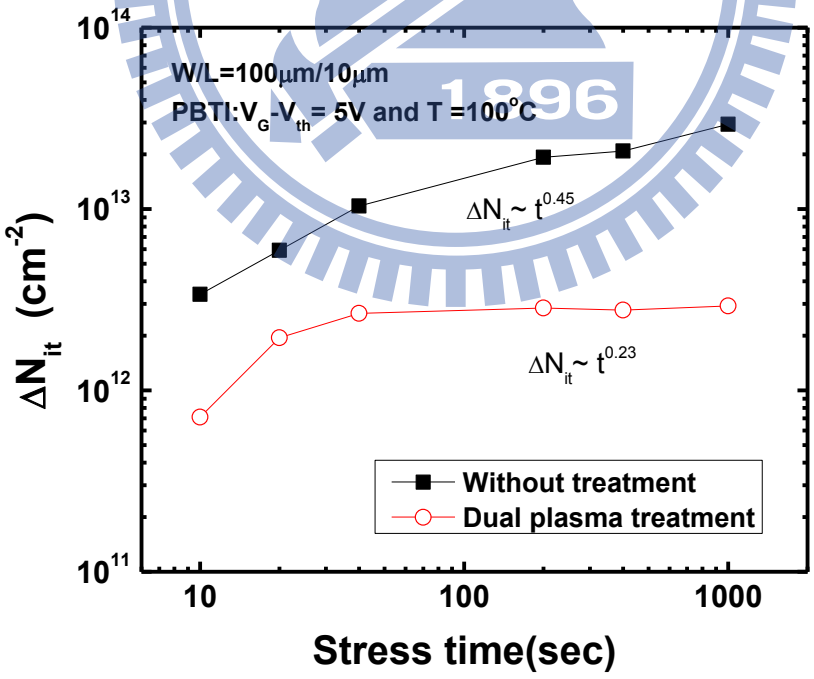


Fig. 4-24 Time evolutions of ΔN_{it} for n-type HfO_2 LTPS-TFT with and without plasma treatment under PBTI stress with V_G-V_{TH} ~ 5V at T=100°C

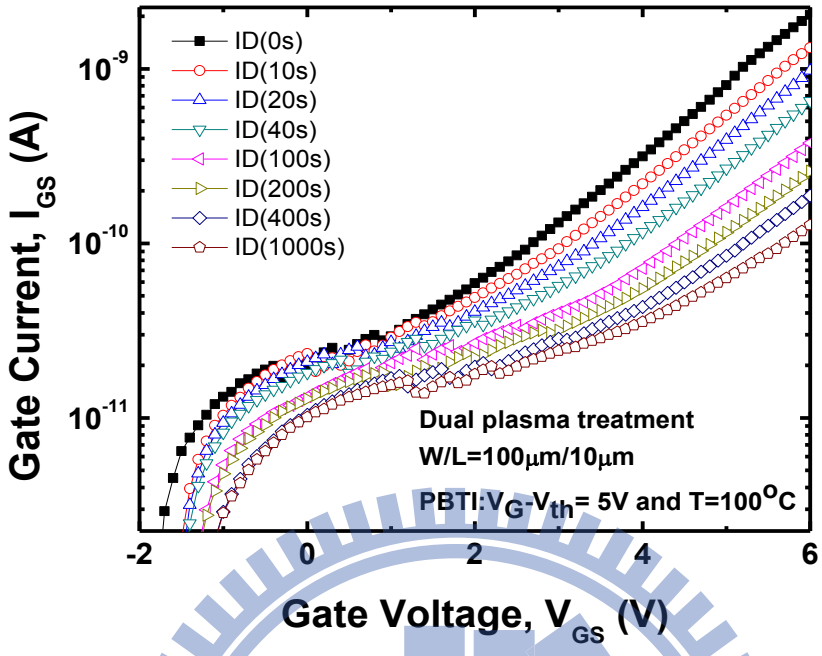


Fig. 4-25 The gate leakage current with stress time for n-type HfO_2 LTPS-TFT with dual plasma treatment under PBTI stress with V_G-V_{TH} ~ 5V at T=100°C.

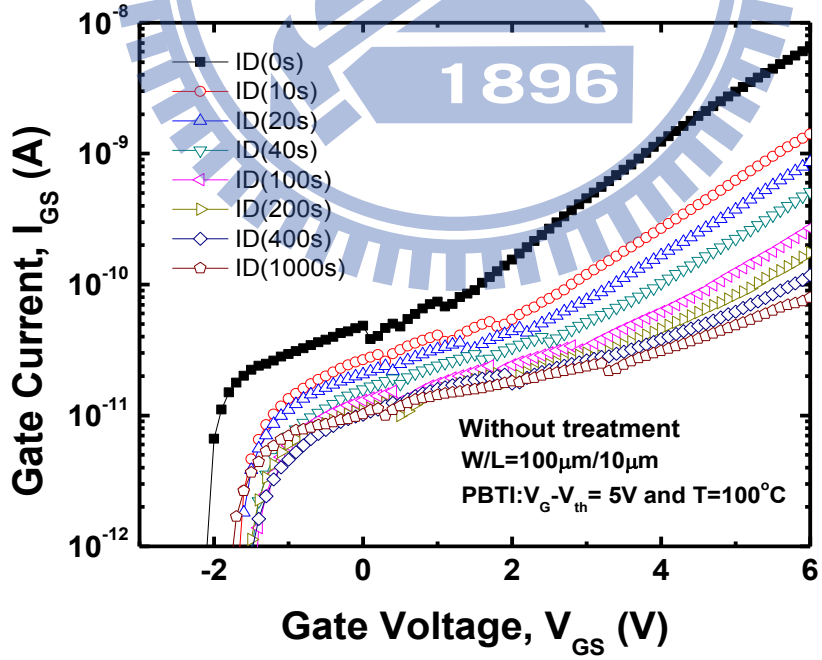


Fig. 4-26 The gate leakage current with stress time for n-type HfO_2 LTPS-TFT without plasma treatment under PBTI stress with V_G-V_{TH} ~ 5V at T=100°C.

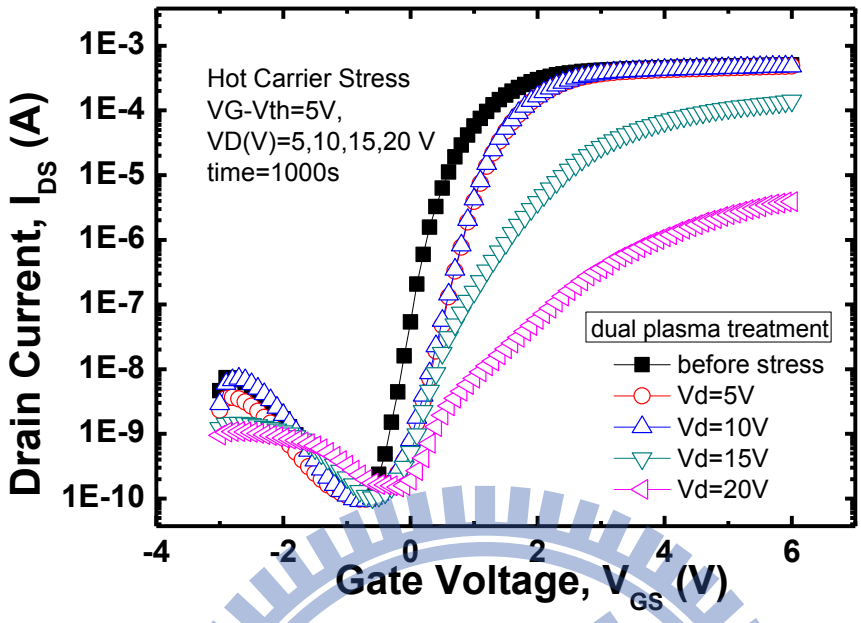


Fig. 4-27 I_D-V_G curves of the dual plasma sample stressed in different drain voltages (5-20V) with V_G-V_T=5V for 1000 sec.

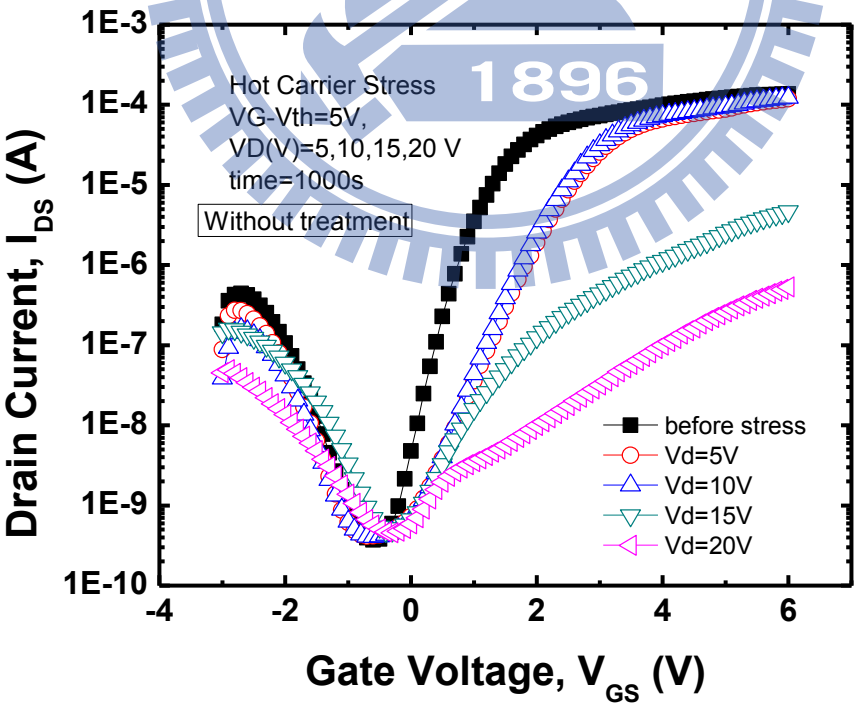
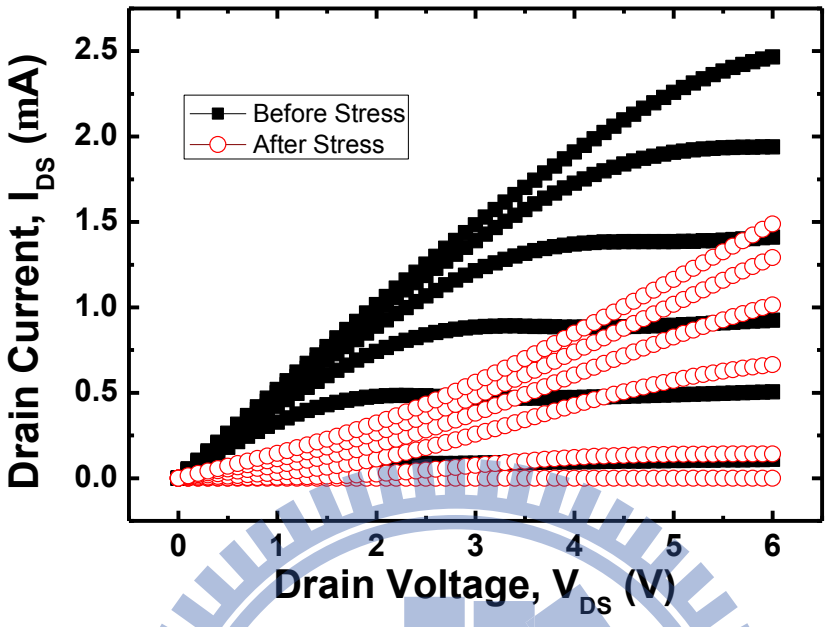
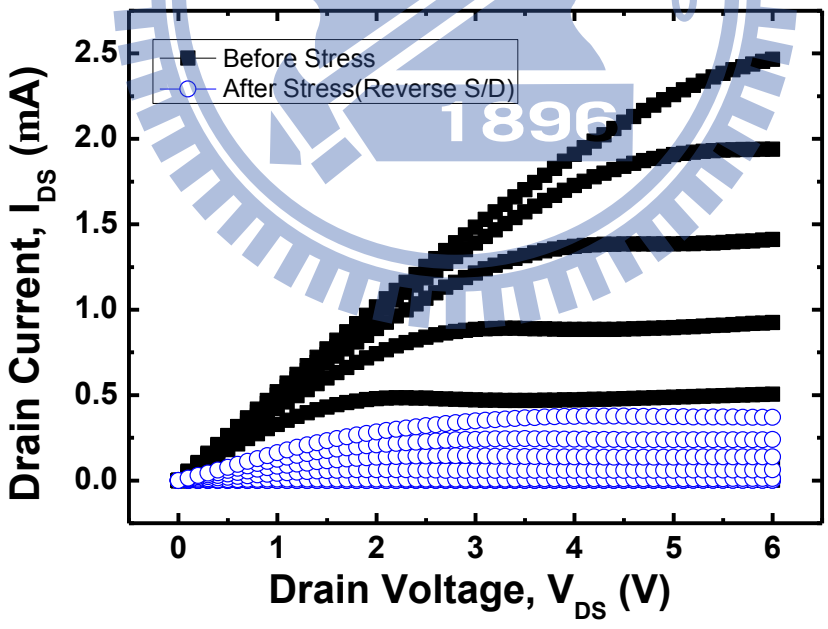


Fig. 4-28 I_D-V_G curves of the control sample stressed in different drain voltages (5-20V) with V_G-V_T=5V for 1000 sec.



(a)



(b)

Fig. 4-29 The output characteristics of the dual plasma sample for (a) normal mode and (b) reverse mode after HCS 1000s with V_{GS}-V_{th}=5V and drain bias 15V.

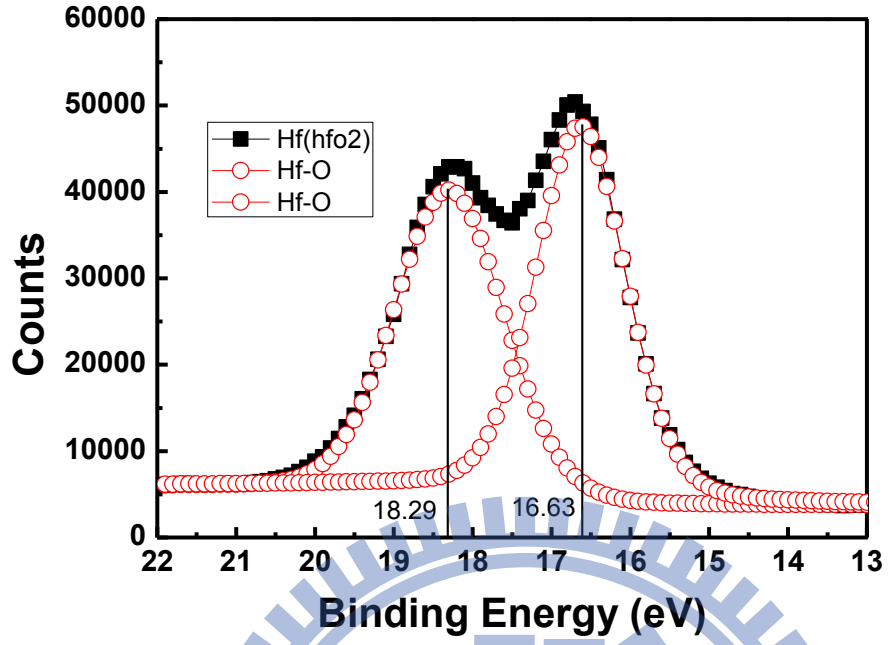


Fig. 4-30 The Hf 4f ESCA spectra of the HfO_2 LTPS-TFT without plasma treatment.

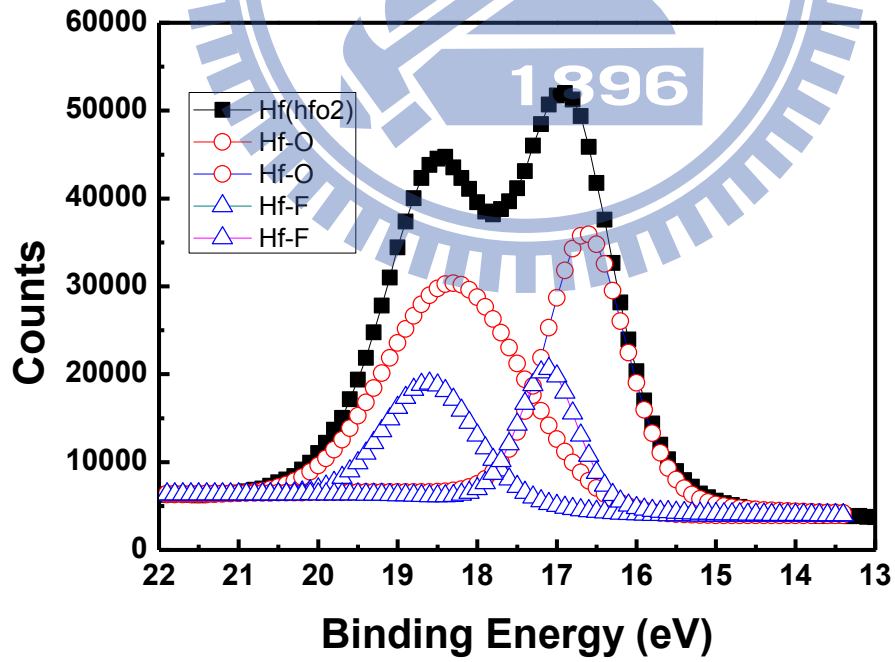


Fig. 4-31 The Hf 4f ESCA spectra of the HfO_2 LTPS-TFT with dual plasma treatment.

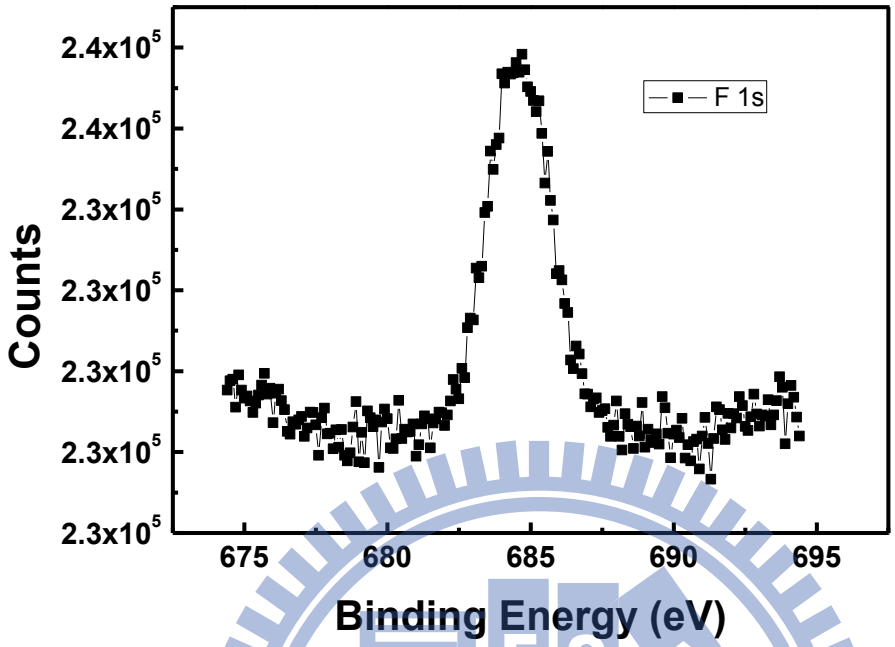


Fig. 4-32 The F 1s ESCA spectra of the HfO_2.

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Chapter 5

Conclusion and Suggestion for future work

5.1 Conclusion

In this dissertation, we have applied dual plasma treatment on MIS capacitor and Low-Temperature Polycrystalline-Silicon (LTPS) Thin Film Transistors (TFTs) with high-κ gate dielectric. In high-κ gate dielectric MIS capacitor, the characteristics of capacitance-voltage (C-V) and current-voltage (J-V) have been briefly described. Second, the frequency dispersion and constant voltage stress (CVS) characteristics of the samples will be analyzed to estimate the improvement. Finally, current conduction mechanisms, such as Schottky emission, Frenkel-Poole (F-P) emission, and Fowler-Nordheim (F-N) tunneling have been discussed. Schottky barrier height, F-P barrier height, and F-N barrier height have been extracted. On the other hand, for high-κ gate dielectric LTPS-TFTs, the electrical improvements have been studied, including the hysteresis and the I-V characteristics. The device parameters, such as Vth, S.S., G_m, μ_{eff}, D_{it}, and N_{trap} have been extracted to study the improvement effect.

In chapter 2, the reliability properties and current conduction mechanisms of HfO_2 gate dielectric films as a function of dual plasma treatment (the combination of CF_4 pre-treatment and nitrogen post-treatment) have been investigated. First, the best conditions which decided form C-V and J-V characteristics were the samples treated by CF_4 plasma for 10 sec and N_2 (NH_3) plasma for 120 sec. According to the current

conduction analysis, the dominant current conduction mechanism was Schottky emission type in the region of low to medium electric fields (1.7 – 3.0 MV/cm); Frenkel-Poole (F-P) emission operated in the region of medium to high fields (4.0 – 6.0 MV/cm); Fowler-Nordheim (F-N) tunneling was dominant at high fields (> 7 MV/cm). Dual plasma treatment was effective in improving interface quality, eliminating shallow trap levels, and enhancing reliability properties. In summary, the effect of dual plasma treatment could be better than single plasma treatment and dual plasma treatment would be an effective technology to improve the reliability of HfO_2 thin films.

In chapter 3, the interface quality and reliability properties of $HfAlO_x$ gate dielectric with dual plasma have been verified. Based on above results, the electrical characteristics including C-V, I-V, hysteresis, frequency dispersion, and CVS characteristics of HfAlOx gate dielectrics could be great improved by dual plasma treatment. According to our study, the best condition is CF_4 pre-treatment for 10 sec and N_2 (NH_3) post-treatment for 90 sec time. Based on the current conduction analysis, the dominant current conduction mechanism was Schottky emission type in the region of low to medium electric fields; Frenkel-Poole (F-P) emission operated in the region of medium to high fields; Fowler-Nordheim (F-N) tunneling was dominant at high fields. In conclusion, dual plasma treatment could improve interface quality and enhance reliability properties of $HfAlO_x$ thin films.

In chapter 4, the dual plasma treatment is successfully utilized on the LTPS-TFTs. The electrical improvement has been studied, including the hysteresis and the I-V characteristics. The device parameters, such as V_{th}, S.S., G_m, μ_{eff}, D_{it}, and N_{trap} are extracted to verify the improvement effect. It shows that the dual plasma samples have better electrical characteristics. Also, according to the 1/*f* noise (or flicker noise)

measurement, dual plasma treatment could effectively reduce the grain-boundary trap-state densities at the channel and the oxide traps at the oxide/poly-Si interface. Furthermore, the reliability properties and mechanisms of high performance HfO_2 gate dielectric LTPS-TFT with dual plasma treatment are investigated, including PBS, NBS, and HCS. Also, the damage region induced by HCS is distinguished by the normal mode and reverse mode (S/D reverse) operation. In conclusion, the sample with dual plasma treatment has better stress immunity than the sample without treatment.

5.2 Suggestion for future work

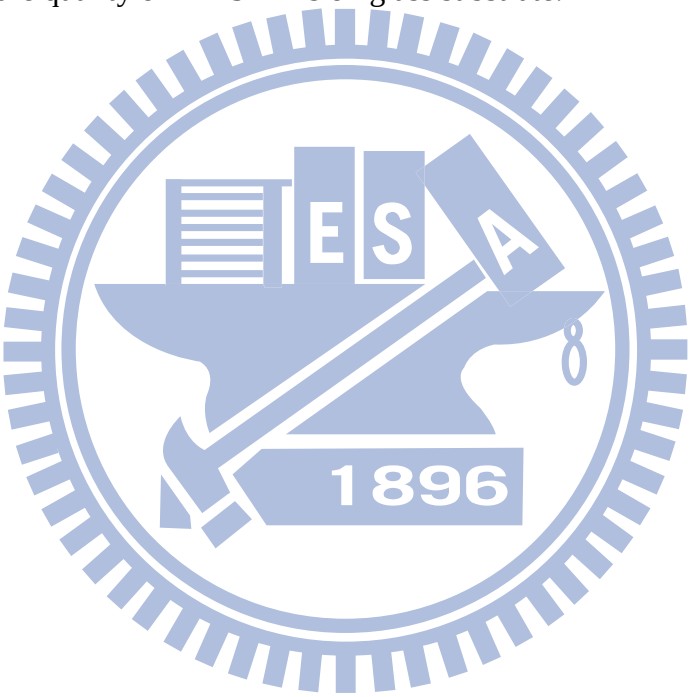
In this dissertation, dual plasma treatment technology has been applied on MIS capacitor and Low-Temperature Polycrystalline-Silicon (LTPS) Thin Film Transistors (TFTs) with high-κ gate dielectric. The effect of dual plasma treatment on devices has been studied, including the electrical characteristics and reliability properties. Even so, there are some topics could be studied in the future:

1. Since the dual plasma treatment has been utilized on LTPS-TFTs in this dissertation, we could integrate the dual plasma treatment on novel devices in CMOS technology, such as Si-based MOSFET, Ge-based MOSFET, nanowire MOSFET, and FinFET et al.

2. In our experiment, the high-κ dielectric film was deposited by MOCVD system or Dual E-gun system. However, the ALD system is another technology to deposit high-κ dielectrics. We could utilize ALD system to deposit high-κ thin film.

3. We could integrate silicide (NiSi) process as S/D of device to reduce the parasitic resistance. Besides, tradition junction formation at S/D requires high temperature annealing (i.e. 900~1000 ^{o}C). This high temperature process will make the high-κ dielectric crystallized. Therefore, we could combine implant to silicide (IIS) method to achieve low temperature dopant activation.

4. In our experiment, the TFTs were fabricated on the silicon substrate capped the thermal oxide layer. Hence, the dual plasma technology could be used for improving the quality of LTPS TFTs on glass substrate.



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博士論文題目:

中文: 雙重電漿處理技術應用於具高介電常數閘極絕緣層的金屬-絕緣層-半導體電容及低溫多晶矽薄膜電晶體之特性研究

英文: **Investigation of Dual Plasma Treatment Technology on MIS Capacitor and Low Temperature Polycrystalline Silicon Thin Film Transistor with High-κ Gate Dielectric**