國立交通大學

電子工程學系　電子研究所

碩士論文

鈦奈米晶體應用於非揮發性記憶體之製程研究

Research and Process Development of Titanium-based Nanocrystals for Nonvolatile Memory

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指導教授：施　敏　教授
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研究生：王派璿　　Student：

指導教授：施敏 博士　　Advisor：Dr. S. M. Sze

張鼎張 博士　　Advisor：Dr. Ting-Chang Chang

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摘要

非揮發性記憶體(NVM)目前在元件尺寸持續微縮下的需求為高密度記憶單元、低功率損耗、快速讀寫操作、以及良好的可靠度(Reliability)。傳統浮動閘極(floating gate)記憶體在操作過程中如果穿隧氧化層產生漏電路徑會造成所有儲存電荷流失回到矽基板，所以在資料保存時間(Retention)和耐操度(Endurance)的考量下，很難去微縮穿隧氧化層的厚度。非揮發性奈米點記憶體被提出希望可取代傳統浮動閘極記憶體，由於奈米點可視為電荷儲存層中彼此分離的儲存點，可以有效改善小尺寸記憶體元件多次操作下的資料儲存能力。近年來發展了許多方法來形成奈米點，一般而言，大多數的方法都需要長時間高溫的熱製程，這個步驟會影響現階段半導體製程中的熱預算和產能。

在本文中，一個簡單的製程方法用來形成鈦（Titanium）奈米點，並應用於非揮發性記憶體。室溫下，共濺鍍(co-sputter)靶材 Ti 和介電質(如:SiO2 、Si、Ge)形成鈦系列相關奈米點的非揮發性記憶體結構，我們認為在退火過程中

形成奈米點，可以簡單並均匀地形成高密度（～10^{12}）的奈米點。我們發現高密度的鈦矽氧奈米點與鍺奈米點交互作用有較佳的儲存能力。此外，這個應用在非揮發性記憶體的製程技術同時也是適用於現階段積體電路製程。

Research and Process Development of Titanium-based Nanocrystals for Nonvolatile Memory

Student: 王派璿　　　　Advisor:　Dr. Ting-Chang Chang

Advisor：Dr. S. M. Sze

Department of Electronic Engineering and Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao Tung University

Abstract

Current requirements of nonvolatile memory (NVM) are the high density cells, low-power consumption, high-speed operation and good reliability for the scaling down devices. However, all of the charges stored in the floating gate will leak into the substrate if the tunnel oxide has a leakage path in the conventional NVM during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down in terms of charge retention and endurance characteristics. The nonvolatile nanocrystal memories are one of promising candidates to substitute for conventional floating gate memory, because the discrete storage nodes as the charge storage media have been effectively improve data retention under endurance test for the scaling down device. Many methods have been developed recently for the formation of nanocrystal.

Generally, most methods need thermal treatment with high temperature and long duration. This procedure will influence thermal budget and throughput in current manufacture technology of semiconductor industry.

In this thesis, we provide a easy fabrication technique of titanium nanocrystals for nonvolatile memory. The nonvolatile memory structure of Titanium nanocrystals embedded in the SiO_2 was fabricated by co-sputtering Titanium-Silicide and semiconductor material at room temperature. We consider that the nanocrystals formed in annealing process are simple and uniformly fabricated in our study. We found that TiSi2 add Ge to fabricate the nonvolatile memory can be obtained better storage effects. These fabrication techniques for the application of nanocrystal memory can be compatible with current manufacture process of the integrated circuit manufacture.

誌　　謝

本篇論文完成的同時，也代表著碩士生涯的告一段落，這一路走來，需要感謝的人很多，在此時我願以誠摯的心向你們各位說聲：「謝謝」。

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最後，給在天上的爸爸王興彪先生，謝謝你過去對我的付出使我能夠在此時完成完成我的碩士學習生涯了，還有最愛我的媽媽吳欲合女士、我摯愛的若琪、以及弟弟派瑜、妹妹筱君，謝謝你們這段時間在精神與生活上的支持與鼓勵，不斷地督促我讓我順利地完成這個碩士學位；這兩年來我投入大部分的心力在學業研究上，和家人相聚的時間變少，謝謝你們的體諒，也感謝若琪這兩年來對我的包容與照顧；最後，僅以此論文獻給你們。

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Chapter 1

Introduction

1.1 Overview of Nonvolatile Memory

Today, flash memory find wide applications and are considered as a technology driver for semiconductor industry in the next generation. It can be classified into two major markets: code storage application and data storage application. NOR type flash memory [1.1] is most suitable for code storage application, such as cellular phones, PC bios, and DVD player. NAND type flash memory [1.2] has been targeted at data storage market, which is an emerging application such as PDA, memory cards, MP3 audio players, digital cameras, and USB flash personal disc. These products all are based on flash memory that is nonvolatile and can keep stored information also when the power supply is switched off. Flash memory also has exhibited several advantages, such as the ability to be electrical programmed and fast simultaneous block electrical erased in a single-cell, smallest cell size to achieve highest chip density, and good flexibility [1.3-1.4]. In addition, the flash memory fabrication process is compatible with the current CMOS process and is a suitable solution for embedded memory applications. Therefore, flash memories are easily scalable replacements for EPROMs (Erasable Programmable Read Only Memory) and EEPROMs (Electrically Erasable Programmable Read Only Memory). Since flash memory possesses these key advantages, it has become the mainstream nonvolatile memory device nowadays.

In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs [1.5]. The conventional floating-gate device structure is shown in Fig. 1-1. The FG acts as the storing electrode and is electrically governed by a capacitively coupled control gate (CG). Charge injected in the FG is maintained there, allowing the difference between threshold voltages of the cell transistor for nonvolatile memory application.

Recently, nonvolatile memory devices are moving toward high density memory array, low cost, low power consumption, high-speed operation, and good reliability. Although conventional flash memory does not require refreshing and thus consumes less power and achieves much higher array density with a stacked floating gate structure. However, floating-gate flash memory is much slower to operation and has poor endurance. In order to improve the write/erase speed of a floating-gate device, the thickness of the tunnel oxide must be reduced. But conventional FG memory devices have limited potential for aggressive scaling of the tunnel oxide thickness. The tunnel oxide must be thin enough to allow quick and efficient charge transport to and from FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to guarantee the data integrity for 10 years. For faster operation speed, thin tunnel oxide is desirable. However, it is desirable to increase the thickness of tunnel oxide for better isolation and reliability. So there is a trade-off between speed and reliability for the optimum tunnel oxide thickness. Currently, commercial flash memory devices use tunnel oxide thicker about 8-11 nm, which results in high programming voltage and slow programming speed [1.6].

To alleviate the tunnel oxide design trade-off for floating-gate memory devices, memory-cell structures employing discrete traps as charge storage media have been proposed. In the conventional floating gate flash memory, if there is one defect created in the tunnel oxide, all the charges stored on the floating-gate will leak back to the channel or the source/drain through the weak spots. Unlike conventional continuous floating gate, charges stored in discrete nodes cannot easily redistribute amongst themselves. Therefore, only a relatively small number of nodes near the oxide defects will be affected. Local charge storage in discrete nodes enables more aggressive scaling of the tunnel oxide by relieving the total charge loss concern. There are two promising candidates, SONOS [1.7-1.9] and nanocrystal nonvolatile memory devices [1.10-1.12], that have been demonstrated to lead to an improvement in retention time compared with conventional floating gate memory. Hence the tunnel oxide thickness can be reduced to allow faster programming and lower voltage operation.

1.1.1 SONOS Nonvolatile Memory Devices

The first nitride-base devices is metal-gate nitride device MNOS (Metal/Nitride/Oxide/Silicon) which was reported in 1967 by Wegener et al [1.13]. However, it is well known that silicon nitride film contains many carrier traps which cause threshold voltage shift. Then the silicon nitride trap-based devices are extensively studied for charge storage device application in the early 70s. Fig. 1-2 illustrates the progression of device cross section, which has led to the present SONOS device structure. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel SNOS devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. The advantages of the ONO triple dielectric structure are: (1) lower programming voltage since the blocking action of the top oxide removes any limitation on the reduction of the nitride thickness; (2) charge injection from and to the gate electrode is minimized for both gate polarities, particularly for hole injection; (3) improved memory retention since there is minimal loss of charge to the gate electrode.

The SONOS (poly-Silicon-Oxide-Nitride-Oxide-Silicon) memory devices, as shown in Fig. 1-3, have attracted a lot of attention due to its advantages over the traditional floating-gate flash device. These include reduced process complexity, high speed operation, lower voltage operation, improved cycling endurance, and elimination of drain-induced turn-on [1.14-1.16]. The main difference between floating-gate and SONOS structure is the method of charge storage. The charge storage media in the floating-gate structure is the conducting polysilicon floating-gate electrode. In the SONOS memory structure, charges are stored in the physical discrete traps of silicon nitride dielectric. A typical trap has a density of the order 10^{18}-10^{19} cm^{-3} according to Yang et al [1.17] and stores both electrons and holes injected from the channel. The charges cannot move freely between the discrete trap locations, hence the SONOS memory device is very robust against the defects inside the tunnel oxide and has good endurance.

The SONOS memory devices still face challenge in the future for high density nonvolatile memory application, which requires low voltage (< 5V), low power consumption, long-term retention, and superior endurance. Various approaches have been proposed for improving the SONOS performance and reliability. Chen *et al.* demonstrated a Si_3N_4 bandgap engineering (BE) control method for better endurance and retention. A nitride with varied relative Si/N ratio throughout the film has increased the charge-trapping efficiency significantly [1.18]. Tan *et al.* showed that over-erase phenomenon in SONOS memory structures can be minimized by replacing silicon nitride with HfO_2 as the charge storage layer. The charge retention and endurance performance is improved by the addition of 10% Al_2O_3 in HfO_2 to form HfAlO, while maintaining the over-erase resistance of HfO_2 [1.19]. She *et al.* demonstrates that high-quality nitride is applied as the tunnel dielectric for a SONOS-type memory device. Compared to control devices with SiO_2 tunnel dielectric, faster programming speed and better retention time are achieved with low programming voltage [1.20]. Lee *et al.* presents a device structure of SiO_2/SiN/Al_2O_3 (SANOS) with TaN metal gate. It is demonstrated that the use of TaN metal gate blocks electron current through Al_2O_3 layer more efficiently than a conventional polysilicon gate, resulting in faster program/erase speed and significant decrease of the saturation level of the erase V_T [1.21].

Chen *et al.* studies a polycrystalline silicon thin-film transistor (poly-Si TFT) with oxide/nitride/oxide (ONO) stack gate dielectrics and multiple nanowire channels for the applications of both nonvolatile silicon-oxide-nitride-oxide-silicon (SONOS) memory and switch transistor [1.22]. The proposed NW SONOS-TFT exhibits superior memory device characteristics with high program/erase efficiency and stable retention characteristics at high temperature. Such a SONOS-TFT is thereby highly promising for application in the future system-on-panel display applications.

New device structures are also indispensable in making flash memory more scalable. Since SONOS flash memory offers a thinner gate stack than floating gate flash memory, and a FinFET structure controls the short channel effect much better than a bulk structure. It has been demonstrated that the FinFET SONOS flash memory devices with a much smaller cell size can provide both excellent performance and reliability. Therefore, FinFET SONOS memory has potential to become the candidate for the next generation flash memory [1.23-1.24].

1.1.2 Nanocrystal Nonvolatile Memory Devices

Nanostructure nonvolatile memories are first introduced in the early 1990s. IBM researchers first proposed flash memory with a granular floating gate made out of silicon nanocrystals [1.25]. Fig. 1-4 illustrates conventional nanocrystal nonvolatile memory (NVM) device structures. It is observed that the nanocrystals are separated from each other within the gate dielectric. The term “nanocrystal” refers to a crystalline structure with a nanoscale dimension and its electronic properties seem more similar to an atom or molecule rather than the bulk crystal. For a nanocrystal NVM device, the charge storage media is in the form of mutually isolated nanocrystals instead of the continuous polysilicon layer. The limited size and capacitance of nanocrystals limit the numbers of stored electron, collectively the stored charges screen the gate charge and control the channel conductivity of the memory transistor.

Nanocrystal-based NVM devices have recently received much attention due to their potential to overcome the limitations of conventional polysilicon-based flash memory. Using nanocrystals as charge storage media offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing non-volatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results from the local charge storage in discrete nodes, which makes the storage more fault-tolerant and immune to the leakage caused by localized oxide defects. Further, the lateral charge migration effect between nanocrystals can be suppressed by the strongly isolation of surrounded dielectric. There are other important advantages though. First, nanocrystal memories use a more simplified fabrication process as compared to conventional stacked-gate FG NVM’s by avoiding the fabrication complications and costs of a dual-poly process. Second, due to the absence of drain to FG coupling, nanocrystal memories suffer less from drain-induced-barrier-lowering (DIBL) and therefore have intrinsically better punch-through characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time [1.26]. Alternatively, it allows the use of shorter channel lengths and therefore smaller cell area. Finally, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the distributed nature of the charge storage in the nanocrystal layer.

Research in this regime has focused on the development of fabrication processes and nanocrystal materials, and on the integration of nanocrystal-based storage layers in actual memory devices.

The fabrication of a nonvolatile memory cell requires a perfect control of four main parameters: (1) the tunnel oxide thickness, (2) the nanocrystal density, (3) the nanocrystal size, and (4) the control oxide thickness. An important consideration is the average size and aerial density of the nanocrystals. Larger-size nanocrystal array provides higher program/erase efficient due to small quantum confinement and coulomb blockade effects, and hence larger tunneling probability. However, it is desirable to reduce the nanocrystal size for better reliability (stress induced leakage during retention). So there is a trade-off between programming speed and reliability in selecting the nanocrystal size. A typical target is a density of at least 10^{12} cm^{-2}, and requires nanocrystal size of 5 nm and below. Moreover, good process control is needed with regards to such nanocrystal features as: planar nanocrystal layer; inter-crystal interaction (lateral isolation); and crystal doping (type and level). Finally, it is preferred that that the fabrication process is simple and that it uses standard semiconductor equipment.

After the first proposal of a memory transistor using silicon nanocrystals as floating gates. In order to improve the data retention in NVM, double layer Si nanocrystals memory has been investigated [1.27]. It seems interesting to use Ge nanocrystals rather than Si nanocrystals because of its smaller band gap. Indeed King and Hu have recently demonstrated the superior memory properties of Ge based nanocrystal memories over those based on Si [1.28]. Recently, germanium/silicon (Ge/Si) nanocrystals have been reported to possess superior charge retention capability than Ge or Si nanocrystals. This is due to the fact that Ge has a smaller band gap than Si and thus by introducing a Si interface around the Ge nanocrystal, it would create an additional barrier height at the Ge/Si interface which makes it harder for electrons to leak out of the nanocrystal [1.29,1.30]. Semiconductor nanocrystal memory may not be the ultimate solution to nonvolatile memory scaling, it still attracts a lot of attention now.

In optimizing nanocrystal NVM devices, the ideal goal is to achieve the fast write/erase of DRAM and the long retention time of Flash memories simultaneously. For this purpose we need to create an asymmetry in charge transport through the gate dielectric to maximize the $I_{G,\ Write/Erase}$/ $I_{G,\ Retention}$ ratio. One approach for achieving this goal is to engineer the depth of the potential well at the storage nodes, thus creating a small barrier for writing and a large barrier for retention between the substrate and the storage nodes. This can be achieved if the storage nodes are made of metal nanocrystals by engineering the metal work function. The major advantages of metal nanocrystals over semiconductor nanocrystals include higher density of states around the Fermi level, scalability for the nanocrystal size, a wide range of available work functions, and smaller energy perturbation due to carrier confinement [1.31]. In addition, an electrostatic modeling from both analytical formulation and numerical simulation is demonstrated that the metal nanocrystals will significantly enhance the electric field between the nanocrystal and the sensing channel set up by the control gate bias, and hence can achieve much higher efficiency in low-voltage P/E [1.32].

Toward better NVM device performance and reliability, numerous attempts have been made using metal nanocrystals. Liu *et al.* reported the growth of Au, Pt, and Ag nanocrystals on SiO_2 using an e-beam deposition method [1.31]. Lee *et al.* proposed a NVM structure using the Ni nanocrystals and high-*k* dielectrics [1.33]. Chen *et al.* present the stacked Ni silicide nanocrystal memory was fabricated by sputtering a comix target followed by a low temperature RTO process [1.34]. W nanocrystals on atomic-layer-deposited HfAlO/Al_2O_3 tunnel oxide were presented for application in a memory device [1.35]. Using W nanocrystal double layers embedded in HfAlO to enhancement of memory window was demonstrated from the short channel devices down to 100nm [1.36]. Tang *et al* demonstrate that a chaperonin protein lattice can be used as a template to assemble PbSe and Co nanocrystal arrays for Flash memory fabrication. This provides a new approach to achieve a high density and good distribution uniformity nanocrystal array [1.37].

In the future, the primary drivers behind nanocrystal memories are the potential to scale the tunnel oxide thickness, resulting in lower operating voltages, and the simplicity of a single poly-silicon process. But there are still challenges await nanocrystal memories in the long road to commercialization. Nanocrystal memories have yet to deliver on most of their promises. In fact, part of the voltage gain is offset because of the poor control gate coupling. For fabrication processes, it is hard to control the uniformity of the nanocrystal size and their physical locations in the channel. It is not a surprise that nanocrystal memories exhibit large device-to-device variation. Moreover, it has yet to be demonstrated that both the nominal and the statistical retention behavior are sufficient to meet true non-volatility requirements. Although single-dot memories have been demonstrated [1.38,1.39], but a more fundamental understanding of the scaling limits of nanocrystal memories is necessary, concentrating especially on the aspect of controlling channel conductance when relying on only a few discrete charge centers [1.40]. Finally, in order for that to happen, their claimed benefits will need to be more unambiguously substantiated, and a more appealing bundle of memory features will have to be demonstrated.

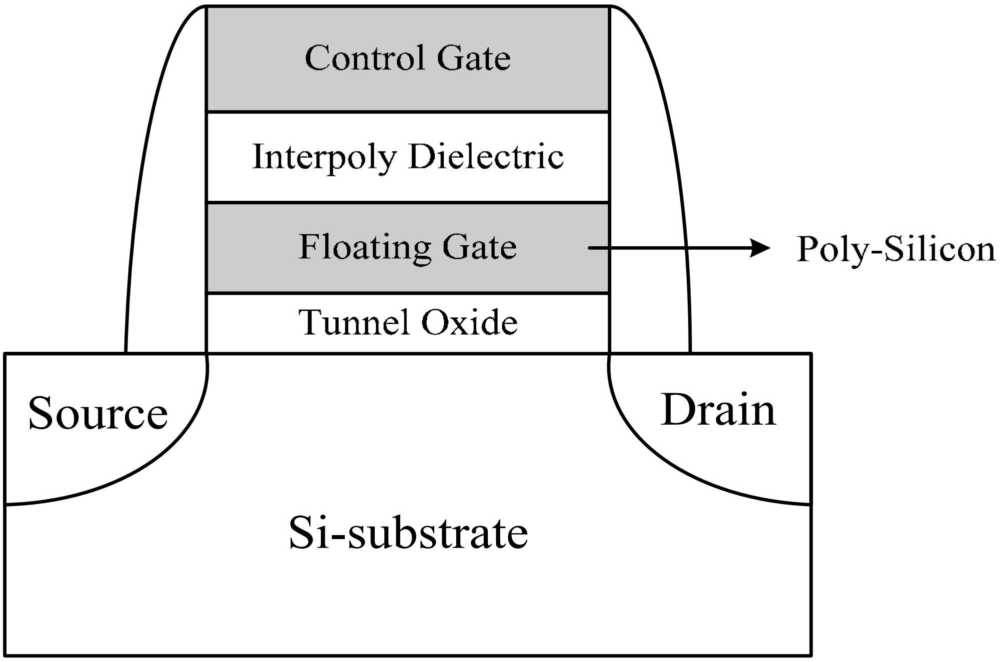
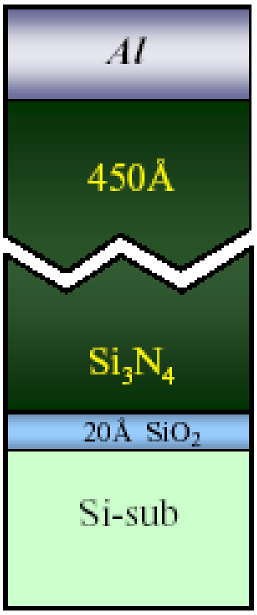
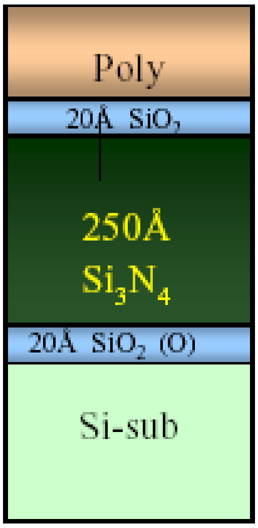


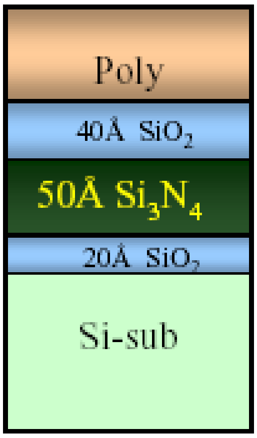
Figure 1-1 The structure of the conventional floating-gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.



MNOS
1960s~1970s



SNOS
1970s~1980s



SONOS
1980s ~

Figure 1-2 The development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

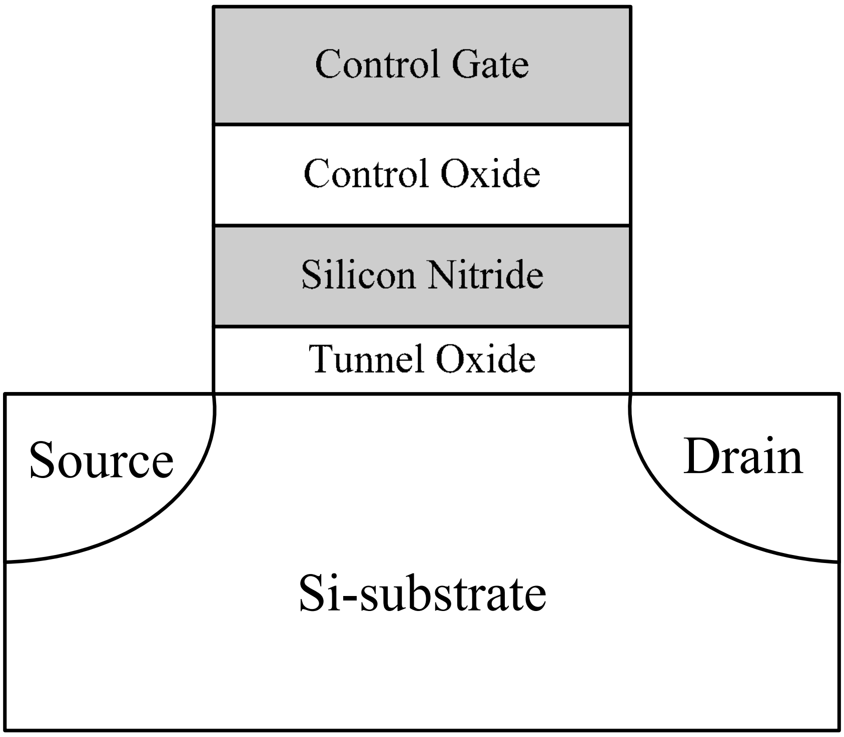


Figure 1-3 The structure of the SONOS nonvolatile memory device. The nitride layer is used as the charge trapping media.

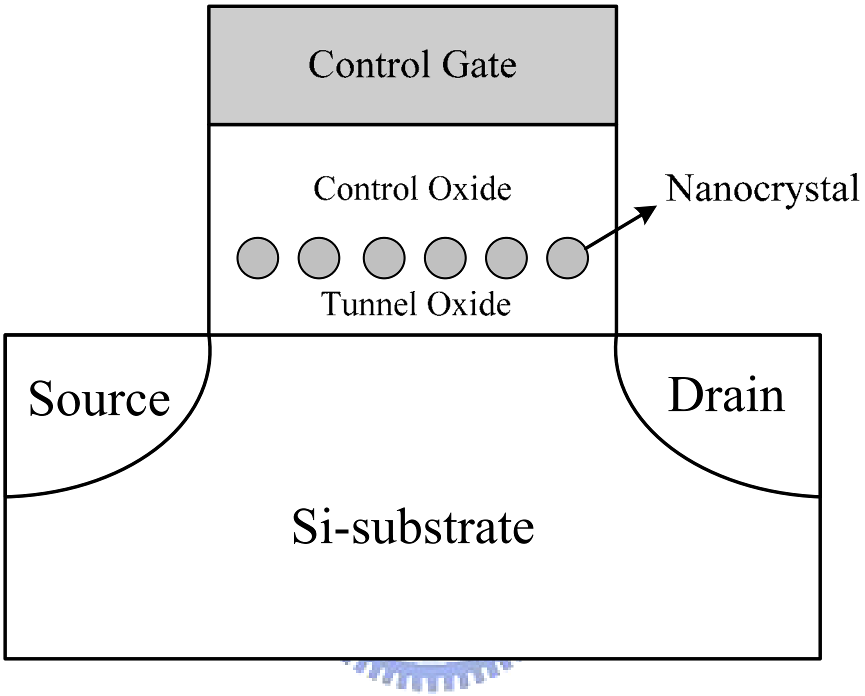


Figure 1-4 The structure of the nanocrystal nonvolatile memory device. The semiconductor nanocrystals or metal nanocrystals are used as the charge storage element instead of the continuous poly-Si floating gate.

Chapter 2

Basic Principle of Nonvolatile Memory

2.1 Introduction

There is a widespread variety of Nonvolatile Memory (NVM) devices, and they all show different characteristics according to the structure of the selected cell and the complexity of the array organization. A NVM memory cell has to commute from one state to the other and that can store the information independently of external conditions. There are several methods to achieve the NVM memory characteristic, such as transistor V_T shifts, charge displacements, and resistance change [2.1]. In this thesis, we focus on one solution that a transistor with a threshold voltage that can change repetitively from a high to a low state, corresponding to the two states of the memory cell. Most operations with a shift in the threshold voltage on novel nonvolatile memories, such as nanocrystal and SONOS memories are base on the concept of Flash memory. If a datum has to be stored in a bit of the memory, there are different procedures. The threshold voltage shift of a Flash transistor can be written as [2.2][2.3]:

$$\Delta V_T = -\frac{\overline{Q}}{C_{FC}}$$

where $\overline{Q}$ is the charge weighted with respect to its position in the gate oxide, and the capacitances between the floating gate and control gate. The threshold voltage of the memory cell can be altered by changing the amount of charge present between the gate and the channel, corresponding to the two states of the memory cell, i.e., the binary values (“1” and “0”) of the stored bit. Figure 2-1 shows the threshold voltage shift between two states in a Flash memory. To a nonvolatile memory, it can be “written” into either state “1” or “0” by either “programming” or “erasing” methods, which are decided by the definition of memory cell itself. There are many solutions to achieve “programming” or “erasing”.

In this chapter, we will discuss program/erase mechanisms from the relation between bias and energy band bending. Tunneling injection, channel hot electron injection, and band to band assisted electron/hole injection will be discussed briefly. The reliability of nonvolatile memory and physical characteristic of nanocrystal NVM will be also discussed.

2.2 Basic Program and Erase Mechanisms

2.2.1 Energy band diagram during program and erase operation

Fig. 2-2 illustrates the program/erase physical operation of a SONOS memory device. In the write operation, a positive voltage is applied on gate electrode relative to the p-type substrate, which forms an electron channel. Then the electrons tunnel through the tunnel oxide into the silicon nitride film and can be stored in deep-level traps. Some electrons which are not trapped in the nitride film will tunnel through a blocking oxide into the gate electrode. The trapped electrons provide the electrostatic screening of the channel from the control gate, and result in a threshold voltage (V_T) shift. During the erase operation under a negative voltage bias on the gate electrode, the holes tunnel from the substrate into the silicon nitride and are partially trapped in a manner similar to electrons. And some holes “pile-up” at the blocking oxide interface because of the larger barrier height (5eV). Further, trapped electrons may be de-trapped into the nitride conduction band and then tunnel back to the channel. Thus, for SONOS memory device operation both carrier types are involved in the transport process.

The write and erase processes for an n-channel semiconductor nanocrystal memory device are illustrated schematically in Fig. 2-3. During the write process, a positive gate voltage is applied to inject channel inversion-layer electrons into the nanocrystals. During the erase process, a reverse gate bias is applied to cause the electrons to tunnel back into the channel and the accumulation layer holes to tunnel into the nanocrystals from the channel.

2.2.2 Carrier Injection Mechanisms

(a) Tunneling Injection

Tunneling is a quantum mechanical process akin to throwing as ball against a wall often enough that the ball goes through the wall without damaging the wall or the ball. It also loses no energy during the tunnel event. The tunneling probability, depending on electron barrier height ($\varphi(x)$), tunnel dielectric thickness (d), and effective mass (m_e) inside the tunnel dielectric, is express as [2-4]

$$T = \exp\left(-2\int_0^d \frac{\sqrt{\phi(x) * m_e}}{\hbar} dx\right)$$

Basically, tunneling injection must to have available states on the other side of the barrier for the carriers to tunnel into. Tunneling through the oxide can be attributed to different carrier-injection mechanisms. Which process applies depends on the oxide thickness and the applied gate field or voltage. Direct tunneling (DT), Fowler-Nordheim tunneling (FN), modified Fowler-Nordheim tunneling (MFN) and trap assistant tunneling (TAT) are the main programming mechanisms employed in memory [2.5-2.7] as shown in Figure 2-4.

Direct Tunneling

Direct Tunneling is the flow of electrons through the full oxide thickness illustrated in Figure 2-4(a). For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [2.8]. As a result, F-N tunneling cannot serve as an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. The direct tunneling is employed in nanocrystal memories instead. In the direct-tunneling regime, a thin oxide with thickness less than 3 nm is used to separate the nanocrystals from the channel. During program/erase operations, electrons/holes can pass through the oxide by direct tunneling, which gives the advantages of fast write/erase and low operation voltage. In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height, two to four orders of magnitude reduction in leakage current can still be achieved if large work function metals, such as Au or Pt [2.9].

Fowler–Nordheim Tunneling

The Fowler–Nordheim (FN) tunneling is the flow of electrons through a triangular potential barrier illustrated in Figure 2-4(b). FN tunneling mechanism occurs when applying a strong electric field (in the range of 8–10 MV/cm) across a thin oxide. In these conditions, the energy band diagram of the oxide region is very steep. Therefore, there is a high probability of electrons’ passing through the energy barrier itself. Using a free-electron gas model for the metal and the Wentzel–Kramers–Brillouin (WKB) approximation for the tunneling probability [2.10], one obtains the following expression for current density [2.11]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp\left[\frac{-4(2m_{OX}^{*})^{1/2} \Phi_B^{3/2}}{3\hbar q F} \right]$$

Where Φ_B is the barrier height, m_{OX}^{*} is the effective mass of the electron in the forbidden gap of the dielectric, h is the Planck's constant, q is the electronic charge, and F is the electrical field through the oxide. The exponential dependence of tunnel current on the oxide-electric field causes some critical problems of process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states.

Modified Fowler–Nordheim Tunneling

Modified Fowler–Nordheim tunneling (MFN) is similar to the traditional FN tunneling mechanism, yet the carriers enter the nitride at a distance further from the tunnel oxide-nitride interface. MFN mechanism is frequently observed in SONOS memories. The SONOS memory is designed for low-voltage operation (< 10V, depending on the Equivalent oxide thickness), a relatively weak electrical field couldn't inject charges by DT or FN mechanism.

Trap Assistant Tunneling

The charge storage mediums with many traps may cause another tunneling mechanism. For example, the charges tunnel through a thin oxide and arrive to the traps of nitride layer at very low electrical field in SONOS systems. During trap assisted injection the traps are emptied with a smaller time constant then they are filled. The charge carriers are thus injected at the same distance into the nitride as for MFN injection. Because of the sufficient injection current, trap assistant tunneling may influence in retention [2.12].

(b) Channel Hot Electron Injection (CHEI)

The physical mechanism of HEI is relatively simple to understand qualitatively. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100 kV/cm [2.13]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are “heated” by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges (channel hot electron, CHE). Figure 2-5 shows schematic representation of CHEI MOSFET and the energy-distribution function with different fields. In the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection rarely is employed in nonvolatile memory operation.

Nevertheless, a description of the injection conditions can be accomplished with two different approaches. The HEI current is often explained and simulated following the “lucky electron” model [2.14]. This model is based on the probability of an electron’s being lucky enough to travel ballistically in the field ε for a distance several times the mean free path without scattering, eventually acquiring enough energy to cross the potential barrier if a collision pushes it toward the Si/SiO$_2$ interface. Consequently, the probability of injection is the lumped probability of the following events [2.15], which are depicted in Figure 2-6

1) The carrier has to be “lucky” enough to acquire enough energy from the lateral electric field to overcome the oxide barrier and to retain its energy after the collision that redirects the electron toward the interface ($P_{\Phi b}$).
2) The carrier follows a collision-free path from the redirection point to the interface (P_{ED}).
3) The carrier can surmount the repulsive oxide field at the injection point, due to the Schottky barrier lowering effect, without suffering an energy-robbing collision in the oxide (P_{OC}).

(c) Band to Band Tunneling (BTBT)

Band to band tunneling application to nonvolatile memory was first proposed in 1989. I. C. Chen and et al. demonstrated a high injection efficiency (~1%) method to programming EPROM devices [2.16].

Band to Band Hot Electron Tunneling Injection

The injection is applied for n-type substrate nonvolatile memory device. Figure 2-7 shows the energy-band diagram and device operation during the band to band tunneling induced hot electron (BBHE) injection. When band-bending is higher than the energy gap of the semiconductor, the tunneling electron from the valence band to the conduction band becomes significant. The electrons are accelerated by a lateral electric field toward the channel region and some of the electrons with sufficient energy can surmount the potential barrier of SiO_2 like hot electron injection [2.16-2.18].

Band to Band Hot Hole Tunneling Injection

In p-type substrate, when a negative gate voltage and a positive drain voltage are applied to the cell, electron-hole pairs are generated by BTBT in the drain region, as shown in Figure 2-8. The holes are accelerated by a lateral electric field toward the channel region and some of them obtain high energy. The hot holes inject into charge trapping layer through the tunnel oxide and recombine the stored electrons. This injection is used for a new erase operation for nonvolatile memory device [2.19].

2.3 Basic Reliability of Nonvolatile Memory

For a nonvolatile memory, the important to concern is distinguishing the state in cell. However, in many times operation and charges storage for a long term, the state is not obvious with charges loss. Endurance and retention experiments are performed to investigate Flash-cell reliability. In general, NVMs are required to withstand up to 10-100K program/erase cycles (endurance) with 10-year memory retention at temperatures as high as 85 °C.

2.3.1 Retention

Retention describes the ability to the NVM to store and recover information after a number of program cycles at a specified temperature. In any nonvolatile memory technology, it is essential to retain data for over ten years. This means the loss of charge stored in the storage medium must be as minimal as possible. For example, in modern Flash cells, FG capacitance is approximately 1 fF. A loss of only 1 fC can cause a 1V threshold voltage shift. If we consider the constraints on data retention in ten years, this means that a loss of less than five electrons per day can be tolerated [2.20]. Possible causes of charge loss are: 1) by tunneling or thermionic emission mechanisms; 2) defects in the tunnel oxide; and 3) de-trapping of charge from insulating layers surrounding the storage medium; 4) mobile ion contamination.

Further, the retention capability of Flash memories has to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

2.3.2 Endurance

The term "endurance" refers to the ability of the nonvolatile memory to withstand repeated program cycles and still meet the specifications in the data sheet. In a conventional Flash memory the maximum number of erase/program cycles that the device must sustain is 10^5.

A typical result of an endurance test on a single cell is shown in Figure 2-9. As the experiment was performed applying constant pulses, the variations of program and erase threshold voltage levels are described as "program/erase threshold voltage window closure" and give a measure of the tunnel oxide aging. In particular, the reduction of the programmed threshold with cycling is due to trap generation in the oxide and to interface state generation at the drain side of the channel, which are mechanisms specific to hot-electron degradation. The initial lowering of V_T the erase is due to a pile-up of positive charge which enhances tunneling efficiency. While the long-term increase of V_T the erase is due to a generation of negative traps.

Actually, endurance problems are mostly given by single-cell failures, which present themselves like a retention problem after program/erase cycles. In fact, a high field stress on thin oxide is known to increase the current density at low electric field. The excess current component, which causes a significant deviation from the current–voltage curves from the theoretical FN characteristics at low field, is known as stress-induced leakage current (SILC). SILC is clearly attributed to stress-induced oxide defects and, as far as a conduction mechanism, it is attributed to a trap assisted tunneling, as shown in Figure 2-10. The main parameters controlling SILC are the stress field, the amount of charge injected during the stress, and the oxide thickness. For fixed stress conditions, the leakage current increases strongly with decreasing oxide thickness [2.21-2.23]

2.4 Basic Physical Characteristic of Nanocrystal NVM

2.4.1 Quantum Confinement Effect

The quantum dot, is quasi-zero-dimensional nanoscaled material, and is composed by small amount atoms. The quantum confinement energy dependence on nanocrystal size has been studied both experimentally and theoretically with the tight-binding model [2.24]. The quantum confinement effect becomes significant when the nanocrystal size shrinks to the nanometer range, which causes the conduction band in the nanocrystal to shift to higher energy compared with bulk material [2.25]. For example, a 3nm Ge nanocrystal can have a conduction band shift of 0.5eV as compared with bulk Ge, which is significant enough to affect the electrical performance of the nanocrystal memory cell.

2.4.2 Coulomb Blockade Effect

When one electron is stored, the nanocrystal potential energy is raised by the electrostatic charging energy $e^2/2C$, where C is the nanocrystal capacitance, which depends mainly on the nanocrystal size, though it also depends on tunnel oxide thickness and control oxide thickness. The capacitance is self-consistently calculated using an electrodynamics method [2.26]. The electron charge will raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density during the write process. It is more dominant at low programming voltages (< 3V). In a flash memory array, device cells often encounter disturbances with low gate voltage soft-programming. The Coulomb blockade effect can effectively inhibit the electron tunneling at low gate voltage and improve the flash memory array immunity to disturbance. However, the Coulomb blockade effect should be reduced by employing large nanocrystal if large tunneling current and fast programming speed were desired. The Coulomb blockade effect has a detrimental effect on the retention time, since the electrons in the nanocrystal have large tendency to tunnel back into the channel if the nanocrystal potential energy is high in retention mode. In the energy band diagram, the Coulomb blockade charging energy only raises the electrostatic potential of the nanocrystal; the quantum confinement energy shifts the nanocrystal conduction band edge upward so that the conduction band offset between the nanocrystal and the surrounding oxide is reduced.

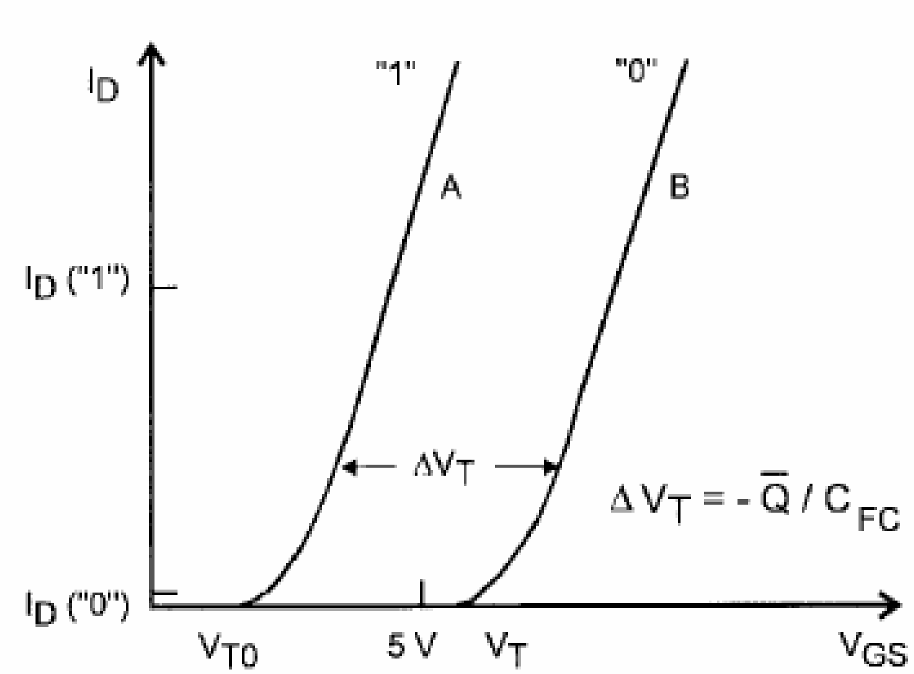
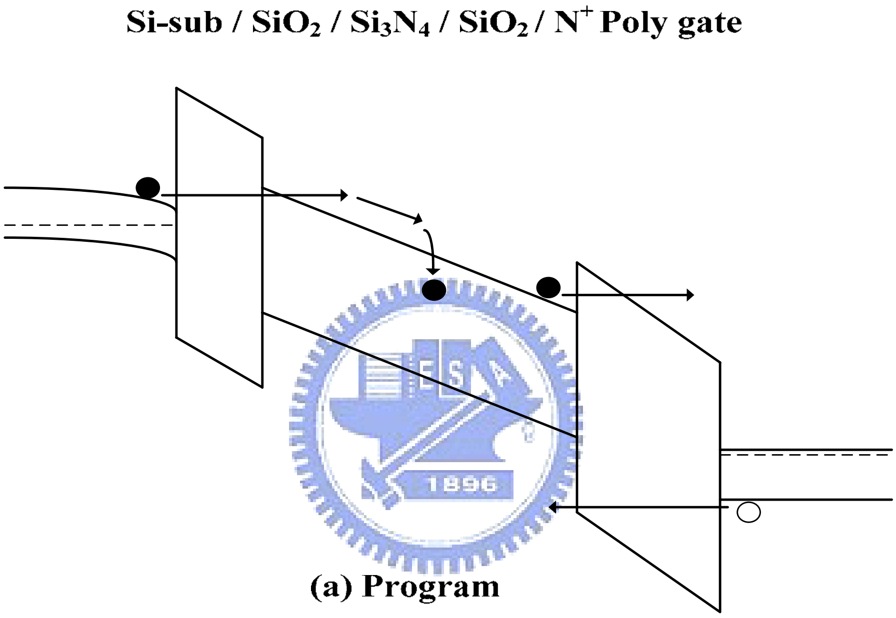
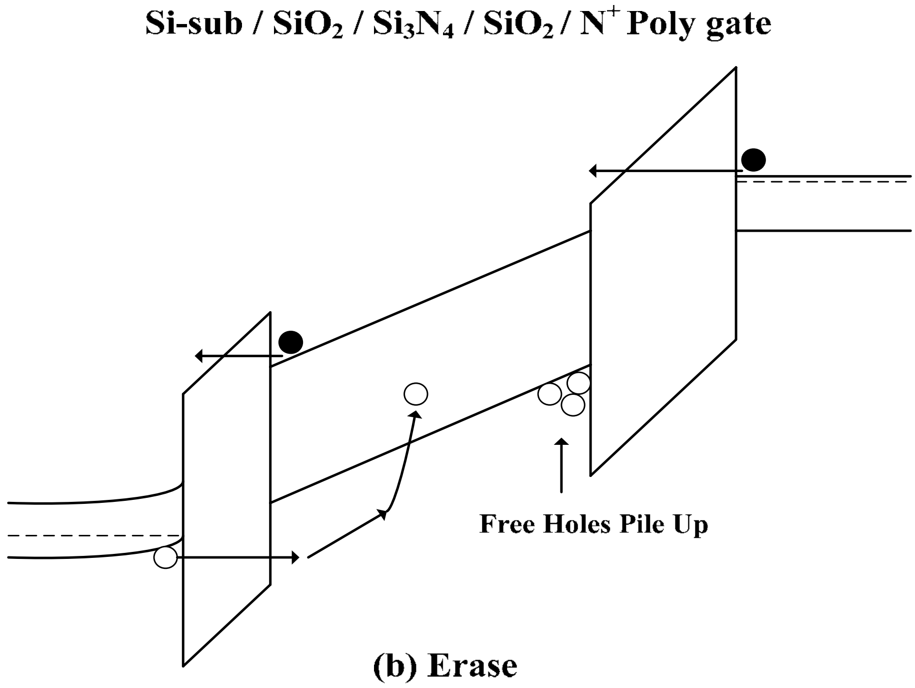

I_D
"1"
"0"
A
B
I_D ("1")
ΔV_T
ΔV_T = - Q̄ / C_FC
I_D ("0")
V_T0
5 V
V_T
V_GS

Figure 2-1 I–V curves of the floating-gate device when there is no charge stored in the floating-gate (curve A) and when a negative charge Q is stored in the floating-gate (curve B).



(a) Program



(b) Erase

Figure 2-2 Energy band diagrams of the SONOS memory device under (a) program (b) erase operation.● electrons, ○ holes.

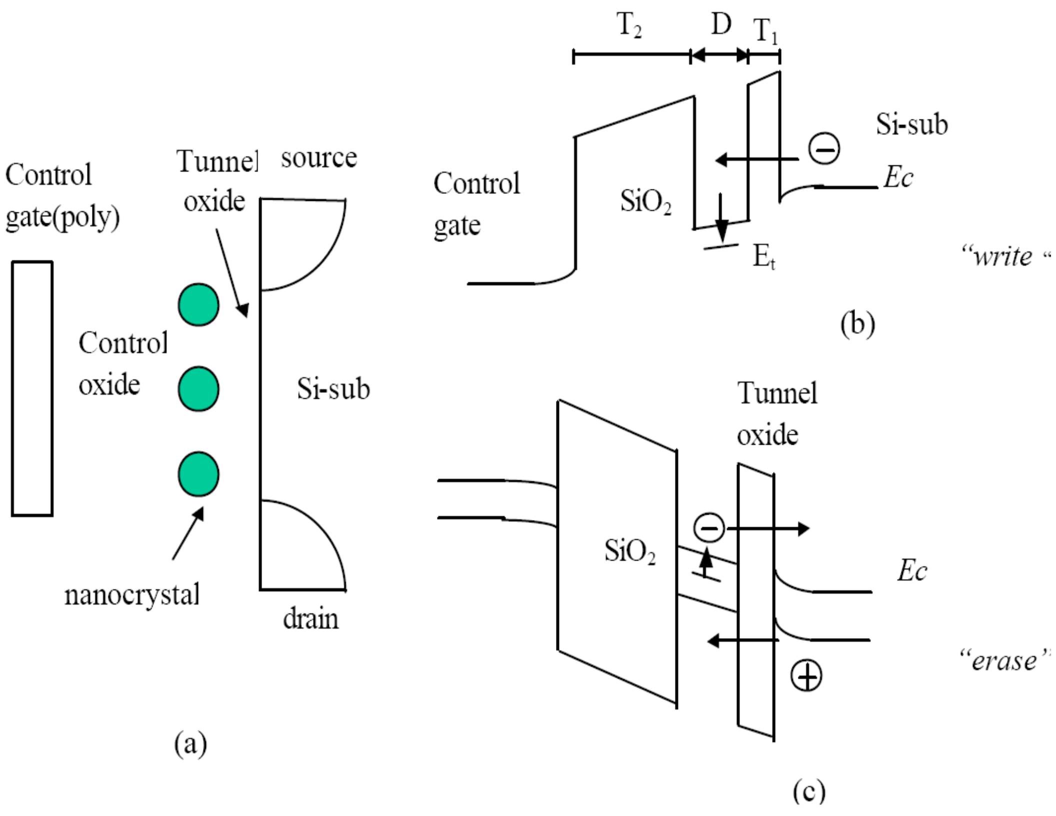
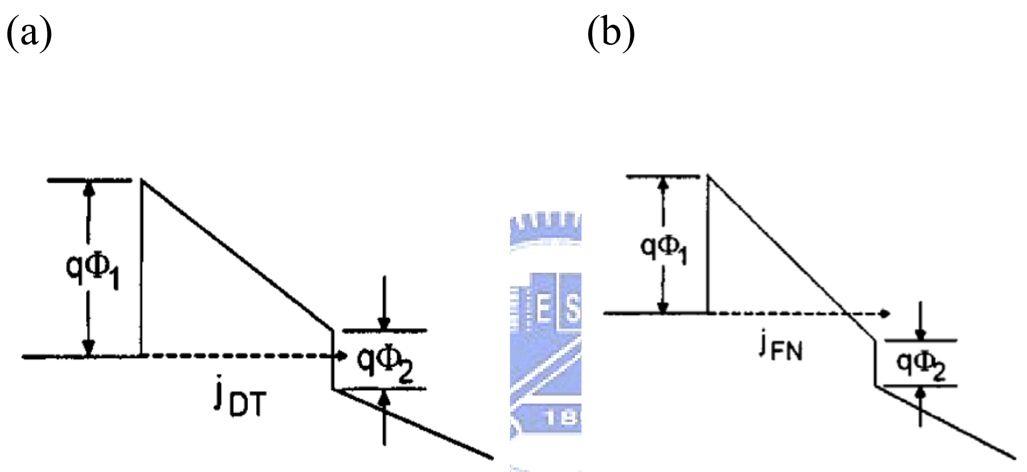
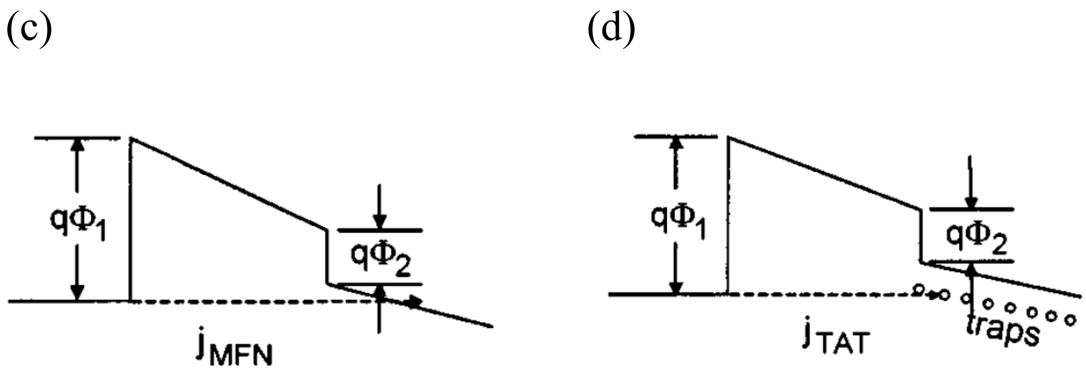


Figure 2-3 (a) Schematic cross-section of nanocrystal memory device structure; (b) illustration of write process: inversion-layer electrons tunnel into the nanocrystal; (c) illustration of erase process: accumulation layer holes tunnel into the nanocrystal, electron in nanocrystal can tunnel back to the channel.



DT occur when $\frac{\phi_1}{X_{OT}} > |E_{OT}| > \frac{\phi_1 - \phi_2}{X_{OT}}$

FN occur when $|E_{OT}| > \frac{\phi_1}{X_{OT}}$



MFN occur when

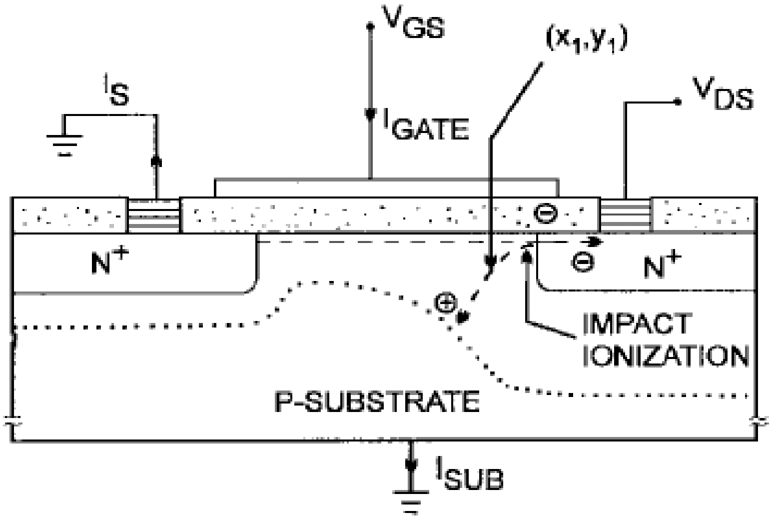
TAT occur when

$$\frac{\phi_1-\phi_2}{X_{OT}} > \left|E_{OT}\right| > \frac{\phi_1-\phi_2}{X_{OT}+\left(\varepsilon_{OX}/\varepsilon_N\right)X_N}$$

$$\frac{\phi_3}{X_{OT}} > \left|E_{OT}\right| > \frac{\phi_3}{X_{OT}+\left(\varepsilon_{OX}/\varepsilon_N\right)X_N}$$

$$\phi_3=\phi_1-\phi_2-\phi_t$$

Figure 2-4 Fourth approaches to programming methods (a) Direct tunneling (DT) (b) Fowler-Nordheim (FN) tunneling (c) Modified Fowler-Nordheim (MFN) tunneling (d) Trap assistant tunneling (TAT).



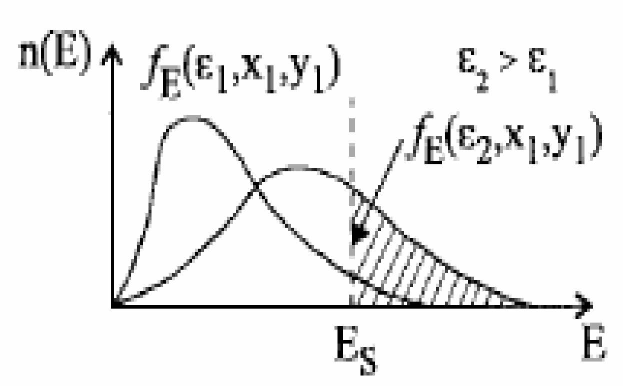


Figure 2-5 Schematics of channel hot electron injection (CHEI). The energy distribution function at point (X_1, Y_1) is also shown.

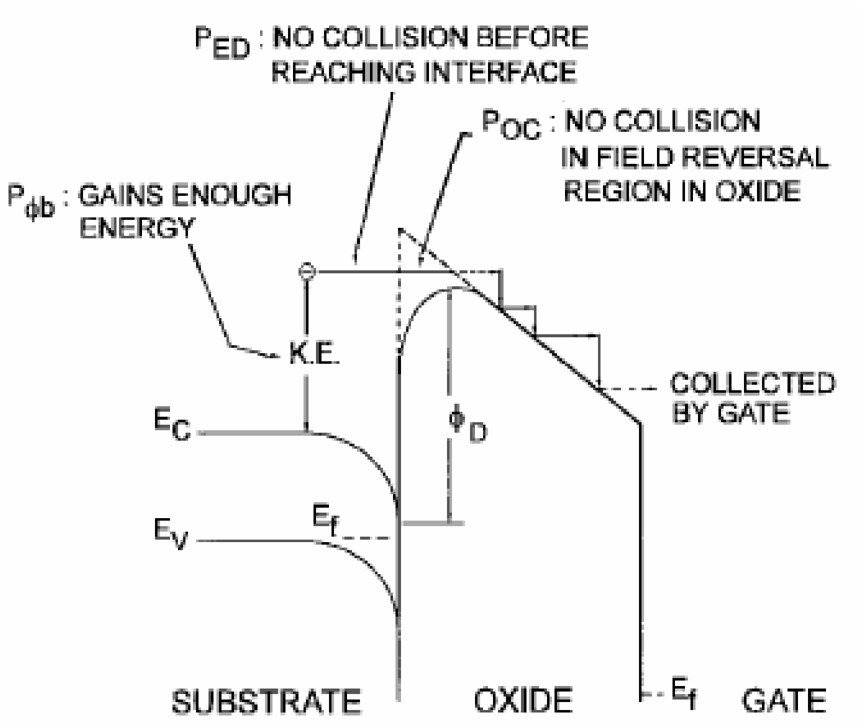
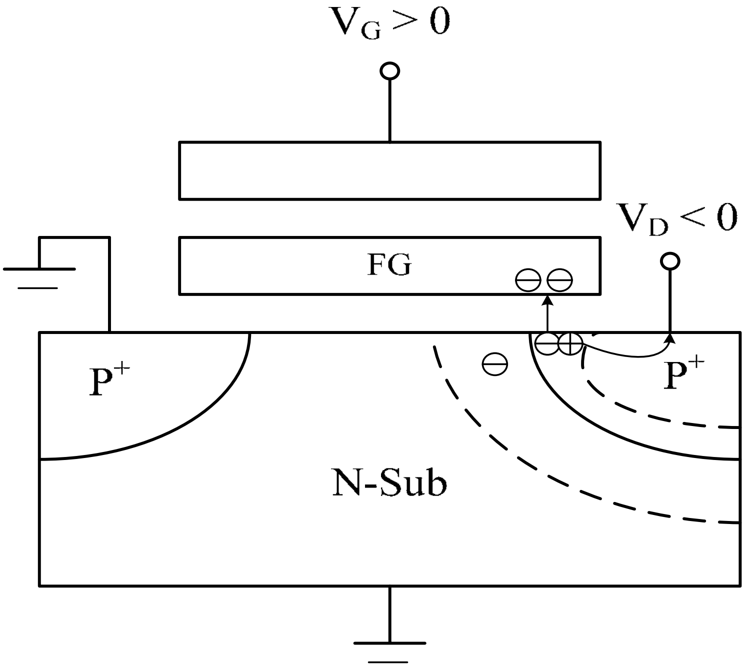


Figure 2-6 A schematic of energy band diagram describing the process involved in electron injection.



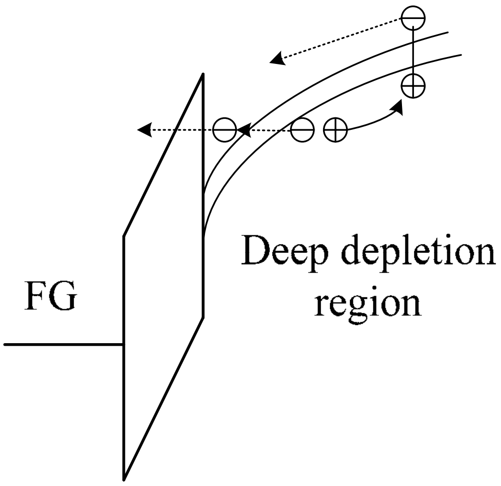


Figure 2-7 Energy-band diagram for the proposed band to band induce hot electron injection mechanism and schematic illustration cross of the Flash memory with p-channel cell. Due to the positive bias to the control gate, holes are not injected into the tunnel oxide.

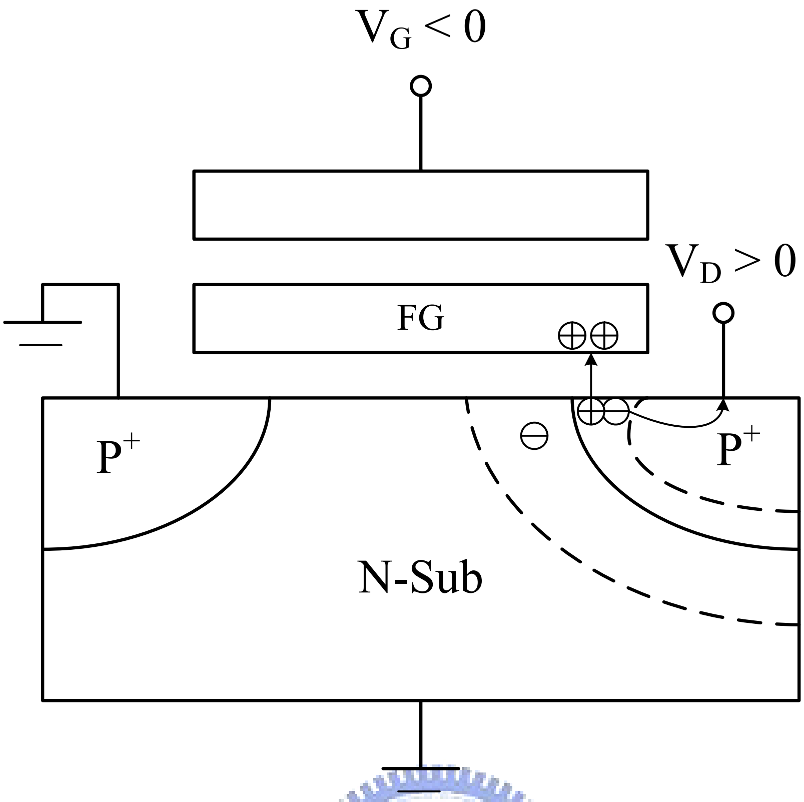


Figure 2-8 Band to band induce hot hole injection mechanism and schematic illustration cross of the Flash memory with p-channel cell.

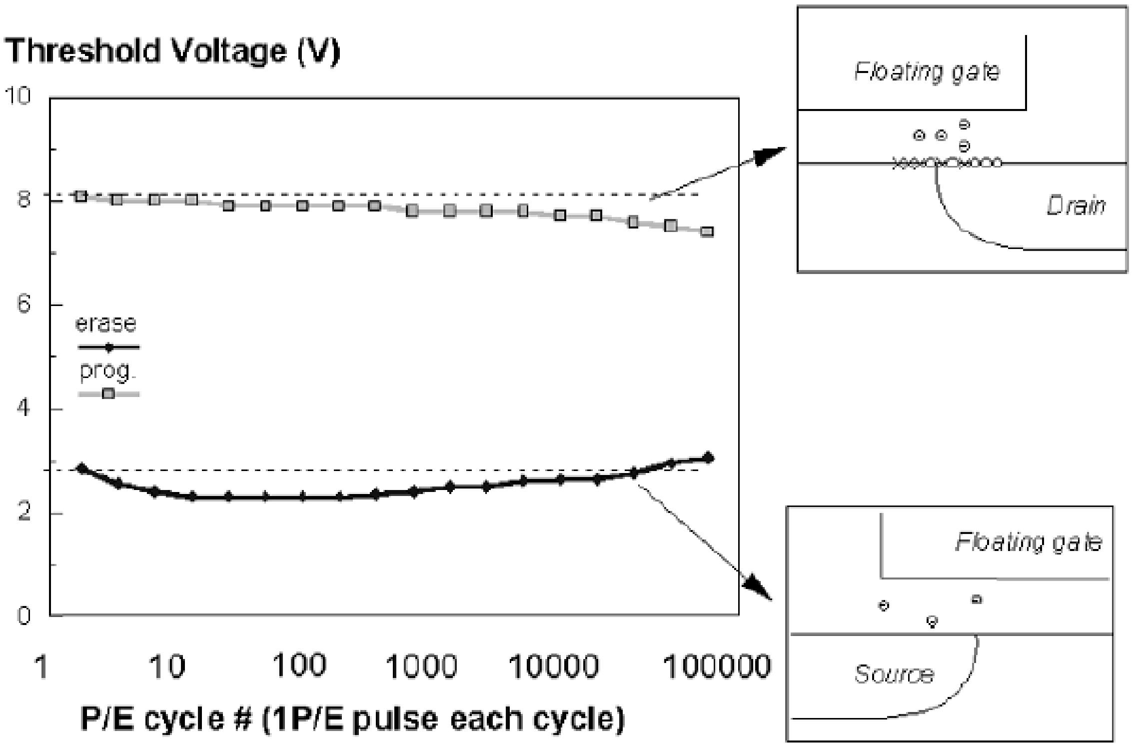


Figure 2-9 A typical result of an endurance test on a single cell. Threshold voltage window closure as a function of program / erase cycles.

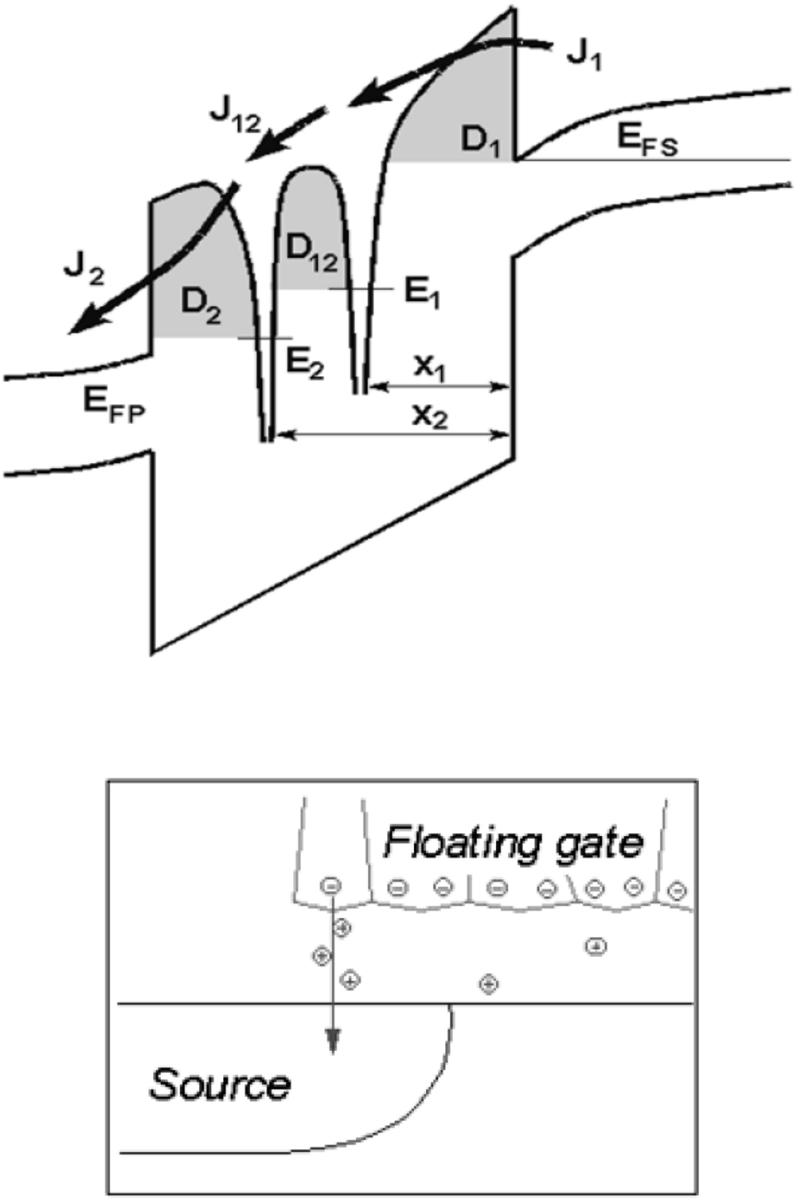


Figure 2-10 Anomalous SILC modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase. The multitrap assisted tunneling is used to model SILC: trap parameters are energy and position.

Formation and nonvolatile memory effect of Ti-Si-O and Ti-O Nanocrystal embedded in SiO2

3.1 Motivation

Nonvolatile memory (NVM) plays an important role in the market of portable electronic products and current requirements of further NVM are the high density cells, low-power consumption, high-speed operation and good reliability for the scaling down devices [3.1-3.3]. However, all of the charges stored in the floating gate will leak into the substrate if the tunnel oxide has a leakage path in the conventional NVM during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down in terms of charge retention and endurance characteristics. The nonvolatile nanocrystal memories are one of promising candidates to substitute for conventional floating gate memory, because the discrete traps as the charge storage media have effectively improved data retention under endurance test for the scaling down device [3.4, 3.5]. The metal nanocrystal memories were extensively investigated over semiconductor nanocrystal, because of several benefits, such as enhanced control ability of gate (i.e. stronger coupling with the conduction channel), higher density of states (DOS) , smaller energy disturbance and larger work function (faster programming time and better data retention) [3.5,3.6]. A nonvolatile memory device for various metal nanocrystals has been formed by several experiment techniques, for instance, self-assembled of tungsten (W) nanocrystal by using thermal oxidation process [3.7], separation of nickel (Ni) or gold (Au) nanocrystal by direct thermal annealing [3.8, 3.9], formation of platinum (Pt) or cobalt (Co) nanocrystal by using molecular beam epitaxy (MBE) [3.10, 3.11].

3.2 Nonvolatile Titanium oxide Nanocrystal Memory by $TiSi_2$ and Si layer

3.2.1 Experimental Procedures

Figure 3-1(a) and (b) exhibit schematics of the experimental procedures. This nonvolatile memory-cell structure in this letter was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 5-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 50-A-thick charge tapping layer was deposited by reactive sputtering of $TiSi_2$ and Si (1 : 1) co-mix target in the Ar and O_2 (24 standard cubic centimeters per minute (sccm)) ambiance at room temperature. This step can obtain an oxygen incorporated $TiSi_2$ and Si layer as a charge trapping layer in our memory structure. Next, the rapid thermal annealing (RTA) process was performed in nitrogen (N_2) atmosphere. The annealing conditions are 500^{o}C for 120 sec. Then, a 40-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300^{o}C. During the foregoing process, the Ti-Si-O nanocrystals could be found to precipitate and embed in SiO_2 layer. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure.

Electrical characteristics, including the capacitance-voltage (C-V), retention, and endurance characteristics, were also performed. The C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

3.2.2 Results and Discussion

Figure 3-2(a) show cross-sectional TEM image of oxygen deficient $TiSi_2$ and Si incorporated layer, respectively. Figure 3-2(a) exhibits the oxygen incorporated $TiSi_2$ and Si layer containing spherical and separated nanocrystals. The average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 1.33×10^{12} cm^{-2}. Furthermore, it is found that the thickness of tunnel oxide is larger than 3 nm by TEM analysis, due to the contribution of SiO_x layer in the charge trapping layer.

Capacitance-voltage (C-V) hysteresis obtained with oxygen deficient $TiSi_2$ and Si layer shown in Fig. 3-3. From Fig. 3-3, it is clearly observed that 1.9 V and 3 V memory windows can be obtained under ±5 V and ±7 V gate voltage operation. Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate [3.16]. Hence, we can be enough to define “1” and “0” states using this nanocrystal memory structure. As a result, our electrical characteristics of C-V show that nonvolatile memory effect is influenced by oxygen doping.

The XPS analysis by using an Al $K\alpha$ (1486.6 eV) x-ray radiation is demonstrated the chemical composition of the charge trapping layer. To correct possible charging effect of the film, the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. As shown in Fig. 3-4, the Ti $2p$ core-level photoemission spectra consist of two main $2p_{3/2}$ (458.8 eV) and $2p_{1/2}$ (464.8 eV) lines and corresponding satellites. According to previous research, the peak position and profile of Ti $2p_{3/2}$ are similar to Ti-Si-O signal by XPS analysis [3.17]. Hence, we can consider that the charge trapping layer is composed of Ti-Si-O ternary element. This consideration is also verified by the XPS O 1*s* photoemission spectra, as shown in Fig. 3-4(b). By the fitting result of experiment data, it is found that the main peak can be composed into two components which center at 530.7 eV and 532.3 eV corresponding to Ti-Si-O bond and Si-O-Si bond, respectively [3.18]. During the course of our investigation, we found that these nanocrystals are enough reasoned to be composed of Ti-Si-O ternary element and embedded in SiO_2..

The reliability issues, such as retention and endurance, were also tested in this work. Figure 3-5 demonstrates the data retention characteristics of the nonvolatile Ti-Si-O nanocrystal memory at room temperature. The memory cell is programmed by 10 V, 5 s, and -10 V, 5 s gate pulses for Data "1" and "0", respectively. The flat band voltage shift is obtained by comparing the *C-V* curves from a charged state and the quasi-neutral state. The memory window significantly decays during the first 100 s due to charge emission from the shallow traps in SiO_2 (partial oxidized *a*-Si) matrix. However, a 1.2 V memory window (charge remained ratio of 40%) from the elongation line of the decay trend can obtain even after 10 years. Endurance characteristics for Ti-Si-O nanocrystals embedded in SiO_2 matrix are shown in Fig. 3-6. Pulses (V_G - V_{FB} = ± 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. The obvious closure of voltage window between the program and erase state results from degradation of SiO_2 dielectric. It is also believed that the SiO_x quality is much worse than the tunnel oxide. The defect generation under P/E operation will increase leakage paths and degrade the charge storage capability. However, it retains a memory window of 1.1V which is enough to define "1" and "0" of memory states.

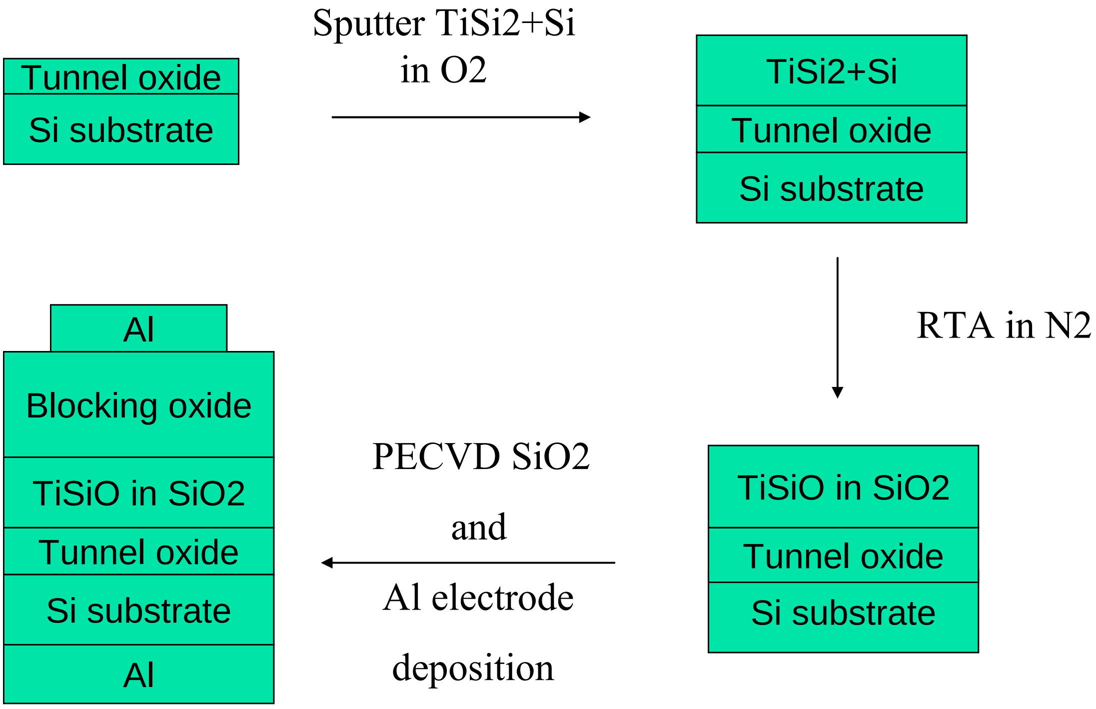


Figure 3-1 Schematics of the experimental procedures. TiSi2 and Si layer.

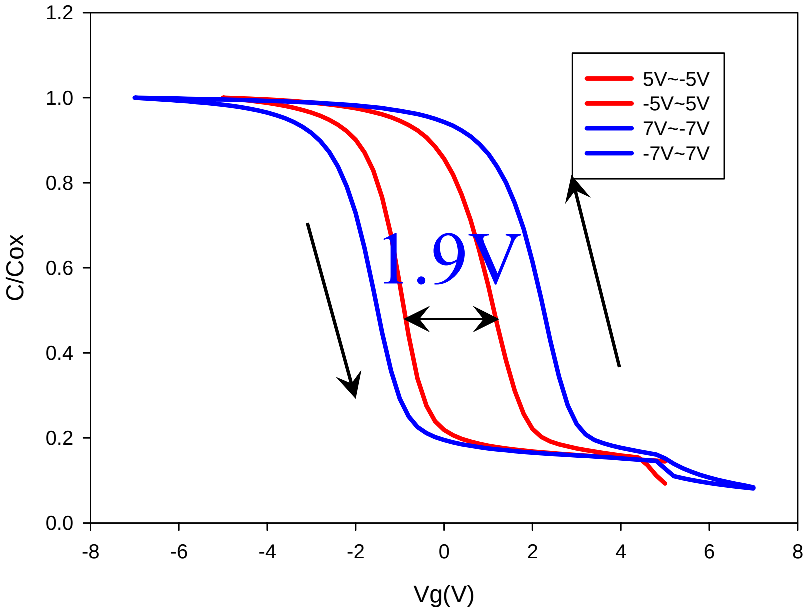


Figure 3-2 Capacitance-voltage (C-V) hysteresis of the fabricated MOIOS structure with TiSi$_2$ and Si layer.

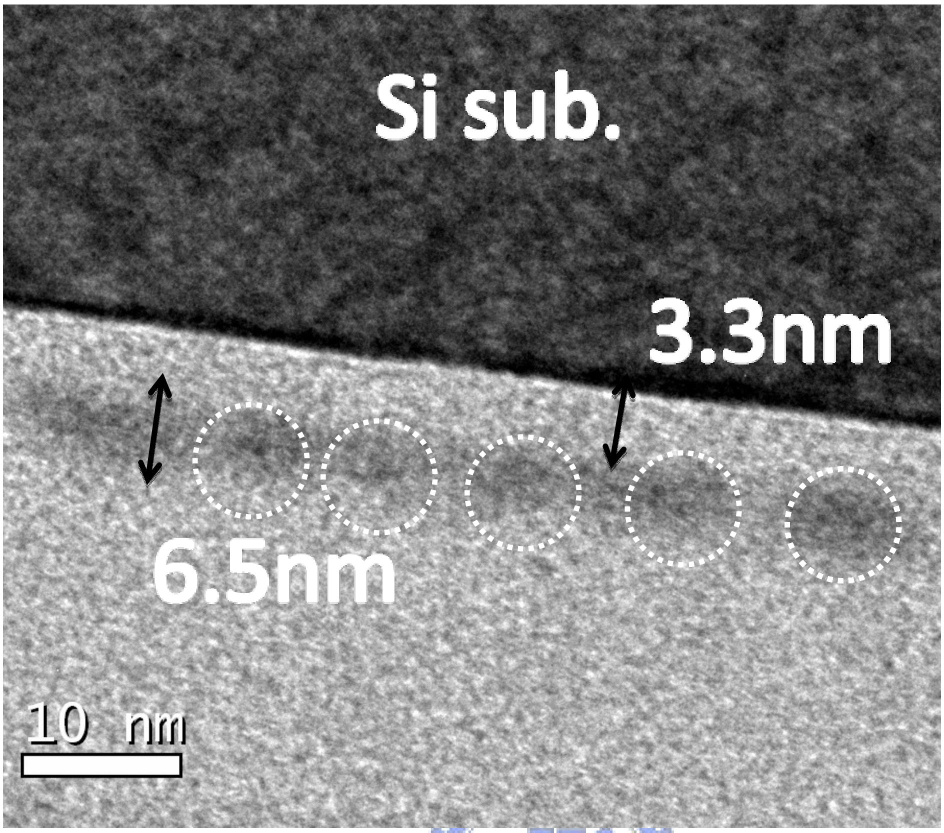


Figure 3-3 Cross-sectional TEM images of the MOIOS structure with $TiSi_2$ and Si layer RTA in N_2

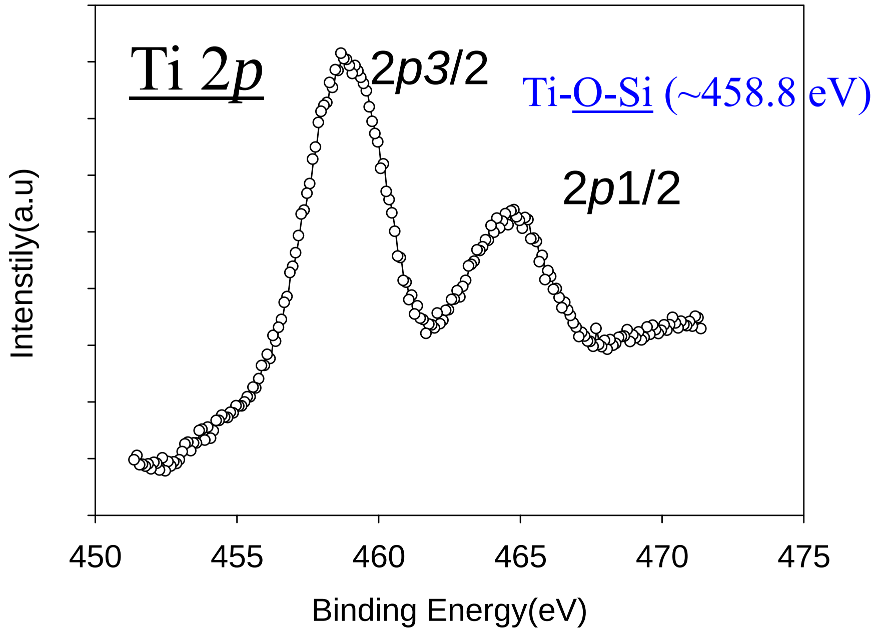


Figure 3-4 Ti 2*p* XPS analysis of the oxygen incorporated TiSi2 and Si layer. The peak position are similar to Ti-Si-O signal.

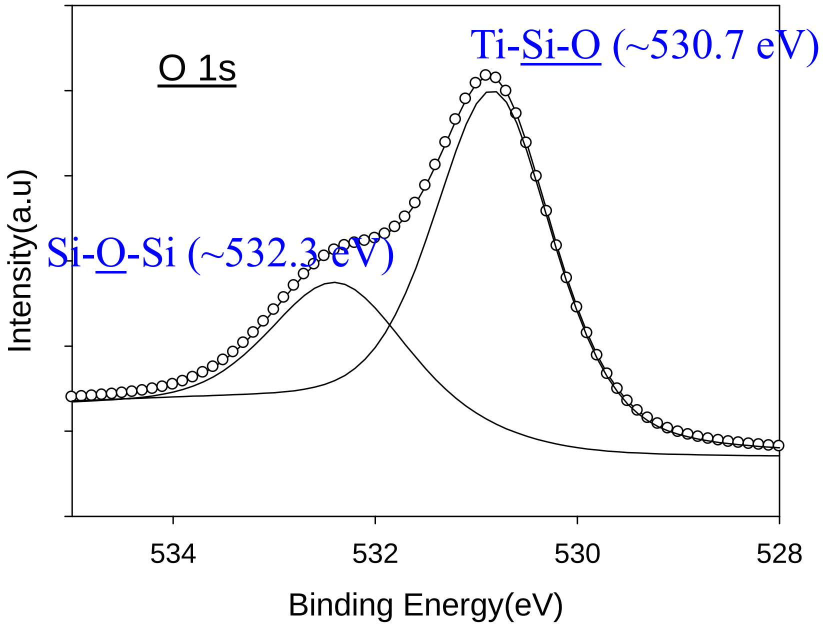


Figure 3-5 O 1*s* XPS analysis of TiSi2 and Si layer. Empty circles and straight line indicate experimental and fitting results, respectively. The main peak can be composed into two components which center at 530.7 eV and 532.3 eV corresponding to Ti –Si-O bond and Si-O-Si bond.

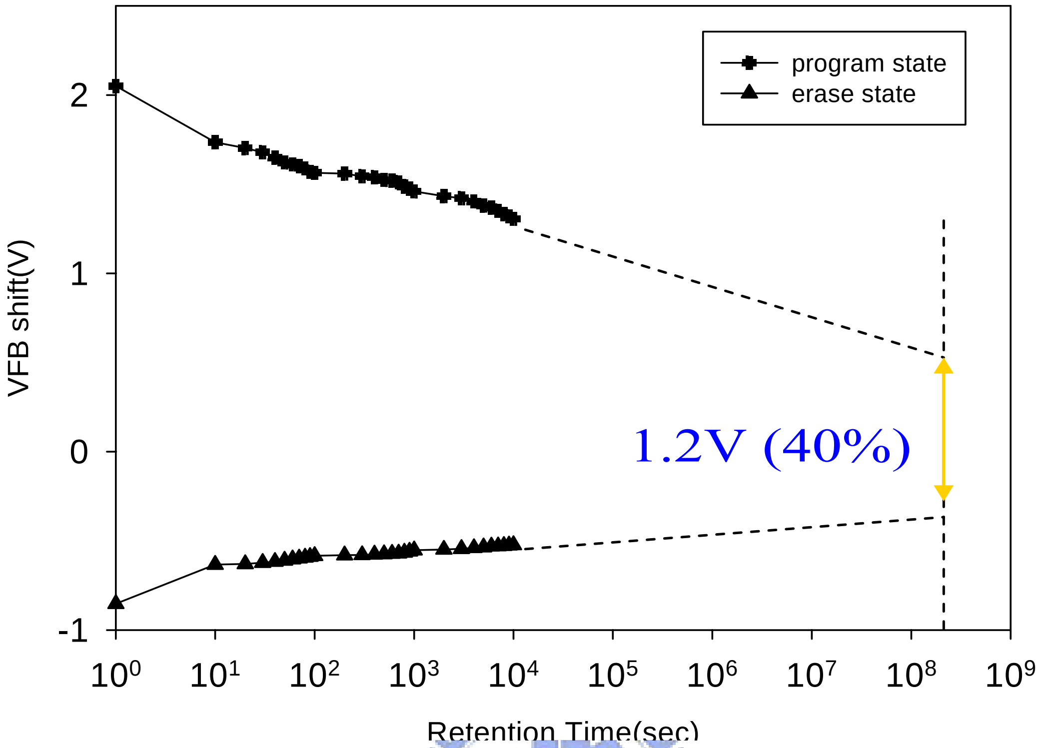


Figure 3-6 Data retention characteristics of the Ti-Si-O nanocrystal memory at room temperature.

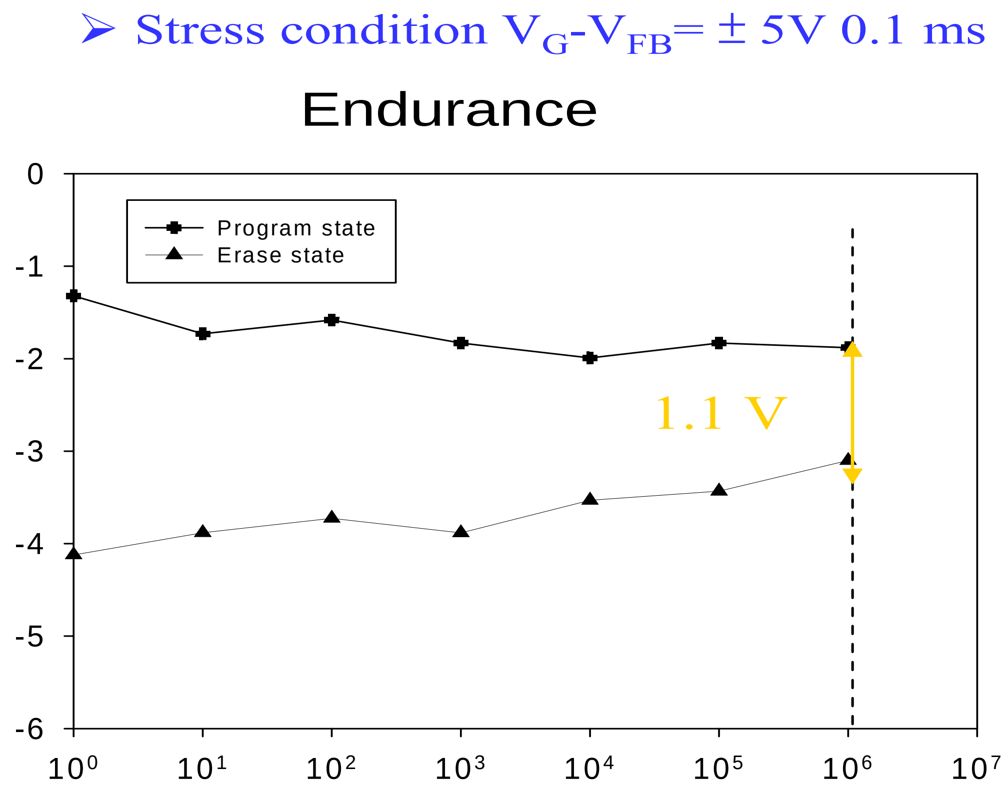


Figure 3-7 Endurance characteristics of the Ti-Si-O nanocrystal memory.

3.3 Nonvolatile Titanium oxide Nanocrystal Memory by TiSi2 and Si layer

3.3.1 Experimental Procedures

Figure 3-1 exhibit schematics of the experimental procedures. This nonvolatile memory-cell structure in this paper was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 5-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 50-A-thick charge tapping layer was deposited by reactive sputtering of $TiSi_2$ and Si (1 : 1) co-mix target in the Ar and O_2 (24 standard cubic centimeters per minute (sccm)) ambiance at room temperature. This step can obtain an oxygen incorporated $TiSi_2$ and Si layer as a charge trapping layer in our memory structure. Next, the rapid thermal annealing (RTA) process was performed in oxygen (O_2) atmosphere. The annealing conditions are 500^{o}C for 120 sec. Then, a 40-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300^{o}C. During the foregoing process, the TiO_2 nanocrystals could be found to precipitate and embed in SiO_2 layer. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure.

Electrical characteristics, including the capacitance-voltage (C-V), retention, and endurance characteristics, were also performed. The C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

3.3.2 Results and Discussion

Figure 3-8 exhibits a cross-sectional TEM image of the nitrogen incorporated TiSi2 and Si layer containing spherical and separated nanocrystals embedded in the SiO_2 matrix. It is found that the thickness of tunnel oxide is larger than 3 nm, due to the contribution of SiO_2 layer by HRTEM analysis. This SiO_2 matrix can be used to improve charge storage ability for nonvolatile memory application [3.19]. Moreover, the average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 4.56×10^{11} cm^{-2} by HRTEM analysis.

To further investigate the nanocrystal, we have performed XPS analysis by using an Al $K\alpha$ (1486.6 eV) X-ray radiation to demonstrate the chemical composition of the nanocrystals. To correct possible charging effect of the film, the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. Figure 3-9(a) shows the XPS Ti $2p$ core-level photoemission spectra which consist of two main peaks, $2p_{3/2}$ (~ 458.1 eV) and $2p_{1/2}$ (~ 464.4eV), with two small satellite peak. Due to the strong electronegativity of nitrogen atom, it is reasonably assumed that the larger Ti $2p_{1/2}$ binding energy (~ 458.1 eV) of the nanocrystals can be assigned to TiO_2 ternary bond.

The typical capacitance-voltage (*C-V)* hysteresis obtained with gate voltage from accumulation to inversion and in reverse is shown in Fig. 3-10. It is clearly observed that 3.2 V and 4.5 V memory windows can be obtained under 5~-5 V and 7~-7 V operation, respectively. The MOIOS structure with the TiO_2 nanocrystals embedded in SiO_2 matrix exhibits clear counterclockwise hysteresis by a flat band voltage (V_{FB}) shift, indicating the significant memory effect. We consider that the charges can be stored in both the TiO_2 nanocrystal and the SiO_2 traps. Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate. Hence, this memory window of TiO_2 nanocrystals embedded in SiO_2 matrix is enough to be defined "1" and "0" states.

Retention characteristics of the memory structure with TiO_2 nanocrystals are illustrated in Fig. 3-11. The retention measurements are performed at room temperature by operating a ±10 V gate voltage stress for 5 s. The flat band voltage shift is obtained by comparing the *C-V* curves from a charged state and the quasi-neutral state. When carriers are stored in the nanocrystals, the stored charges will raise the nanocrystal potential energy and increase the probability of escaping from the nanocrystal to the silicon substrate [3.23]. Moreover, carriers trapped in the shallow traps are unstable and can easily leak back to the silicon substrate. It is found that the window of V_{FB} significantly reduces during the first 100 s, and becomes more stable for long retention time. This result is consistent with partial carriers trapping in the shallow trap state of the SiO_2 matrix around the nanocrystals. However, the long-term extrapolated gives a memory window of 1.4V (total charge loss ratio 58%) after ten years. The majority carriers stored in the deep trapping states of TiO_2 nanocrystals surrounding with SiO_2 matrix exhibit good retention characteristics.

Endurance characteristics for TiO_2 nanocrystals embedded in SiO_2 matrix are shown in Fig. 3-12. Pulses (V_G - V_{FB} = ± 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. An obvious difference of two logical states can be maintained until 10^4 P/E cycles. Subsequently, the closure of window between two logical states appears after 10^4 P/E cycles. We consider that this closure is caused by the degradation of SiO_x dielectric. However, this memory structure exhibits better endurance characteristics than TiO_2 nanocrystal memory. Consequently, it retains a large window of 1.1V which is enough to define “1” and “0” of memory state.

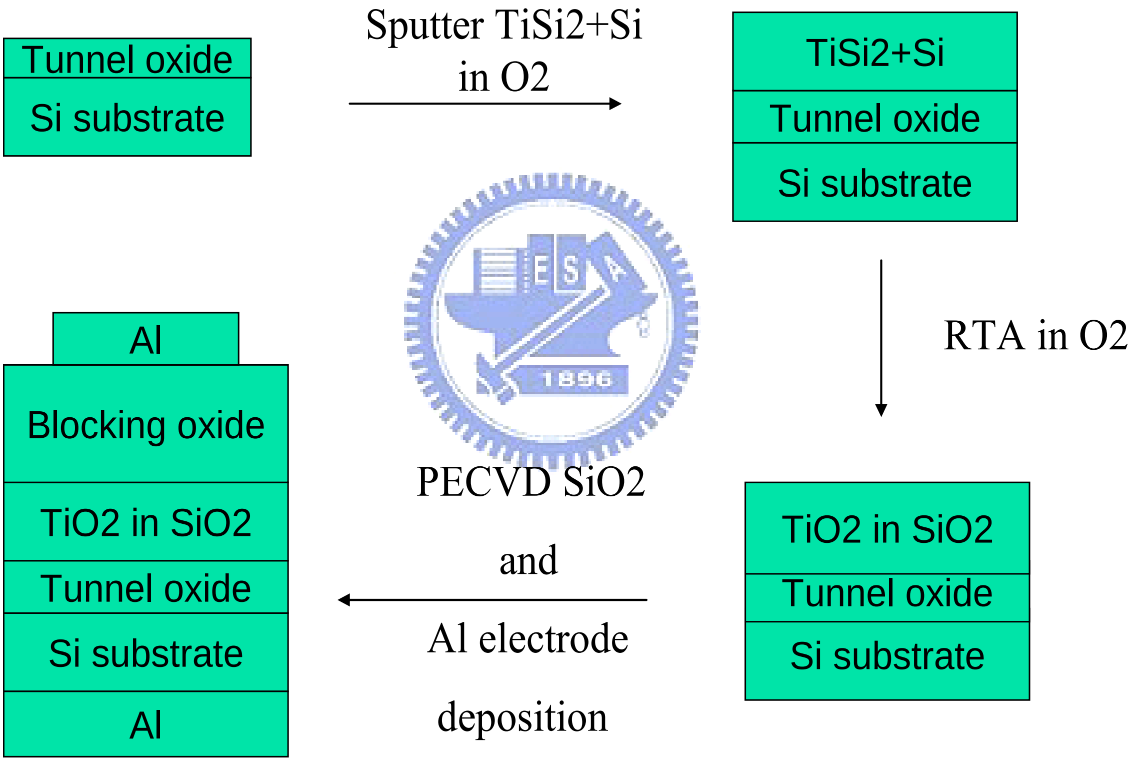


Figure 3-8 Schematics of the experimental procedures with TiSi2 and Si layer.

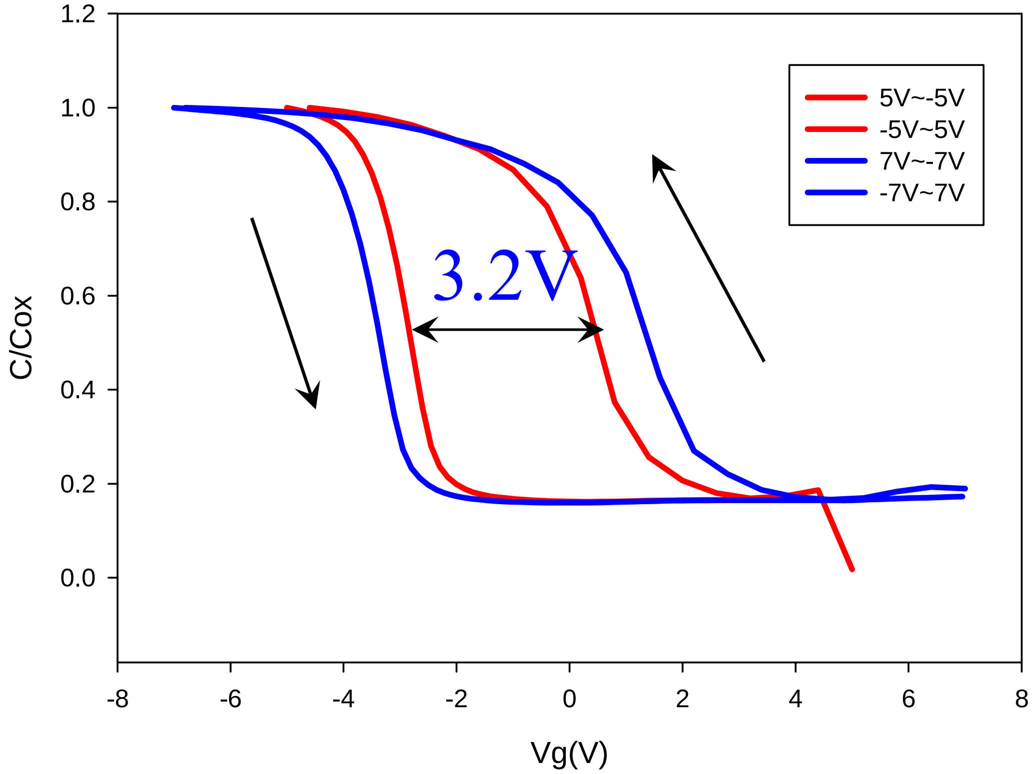


Figure 3-9 Capacitance-voltage (C-V) hysteresis of the fabricated MOIOS structure

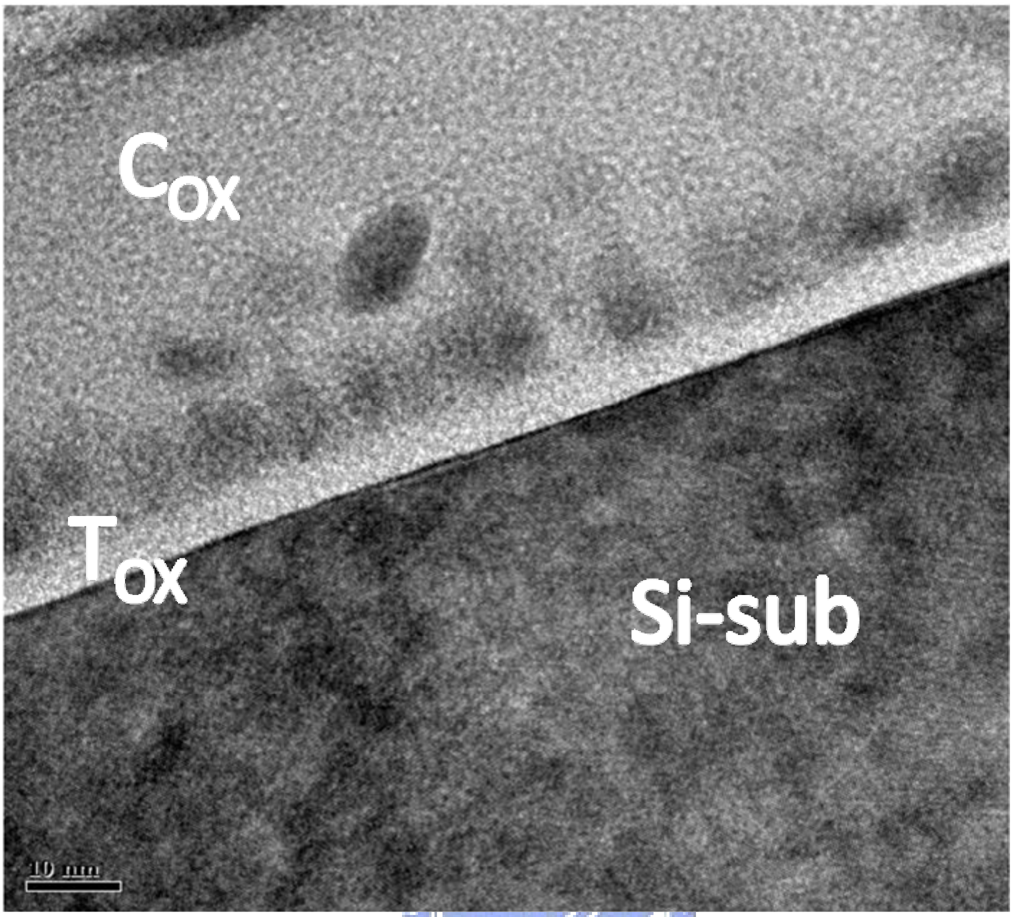


Figure 3-10 Cross-sectional TEM images of the MOIOS structure with TiSi2 and Si RTA in O2

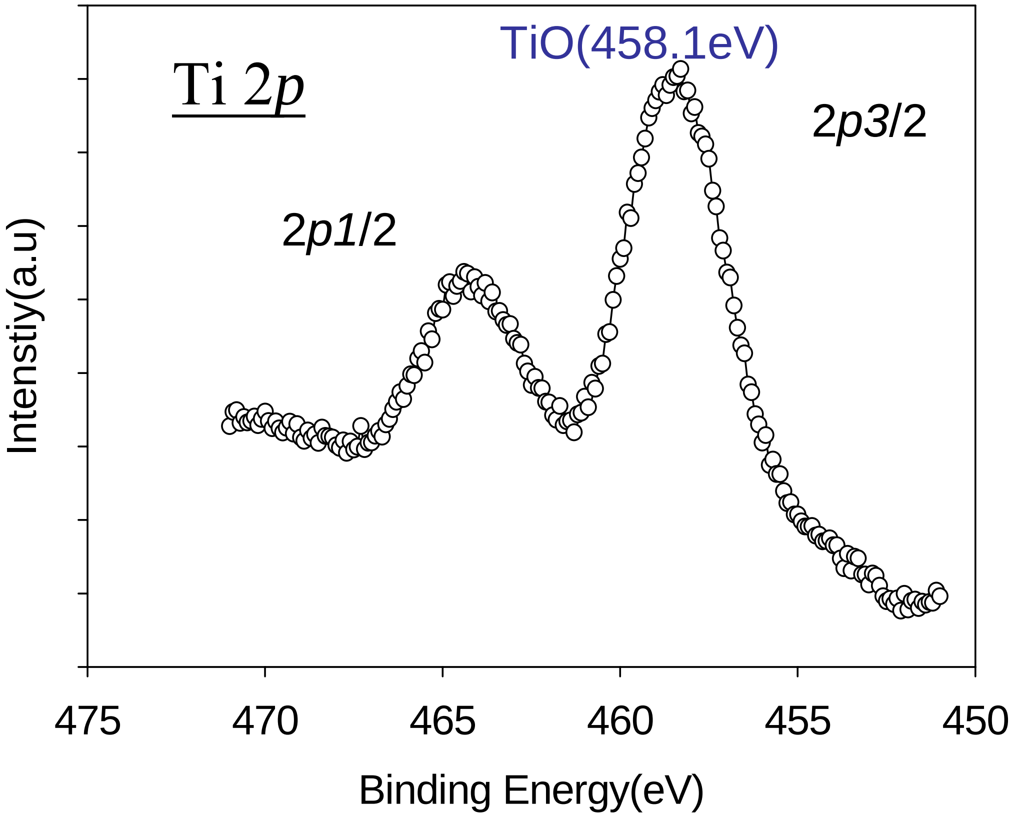


Figure 3-11 Ti 2*p* XPS analysis of TiSi2 and Si layer. The peak position Ti $2p_{3/2}$ are similar to Ti-O signal.

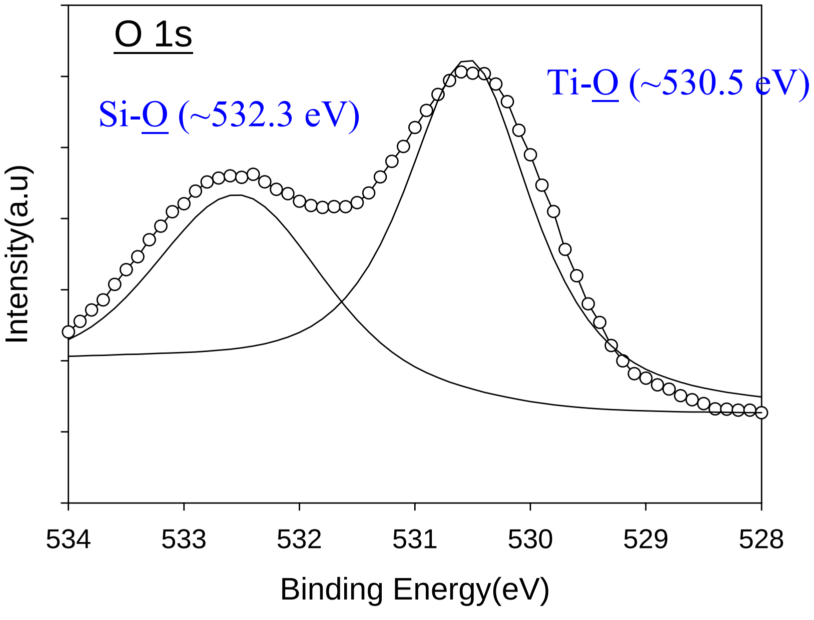


Figure 3-12 O 1*s* XPS analysis of TiSi2 and Si layer. The main peak can be composed into two components which center at 530.5 eV and 532.3 eV corresponding to Ti-O bond and Si-O-Si bond.

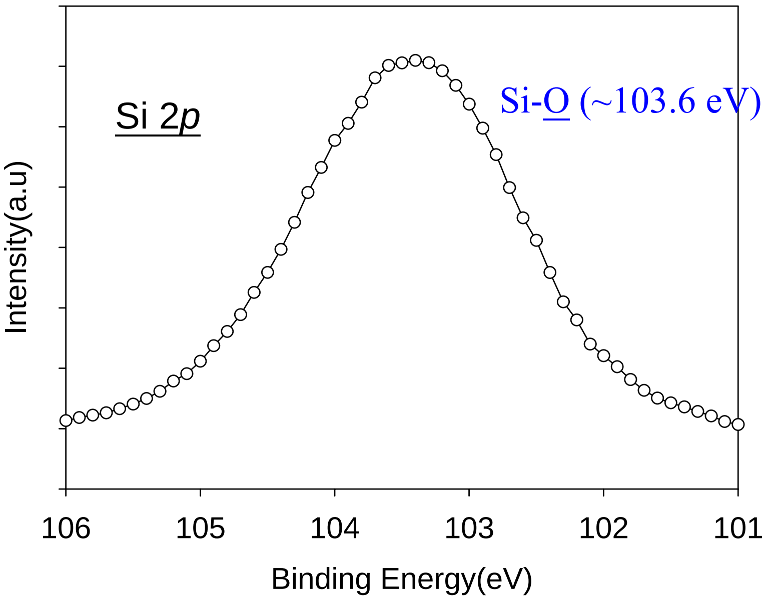


Figure 3-12 Si 2p XPS analysis of the TiSi2 and Ge layer. The main peak at 103.6 eV corresponding to SiO2.

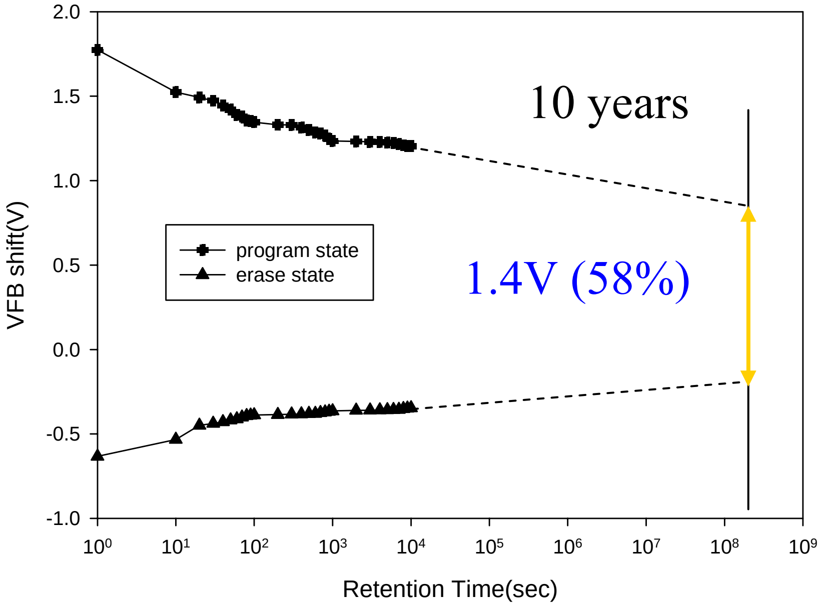


Figure 3-13 Data retention characteristics of the Ni-Si-O nanocrystal memory at room temperature.

➢ Stress condition V_G-V_{FB}= ± 5V 0.1 ms

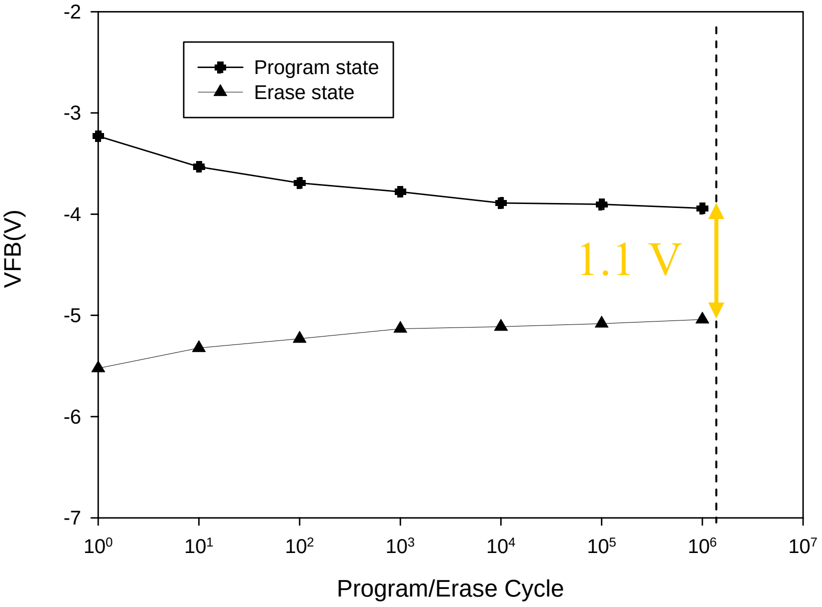


Figure 3-14 Endurance characteristics of the Ni-Si-O nanocrystal memory.

3.4 Nonvolatile Titanium oxide Nanocrystal Memory by TiSi2 and SiO2 layer

3.4.1 Experimental Procedures

Figure 3-1(a) exhibit schematics of the experimental procedures. This nonvolatile memory-cell structure in this letter was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 5-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 50-A-thick charge tapping layer was deposited by reactive sputtering of $TiSi_2$ and SiO_2 (1:1) co-mix target in the Ar and O_2 (24 standard cubic centimeters per minute (sccm)) ambiance at room temperature. This step can obtain an oxygen incorporated $TiSi_2$ and SiO_2 layer as a charge trapping layer in our memory structure. Next, the rapid thermal annealing (RTA) process was performed in nitrogen (N_2) atmosphere. The annealing conditions are 500°C for 120 sec. Then, a 40-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300°C. During the foregoing process, the TiO_2 nanocrystals could be found to precipitate and embed in SiO_2 layer. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure.

Electrical characteristics, including the capacitance-voltage (C-V), retention, and endurance characteristics, were also performed. The C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

Results and Discussion

Figure X-X exhibits a cross-sectional HRTEM image of the nitrogen incorporated $TiSi_2$ and SiO_2 layer containing spherical and separated nanocrystals embedded in the SiO_2 matrix. It is found that the thickness of tunnel oxide is larger than 3 nm, due to the contribution of SiO_2 layer by HRTEM analysis. This SiO_2 matrix can be used to improve charge storage ability for nonvolatile memory application [3.19]. Moreover, the average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 1.08×10^{12} cm^{-2} by HRTEM analysis.

To further investigate the nanocrystals, we have performed XPS analysis by using an Al $K\alpha$ (1486.6 eV) X-ray radiation to demonstrate the chemical composition of the nanocrystals. To correct possible charging effect of the film, the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. Figure 3-9 shows the XPS Ti 2*p* core-level photoemission spectra which consist of two main peaks, $2p_{3/2}$ (~ 464.5 eV) and $2p_{1/2}$ (~ 458.1 eV), with two small satellite peak. However, above-mentioned peak signals are not obviously observed at the Ti $2p_{1/2}$ peak by XPS analysis. By the fitting result of binding energy, it is found that TiO_2 nanocrystals exist in our layer. By the fitting result of binding energy, it is found that the main peak at 103 eV corresponding to

Si–O bond.

The typical capacitance-voltage (*C-V)* hysteresis obtained with gate voltage from accumulation to inversion and in reverse is shown in Fig. 3-10. It is clearly observed that 5.6 V and 8.1 V memory windows can be obtained under ±5 V and ±7 V operation, respectively. The MOIOS structure with the TiO_2 nanocrystals embedded in SiO_2 matrix exhibits clear counterclockwise hysteresis by a flat band voltage (V_{FB}) shift, indicating the significant memory effect. We consider that the charges can be stored in both the TiO_2 nanocrystal and the SiO_2 traps. Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate. Hence, this memory window of Ti-O nanocrystals embedded in SiO_2 matrix is enough to be defined "1" and "0" states.

Retention characteristics of the memory structure with TiO_2 nanocrystals are illustrated in Fig. 3-11. The retention measurements are performed at room temperature by operating a ±10 V gate voltage stress for 5 s. The flat band voltage shift is obtained by comparing the *C-V* curves from a charged state and the quasi-neutral state. Moreover, carriers trapped in the shallow traps are unstable and can easily leak back to the silicon substrate. It is found that the window of V_{FB} significantly reduces during the first 100 s, and becomes more stable for long retention time. This result is consistent with partial carriers trapping in the shallow trap state of the SiO_x matrix around the nanocrystals. However, the long-term extrapolated gives a memory window of 1.8V (total charge loss ratio 63%) after ten years. The majority carriers stored in the deep trapping states of TiO_2 nanocrystals surrounding with SiO_2 matrix exhibit good retention characteristics.

Endurance characteristics for TiO nanocrystals embedded in SiO_2 matrix are shown in Fig. 3-12. Pulses (V_G - V_{FB} = ± 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. An obvious difference of two logical states can be maintained until 10^4 P/E cycles. Subsequently, the closure of window between two logical states appears after 10^4 P/E cycles. We consider that this closure is caused by the degradation of SiO_2 dielectric. However, this memory structure exhibits better endurance characteristics than Ti-Si-O nanocrystal memory. Consequently, it retains a large window of 1V which is enough to define “1” and “0” of memory state.

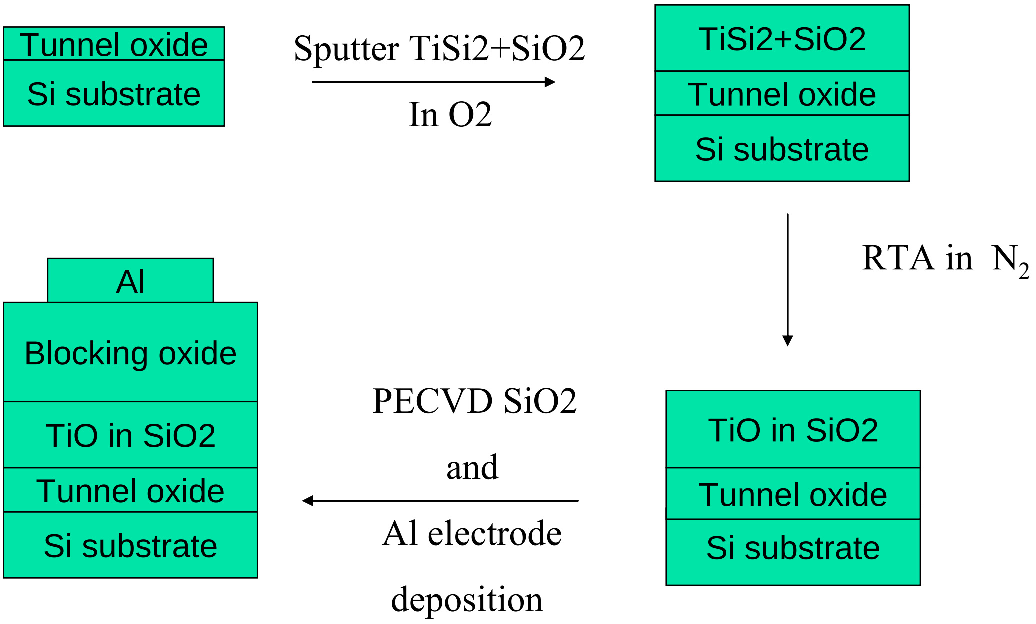


Figure 3-15 Schematics of the experimental procedures with TiSi2 and SiO2 layer.

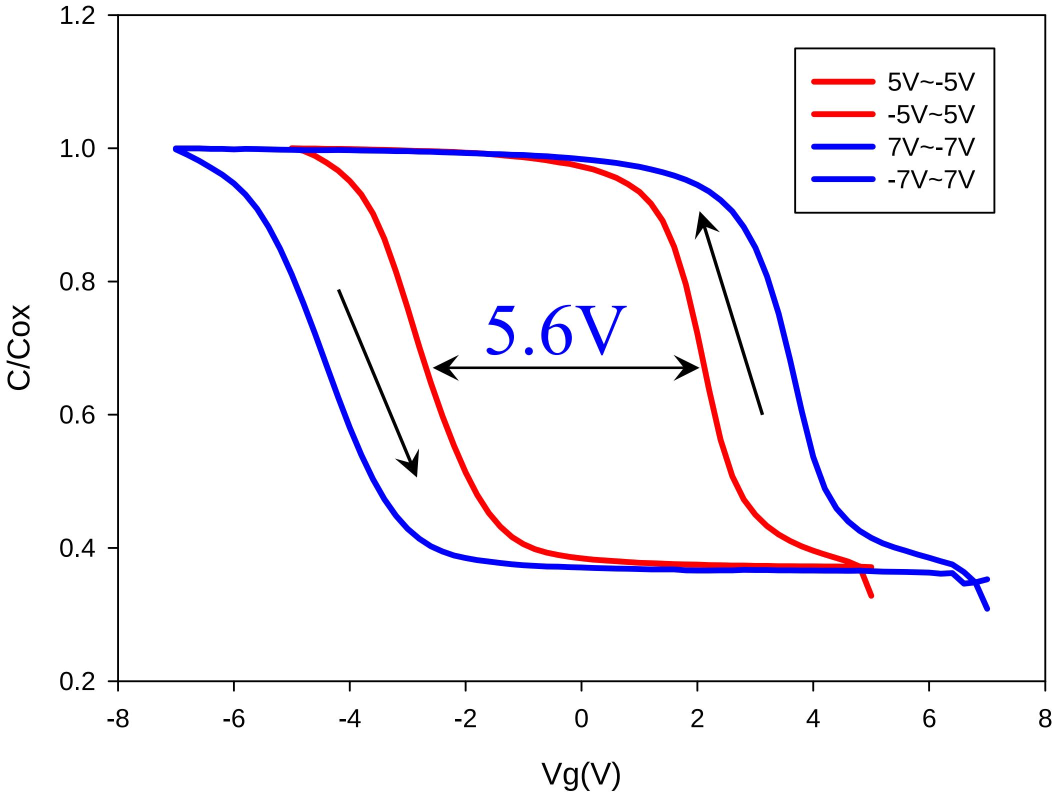


Figure 3-16 Capacitance-voltage (C-V) hysteresis of the fabricated MOIOS structure with TiSi2 and SiO2.

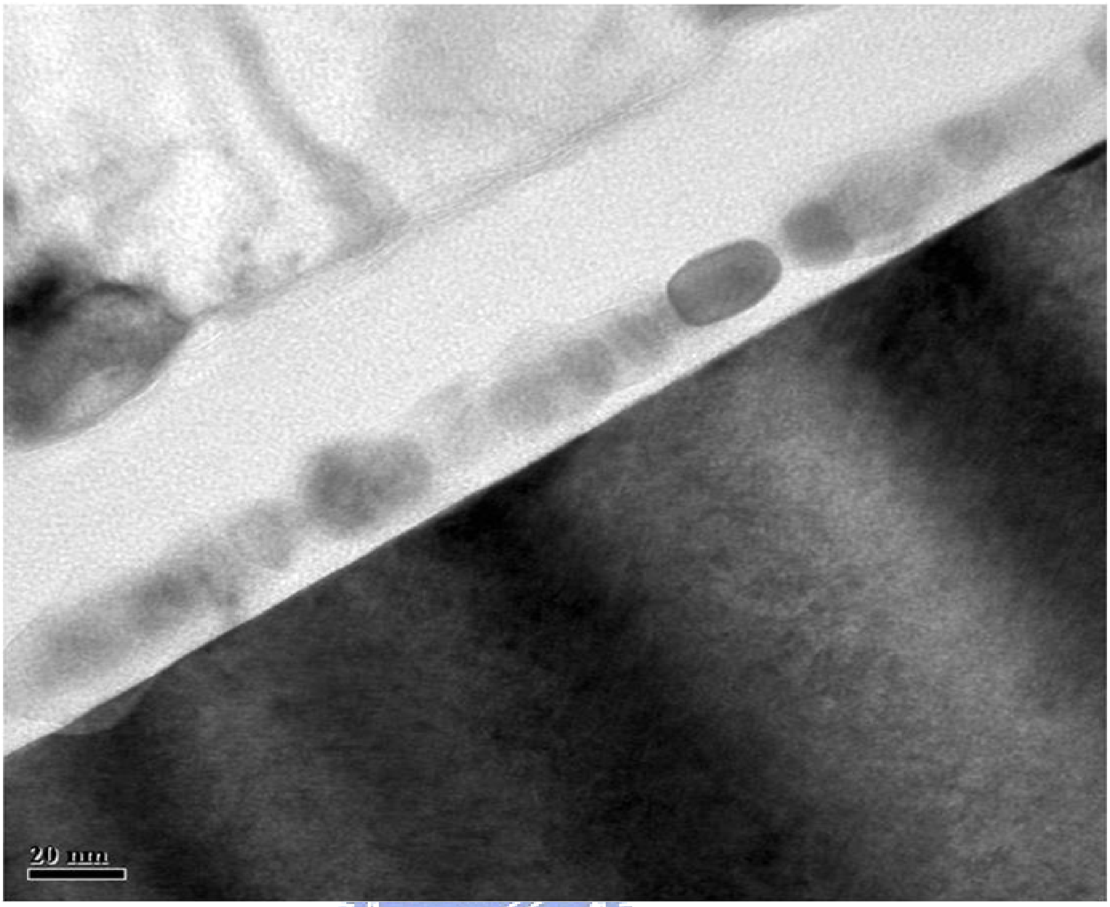


Figure 3-17 Cross-sectional TEM images of the MOIOS structure with Ti-O nanocrystals

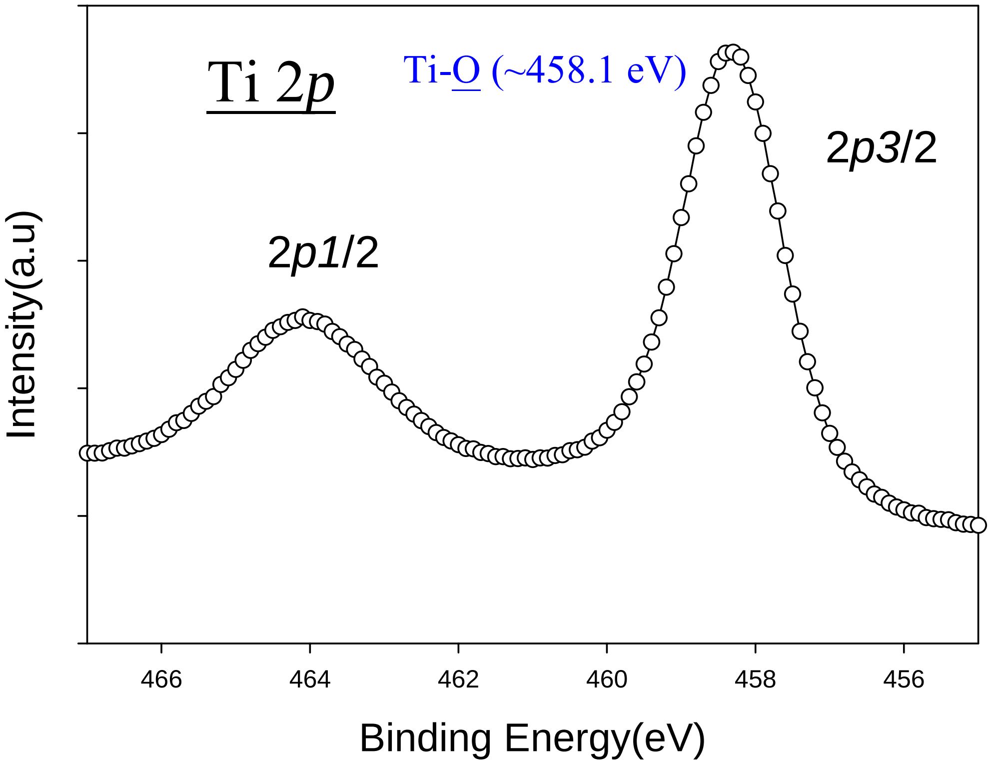


Figure 3-18 Ti 2*p* XPS analysis of the TiSi2 and SiO2 layer. The peak position and profile of Ti $2p_{3/2}$ are similar to Ti -O signal.

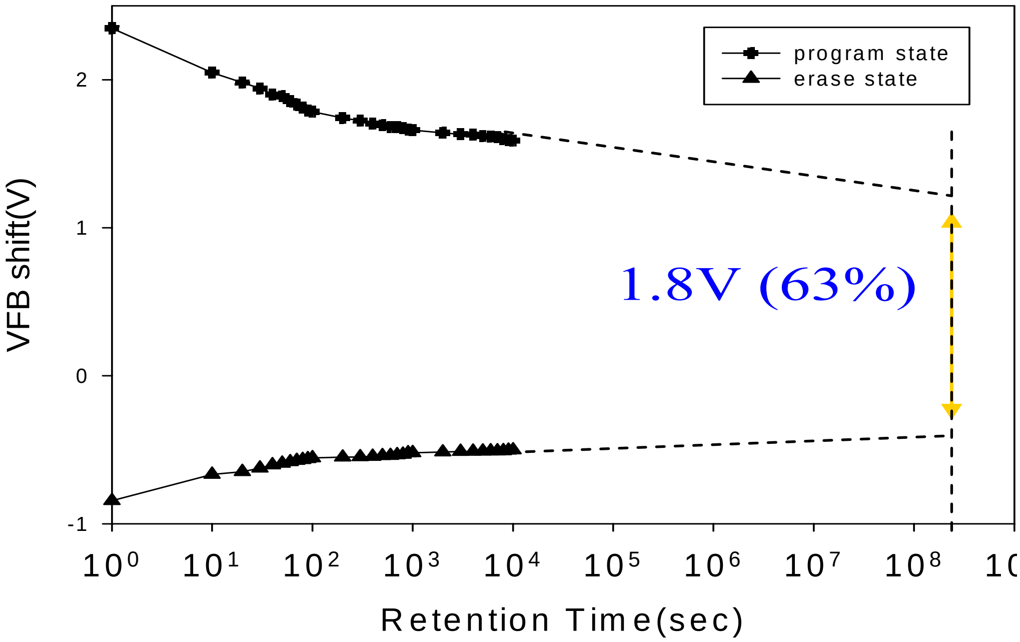


Figure 3-19 Data retention characteristics of the T-O nanocrystal memory at room temperature.

➢ Stress condition V_G-V_{FB}= ± 5V 0.1 ms

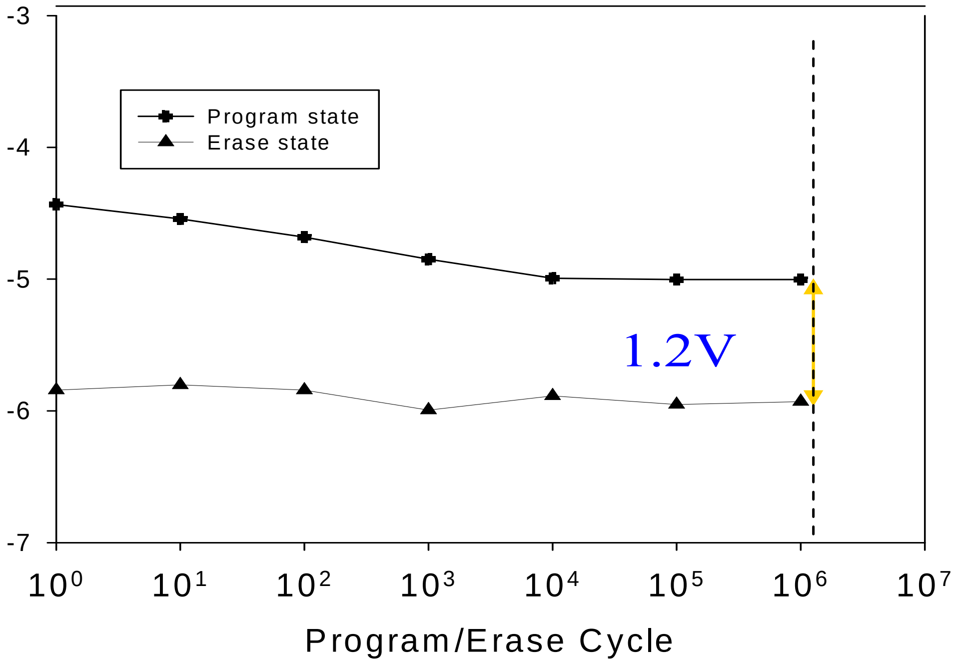


Figure 3-20 Endurance characteristics of the Ti-O nanocrystal memory.

3.5 Summary

The nonvolatile memory structure of TiO_2 nanocrystals embedded in the SiO_2 layer was fabricated by annealing TiSi layers at RTA. The high density and good uniformity nanocrystals can be fabricated through this simple process. The memory window of Ti-Si nanocrystals is large enough to define “1” and “0” for the nonvolatile memory application. The retention characteristic are good enough to be maintained after 10 years. In addition, this new fabrication technique of TiO_2 nanocrystals can be compatible with modern manufacture process of the integrated circuit manufacture.

	Memory window (under ± 5V)	Memory window after 10 years	Memory window after 10^6 P/E cycles
TiSi+Si RTA in N2	2.2V	1.2V(40%)	1.1V
TiSi2+Si RTA in O2	3.2V	1.4V(58%)	1.1V
TiSi2+SiO2 RTA in N2	5.6V	1.8V(63%)	1.2V

Table 3-1 electric characteristics comparison of TiSi+Si RTA in N2 and TiSi2+Si RTA in O2 and TiSi2+SiO2 RTA in O2.

Chapter 4

4.1 Nonvolatile Titanium oxide Nanocrystal Memory by TiSi2 and Ge layer

4.1.1 Experimental Procedures

Figure exhibit schematics of the experimental procedures. This nonvolatile memory-cell structure in this letter was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 5-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 50-A-thick charge tapping layer was deposited by reactive sputtering of $TiSi_2$ and Ge (1:1) co-mix target in the Ar and O_2 (24 standard cubic centimeters per minute (sccm)). This step can obtain an oxygen incorporated $TiSi_2$ and Ge layer as a charge trapping layer in our memory structure. Next, the rapid thermal annealing (RTA) process was performed in nitrogen (N_2) atmosphere. The annealing conditions are 500^{o}C for 120 sec. Then, a 40-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300^{o}C. During the foregoing process, the TiO_2 and Ge nanocrystals could be found to precipitate and embed in SiO_2 layer. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure.

Electrical characteristics, including the capacitance-voltage (C-V), retention, and endurance characteristics, were also performed. The C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 100 kHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

Results and Discussion

Figure X-X exhibits a cross-sectional HRTEM image of the nitrogen incorporated TiSi2 and Ge layer containing spherical and separated nanocrystals embedded in the SiO_2 matrix. It is found that the thickness of tunnel oxide is larger than 3 nm, due to the contribution of SiO_2 layer by HRTEM analysis. This SiO_2 matrix can be used to improve charge storage ability for nonvolatile memory application [3.19]. Moreover, the average diameter of the nanocrystals the area density of the nanocrystals is estimated to be about 1.48×10^{12} cm^{-2} by HRTEM analysis.

To further investigate the nanocrystal, we have performed XPS analysis by using an Al $K\alpha$ (1486.6 eV) X-ray radiation to demonstrate the chemical composition of the nanocrystals. To correct possible charging effect of the film, the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. Figure 3-9(a) shows the XPS Ti $2p$ core-level photoemission spectra which consist of two main peaks, $2p_{3/2}$ (~ 464.5 eV) and $2p_{1/2}$ (~ 458.3 eV), with two small satellite peak. However, above-mentioned peak signals are not obviously observed at the Ti $2p_{1/2}$ peak by XPS analysis. Due to the strong electronegativity of nitrogen atom, it is reasonably assumed that the larger Ti $2p_{1/2}$ binding energy (~ 458.2 eV) of the nanocrystals can be assigned to Ti–Si–O ternary bond.

This result of the XPS Ge 3d photoemission spectra, as shown in Fig.XXX, by fitting result of binding energy, it is found that the main peak can be compose of two components which center at 29eV and 32eV corresponding to Ge bond and Ge-O bond respectively.

This result is also supported by the XPS Si 2p photoemission spectra, as shown in Fig. 3-9(b). By the fitting result of binding energy, it is found that the main peak can be compose into two components which center at 103 eV corresponding to Si–O bond.

The typical capacitance-voltage (*C-V)* hysteresis obtained with gate voltage from accumulation to inversion and in reverse is shown in Fig. 3-10. It is clearly observed that 3.2 V and 6.1 V memory windows can be obtained under ±4 V and ±6 V operation, respectively. The MOIOS structure with the Ti-Si-O and Ge nanocrystals embedded in SiO_x matrix exhibits clear counterclockwise hysteresis by a flat band voltage (V_{FB}) shift, indicating the significant memory effect. We consider that the charges can be stored in both the Ti-Si-O nanocrystal and the Ge nanocrystal. Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate. Hence, this memory window of Ti-Si-O and Ge nanocrystals embedded in SiO_x matrix is enough to be defined “1” and “0” states.

Retention characteristics of the memory structure with Ti-Si-O and Ge nanocrystals are illustrated in Fig. 3-11. The retention measurements are performed at room temperature by operating a ±10 V gate voltage stress for 5 s. The flat band voltage shift is obtained by comparing the *C-V* curves from a charged state and the quasi-neutral state. When carriers are stored in the nanocrystals, the stored charges will raise the nanocrystal potential energy and increase the probability of escaping from the nanocrystal to the silicon substrate [3.23]. Moreover, carriers trapped in the shallow traps are unstable and can easily leak back to the silicon substrate. It is found that the window of V_{FB} significantly reduces during the first 100 s, and becomes more stable for long retention time. This result is consistent with partial carriers trapping in the shallow trap state of the SiO_2 matrix around the nanocrystals. However, the long-term extrapolated gives a memory window of 1.2V (total charge loss ratio 60%) after ten years. The majority carriers stored in the deep trapping states of Ti-Si-O and Ge nanocrystals surrounding with SiO_2 matrix exhibit good retention characteristics.

Endurance characteristics for Ti-Si-O and Ge nanocrystals embedded in SiO_x matrix are shown in Fig. 3-12. Pulses ($V_G - V_{FB} = \pm 5$ V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. An obvious difference of two logical states can be maintained until 10^4 P/E cycles. Subsequently, the closure of window between two logical states appears after 10^4 P/E cycles. We consider that this closure is caused by the degradation of SiO_2 dielectric. However, this memory structure exhibits better endurance characteristics than Ti-Si-O nanocrystal memory. Consequently, it retains a large window of 1V which is enough to define “1” and “0” of memory state.

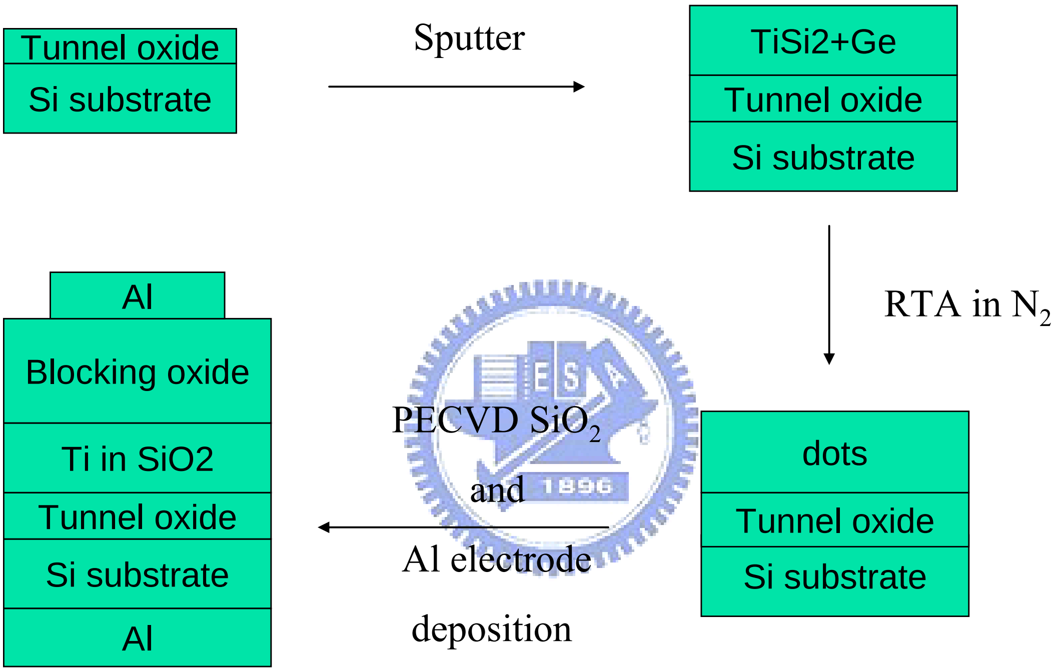


Figure 4-1 Schematics of the experimental procedures with TiSi2 and Ge layer.

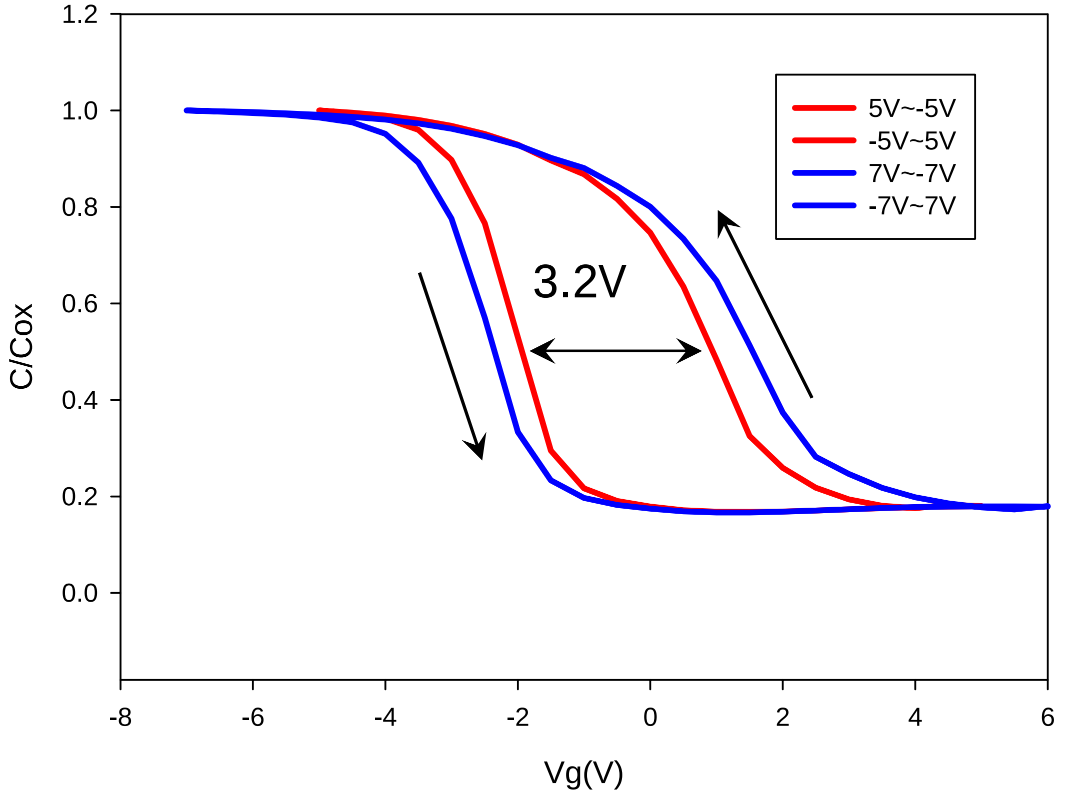


Figure 4-2 Capacitance-voltage (C-V) hysteresis of the fabricated MOIOS structure with TiSi2 and Ge.

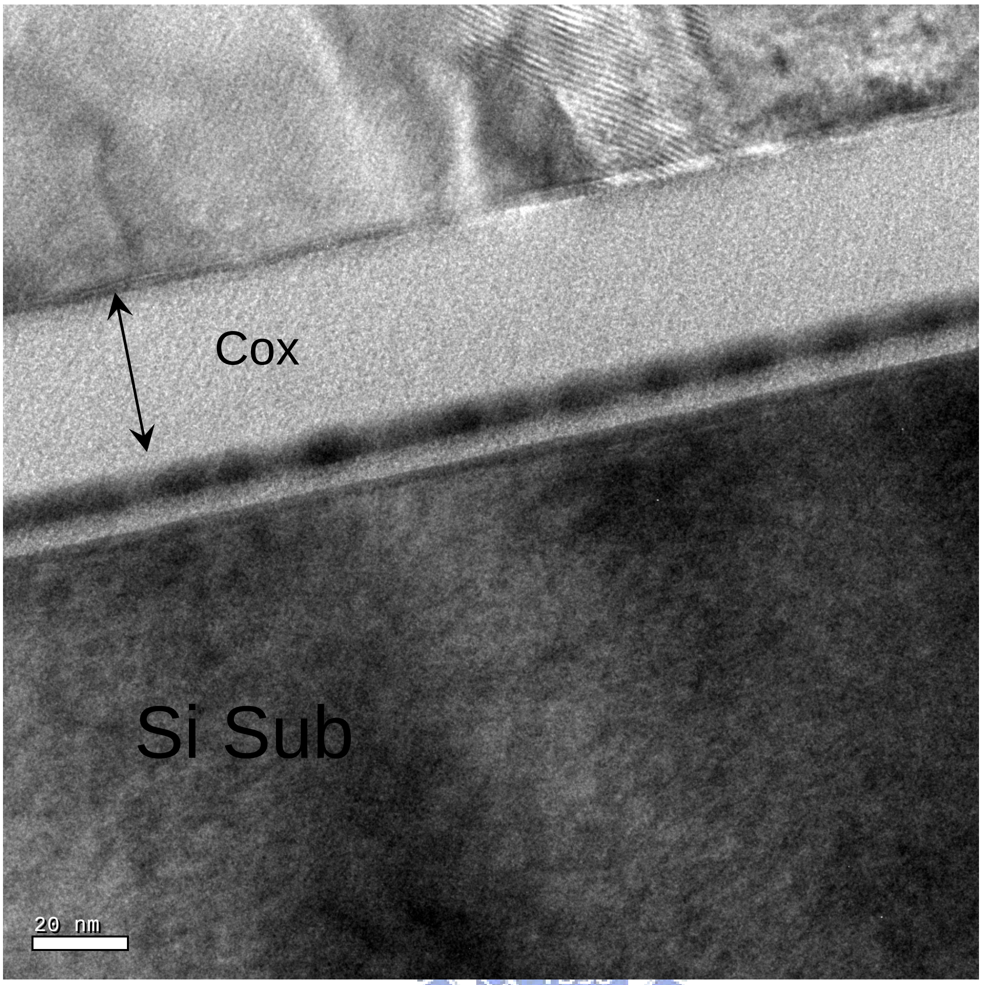


Figure 4-3 Cross-sectional TEM images of the MOIOS structure with TiSi2 and Ge.

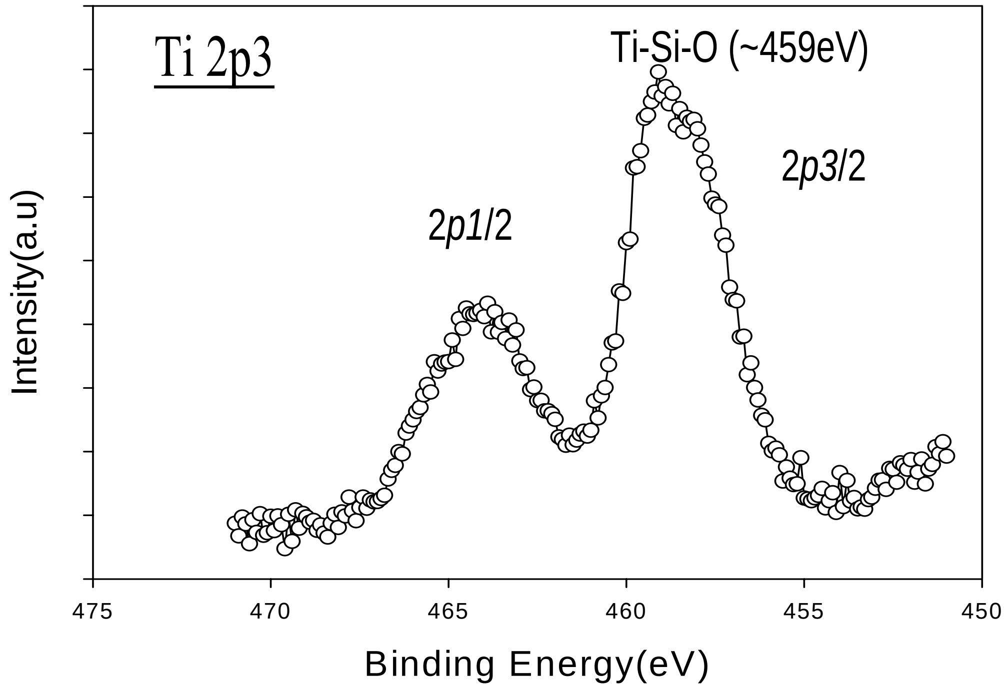


Figure 4-4 Ti 2*p* XPS analysis of TiSi2 and Ge layer. The peak position and profile of Ti 2$p_{3/2}$ are similar to Ni-Si-O signal

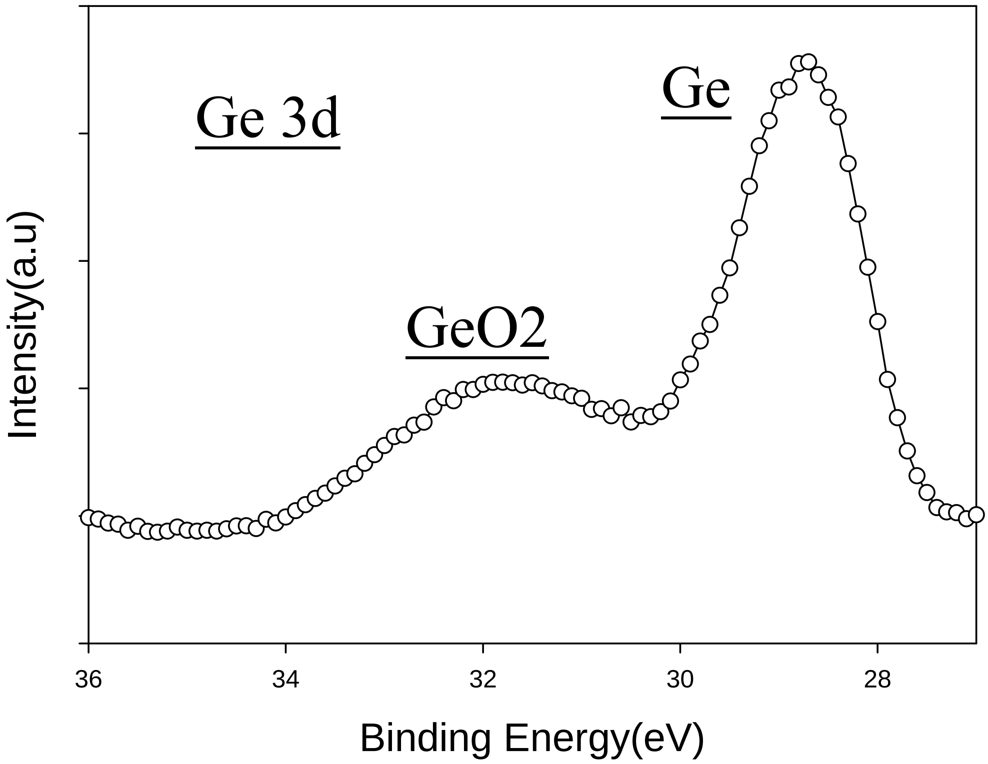


Figure 4-5 Ge 3d XPS analysis of TiSi2 and Ge layer. The peak position and profile

compose of Ge and GeO2.

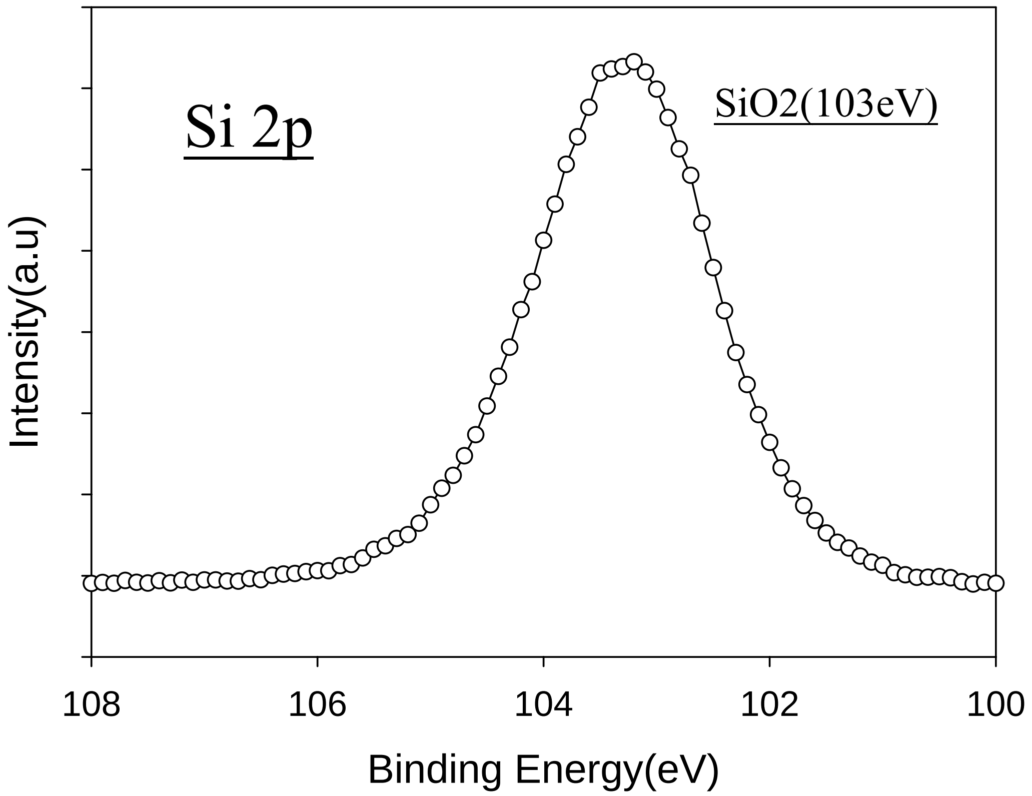


Figure 4-6 Si 2p XPS analysis of the TiSi2 and Ge layer. The main peak at 103 eV corresponding to SiO2.

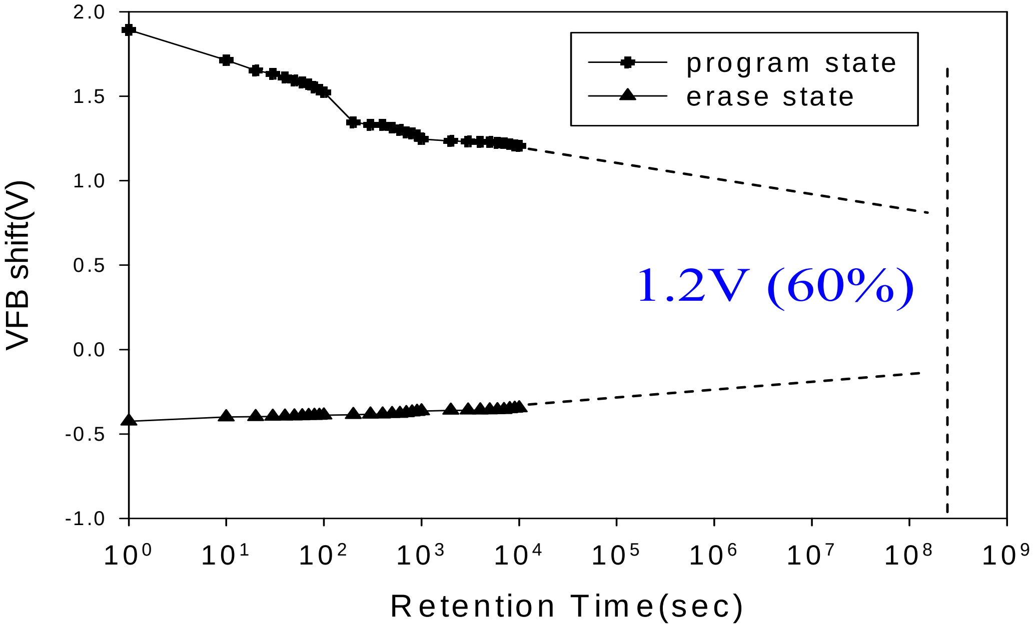


Figure 4-7 Data retention characteristics of the Ti-Si-O nanocrystals memory at room temperature.

➢ Stress condition V_G-V_{FB}= ± 5V 0.1 ms

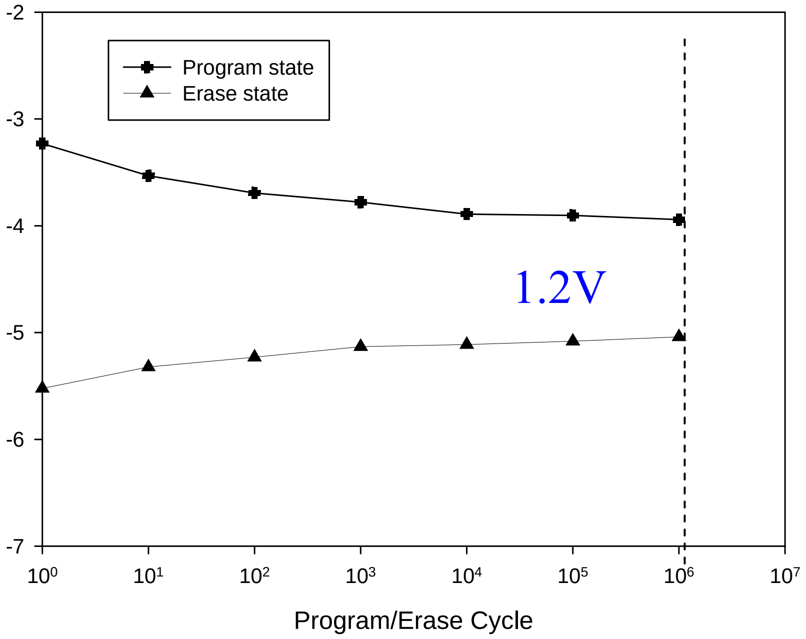


Figure 4-8 Endurance characteristics of the Ti-Si-O nanocrystal memory.

	Memory window	Retention	Endurance
TiSi+Si RTA in N2	1.9V	(40%)	1.1V
TiSi+Ge RTA in N2	3.2V	(60%)	1.2V

Table 3-2 electric characteristics comparison of TiSi+Si RTA in N2 and TiSi2+Ge RTA in N2

Chapter 5

Conclusions

5.1 Conclusions

In this thesis, a novel and ease fabrication technique of Ti-Si-O and TiO2 nanocrystals was demonstrated for the application of nonvolatile memory. The nonvolatile memory structure of Ti-Si-O nanocrystals embedded in the SiO_2 layer was fabricated by sputtering a co-mix target (TiSi2 and Si) in an Ar/O_2 environment at room temperature. Then rapid thermal annealing in N_2. It can be considered that the oxygen plays a critical role during sputter process for the formation of nanocrystal. The high density (~10^{12} cm^{-2}) nanocrystal can be simple and uniform to be fabricated. Another similar process for TiO_2 nanocrystals is also proposed by sputtering a co-mix target ($TiSi_2$ and Si) in the argon (Ar) and oxygen (O_2) mix-gas environment at room temperature. Then rapid thermal annealing in O_2. It was also found that high density TiO_2 nanocrystals embedded in the silicon oxide (SiO_2). This fabrication technique for the application of nonvolatile nanocrystal memory can be compatible with current manufacture process of the integrated circuit manufacture.

A rapid thermal annealing (RTA) in O_2 is used to improve the crystalline quality of nanocrystals and memory characteristic. During the RTA in O_2 process, the TiO_2 nanocrystals precipitate and show good crystalline quality. The TiO_2 nanocrystal with good crystalline quality has higher density of states to store charge and cause larger memory window. The reliability issues, such as retention and endurance, are significantly improved after the RTA in O_2 process. According the results of TEM analysis and XPS analysis, thermal treatment (RTA) can reduce the defects in the dielectric (SiO_2) which surrounds the nanocrystal. It decreases the probability of charge escaping from the nanocrystal. The quality of dielectric is also strengthened to bear the P/E cycling stress.

In the sputter process, we introduce Ge as storage center that can get better electric characteristics.

References

Chapter 1

[1.1] S. Lai, Future Trends of Nonvolatile Memory Technology, December 2001.

[1.2] S. Aritome, IEEE IEDM Tech. Dig., 2000, p.763.

[1.3] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells—An overview" *Proc. IEEE*, vol. 85, pp. 1248–1271, Aug. 1997.

[1.4] Roberto Bez, Emilio Camerlenghi, Alberto Modelli, and Angelo Visconti, "Introduction to Flash Memory" *Proc. IEEE*, vol. 91, NO.4, April 2003.

[1.5] D. Kahng and S. M. Sze, "A floating gate and its application to memory devices", *Bell Syst. Tech,* 46, 1288 (1967).

[1.6] J. D. Blauwe, "Nanocrystal nonvolatile memory devices", *IEEE Transaction on Nanotechnology*, 1, 72 (2002).

[1.7] M. H. White, Y. Yang, A. Purwar, and M. L. French, "A low voltage SONOS nonvolatile semiconductor memory technology", *IEEE Int'l Nonvolatile Memory Technology Conference*, 52 (1996).

[1.8] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE circuits & devices*, 16, 22 (2000).

[1.9] H. E. Maes, J. Witters, and G. Groeseneken, *Proc. 17 European Solid State Devices Res. Conf. Bologna 1987*, 157 (1988).

[1.10] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, "Volatile and non-volatile memories in silicon with nano-crystal storage", *IEEE Int. Electron Devices Meeting Tech. Dig.*, 521 (1995).

[1.11] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee, "Room temperature operation of a quantum-dot flash memory", *IEEE Electron Device Lett.*, 18, 278

(1997).

[1.12] Y. C. King, T. J. King, and C. Hu, “MOS memory using germanium nanocrystals formed by thermal oxidation of $Si_{1-x}Ge_x$”, *IEEE Int. Electron Devices Meeting Tech. Dig.*, 115 (1998).

[1.13] H.A.R. Wegener, A.J. Lincoln, H.C. Pao, M.R. O’Connell, and R.E. Oleksiak, The variable threshold transistor, a new electrically alterable, non-destructive read-only storage device,” *IEEE IEDM Tech. Dig.*, Washington, D.C., 1967.

[1.14] T.Y.Chan, K.K.Young and C.Hu, “A true single-transistor oxide- nitride-oxide EEPROM device”. *IEEE Electron Device Letters*, vol.8, no.3, pp.93-95, 1987.

[1.15] M.K. Cho and D.M.Kim, “High performance SONOS memory cells free of drain turn-on and over-erase: compatibility issue with current flash technology”, *IEEE Electron Device Letters*, pp.399-401, Vol.21, No.8, 2000.

[1.16] I. Fijiwara, H.Aozasa, K.Nomoto, S.Tanaka and T.Kobayashi, “ High speed program/erase sub 100nm MONOS memory cell”, *Proc. 18th Non-Volatile Semiconductor Memory Workshop*, p. 75, 2001.

[1.17] H. Reisinger, M. Franosch, B. Hasler, and T. Bohm, *Symp. on VLSI Tech. Dig.* ,

9A-2, 113 (1997).

[1.18] C. Tung-Sheng, W. Kuo-Hong, C. Hsien, and K. Chi-Hsing, “Performance improvement of SONOS memory by bandgap engineering of charge-trappinglayer”, *IEEE Electron Device Lett.*, vol. 25, no. 3, pp.205–207, Mar. 2004.

[1.19] Y. N. Tan, W. K. Chim, and B. J. Cho, W. K. Choi, “Over-Erase Phenomenon in SONOS-Type Flash Memory and its Minimization Using a Hafnium Oxide Charge Storage Layer”, IEEE Transations on Eelectron Devices, vol.51, no.7, July 2004.

[1.20] Min She, Hideki Takeuchi, and Tsu-Jae King, "Silicon-Nitride as a Tunnel Dielectric for Improved SONOS-Type Flash Memory", IEEE Electron Device Letters, vol. 24, no. 5, MAY 2003.

[1.21] Chang-Hyun Lee, Kyu-Charn Park, and Kinam Kim, "Charge-trapping memory cell of SiO_2/SiN/high-*k* dielectric Al_2O_3 with TaN metal gate for suppressing backward-tunneling effect", Applied Physics Letters 87, 073510 (2005)

[1.22] Shih-Ching Chen, Ting-Chang Chang, Po-Tsun Liu, Yung-Chun Wu, and Ping-Hung Yeh, "Nonvolatile polycrystalline silicon thin-film-transistor memory with oxide/nitride/oxide stack gate dielectrics and nanowire channels", Applied Physics Letters 90, 122111 (2007)

[1.23] Peiqi Xuan, Min She, Bruce Harteneck, Alex Liddle, Jefkey Bokor, and Tsu-Jae King, "FinFET SONOS Flash Memory for Embedded Applications", IEEE IEDM 609-612 (2003).

[1.24] Tzu-Hsuan Hsu, Hang Ting Lue, Ya-Chin King, Jung-Yu Hsieh, Erh-Kun Lai, Kuang-Yeu Hsieh, and Chih-Yuan Lu, "A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory", IEEE Electron Device Letters, vol. 28, no. 5, MAY 2007.

[1.25] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and Doug Buchanan, IEDM Tech. Dig., p.521 (1995)

[1.26] J De Blauwe, "Nanocrystal nonvolatile memory devices", IEEE Trans. Nanotechnol, 2002.

[1.27] R. Ohba, N. Sugiyama, K. Uchida, J. Koga, and A. Toriumi, IEEE Trans. Electron Devices **49**, 1392 (2002).

[1.28] Y. C. King, T. J. King, and C. Hu, IEEE Trans. Electron Devices **48**, 696 (2001)

[1.29] Y. Shi *et al.*, in Proceedings of the First Joint Symposium on Opto- and Microelectronic Devices and Circuits, 2000, pp. 142–145.

[1.30] H. G. Yang, Y. Shi, S. L. Gu, B. Shen, P. Han, R. Zhang, and Y. D. Zhang, Microelectron. J. **34**, 71 (2003).

[1.31] Zengtao Liu, Chungho Lee, Venkat Narayanan, Gen Pei, and Edwin Chihchuan Kan, "Metal Nanocrystal Memories—Part I: Device Design and Fabrication", IEEE Trans. Electron Devices, VOL. 49, NO. 9, SEPTEMBER 2002.

[1.32] Chungho Lee, Udayan Ganguly, Venkat Narayanan, and Tuo-Hung Hou, "Asymmetric Electric Field Enhancement in Nanocrystal Memories", IEEE Eelectron Electron Letters, vol. 26, NO. 12, DECEMBER 2005.

[1.33] Jong Jin Leea, Yoshinao Harada Jung, Woo Pyun, and Dim-Lee Kwong "Nickel nanocrystal formation on HfO2 dielectric for nonvolatile memory device applications", Applied Physics Letters 86, 103505 (2005)

[1.34] Wei-Ren Chen, Ting-Chang Chang, Po-Tsun Liu, Po-Sun Lin, Chun-Hao Tu, and Chun-Yen Chang "Formation of stacked Ni silicide nanocrystals for nonvolatile memory application", Applied Physics Letters 90, 112108 (2007)

[1.35] S. K. Samanta, Won Jong Yoo, and Ganesh Samudra, "Tungsten nanocrystals embedded in high-*k* materials for memory application", Applied Physics Letters 87, 113110 (2005)

[1.36] S. K. Samanta, P. K. Singh, Won Jong Yoo, Ganesh Samudra, and Yee-Chia Yeo, "Enhancement of Memory Window in Short Channel Non-Volatile Memory Devices Using Double Layer Tungsten Nanocrystals", IEEE (2005)

[1.37] Shan Tang, Chuanbin Mao, Yueran Liu, and Sanjay K. Banerjee "Protein-Mediated Nanocrystal Assembly for Flash Memory Fabrication", IEEE Trans. on Electron Letters, vol. 54, no. 3, March 2007.

[1.38] L. Guo, E. Leobandung, and S. Y. Chou, "Si single-electron MOS memory with nanoscale floating-gate and narrow channel," in *Int. Electron Devices Meeting Tech. Dig.*, 1996, pp. 955–956.

[1.39] N. Takahashi, H. Ishikuro, and T. Hiramoto, "A directional current switch using silicon electron transistors controlled by charge injection into silicon nano-crystal floating dots," in *Int. Electron Devices Meeting Tech. Dig.*, 1999, pp. 371–374.

[1.40] J. Wahl, H. Silva, A. Gokirmak, A. Kumar, J. J. Welser, and S. Tiwari, "Write, erase and storage times in nanocrystal memories and the role of interface states," in *Int. Electron Devices Meeting Tech. Dig.*, 1999, pp. 375–378.

Chapter 2

[2.1] Chih-Yuan and Chin-Chieh Yeh, "Advenced Non-Volatile Memory Devices with Nano-Technology", *Invited Talk for 15th International Conference on Ion Implantation Technology, 2004.*

[2.2] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, Proceedings of The IEEE, 85, 1248 (1997)

[2.3] M. Woods, Nonvolatile Semiconductor Memories: Technologies, Design, and Application, C. Hu, Ed. New York: IEEE Press, (1991) ch. 3, p.59.

[2.4] T. Ohnakado, H. Onoda, O. Sakamoto, K. Hayashi, N. Nishioka, H. Takada, K. Sugahara, N. Ajika and S. Satoh, "Device characteristics of 0.35 μm P-channel DINOR flash memory using band-to-band tunneling-induced hot electron (BBHE) programming", *IEEE Trans. Electron Devices*, Vol. 46, pp. 1866-1871, 1999.

[2.5] J. Bu, M. H. White, Solid-State Electronics., 45, 113 (2001)

[2.6] M. L. French, M. H. White., Solid-State Electron., p.1913 (1995)

[2.7] M. L. French, C. Y. Chen, H. Sathianathan, M. H. White., IEEE Trans Comp

Pack and Manu Tech part A., 17, 390 (1994)

[2.8] Y. S. Hisamune, K. Kanamori, T. Kubota, Y. Suzuki, M. Tsukiji, E. Hasegawa, A. Ishitani, and T. Okazawa, IEDM Tech. Dig., p.19 (1993)

[2.9] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, IEEE Transactions of Electron Devices., 49, 1606 (2002)

[2.10] J. Moll, Physics of Semiconductors. New York: McGraw-Hill, (1964)

[2.11] M. Lezlinger and E. H. Snow, J. Appl. Phys., 40, 278 (1969)

[2.12] Christer Sevensson and Ingemar Lundstrom, J. Appl. Phys., 44, 4657 (1973)

[2.13] P. E. Cottrell, R. R. Troutman, and T. H. Ning, IEEE J. Solid-State Circuits, 14, 442 (1979)

[2.14] C. Hu, IEDM Tech. Dig., p.22. (1979)

[2.15] S. Tam, P. K. Ko, C. Hu, and R. Muller, IEEE Trans. Elec. Dev., 29, 1740 (1982)

[2.16] I. C. Chen, C. Kaya, and J. Paterson, IEDM Tech. Dig., p.263 (1989)

[2.17] I. C Chen, D. J. Coleman, and C. W. Teng, IEEE Elec. Dev. Lett., 10, 297 (1989)

[2.18] T. Ohnakado, K. Mitsunaga, M. Nunoshita, H. Onoda, K. Sakakibara, N. Tsuji, N. Ajika, M. Hatanaka and H. Miyoshi, IEDM Tech. Dig., p.279 (1995)

[2.19] Suk-Kang Sung, I1-Han Park, Chang Ju Lee, Yong Kyu Lee, Jong Duk Lee, Byung-Gook Park, Soo Doo Chae, and Chung Woo Kim, "Fabrication and Program/Erase Characteristics of 30-nm SONOS Nonvolatile Memory Devices, " IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL.2, NO.4, DECEMBER 2003.

[2.20] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, Proceedings of The IEEE, 85, 1248 (1997)

[2.21] D. Ielmini, A. Spinelli, A. Lacaita, and A. Modelli, "Statistical model of reliability and scaling projections for Flash memories," in *IEDM Tech. Dig.*, 2001, pp.32.2.1–32.2.4.

[2.22] D. Ielmini, A. S. Spinelli, A. L. Lacaita, L. Confalonieri, and A. Visconti,"New technique for fast characterization of SILC distribution in Flash arrays," in *Proc. IRPS*, 2001, pp. 73–80.

[2.23] D. Ielmini, A. S. Spinelli, A. L. Lacaita, R. Leone, and A. Visconti, "Localization of SILC in Flash memories after program/erase cycling," in *Proc. IRPS*, 2002, pp. 1–6.

[2.24] Y. M. Niquet, G. Allan, C. Delerue and M. Lannoo, "Quantum confinement in germanium nanocrystals," *Applied Physics Letters*, vol.77, pp.1182-1184 (2000)

[2.25] T. Takagahara and K.Takeda, "Theory of the quantum confinement effect on excitons in quantum dots of indirect- gap materials," *Phys. Rev. B*, Vol. 46, p. 15578, 1992.

[2.26] J.D.Jackson, "Classcial Electrodynamics", published by John Wiley & Sons, 1999.

Chapter 3

[3.1] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, Proceedings of the IEEE **91**, 4 (2003).

[3.2] J. D. Blauwe, IEEE Trans. Nanotechnol. **1**, 72 (2002).

[3.3] C. Y. Lu, T. C. Lu, and R. Liu, Proceedings of 13th IPFA (2006).

[3.4] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, IEDM Tech. Dig. 521 (1995).

[3.5] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, IEEE Trans. Electron Devices. **49**, 9 (2002).

[3.6] S. K. Samanta, W. J. Yoo, G. Samudra, E. S. Tok, L. K. Bera, and N. Balasubramanian, Appl. Phys. Lett. **87**, 113110 (2005).

[3.7] T. C. Chang, P. T. Liu, S. T. Yan, and S. M. Sze, Electrochem. Solid-State Lett. **8** (3) G71-G73 (2005).

[3.8] J. J. Lee, Y. Harada, J. W. Pyun, and D. L. Kwong, Appl. Phys. Lett. **86**, 103505 (2005).

[3.9] C. C. Wang, J. Y. Tseng, T. B. Wu, L. J. Wu, C. S. Liang, and J. M. Wu, J. Appl. Phys. **99**, 026102 (2006).

[3.10]Ch. Sargentis, K. Giannakopoulos, A. Travlos, and D. Tsamakis, Journal of Physics: Conference Series 10, 53-56 (2005).

[3.11] D. Zhao, Y. Zhu, R. Li, and J. Liu, Solid-State Electronics. **50**, 2 (2006).

[3.12] R.E. dos Santos, I. Doi, J.A. Diniz; J.W. Swart, S.G. dos Santos Filho, “Investigation of Ni silicides formation on (100) Si by X-ray Diffraction (XRD)”, Revista Brasileira de Aplicacoes de Vacuo, v. 23, n. 1, 32-35, 2004.

[3.13] P. H. Yeh, C. H. Yu, and L. J. Chen, H. H. Wu, P. T. Liu, and T. C. Chang, Appl. Phys. Lett **87**, 193504 (2005).

[3.14] Wei-Ren Chen, Ting-Chang Chang, Po-Tsun Liu, Po-Sun Lin, Chun-Hao Tu, and Chun-Yen Chang “Formation of stacked Ni silicide nanocrystals for nonvolatile memory application”, Applied Physics Letters 90, 112108 (2007)

[3.15] C. Lee, T. H. Hou, and E. C. Kan, IEEE Trans. Electron Devices **52**, 12 (2005)

[3.16] D. N. Kouvatsos, V. L. Sougleridis, and A. G. Nassiopoulou, Appl. Phys. Lett. **82**, 397 (2003)

[3.17] R. Zhao, Y. H. Lin, X. Zhou, M. Li, and C. W. Nanb, J. Appl. Phys. **100**, 046102 (2006)

[3.18] A. A. Galuska, J. Vac. Sci. Technol. **A(9)**, 6 (1991)

[3.19] C. Lee, T. H. Hou, and E. C. Kan, IEEE Trans. Electron Devices **52**, 12 (2005)

[3.20] C. D. Wagner, W. M. Riggs, L. E. Davis, J. F. Moulder, and G. E. Muilenberg, Handbook of X-Ray Photoelectron Spectroscopy, Perkin-Elmer Corp., Eden Prairie, MN (1975).

[3.21] I. Crupi, D. Corso, G. Ammendola, S. Lombardo, C. Gerardi, B. DeSalvo, G. Ghibaudo, E. Rimini, and M. Melanotte IEEE Trans. Nanotechnol. **2**, 4 (2003).

[3.22] Y. Wang, Z. W. Fu,X. Li. Yue, and Q. Z. Qin, J. Electrochem. Soc. **151** (4) E162-E167 (2004).

[3.23] C. W. J. Beenakker, Phys. Rev. B **44**, 1646 (1991).

[3.24] D. R. Lide, Handbook of Chemistry and Physics, 81st Edition (2000).

[3.25] E. K. Parks, G. C. Nieman, K. P. Kerns, and S. J. Riley, J. Chem. Phys. **108**, 9 (1998).

[3.26] L. Aballe, L. Gregoratti, A. Barinov, and M. Kiskinovaa, Appl. Phys. Lett. **84**, 24 (2004).

Chapter 4

[4.1] R.E. dos Santos, I. Doi, J.A. Diniz, J.W. Swart, and S.G. dos Santos Filho "INVESTIGATION OF Ni SILICIDES FORMATION ON (100) Si BY X-RAY DIFFRACTION (XRD)" Revista Brasileira de Aplicacoes de Vacuo, v. 23, n. 1, 32-35 (2004)

[4.2] D. N. Kouvatsos, V. L. Sougleridis, and A. G. Nassiopoulou, Appl. Phys. Lett. **82**, 397 (2003)

[4.3] C. D. Wagner, W. M. Riggs, L. E. Davis, J. F. Moulder, and G. E. Muilenberg, Handbook of X-Ray Photoelectron Spectroscopy, Perkin-Elmer Corp., Eden Prairie, MN (1975).

[4.4] J. Kedzierski, *et al*, "Threshold voltage control in NiSigated MOSFETs through silicidation induced impurity segregation (SIIS)", IEDM Tech. Dig., 2003, pp. 315-318.

[4.5] I. Crupi, D. Corso, G. Ammendola, S. Lombardo, C. Gerardi, B. DeSalvo, G. Ghibaudo, E. Rimini, and M. Melanotte IEEE Trans. Nanotechnol. **2**, 4 (2003).

[4.6] Y. Wang, Z. W. Fu,X. Li. Yue, and Q. Z. Qin, J. Electrochem. Soc. **151** (4) E162-E167 (200

簡　歷

姓　　名：王派璿

出生日期：民國七十二年五月二十三日

住　　址：桃園縣平鎮市中豐路山頂段九十巷四十二號

學　　歷：國立交通大學 應用數學系 學士
(2001.09 ~ 2006.02)
國立交通大學 電子工程研究所
固態組 碩士班
(2006.09 ~ 2008.09)