國 立 交 通 大 學

電子工程學系　　電子研究所

碩 士 論 文

原子層沉積高介電係數氧化鋁閘極介電層之

三五族元件電物性研究

Electrical and physical characteristics of III-V devices with atomic-layer-deposited Al_2O_3 high-κ gate dielectric

研　究　生：　江欣哲

指 導 教 授：　簡昭欣 博士

中 華 民 國 九 十 七 年 九 月

原子層沉積高介電係數氧化鋁閘極介電層之三五族元件電物性研究

Electrical and physical characteristics of III-V devices with atomic-layer-deposited Al_2O_3 high-κ gate dielectric

研 究 生：江欣哲　　*Student : Hsin-Che Chiang*

指導教授：簡昭欣 博士　　*Advisor : Dr. Chao-Hsin Chien*

國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering
& Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
In Partial Fulfillment of the Requirements
For the Degree of Master
In
Electronics Engineering
September 2008
Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 七 年 九 月

原子層沉積高介電係數氧化鋁閘極介電層之三五族元件電物性研究

學生：江欣哲　　指導教授：簡昭欣 博士

國 立 交 通 大 學

電子工程學系 電子研究所 碩士班

摘　　要

在這篇文獻中,我們已經最佳化利用硫鈍化處理的方式處理砷化鎵表面,並且成功地使Dit值下降到5E12$cm^{-2}eV^{-1}$。一開始的時候,我們利用XPS方式去分析Ga2p3和As2p3在不同的硫鈍化處理下成份變化情形,我們發現到當我們把硫化濃度和溫度提高時,砷化鎵表面的氧化物會被有效的抑制;同時,我們也觀察到利用硫化氨配合丁醇的方式對於表面氧化物抑制確實比傳統硫化氨配合水來的有效。在另一方面,我們也同時去研究反應頻率的表現在其他三五族砷化銦和砷化銻。對於較小能矽材料來說,相對的它的反應頻率也就越快。對於這篇研究說,利用不同硫化處理的方式在這兩種材料似乎對於氧化物和基板介面並沒有太大改善。針對電容研究的情形,我們最後使用硫化氨加丁醇方式去製作出砷化鎵場效應電晶體來。

此外,我們也使用不同合金材料去做一些歐姆接觸方面的研究,基本上我們是以金-鍺為基底分別鍍上鎳、鍺、金材料,接著利用快速退火的方式達到較低的毆姆接觸。我們發現,當溫度越高時,表面的粗操度也就越大,對於阻值會有一定的影響。

最後,我們綜合前面的結果在半絕緣的基版上面製作金半場效應電晶體和金氧半場效應電晶體。我們已經成功低將電子遷移率提升到 460$cm^{2}V^{-1}S^{-1}$,相對來說還是比較低的值,可能是因為表面蝕刻後粗操度和高濃度摻雜後庫倫散射所造成。因此,我們可以推論出硫化氨加丁醇鈍化方式在表面形成保護層,以及利用氧化物退火的方式去完成較好品

質的場效應電晶體。再之後我們利用超高真空化學氣相沉積的方式去沉積矽鍺緩衝層，利用這種方式使三五族長在矽的基板上去降低材料成本，我們認為這將是未來應用上重要結構, 並且對於後矽時代高遷移率量產上會有所幫助。

Electrical and physical characteristics of III-V devices with atomic-layer-deposited Al_2O_3 high-κ gate dielectric

Student：Hsin-Che Chiang　　Advisors：Dr. Chao-Hsin Chien

Department of Electronics Engineering and Institute of Electronics
National Chiao Tung University

ABSTRACT

In this thesis, we had optimized the sulfide treatment on GaAs surface and also eliminate the surface state to 5E12 ($cm^{-2}eV^{-1}$) successfully. In the beginning, we analyzed the component of Ga 2p3 and As 2p3 photoemission spectra with different sulfide passivation. We found the oxide decrease due to increasing sulfur concentration and process temperature; and we found this solution did result in superior electrical characteristics than the conventional $(NH_4)_2S$ solution (H_2O). On the other hand, we also fabricated the Pt/ALD-Al_2O_3/InSb InAs capacitors to discuss the minority response. The smaller band gap resulted in high transition frequency. Interface density of InSb and InAs were not changeable with any surface treatment in this study. We choose the better condition: $(NH_4)_2S+C_4H_9OH$ at 60 ℃ to fabricate GaAs nMOSFET.

In addition, we also tried different alloy metal material to form S/D ohmic contact. The most common approach to the formation of AuGe-based ohmic contacts is to evaporate layers of Ni, Ge, and Au metals onto the GaAs sample followed by annealing. Obviously, the higher the temperature used, the rougher the top surface and metal-substrate interface was observed.

Finally, we had fabricated MESFET and MOSFET on semi-insulator substrate. The electronic mobility we extracted is 460 $cm^2V^{-1}S^{-1}$; the lower mobility was due to rough surface and Column scattering. Therefore, we conclude that the high quality MOSFET can be achieved integrating $(NH_4)_2S+C_4H_9OH$ and dielectric annealing process. Finally, we grew heavy-doped channel on Si substrate, which can be considered as the potential structure of novel device for metal-oxide-semiconductor field effect transistor application.

誌　謝

兩年的日子說長不長,說短不短,研究所兩年中我想最感謝的是我的指導教授簡昭欣博士,在實驗上讓我有充足的資源可以發揮,並且教導我們正確的研究方法以及嚴謹的態度去探討問題,還有每次meeting都能喝到上等的台灣茶,遇到這樣的好老師,是我們學生的福氣。

其次我要最感謝的是兆欽學長,學長對於研究的執著以及熱忱,都是我學習的目標,還有時間規劃和做事效率,我只能忘其項背跟隨你的腳步,這兩年來遇到很多無法理解的現象,也是和你一一討論而終於豁然開朗,最後還有榮幸到日本去參加conference,我只能說,學長,你真的太照顧我了。明瑞學長和志彥學長,謝謝你們在NDL的幫忙以及meeting上的建議,讓我在報告上面更有信心。世璋學長,雖然很久沒見到面,不過咖啡的日子還有明信片,都讓我在小小碩一的時候生活添加許多樂趣。

接下來是實驗室畢業的學長,阿國和熊哥,在我碩一懵懵懂懂的時候就帶我train各式不同的機台,以及實驗上該注意的事項,有了你們的幫助,往後的實驗讓我順利不少。小劉,有了你的加入,讓我們實驗室增加不少風采,少了你的感覺,我還真的有點不太習慣。家豪學長,你現在已經是實驗室的支柱了,也謝謝學長教我L-EDIT和在實驗上提供我一些寶貴的建議,讓我收益不少,也祝福你往日的實驗也能夠順利。阿壘和漢堡神偷妍心,常常受到你們的照顧,還有去你們Lab吃東西和用機台,以後回來再喝你們的喜酒喔!stone,你讓我見識到強者的威力,也希望你工作能順利。儀科中心的志忠學長,沒有你大力協助,我想我們的實驗很難有所突破,往後的學弟也麻煩你了。蕭副、劉帥、李博、文浩、大致傑、小智傑學長,也謝謝你門在實驗上的建議,讓我可以學到一些不同領域的東西。貴儀的黃繡吟小姐和NDL沈奕玲小姐,謝謝你們XPS和AES上的幫助,讓這篇論文更有可看性。中科院的至宏學長,謝謝你在最後提供MBE磊晶的片子,沒有你鼎力相助,我想現在還只是個半成品。

實驗室的好伙伴,效諭(rain)和胖虎(冏),前者是殺人於無形,功力高深莫測,後者是誹聞製造機,時常都會有新歡出現,實驗室有我們三個好像話題增加了不少,我想沒有

你們我大概會很無聊吧!胖哥,也希望你的黑珍珠能夠順利長大。阿倫和弘森,有了你們,讓我們總是有話題可以討論,搞不好在軍中又可以聚聚囉!宇彥和阿飛,今後也要堅持自己所選的路,也住你們在往後不管是學業或工作都能順利。學弟宗佑,III-V的發揚光大就靠你了,我相信你可以的,政庭、耀昇、大鳥和小豬,實驗室就交給你們把持住了!老高,謝謝你總是在我寂寞的時候介紹許多女生給我,讓我見識到什麼是真男人。阿威,你這個跟我生活一起兩年的好朋友,讓我見識到impossible is nothing,也祝你能早日脫離水生火熱的日子。三平,打牌以後還是要找我喔!趙天生group學長學弟,籃球場上奔跑的日子是我難以忘懷的!阿杰,國軍online後我們一定會再見的;校長實驗室的塞哥、師傅、Joner、吱吱、勾勾揚和陶淵明,無塵室的日子是我一輩子難忘的回憶。還有心卉學姊,你的照顧讓我備受溫暖,怡誠學長,日本妹就靠你了。

大學的好朋友博文、老許、馬保、信雄、佩真、小龜、吉拉、老柯、春薇、阿炮、阿腿以及五家的學長姊們,回台北的日子有你們陪伴真好!

最後,我想感謝我的家人,江錦發先生和吳瓊珠小姐,不果是精神方面或者是物質方面,都讓我無後顧之憂,老哥明晏,也在我這個任性的弟弟下包容我不少。誌謝的最後,我想謝謝妳,謝謝妳讓我懂得珍惜,讓我成長不少。謹以此篇論文獻給所有幫助過我的人,謝謝你們。

江欣哲

於　新竹國立交通大學

2008 年 9 月

Contents

Chapter 3

Alloyed Source/Drain Ohmic Contact on GaAs

Chapter 4

Electrical characteristics of GaAs MESFET&MOSFET with atomic-layer-deposited Al_2O_3 dielectric

Chapter 5

Conclusions and Suggestions

Table Captions

Chapter 2

Chapter 4

Chapter 5

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 1

Introduction

1-1 General Background

Today, the electronic products pursue not only the higher speed, better performance, and huger packing density, but also less power consumption and lower cost. For market requirements, the scale of Si device's dimension was the major issue in the past. Until now, the feature sizes of conventional Si MOSFET's have approximated to its physical limits. Shrinking the channel length and/or the dielectric thickness can't perform the excellent switching ratio, high driving capability, low leakage current, and acceptable reliability. For the excellent performances, novel device structures and materials must be investigated. The GaAs device applications have become very critical due to the requirement for global communication industrial growth.

GaAs metal-oxide-semiconductor field transistors (MOSFET) with high electron mobility in the semiconductor have application in high-speed electronic devices. Furthermore, semi-insulating substrates not available in silicon, is necessary to reduce the RC time delay between high-speed signal line in dense GaAs circuit. For both microwave and digital applications, GaAs MOSFET technology promises the advantages of low-power consumption

and circuit simplicity. Realization of the above devices depends on achievement of a low interfacial state density (D_{it}) existed between the gate dielectric and GaAs.

Si technology with its devices of 90nm gate length in production and 50 nm or smaller in research and development, and with SiO_2 gate oxide thickness close to quantum tunneling limit of 1.0 nm, has called for alternative high-*k* gate dielectrics. However, Coulomb scattering from charge trapping and the phonon issue related to high-*k* gate dielectric have resulted the degradation in channel mobility. In general, choices of suitable gate dielectric in MOSFETs will require (a) that the oxide does not react with the semiconductor, and (b) that the band offset of the oxide on the semiconductor is required to have over 1eV [1] to inhibit leakage. The band offset of various gate dielectrics, including HfO_2, Al_2O_3, Gd_2O_3, Si_3N_4 and SiO_2 [2~15] on III-V semiconductors such as GaAs, InAs, GaSb and GaN have been calculated using the method of charge neutrality levels. Here, we showed the band offset of GaAs in Fig 1-1.

1-2 Motivation

III-V compound semiconductors offer the advantages of high electron mobility rich band gap engineering, low power consumption [16-19] and high breakdown fields and thus are expected to outperform Si in certain metal-oxide-semiconductor (MOS) applications such as high-speed and high power devices. In contrast to the present commercially available III-V

metal-semiconductor field transistors (MESFETs) and high electron mobility transistors (HEMTs), which exhibit small forward gate voltages limited by the Schottky barrier heights, the III-V MOSFETs feature a much larger logic swing which gives a greater flexibility for digital integrated circuit (IC) designs and higher current gain cutoff frequency.

One key challenge in the III-V technology is to identify thermodynamically stable insulators on the III-V's that give a low D_{it} and low gate leakage (J_g). The intensive efforts in questing for such competitive insulator/III-V systems have finally yielded fruitful results with the discovery of high-k dielectric Ga_2O_3-Gd_2O_3 [20, 21] mixture or Gd_2O_3 [22, 23] on gallium arsenic (GaAs) and atomic layer deposition (ALD) Al_2O_3 [24-32] on GaAs, in which the reduced values in D_{it} and J_g have been demonstrated. The employment of ALD-Al_2O_3 as a gate dielectric layer, along with an implantation, followed by rapid thermal annealing (RTA) for activation process, have led to the demonstration of the first inversion-channel n-GaAs MOSFETs. On the other hand, we also displayed the advantages and disadvantages by using ALD and compared it with other PVD & CVD in Fig. 1-2. As can be seen, it indeed played an important role in fabricating the novel structure in the future. In Chapter 2 we further showed ALD growth principle in details.

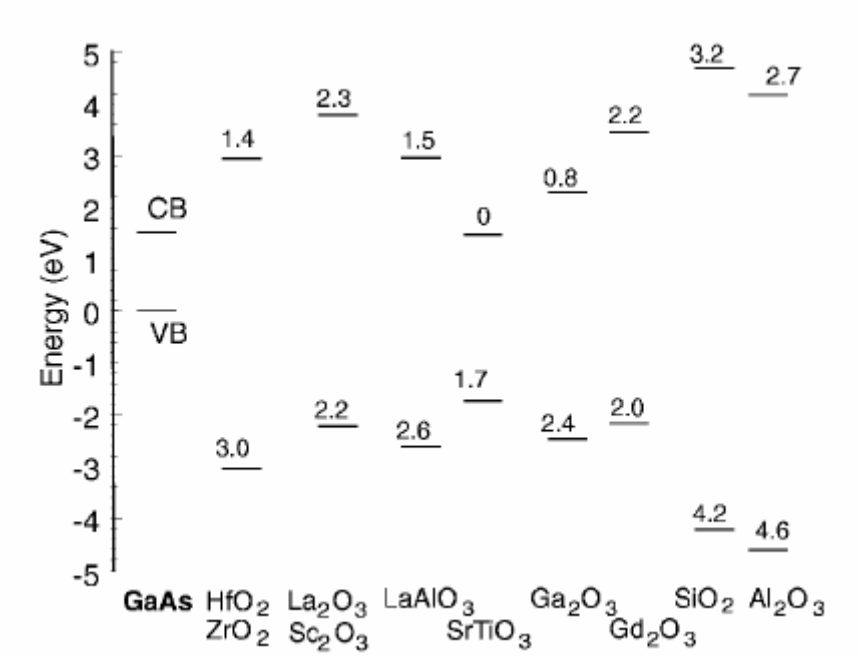


Fig 1-1 Predicted band offsets on GaAs with different high-k materials

Method	ALD	MBE	CVD	Sputter	Evapor	PLD
Thickness Uniformity	good	fair	good	good	fair	fair
Film Density	good	good	good	good	poor	good
Step Coverage	good	poor	varies	poor	poor	poor
Interface Quality	good	good	varies	poor	good	varies
Number of Materials	fair	good	poor	good	fair	poor
Low Temp. Deposition	good	good	varies	good	good	good
Deposition Rate	fair	poor	good	good	good	good
Industrial Applicability	good	fair	good	good	good	poor

ALD = atomic layer deposition, MBE = molecular beam epitaxy.
CVD = chemical vapor deposition, PLD = pulsed laser deposition.

Fig 1-2. All of the novel deposit thin film technique comparison

1-3 Organization of the Thesis

In Chapter 2, we developed the cleaning processes of GaAs substrates at first; different surface treatments were tested. During cleaning, it is important to suppress GaAs native oxides and As layer. Accordingly, we examined the chemical ratio after different cleaning processes by performing ex-situ XPS measurements. Subsequently, we deposited ALD-Al_2O_3 as dielectric film to fabricate MOS capacitors and examine the impact of interface quality on the electrical characteristics; the capacitance-voltage *(C−V)* and gate leakage current (*I−V*) characteristics were studied. In addition, InAs and InSb MOS capacitors were also discussed. In Chapter 3, we optimized the alloy condition for ohmic contact formed on GaAs. Three different materials, AuGeNi, PdGe, and PtIn, were tested and we extracted the respective specific contact resistance. We also undertook the physical analyses, including Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM) and Auger Depth Profiling, respectively. In Chapter 4, we fabricated the GaAs MESFET and MOSFET structures on semi-insulating GaAs and discussed their I_d-V_g and I_d–V_d electric characteristics. We also determined the electronic mobility with different surface treatments.

In the end of this thesis, chapter 5, we deposited GaAs thin film on Si substrate with Ge/SiGe buffer layer. The *C-V* and *I-V* curves were analyzed and surface performance was improved by sulfur chemical treatment. Finally, we gave the conclusions and suggestions for future work.

References

[1] J. Robertsona_ , B. Falabretti "Band offsets of high K gate oxides on III-V semiconductors." J. Appl. Phys. 100, (2006) 014111.

[2] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "High-quality ultrathin CVD HfO_2 gate stack with poly-Si gate electrode," in IEDM Tech. Dig., 2000, pp. 31-34.

[3] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS characteristics of ultra thin rapid thermal CVD ZrO_2 and Zr silicate gate dielectrics," in IEDM Tech. Dig., 2000, pp. 27-30.

[4] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A sub-400°C germanium MOSFET technology with high-k dielectric and metal gate," in IEDM Tech. Dig., 2002, pp. 437-440.

[5] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS characteristics with CVD HfO_2 gate dielectrics and TaN gate electrode," in VLSI Symp. Tech. Dig., 2003, pp. 121-122.

[6] A. Ritenour, S. Yu, M. L. Lee, N. Lu,W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, "Epitaxial strained germanium p-MOSFETs with HfO_2 gate dielectric and TaN gate electrode," in IEDM Tech. Dig., 2003, pp. 433-436.

[7] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, "A germanium NMOSFET process integrating metal gate and improved high-k dielectrics," in IEDM Tech. Dig., 2003, pp. 437-440.

[8] K. Kita, M. Sasagawa, K. Tomida, K. Kyuno, and A. Toriumi, "Oxidation-induced damages on germanium MIS capacitors with HfO_2 gate dielectrics," in Proc. SSDM, 2003, pp. 292-293.

[9] J. J. Chen, N. A. Bojarczuk, H. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge," in IEEE Trans. Electron Devices, vol. **51**, no. 11, Nov. 2004, pp. 1441-1447.

[10] D. S. Yu, C. H. Huang, A. Chin, C. Zhu, M. F. Li, B. J. Cho, and D. L. Kwong, "Al_2O_3-Ge-on-insulator n- and p-MOSFETs with fully NiSi and NiGe dual gates," in IEEE Electron Device Lett., vol. **25**, 2004, pp. 138-140.

[11] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High quality La_2O_3 and Al_2O_3 gate dielectrics with equivalent oxide thickness 5-10 Å," in VLSI Symposium Technical Digest, 2000, pp. 16.

[12] C. H. Lee et al., "MOS devices with high quality ultra thin CVD ZrO_2 gate dielectrics and self-aligned TaN and TaN/Poly-Si gate electrodes," in VLSI Tech. Dig., 2001, pp. 137-138.

[13] B. H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W-J. Qi, C. Kang, and J. C. Lee, "Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8–12Å)," in IEDM Tech. Dig., 2000, pp. 39-42.

[14] S. J. Lee et al., "Performance and reliability of ultra thin CVD HfO_2 gate dielectrics with dual poly-Si gate electrodes," in VLSI Tech. Dig., 2001, pp. 133-134.

[15] G D. Wilk, and R. M. Wallace, "Hafnium and zirconium silicates for advanced gate dielectrics," in J. Appl. Phys., vol. **87**, 2000, pp. 484-492.

[16] M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science 283, 1897 (1999)

[17] K. Iiyama, Y. Kita, Y. Ohta, M. Nasuno, S. Takamiya, K. Higashimine, and N. Ohtsuka, IEEE Trans. Electron Devices 49, 1856 (2002)

[18] J. K. Yang, M. G. Kang, and H. H. Park, J. Appl. Phys. 96, 4811 (2004)

[19] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H. J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. K. Ng, and J. Bude, IEEE Electron Device Lett. 24, 209 (2003)

[20] M. Hong, M. Passlackm, J. P. Mannaerts, J. Kwo, S. N. G. Chu, N. Moriya, S. Y. Hou, and V. J. Fratello, J. Vac. Sci. Technol. B 14, 2297 (1996)

[21] J. Kwo, D. W. Murphy, M. Hong, R. L. Opila, J. P. Mannaerts, A. M. Sergent, and R. L. Masaitis, Appl. Phys. Lett. 75, 1116 (1999)

[22] M. Passlack, M. Hong, and J. P. Mannaerts, Appl. Phys. Lett. 68, 1099 (1996)

[23] B. Yang, P. D. Ye, J. Kwo, M. R. Frei, H. J. L. Gossnann, J. P. Mannaerts, M. Sergent , M. Hong, K. Ng, and J. Bude, J. Cryst. Growth 251, 837 (2003)

[24] Yang WS, Kim YK, Yang SY, Choi JH, Park HS, Lee SI, et al. Surf. Coat. Tech. 2000; 131:79

[25] Higashi GS, Fleming CG. Appl. Phys. Lett. 1989; 55:1963-5.

[26] Fan J, SugiokaK, Toyoda K. Jpn J. Appl. Phys. 1991; 30:L1139-41

[27] Kattelus H, Ylilammi M, Saarilahti J, Antson J, Lindfors S. Thin Solid Films 1993; 225:296

[28] Lin HC, Ye PD, Wilk GD. Appl. Phys. Lett. 2005; 87:182904

Chapter 2

Improved electrical characteristics of ALD-Al_2O_3/III-V MOS capacitors with sulfide treatment

2-1 Introduction

Recently, GaAs materials are used widely in such applications as optoelectronic devices, photodiodes, high electron-mobility transistors (HEMT), and other high-frequency devices. In attempts to obtain superior performance rivaling or exceeding that of transistors on traditional Si-based substrates, various high-*k* gate dielectrics have been examined on high-mobility III-V substrates, especially GaAs- and InSb-based compound materials. Studies into competitive insulators on compound semiconductors and efficient passivation methods have been performed for more than four decades; the poor quality of the insulator-substrate interface has been the foremost obstacle hindering the realization of III-V metal oxide semiconductor MOS devices. In addition to SiO_2 and Si_3N_4, atomic-layer-deposited ALD Al_2O_3, $Gd(Ga)O_3$, and HfO_2 high-*k* dielectrics are also potential candidates for use on GaAs substrates. Surface sulfide treatment and the use of ultrathin Si or Ge interfacial passivation layers are both practical techniques for improving electrical characteristics. The passivation of

GaAs surfaces with Na_2S [1] or ammonium sulfide $(NH_4)_2S$ [2] prior to deposition of the gate dielectric has been reviewed comprehensively; the improvement in the device performance depends strongly on the sulfide treatment procedure. The *in-situ* deposition of several Si or Ge monolayers [3.4] on GaAs can reduce the D_{it} to approximately 10^{10}–10^{11} cm^{-2} eV^{-1}; this passivation technique has received renewed interest in recent years., Subsequent thermal annealing can further improve the quality of insulator films deposited on GaAs. Meanwhile, during high temperature processing it is important to inhibit the loss of As within the GaAs substrate and also suppress the formation and subsequent incorporation of native oxides; these processes lead directly to electrical deterioration in GaAs MOS capacitors. The impact of rapid thermal annealing on the properties of various high-*k*/GaAs structures has been studied previously; the gas used in the annealing process influences the thermochemical mechanism as well as the interfacial quality. Nevertheless, correlations between these thermal reactions and the MOS performance have not been established in detail. In this study, we examined the material and electrical characteristics of ALD-Al_2O_3 thin films deposited on an $(NH_4)_2S$-treated GaAs surface and then monitored the impact of thermal annealing processing.

As mentioned in chapter 1, there are more defects on the interface between high-*k* materials and GaAs substrate. Thus, we should find a suitable deposition system to decrease these defects on the dielectric interface, achieving to obtain the high-quality dielectric film on

GaAs; ALD-Al_2O_3 is just what we want. As it is well known, Al_2O_3 is a widely used insulating material for gate dielectrics, tunneling barriers and protection coatings due to its excellent dielectric properties, strong adhesion to dissimilar materials, and its exceptional thermal and chemical stabilities. Besides, Al_2O_3 has a high band gap (~ 9 eV), a high breakdown electric field (5-30 MV/cm), high permittivity (8.6-10), high thermal stability (up to at least 1000^oC), and remains amorphous under typical processing conditions. The leakage current observed in ultrathin Al_2O_3 on GaAs is equivalent to or lower than that of the state-of-the-art SiO_2 on Si. The breakdown electric field of Al_2O_3 film thicker than 50 Å can be up to ~ 10 MV/cm; this value is near the bulk breakdown electric field for SiO_2.

ALD is an ultrathin film deposition technique based on sequences of self-limiting surface reactions, which enables thickness control on the atomic scale. ALD deposition mechanism is like chemical vapor deposition (CVD). We introduce the unique feature of the step-by-step deposition in ALD by using a general example of Al_2O_3 film deposition. It is well known that Al_2O_3 films can be grown by using alternating pulses of $Al(CH_3)_3$ (TMA, the aluminum precursor) and H_2O (the oxygen precursor) in the presence of N_2 carrier gas flow. Its mechanism procedures for one deposition cycle are illustrated in Fig. 2-1. At first, TMA is fed into the reactor and react with the OH bond on the GaAs substrate. Second, the reactor is purged with pure N_2 gas to clean out residual TMA. Third, H_2O is purged into the reactor and forms Al_2O_3 on surface. Finally, the reactor is purged with pure N_2 gas again to clean out

residual H_2O.

2-2 Experimental Procedures

MOSCAP structures were fabricated on high Si-doped (n-type, ~ 1x 10^{18} cm^{-3}) GaAs (100) substrates. At first, the GaAs was rinsed in the diluted NH_4OH (1%) solution for 1min. And then, we performed $(NH_4)_2S$ chemical treatment in combination with either H_2O or C_4H_9OH solution on GaAs surface prior to high-*k* deposition. Surface chemistry was analyzed by employing x-ray photoelectron spectroscopy (XPS) that Al *K*α is used as an excitation source. The Al_2O_3 gate dielectric was then deposited by ALD at 300 °C, followed by post deposition annealing (PDA) at 600 °C for 30 s in an O_2 ambient. Sputtered Pt dots about 700 Å were patterned as circular gate electrodes through the specific shadow mask with the Al for backside contact. The complete process flow was shown in Fig. 2-2. The *C*−*V* and *I*−*V* curves on Pt/Al_2O_3/GaAs MOS capacitors were measured using an HP4284 and Keithley 4200, respectively.

2-3 Results and Discussions

2-3-1 Wet cleaning on GaAs

In the beginning, we chose different wet cleaning processes (WCPs) to eliminate native oxide such as Ga_2O_x and As_2O_3. Table.1 shows these WCPs used in the study.

clean	*ACE*	*NH_4OH*
WCP1	*1min*	*1%-1min*
WCP2	*1min*	*10%-1min*

Table .1 Wet cleaning process of GaAs in this study

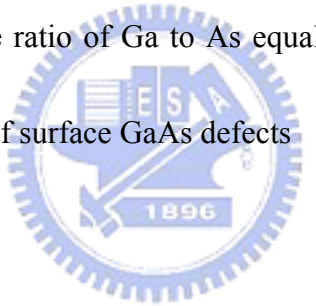
Here, NH_4OH with different concentrations were explored. Fig. 2-3 displays the core-level spectra of As *2p3*, As *3d*, Ga *2p3*, and Ga *3d* for GaAs substrates after WCPs, respectively. The binding energies of As_2O_3, As-As (called As layer), and GaAs substrate are 1326 eV, 1324.6 eV, and 1322.9 eV in As *2p3* spectrum, respectively. As seen, GaAs after WCP1 displays less As_2O_3 and As_2O_5 components than that after WCP2. Besides, the more the NH_4OH concentration used in GaAs clean, the more the As-rich surface was. Subsequently, an ALD-Al_2O_3 gate dielectric was deposited at 300 °C to decompose surface As-oxides because of the breaking of As-O bonding at 150~250 °C. Characteristics of Pt/Al_2O_3/GaAs MOS capacitors after different NH_4OH WCPs with and without PDA at 600 °C for 30 sec in O_2 ambient are plotted in Figs. 2-4 (a) and (b). We found that the annealed Al_2O_3/GaAs MOS capacitors with 1%-NH_4OH showed higher accumulation capacitance than that with 10%-NH_4OH. Fig. 2-5 displays the gate leakage current without (control) and with PDA (both of WCP1 and WCP2). It was found that the 10%-NH_4OH WCP, relative to the 1% case, caused the higher gate leakage current in GaAs MOS capacitor. Fig. 2-6 displays the

corresponding *G-V* characteristic with and without PDA. As we mentioned earlier, WCP with higher NH_4OH concentration caused the onset of more As_2O_X, which is the origin of higher gate leakage current. According to the chemical reaction: $As_2O_3 + GaAs \rightarrow Ga_2O_3 + 4As$ ($\triangle G$=-270 $KJmol^{-1}$ at 300^oC), we suggested that the lower As oxides existed close to the dielectric interface should accompany with the reduced formation of the metallic As by-product after thermal processing, thus, a lower leakage current was characterized. We also found that gate leakage increased after 600 °C PDA for 30 s in O_2 ambient. The result can be attributed to the thermal process providing more driving energy to accelerate the chemical reaction.

2-3-2 Surface treatment on GaAs

Figures 2-7 (a) and (b) display As*2p3* and Ga*2p3* photoemission spectra with different surface sulfur treatments; the composition ratios were summarized in Table II and Table III. It was observed that both kinds of native oxides, especially for As_2O_x (x=3, 5), were obviously reduced with using $(NH_4)_2S$ solutions; moreover, the sulfide solution dissolved in C_4H_9OH is more effective as compared to that dissolved in H_2O. The values of As_2O_x/As_{tot}(As-As/As_{tot}) were 97.8%(30.1%) for GaAs surface with deionized water (DIW) rinse only; its value can be reduced to 52.6%(22.6%) and 38.8%(20.1%) for the sulfide solution (H_2O) [5-9]and the sulfide solution (C_4H_9OH) treatments, respectively. Increasing

the concentration of the sulfide solution (C_4H_9OH) can further eliminate the formation of As oxides. Furthermore, we found that an increase in sulfide treatment temperature could reduce more As oxides on the surface. On the other hand, raising the sulfide concentration caused the formation of more Ga-S bonding with a decrease in As-S bonding; this can be attributed to the fact that the As-S bond was decomposed around 300 °C, and it might transform to stable Ga-S and metallic (The Gibber free energy was (-166 $kJmol^{-1}$) at room temperature). Figs. 2-8(a) and (b) display the core-level spectra of Ga *3d* and As *3d* for GaAs substrate after ALD process, respectively. We found that the GaAs surface through sulfur treatment can return the ratio of Ga to As equal to 1, i.e., the stoichiometric GaAs, due to the effective reduction of surface GaAs defects



2-3-3 Surface roughness of sulfide GaAs

Figure 2-9 (a) shows the variation of GaAs surface roughness after the diluted NH_4OH/D.I.W.(1%) cleaning with four sulfide conditions of (a) without (b) 1% C_4H_9OH RT (c) 10% C_4H_9OH (d) 10% C_4H_9OH, 60°C. The surface roughness decreased from 0.284 to 0.232 nm as sulfide concentration and temperature increased. All the variations of surface roughness after different treatment were summarized in Fig. 2-8 (b), and the GaAs surface roughness indeed became smooth with $(NH_4)_2S$-C_4H_9OH treatment.

2-3-4 Electrical and material characteristics of MOSCAP

Fig. 2-10 shows 10 kHz *C-V* characteristics of $Pt/Al_2O_3/GaAs$ MOS capacitor different surface treatments. If the sulfur concentration increased to 10%, the higher capacitance we obtained on both accumulation and depletion regions. After the sulfur temperature was increased to 60 ^oC, this property was obtained emphatically. The reason could be probably attributed to an increase in either the interface state or the bulk trap density. Fig. 2-11 shows a simple device circuit biased in different conditions. It according to the following equation,

$$C_{it} = q\, D_{it} A \tag{2.1}$$

We thus calculated the value of C_{it} approximately close to 100 pF. The value is closed to C_d . In other words, the more the D_{it} is, the various the capacitance is. From the J_g characteristics shown in Fig. 2-12, we observed that GaAs capacitors through 10% sulfide-C_4H_9OH treatment actually possessed the higher thermal stability due to the smaller amounts of the As-As species and As oxides. According to two chemical reaction: One was $As_2O_3 + GaAs \rightarrow Ga_2O_3 + 4As$, The other was $As_2S_3 + 3GaAs \rightarrow 3GaS + 5As$, we suggested that the lower As oxides and As-S components existed close to the dielectric interface should accompany with the reduced formation of the metallic As by-product after thermal processing; therefore, a lower leakage current was characterized as well. As-S chemical bonds were broken at a relatively low temperature, approximately 150-250 ^oC, whereas adsorption of sulfur from the surface, through breaking Ga-S bonds occurs above 500 ^oC. At 300 ^oC ALD process, only

Ga-S bonds remained stable, whereas As-S bonds were possibly reduced into the metallic As. The Al_2O_3/GaAs after sulfur+H_2O pretreatment showed the similar electrical characteristic as sulfur+C_4H_9OH we mentioned earlier. *C-V* and *J-V* characteristics were shown in Fig.2-13 (a) and (b), respectively. Figs. 2-14 (a) and (b) displayed the multi-frequency *C-V* curves after different sulfide treatments before and after PDA. Figs. 2-15 (a) and (b) displayed the calculated results of the frequency dispersion in these GaAs capacitors. We employed the variation of ΔC and ΔV values to examine the interface quality [10]. Here, the equations of ΔC and ΔV are reproduced as below

$$\Delta C = \frac{C(@1\text{ kHz}) - C(@100\text{ kHz})}{C(@1\text{ kHz})} \tag{2.2}$$

$$\Delta V = V(@\ 100\text{ kHz } C_{FB}) - V(@\ 1\text{ kHz } C_{FB}) \tag{2.3}$$

where

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_{DL}}, \tag{2.4}$$

C_{DL}=1066 pF for GaAs, and C_{ox}=1 kHz C_{max}. From Fig. 2-15, we would find thatΔC andΔV were lowed after passivation, especially with thermal sulfur treatment .In other words, D_{it} was improved by passivation. It was observed that the sample subject to sulfide solution (C_4H_9OH) revealed the smaller △C/△V than that with sulfide solution (H_2O). The values of the △C and △V were 17-20% and 0.9-1.4 V for the as-deposited sample and we can improve these two values to 17-14% and 0.6-0.7 V by using 10% sulfide solution (C_4H_9OH) . In Fig 2-15., we studied the variation of density of state (D_{it}) using single-frequency method [11], and equation was shown below.

$$D_{it} \approx \frac{(2/qA)(G_{\max}/\omega)}{[(G_{\max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2]} \quad (2.5)$$

where G_{max} was the maximum conductance in the G-V plot with it's corresponding capacitance (Cm) . The D_{it} showed the decreasing with sulfide temperature and the input of NH_4OH solution. The lowest density state by wet chemical and sulfur passivation GaAs in this work had reduced to 8.5×10^{12} cm^{-2} eV^{-1}.

The corresponding ALD-Al_2O_3/GaAs MOS capacitors after optimizing surface treatment showed the comparable insulating properties with respect to $HfSiO_x$ dielectrics reported on n-GaAs in Fig. 2-16(a). The value of leakage current was about 10^{-7} A/cm^2 at CET=3.8 nm in our study. From the TEM image in Fig. 2-16(b), the physical thickness was 62 A, corresponding to the dielectric constant of ca. 6.9 for the deposited Al_2O_3 film by using Eq. (2.6).

$$\varepsilon_r = \frac{t_{phy}}{CET}\varepsilon_{sio_2} \quad (2.6)$$

2-3-5 InAs and InSb MOSCAP characteristics

The material parameters of GaAs, InAs, and InSb are listed in Table III. Though simple equation calculations, we can determine the minority carrier response time (τ) and transition frequency (f_{tran}). Here, $\tau = C_d/G_{inv}$ is defined, where C_d is the depletion capacitance and G_{inv} is the conductance measured in inversion. Using the data of diffusion length L_{diff} = ~10 um, diffusion time τ_d~ 3 x 10^{-4} s, n_i = 1E15 cm^{-3}, and substrate doping

concentration N_d = 1E17 cm^{-3} for InAs, while the L_{diff} = ~10 um, τ_d ~ 5x 10^{-4} s, n_i = 2E16 cm^{-3}, N_d = 1E17 cm^{-3} for InSb. The values of G_{inv} were about 3 x 10^{-2} and 4 x 10^{-3} S/cm^2 at RT for InAs and InSb, respectively. Also, from the equation $C_d = \varepsilon_r/W_d$, where ε_r is material dielectric constant and W_d is the maximum depletion width in inversion. We can estimate that the values of C_d are ca. 33 and 62 nF/cm^2 for InAs and InSb, respectively. Accordingly, the values of τ are calculated to be ca. 5 and 7 μs for InAs and InSb, which were more than three orders of magnitude shorter than the value obtained in Si MIS capacitors. This large difference can be understood due to the result of $\tau \sim 1/G_{inv} \sim 1/n_i$ around RT as well as the lower energy gap, where n_i values in InAs and InSb materials are more than five orders of magnitude higher with respect to the conventional Si (1.5E10 cm^{-3}). Due to the short minority response time in InAs and InSb, an inversion layer is formed fast in response to an external *ac* signal at the gate, so that a high capacitance, equal to C_{ox} is formed even at high frequencies i.e., 1 kHz. This is clearly observed in Fig. 2-17 where room temperature *C-V* curves are recorded at several frequencies. The response time τ also determines the transition frequency $f_{tran.} \sim (2\pi\tau)^{-1}(C_d/C_{ox})$, at which the capacitance in inversion achieves the half of oxide capacitance C_{ox}, marking the transition from low frequency to high frequency behavior. We calculated the corresponding values of $f_{tran.}$ are 380 and 8500 kHz for InAs and InSb two materials, which is consistent with the experimental observations in *C-V* curves. Our calculation results indeed showed that the

high n_i value in InAs and InSb is a good source of minority carriers for building-up of the inversion layer fast. We also use different IPL such as sulfur treatment and Si passivation layer to eliminate native oxides in InAs and InSb. We found that the Si passivation was better than sulfur treatment in improving electrical characteristics. Figs. 2-18 (a)-(c) display the *C-V* and *I-V* characteristics, respectively, it was not efficient to reduce native oxides on both III-V materials, especially for InAs. In general, we assigned Fermi-level pinning and gate leakage to the resultant As-riched surface. However, we tried to deposit different Si passivation layer thickness to improve this phenomenon; unfortunately, the result was out of expectation. We summarize the leakage current characteristics versus the CET of these In-based MOS capacitors in Fig. 2-19. It was found that the higher the deposited temperature was employed, the severer degradation the surface occurred in both InAs and InSb. Finally, we still used the single frequency conductance method to calculate the D_{it} value as the results displayed in Fig. 2-20. Obviously, it showed that these passivation methods were only suitable in GaAs MOS capacitor rather than In-based ones, in other words, it is essential to explore other passivation solutions to reduce the order of D_{it} as well as the surface quality after dielectric deposition. In conclusions, it is believed that Fermi level pinning and gate leakage will be two main challenges in In-based substrates.

2-4 Summary

We systematically investigated the surface treatment effects on the electrical and material characteristics of GaAs MOS capacitors with ALD-Al_2O_3 gate dielectric. The sulfidization pretreatment diminished the formation of GaAs native oxides and elemental As coverage close to dielectric interface, thus improving the effect of Fermi level pinning on the Al_2O_3/GaAs capacitors. The sulfidized GaAs samples displayed not only smaller frequency dispersion with higher oxide capacitance but also decreased D_{it}, and J_g, respectively. Post thermal annealing of GaAs MOSCAP can alleviate the charge trapping behavior, and decrease the amount of metallic As and the value of D_{it}. it is believed that Fermi level pinning and gate leakage will be two main challenges in In-based substrates. On the other hand, we calculated t he corresponding values of $f_{tran.}$ are 380 and 8500 kHz for InAs and InSb MOSCAPs, consistent with the experimental observations in *C-V* curves. It also reflects that a high n_i value is a good source of minority carriers for building-up of the inversion layer fast in these two lower band-gap materials. We also found the passivation methods used in GaAs MOSCAP are not suitable in InAs and InSb MOSCAPs. So that, it is essential to explore other passivation solutions to improve the dielectric/InAs(Sb) interface quality. In conclusions, we believed that Fermi level pinning and gate leakage will be two main challenges in In-based substrate.

References

[1] V. N. Bessolov, E V. Konenkova, M V. Lebedeva) , J. Vac. Sci. Technol. B, 14(1996).

[2] V.N. Bessolovy, M.V. Lebedevy, N. M. Binhz, M. Friedrichz , D. T. Zahnz" *Sulphide passivation of GaAs: the role of the sulphur chemical activity.*" Semicond. Sci. Technol. **13** (1998) 611–614.

[3] Hyoung-Sub Kim, Injo Ok, Manhong Zhang, Tackhwi Lee, Feng Zhu, Lu Yu, and Jack C. Lee, Appl. Phys. Lett. 89, (2006) 222903

[4] Hyoung-Sub Kim, Injo Ok, Manhong Zhang, Changhwan Choi, Tackhwi Lee, Feng Zhu, Gaurav Thareja, Lu Yu, and Jack C. Lee, Appl. Phys. Lett. 88, (2006)252906

[5] J. F. Fan, H. Oigawa, and Y. Nannichi, Jpn. J. Appl. Phys., Part 1 27, L1331 (1998)

[6] H. Sugahara, M. Oshima, H. Oigawa, H. Shigekawa, and Y. Nannichi, J. Appl. Phys. 69, 4349 (1991)

[7] N. Yokoi, H. Andoh, and M. Takai, Appl. Phys. Lett. 64, 2578 (1994)

[8] X. Y. Hou, W. Z. Cai, Z. Q. He, P. H. Hao, Z. S. Li, X. M. Ding, and X. Wang, Appl. Phys. Lett. 60, 2252 (1992)

[9] A. Jaouad, V. Aimez, C. Aktik, K. Bellatreche, and A. Souifi, J. Vac. Sci. Technol. A 22, 1027 (2004)

[10] W. P. Li, X. W. Wang, Y. X. Liu, S. I. Shim, and T. P. Ma, Appl. Phys. Lett. 90, 193503 (2007)

[11] Hill.W.A, Coleman, C. C, *Solid-State Electronics*, v 23, n 9, Sep, 1980, p 987-993

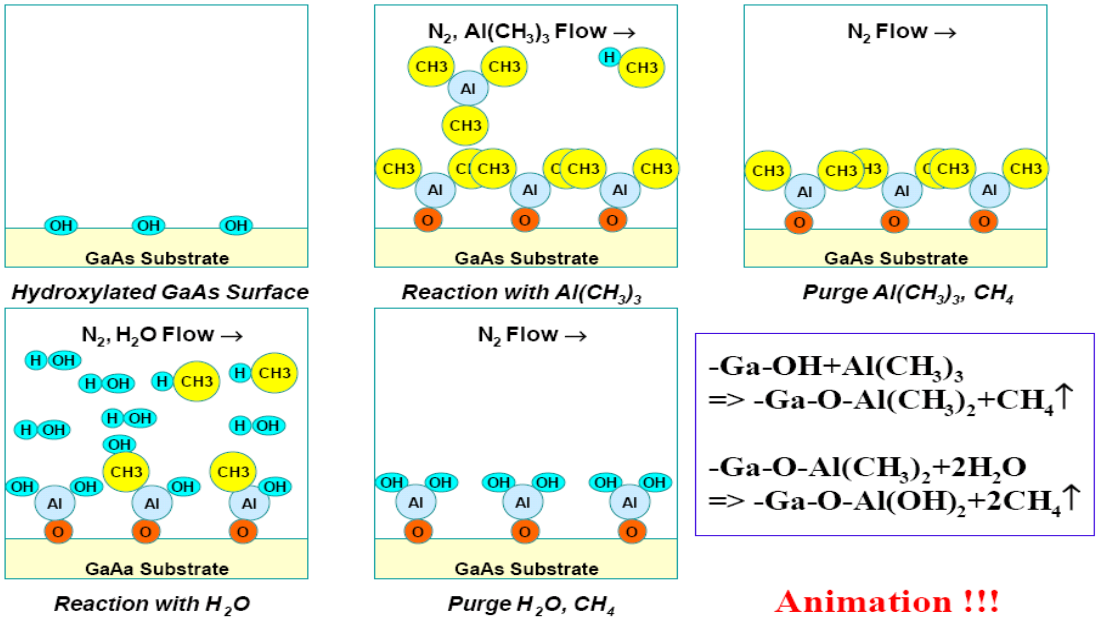


Fig. 2-1 Atomic layer deposition (ALD) mechanism and chemical reaction

~ *MOSCAP Process Flow* ~

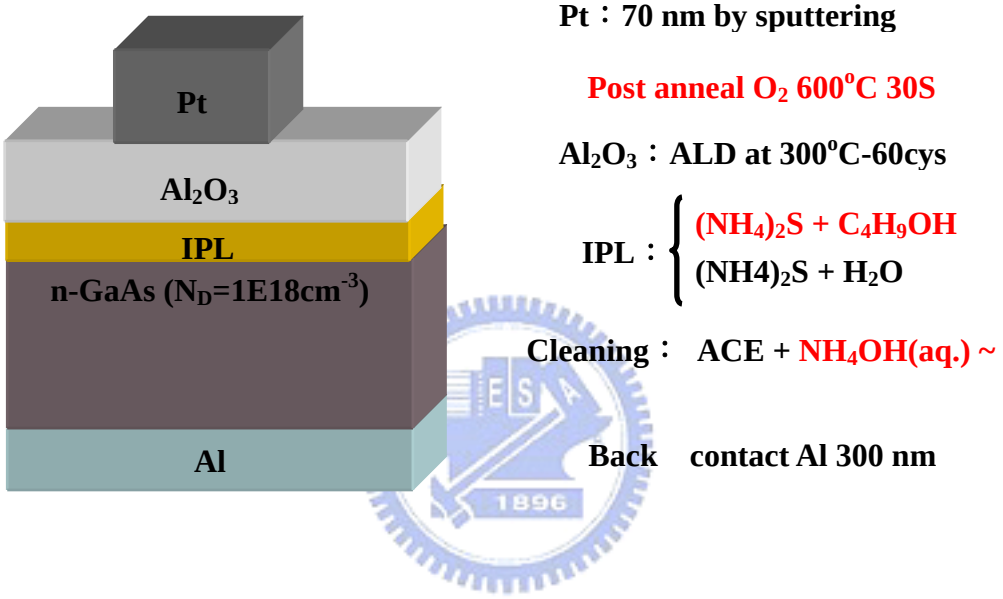


Fig. 2-2 $Pt/Al_2O_3/n$-GaAs MOS capacitors process flow

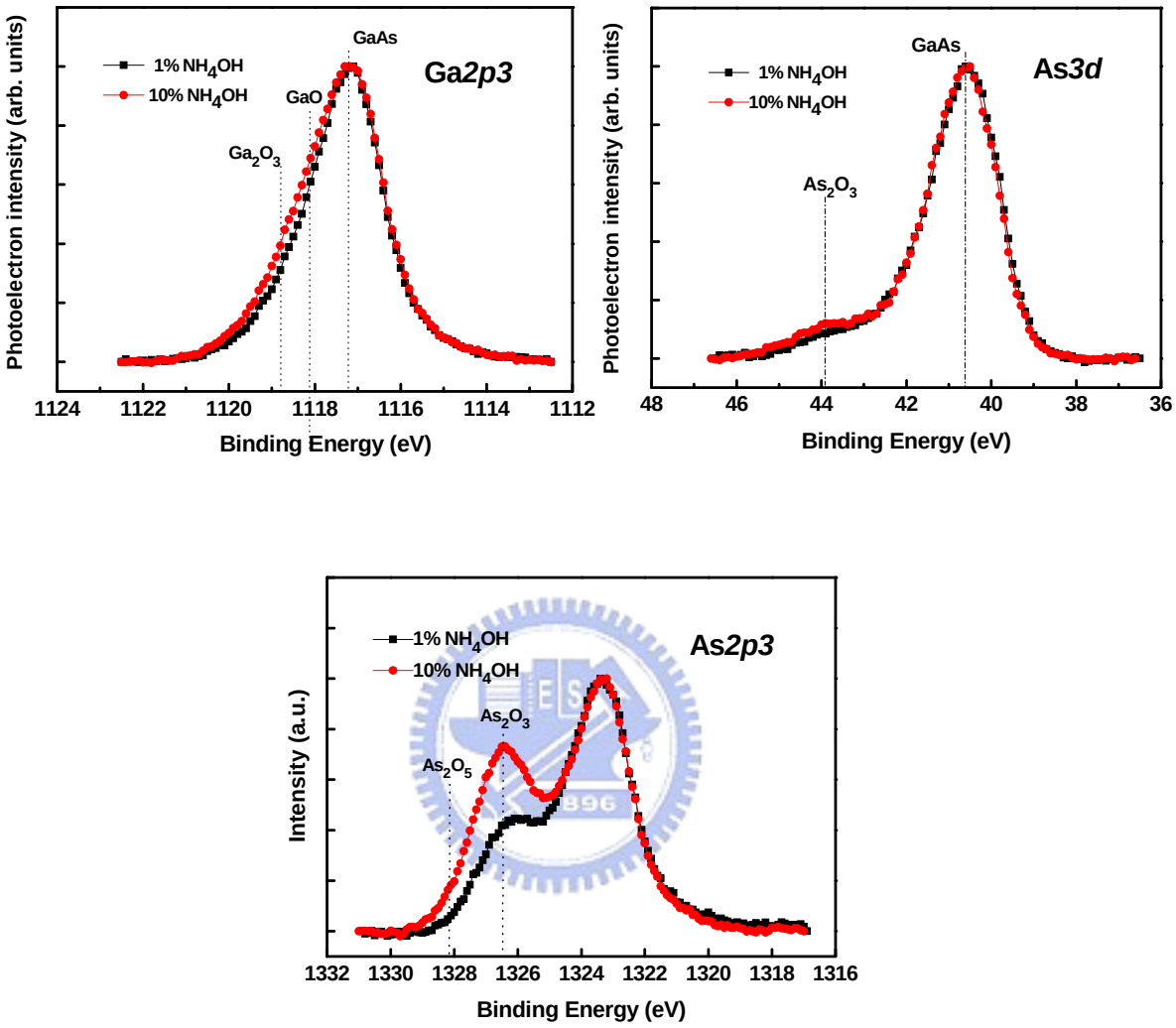


Fig. 2-3 *XPS* spectrum *Ga2p3 As2p3 As3d* after different concentration of dilute ammonia

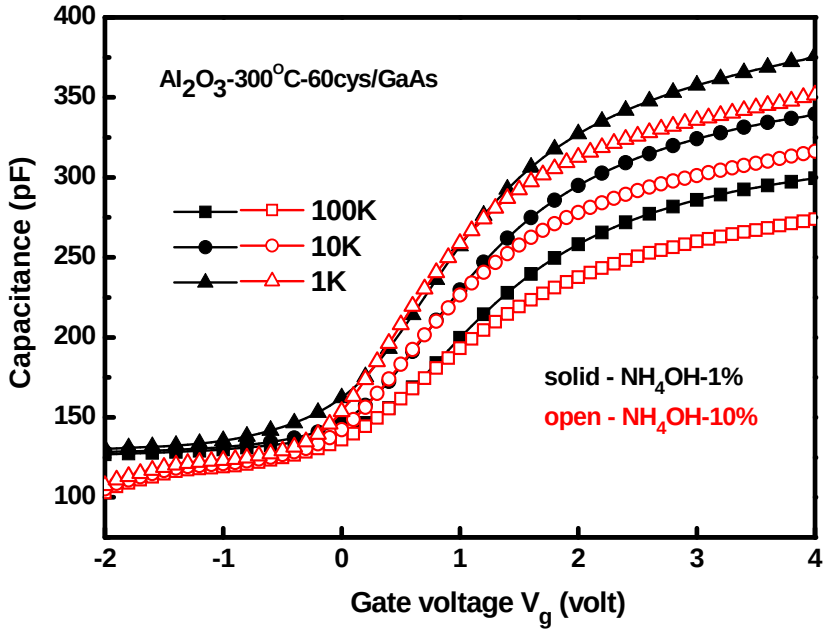


Fig. 2-4 (a) Multi-frequency C-V characteristics of MOS capacitors ($Pt/Al_2O_3/GaAs$) with 1% and 10% concentration of dilute ammonia. The Al_2O_3 was deposited by ALD (300 ^oC, 60 cycles)

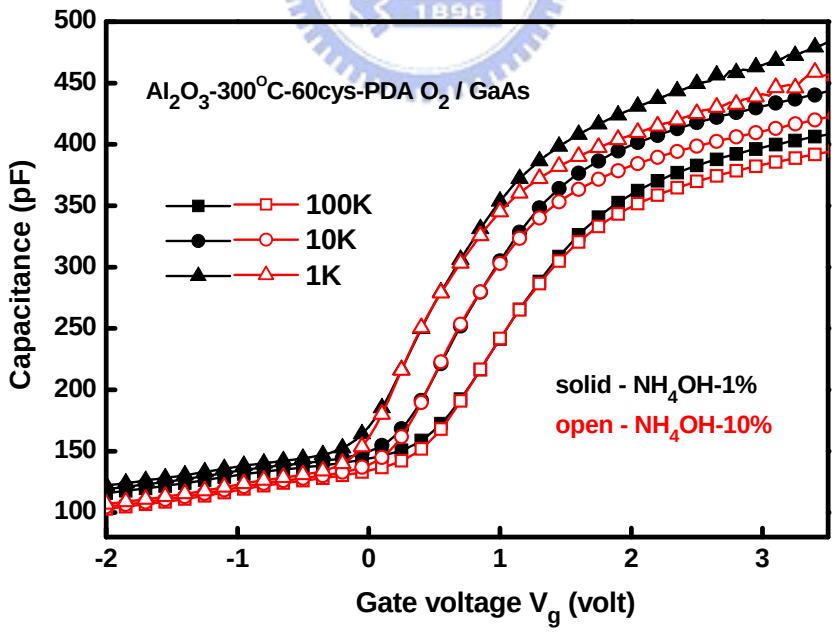


Fig. 2-4 (b) Multi-frequency C-V characteristics of MOS capacitors ($Pt/Al_2O_3/GaAs$) with post deposit annealing at 600 ^oC in the O_2 ambient. (ALD ,300 ^oC, 60 cycs).

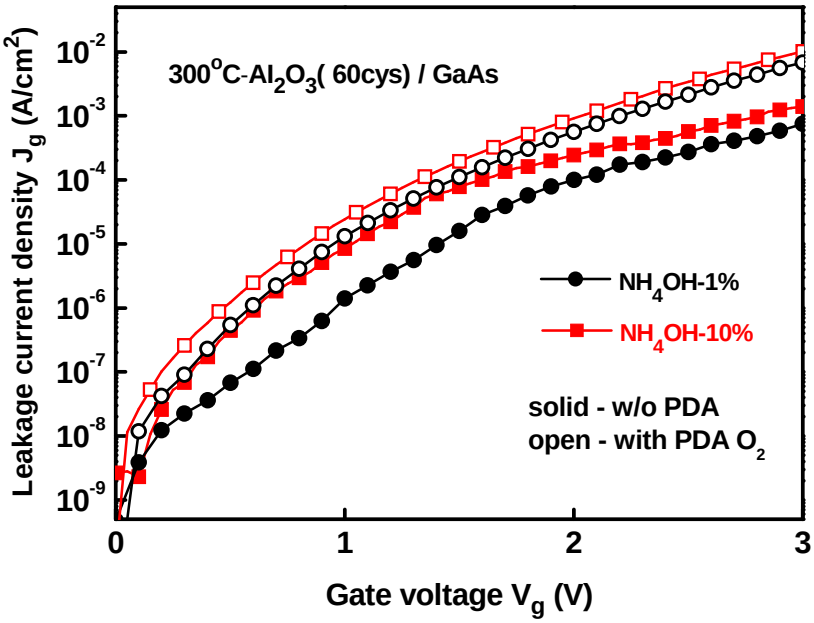


Fig 2-5 J-V characteristics of $Pt/Al_2O_3/GaAs$ MOS capacitor with 1% and 10% concentration of dilute ammonia. The Al_2O_3 was deposited by ALD (300 °C, 60 cycles).

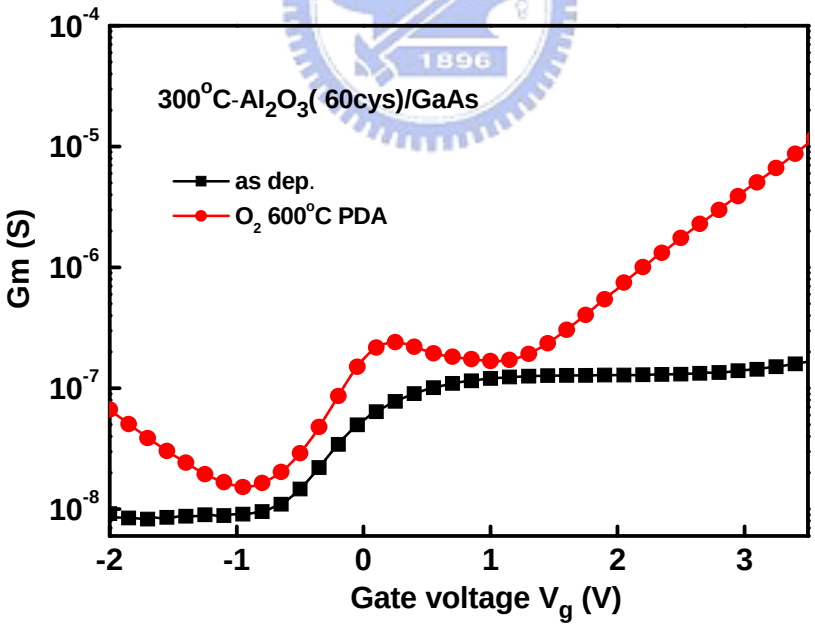


Fig. 2-6 G-V characteristics of $Pt/Al_2O_3/GaAs$ MOS capacitor with and without 600 °C O_2 annealing. The Al_2O_3 was deposited by ALD (300 °C, 60 cycles).

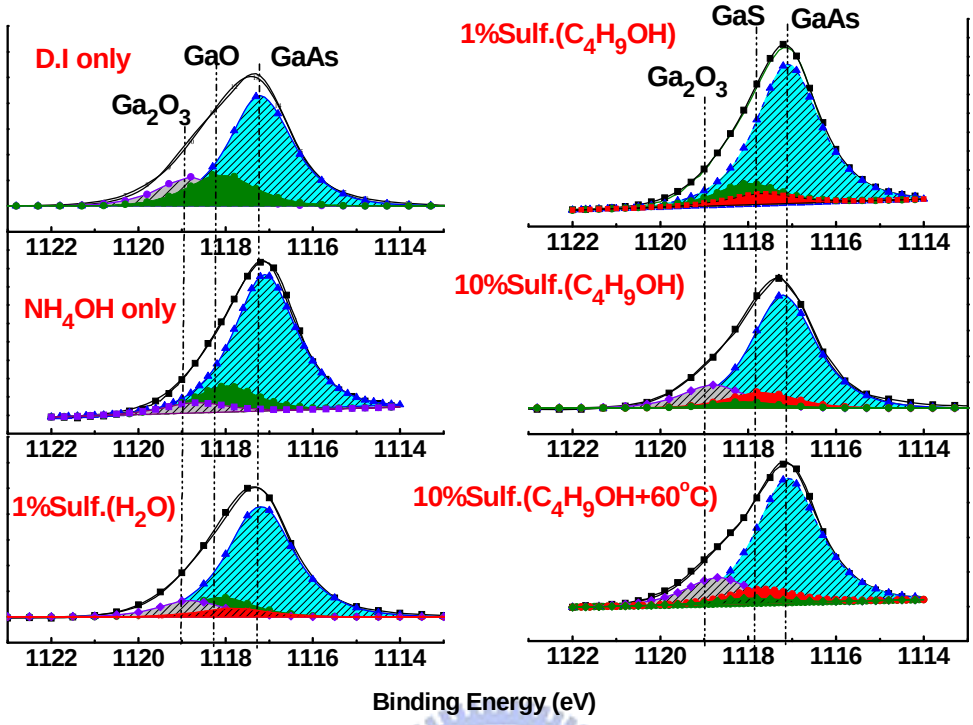


Fig. 2-7 (a) XPS spectrum Ga *2p3* after different cleaning processes of Table II.

condition	*Ga-S/Ga $_{total}$*	*Ga_2O_x/Ga $_{total}$*
D.I water only	***--***	***54.3%***
NH_4OH only	***--***	***25.8%***
1%Sulf.(H_2O)	***7.1%***	***26.4%***
1%Sulf.(C_4H_9OH)	***7.3%***	***22.7%***
10%-(C_4H_9OH)	***10.9%***	***24.6%***
10%(C_4H_9OH)- 60°C	***13.9%***	***25.1%***

Table II. Chemical ratio by XPS spectra of Ga *2p3* corresponding to different cleaning processes and sulfur treatment.

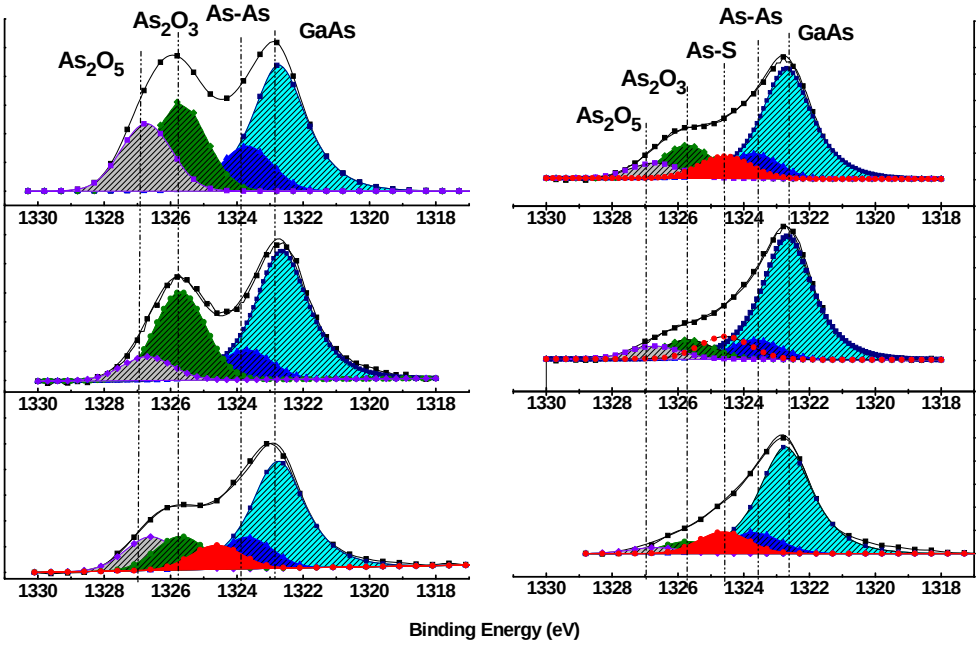


Fig. 2-7 (b) XPS spectrum As *2p3* after different cleaning processes of Table III.

condition	*As-As/As$_{total}$*	*As-S/As$_{total}$*	*As$_2$O$_3$/As$_{total}$*
D.I water only	***30.1%***	***--***	***97.8%***
NH$_4$OH only	***23.5%***	***--***	***73.4%***
1%Sulf.(H$_2$O)	***22.6%***	***18.9%***	***52.6%***
1%Sulf.(C$_4$H$_9$OH)	***20.1%***	***17.8%***	***38.8%***
10%Sulf.(C$_4$H$_9$OH)	***13.9%***	***16.3%***	***23.2 %***
10%Sulf.(C$_4$H$_9$OH - 60^{o}C	***17.1%***	***15.7%***	***14.2 %***

Table III. Chemical ratio by XPS spectra of As *2p3* corresponding to different cleaning processes and sulfur treatment.

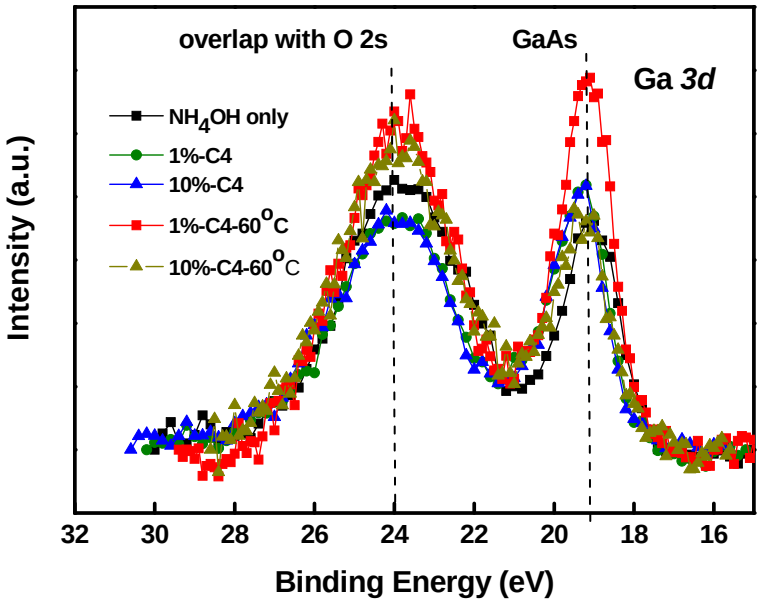


Fig. 2-8 (a) XPS spectrum Ga *3d* with different surface treatment after ALD process

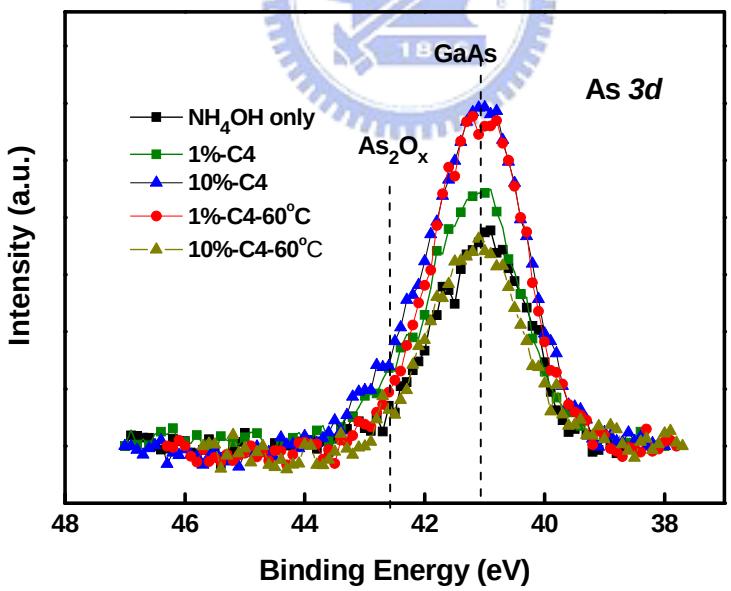


Fig. 2-8 (b) XPS spectrum As *3d* with different surface treatment after ALD process

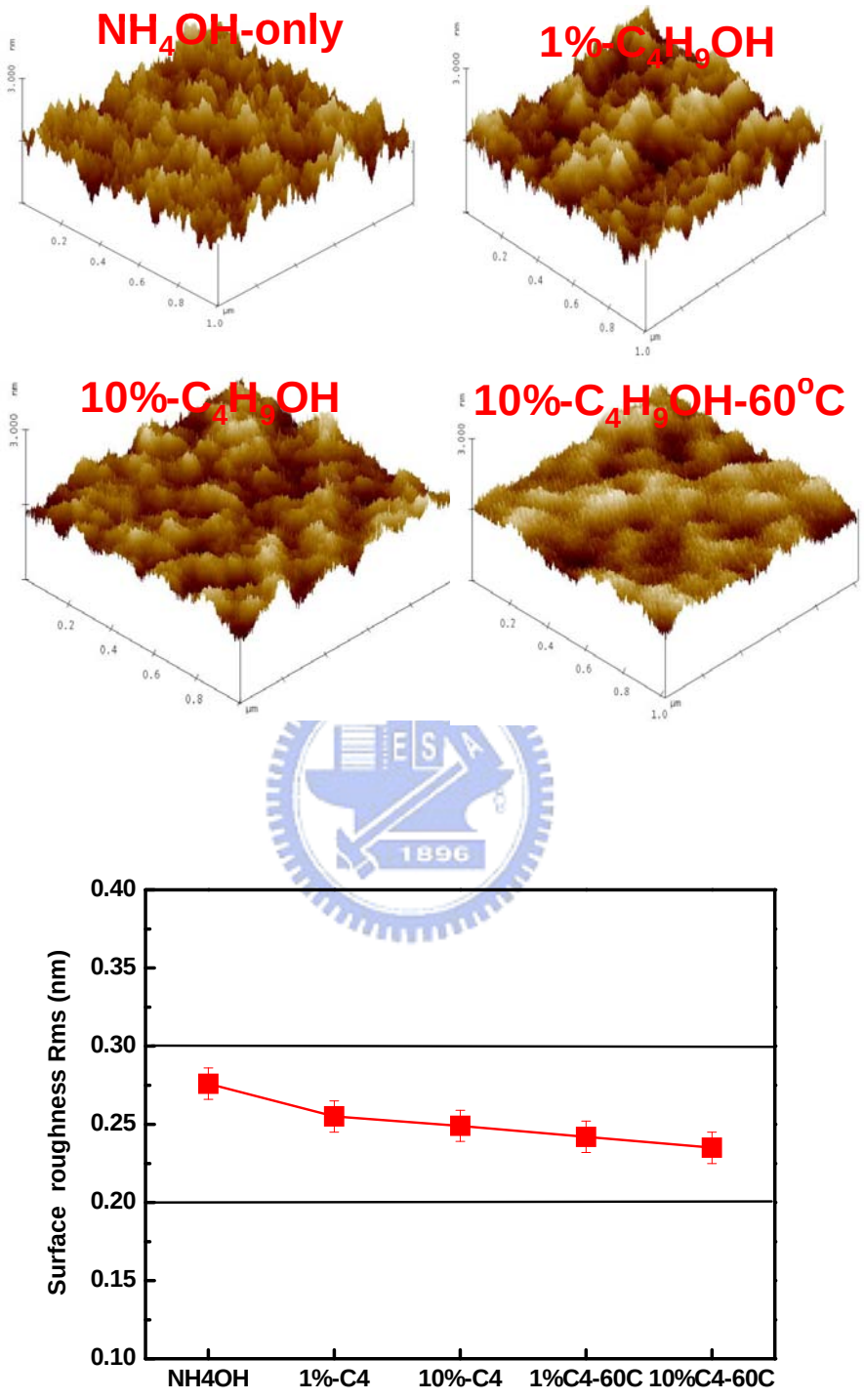


Fig 2-9 (a) surface morphology (b) surface roughness after sulfide treatment

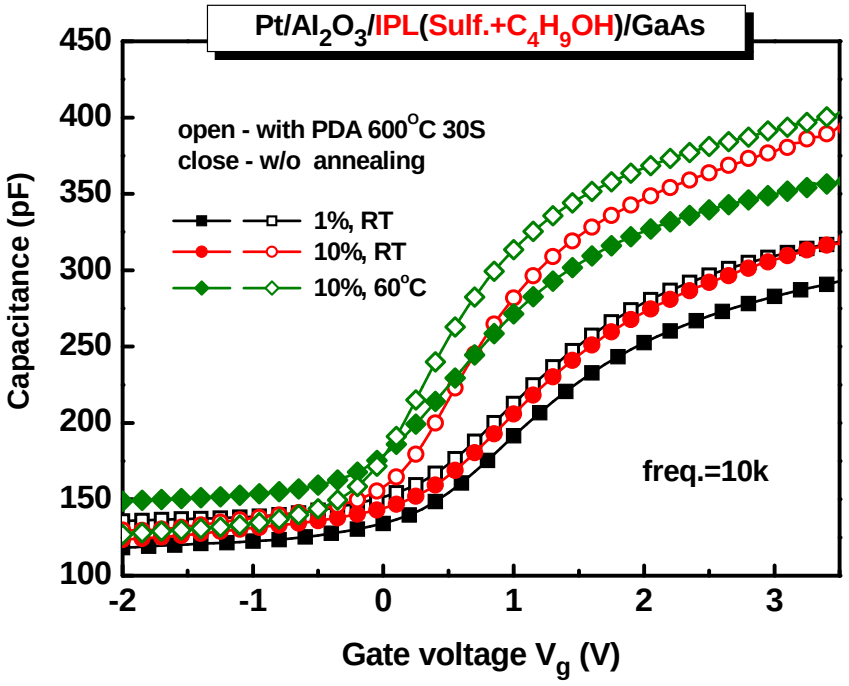


Fig. 2-10 The C-V(10kHz) curves of $Pt/Al_2O_3/GaAs$ MOS capacitors with $(NH_4)_2S+C_4H_9OH$ treatments. The Al_2O_3 was deposited by ALD (300 °C, 60 cycs.).

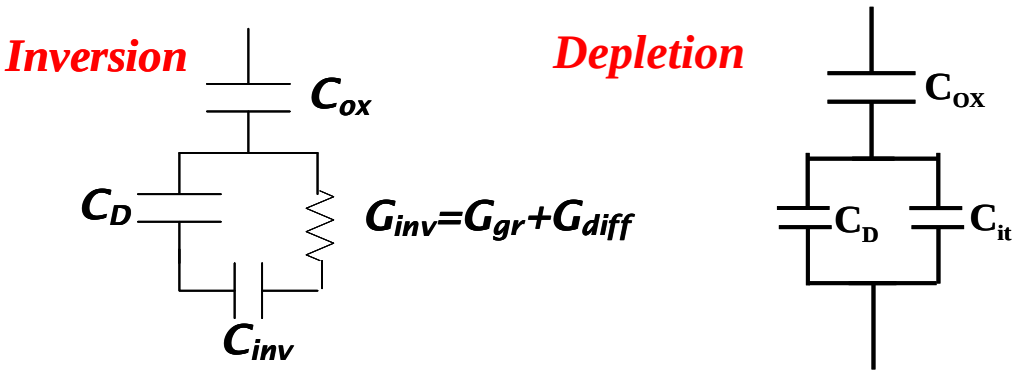


Fig. 2-11 Capacitances of an MOS capacitors for various bias conditions

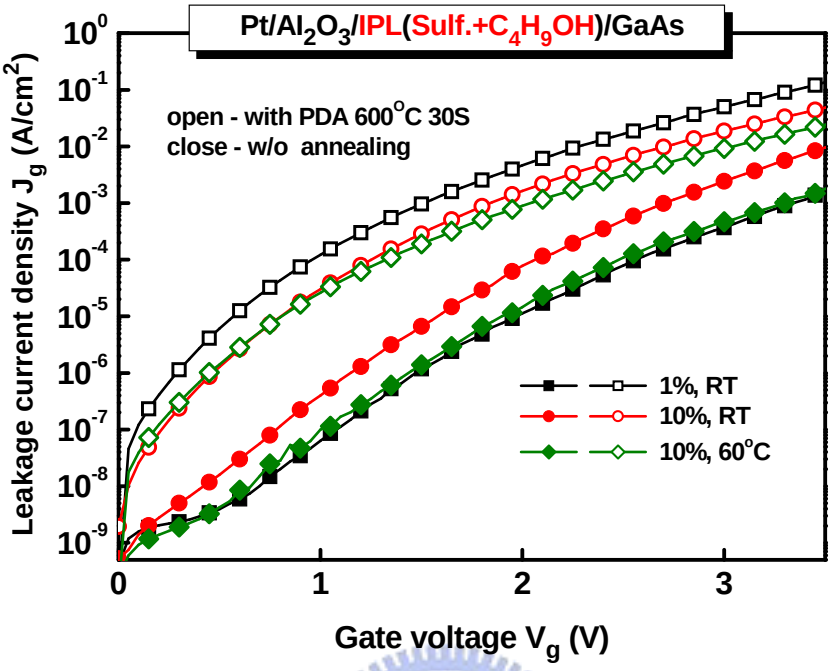


Fig. 2-12 J-V characteristics of Pt/Al_2O_3/GaAs MOS capacitor $(NH_4)_2S+C_4H_9OH$ with and without 600 °C O_2 PDA. The Al_2O_3 was deposited by ALD (300 °C, 60 cycles)

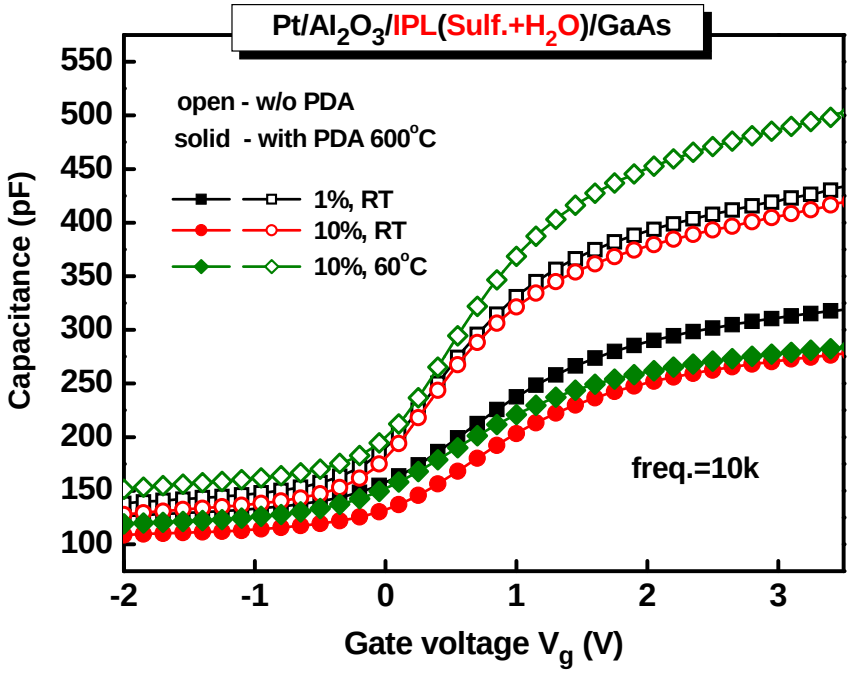


Fig. 2-13 (a) C-V(10kHz) curves of $Pt/Al_2O_3/GaAs$ MOS capacitors with $(NH_4)_2S+H_2O$

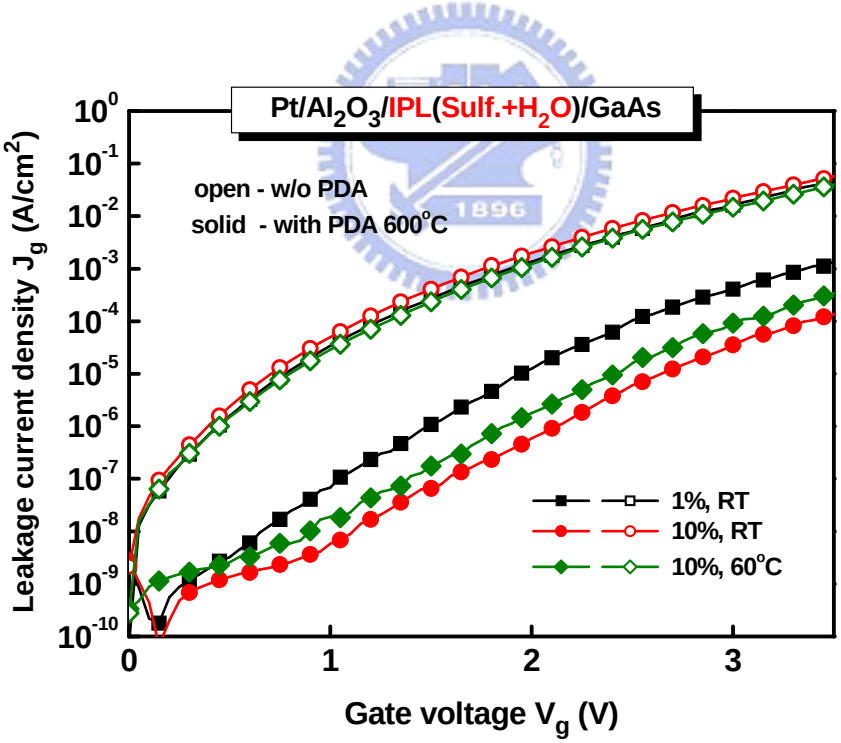


Fig. 2-13 (b). J-V characteristics of $Pt/Al_2O_3/GaAs$ MOS capacitor $(NH_4)_2S+H_2O$ with and without 600 °C O_2 PDA. The Al_2O_3 was deposited by ALD (300°C, 60 cycles)

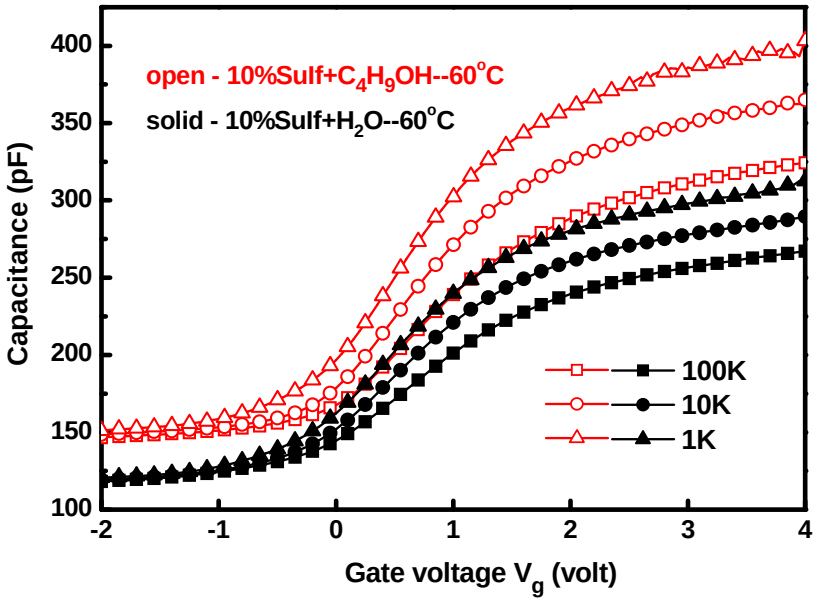


Fig. 2-14 (a) Multi-frequency C-V characteristics of MOS capacitors ($Pt/Al_2O_3/GaAs$) with $(NH_4)_2S+C_4H_9OH$ and H_20 at 60°C.

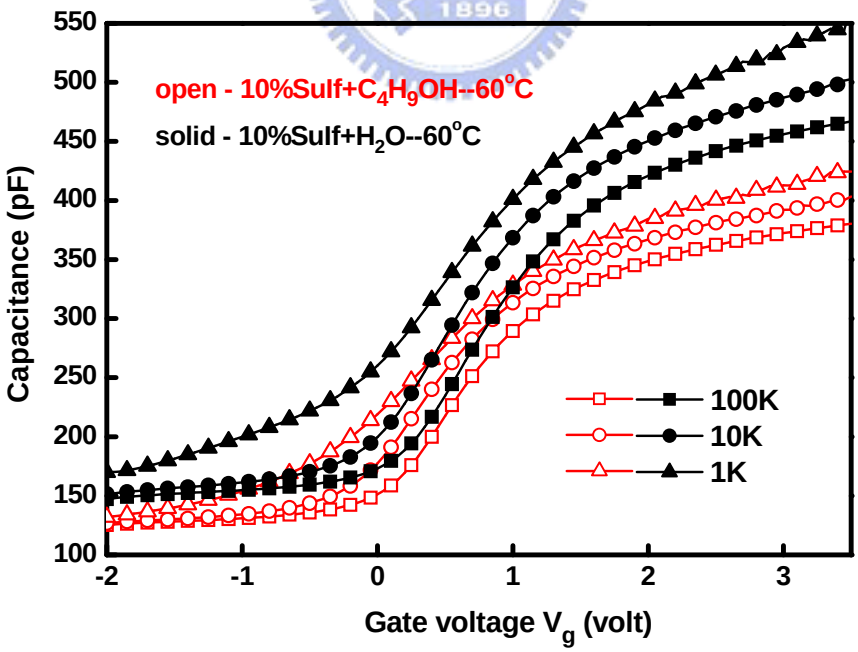


Fig. 2-14 (b) Multi-frequency C-V characteristics of MOS capacitors ($Pt/Al_2O_3/GaAs$) with $(NH_4)_2S+C_4H_9OH$ and H_20 at 60 °C with 600 °C O_2 PDA.

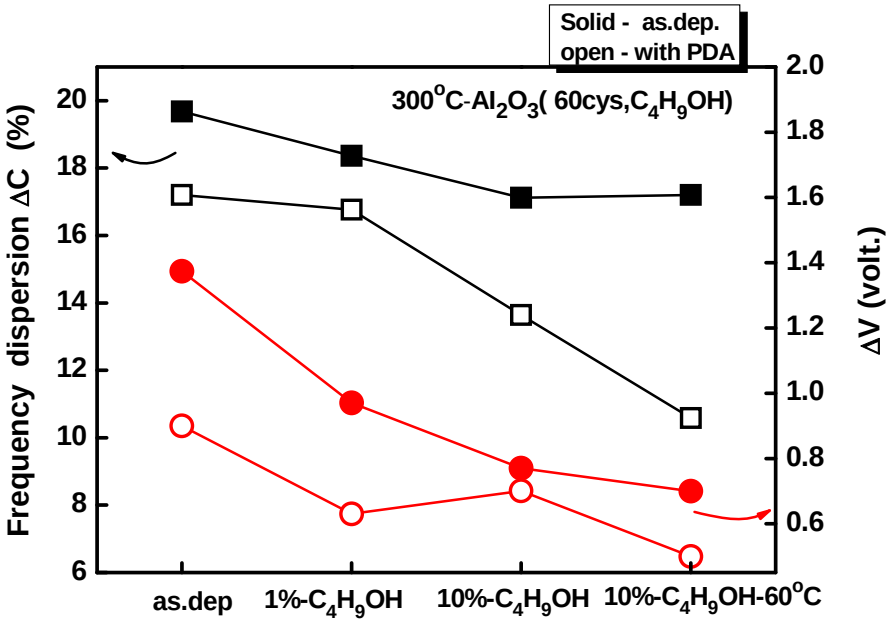


Fig. 2-15 (a) ΔC and ΔV versus different IPLs with $(NH_4)_2S$+$C_4H_9OH$by ALD (300 °C, 60 cycles)

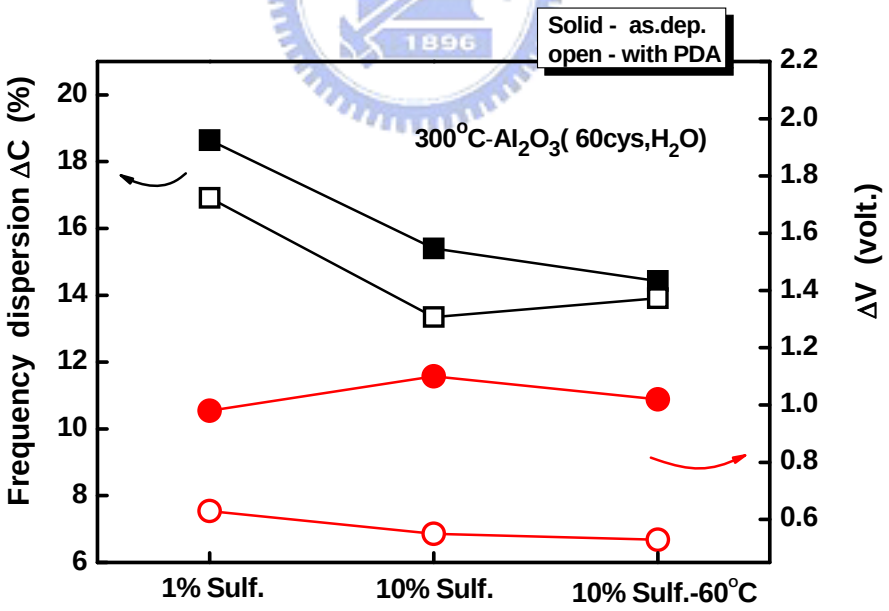


Fig. 2-15 (b) ΔC and ΔV versus different IPLs with $(NH_4)_2S$+H_2O by ALD (300°C, 60 cycles)

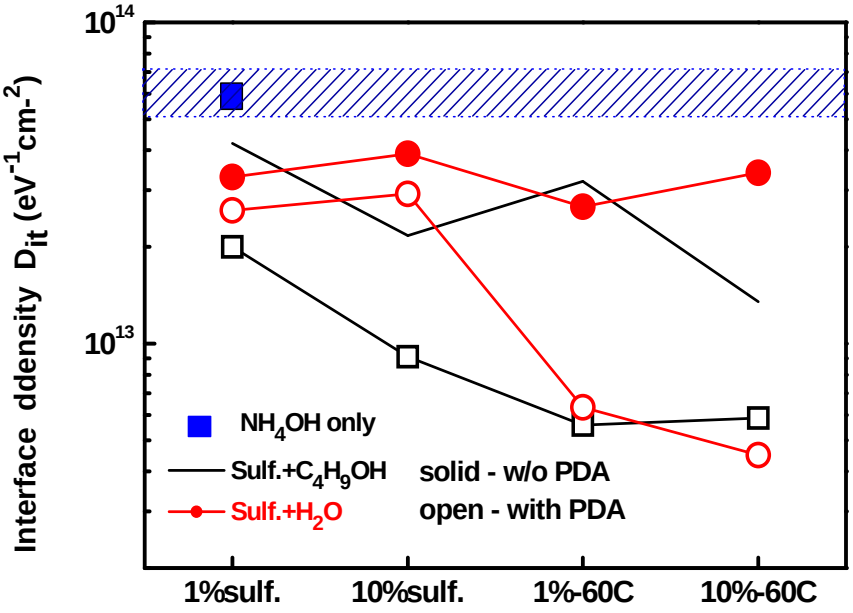


Fig. 2-16 D_{it} versus different IPLs for MOS capacitors $Pt/Al_2O_3/GaAs$ made by ALD (300^oC, 60 cycles)

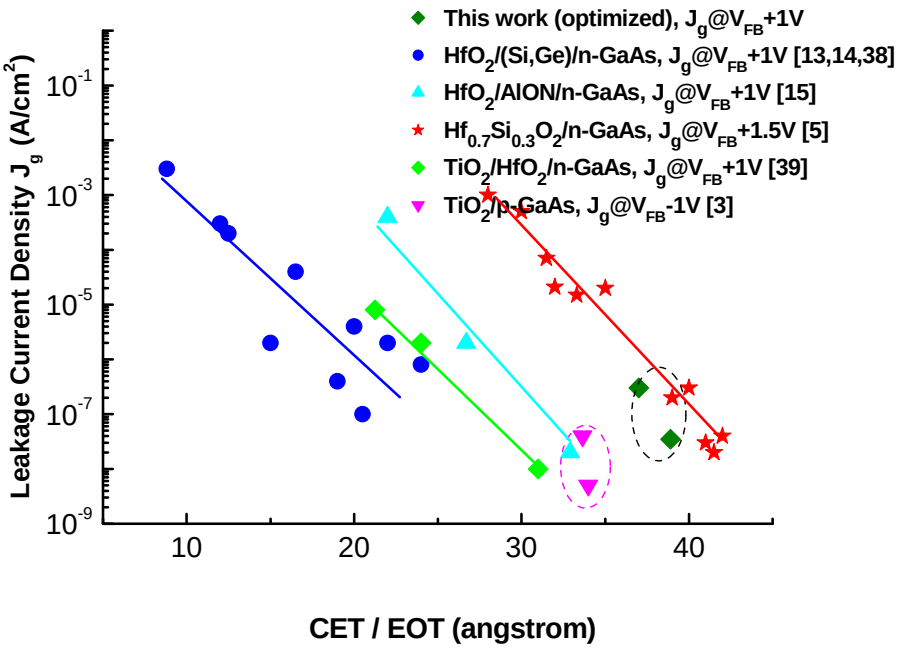


Fig. 2-17 (a) Comparison of J_g versus CET or EOT characteristics in this work with other's published data.

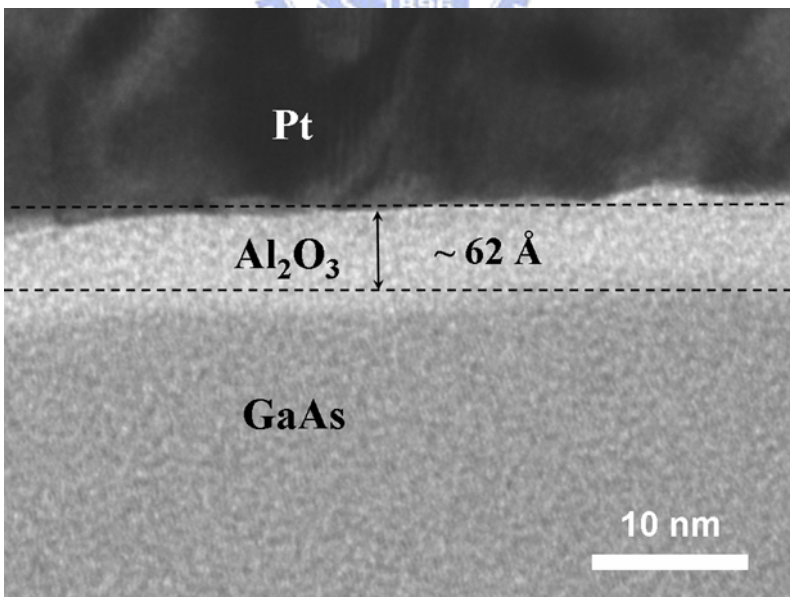


Fig. 2-17 (b) The HRTEM images of Al_2O_3 film by ALD 60 cycles on GaAs. The sulfide treatment was $(NH_4)_2S+C_4H_9OH$

Parameter (@300K)	n_i *(cm^{-3})*	E_g *(eV)*	μ_p *($cm^2 V^{-1}S^{-1}$)*	L_p *(um)*	C_d *(nF/cm^{-2})*	C_{ox} *(nF/cm^{-2})*	G_{gr} / G_{diff}	τ *(nS)*	f_{trans} *(KHz)*
GaAs	*2.1E6*	*1.43*	*200*	*~40*	*~250*	*1000*	*5E-4/ ---*	*3000*	*~0.1*
InAs	*1E15*	*0.36*	*100*	*~10*	*~33*	*700*	*--- / 1.6*	*20*	*~380*
InSb	*2E16*	*0.12*	*500*	*~10*	*~62*	*600*	*--- / 32*	*1.9*	*~8200*

Table III. The parameters of GaAs, InAs and InSb

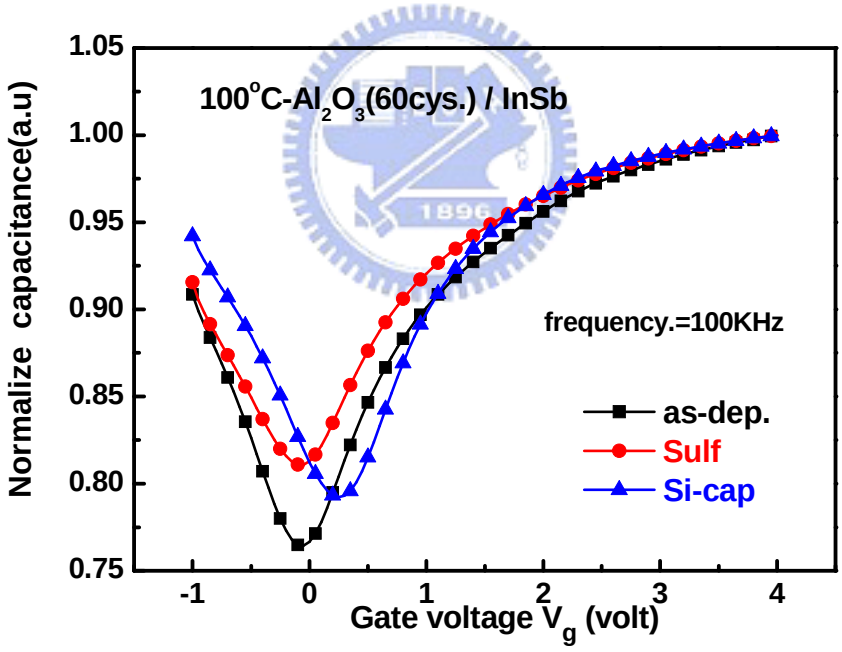


Fig. 2-18 Pt/Al_2O_3/InSb normalize *C-V* curves are recorded at 100kHz with different treatment.

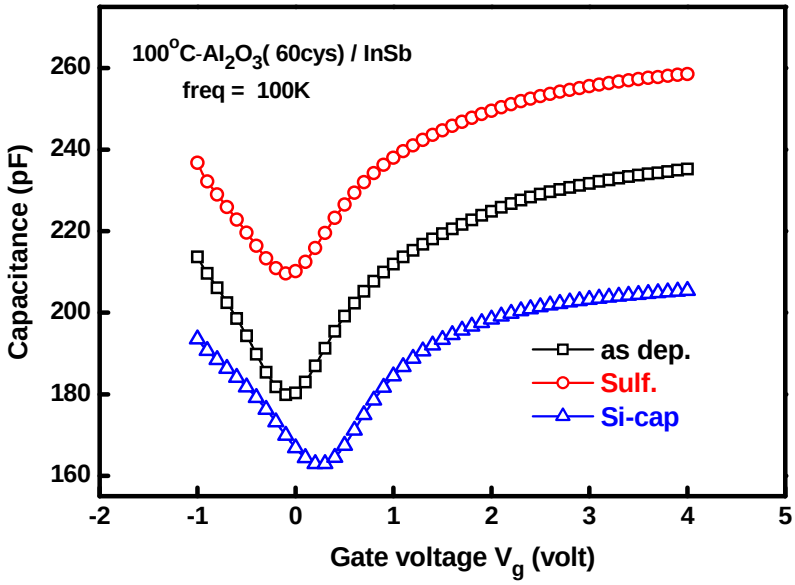


Fig. 2-19 (a). Pt/Al_2O_3/InSb *C-V* curves are recorded at 100kHz with different treatment.

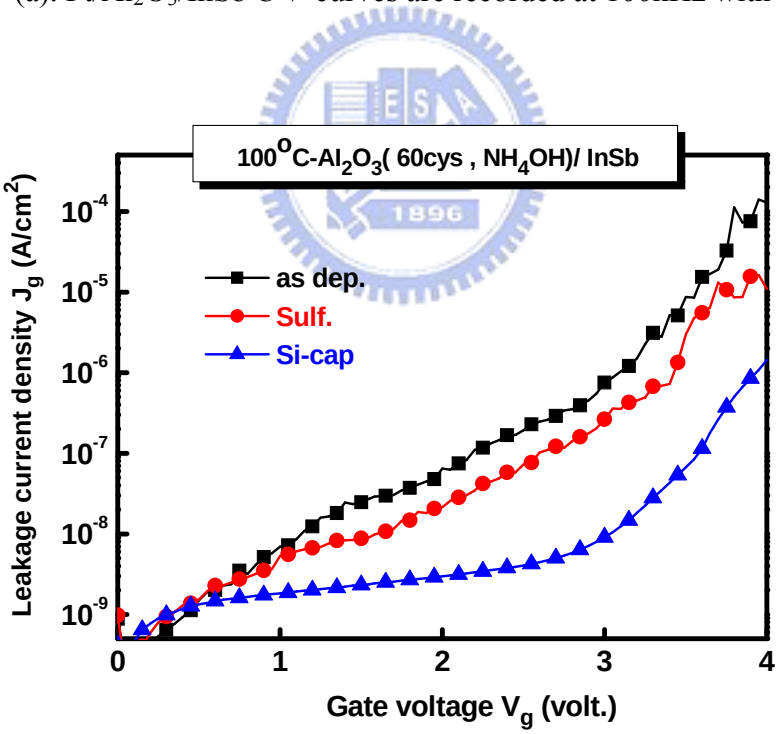


Fig. 2-19 (b) Pt/Al_2O_3/InSb Room temperature *J-V* curves are recorded with different surface treatment.

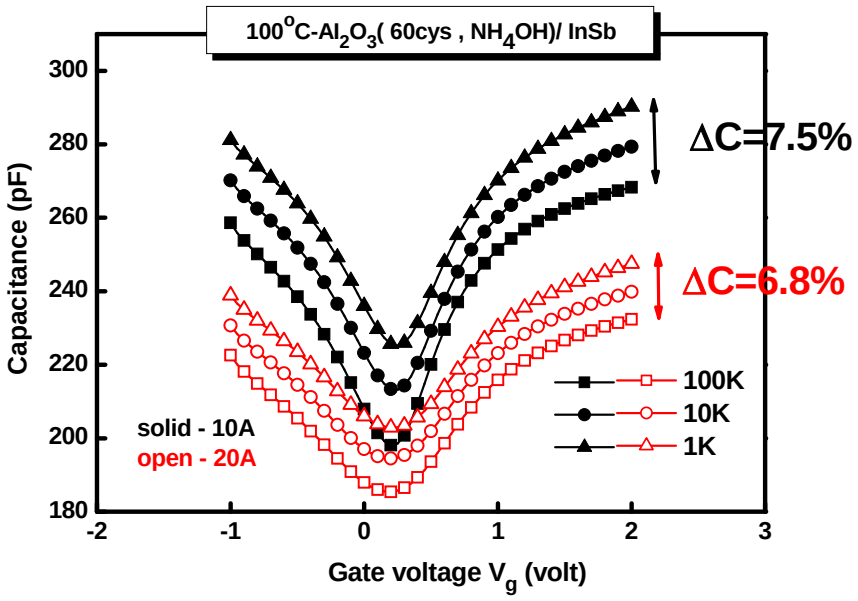


Fig. 2-19 (c) Multi-frequency C-V characteristics of MOS capacitors ($Pt/Al_2O_3/InSb$) with different Si capping thickness.

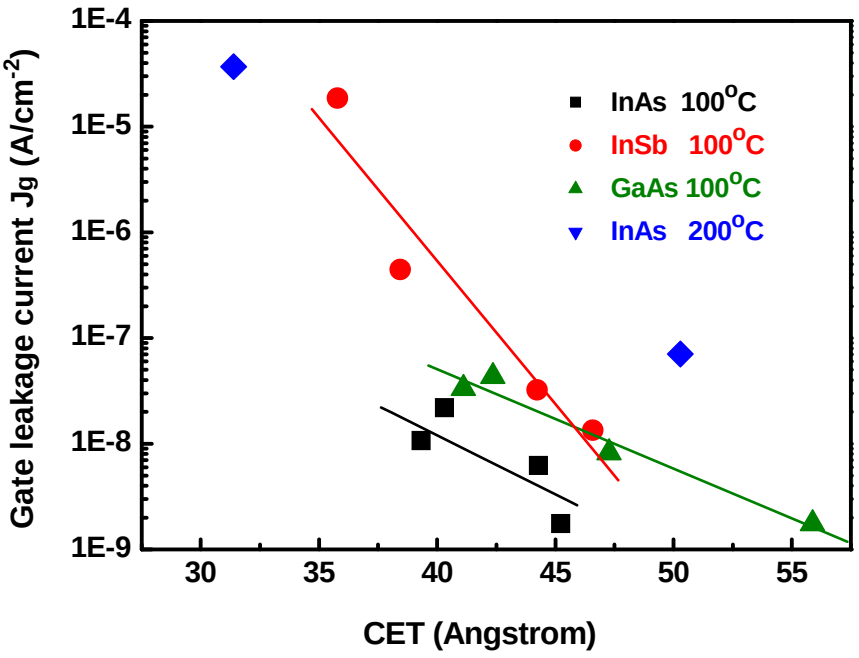


Fig. 2-20 J_g vs. CET for MOS capacitors (Pt/Al_2O_3/III-V) made by ALD (100 °C and 200°C)

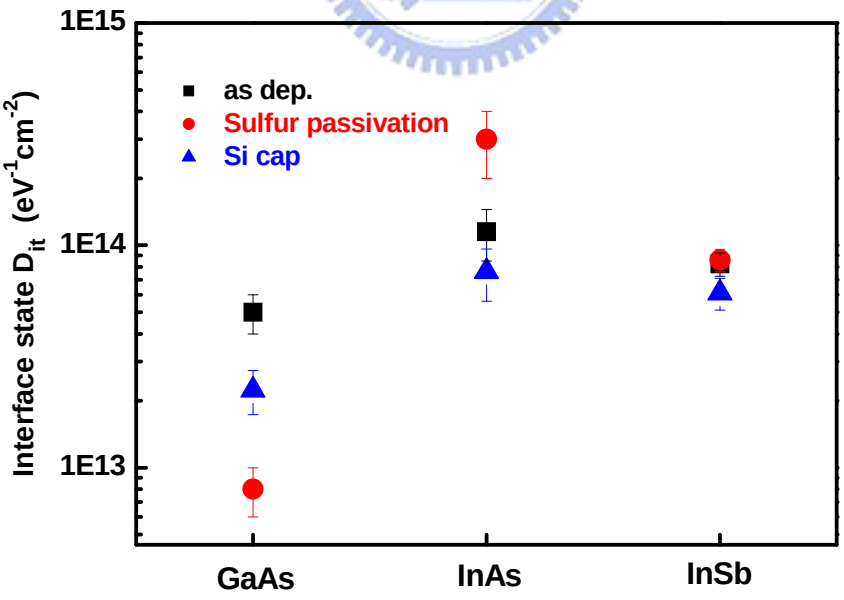


Fig. 2-21 D_{it} vs different surface treatment characteristics of Pt/Al_2O_3/III-V MOS capacitor made by ALD (60cycles) at 100 °C and 300 °C

Chapter 3

Alloyed Source/Drain Ohmic Contact on GaAs

3-1 Introduction

One important factor influencing the performance of GaAs MOSFET is the characteristic of ohmic contact at the drain and source terminals. Contact qualities, including specific contact resistance, contact uniformity and surface morphology, showed a strong dependence on the control of overall process conditions. After optimization, a specific contact resistance of 10^{-6} Ω-cm^2 was achieved. The key to the success of this device is the fabrication of a high quality gate oxide on GaAs. In addition to the gate oxide, the ohmic contacts to the n-GaAs channel at the source and drain terminals of the device are very important to the MOSFET performance. In this chapter, we deposited several metal alloys under different annealing temperature to form Ohmic contact on GaAs. We also used transmission line model (TLM) to calculate the specific contact resistance .Various material analysis techniques, such as AFM, SEM, Auger Depth profiling, and Transmission Electron Microscopy (TEM) were performed to observe the alloyed characteristics. Finally, we sought the optimized condition to fabricate GaAs MESFET and MOSFET in the next chapter.

3-2 Experimental Procedures

We used Acetone to remove metal-organic residues and diluted hydrochloric acid (HCl) about 10% to reduce native oxides. Next, the mesa etching structure was made to suppress the extra transport current through the etching solution (H_3PO_4 : H_2O_2 : H_2O = 60 : 20 : 1500). The TLM structure in Fig. 3-1 showed that the height was 50 um and the width was 100 um, in which the corresponding space of each pattern was 5, 10, 15, 20, 25, 30, 40 um, respectively. By using the TLM pattern, we soaked the samples in HCl solution for ca. 3 min and then deposited different materials, such as Au/Ge/Ni [1], Pd/Ge, Pt/In, on n-GaAs [2] substrate via lift-off process. Ohmic contact was formed by RTA at different temperatures and annealing times.

3-3 Results and Discussions

The conduction mechanisms for a metal on n-type semiconductor are illustrated in Fig. 3-2. For the low-doped semiconductor, the current flows as a result of thermionic emission (TE) [3]. In the intermediate doping range, thermionic-field emission (TFE) dominates; the carriers are thermally excited to have an energy where the barrier was sufficiently narrow for tunneling to take place. For high doping densities, the barrier was sufficiently narrow near the bottom of the conduction band for the electrons to tunneling directly, know as field emission (FE). The three regimes can be differentiated by considering the characteristic energy E_{00}

[4]defined by

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{K_S \varepsilon_0 m^*_{tun}}} \tag{3.1}$$

Where N was the doping density, and m* was the tunneling effective mass (In general, $E_{00} < 0.2$ kT for TE, for TFE, 0.2 kT $< E_{00} <$ 5 kT, and for FE, $E_{00} >$ 5 kT) [8]. Indeed, we characterized that the contact resistance is strongly dependent on GaAs doping level in our experiments.

When current flows from the semiconductor to the metal, it sees the ρ_c and ρ_S resistance. The potential distribution under the contact can be determined by both ρ_c and ρ_S, according to Eq. 3.2,

$$V(x) = \frac{I\sqrt{\rho_S \rho_C}\cosh(L - x/L_T)}{Z\sinh(L/L_T)} \tag{3.2}$$

Where L was the contact length, Z was the contact width and I was the current flowing into the contact. With V measured between two contact metal, the contact resistance can be described from Eq. 3.3

$$R_{cf} = \frac{V}{I} = \frac{\rho_c}{L_T Z}\coth\left(\frac{L}{L_T}\right) \tag{3.3}$$

For $L \geq 1.5\ L_T$, $\coth(L/L_T) \sim 1$ and R_c can be described as follow

$$coth\left(\frac{L}{L_T}\right) \approx 1 \qquad Rc \approx \frac{\rho_c}{L_T Z} \tag{3.4}$$

We can calculated the specific contact resistance through above equations.

The most common approach to the formation of AuGe-based ohmic contacts [6][7] is to evaporate layers of Ni, Ge, and Au metals onto the GaAs sample followed by annealing. It is known that the specific contact resistance [5] became increasing and unstable at annealing temperature above 400 °C. so that the appropriate RTA temperature was about 400 °C in this study. Figs. 3-3 (a)-(c) display the specific contact resistance at 350, 400 and 450 °C, respectively. The annealing time ranging from 30 to 120 s was also examined, as the results showed in Fig. 3-4. From the experiments, we can conclude the optimized condition for GaAs Ohmic contact that was annealed at 400 °C for 60 s by depositing AuGeNi alloy on GaAs. During the alloying process, Ge diffuses into the GaAs channel layer and creates a highly conductive n-type layer below the contact at 300 °C. Here, we display the AES depth profiling before and after different processing temperatures of 400 °C and 450 °C in Fig. 3-5 (a)-(c). It was found that Ge diffuses into GaAs at 400 °C, while Ga and As are out-diffused through Ni at the same time. We could observe serious Ge out diffusion at 450 °C, accompanying with an increase interface roughness. Figs. 3-6 and 3-7 show the AFM and SEM images after various annealing temperatures, respectively. Obviously, the higher the temperature used, the rougher the top surface and metal-substrate interface was observed. Here, Ni is added into the alloy as a wetting agent. The low surface tension of Ni helps to prevent the AuGe metal from ”balling-up” during alloying and to improve the contact

adherence. Au enhances the out-diffusion of Ga, resulting in Ge substituting Ga sites, which produces the desired highly doped n^+-GaAs layer. These properties make the Au–Ge–Ni alloy favorable than the nonalloy contacts in producing low-resistance ohmic contacts on a lightly doped GaAs because nonalloy contacts require a higher doping concentration in the GaAs to achieve ohmic and reduce resistance. However, an excess of Au or Ni can degrade the contact resistance. Excess Au most likely leads to excess Ga out-diffusion, which leaves behind an excess As. Also, Au and Ni act as acceptors and may compensate the donors in the underlying n-doped highly conductive layer. Here, we showed TEM image of AuGeNi/GaAs in Fig. 3-8.Several components, like Ni-Ge, Ni-As-Ge grains and Au-Ga grains were observed [9][10].

The advantages of Pd include an excellent contact resistance and an excellent smooth morphology. According to previous studies, the roughness of Pd/Ge was lower than that of Au/Ge/Ni in Ohmic contact. Pt/In structure was tested on n-GaAs because In metal produced the As-riched surface easily and caused a strong Fermi level pinning (and in turn obtained a good Ohmic contact). Unfortunately, we did not get the optimized condition in this material due to low thermal stability of In material. All materials we tried in Ohmic contact were displayed in Fig. 3-9. Finally, AuGeNi alloy was employed in the fabrication of GaAs MESFET and MOSFET in next chapter.

3-4 Summary

We had tested PdGe, and PtIn, AuGeNi metal alloys on n-GaAs to form Ohmic contact. From our experiments, the respective specific contact resistivity of PdGe and PtIn metal alloys on GaAs were found to be 1E-3 and 8E-3 Ω-cm^2, respectively. We can obtain the lowest specific contact resistivity of 2.2E-5 Ω-cm^2 for AuGeNi on GaAs after 400 ^{o}C for 30 s in N_2 ambient. Besides, we could get the smaller specific contact resistance on highly-doped GaAs. It was believed that the Ohmic contact resistivity can be improved by optimizing the respective metal-alloy thickness, processing temperature, and time, etc.

References

[1] Hung-Cheng Lin, Sidat Senanayake, Keh-Yung Cheng, , Minghwei Hong, ,J. Raynien Kwo, Bin Yang, and J. P. Mannaerts*"Optimization of AuGe–Ni–Au Ohmic Contacts for GaAs MOSFETs."* IEEE Trans Electron Dev. 50, (2003)

[2] N.Braslau,"Alloyed Ohmic Contacts to GaAs. ", J.Vac.Sci.Technol.19, 803 (1981); Thin Solid Films, 104(1983) 391

[3] S. M. Sze, Physics of Semiconductor Devices, Wiley, New York, Chapter 8 (1969).

[4] E. H. Rhoderick, Metal-semiconductor Contacts, Clarendon Press, Oxford (1978).

[5] G. S. Marlow and M. B. Das, "The Effects of Contact Size and Non-zero Metal Resistance on the Determination of Specific Contact Resistance," Solid-State Electronics. Vol. 25. No. 2, pp.91-94, 1982.

[6] K.A. Jones, K.P. Hilton, B.T. Hughes, M.W. Cole, and W.Y. Han, "Analysis of Ohmic Contacts to GaAs Based Microwave HBT's " 1995 British Crown Copyright.

[7] Nacy E. Lumpkin, Gregory R. Lumpkin, "Investigation of the roleof Ni in forming ultra-low resistance Au-Ge-Ni Ohmic Contacts to n+ GaAs (1997 IEEE)

[8] H.H. Berger, "Contact Resistance and Contact Resistivity." , J.Electrochem. Soc., pp.507-514(1972)

[9] K.A. Jones, K.P. Hilton, B.T. Hughes, M.W. Cole, and W.Y. Han, "Analysis of Ohmic Contacts to GaAs Based Microwave HBT's " 1995 British Crown

Copyright.

[10] R.E.William, in Gallium Arsenide Processing Techniques (Artech House, Massachusetts, 1984), pp.225-258

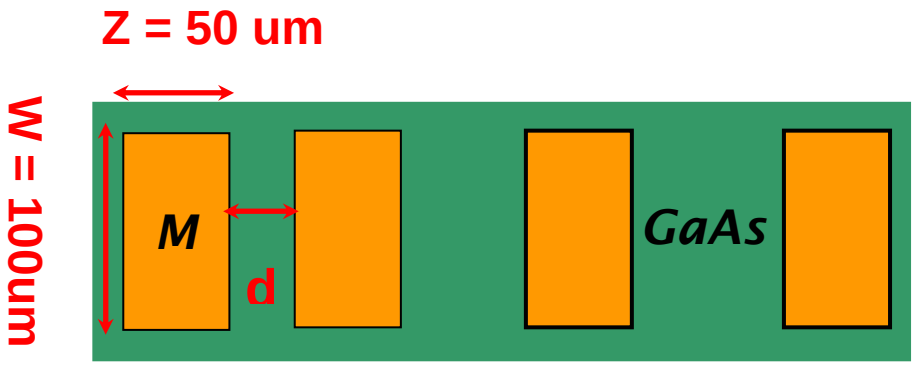


Fig. 3-1 Transfer length method (TLM) test structure (Z=50um W=100um)

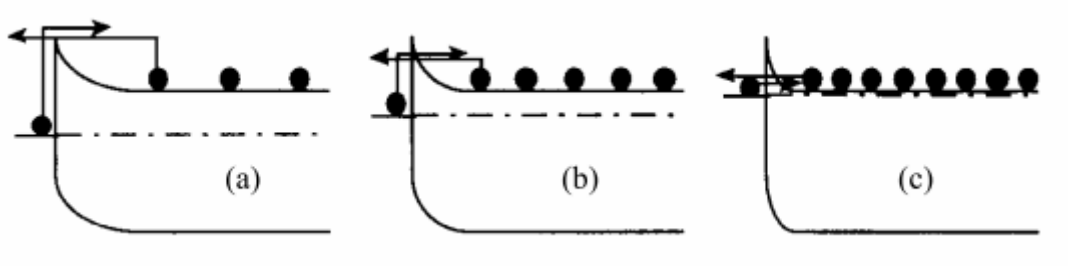


Fig. 3-2 Depletion-type contacts to n-type substrates with increasing doping concentrations. The electron flow is schematically indicated by the electron and their arrows (a) Thermionic emission (b) Thermionic/Field emission (c) Field emission

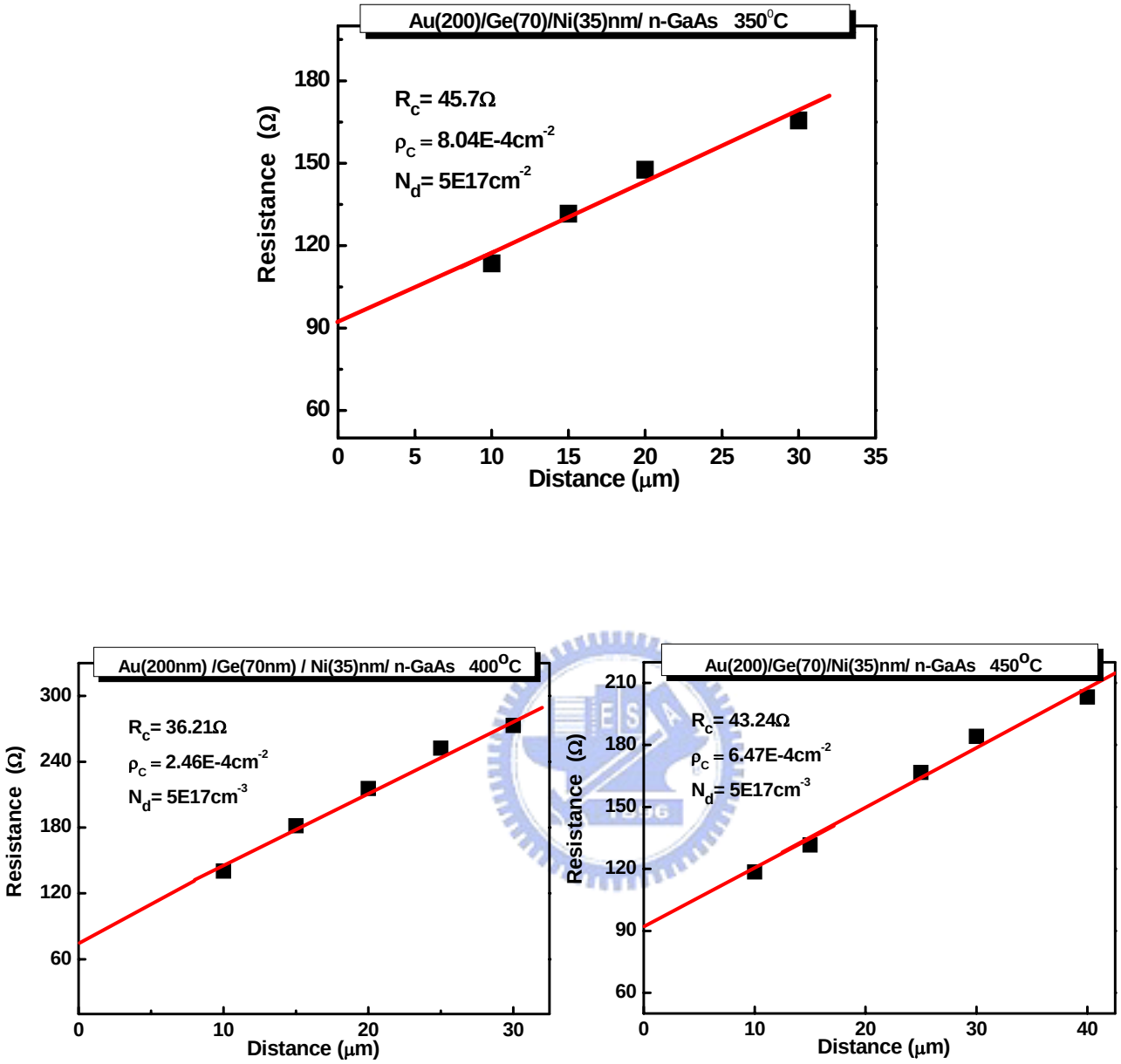


Fig. 3-3 The specific contact resistuvity of alloy AuGeNi annealing at (a)350 °C (b) 400 °C (c)450 °C, respectively.

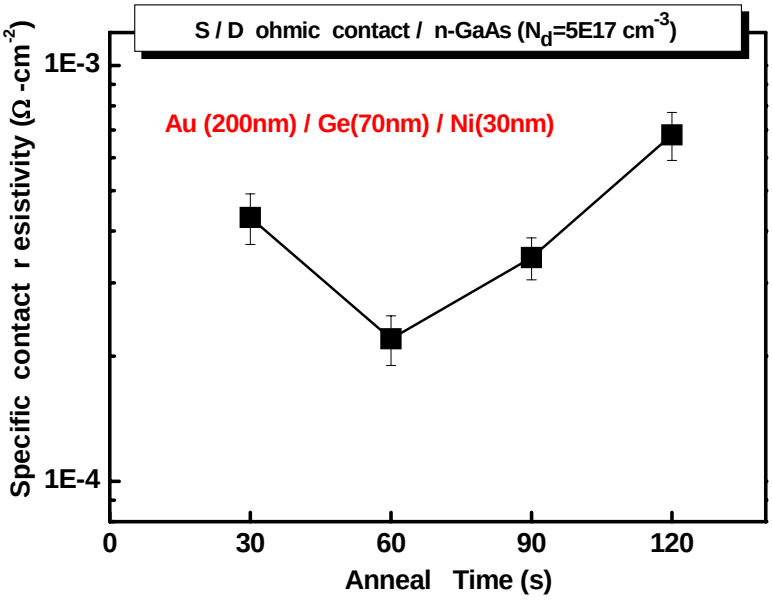
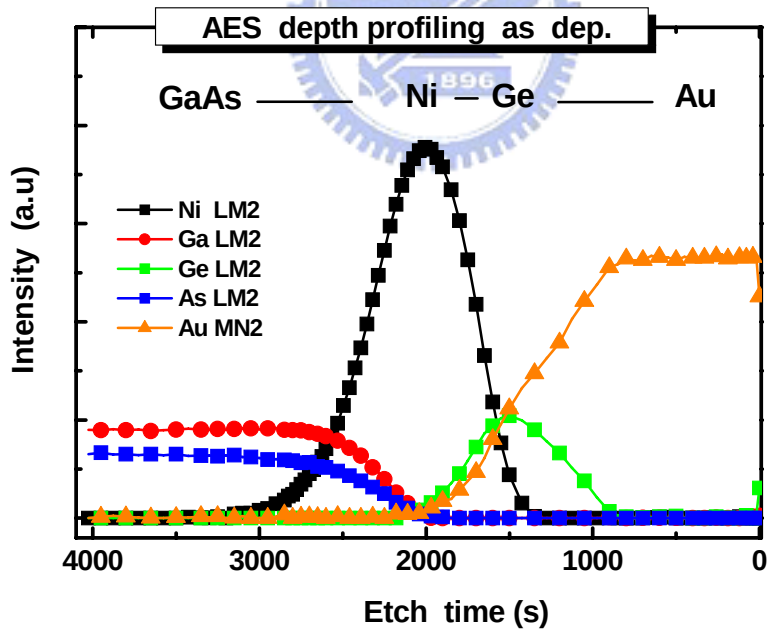
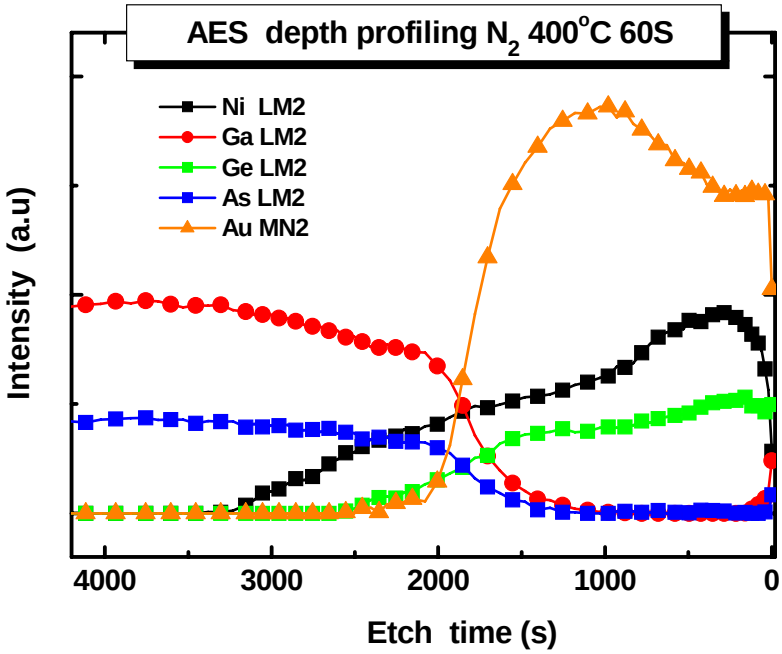


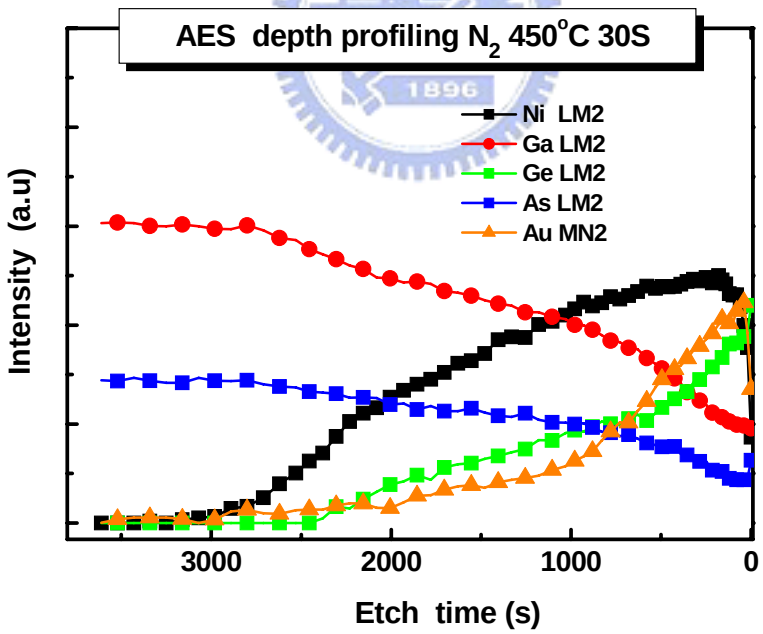
Fig. 3-4 The specific contact resistivity as a function of anneal time with AuGeNi



(a)



(b)



(c)

Fig. 3-5 AES depth profiling of AuGeNi at (a) 350 °C (b) 400 °C (c) 450 °C

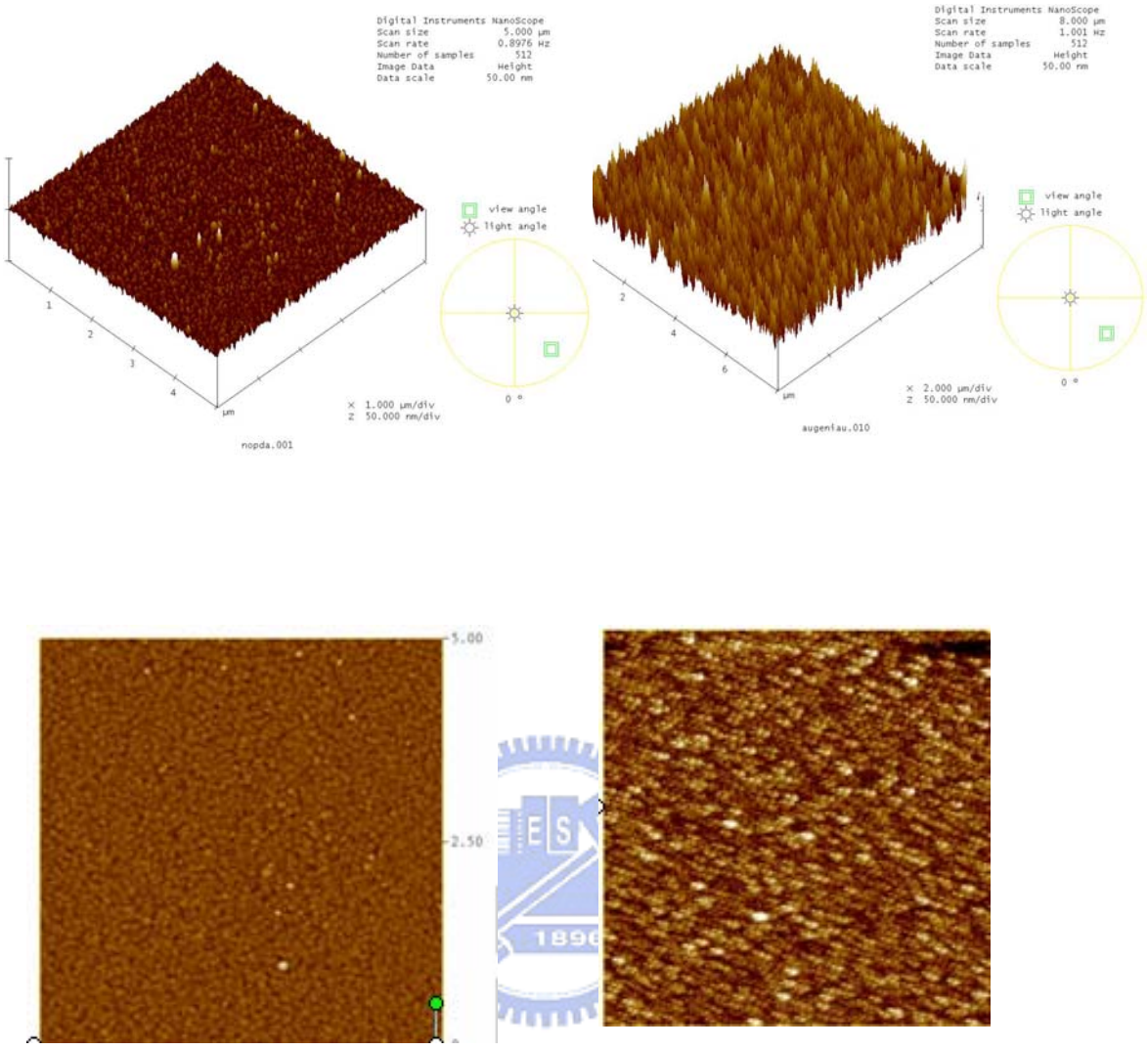


Fig 3-6. AFM surface morphology of AuGeNi at (a) as dep. (b) 400 °C

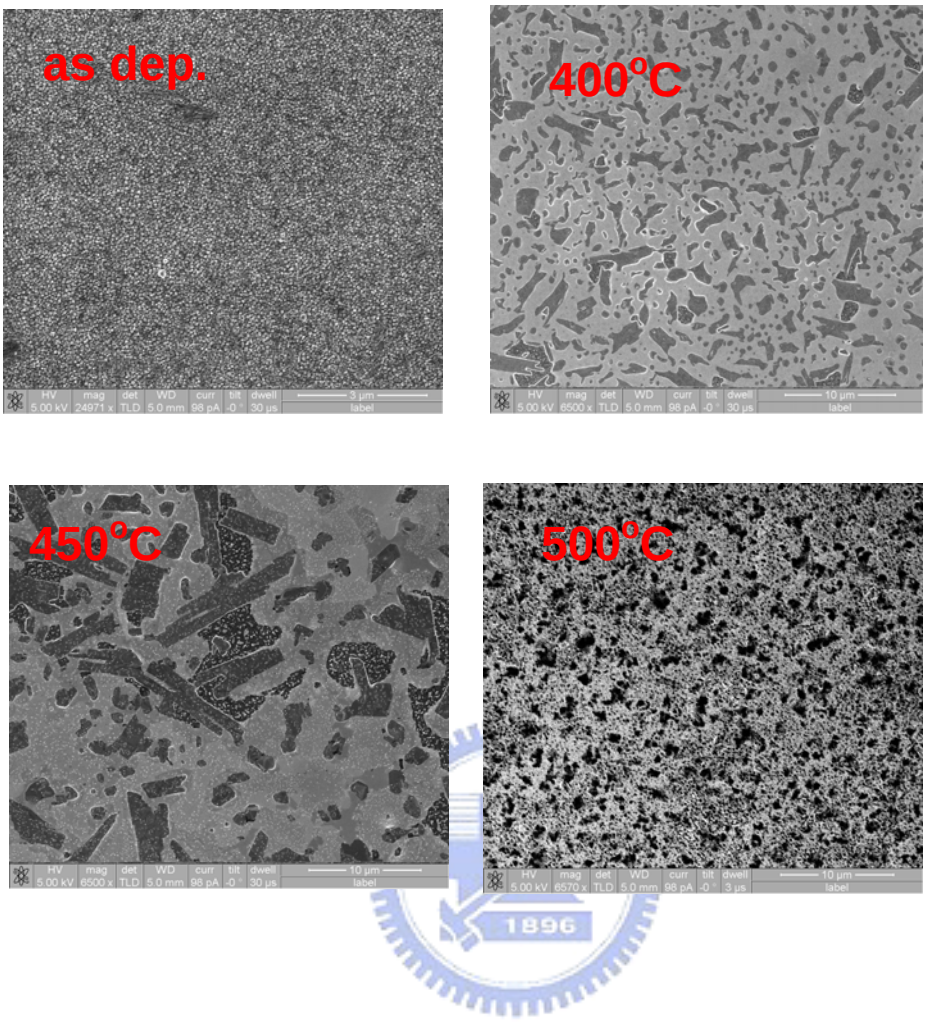


Fig 3-7. SEM surface morphology of AuGeNi at (a) as dep. (b) 400 °C (c) 450 °C (d) 500 °C

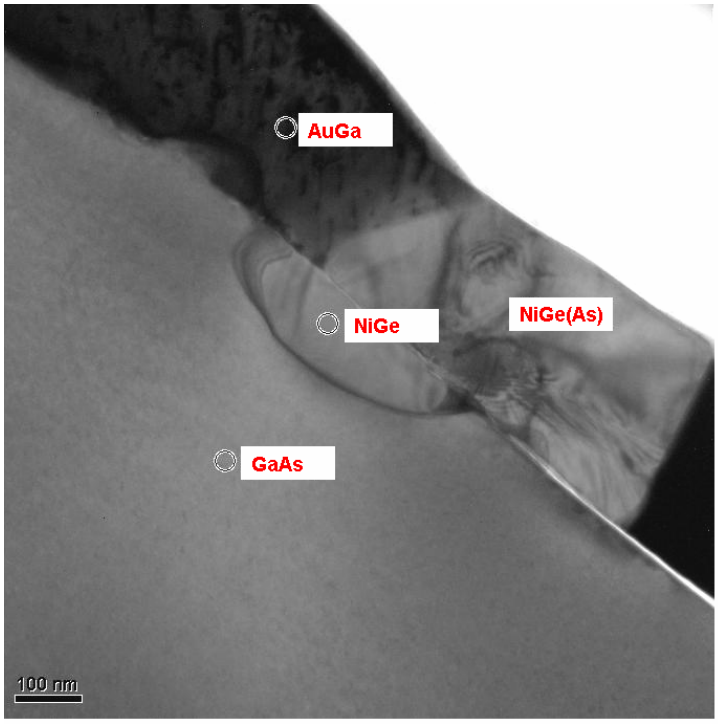


Fig 3-8. The HRTEM images of AuGeNi/n-GaAs at 400 °C in the N_2 ambient

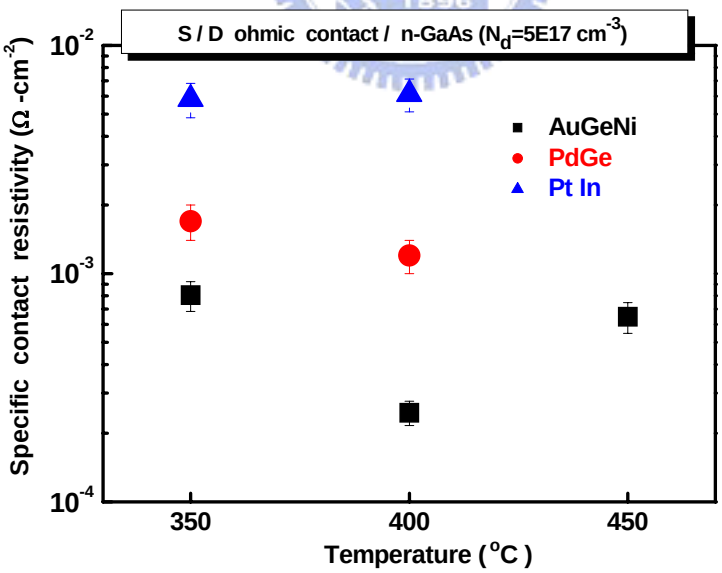


Fig 3-9. The specific contact resistivity of various materials at different temperatures.

Chapter 4

Electrical characteristics of GaAs MESFET & MOSFET with ALD- Al_2O_3 dielectric

4-1 Introduction

In small signal GaAs metal semiconductor field-effect transistors MESFET [1-3], where transconductance is of prime importance and the devices are operated at comparatively low current and biasing voltage, gate recesses are usual. For good high-frequency and noise performance, the depth and shape of the recess are both important. From design and fabrication points of view the question to answer is: to what extent can the gain loss due to high output conductance be compensated for by increased transconductance ? It is difficult to separate the consequences of having gate recess from other factors because, to a degree, they are interdependent. The advantages and disadvantages associated with the recessed-gate technology suggest that there should be an optimum value of residual channel thickness after the gate recess etching.

Since the higher electron mobility in GaAs and availability of semi-insulating GaAs substrate, GaAs-based devices, such as GaAs MESFET, are widely used for high speed circuit applications and monolithic microwave integrated circuits. However, the gate current of the

Schottky contact becomes appreciable for the forward bias of several tenths of a volt, which severely limits on the maximum drain currents, the noise margin, and the flexibility of the circuit design. The insulating gate of MOSFET can improve the drawbacks. Compared to GaAs MESFETs, GaAs MOSFETs [4-13] feature a larger maximum drain current, much lower gate leakage current, a better noise margin, and much greater flexibility in digital integrated circuit design. Nevertheless, The main obstacle to GaAs-based MOSFET devices is the lack of high-quality, thermodynamically stable insulators on GaAs that can match the device criteria as SiO_2 on Si. The recent development of high-quality ALD gate dielectrics on III-V compound semiconductors. This process does not require ultra high-vacuum conditions for wafer transfer between semiconductor epi-layer growth and oxide layer deposition and may find wide applications in microelectronics manufacturing. In this chapter, we deposited Al_2O_3 as gate dielectric and compared MESFET and MOSFET characteristic difference.

4-2 Experimental Procedures

4-2-1 Device structure (MESFET)

For the n-channel GaAs MESFET, we used different channel concentrations to adjust driving current performance. The channel layer of 1000 Å with Si-doped N_d = 6E16 cm^{-3} and the S/D capping layer (500 Å, N_d = 4E17 cm^{-3}). Device isolation was achieved by wet etching with H_3PO_4 : H_2O_2 : H_2O = 60 : 20 : 1500, which etching rate is about 10 Å/s and

showed in Fig. 4-1. In MESFET fabrication, the first step is the mesa etching to semi-insulator GaAs substrate for the definition of active area region, as the image shown in Fig. 4-2. Next, E-beam evaporated Ni/Ge/Au (300 Å/700 Å/2000 Å) was deposited as S/D ohmic contact, followed by RTA at 400 ^{0}C for 60s in N_2 ambient. And then, we used T-gate mask to achieve recess gate and etched by the solution as mentioned above. After recess gate etching, we deposited Ti/Pt/Au (300 Å/250 Å/1800 Å) as Schottky contact through lift-off process. Finally, a forming gas annealing at ~ 400 ^{o}C for 10 min was used to reduce interfacial trapped charge. The fully process flow was shown in Fig. 4-3.

4-2-2 Device structure (MOSFET)

Depletion-mode GaAs MOSFET was fabricated on semi-insulator GaAs substrate. A 2000 Å undoped GaAs buffer layer and a 1000 Å Si-doped GaAs layer (4E17 cm^{-3}) were sequentially grown by MBE on a (100)-oriented semi-insulating 2-in GaAs substrate. Here we split two structures in our researches: one is the channel layer of 1000 Å with Si-doped N_d = 6E16 cm^{-3} and the S/D capping layer (500 Å, N_d = 4E17 cm^{-3}), while another is the channel layer of 1500 Å with Si-doped N_d = 5E17 cm^{-3} and the S/D capping layer (400 Å, N_d = 2E18 cm^{-3}). First, the mesa etching was succeeded by wet etching as mentioned before. Second, we deposited Al_2O_3 by ALD process for gate dielectric and then deposited 5000 Å-Al for T-gate. Al gate etching was performed by wet etching with the solution (HNO_3 :

H_3PO4 : CH_3COOH : H_2O = 40 : 60 : 20 : 1500). The nominal source-to-gate and drain-to-gate spacing of the fabricated devices were 3 um, and the gate width was 100 um. The fully process flow was shown in Fig. 4-4 and the HRTEM images were displayed in Fig. 4-5.

4-3 Results and Discussions

4-3-1 Electrical characteristics of GaAs MESFET

DC characteristics of GaAs MESFETs were measured by HP4200 and HP4284, respectively. The contact resistance was compared with capping layer different. Fig.4-6 demonstrated Schottky Igs-Vgs characteristics with (control) and without the recess gate formation. As seen, the breakdown field increased after etching n^+ capping layer obviously. FGA repaired the metal-semiconductor interface, thus revealing the better I_g–V_g Schottky and I_{ds}–V_{gs} characteristics, as displayed in Figs. 4-7 (a) and (b). We found that the subthresold swing and threshold voltage decreased after forming gas annealing. According to the following equation (4.1),

$$V_T = V_{bi} - V_P \tag{4.1}$$

Where $V_{bi} = \varphi_{Bn} - \varphi_n$ $V_p = \frac{x_C^2 q N_D}{2\varepsilon_{GaAs}}$

The possible reason we attributed is the decrease in Schottky barrier height after forming

gas annealing. S/D Ohmic contact with and without FGA were shown in Fig. 4-8 [14-16] ; we obviously observed the lower specific contact resistance. Fig. 4-9 shows I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics; the dc characteristics showed a clear pinch-off and channel modulation, with a peak extrinsic transconductance of 5.5 mS/mm and depletion-mode operation (threshold voltage of -0.38 V). Finally, the common drain current–voltage (*I*–*V*) characteristics for a 25- um gate length device with and without forming gas annealing shown in Fig. 4-10. The drain current I_{ds} increased due to reduced contact resistance at S/D after FGA process. As it is well known that the drawback of MESFET was narrower in the operated gate bias; so that the drain current decreased rapidly at V_g above 2V. The higher the gate bias was, the more the gate leakage was. To solve this problem, we inserted the oxide layer to prevent the issue of a large gate leakage.

4-3-2 Effective channel thickness and depletion width calculation

According to Eq. (4.2), we could estimate the pinch-off voltage ideally,

$$V_{po} = V_{bi} - V_T = (\phi_m - \chi - \phi_n) - V_T \tag{4.2}$$
$$\phi_n = \frac{kT}{q}\ln(\frac{N_C}{N_d})$$

for gold, Φm = 5.2 eV; for GaAs: χ = 4.07 eV ; Φ_{Bn} = 1.13 eV where T = 300 K N_c = 4E17 cm^{-3} N_d = 3E17 cm^{-3}

The doping concentration of channel layer was characterized by SIMS analysis in Fig. 4-11, which was about 4E17 cm^{-3}, close to the extracted value of 1E17 cm^{-3} through capacitance measurements. The ε_r is the dielectric coefficient, ε_0 was dielectric constant, and V_A was the reverse bias. Based on Eq. (4.3)

$$(\frac{1}{C})^2 = \frac{2(V_{bi} + V_A)}{q\varepsilon_s N_d} \qquad d = \frac{\varepsilon A}{C} \tag{4.3}$$

We also could calculate the depletion width easily. Figs. 4-12 (a) and (b) show the concentration dependence under various gate biases and channel layer thickness, which were similar to SIMS results. According to the following equation, Eq. (4.4),

$$a = \{\frac{\mu_n (eN_d)W}{6\varepsilon_s I_{sat} L} . \{1 - 3[1 - (\frac{V_{GS-} V_T}{V_{P0}})] + 2[1 - (\frac{V_{GS-} V_T}{V_{po}})]^{\frac{3}{2}}\}\}^{\frac{-1}{3}} \tag{4.4}$$

We could estimate the effective channel layer thickness , which was about158 A.

$$W = \{\frac{2\varepsilon_S}{qN_d}(V_{bi} - V)\}^{\frac{1}{2}} \tag{4.5}$$

We show the property of MESFET in Table. 4-1

Device	*V_T*	*Measure $I_{d(sat)}$ (mA)*	*Effective Channel Thickness(A)*	*Depletion Width(A)*	*Unknow(A)*	*Calculate ideal $I_{d\ (sat)}$ (mA)*
MES FET	*-0.38*	*0.4*	*(4E17)/74 (6E16)/84*	*(4E17)/394 (6E16)/985*	*~32 ~21*	*3.2 0.18*

Table. 1 The effective channel layer thickness and depletion width were prepared in this study.

(gate length=25um, gate width=100um)

4-3-3 Electrical characteristics of depletion mode GaAs nMOSFET

For lower doping (N_d=6E16cm^{-3}) channel device, a gate length of 10 um and with of 100 um had a saturation current density 0.8 mA/mm (at V_g = -1.5 V and V_d = 2 V) and maximum G_m of~ 1.2 ms/mm. Fig. 4-13 displays the I_d-V_d with and without PDA 600^{o}C in O_2 ambient .We observed that the drain current decreased after PDA process due to the increased gate leakage current. The other possible origin might be attributed to S/D Ohmic contact difference. We also found that the bulk trap window decrease after 600 ^{0}C in O_2 ambient in Fig. 4-14. After thermal process, the oxide trap charges decreased as the Chapter 2 as mentioned before. Here, the smaller saturation current density is correlated to the lower doping concentration and larger specific contact resistance, in other words, the driving current was restricted by S/D ohmic contact. In order to improve this drawback, we selected high

doping channel (N_d=4E17 cm^{-3}) device to enhance its saturation current density. Figs. 4-15(a) and (b) exhibit the GaAs MOSFET with high doping capping layer, we could get smaller specific contact resistance and better DC characteristics. Fig. 4-16(a) and (b) showed I_d-V_d and I_d-V_g characteristics with a gate length of 10 um and gate width of 100 um. As seen, the devices had a saturation current density 16 mA/mm (at V_g = 0V and V_d = 3V) and maximum G_m of~ 12 ms/mm. It was apparent that the saturation current density increased with high doping capping layer. According to Eq-6, we can simple determine threshold voltage for each case [17][18] .

$$V_{th} = V_{fb} - (V_{ox} + V_{semi}) \quad ; \quad V_{fb} \sim V\,(@G_m\ max) \tag{4.6}$$

$$V_{ox} = \frac{Q_d}{C_{OX}} = \frac{qN_d X_c}{C_{OX}} \qquad V_{semi} = \frac{x_C^2 qN_D}{2\varepsilon_{GaAs}}$$

Epi layer thickness and doping concentration play two important roles to affect nMOSFET operation. For the highest doping channel layer, the threshold voltage was too large to fully shut off. The possible reason was attributed to large gate leakage for F-N tunneling, as shown in Fig. 4-17(a). For the lowest doping channel layer in Fig. 4-17(b), the threshold voltage was adjusted at -3.5 V, but the large specific contact resistance limited the saturation current, which affects the cut-off frequency (f_T) in power IC. In our case, we choose high doping concentration for source and drain to reduce the contact resistance and lower doping channel concentration to define V_{th} in small gate bias region. We did a count to calculate Al_2O_3 physical thickness in Fig. 4-18; the roughness of without capping layer etching was smaller

than with wet etching. However, the surface roughness was the serious problem, resulting in the degradation of surface electron mobility. To solve this problem, we eliminated etching rate to 6.5 Å/s and used the sulfur passivation to improve surface quality [19]. At first, Fig. 4-19 (a) and (b) display the I_d-Vg and I_d-V_d curves without sulfur passivation. We found that the drain current I_d cannot be fully shut off. For gate biases (V_g) less than -5 V, I_d is independent of gate of gate bias, indicating that I_d had two components: one was the channel current (I_{dc}) component that can be modulated by the gate bias and the other one is leakage current (I_{dl}) component that was independent of gate bias. The value of the leakage current I_{dl} was equal to the I_d value at V_g = -5 V. We suggested that the high doping layer was not fully removed, resulting in a quite high subthreshold swing of 1030 mV/decade. The possible reasons for a large subthreshold swing include a large D_{it}, small C_{ox} (thick dielectric layer), and large depletion layer capacitance C_d (small depletion layer thickness) [20]. The maximum transconductance was 55 mS/mm. In order to dissolve the problem, we used $(NH_4)_2S$ sulfur with different solutions to decrease D_{it}. Fig. 4-20(a) and (b) show the I_d-V_g, I_d-V_d characteristics with $(NH_4)_2S$+C_4H_9OH surface passivation, respectively. We suggested the D_{it} value decreased, so that the subthreshold swing was improved. To substantiate this suggestion, we used single frequency method to calculate interface density (D_{it}) the *C-V* dispersion and Fermi-level pinned were improved with surface sulfur passiviation, as we mentioned in Chapter 2. The D_{it} value was decreased from 4.5E13 to 2.53E13 cm^2eV^{-1}. In this study we

also showed DC characteristics after different surface treatments such as $(NH_4)_2S+H_2O$, $(NH_4)_2S+C_4H_9OH$; no obvious differences between two solutions were characterized. Field effective mobility of GaAs MOSFET was extracted from $I_d - V_{gs}$ data shown in Fig. 4-21. The peak electron mobility of 460 $cm^2V^{-1}S^{-1}$ has been obtained in this study, however, this value was still far below GaAs bulk mobility ~ 8500 $cm^2V^{-1}S^{-1}$. This mobility degradation could be probably attributed to the Coulomb scattering induced by the interfacial traps and bulk traps. Figure 4-22 displays the cross-sectional HRTEM image of 120 cycles Al_2O_3 film on GaAs substrate with surface sulfur passiviation. A uniform, continuous, and amorphous Al_2O_3 film was observed, and its thickness was about 11 nm. The interface between Al_2O_3 and GaAs substrate was clear, and we could observe interfacial layer on GaAs surface. Fig. 4-23 compared the normalized transconductance of MESFET and MOSFET. The transfer curve of MOSFET was wide than that of MESFET, which means the MOSFET can be operated in a wilder gate voltage-bias region.

4-4 Summary

By using MBE system, we have grown superior III-V epi layer and also succeeded in demonstrating on both MESFET and MOSFET through the standard 3 mask processes. In this chapter we presented all the electrical performances and extracted device parameters for those GaAs FET with different channel doping concentration and device structures. By analyzing

the $I_d - V_g$ and $I_d - V_d$ electrical characteristics and extracting those parameters such as V_{th} , S.S. Pc,, and μ_{FE} , we have the ideal about what would happen and should be paid heed to when deal with such a nasty substrate material. For our cases, we used different surface treatments to eliminate native oxide formation. It should be better to continue improving Fermi-level pinning for realization of an acceptable transistor. We will further fabricate the enhanced-mode GaAs MOSFET based on the experience of the depletion-mode GaAs MOSFET.

References

[1] M. Hong, J. P. Mannaerts, J. E. Bowers, J. Kwo, M. Passlack, W.-Y Hwang, and L. W. Tu: J. Cryst. Growth 175 (1997) 422.

[2] M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent Science 283 (1999) 1897.

[3] Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk: Appl. Phys. Lett. 88 L. Gossmann, J. P(2006) 263518.

[4] N. Goel, P. Majhi, C. O. Chui, W. Tsai, D. Choi, and J. S. Harris: Appl. Phys. Lett. 89 (2006) 163517

[5] S. Koveshnikov, W. Tsai, I. Ok, J. C. Lee, V. Torkanov, M. Yakimov84 (2004) 434. and S. Oktyabrsky: Appl. Phys. Lett. 88 (2006) 022106. Appl. Phys. Lett. 87

[6] N. Yokoyama, T. Mimura, and M. Fukuta: IEEE Trans. Electron Devices 27 (1980) 1124

[7] M. Hong, J. N. Baillargeon, J. Kwo, J. P. Mannaerts, and A. Y. Cho: Proc. 2000 IEEE Int. Symp. Compound Semiconductors, 2000, p. 345.

[8] J. Robertson and B. Falabretti: J. Appl. Phys. 100 (2006) 014111.

[9] C. P. Chen, Y. J. Lee, Y. C. Chang, Z. K. Yang, M. Hong, J. Kwo, H. Y. Lee, and T. S. Lay: J. Appl. Phys. 100 (2006) 104502.

[10] Y. C. Wang, M. Hong, J. M. Kuo, J. P. Mannaerts, J. Kwo, H. S. Tsai, Vac. Sci. Technol. B 16 (1998)

[11] J. K. Yang and H. H. Park: Appl. Phys. Lett. 87 (2005) 022104.

[12] J. K. Yang and H. H. Park: Appl. Phys. Lett. 87 (2005) 202102.

[13] J. Robertson and B. Falabretti: J. Appl. Phys. 100 (2006) 014111.

J. Krajewski, Y. K. Chen, and A. Y. Cho: IEEE Electron Device Lett. 20 (1999) 457.

[14] M. L. Huang, Y. C. Chang, C. H. Chang, T. D. Lin, J. Kwo, T. B. Wu, and M. Hong: Appl. Phys. Lett. 89 (2006) 012903.

[15] J. Y. Wu, H. H. Wang, Y. H. Wang, and M. P. Houng: IEEE Trans. Electron Devices 48 (2001) 634

[16] E. F. Yu, J. Shen, M. Walther, T. C. Lee, and R. Zhang: Electron. Lett. 36 (2000) 359

[17] K. Yamaguchi and S. Takahashi: IEEE Trans. Electron Devices 28

[18] M. Hong, Z. H. Lu, J. Kwo, A. R. Kortan, J. P. Mannaerts, J. J. Krajewski, K. C. Hsieh, L. J. Chou, and K. Y. Cheng: Appl. Phys. Lett.

[19] B. Yang, P. D. Ye, J. Kwo, M. R. Frei, H.-J. L. Gossmann, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude: 2002 GaAs IC Symp., 2002, p. 139

[20] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts,J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, Enhancement-mode p-channel GaAs MOSFETs on semi-insulating substrates," IEDM Tech

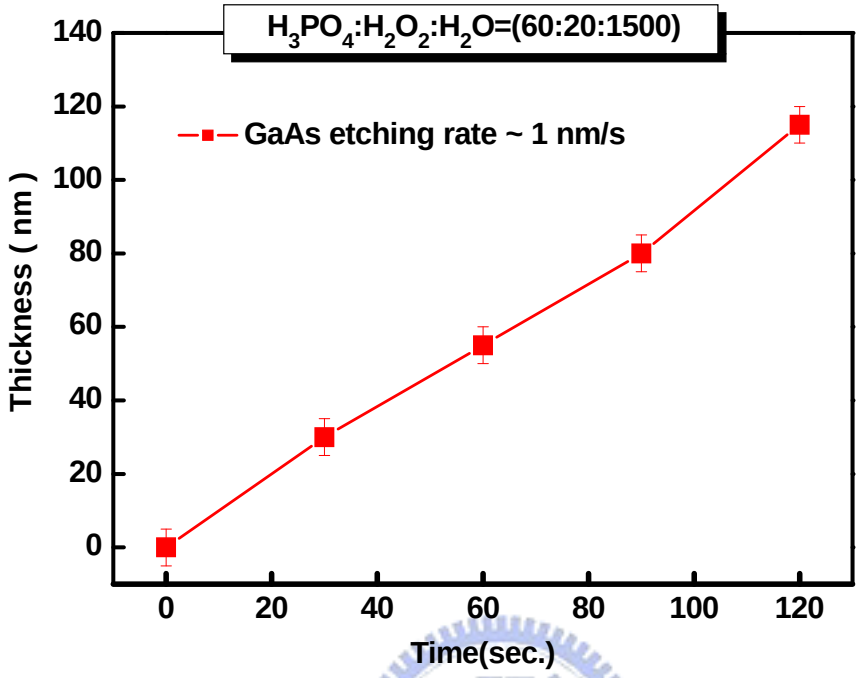


Fig.4-1 Wet etching rate as a function of etching times for GaAs substrate

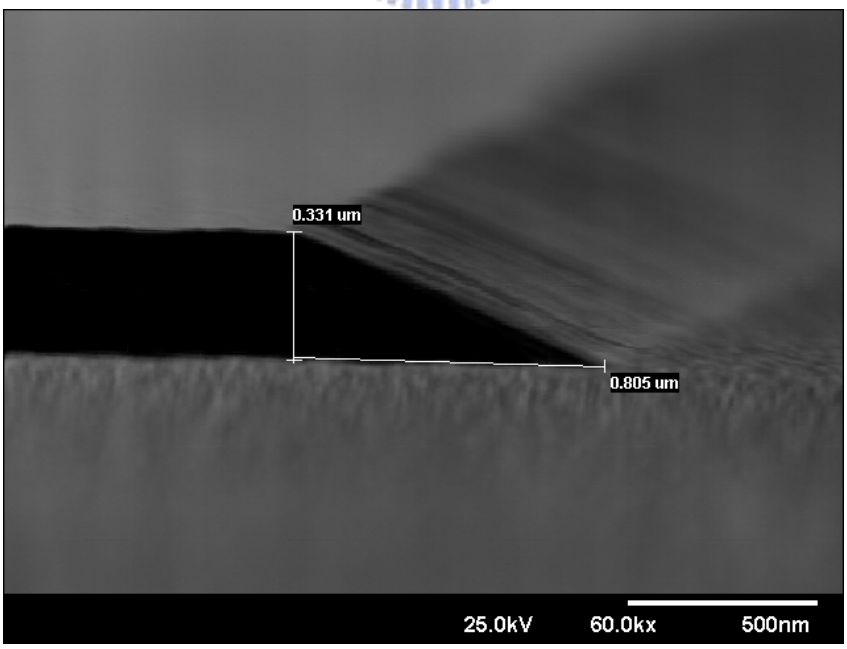


Fig.4-2 The Scanning electron microscope of Mesa etching isolation

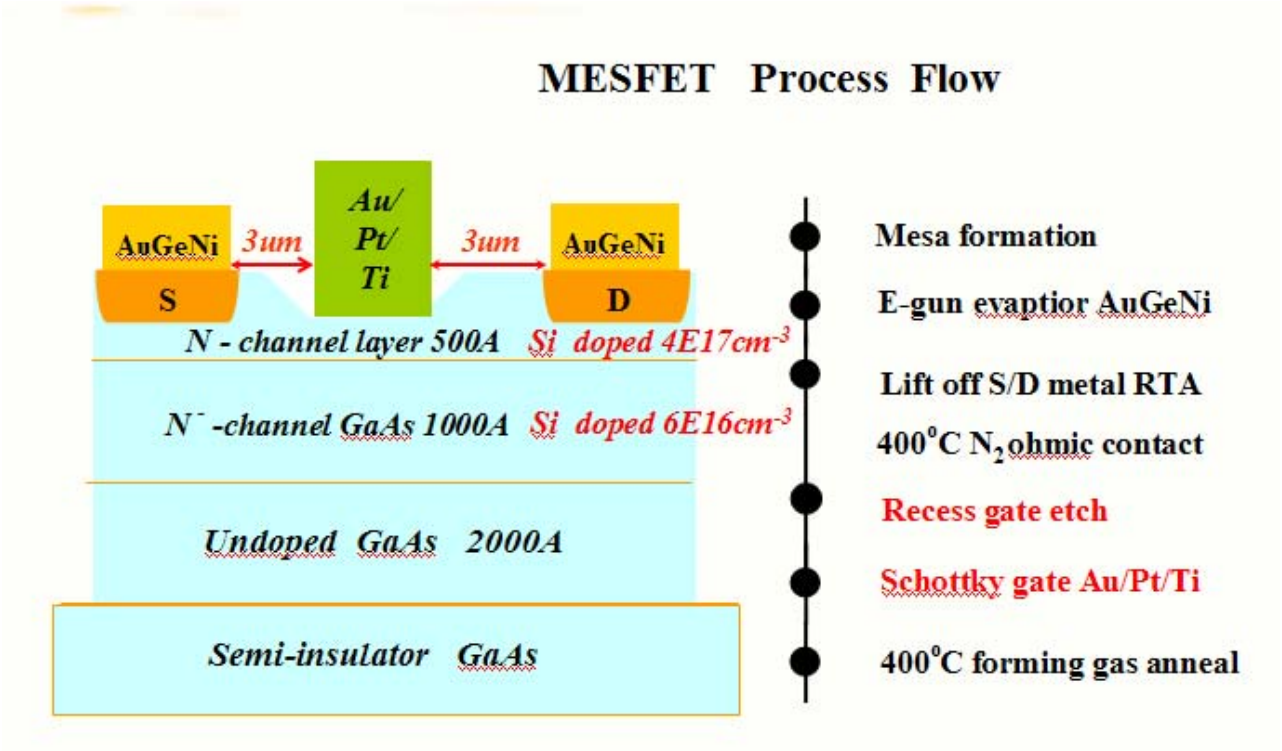


Fig. 4-3 Fabricated GaAs MESFET process flow

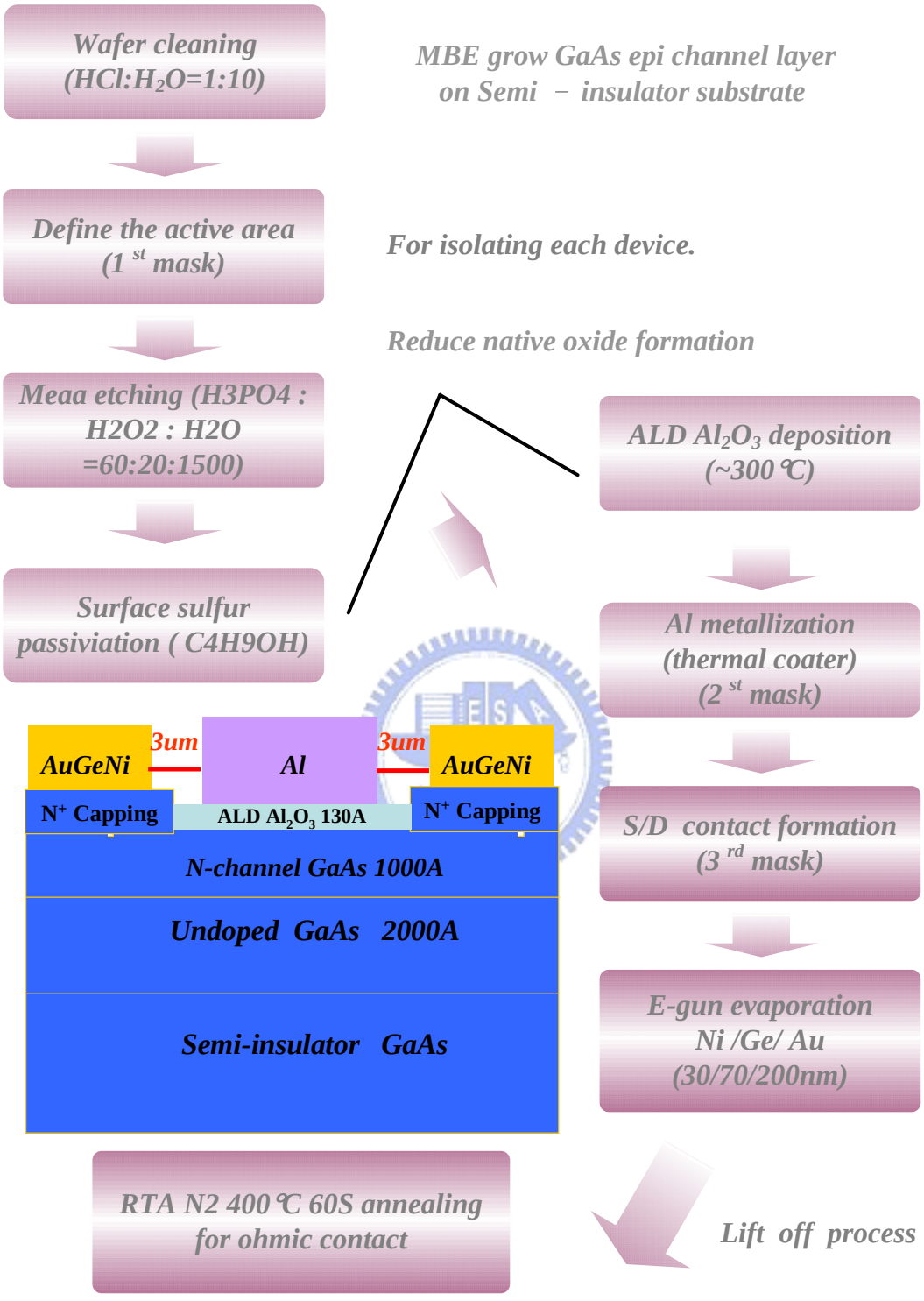


Fig. 4-4 Fabricated GaAs MOSFET process flow

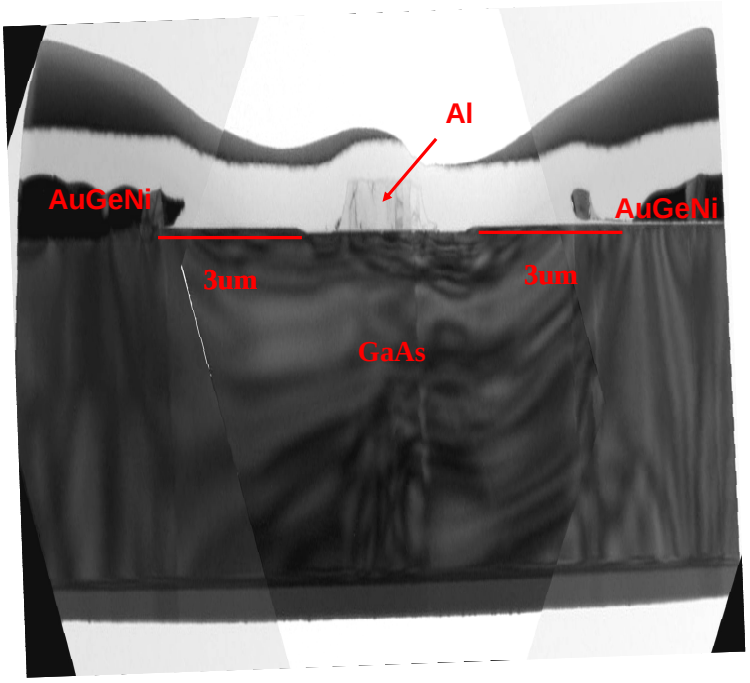


Fig. 4-5 The HRTEM images of GaAs Metal-Oxide-Semiconductor Field Effect Transistor

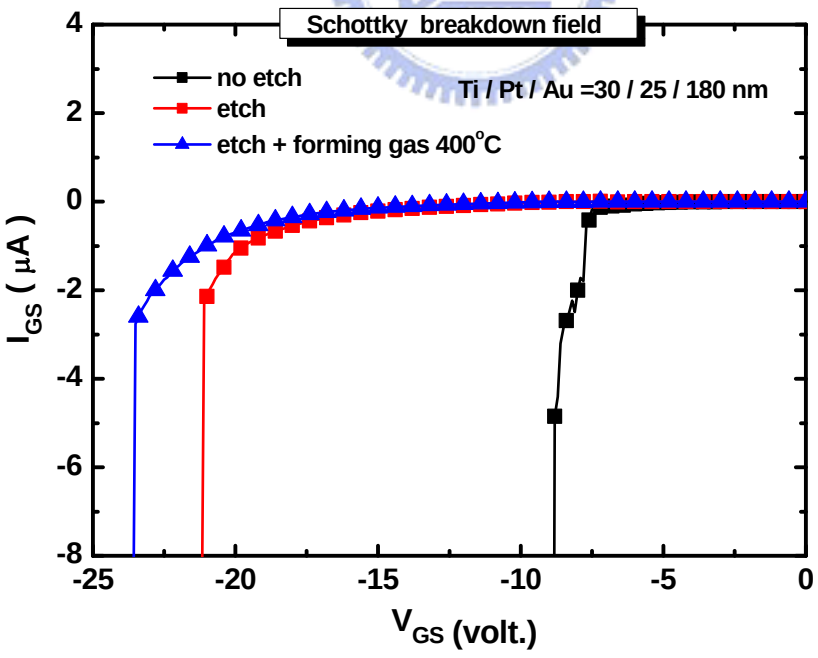


Fig 4-6. Schottky breakdown field as function of gate bias with and with not treatments

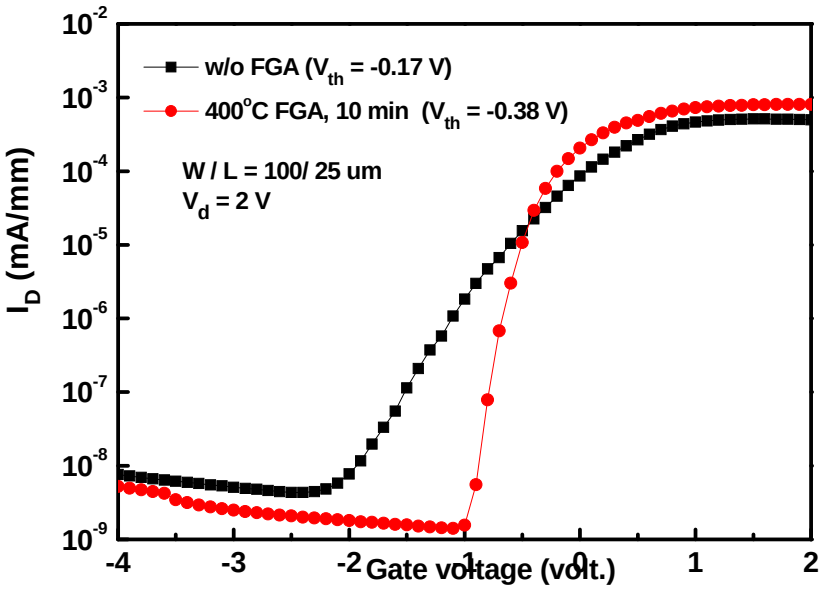


Fig. 4-7 (a) Drain current versus drain bias as a function of gate bias for a 25um x100 um MESFET

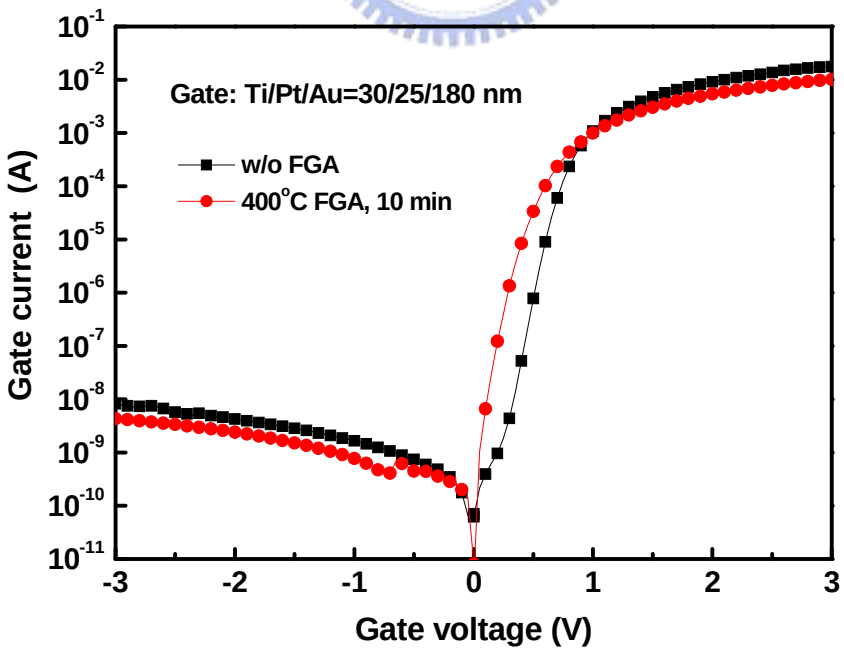


Fig. 4-7 (b) Schottky characteristics with and without 400°C 10 min forming gas annealing

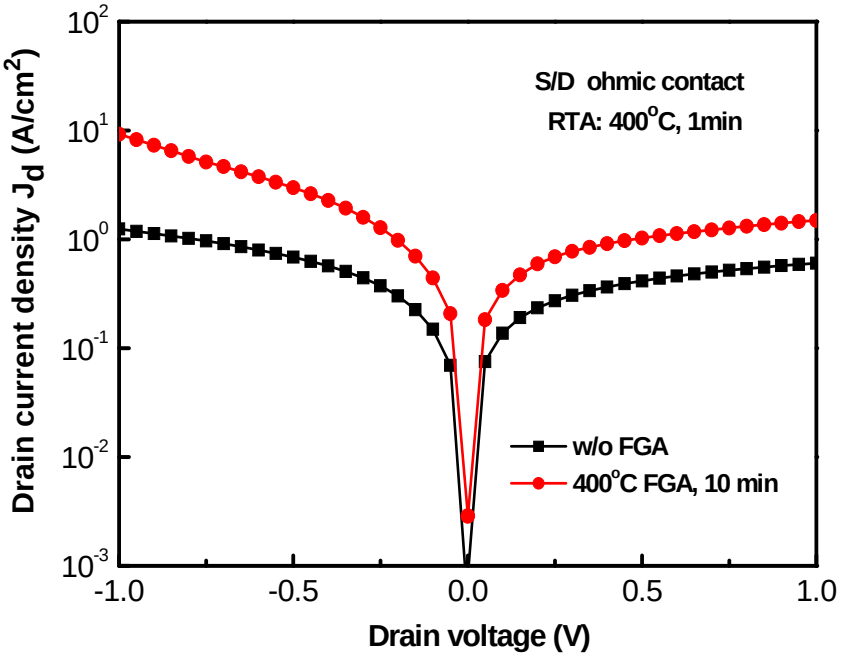


Fig.4-8. S/D ohmic contact with and with not 400°C 10 min forming gas annealing

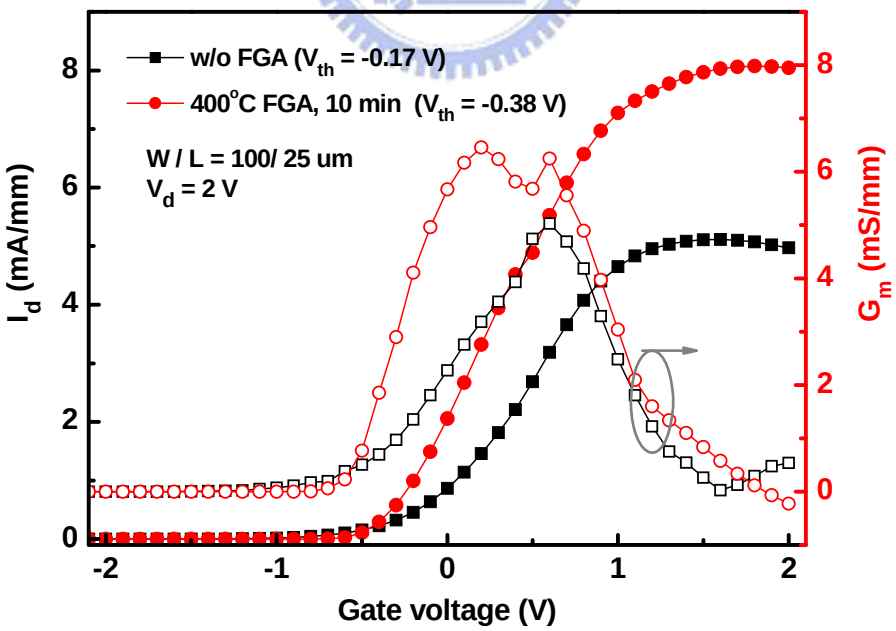


Fig. 4-9 Drain current and transconductance versus gate bias as a function of gate bias for a 25um x100 um MESFET.

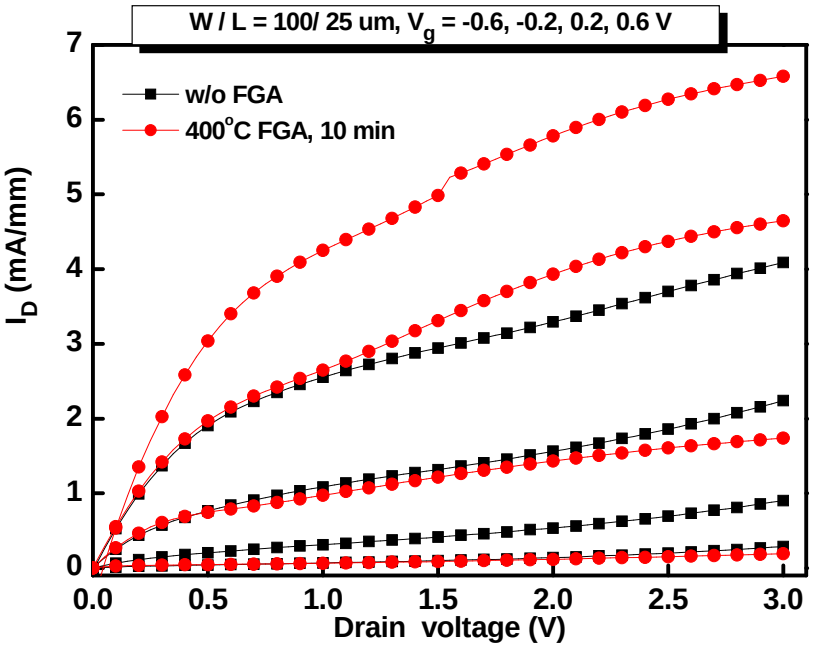
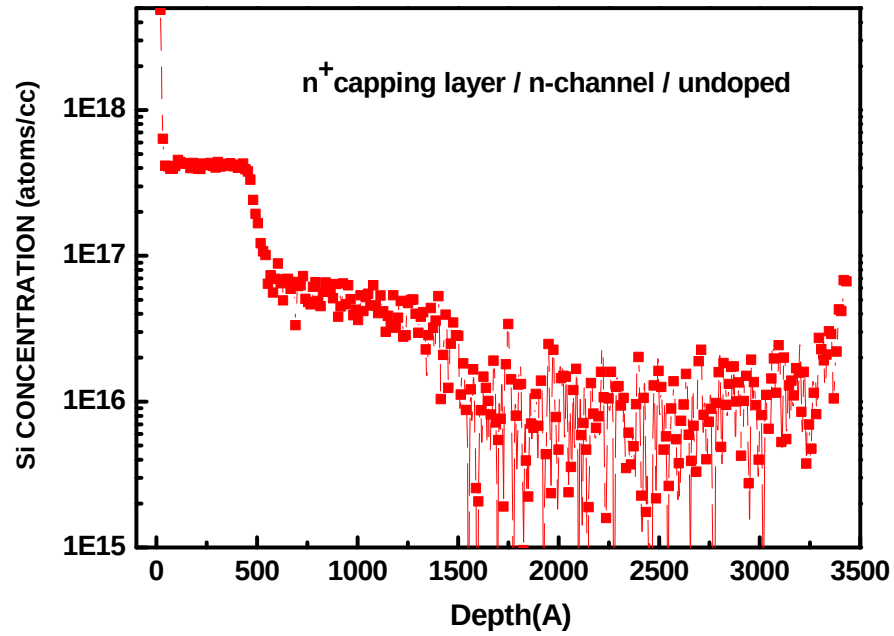
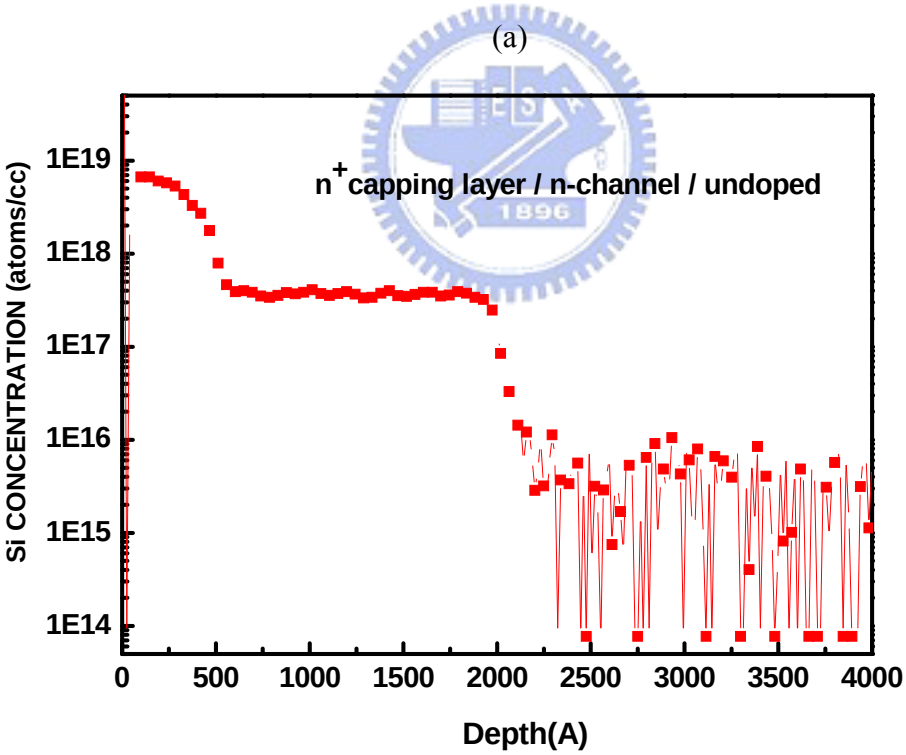


Fig. 4-10 Drain current versus drain bias as a function of drain bias for a 25um x100um MESFET with and without forming gas annealing.

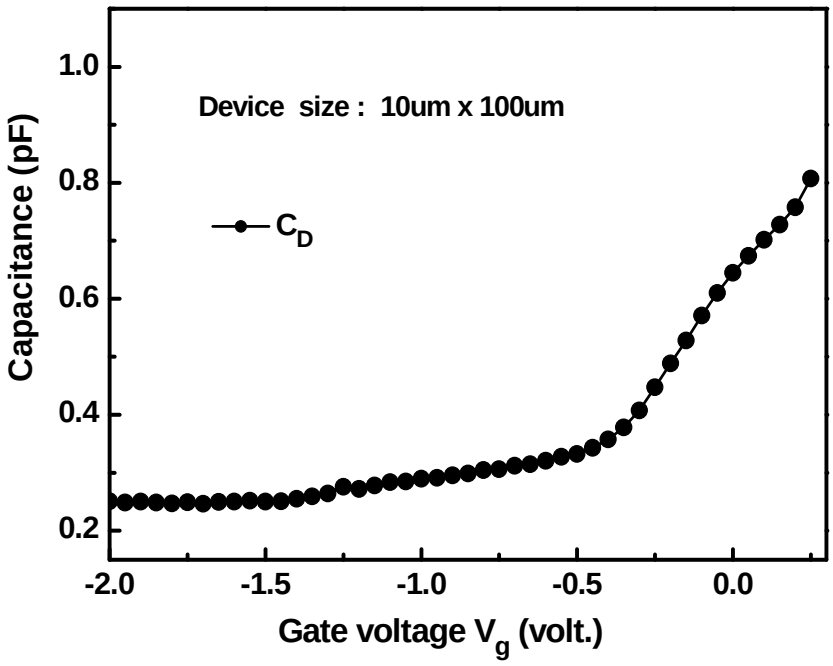


(a)

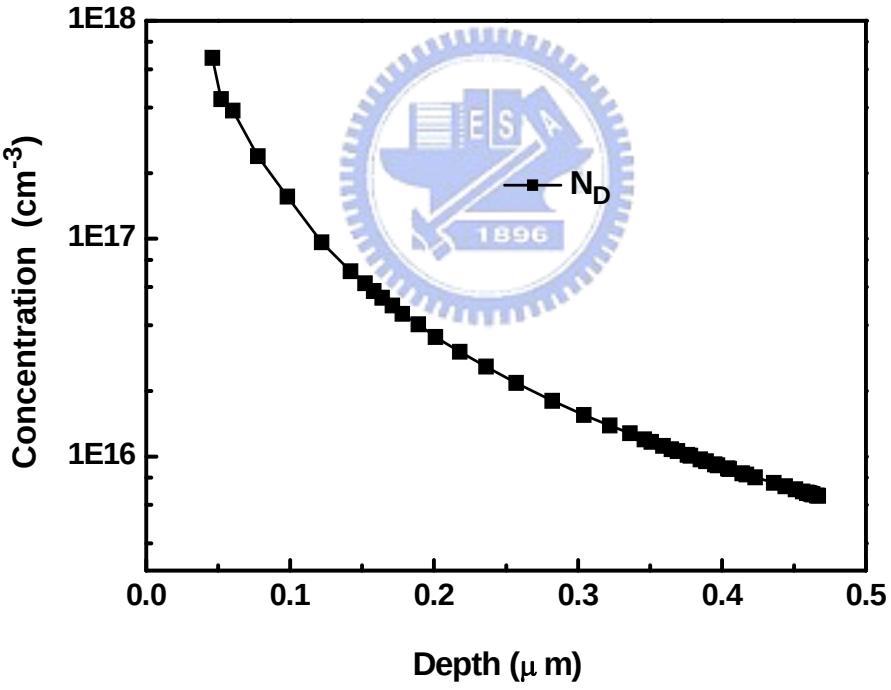


(b)

Fig. 4-11 SIMS analysis for (a) lower doping (b) high doping GaAs channel was grown semi-insulator substrate



(a)



(b)

Fig. 4-12 (a) The capacitance as a function of reverse gate bias with 10umX100um

(b) The measure channel concentration as a function of depletion width

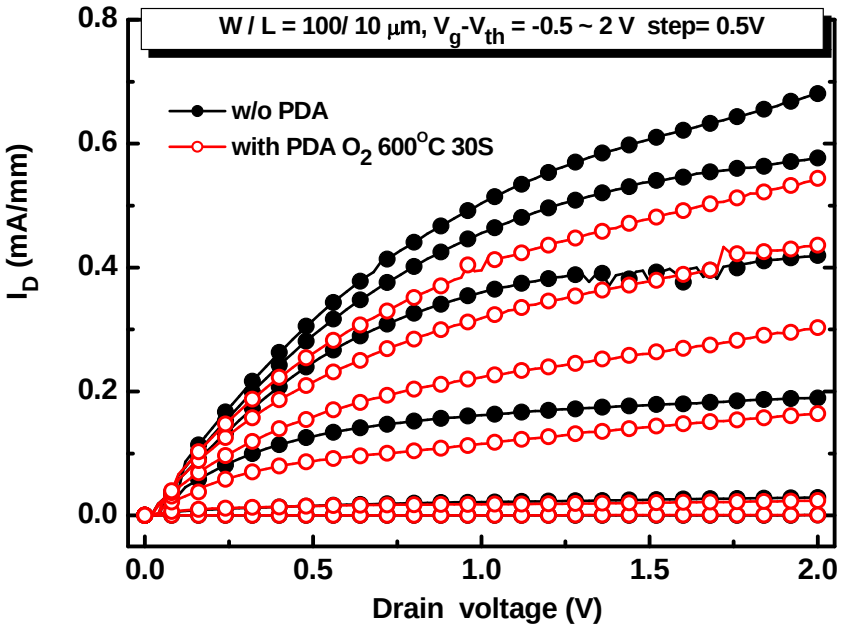


Fig. 4-13 Drain current density as a function of drain voltage with and without 600°C annealing

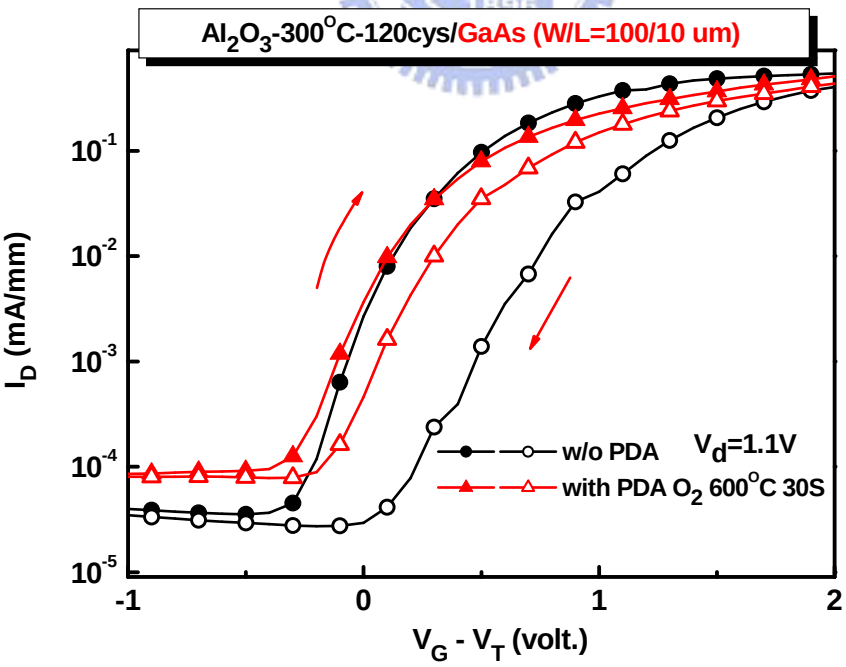
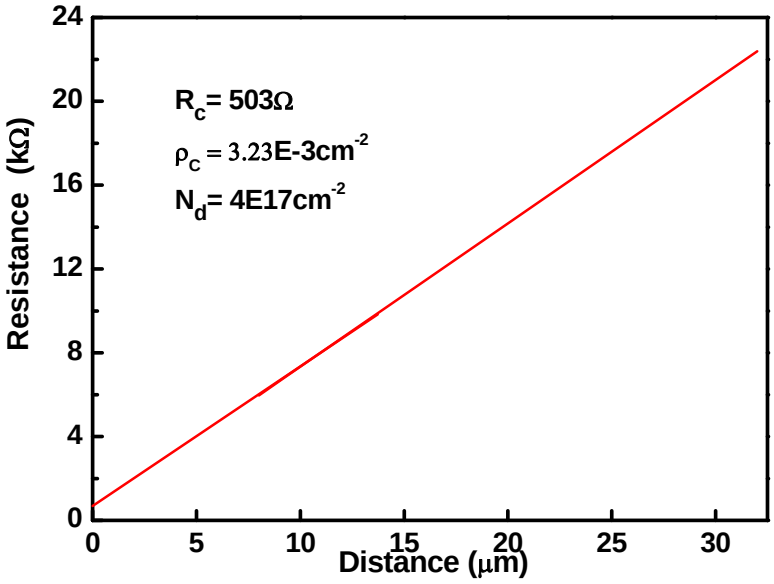
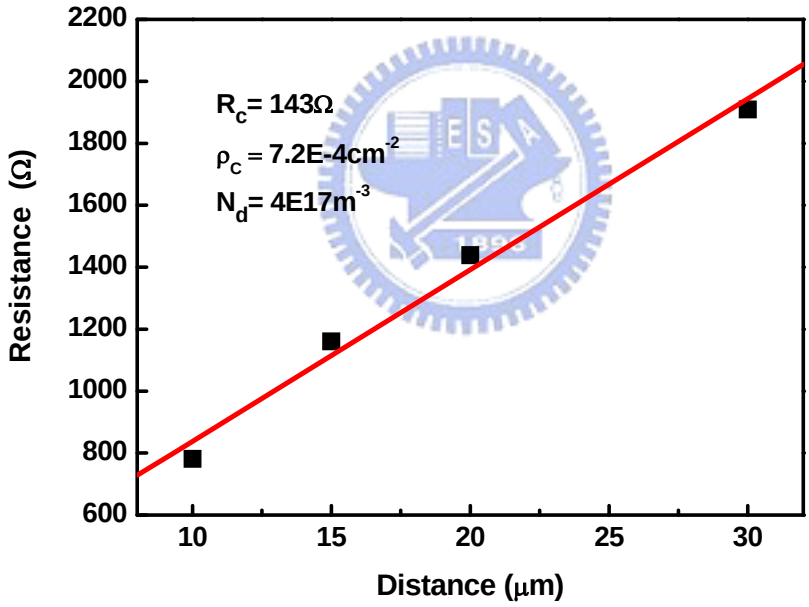


Fig. 4-14 The trapping window with and without 600°C annealing in O_2 ambient



(a)



(b)

Fig. 4-15. Characteristics of the specific contact resistance (a) without and (b)with high doping capping layer.

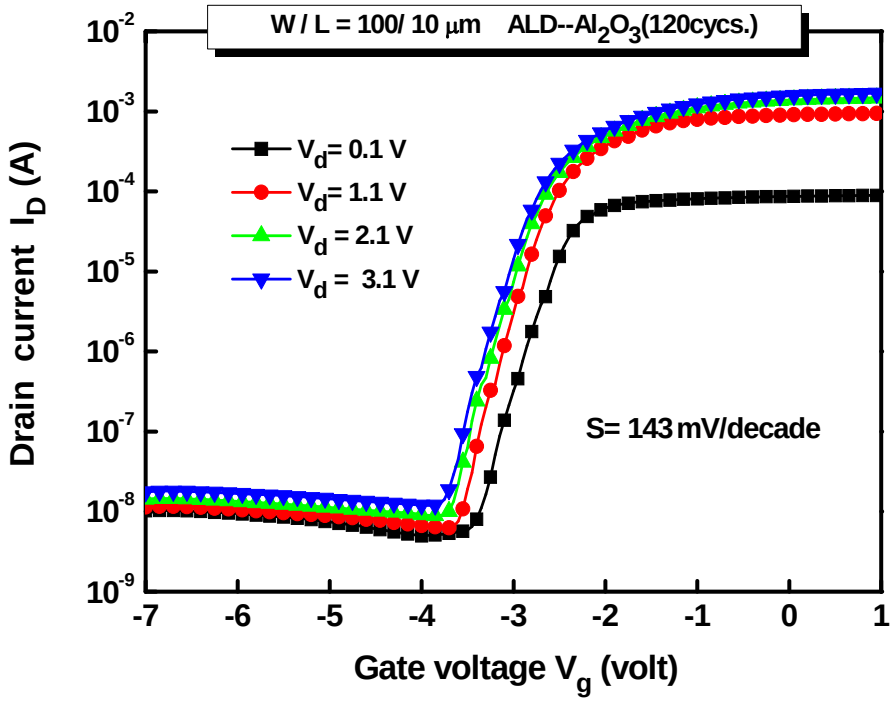


Fig. 4-16 (a) Drain current as a function of gate bias with doping layer (N_d=4E17cm^{-3})

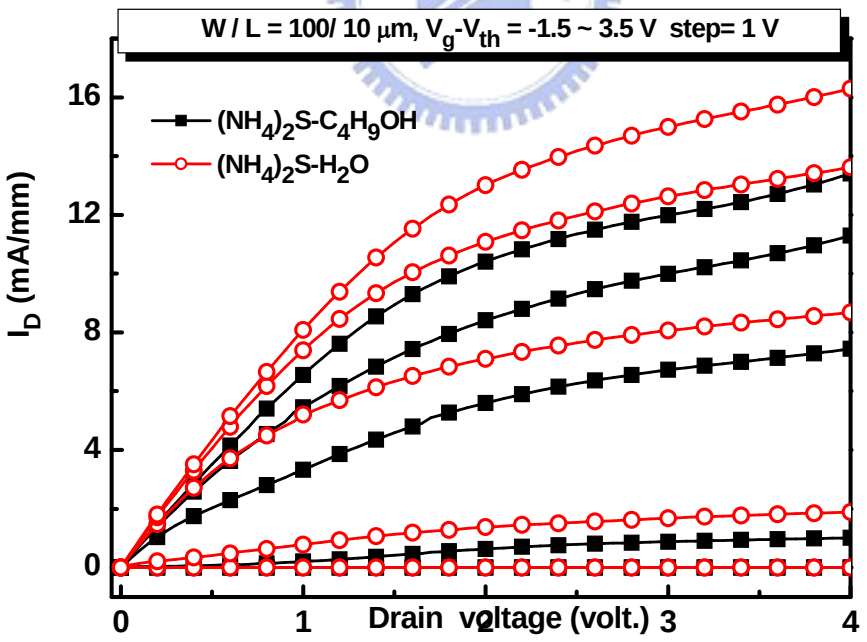


Fig. 4-16 (b) Drain current as a function of drain bias with sulfur passivation

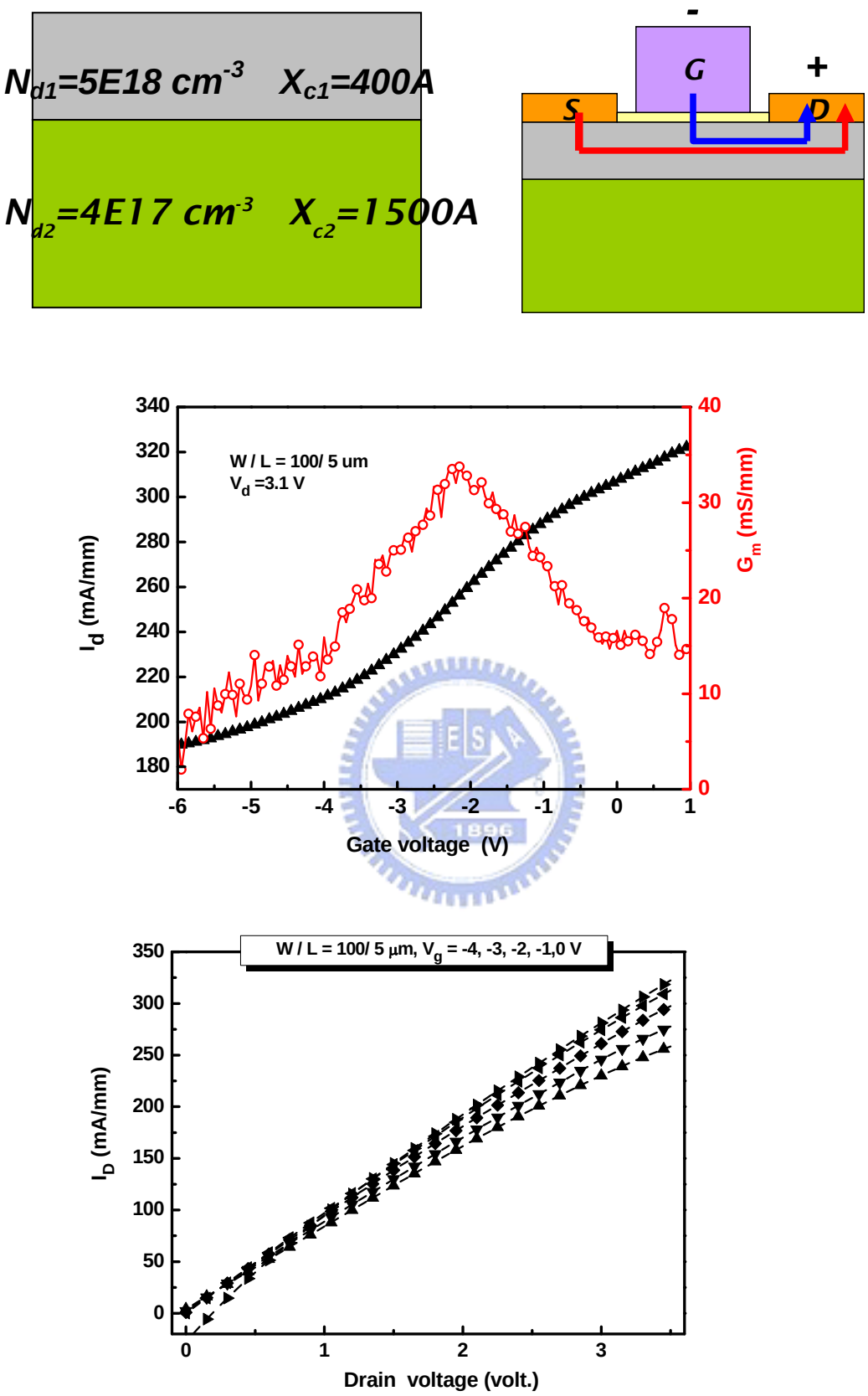


Fig.4-17 (a) Case I(N_d=5E18cm^{-3}) for (a) I_d-V_g (b) I_d-V_d DC electric characteristics

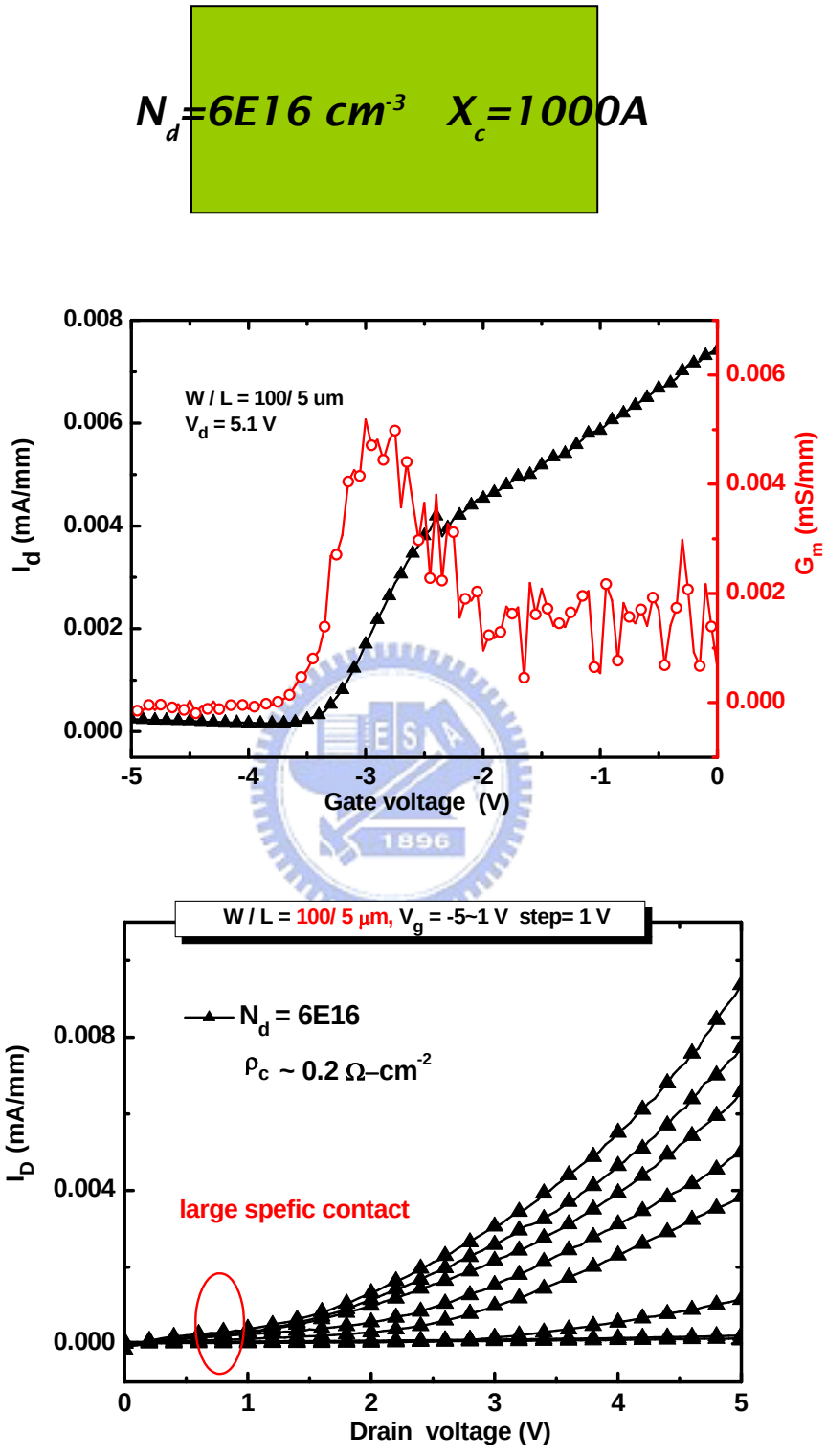


Fig.4-17(b) Case II (N_d=6E16cm^{-3}) for (a) I_d-V_g (b) I_d-V_d DC electric characteristics

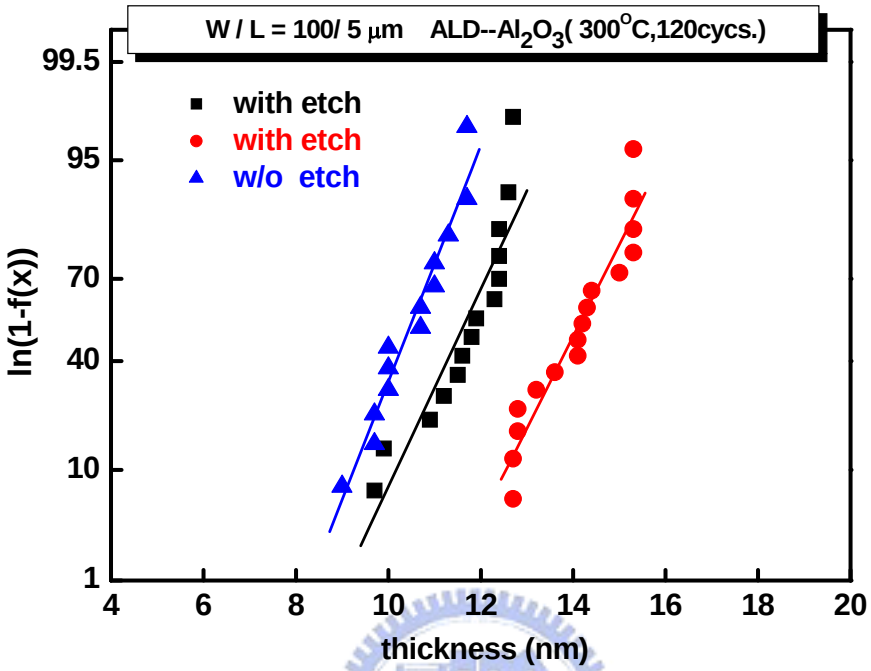


Fig.4-18 Weibull distribution of Al_2O_3 physical thickness with and without gate etching

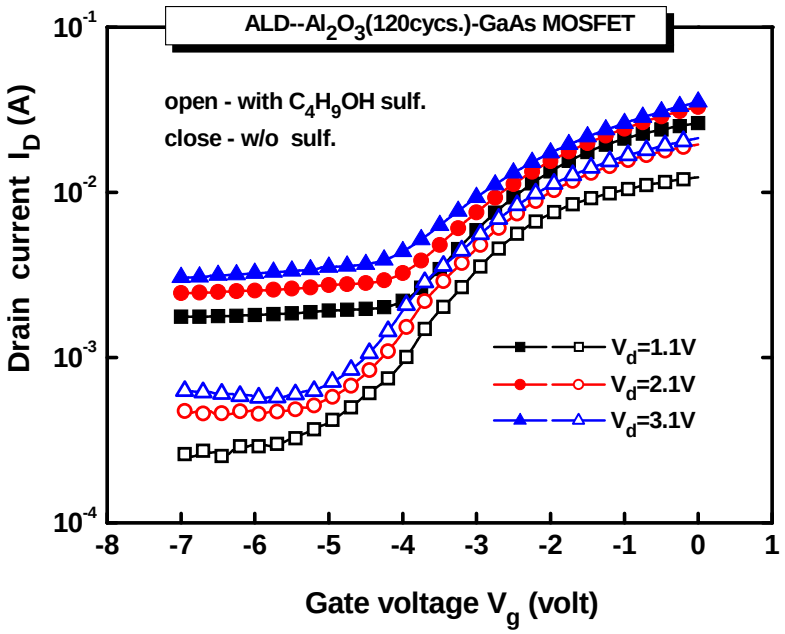


Fig. 4-19 (a) Drain current as a function of gate bias with and without $(NH_4)_2S+C_4H_9OH$ surface passivation.

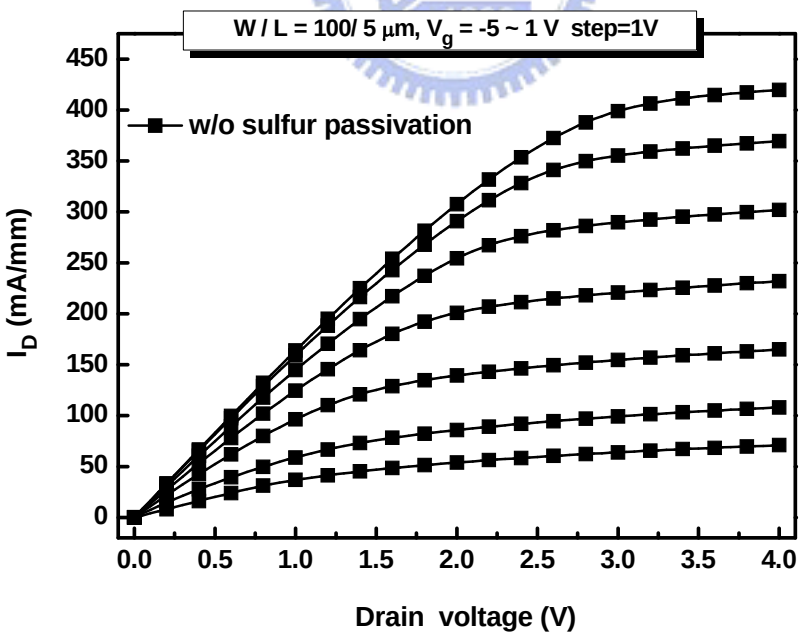
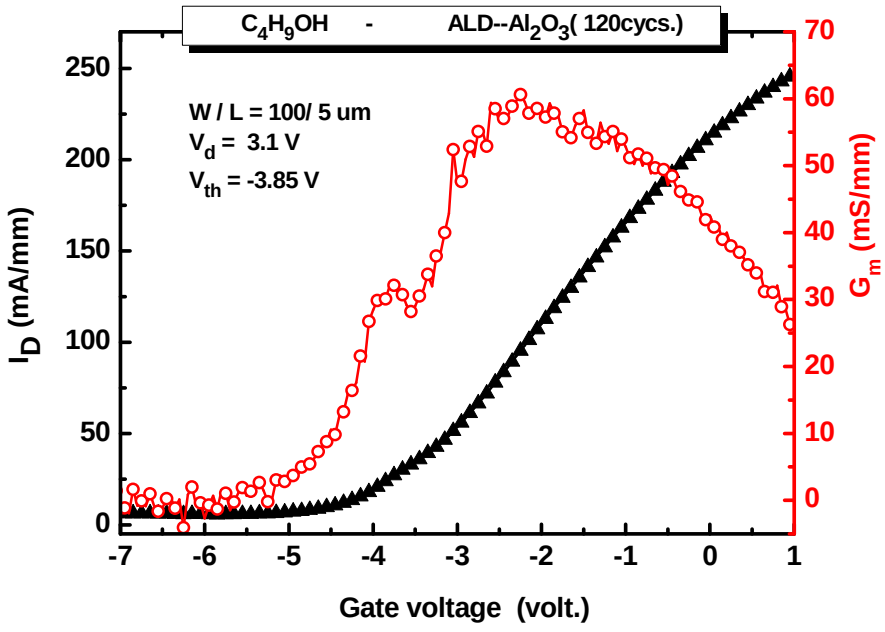
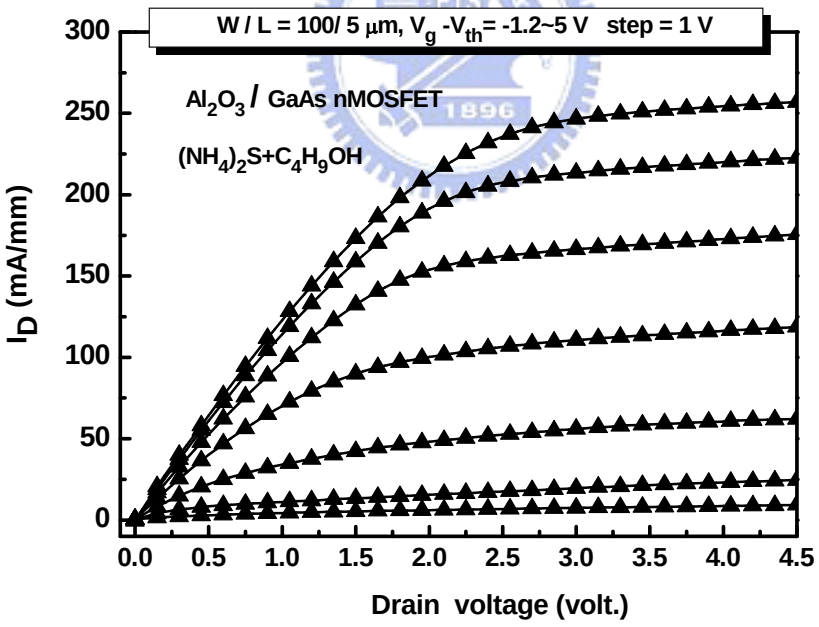


Fig. 4-19 (b) Drain current as a function of drain bias without surface passivation.



(a)



(b)

Fig.4-20 (a) I_d-Vg (b) I_d-V_d electronic characteristics with $(NH_4)_2S+C_4H_9OH$ surface treatment

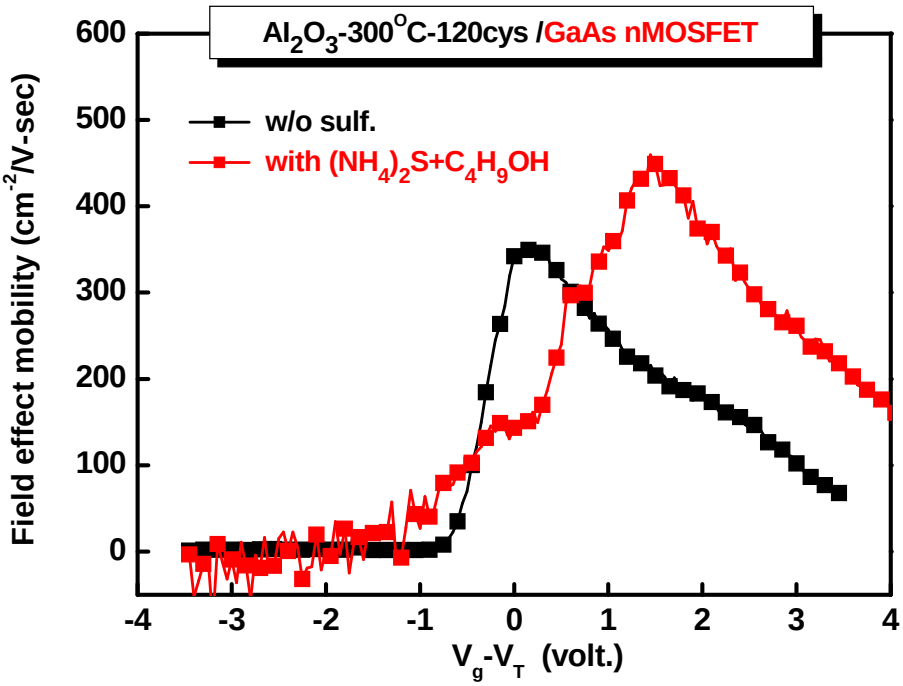


Fig.4-21 The peak of electron mobility we extract with and without sulfur passuvation

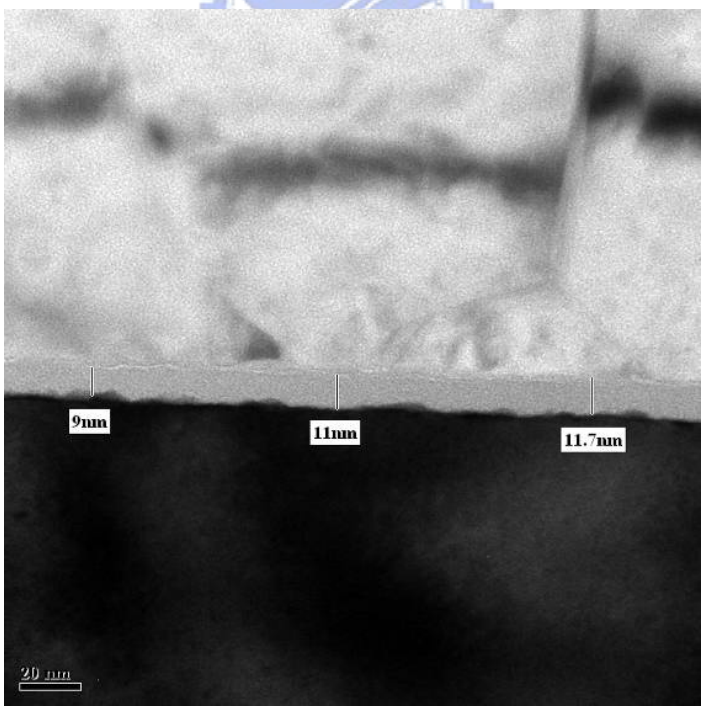


Fig. 4-22 The HRTEM images of Al_2O_3 film by ALD 120 cycles on GaAs MOSFET

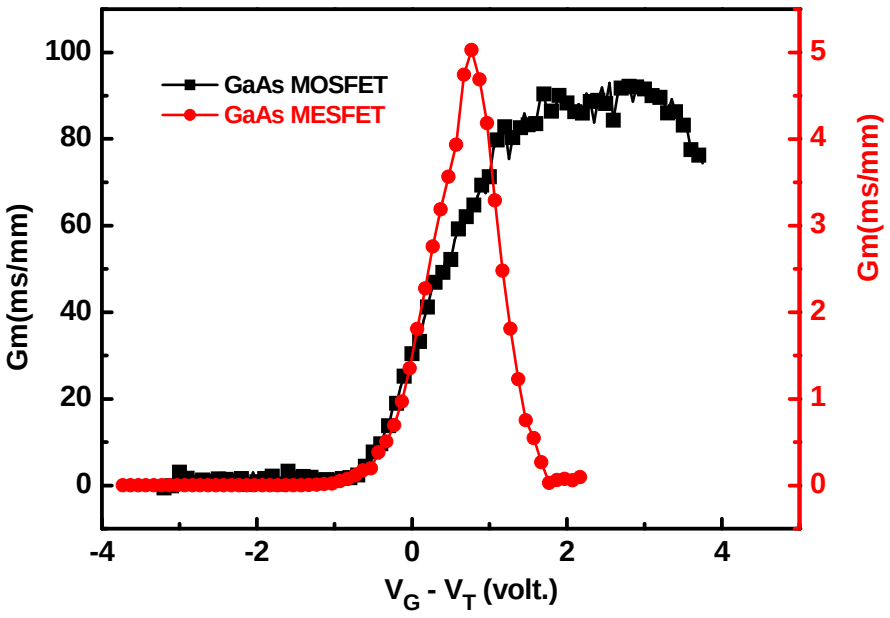


Fig 4-23. The transconductance as a function of V_g-V_t for GaAs MESFET and MOSFET

Chapter 5

Conclusions and Suggestions

Conclusions

Firstly, the flatness of the GaAs surface was needed, but the thermal stable surface is more important. The optimized surface roughness was about 0.238 nm after the NH_4OH/DIW and $(NH_4)_2S$+C_4H_9OH at 60 °C. From the XPS examination, it shows that the growth of native oxide on GaAs surface still exists. This diluted sulfur-solution really suppresses the GaAs oxides, and increases sulfur temperature to bond strongly. The 60 °C sulfur solution increases Ga-S bond when NH_4OH cleaned GaAs surface is used.

Next, the specific contact resistivity was decrease when we increase substrate doping concentration. The optimized specific contact resistivity we extracted was about 2E-5 Ω-cm^2. The interface between metal and GaAs was smooth due to form Ni-Ge. Surface roughness was still a serious problem in our study.

Finally, we had fabricated GaAs MOSFET and MESFET on semi-insulator substrate. The electronic mobility was not good enough because of rough surface and heavy doping channel layer. We believed that the continuous optimization of the surface treatment through process modification is expected to further improve the electrical performance of oxide/GaAs, which thus be considered as a promising gate dielectric of GaAs MOSFET.

Future Work

Order to diminish the cost, we must to grow III-V on Si substrate. Here we used Si-Ge buffer layer to relax strain and eliminate dislocation. The process will describe as follow:

Deposition high quality Ge buffer layer on Si substrate —because lattice constant of GaAs matches with Ge. we must have good Ge buffer layer, then growth high quality GaAs. We use Ultra High Vacuum Chemical vapor phase deposition system (UHVCVD) growth $Si_{1-x}Ge_x$ (x=0.9) as the bottom layer, and use the high-vacuum in-situ annealing, and continue to growth $Si_{1-x}Ge_x$ (x=0.95) as the modulation layer, follow high-vacuum in-situ annealing, which is in order to limit the dislocation under the bottom layer, finally, deposite the pure Ge buffer layer, structure is the Fig. 5-1. From Fig. 5-2, we can observe obviously that low dislocation exist in this structure.

We also did the Pt/Al_2O_3/epi-GaAsMOSCAP in this substrate. The C-V and I-V characteristics were shown in Fig. 5-3(a)~(e) and Fig. 5-4, respectively. The surface morphology and Hall measurement were shown in Fig.5-5 and Table 5-1, respectively. Although it has many problem to improve and solve, but we still considered this structure will be a trend of CMOS in the future.

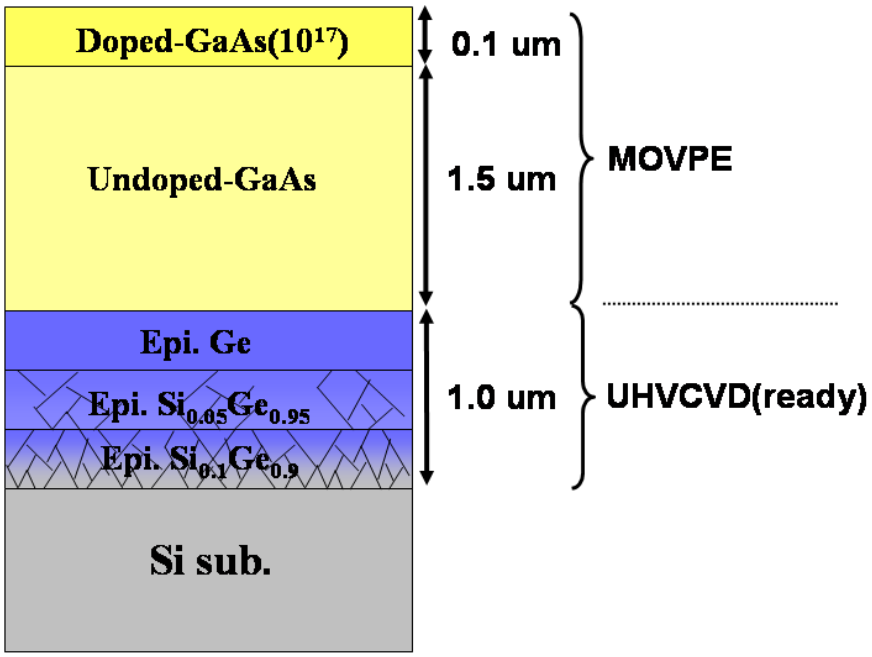


Fig. 5-1 The structure of growing GaAs on Si substrate with SiGe buffer layer

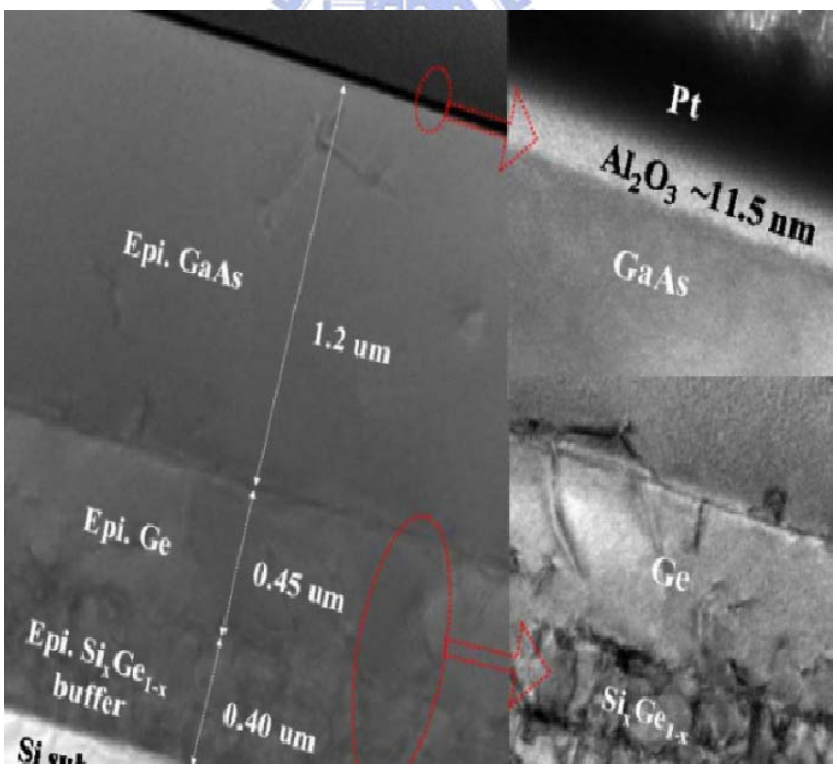


Fig. 5-2 The HRTEM image of growing GaAs on Si substrate with Ge buffer layer

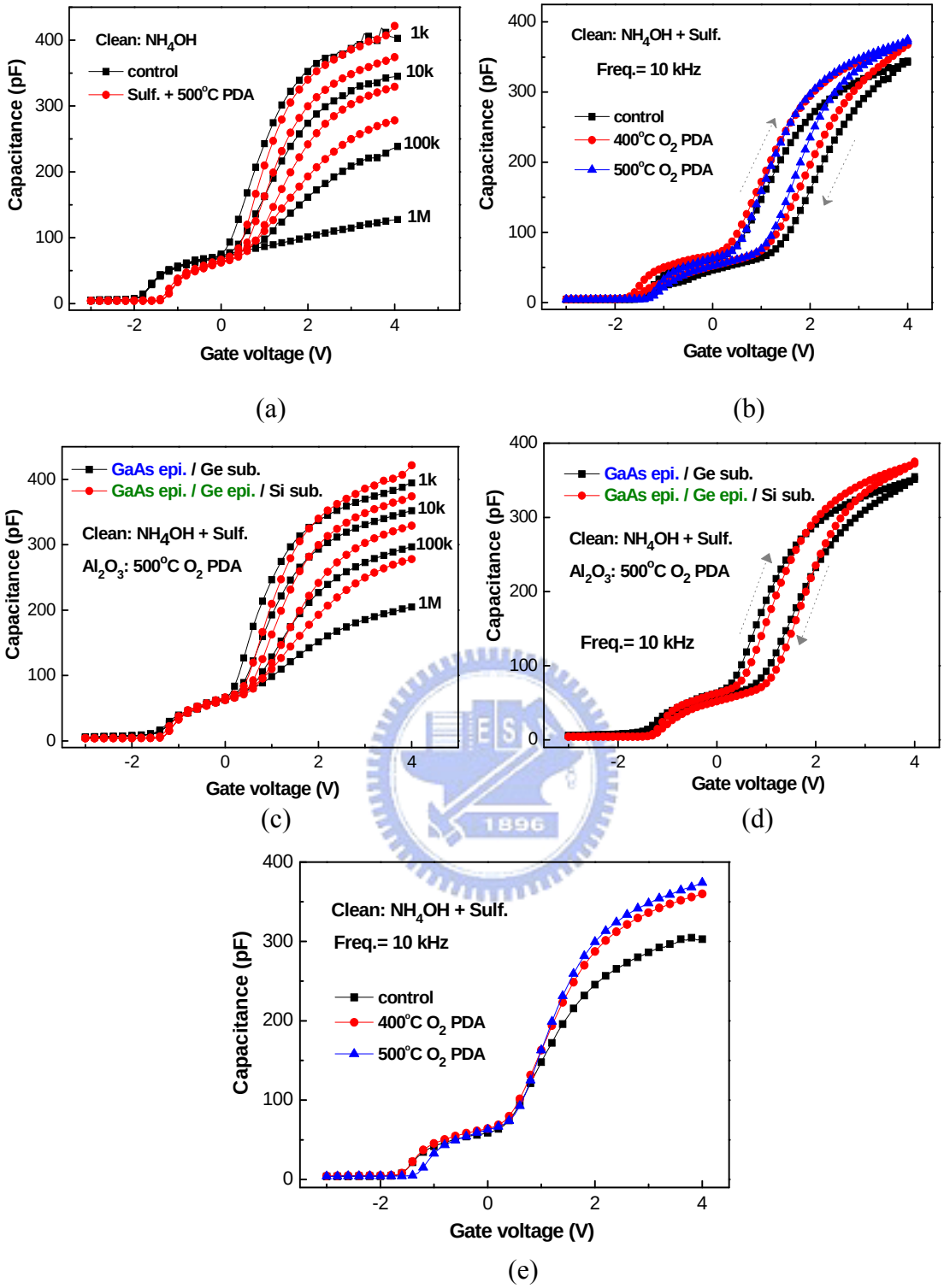


Fig. 5-3 The C-V characteristics of Pt/Al_2O_3/epi-GaAs (a)with and without sulf.+PDA(b) Hysteresis of 10kHz frequency of MOS capacitors with different annealing temperature(c)Multi-frequency (d) Hysteresis with two epi substrate (i) Si (ii) Ge (e) The capacitance of 10kHz frequency of Pt/Al_2O_3/epi-GaAs with different annealing

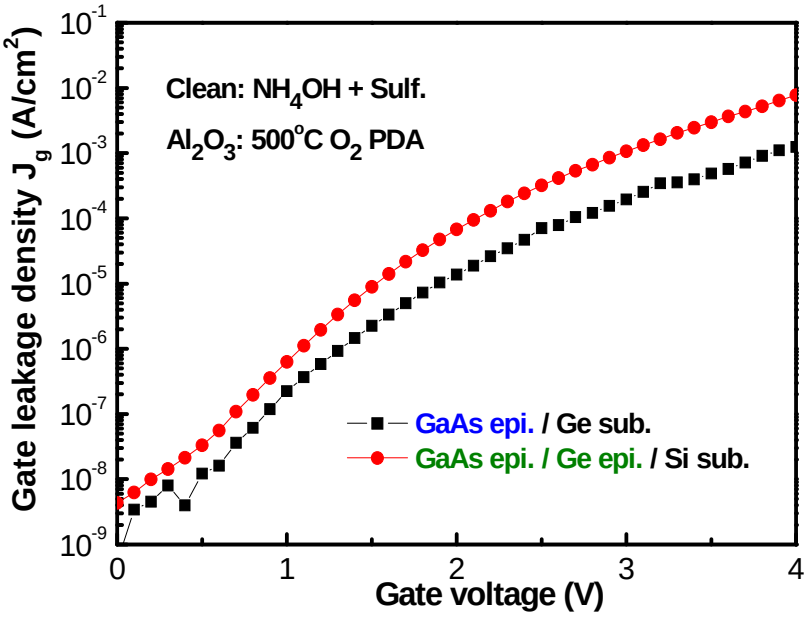


Fig. 5-4 The leakage current with two different epi substrate (i) GaAs/Ge sub. (ii) GaAs/Ge/Si sub.

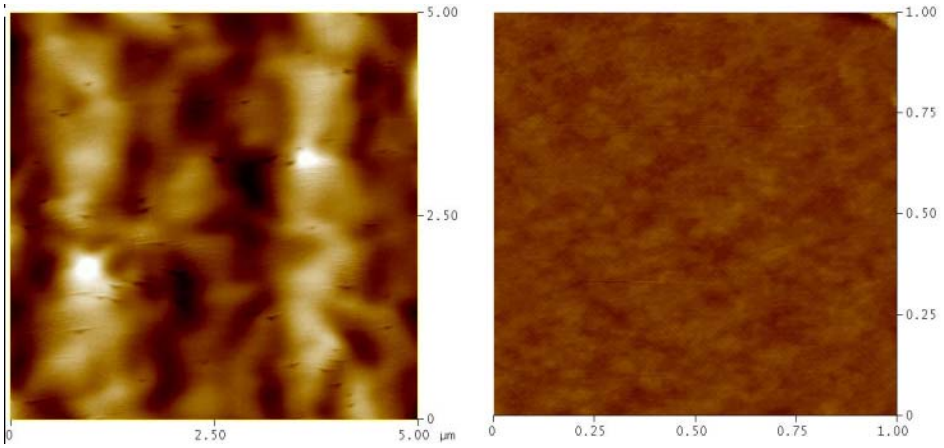


Fig. 5-5 Surface morphology of (a)MOCVD-epi GaAs (b)bulk GaAs substrate

Parameter (@300K)	R_{ms} *(nm)*	R_S	μ_{Hall} *($cm^2 V^{-1} S^{-1}$)*	N_d *(cm^{-3})*
Epi-GaAs	***3.46 (0.3)***	***108***	***598 (8500)***	***6.5E17***

Table 5-1 The Hall measurement of MOCVD-epi GaAs on Si with SiGe buffer layer

簡　歷

姓名　：　江欣哲

性別　：　男

生日　：　中華民國七十三年八月十九日

出生地：　台灣省台北市

地址　：　台北市北投區承德路七段 344 巷 12 號 5 F

學歷　：　國立台北教育大學自然科學教育學系

(民國九十一年九月 – 民國九十五年六月)

國立交通大學電子工程研究所碩士班

(民國九十五年九月 – 民國九十七年九月)

碩士論文題目：

原子層沉積高介電係數氧化鋁閘極介電層之三五族元件電物性研究

(***Electrical and physical characteristics***

of III-V devices with atomic-layer-deposited Al_2O_3 high-κ gate dielectric)