國立交通大學

電子工程學系　電子研究所

碩　士　論　文

一個與電壓控制震盪器整合的 *K* 頻帶互補式金氧半 E 類功率放大器

A *K*-Band CMOS Class E Power Amplifier Integrated with Voltage-Controlled Oscillator

研 究 生：彭國權　　(Guo-Quan Peng)

指導教授：吳重雨教授 (Prof. Chung-Yu Wu)

中華民國九十九年十一月

一個與電壓控制震盪器整合的 *K* 頻帶互補式金氧半 E 類功率放大器

A *K*-Band CMOS Class E Power Amplifier Integrated with Voltage-Controlled Oscillator

研 究 生：彭國權　　Student: Guo-Quan Peng

指導教授：吳重雨教授　　Advisor: Prof. Chung-Yu Wu

國立交通大學

電子工程學系　電子研究所

碩士論文

A Thesis
Submitted to Department of Electronics Engineering and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao-Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master
in
Electronics Engineering
November 2010

Hsin-Chu, Taiwan, Republic of China

中華民國九十九年十一月

一個與電壓控制震盪器整合的 *K* 頻帶互補式金氧半 E 類功率放大器

研究生: 彭國權　　指導教授: 吳重雨 博士

國立交通大學

電子工程學系 電子研究所碩士班

摘要

具有高操作頻率高傳輸速率的通訊系統已被視為次世代通訊系統的主軸。在最近幾年，*K* 頻帶中，已有許多頻帶如 24.05–24.25-GHz 的 ISM-band 及 22–29 GHz 被 FCC 釋出作為汽車雷達應用等用途。

此論文中介紹實現一個與電壓控制震盪器整合操作在 *K* 頻帶的互補式金氧半 E 類功率放大器。此電路包含了一個 LC 槽的電壓控制震盪器以及一個 E 類功率放大器等電路並且使用了 0.13-μm CMOS 技術來設計並製造。藉由使用電壓控制震盪器與高功率效益 E 類功率放大器，使得在大訊號操作高輸出功率的傳送器電路上可以得到高功率效益的性能。

此電路包含了電壓控制震盪器以及 E 類功率放大器等電路,已被模擬、實現於 1.05 mm^2 的晶片面積、以及量測。根據量測結果，此電路由於佈局時的錯誤、EM、寄生效應的考慮沒有詳盡，使得輸出功率減少 12.56 dB。然而，從修改後的模擬結果與其它所發表電路比較可知，此電路操作在較低的供應電壓下，仍有較高的功率效益。因此，E 類功率放大器電路非常適合用在高功率效益的應用，尤其是高整合度、低成本的 CMOS 製程。

A *K*-Band CMOS Class E Power Amplifier Integrated with Voltage-Controlled Oscillator

Student: Guo-Quan Peng Advisor: Dr. Chung-Yu Wu

Department of Electronic Engineering &
Institute of Electronics
National Chiao Tung University

Abstract

In the next-generation wireless communication, high data rate transmission with a high operating frequency is expected to be realized. Over the past few years, the 24.05–24.25-GHz Industrial, Scientific, and Medical (ISM) band, 22–29 GHz band provided by Federal Communications Commission (FCC) for the operation of vehicular radar have been released.

In this thesis, a *K*-band CMOS class E power amplifier integrated with voltage-controlled oscillator is presented. The proposed circuits which consist of a LC-tank voltage-controlled oscillator and a class E power amplifier are designed using 0.13-μm CMOS technology. By adopting voltage-controlled oscillator and high efficiency class E power amplifier, the large-signal operated high output power transmitter circuit can be implemented with high efficiency performance.

The proposed circuits, including a voltage-controlled oscillator and a class E power

amplifier, are simulated, fabricated with a chip size of 1.05 mm^2, and measured. Because of the layout mistake, and the effects such as EM, parasitic effect which are not carefully considered before fabrication, the measured output power decreases 12.56 dB. Comparing the results of the re-design circuits with other proposed circuits, however, the class E power amplifier can have better efficiency under lower supply voltage. Therefore, class E power amplifier is suitable for high efficiency application, especially for high-integrated low-cost CMOS technology.

誌　　謝

本論文能夠順利完成，首先要感謝的是我的論文指導教授吳重雨老師這幾年下來辛勤的指導。在老師的教誨下，讓我學到很多類比積體電路設計的專業知識和待人處世的方法，使我受益匪淺。

另外要感謝博士班的王文傑學長、黃祖德學長、陳旻珓學長、虞繼堯學長、蘇煊毅學長、Fadi 學長、台祐學長、世豪學長等曾經給我的指點、討論和協助，讓我在研究的過程中能順利的進行。再來我要感謝碩班已畢業的學長們以及實驗室的同學與學弟妹們:順維學長、國忠學長、維德學長、柏宏學長、廷偉學長、晏維學長、昌平學長、大仔、塔哥、區文、威宇、政邦、建名、歐陽、科科、紹歧、北鴨、世範、宗恩、亭州、順天學弟、育祥學弟、kitty 學弟、敬程學弟、韋丞學弟、宗昀學弟、慧君學妹、慧雯學妹、世昕學弟、邱神學弟、佳琪學妹、堂龍學弟、書瑾學妹、子薰學弟、明翰學弟、、、等。在這幾年中我們一起研究功課，在失落的時候互相鼓勵，使我在碩士生涯不會有孤單奮戰的感覺。

另外，我要謝謝我的女朋友佐芝，謝謝妳陪我走過我的碩士生涯，在我最失落失意的時候，能忍受我的脾氣並鼓勵、接受著我。

最後，我要謝謝我的家人，謝謝你們無限制的容忍著我的失敗與失落，讓我感受到無論發生什麼事都有人支持著我，而使我能無後顧之憂的向成功邁進。

其他要感謝的人還有很多，無法一一列出，在此一併謝過。

彭國權

于　風城交大

99 年　　冬

A *K*-Band CMOS Class E Power Amplifier Integrated with Voltage-Controlled Oscillator

Contents

Table Captions

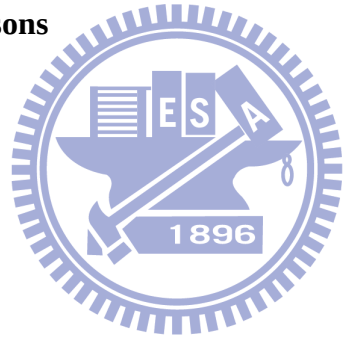


Figure Captions

Chapter 1

Introduction

1.1. Background

Recently, the research on radio-frequency integrated circuits (RFICs) in higher frequencies have been accelerated since the frequency spectra below 10 GHz have gradually become crowded by massive requirements of data transmission from the modern wireless applications such as Bluetooth, wireless local area network (WLAN) and ultra-wideband (UWB), etc. Many researchers investigate RF transceiver front-end circuits in 24 GHz because higher operating frequency can provide more bandwidth. In addition, the 24.05–24.25-GHz Industrial, Scientific, and Medical (ISM) band [1], 22–29 GHz band provided by Federal Communications Commission (FCC) for the operation of vehicular radar [2]–[3], and the 24-GHz band plan as shown in Fig. 1-1 [4] are released.

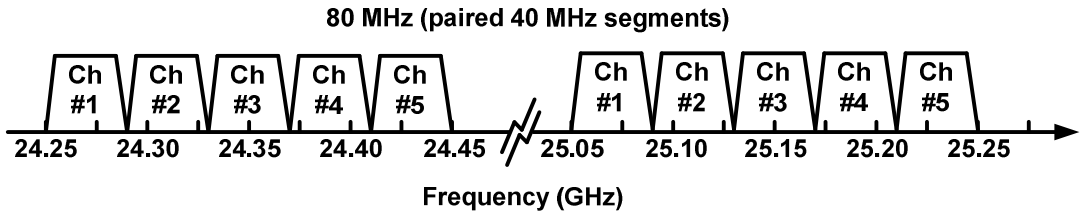


Fig. 1-1 24-GHz service band plan release by FCC

In RF transmitter front-end, key components such as voltage-controlled oscillators (VCOs) and power amplifiers (PAs) have been reported in many CMOS designs [5]–[7]. Nevertheless, in standard CMOS technologies, the active devices have poor inherent characteristics comparing to GaAs and SiGe, and the passive components such as planar inductors have higher losses from lossy substrate. These inherent characteristics seriously degrade the performance of the transmitter front-end circuits. However, today's consumers demand wireless systems that are low-cost, power efficient, reliable and have a high integration form. High levels of integration are desired to reduce cost and achieve compact form. Hence the long term vision of goal for wireless transceiver is to merge as many components as possible to a single die in an inexpensive technology. Therefore, there is a growing interest in utilizing CMOS technologies for RF power amplifier (PAs) [8]. Although the output power of the transmitter can be increased by utilizing multiple parallel transistors to implement power amplifiers [5], the power-added efficiency (PAE) remains the same in such a structure. To improve the PAE, several design techniques have been proposed. By using the special structure of transmission line and additional algorithms, the PAE of a RF CMOS PA can be improved to around 10% [6]–[7].

1.1.1. Review on Class E Power Amplifier

Class E power amplifier is a single transistor operated as a switch. It uses a high order reactive network to shape the switch voltage to have both zero value (zero voltage switching; ZVS) and slope (zero derivative switching; ZDS) at the switch turn-on. Therefore, the ideal efficiency is 100 %. A class E power amplifier is showed in Fig. 1-2. The drain voltage and current waveform of ideal class E power amplifier is showed in Fig. 1-3.

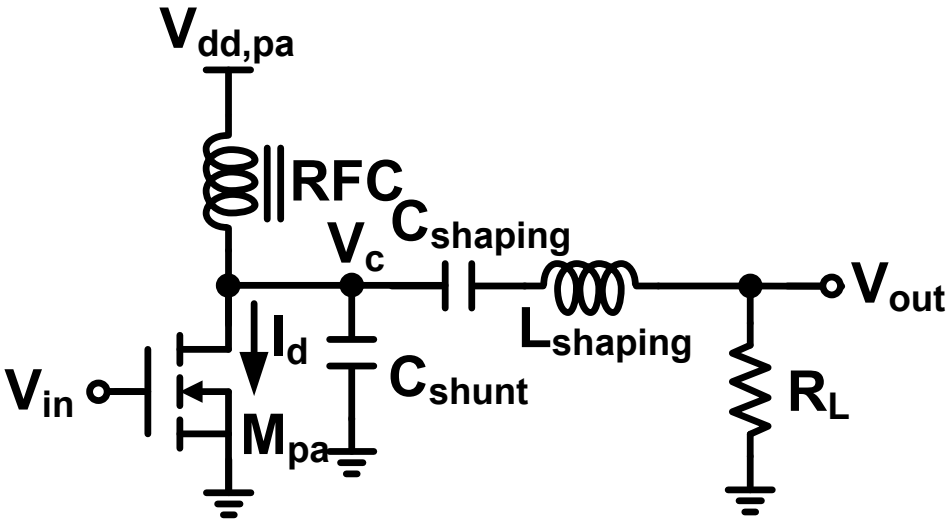


Fig. 1-2 Class E power amplifier

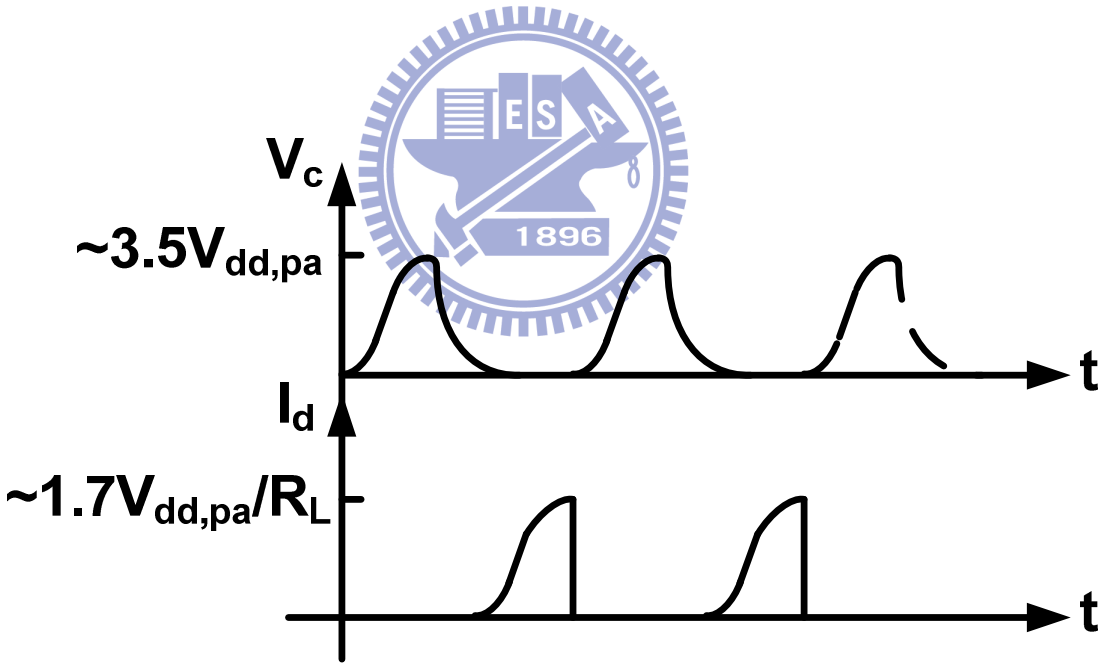


Fig. 1-3 Drain voltage and current waveforms of ideal class E power amplifier

Obviously, the current of the transistor is near maximum when the switch turns off. However, it will introduce a significant switch turn off losses because the switch is not infinitely fast. Hence, it will reduce the efficiency. Another drawback is the large peak voltage approximately 3.56 $V_{dd,pa}$ when the switch sustains in the off state. Therefore, it needs a high breakdown voltage and is not a good choice for short-channel devices.

An 18 GHz fully-integrated class E power amplifier is proposed in [9], as shown in Fig. 1-4. It consists of a two-stage cascode amplifier, a common source driver, and an output stage. Due to the limited voltage headroom, common-source amplifiers are used in the last two stages. The cascode amplifiers are used to provide sufficient gain, good input matching and isolation from the last two stages which potentially could oscillate. Besides, this proposed fully-integrated class E power amplifier also adopts a mode-locking (also known as injection-locking) technique exploiting the instability of driver amplifier which is used to improve the drive for the gate of output stage. The mode-locking technique actually increases the gain of the circuit and reduces the drive requirement for switching the output transistor. The comparison table in [9] shows that this class E power amplifier has significantly higher efficiency and lower input requirement than that for the previously reported CMOS PA operating near 20 GHz. It also suggests CMOS technology is a viable candidate for building fully-integrated transmitter near 20 GHz. But the method of its isolation is too complicated; we develop another kind of isolation technique to improve this disadvantage as will be discussed after. Due to the limited voltage headroom, the power supply of [9] is too high and the power added efficiency (PAE) is not high enough.

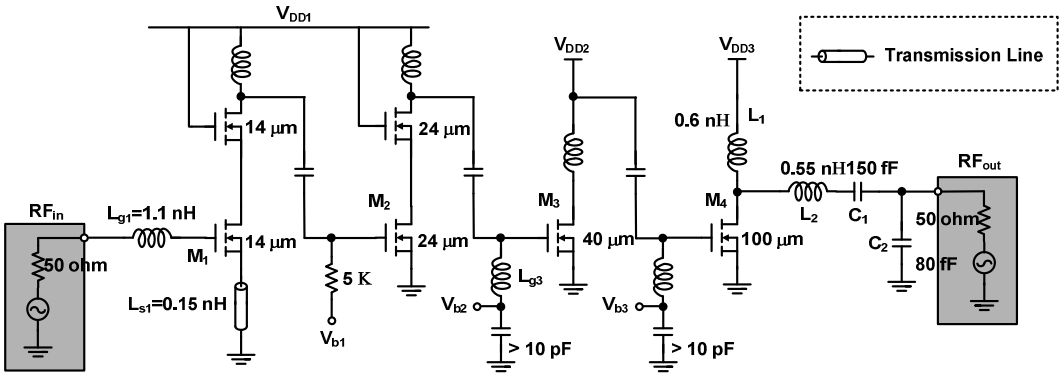


Fig. 1-4 Schematic of proposed class E power amplifier in [9]

1.1.2. Review on K-Band (18 - 26.5 GHz) Power Amplifier

Schematic shown in Fig. 1-5 is a 24 GHz current-mode power amplifier proposed in [10]. It is accomplished by using two-stage cascade current-mirror structure and it also operates in class AB mode. Besides, the proposed current-mode power amplifier also uses L_7 and L_8 to resonate the device capacitance between gate and drain of M_8 and M_{10}. It also uses R_3 for low frequency stability consideration. And the optimized output impedance transfer network is determined by the load-pull simulation. From the comparison table in [10], it shows that the proposed CMOS current-mode power amplifier has the highest PAE and the largest output power among the RF PAs.

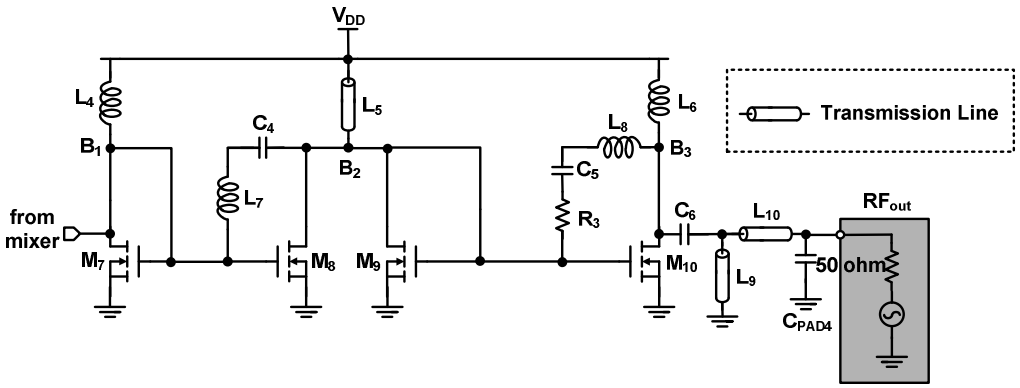


Fig. 1-5 Schematic of proposed current-mode power amplifier in [10]

Schematic shown in Fig. 1-6 is another *K*-band power amplifier proposed in [11]. It is composed of 3 stages. The first two stages are driver stage, and the third stage is

formed by two parallel power cells. The typical topologies of the CMOS transistors are common source and cascode. The biasing point of this design is at class A for better linearity. The devices selected in the power cell were determined by the load-pull simulation from the large signal model provided by TSMC, and the G_{max} simulation. The power stage includes two power cells. And the power cells are in-phase combined directly. Two odd-mode suppression resistors of 11 Ω are placed within two power cells for stability consideration. Each power cell was pre-matched to 100 Ω by an appropriate matching network before binary combining. The matching network includes an inductor (used for inductive peaking), and impedance transform network, which is implemented by thin film micro-strip lines (TFMS) used for lower loss than lumped elements for wide band power match. Appropriate bypass circuits are placed at each bias point for low frequency stability consideration. The comparison table in [11] shows that the proposed *K*-band power amplifier has the highest gain and good output power in standard CMOS process.

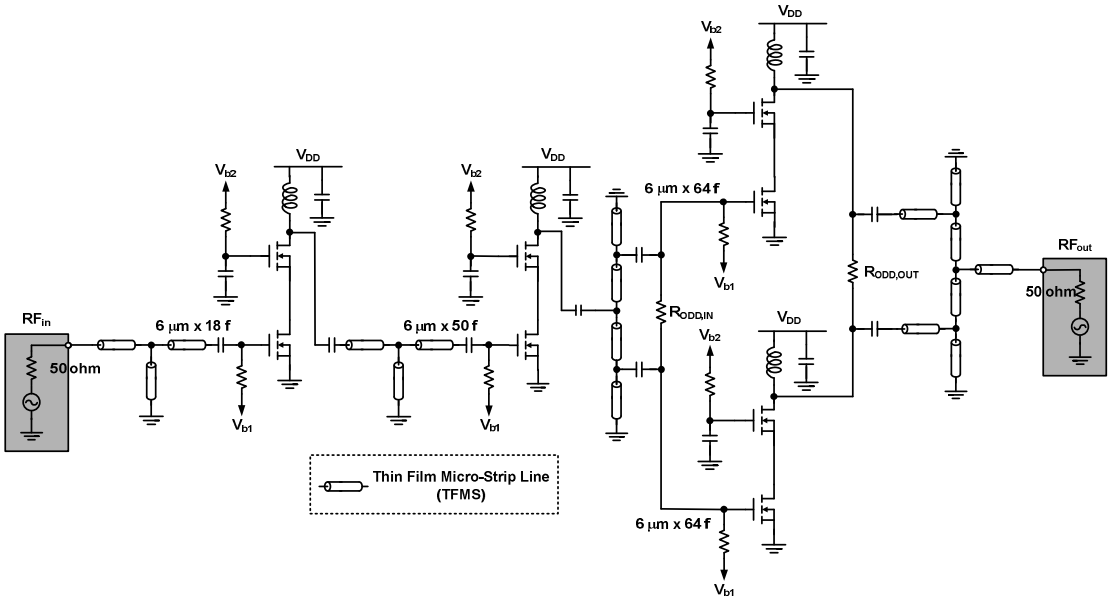


Fig. 1-6 Schematic of proposed *K*-band power amplifier in [11]

Schematic shown in Fig. 1-7 is a 24 GHz power amplifier proposed in [12]. By shunt combining N times transistors with device size of (W/N), the parasitic capacitance C_{gd} of each transistor is reduced, which means higher gain and output power performance are maintained. The binary combining method is a simple way to combine output power of each transistor with equal phase and loss. To maintain low loss in output matching circuits with good stability at low frequency, output high pass matching network is chosen. A shunt short stub is connected to the device to resonance the parasitic capacitance and provides dc biasing path. By shunting the resonance stubs, the optimum load impedance is calculated via the load line estimation and the load-pull simulation. The T-shaped high-pass matching is used as impedance transformer and ensures the low frequency stability. In order to achieve higher gain and better linearity performance, the cascode pairs are all biased in class A. It also uses thin-film micro-strip line (TFMS) for interconnection and matching stubs. The proposed 24 GHz power amplifier provides larger gain and power compared to commercial designs. From the comparison table in [12], the proposed power amplifier shows the highest OP_{1dB} and saturation power among the CMOS PAs above 20 GHz.

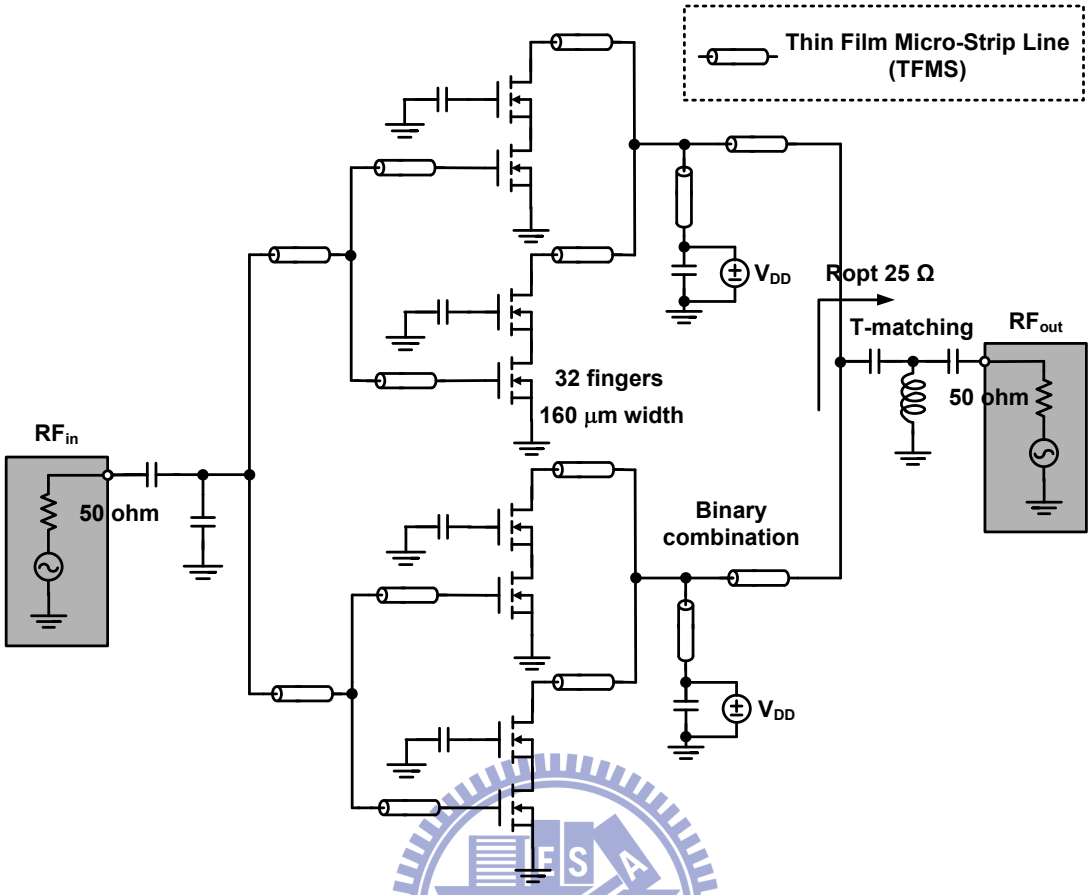


Fig. 1-7 Schematic of proposed 24 GHz power amplifier in [12]

Schematic shown in Fig. 1-8 is a 24 GHz power amplifier proposed in [13]. The PA has two gain stages with each gain stage consisting of a cascode transistor pair to ensure stability and increase breakdown voltage. The PA is designed to operate in class AB mode. The output and inter-stage matching networks in the PA are realized with the substrate-shielded coplanar waveguide structure to reduce power losses and area. The substrate-shielded coplanar waveguide is leading to more than a factor of two reductions in wavelength at 24 GHz when compared to a standard coplanar waveguide structure in silicon dioxide. The short wavelengths can improve isolation and make this structure particularly suitable for integrating multiple power amplifiers on the same die. Amplifier stability is improved by the RC network at the input of each stage, which guarantees low frequency stability.

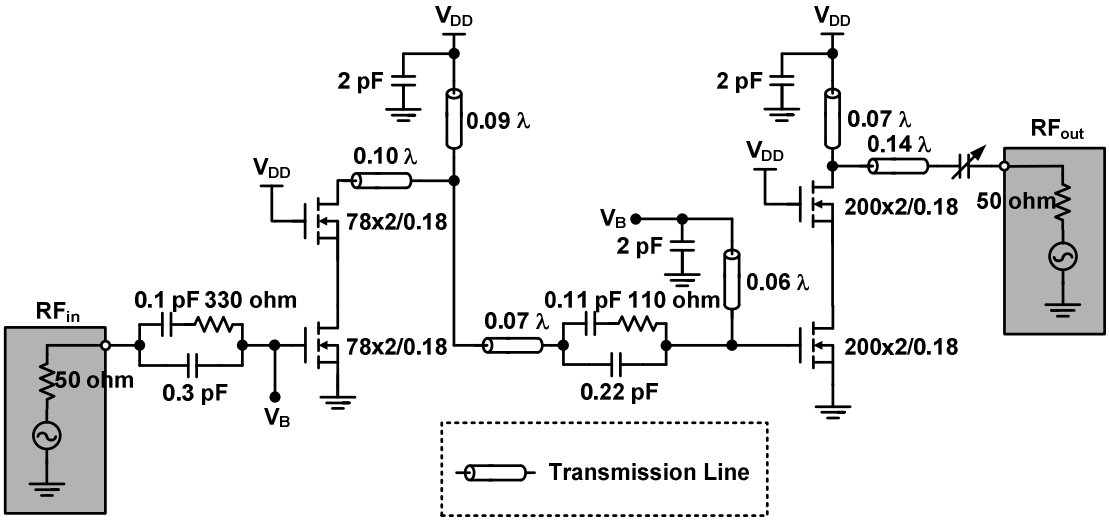


Fig. 1-8 Schematic of proposed 24 GHz power amplifier in [13]

1.2. Motivation

This research focuses on the novel approach for designing and implementing 24-GHz transmitter circuits by CMOS technology.

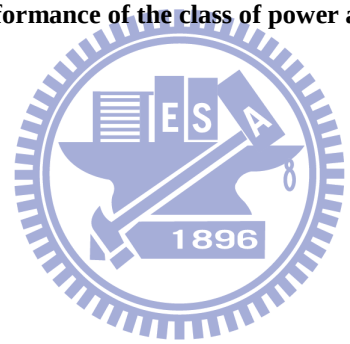
Because of the applications released in 24-GHz frequency range, many researchers are attracted to design high-performance and low-cost wireless applications in this frequency band with advanced CMOS technologies. However, CMOS technology has limitation of low supply voltage. That is why traditional commercial implementation of wireless transceivers typically utilizes a mixture of technologies in order to implement a high-performance, completed system. Nevertheless, considering the cost and integration capability, CMOS technology is still the most suitable choice for designing RF circuits.

When implementing 24-GHz transmitter circuits by CMOS technology, the output power of the transmitter can be increased by utilizing some structures to implement power amplifiers. The higher output power can be achieved, but the power-added efficiency remains the same in such structures. Therefore, the improvement of the PAE of a RF CMOS PA at the higher output power level is a main course of discussion. According to theses reasons as mentioned above, the class E power amplifier compared with other class of power amplifiers at *K*-band as the Table 1-1 shown can provide higher power-added efficiency. Therefore, at 24-GHz, we adopt the class E power amplifier as our design which tries to improve the PAE of a RF CMOS PA at the higher output power level and use the voltage-controlled oscillator as the input signal of class E power amplifier. The use of class E power amplifier has solved the design conflict between improvement of power efficiency and maintenance of amplifier linearity in *K*-band system. Besides, in order to solve the isolation problem, a neutralization technique must be developed.

	[9]		*[10]	[11]	[12]	[13]
Technology	0.13-μm CMOS		0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Topology	Class E		Class AB	Class A	Class A	Class AB
Supply Voltage (V)	1.5		1.2	3.6	3.6	2.5
Freq (GHz)	18	20	24	18-23	24	24
Output Power (dBm)	10.9	10.2	17.1	20.1	22	14
Peak PAE (%)	23.5	20.5	23.9	9.3	20	6.5
Chip Area (mm^2)	0.782		1.05	2.4	0.42	14.28

*[10] : redesign post-sim results of proposed power amplifier in [10]

Table 1-1 Performance of the class of power amplifiers at *K*-band



1.3. Main Results and Thesis Organization

In this work, the voltage-controlled oscillator and class E power amplifier are designed. The voltage-controlled oscillator is realized by cross-coupled NMOS with LC tank and PMOS current source oscillator. Besides, the voltage-controlled oscillator cascades with a cascode buffer. A differential single stage common source class E amplifier is proposed for the power amplifier. This is the first work including a voltage-controlled oscillator and a power amplifier for *K*-band applications.

Measurement results show that the measured output center frequency and maximum output power are 23.2 GHz and –2.41 dBm, respectively. The measured phase noise is -108 dBc at 10 MHz. The measured output power of cascode buffer with power amplifier is lower than original post layout simulation about 13 dB. And the measured total power consumption of VCO and power amplifier is 29.4 mW from 1.2 V power supply. From the analysis, experimental results, and re-design circuit, the proposed circuit is suitable for high efficiency application.

The post layout simulation results of the re-design circuits show that the output center frequency and maximum output power are 24.26 GHz and 10.41 dBm, respectively. The phase noise is -119.9 dBc at 10 MHz. The output power of cascode buffer with power amplifier is almost the same to the original post layout simulation. And the total power consumption of VCO and power amplifier is 56.13 mW from 1.2 V power supply. The power consumption is less than other type power amplifier because the class E power amplifier operates at the threshold voltage.

The thesis is divided into five chapters. Chapter 1 introduces the background, motivation and main results of this research. The whole circuit design and simulation results of this thesis will be presented at Chapter 2. Design considerations are discussed in Section 2.1. Then the power amplifier, voltage-controlled oscillator and

the whole circuits design procedures are presented in Section 2.2.1, 2.2.2, and 2.2.3, respectively. Post-simulation results are shown in Section 2.3.

The chip microphotograph, measurement setup, experimental results, revised post simulation and re-design will be included in Chapter 3. Finally, the conclusions and future work will be presented in Chapter 4.

Chapter 2

Circuit Design and Simulation Results

2.1. Design Considerations

How to use CMOS technology to design large-signal transmitter front-end circuits is the most challenge part. In order to obtain enough trans-conductance, the transistors' sizes must be increased. However, the larger the size it is, the more serious parasitic effect it will be. The parasitic capacitance effect will provide leakage path for high-frequency signal or degrade reverse isolation and stability. In this research, these leakage paths for RF signal and stability-degraded effects are resonated and neutralized by on-chip inductors, respectively. The output matching network of power amplifier is determined by load-pull analysis which considers the imaginary part caused by the parasitic effect.

The block diagrams of polar loop structure are shown in Fig. 2-1. In this research, as shown in Fig. 2-1, the proposed circuits included a voltage-controlled oscillator with cascode buffer and a class E power amplifier are realized with 0.13-μm standard CMOS technology. The designed VCO is implemented by the cross-coupled NMOS with LC tank concept in order to provide a signal source for class E power amplifier. The class E power amplifier is also realized by push-pull concept. The 1st-stage of cascode buffer the RF signal comes from designed VCO to drive the 2nd-stage of class E power amplifier. The 2nd-Stage is designed to have capability to provide enough signal swing that the required output power can be achieved. The specification of the designed whole circuits is to output more than 10-dBm output power at 24 GHz.

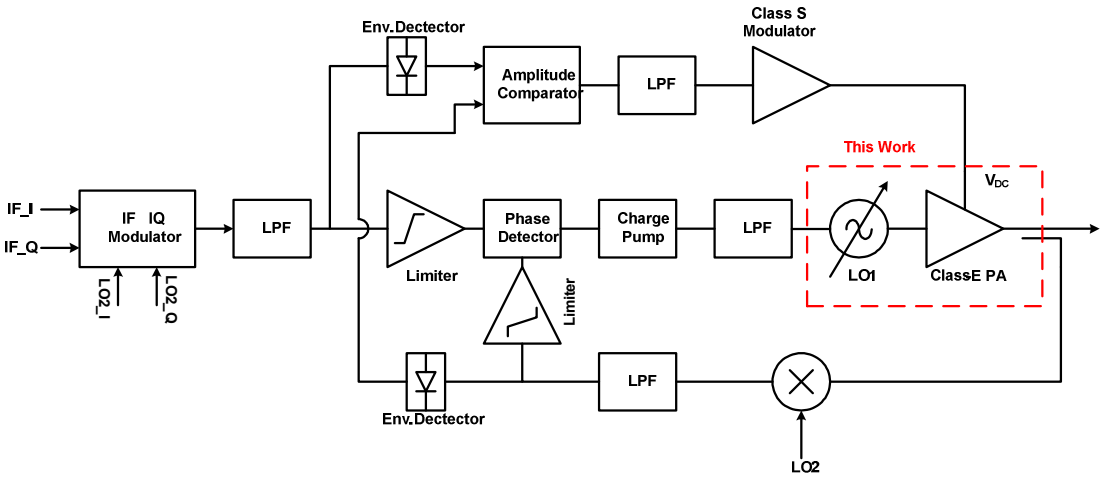


Fig. 2-1 Block diagrams of polar loop structure

2.2. Circuit Design

2.2.1. Class E Power Amplifier

Class E power amplifiers (PA) have been proved to be popular radio frequency (RF) PAs with high efficiency. Using Class E power amplifier can maintain high enough efficiency at high output power level. To achieve high enough efficiency, the output load network must be carefully designed to eliminate the overlap between voltage and current waveform at the designated operating frequency and output power level. Generally speaking, the transistor output capacitance included the parasitic capacitances constructs an optimum parallel reactance at the output load network and satisfies the optimum Class E power amplifier conditions. The conditions of Class E power amplifier were given by Sokal [14], and can be put in the form:

$$Class\ \text{E} \Leftrightarrow \begin{cases} v_{sw}(t_{on}) = 0 \\ \left.\dfrac{dv_{sw}}{dt}\right|_{t_{on}} = 0 \end{cases} \tag{2.1}$$

Where t_{on} represents the instant at which the switch closes, and $v_{sw}(t)$ represents the switch voltage. These conditions can be guaranteed by the use of the load network shown in Fig. 2-2. And the voltage and current waveforms of Class E power amplifier are also shown in Fig. 2-3. Above equations show the typical properties of Class E power amplifiers, where the passive components are used to minimize the drain-source voltage when the switch closes. This property of Class E power amplifiers is usually called “zero voltage switching”. Furthermore, another one property can demand that the derivative of the switch voltage also equals zero at the switching moment. Which is usually called “zero derivative switching”. These demands will make the amplifier less sensitive to timing errors and component variations [15].

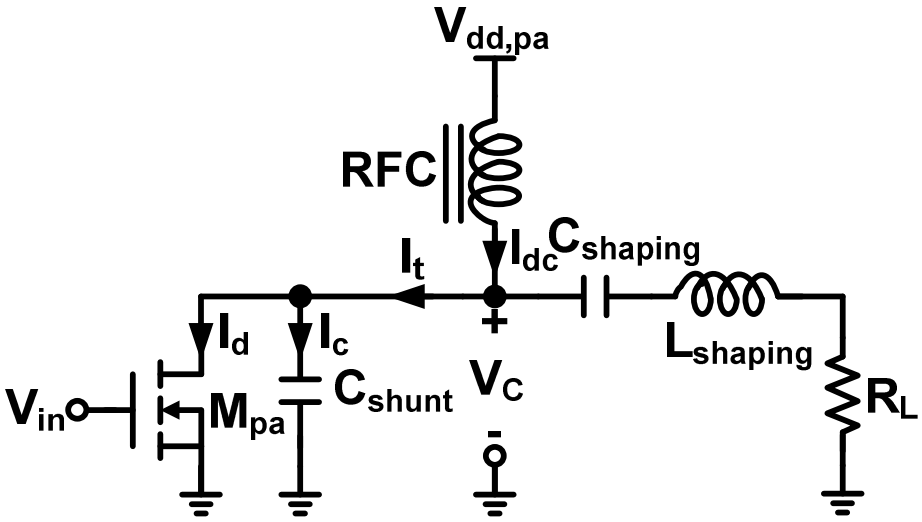


Fig. 2-2 The load network of class E power amplifier

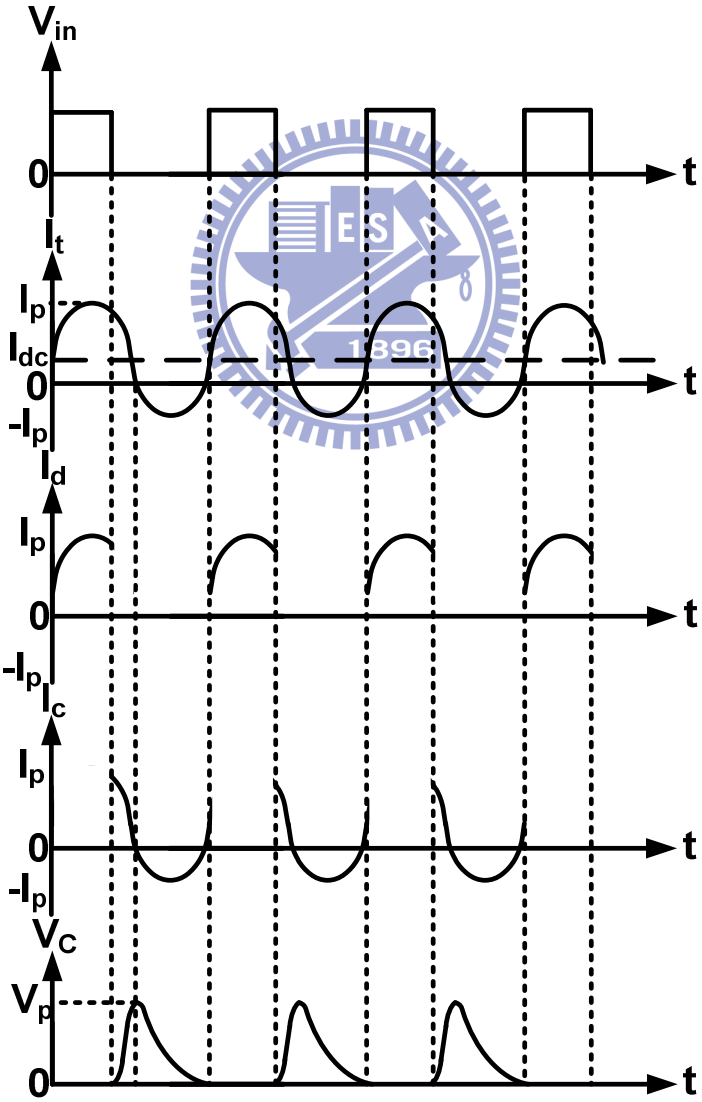


Fig. 2-3 Voltage and current waveforms of class E power amplifier

After the switch turns off, the load network operates as a damped second-order system as shown in Fig. 2-4 with initial conditions across C_p and C_s and in L_s. The time response depends on the quality factor Q of the network for underdamped, overdamped, and critically damped conditions. We note that in the last case, V_X approaches zero volt with zero slope.

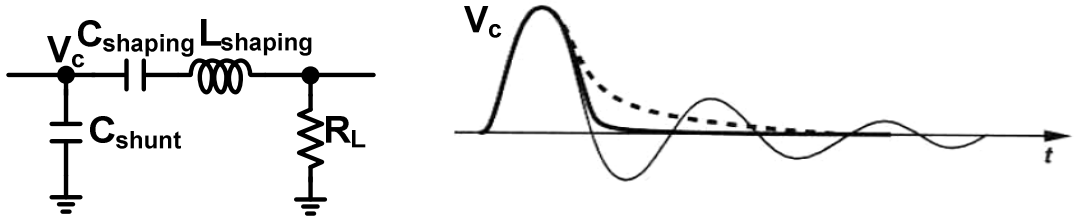


Fig. 2-4 Response of class E power amplifier when the transistor turns off

When implementing a power amplifier at high output power level, the most critical node in the power amplifier circuit is its output node and resultant large voltage and current swing are required. Operated at high output power level which implies to need large DC bias means that the reliability such as metal current density must be considered. Besides, large voltage and current swing which implies to the large-signal operation viewpoint must also be considered with the small-signal operation viewpoint at the same time. Therefore, for the power amplifiers of RF systems, the output impedance transformation networks (output matching networks) are always implemented by load-line or load-pull analysis method instead of traditional conjugate matching analysis method.

The traditional conjugate matching analysis method can provide maximal power transfer only under the condition of no current and voltage swing limitation. In other words, it is always true for small-signal operation. That's why most of RF systems, such as receiver, adopt traditional conjugate matching analysis method for their matching networks. However, in the transmitter front-end, especially for the output of power amplifier, the large voltage and current swing are large signal operation

viewpoints. Because the output of power amplifier always produces high output power level, the current or voltage swing always reaches the limitation of its supply. Therefore, the output matching networks of power amplifiers are usually determined by two methods – load-line or load-pull analysis methods instead of traditional conjugate matching analysis method.

Fig. 2-5 shows the quantitative description of the above analysis methods for the difference of optimal load if the voltage and current swing are limited. For traditional conjugate matching analysis method, the load resistance R_{LOAD} is chosen to equal to R_S. Under the voltage and current swing are limited conditions, the "V_{MAX}/I_{MAX}" load resistance has maximal output power delivered capability than any other load resistance.

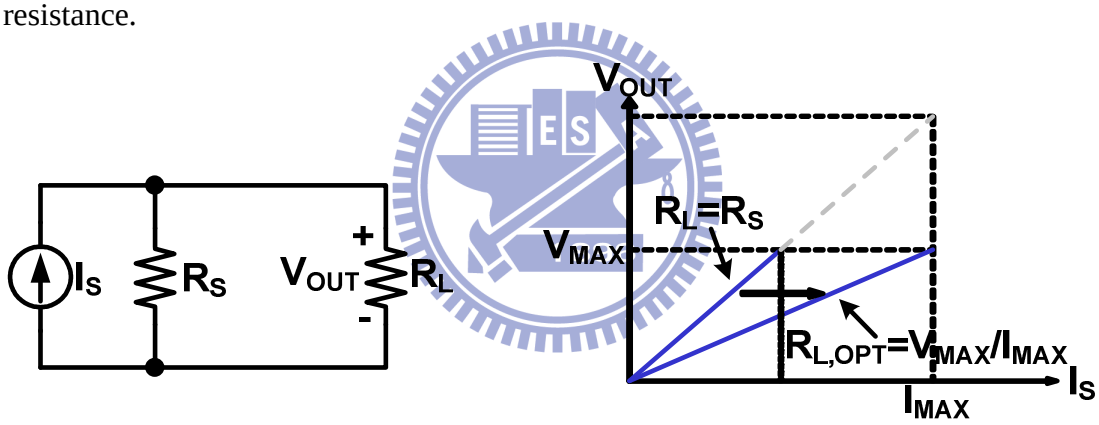


Fig. 2-5 Effect for optimal load when swing is limited

The hand-calculated procedure for load-line analysis can be accessed through (2.2)–(2.3).

$$P_{OUT,MAX} = \frac{1}{2}(V_{DC} - V_{knee})I_{DC} \tag{2.2}$$

$$R_{L,OPT} = \frac{V_{DC} - V_{knee}}{I_{DC}} \tag{2.3}$$

According to these equations, the load-line analysis on a common-source transistor I-V curve is illustrated in Fig. 2-6.

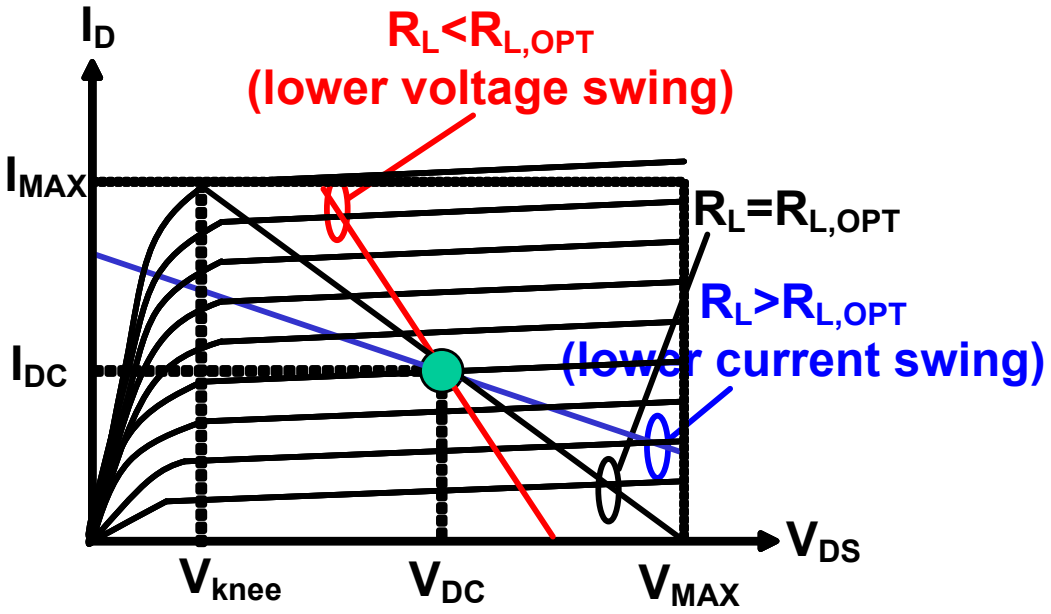


Fig. 2-6 Optimal load resistance determined by load-line analysis

The black color load-line is the optimal load resistance determined by load-line analysis. And the optimal load resistance value also equals "V_{MAX}/I_{MAX}". It shows that the black color load-line has maximal output power under this voltage and current swing limitation. The red color load-line is the load resistance which is smaller than the optimal resistance. It will have the same current swing but smaller voltage swing and resultant smaller output power. The blue color load-line is the load resistance which is larger than the optimal resistance. It will have the same voltage swing but smaller current swing and resultant smaller output power.

Based on the figures and equations of load-line analysis above, the load-line analysis can be used for quickly determining optimal load resistance, but not reactance. That is, only the real part of the load impedance (Z_L) can be determined by this analysis, the effect of imaginary part caused by the parasitic effect of the circuit will be completely neglected. Because the load-line analysis bases on I-V curve, the junction parasitic effect is exclusive. Unfortunately, when the signal is operated at high frequency, the parasitic effect induces lose. Besides, the larger size of the transistor it is, the parasitic effect is worse and cannot be ignored.

Considering the parasitic effect and comparing to the load-line analysis, the load-pull analysis can be used to determine the load impedance Z_L, both real and imaginary part, of power amplifiers. The load-pull analysis is mainly to sweep Z_L to see how PAs perform. The analysis procedures are：First, add a load tuner (Z_L) at the output of power amplifier. Second, sweep the value of load tuner (Z_L) to see the difference of output power (P_{OUT}) and power-added efficiency (PAE). Because of each point on Smith chart is a reflection coefficient, and the reflection coefficient and impedance are one-to-one mapping for 50 Ω characteristic impedance. When changing the value of load tuner (Z_L), the swept data of the same output power and the same PAE was recorded. The swept data can be used to construct constant P_{OUT} and constant PAE contours. Third, choose one reflection coefficient (load impedance) on Smith chart by trade-off between constant P_{OUT} and constant PAE contours. Using load-pull analysis to determine Z_L has several advantages. Because the constant P_{OUT} and PAE contours are drawn on the same Smith chart, it is easy and obvious to trade-off between them. Besides, because of the one-to-one mapping characteristic, both real and imaginary part of Z_L can be determined as soon as the trade-off point has been chosen.

Another difficulty for designing power amplifier is the parasitic effect. Because high output power is required, a large size of each transistor and resultant seriously parasitic effect are inevitable. Large parasitic C_{gd} provides a short path between input and output at high frequency in common-source amplifier. Therefore, a resonated inductor (L_{gd}) must be added between these two nodes shown in Fig. 2-7 for resonating parasitic C_{gd} for stability consideration.

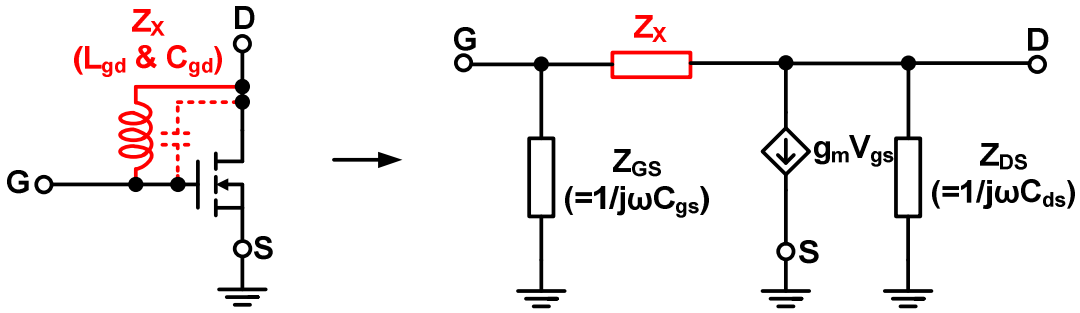


Fig. 2-7 Neutralization for resonating parasitic C_{gd}

The small-signal model for a common-source amplifier is shown in Fig. 2-8. Because the S-parameter S12 is desired, input phasor E_2 is placed at port 2 (drain).

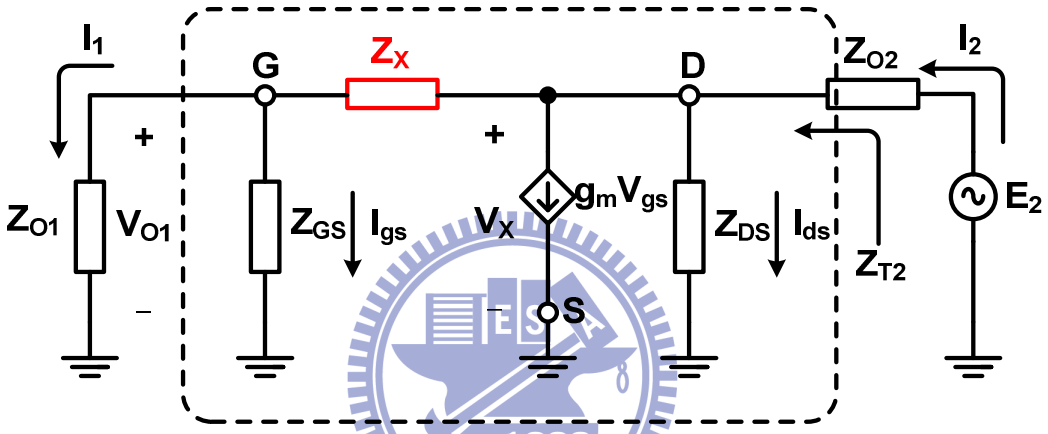


Fig. 2-8 Small-signal model of common-source transistor

According to the definition of S12 shown in (2.4) [16], the term "V_{O1}/E_2" can be expressed by (2.5). Although equations (2.4) and (2.5) can show the effect for value of Z_X, it is not obvious. In order to further simplify this equation, the matched condition at output node is assumed. This condition is always true for RF systems. The S22 of common-source amplifier can be calculated through (2.6) to (2.7). α and β are the substituted variables for the numerator and denominator in (2.6), respectively. Under the matched condition, the condition "$Z_{O2}\beta=\alpha$" can be derived as shown in (2.8). Thus the equation (2.5) can be further simplified by this derived condition and the final result for S12 of common-source amplifier is shown in (2.9).

For a traditional common-source amplifier, Z_X is "$1/j\omega C_{gd}$" and S12 will become the equation in (2.10). Thus larger the transistor size it is, larger the value of parasitic

C_{gd} it has and worse the reverse isolation it becomes. For extremely case of infinitely large C_{gd} value, the S12 will become the equation shown in (2.11) and equal to 1 (or 0 dB) in general for RF circuits (for $Z_{O1} = Z_{O2} = Z_O = 50$ ohm, general case in RF circuits). 0-dB S12 means this circuit has no any reverse isolation or the equivalent circuit for this two-port network is short circuit. It is reasonable because the infinitely large C_{gd} provides a zero-impedance short path between port-1 and port-2.

If the resonated inductor L_{gd} is adopted and placed between gate-drain, the impedance Z_X in (2.9) will become (2.12). Thus S12 can be zero as long as the condition in (2.13) is achieved. That is the reason why a resonated inductor is always adopted for large-sized common-source amplifier.

$$S12 \equiv 2 \times \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \times \frac{V_{O1}}{E_2} \tag{2.4}$$

$$\frac{V_{O1}}{E_2} = \frac{Z_{O1} Z_{GS} Z_{DS}}{Z_{O2} \times \left[\left(g_m Z_{O1} Z_{GS} Z_{DS} \right) + \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right) + \left(Z_{O1} Z_{DS} + Z_{GS} Z_{DS} \right) \right] + Z_{DS} \times \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right)} \tag{2.5}$$

$$Z_{T2} = \frac{Z_{DS} \times \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right)}{\left(g_m Z_{O1} Z_{GS} Z_{DS} \right) + \left(Z_X Z_{O1} + Z_X Z_{GS} + Z_{O1} Z_{GS} \right) + \left(Z_{O1} Z_{DS} + Z_{GS} Z_{DS} \right)} \tag{2.6}$$

$$S22 \equiv \frac{Z_{T2} - Z_{O2}}{Z_{T2} + Z_{O2}} = \frac{\alpha - Z_{O2}\beta}{\alpha + Z_{O2}\beta} \tag{2.7}$$

$$S22 \to 0 \Rightarrow Z_{O2}\beta = \alpha \tag{2.8}$$

$$S12 \equiv 2 \times \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \times \frac{V_{O1}}{E_2} = \left(2 \times \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \right) \times \frac{Z_{O1} Z_{GS} Z_{DS}}{Z_{O2}\beta + \alpha}$$

$$= \left(\frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \right) \times \frac{Z_{O1} Z_{GS} Z_{DS}}{Z_X \left(Z_{O1} Z_{DS} + Z_{GS} Z_{DS} \right) + Z_{O1} Z_{GS} Z_{DS}} \tag{2.9}$$

$$S12 = \left(\frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \right) \times \frac{Z_{O1} Z_{GS} Z_{DS}}{\left(\frac{1}{j\omega C_{gd}} \right) \times \left(Z_{O1} Z_{DS} + Z_{GS} Z_{DS} \right) + Z_{O1} Z_{GS} Z_{DS}} \tag{2.10}$$

$$S12 \approx \frac{\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \tag{2.11}$$

$$Z_X = j\omega L_{gd} \,//\, \frac{1}{j\omega C_{gd}} = \frac{j\omega L_{gd}}{1 - \omega^2 L_{gd} C_{gd}} \tag{2.12}$$

$$if \ \omega^2 L_{gd} C_{gd} = 1 \Rightarrow Z_X \to \infty \Rightarrow S12 \to 0 \tag{2.13}$$

For RF system, an ideal inductor is equal to a short path for DC because its impedance is "jωL". Therefore, as long as the resonated inductor is implemented, a blocking capacitor is always used for blocking unnecessary DC path. This blocking capacitor, C_b, comes from the consideration during measurement. The cable inherent resistance between probe and DC power supply is around 3 Ω. It's not a serious issue for small-signal systems such as receiver front-end. However, for hundreds milli-ampere transmitter front-end, it may cause milli-volt or even several volts drop during measurement. Because such voltage drop may downgrade internal biasing points by different levels, DC current may be sunk into unexpected path when measurement. In order to avoid this phenomenon, a capacitor must be added to block DC current from stage to stage.

Fig. 2-9 is the equivalent network between gate-drain of common-source transistor. If C_b is an ideal blocking capacitor (infinite large), parasitic C_{gd} can be resonated by L_{gd} at desired frequency to increase reverse isolation. However, the effective value of inductor (L'_{gd} in Fig. 2-10) is slightly smaller than L_{gd}. It will slightly shift the resonant frequency caused by L'_{gd} and parasitic C_{gd}. This problem can be corrected by fine tuning the value of L_{gd} [10].

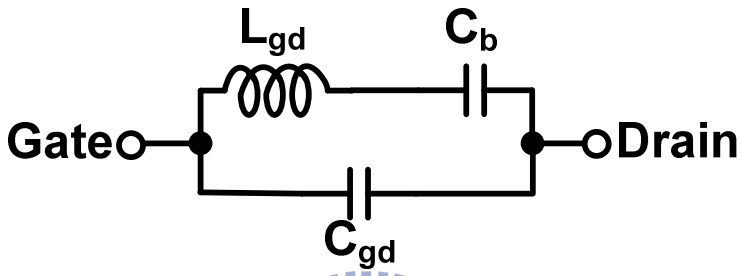


Fig. 2-9 Equivalent network between gate-drain of common-source transistor

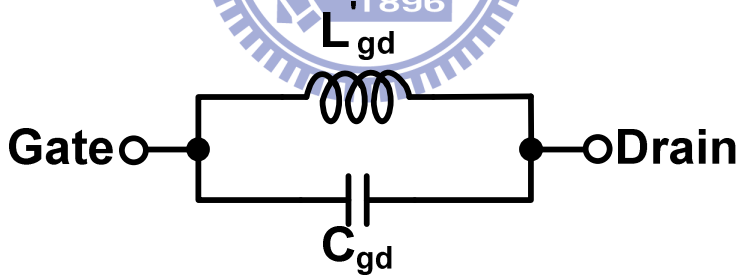


Fig. 2-10 Equivalent network between gate-drain of common-source transistor (L'_{gd} is the combination of L_{gd} and C_b)

By (2.2)–(2.3), the transistors' dimensions and optimal load resistance can be roughly predicted by hand calculation. Because the biasing is fixed to V_{DD}, the variable for transistor itself is size. And the operation mode is class E, the gate biasing is also fixed to the transistor threshold voltage. The transistor's size is also determined by the required output power. In order to determine the transistor's size, some analysis steps on transistor which is operated at class E condition are needed. At first, the transistor

operates at ideal case which means that the transistor turn-on resistance ideally equals zero. According to the assumption, some initial design steps can be provided. But because of the assumption, these initial design steps are not suited to design the circuits. These initial design steps can only determine some initial circuit parameters. Therefore, the transistor turn-on resistance should be considered and the modified design steps could be provided. These design steps are shown below. The load network of ideal case class E power amplifier is shown in Fig. 2-11.

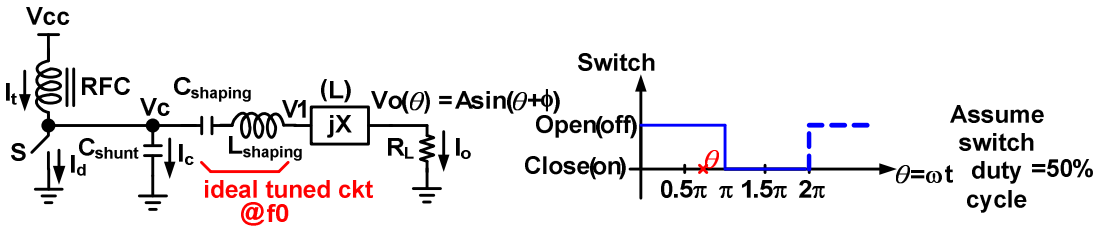


Fig. 2-11 The load network of ideal case class E power amplifier

At first, the output node Vo is described in (2.14). And we get Io in (2.15). The voltage of the shunt capacitor Vc can be calculated through (2.16) to (2.18). In order to get c_1, we use the Fourier integral as shown in (2.19) and (2.20). Equation (2.21) and (2.22) show the results of the Fourier integral. Because RF choke has no voltage drop, the average voltage of Vc is Vcc. Therefore we can get equation (2.23). By the equation (2.23), we can define the equal load resistance R_{DC} measured from the power supply. According to this, the output AC power can be shown in (2.24). The overall drain efficiency η also can be shown in (2.25). The amplitude A of output waveform equals a constant c.

$$V_O(\theta) = c\sin(\omega t + \varphi) = c\sin(\theta + \varphi) \tag{2.14}$$

$$i_O(\theta) = \frac{V_O(\theta)}{R_L} = \frac{c}{R_L}\sin(\theta+\varphi) \quad where \begin{cases} c: output\ voltage\ magnitude \\ \varphi: phase\ difference\ at\ output \end{cases} \tag{2.15}$$

$$V_c(\theta) = \frac{1}{B}\int_0^{\theta} I_C(u)du \tag{2.16}$$

$$I_c(u) = I_t - I_O(u) = I_t - \frac{c}{R_L}\sin(u+\varphi) \tag{2.17}$$

$$\therefore V_c(\theta)=\frac{I_t}{B}\theta+\frac{c}{BR_L}[\cos(\theta+\varphi)-\cos\varphi],\ \mathrm{B}\triangleq\omega c_{shunt} \tag{2.18}$$

$$\begin{cases} c_1=\dfrac{1}{\pi}\int_0^{2\pi}V_c(\theta)\sin(\theta+\varphi_1)d\theta & (2.19)\\ 0=\dfrac{1}{\pi}\int_0^{2\pi}V_c(\theta)\cos(\theta+\varphi_1)d\theta & (2.20)\end{cases}$$

$$c=I_t\cdot R_L\cdot\frac{\pi\cos\varphi_1-2\sin\varphi_1}{\pi BR_L\rho-\frac{\pi}{2}\sin\psi+2\cos\varphi\cos\varphi_1}\triangleq I_t\cdot R_L\cdot h(\varphi,\psi,B,R_L,P)\ where\ c_1=\rho c \tag{2.21}$$

$$c=I_t\cdot R_L\cdot\frac{\pi\sin\varphi_1+2\cos\varphi_1}{2\cos\varphi\sin\varphi_1+\frac{\pi}{2}\cos\psi}\triangleq I_t\cdot R_L\cdot g(\varphi,\psi)\ \ where\ \ \psi=\varphi_1-\varphi \tag{2.22}$$

$$V_{cc}=\frac{1}{2\pi}\int_0^{2\pi}V_c(\theta)d\theta=I_t\cdot\frac{1}{2\pi B}[\frac{\pi^2}{2}-2g\sin\varphi-\pi g\cos\varphi]\triangleq I_t\cdot R_{DC} \tag{2.23}$$

$$P_{out}\triangleq\frac{(c/\sqrt{2})^2}{R_L}=\frac{1}{2}\frac{c^2}{R_L}=\frac{1}{2}\cdot I_t^{\,2}g^2R_L=\frac{V_{cc}^{\,2}g^2R_L}{2R_{DC}^2} \tag{2.24}$$

$$\eta\triangleq\frac{P_{out}}{P_{DC}}=\frac{g^2}{2}\cdot\frac{R_L}{R_{DC}} \tag{2.25}$$

According to the class E power amplifier boundary equation, we can get equation (2.26) and (2.27). We can get (2.28) from (2.26) and (2.29) from (2.27). So the ϕ equals -32.482^0 or -0.5669 rad. Because the ideal drain efficiency of class E power amplifier η is 100 %, we can get a group of initial design values through (2.30) to (2.36).

$$\begin{cases} V_c(\theta)\big|_{\theta=\pi}=0 & (2.26)\\ \left.\dfrac{dV_c(\theta)}{d\theta}\right|_{\theta=\pi}=0 & (2.27)\end{cases}$$

$$\cos\varphi=\pi/2g \tag{2.28}$$

$$\sin\varphi=-1/g \tag{2.29}$$

$$\varphi=\text{-}32.482^0=\text{-}0.5669\ \text{rad} \tag{2.30}$$

$$R_{DC}=\frac{1}{\pi B}=1.7337R_L \tag{2.31}$$

$$B=\frac{1}{5.4466R_L} \tag{2.32}$$

$$\psi=49.052^0=0.85613\ \text{rad} \tag{2.33}$$

$$X=1.1525R_L \tag{2.34}$$

$$V_c(\theta)_{max}=3.562V_{cc} \tag{2.35}$$

$$c=1.074V_{cc} \tag{2.36}$$

Next, the transistor turn-on resistance should be considered and the modified design steps could be provided. These design steps are also shown below. The load network of Ron case class E power amplifier is shown in Fig. 2-12.

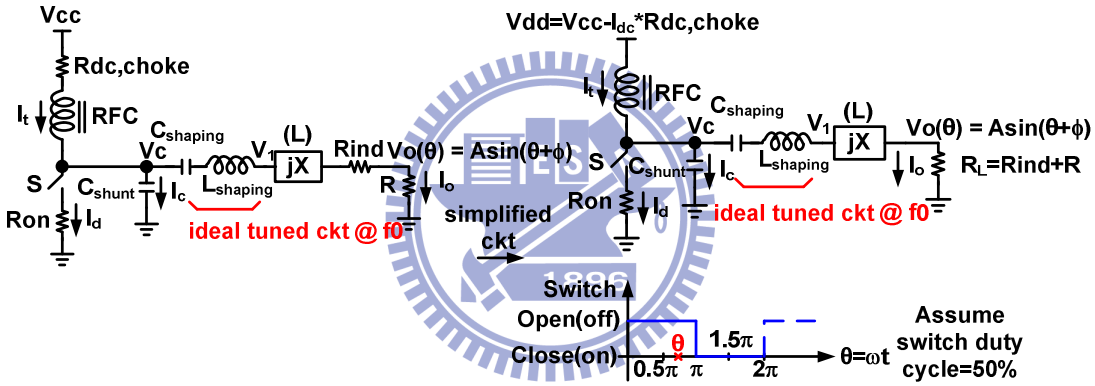


Fig. 2-12 The load network of Ron case class E power amplifier

At first, the output node Vo also can be described in (2.37). Therefore we get Io in (2.38). So the node V1 can be described in (2.39). Because the transistor has the on state and off state, the voltage of the shunt capacitor Vc can be calculated in two equations (2.40) and (2.41). According to the two boundary equations (2.42) and (2.43), we can get (2.44). The amplitude A of output waveform equals a constant c.

$$V_o(\theta)\triangleq c\sin(\theta+\varphi) \tag{2.37}$$

$$i_o(\theta)=\frac{V_o(\theta)}{R_L}=\frac{c}{R_L}\sin(\theta+\varphi) \tag{2.38}$$

$$V_1(\theta) = c\sin(\theta+\varphi) + jX\frac{c}{R_L}\sin(\theta+\varphi) = c_1\sin(\theta+\varphi_1)$$

$$where\begin{cases} c_1 = c\cdot\sqrt{1+(\frac{X}{R_L})^2} \triangleq \rho c \\ \varphi_1 = \tan^{-1}\frac{X}{R_L}+\varphi \qquad , \ \rho = \sqrt{1+(\frac{X}{R_L})^2} = \sqrt{1+\tan^2\psi} \\ \psi \triangleq \tan^{-1}\frac{X}{R_L} \end{cases} \quad (2.39)$$

$$V_{c,on} = [I_t - \frac{c}{R_L}\sin(\theta+\varphi)]\times R_{on} \quad (2.40)$$

$$V_{c,off} = \frac{1}{B}\int_0^\theta I_c(u)du = \frac{1}{B}\int_0^\theta [I_t - \frac{c}{R_L}\sin(u+\varphi)]du = \frac{I_t}{B}\theta + \frac{c}{BR_L}\cdot[\cos(\theta+\varphi)-\cos\varphi] \quad (2.41)$$

$$V_{c,off}(\theta=0) = V_{c,on}(\theta=2\pi) \quad (2.42)$$

$$V_{c,off}(\theta=\pi) = V_{c,on}(\theta=\pi) = 0 \quad (2.43)$$

$$V_c(\theta) = \begin{cases} [I_t - \frac{c}{R_L}\sin(\theta+\varphi)]\times R_{on}, \ \pi \le \theta \le 2\pi \\ \frac{I_t}{B}\theta + \frac{c}{BR_L}\cdot[\cos(\theta+\varphi)-\cos\varphi] + R_{on}[I_t - \frac{c}{R_L}\sin\varphi], \ 0 \le \theta \le \pi \end{cases} \quad (2.44)$$

Next, we also use the Fourier integral to get c_1 which is described through (2.45) to (2.48). For high efficiency of class E power amplifier, $V_c(\theta=\pi)$ equals zero at the instant that the transistor turns on as shown in (2.49). Therefore we can get equations (2.50) and (2.51). For high efficiency of class E power amplifier, $dV_c(\theta)/d\theta$ at $\theta=\pi$ equals zero. As a result, we can get equation (2.52). And the average voltage of $V_c(\theta)$ equals V_{cc}', equation (2.53) can be obtained. According to (2.53), we can define the dc resistance R_{DC} in (2.54). Through (2.50) to (2.52), the dc resistance R_{DC} can be derived in (2.55).

$$c = I_t R_{eq}\frac{\pi\cos\varphi_1 - 2\sin\varphi_1}{\rho\pi BR_L - \frac{\pi}{2}\sin\psi + 2\cos\varphi\cos\varphi_1 + 2BR_{on}\sin\varphi\cos\varphi_1 + \frac{\pi}{2}BR_{on}\cos\psi} \quad (2.45)$$

$$c \triangleq I_t\cdot R_L\cdot h(\varphi,\psi,B,R_L,R_{on},\rho) \quad (2.46)$$

$$c = I_t R_L \frac{\pi \sin\varphi_1 + 2\cos\varphi_1}{\frac{\pi}{2}\cos\psi + 2\cos\varphi \sin\varphi_1 + 2BR_{on}\sin\varphi\sin\varphi_1 + \frac{\pi}{2}BR_{on}\sin\psi} \quad (2.47)$$

$$c \triangleq I_t \cdot R_L \cdot g(\varphi, \psi, B, R_{on}) \quad (2.48)$$

$$V_{c,off}(\pi) = 0 = V_{c,on}(\pi) \quad (2.49)$$

$$\begin{cases} g = \dfrac{\pi + BR_{on}}{BR_{on}\sin\varphi + 2\cos\varphi} & (2.50) \\ I_t = -\dfrac{c}{R_L}\sin\varphi & (2.51) \end{cases}$$

$$g = h = -\frac{1}{\sin\varphi} \quad (2.52)$$

$$V_{cc}' = \frac{1}{2\pi}\int_0^{2\pi} V_c(\theta)d\theta = \frac{1}{2\pi}\int_0^{\pi} V_{c.off}(\theta)d\theta + \frac{1}{2\pi}\int_{\pi}^{2\pi} V_{c.on}(\theta)d\theta \quad (2.53)$$

$$R_{DC} = \frac{1}{2\pi B}[\frac{\pi^2}{2} + 2\pi BR_{on} - g\sin\varphi(2 + \pi BR_{on}) - g\cos\varphi(\pi - 2BR_{on})] \quad (2.54)$$

$$R_{DC} = \frac{1}{2\pi B}[2 + BR_{on}(2BR_{on} + 3\pi)] \quad (2.55)$$

According to the above equations, we can build up a design flow by iteration method to design our circuits. The design flow is shown below. First, the output power level should be set up. Second, we should overdesign our circuits to prevent parasitic effect. Third, we can figure out the initial design parameters from ideal case. Fourth, we can use equations (2.50) to (2.52) to get an initial design parameter $\phi_{initial}$. Fifth, according to this design parameter $\phi_{initial}$ value, we can get some other design parameter such as ϕ and ρ. Sixth, we can define an error value ε between the left and the right of the identically equal equation form our calculate process. Seventh, we can set up the error ε tolerate value. The set up error ε tolerate value which we define is ε_0. The error ε tolerate value ε_0 is as small as possible. Eighth, if the absolute value of ε is smaller or equal than ε_0, the design parameter B and ϕ are got with the designed parameters such as R, R_{on}, and f. If the absolute value of ε is larger than ε_0, it describes

that the iteration is not convergence. According to this, the iteration should be continued until the iteration is convergence. Ninth, in accordance with every R_{on}, we can build up a design table. Tenth, we can design a matching network to transform the 50 Ω terminal to R_{on}. Eleventh, because of parasitic resistance of tank circuit, it will produce appended power loss. And the quality factor of the tank is defined as Q_{tank}. And the quality factor of the load R of the LC tank is defined as loaded-Q, Q_L. When the Q_{tank} increases, the power loss decreases. Therefore, the quality factor of inductor must be high enough. And the bandwidth of the class E PA is depended on the Q_L. At the same time, the L_{tank} and C_{tank} are resonated at operating frequency. Twelfth, to consider the MOS drain capacitor C_j, there are two ways to design our circuit. If the shunt-to-ground capacitor C_{shunt} is larger than C_j, we must shunt capacitor at the drain terminal of MOS to compensate. If the shunt-to-ground capacitor C_{shunt} is smaller than C_j, we must shunt inductor at the drain terminal of MOS to compensate. Thirteenth, we merge all the components and achieve final class E PA.

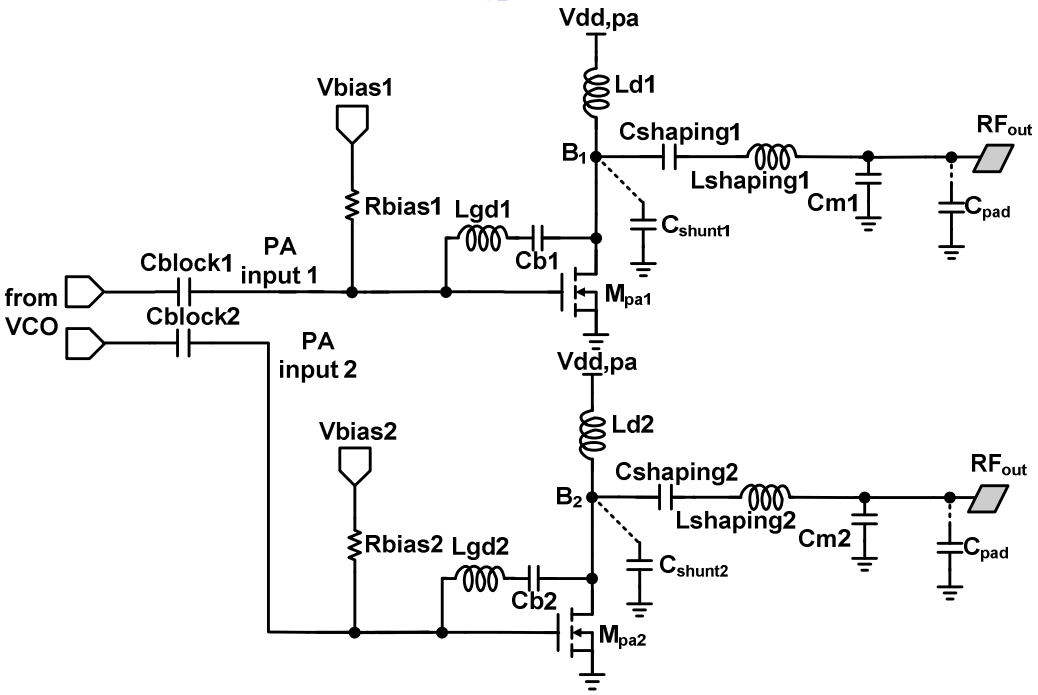


Fig. 2-13 Schematic of designed power amplifier

Shown in Fig. 2-13 is the designed power amplifier. The proposed PA consists of two push-pull amplifiers to amplify the signal which comes from the voltage-controlled oscillator.

By (2.2)-(2.3), the transistors' dimensions and optimal load resistance can be roughly predicted by hand calculation. Because the biasing is fixed to threshold voltage and V_{DD}, the variable for transistor itself is size. The transistor's size of class E power amplifier is determined by the required output power.

Two on-chip inductors, L_{d1} and L_{d2}, are used to resonate out the parasitic capacitance of the drain (that is, node B_1 and B_2) and to bias the drain DC voltage to V_{DD}. Because of large size transistors and resultant seriously parasitic capacitance, two on-chip inductors, L_{gd1} and L_{gd2}, are used to resonate out the gate-drain parasitic capacitance $C_{gd,Mpa1}$ and $C_{gd,Mpa2}$ of transistors M_{pa1} and M_{pa2}, respectively.

The inductors L_{d1} and L_{d2}, which are used for resonating parasitic capacitance of the internal nodes of power amplifier (B_1 and B_2), are determined and simulated with core circuit of power amplifier during the load-pull analysis. When the inductors L_{d1} and L_{d2} are modified, the output impedance transformation network which is determined by load-pull analysis will be affected. However, the chosen Z_L and its corresponding transformation network are for previous circuit – core circuit of PA with non-modified inductors, load-pull analysis has to be simulated again for modified inductors. Therefore the load-pull analysis has to be simulated again as long as any part of circuit is modified; iterative simulations may be needed to determine the values of resonated inductors and output impedance transformation network. For iterative procedure, it is endless if it is not convergent. From this point of view, the better way is to increase reverse isolation so that these resonated inductors need no any modification when the output impedance transformation network is connected to the circuit. That is the reason why both two inductors (L_{gd1} and L_{gd2}) are used between

gate-drain for both stages of PA.

Two capacitors, C_{b1} and C_{b2}, are adopted to cut out unnecessary DC paths provided by L_{gd1} and L_{gd2}. To consider the stability effect, the k and b stability factor are shown in Fig. 2-14 – 2-15. The stability factor (k factor) is described in (2.56). And the stability means (b factor) is also described in (2.58). The output impedance transformation network is composed of $C_{shaping}$, $L_{shaping}$, C_m and the parasitic capacitance of the output pad C_{pad}.

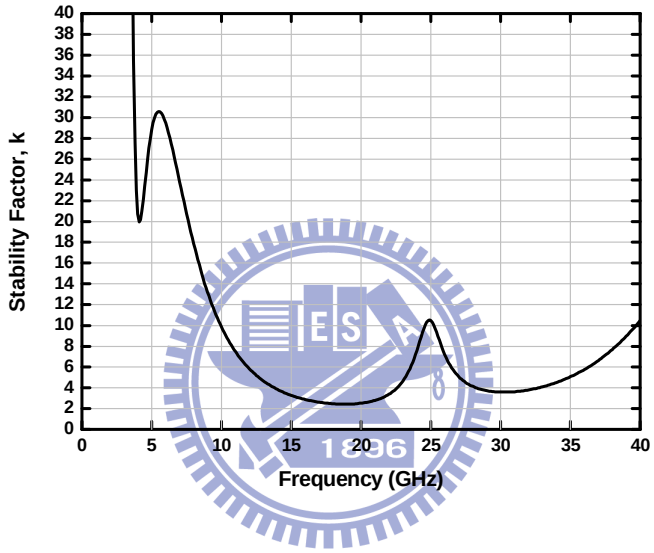


Fig. 2-14 Stability factor (k factor)

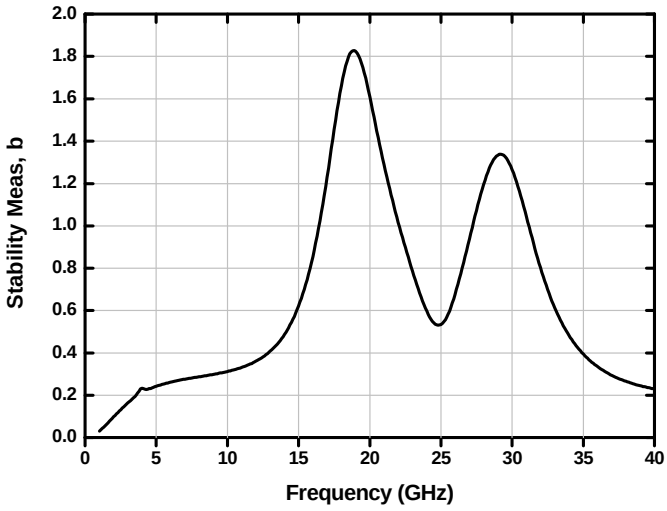


Fig. 2-15 Stability means (b factor)

$$k = \frac{1 - |S11|^2 - |S22|^2 + |\Delta|^2}{2|S12S21|} \tag{2.56}$$

$$\Delta = S11S22 - S12S21 \tag{2.57}$$

$$b = 1 + |S11|^2 - |S22|^2 - |\Delta|^2 \tag{2.58}$$

In order to minimize chip area, internal nodes such as PA's input (connected to VCO) are not implemented any matching networks. Instead, shunt inductors are adopted to resonate out the parasitic capacitance of these nodes. Because any parasitic capacitance is equivalent as a short path for high frequency, it may degrade RF signal by leakage RF signal to ground. The output node, however, is connected to external 50-Ω impedance probe during measurement. Therefore, output transformation network is needed and implemented by load-pull analysis. Fig. 2-16 is the constant P_{out}, constant PAE contours and the chosen Z_L by trade-off between them. Fig. 2-17 is the impedance transformation network, which transfers 50-Ω port to chosen Z_L determined by the load-pull analysis. The transferred load impedance seen by power amplifier is shown in Fig. 2-18.

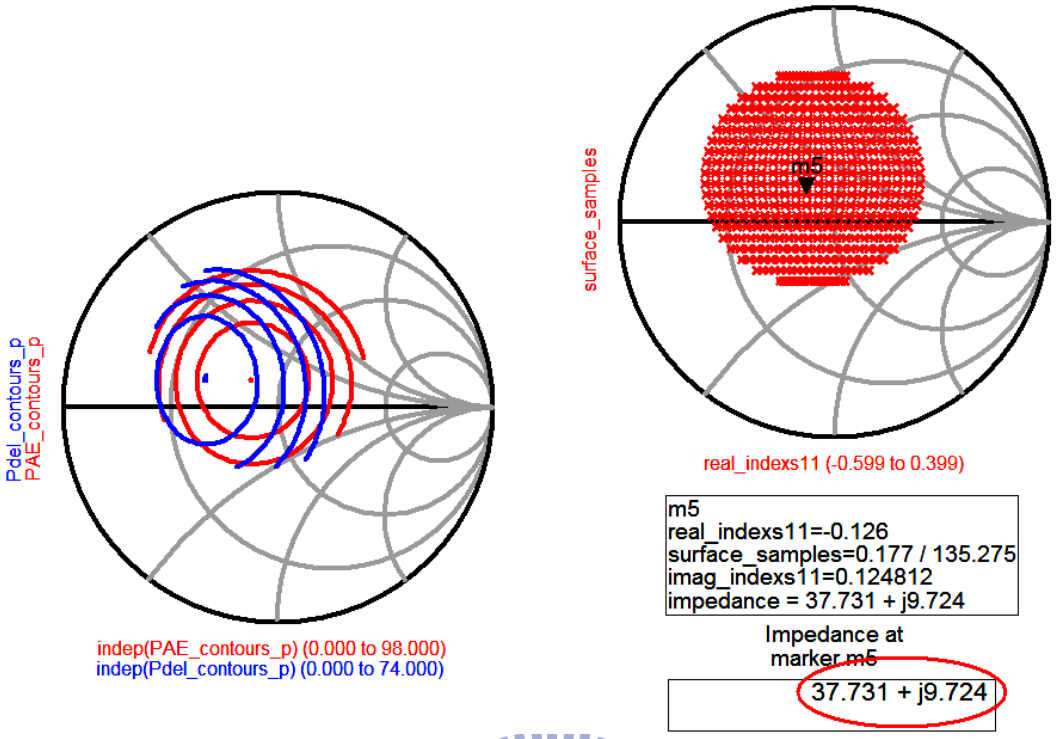


Fig. 2-16 Constant P_{out} constant PAE contours and the chosen Z_L

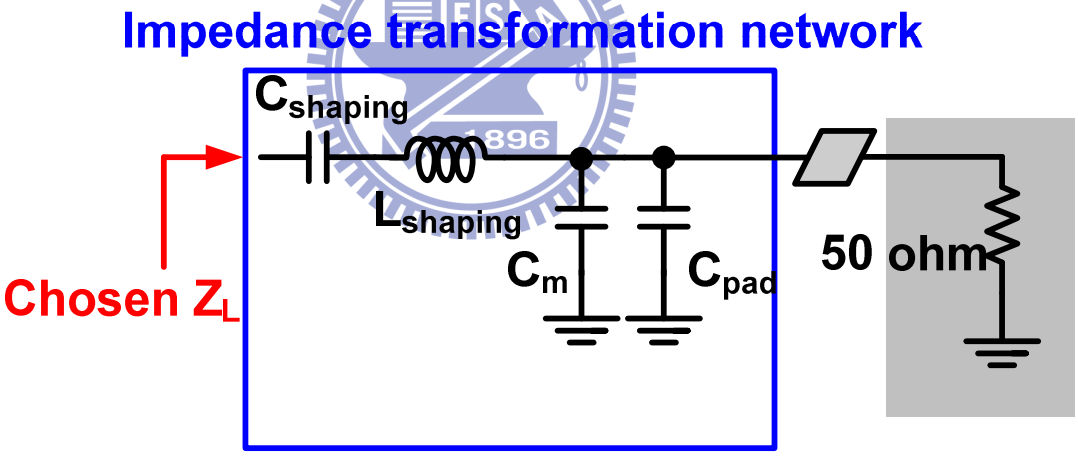


Fig. 2-17 Impedance transformation network of power amplifier

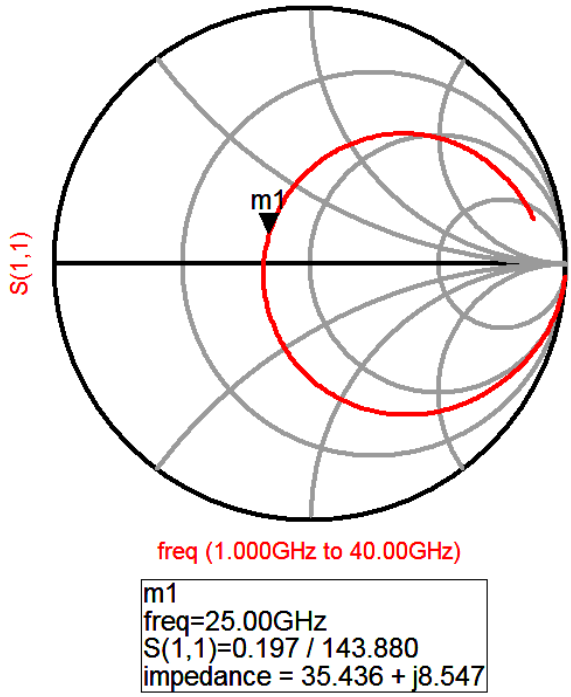


Fig. 2-18 Load impedance transferred by transformation network

2.2.2. Voltage-Controlled Oscillator with Cascode Buffer

We can design a voltage-controlled oscillator as a voltage source of class E power amplifier. There are several ways to build a VCO. In research work, we adopt the LC tank VCO which has the best normalized phase noise compared to other fully integrated structures like ring oscillators, relaxation oscillators, and g_m-C oscillators. In other words, this architecture has the lowest phase noise for a given amount of power. The various VCO constructed by modern CMOS technology are also reported. Due to the lack of high Q elements in the conventional CMOS technology, the differential oscillator feature is the mostly often-used configuration.

LC-tank voltage-controlled oscillators are designed in NMOS cross-coupled pair with an inductor L in parallel with a capacitor C resonates at a center frequency and a PMOS current source. The design of LC-tank VCO is shown in Fig. 2-19.

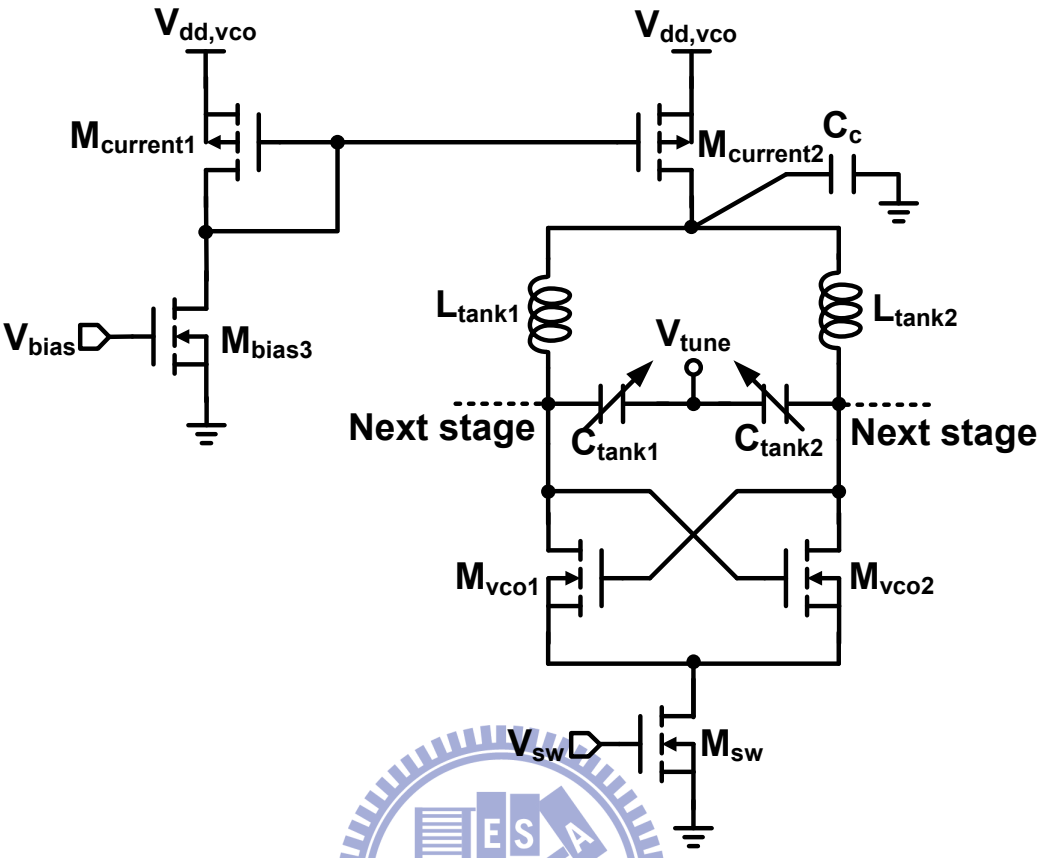


Fig. 2-19 The design of LC-tank VCO

A NMOS cross-coupled pair can provide a negative impedance to compensate the loss of the tank and other parasitic impedance to sustain the oscillation. This circuit is the well-known "negative-G_m oscillator". And then the different ideal current sources are used to obtain the different biased currents of VCO, the appropriate size of CMOS and values of inductors and capacitors.

The active devices provide a negative resistance to cancel the loss of the tank. We should optimize these effects of these devices such as: (1) quality factor (2) gain of MOS (3) all capacitance of device (4) varactor (5) phase noise (6) effects of pulling or pushing frequency. There are many relations between any effects and a tradeoff each other.

The maximal energy stored in the inductor must equal the maximal energy stored in the capacitor as:

$$\frac{C_{tank}V_{peak}^{\ 2}}{2}=\frac{L_{tank}I_{peak}^{\ 2}}{2} \tag{2.59}$$

Where the V_{peak} is the peak voltage amplitude of the capacitor and I_{peak} is the peak current amplitude of the inductor. And then the loss in the tank is:

$$P_{loss}=RC_{tank}^{\ 2}\omega_c^{\ 2}V_{peak}^{\ 2}=\frac{R}{L_{tank}^{\ 2}\omega_c^{\ 2}}V_{peak}^{\ 2} \tag{2.60}$$

Where the ω_c is the center frequency of the LC tank. According to (2.60), the power loss decreases linearly for lower series resistances R in the resonance tank. The tank inductance (L) can be increased and the power consumption will decrease.

The most important design issue in the cross-coupled pair NMOS is to ensure that the negative impedance is enough to sustain the oscillation. The channel length is set to minimum to reduce parasitic capacitance to achieve the highest trans-conductance. Because of the channel length modulation, the phase noise sideband near the center frequency is made by the noise of harmonics mixed with fundamental oscillation frequency. Therefore, we use bypass capacitor C_c to filter out the second harmonic tone of the center frequency which is composed of PMOS current source and cross-coupled pair NMOS. It is in order to avoid the second harmonic tone of the center frequency to mix up with the center frequency. By using bypass capacitor C_c, it also can make sure that the connected node is a perfect AC ground. And the design of voltage-controlled oscillator with cascode buffer is shown in Fig. 2-20.

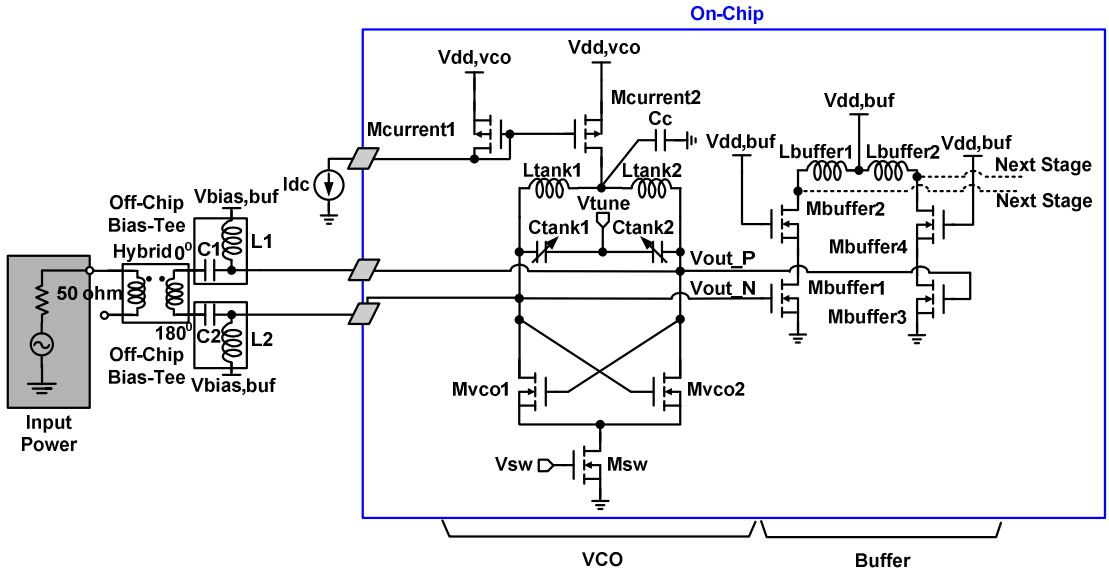


Fig. 2-20 The design of voltage-controlled oscillator with cascode buffer

In order to measure the cascode buffer and class E power amplifier performance, we use a hybrid component at the input to divide the input power signal path into two paths. And we use two Bias-Tees to bias the common source transistors of cascode buffer. But it will form a serious problem. When we bias as that, the Bias-Tee circuits also turn on the cross-coupled pair NMOS. It will provide a signal loss path. Therefore, we add a large size NMOS Msw at the bottom of the cross-coupled pair NMOS to cut off the signal loss path. In normal case, Vsw will be biased at Vdd,vco. In such case, Vsw will be biased at ground. At the output node of voltage-controlled oscillator, we add a cascode buffer to provide enough reverse isolation between voltage-controlled oscillator and class E power amplifier. It also provides gain at the same time.

2.2.3. Class E Power Amplifier Integrated with Voltage-Controlled Oscillator

Shown in Fig. 2-21 are the integrated whole circuits which consist of a differential voltage-controlled oscillator integrated with cascode buffer and a push-pull pair class E power amplifier. The dimensions and functions of other components are described as mention in section 2.2.1 and 2.2.2.

L_1, L_2, C_1 and C_2 are the equivalent circuit of two off-chip Bias-Tees for testing the cascode buffer with power amplifier. The off-chip hybrid is used to transform single-ended RF signal to differential one. The output impedance transformation network which consists of $L_{shaping}$, $C_{shaping}$, C_m, and parasitic capacitance of RF output PAD (C_{pad}) is designed through the load-pull analysis.

The effective schematic diagram which includes routing effect after layout is shown in Fig. 2-22. High-frequency electro-magnetic (EM) effect of routing has been simulated individually by EM-simulated EDA tool named HFSS. There are several sections, such as the inter-stage of VCO–PA, the drain of power amplifier, and the node between impedance transformation network and RF output pad. The routing effect of inter-stage node comes from the distance between voltage-controlled oscillator and power amplifier; others are connected by long wire because of the guard-ring of inductance. These wire connections are longer than λ/10 that their EM effect can not be neglected, thus they are simulated by HFSS and modeled by the S2P file (2-port network). The other one is the input port of RF signal for testing the cascode buffer with power amplifier. Two S2P files consist of wire connected from the gate of $M_{buffer3}$ to RF+ PAD for positive path and $M_{buffer1}$ to RF– PAD for opposite path. The last one is the three-port network which locates at the gate terminal of power amplifier. The output transformation network which includes some S2P files can transfer 50-Ω impedance of output port to desired impedance as shown in Fig. 2-19. The procedure and model view for EM analysis are illustrated in Fig. 2-23. Dimension for all components are summarized in Table 2.1 and Table 2.2.

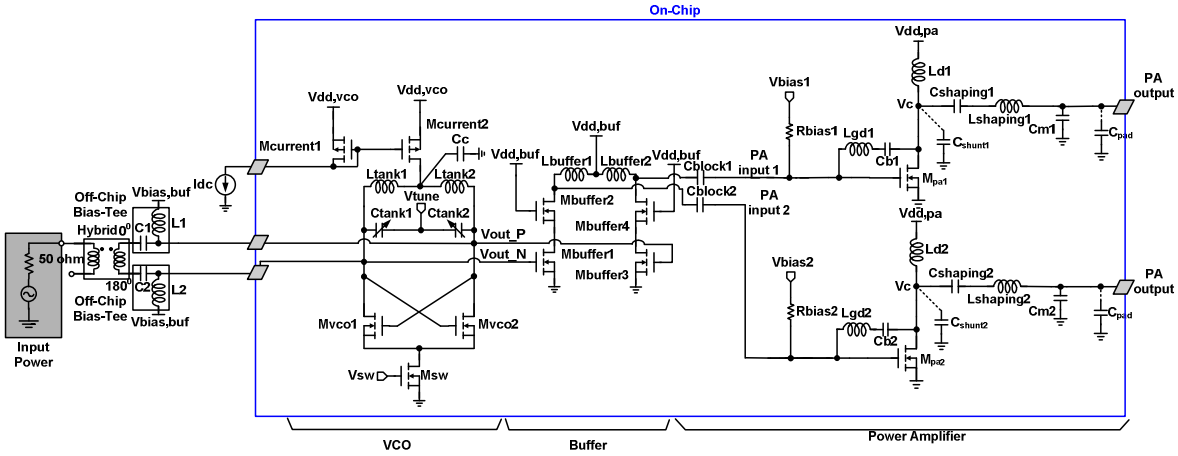


Fig. 2-21 Schematic of designed whole circuits

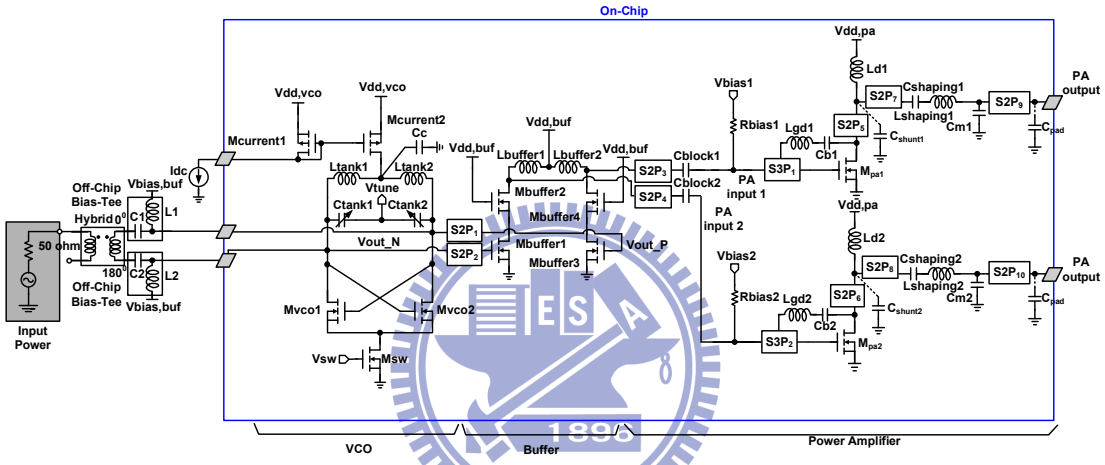


Fig. 2-22 Schematic of designed whole circuits

(with parasitic routing effect)

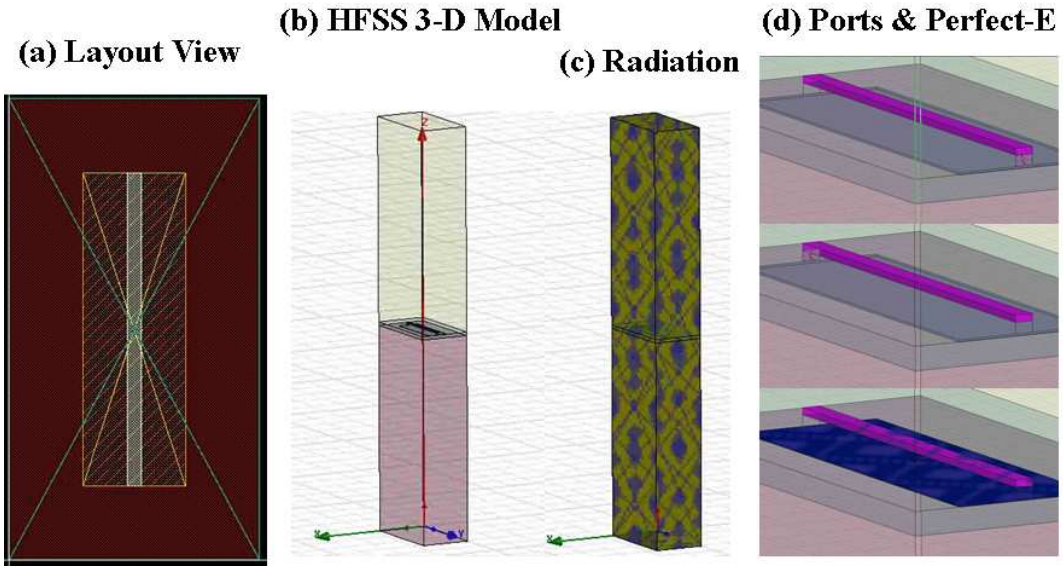


Fig. 2-23 Layout, 3-D model and setting for EM analysis (2-port networks)

Table 2-1 Summaries of device value

	Dimension (μm)
M_{pa1}	5*30/0.13
M_{pa2}	5*30/0.13
$M_{current1}$	3*20*1/0.35
$M_{current2}$	3*20*7/0.35
M_{vco1}	3*8/0.13
M_{vco2}	3*8/0.13
M_{sw}	3*40/0.13
$M_{buffer1}$	3*10/0.13
$M_{buffer2}$	3*8/0.13
$M_{buffer3}$	3*10/0.13
$M_{buffer4}$	3*8/0.13

	Value
L_{gd1}–L_{gd2}	827.1 pH
L_{d1}–L_{d2}	395.9 pH
$L_{shaping1}$–$L_{shaping2}$	868.2 pH
L_{tank1}–L_{tank2}	270 pH
$L_{buffer1}$–$L_{buffer2}$	270 pH
$V_{dd,vco}$; $V_{dd,buf}$; $V_{dd,pa}$	1.2 V
V_{bias1}-V_{bias2}	0.3 V
I_{dc}	0.6 mA

	Value
R_{bias1}–R_{bias2}	10 Kohm
C_{b1}–C_{b2}	1.38 pF
$C_{shaping1}$–$C_{shaping2}$	70.1 fF
C_{m1}–C_{m2}	109.1 fF
C_{pad}	30 fF
C_{block1}–C_{block2}	0.997 pF
C_c	2.5 pF
C_{tank1}–C_{tank2}	8-18 fF

Table 2-2 Dimension summaries of transmission line

Transmission Line	Width (μm)	Length (μm)
$S2P_1$	6	33.95+75.62+105.05
$S2P_2$	6	41.3+50.51+95.4
$S2P_3$	6	32.37+22.94
$S2P_4$	6	37.22
$S2P_5$	6	112.31+50.8
$S2P_6$	6	112.31+50.8
$S2P_7$	6	77.29+5.64
$S2P_8$	6	77.29+5.64
$S2P_9$	6	35
$S2P_{10}$	6	35
$S3P_1$	6	149.98+62.65+9.49
$S3P_2$	6	149.98+62.65+9.49

2.3. Post-Simulation Results

The *K*-Band integrated transmitter circuits are designed in 0.13-μm 1P8M CMOS technology. And the TSMC 1.2 V NMOS with DNW components are used. From the supply voltage of 1.2 V, the current consumption of the LC tank voltage-controlled oscillator, cascode buffer and class E PA are 4.8 mA, 7.97 mA and 25.91 mA, respectively. The total power dissipation is 46.42 mW.

With and without neutralization technique analysis, neutralization technique phase shift, neutralization technique phase shift effect, drain voltage and current waveforms, large signal S-parameter (LSSP), output power (P_{out}) and PAE versus input power (P_{in}) of re-matching stand-alone class E power amplifier presented by post-simulation are illustrated in Fig. 2-24, Fig. 2-25, Fig. 2-26, Fig. 2-27, Fig. 2-28, and Fig. 2-29, respectively. As shown in Fig. 2-24, the S12 of re-matching stand-alone class E power amplifier presented by post-simulation with neutralization technique analysis at 25 GHz equals -23.6 dB which has better performance than the S12 which equals -7.8 dB of that without neutralization technique analysis. Therefore, the neutralization technique can improve the reverse isolation of class E power amplifier. As shown in Fig. 2-25, we can find that the neutralization technique phase shift (fundamental tone 25 GHz) equals 1.9 degree. As shown in Fig. 2-26, the 1.9 degree neutralization technique phase shift can improve PAE (7.49 %) and output power (0.72 dB). As shown in Fig. 2-27, we can find that it still has overlapping waveform and DC power consumption. The overlapping waveform is formed by the parasitic effect which can provide phase shift on the drain voltage and current waveforms. And the DC power consumption is formed by the turn-on resistance effect which can provide a DC voltage on the drain voltage waveform. Meanwhile, the switch waveform is not a square-wave because that the input signal comes from VCO. Due to turn-on resistance and parasitic effect, the ZVS and ZDS points are not exactly on

the point when the switch turns on. And the peak voltage value is about 1.81 Vdd. The peak voltage value does not exceed the breakdown voltage of MOS component. Therefore, it is still a reliable and stable design. According to Fig. 2-28, the large signal S-parameter of re-matching stand-alone class E PA has S11 of –8.6 dB, S12 of –23 dB, S21 of 4.9 dB, and S22 of –4 dB at 25 GHz. Due to the re-matching, the S11 has a good performance. When we simulate the large signal S-parameter, we define the input (4 dBm) and output power (10.49 dBm) of the input and output terminal at the same time. Because the class E PA operates in large signal, the S21 has positive gain. Because of the load-pull analysis, the S22 will not be matched to 50 ohm terminal. "P_{out} versus P_{in}", "PAE versus P_{in}" and "Drain Efficiency versus P_{in}" curves in Fig. 2-29 show this power amplifier has variable power gain because class E power amplifier is a kind of nonlinear power amplifier. The maximum PAE is 38.67 % at the input power of 4 dBm and output power of 10.49 dBm.

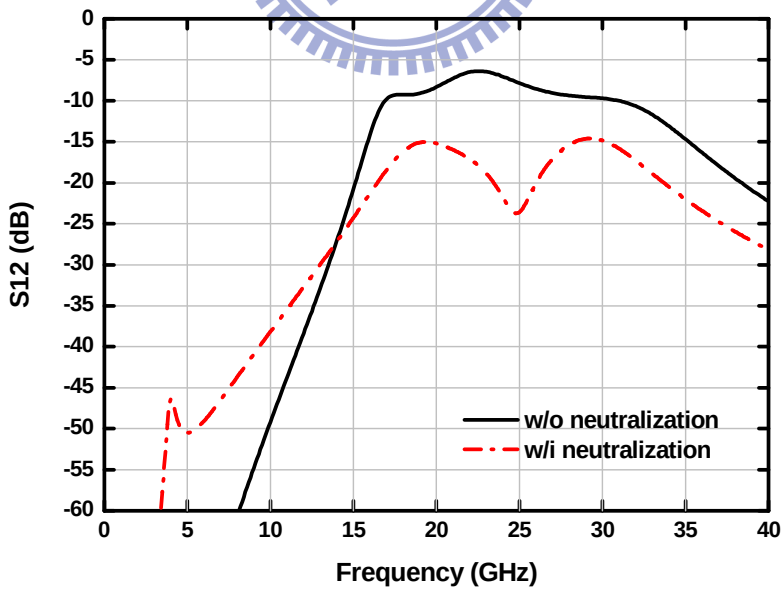


Fig. 2-24 With and without neutralization technique analysis of re-matching stand-alone class E power amplifier

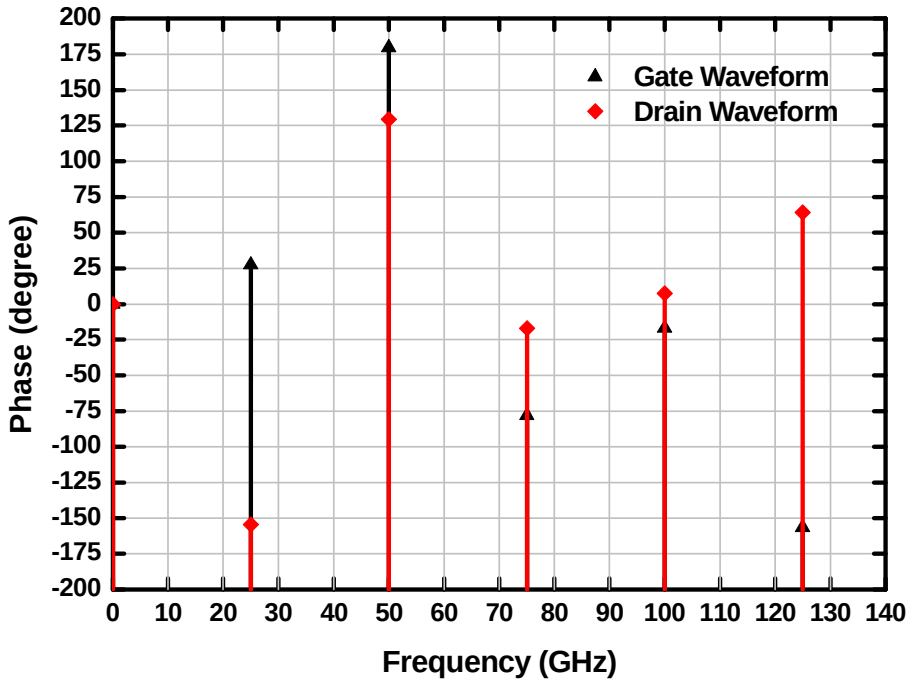


Fig. 2-25 Neutralization technique phase shift of re-matching stand-alone class E power amplifier

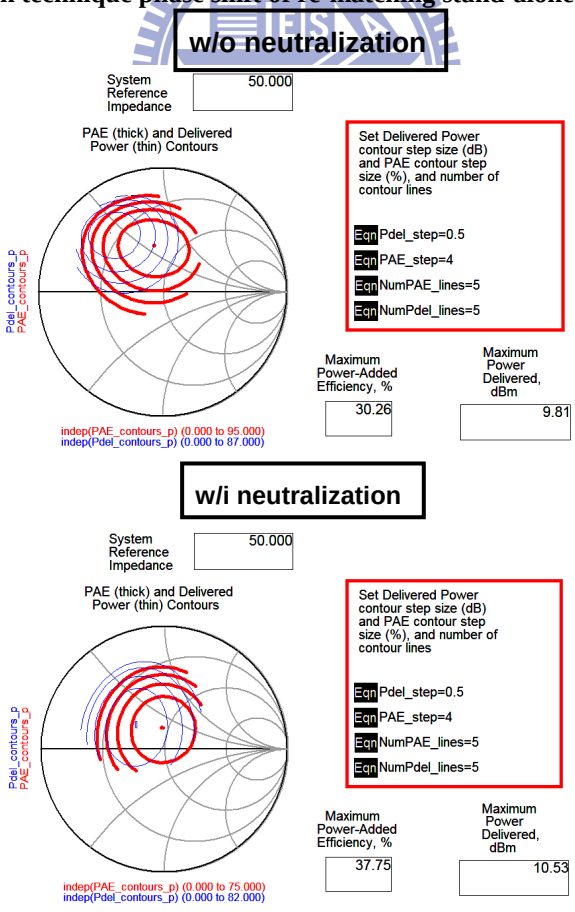


Fig. 2-26 Neutralization technique phase shift effect

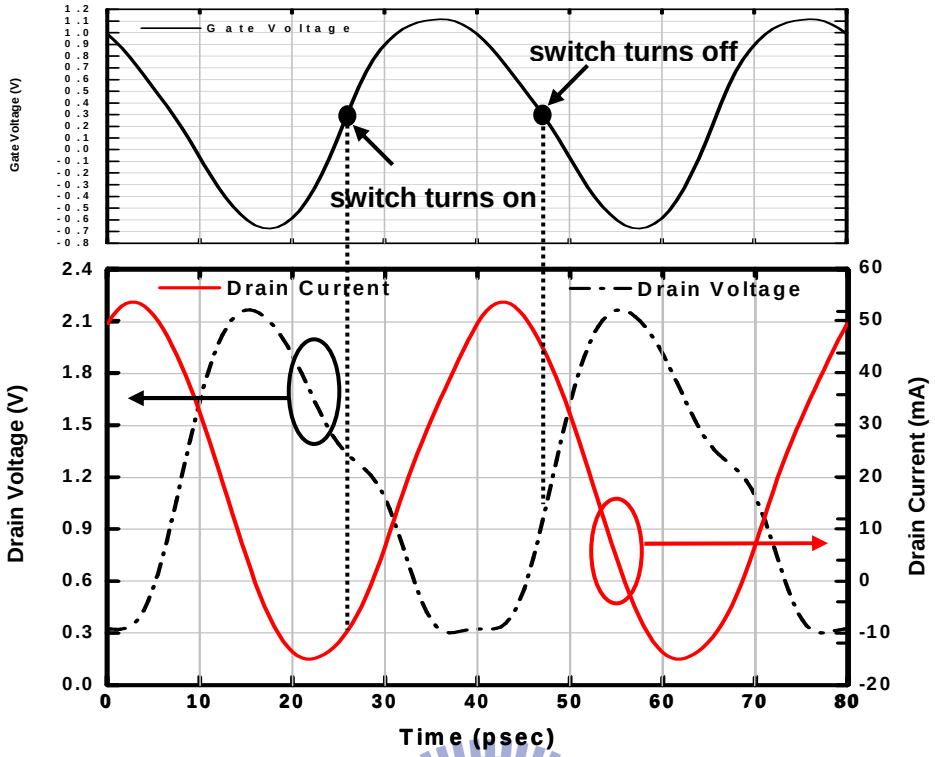


Fig. 2-27 Drain voltage and current waveforms with gate voltage waveform of re-matching stand-alone class E power amplifier

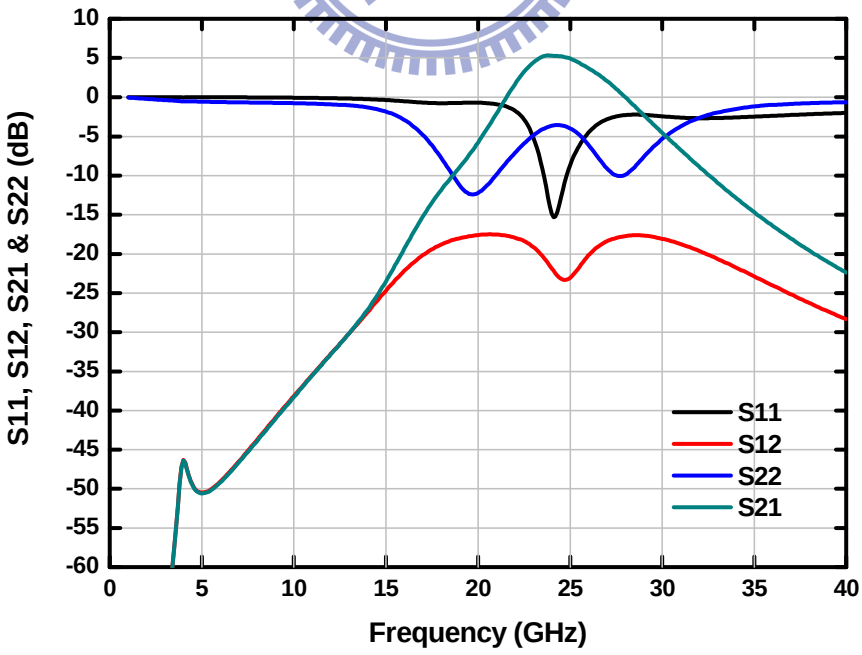


Fig. 2-28 Large signal S-parameter (LSSP) for re-matching stand-alone class E power amplifier

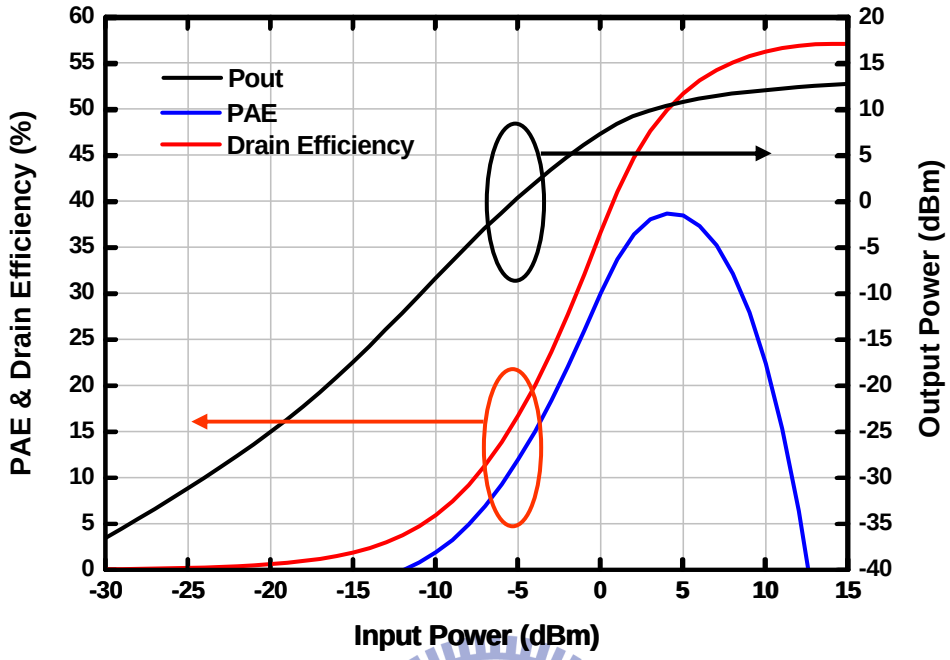


Fig. 2-29 P_{out} vs P_{in}, PAE vs P_{in} and Drain Efficiency vs P_{in} for re-matching stand-alone class E power amplifier

Fig. 2-30–Fig. 2-31 show the post-simulation performance of voltage-controlled oscillator and cascode buffer with the loading equaled to the PA's input impedance.

Fig. 2-30 is the tuning range of voltage-controlled oscillator. When the tuning voltage changes from 0 V to 1.2 V, the frequency changes from 23.99 GHz to 24.79 GHz. Therefore, the tuning range of voltage-controlled oscillator is 0.8 GHz.

Fig. 2-31 is the phase noise of voltage-controlled oscillator. From this figure, it's obvious that the chosen bypass capacitor C_c and PMOS current source can improve the phase noise of voltage-controlled oscillator. Therefore, the phase noise of voltage-controlled oscillator is -117 dBc at 10 MHz.

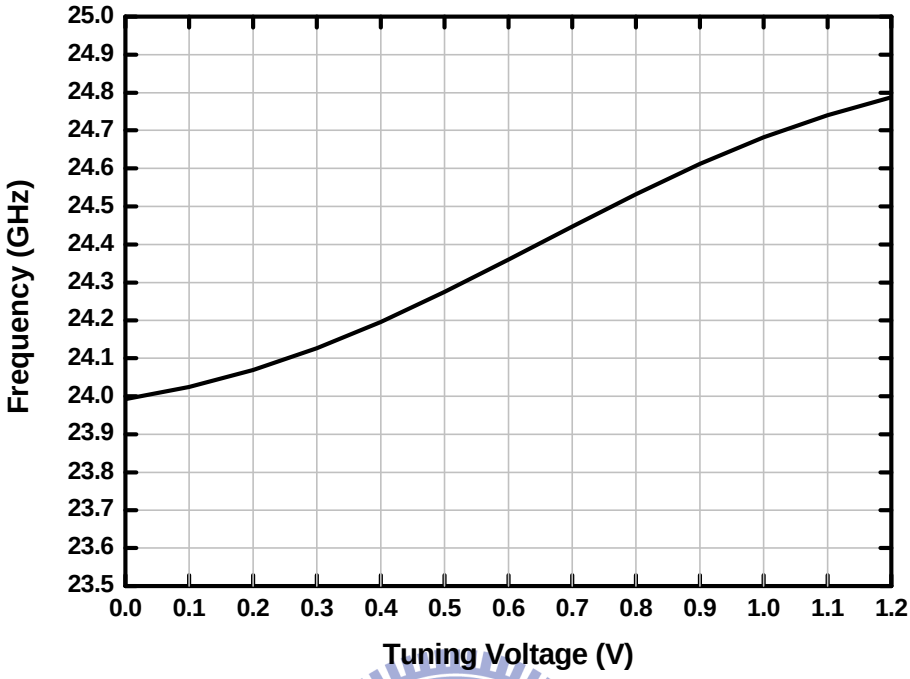


Fig. 2-30 Tuning range of voltage-controlled oscillator

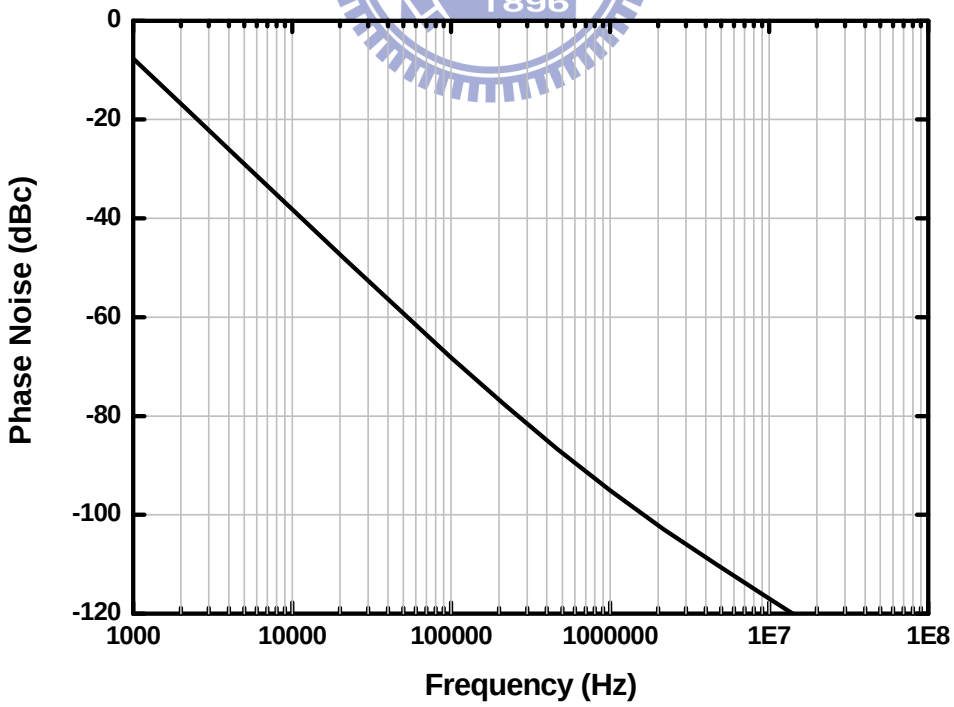


Fig. 2-31 Phase noise of voltage-controlled oscillator

The post-simulation results for whole circuits are shown in Fig. 2-32–2-34. Fig. 2-32–2-33 illustrate the output power and overall drain efficiency versus tuning voltage. As Fig. 2-32 shown, it is obvious that the output power is all about 10 dBm when the tuning voltage changes from 0 V to 1.2 V. As Fig. 2-33 shown, it is obvious that the overall drain efficiency is all about 20 % when the tuning voltage changes from 0 V to 1.2 V. The DC power consumption mentioned in Fig. 2-33 is included with the DC power consumption of whole circuits not only class E power amplifier. Fig. 2-34 shows the output power spectrum for whole circuits. As Fig. 2-34 shown, it has about 50 dB harmonic rejection capability. Due to the differential architecture, it has a good harmonic rejection capability.

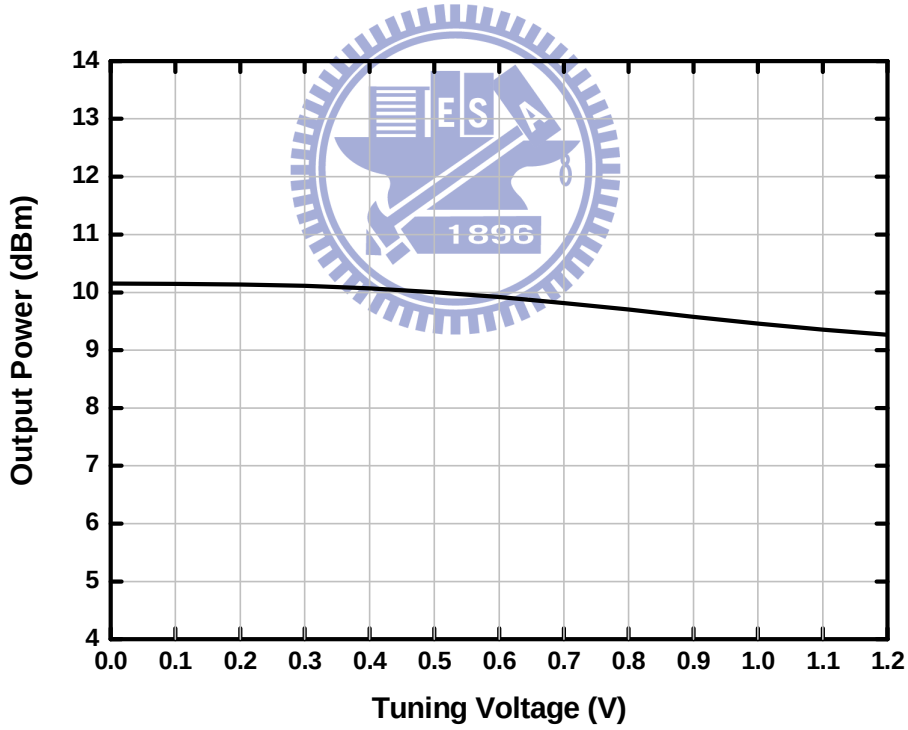


Fig. 2-32 P_{out} vs V_{tune} for whole circuits

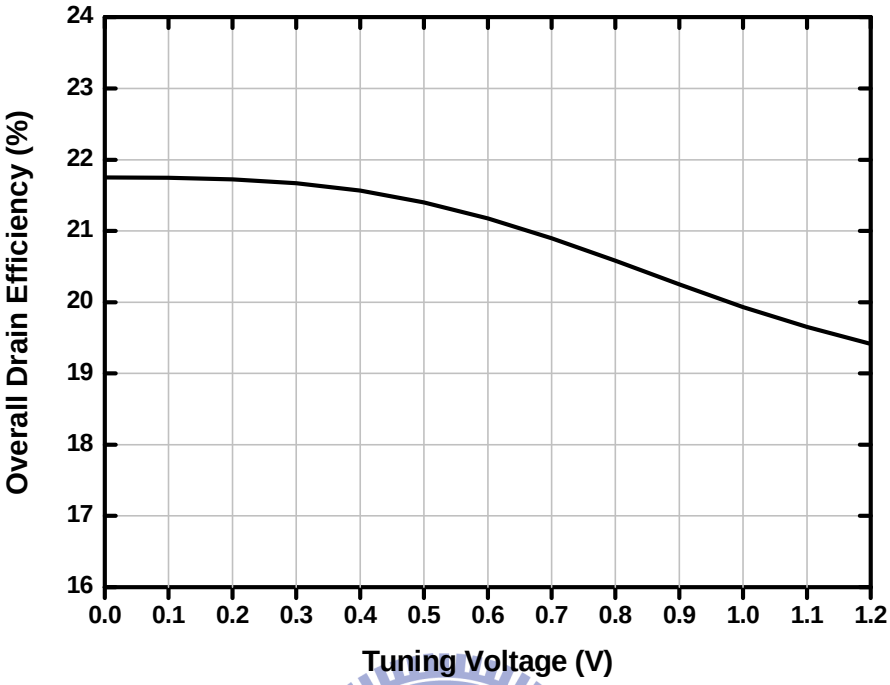


Fig. 2-33 Overall drain Efficiency vs V_{tune} for whole circuits

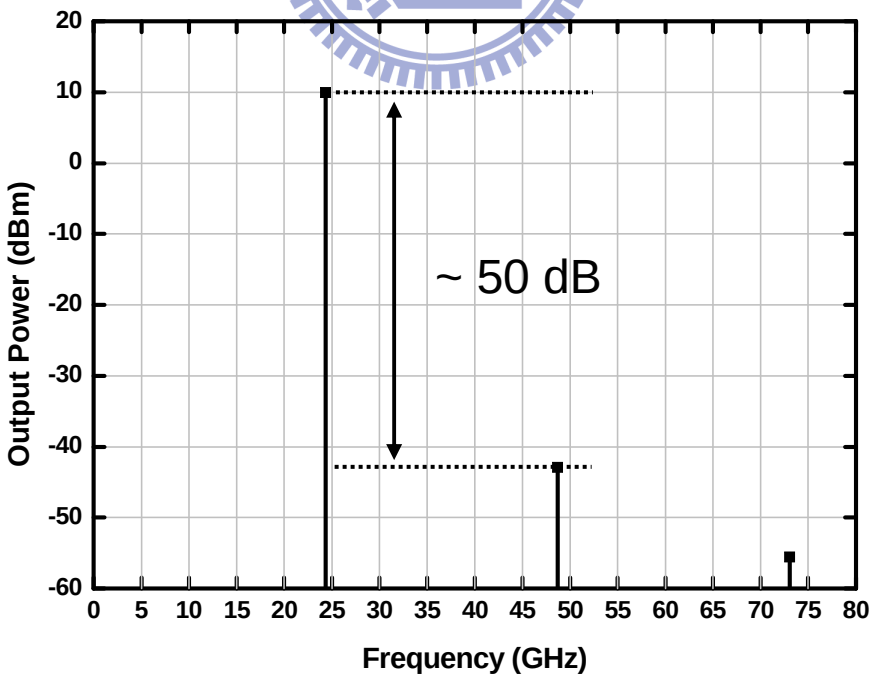


Fig. 2-34 Output power spectrum for whole circuits

Fig. 2-35 shows the post-simulation results for the cascode buffer with power amplifier. "P_{out} versus P_{in}", "PAE versus P_{in}" and "Drain Efficiency versus P_{in}" curves are shown in Fig. 2-35. The maximum PAE is 21.25 % at the input power of 0 dBm and output power of 9.73 dBm. It is because that the input of cascode buffer is off-chip Bias-Tee and the DC power consumption is included with the DC power consumption of cascode buffer not only class E power amplifier.

Table 2-3 and Table 2-4 give the performance summaries of voltage-controlled oscillator, power amplifier, and integrated whole circuits.

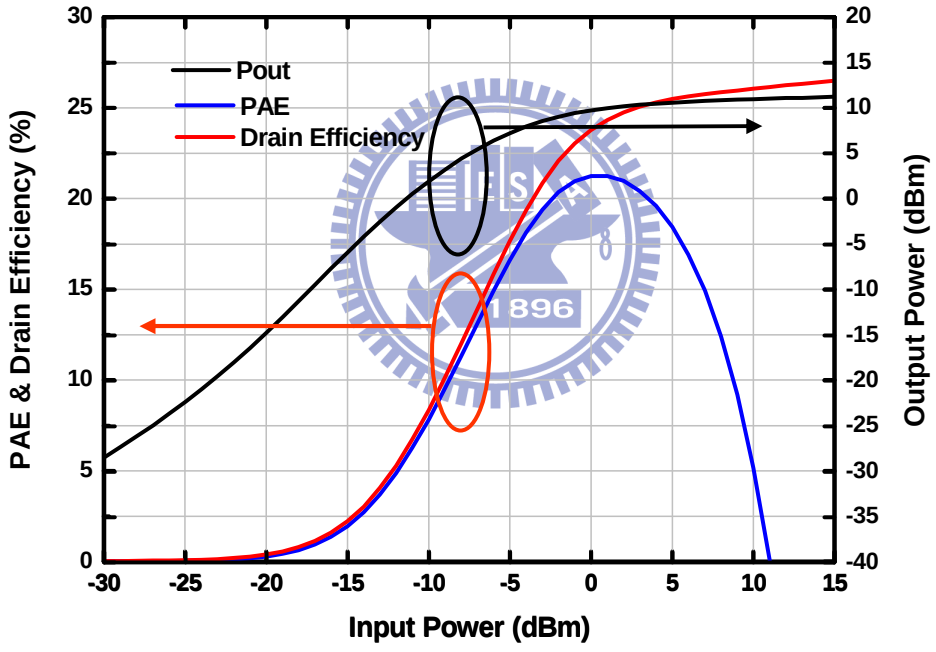


Fig. 2-35 P_{out} vs P_{in}, PAE vs P_{in} and Drain Efficiency vs P_{in} for cascode buffer with power amplifier

Table 2-3 Summaries of original post-sim results1

		Post-Sim (Original)
Technology		0.13-μm CMOS
Supply Voltage (V)		1.2
RF (GHz)		25
Power (mW)	Voltage-Controlled Oscillator with Cascode Buffer	15.3
	Class E Power Amplifier	31.1
	Total	46.4

Table 2-4 Summaries of original post-sim results2

		Post-sim (Original)	Spec.
VCO	Tuning Range (GHz)	0.8	-
	Phase Noise @ 10 MHz (dBc)	-117	-
Power Amplifier	Peak PAE (%)	38.67	-
	Max. P_{out} (dBm)	10.49	>10
	S11 / S22 (dB)	–30.3 / –3.3	-
Whole Circuits	Tuning Range (GHz)	0.795	-
	Phase Noise @ 10 MHz (dBc)	-117	-
	Max. P_{out} (dBm)	10.15	>10
	Overall Drain Efficiency (%)	22.31	-
Cascode Buffer with Power Amplifier	Peak PAE (%)	21.25	-

Chapter 3

Experimental Results

The proposed *K*-band CMOS class E power amplifier integrated with voltage-controlled oscillator is designed and fabricated using TSMC 0.13-um CMOS process. This chapter presenting the chip layout, test environment, and experiment results. Measured performance is compared with post-simulation results and discussion which is made for further study.

3.1. Chip Layout Descriptions

The chip microphotograph for the proposed circuits is given by Fig. 3-1 where the total chip area, including testing PADs, is 0.92 mm × 1.14 mm. The path from inductor to device is minimized in order to minimize impact on its quality factor. The parasitic inductance and capacitance of inevitable metal line are considered and pre-simulated in advance. Because of the differential structure of the designing VCO, symmetric style is adopted for VCO layout. The power line cell consisted of metal layers 1^{st}, 3^{rd}, 5^{th}, and 7^{th} for ground and metal layers 2^{nd}, 4^{th}, 6^{th}, and 8^{th} for V_{DD} is used in layout. These power line cells can provide power line between DC pad and core circuits and enough metal density at the same time. Besides, because the cell has bypass capacitance between each two layers, it also can provide enough bypass paths between V_{DD}/bias to ground.

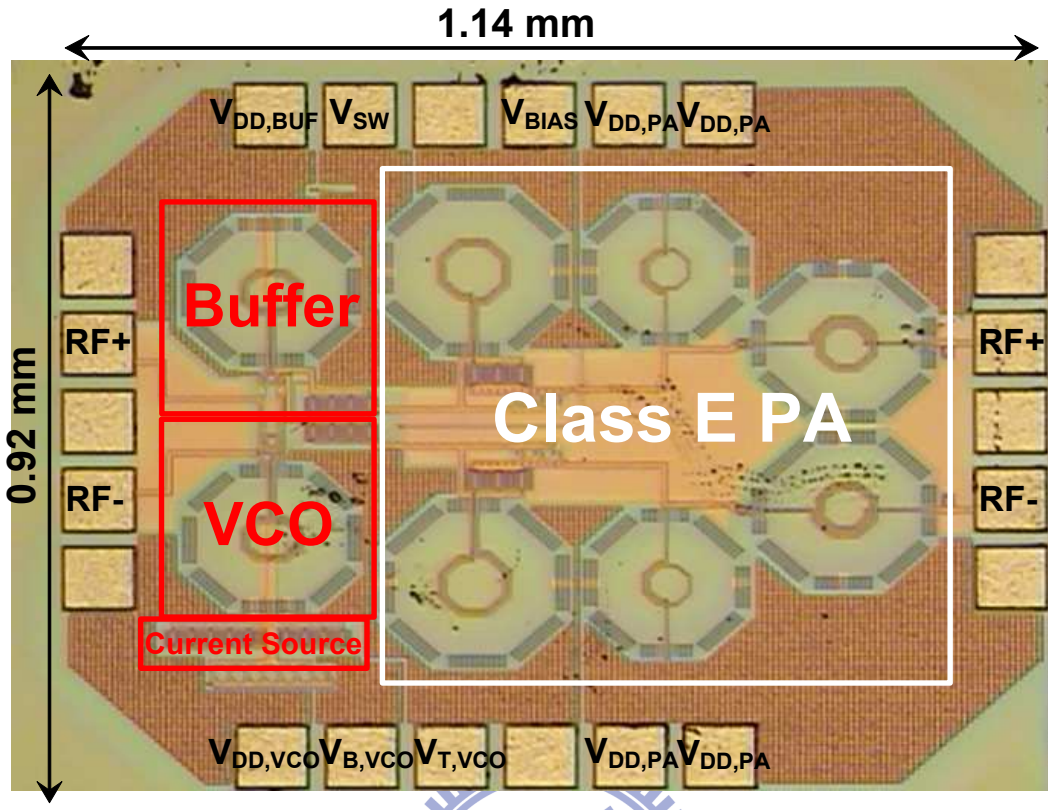


Fig. 3-1 Chip microphotograph of the proposed whole circuits

3.2. Measurement Setup

The measurement setup is shown in Fig. 3-2. This proposed circuits are on-wafer measuring. Two Infinite GSGSG-100 probes are used for differential signal PADs. Two 6-pin DC probe cards with 100-μm pitch are used for DC PADs. Besides, because of the off-chip components are needed at the RF output PAD and the RF input PAD, a Mini-Circuit ZFSCJ-2-1 transformer and two Anritsu V255 Bias-Tees are adopted. The S-parameter of the proposed whole circuits is measured by Agilent E8364B PNA. The Agilent E8257D signal generator and Agilent E4448A spectrum analyzer are used for linearity and output delivered power measurement.

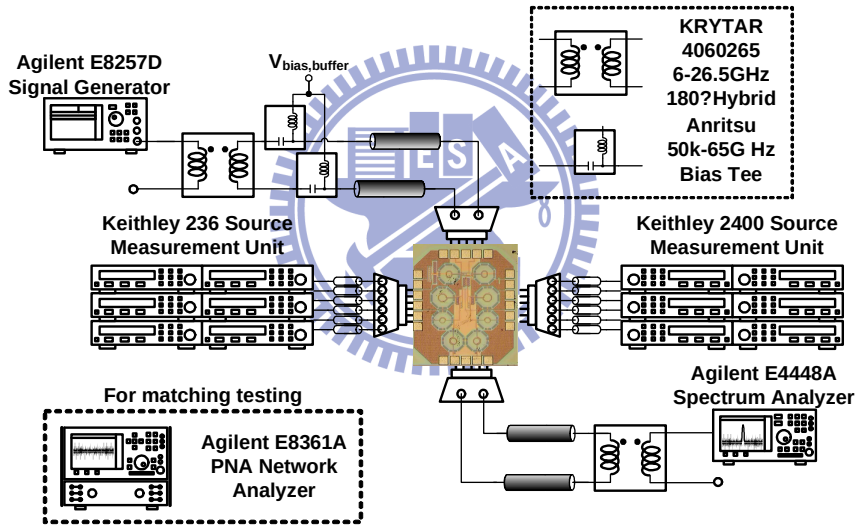


Fig. 3-2 Measurement setup for the proposed whole circuits

3.3. Experimental Results

The measured results of the proposed whole circuits are given by Fig. 3-3–Fig. 3-7. The measured results of sweep tuning voltage from 0 V to 1.2 V are given in Fig. 3-3–Fig. 3-4. As Fig. 3-3 shown, by comparing with the simulation results, it is obvious that the output center frequency is drifted from 24.4 GHz to near 23.2 GHz. As Fig. 3-4 shown, by comparing with the simulation results, it is obvious that the output power is decreased about 13 dB.

The measured results of phase noise, output power spectrum and cascode buffer with power amplifier are shown in Fig. 3-5–Fig. 3-7. In some figures, the cable losses of measurement setup at RF ports are calibrated already.

As Fig. 3-5 shown, by comparing with the simulation results, it is obvious that the phase noise at 10 MHz is decreased from -117 dBc to -108 dBc.

As Fig. 3-6 shown, the center frequency is about 23.20 GHz and the output power is -9.96 dBm when the tuning voltage equals 0.6 V.

As Fig. 3-7 shown, in order to test the cascode buffer with power amplifier, extra cables and off-chip components such as Bias-Tees and hybrid must be used. By comparing with the simulation results, it is obvious that the output power is decreased also about 13 dB. The summaries and comparison table with the simulation results are given by Table 3-1.

As Fig. 3-8 shown, the drain efficiency is low and the PAE is negative. It is because that the output power is smaller than input power. Due to that the output power is decreased also about 13 dB, the PAE of cascode buffer and power amplifier has negative value.

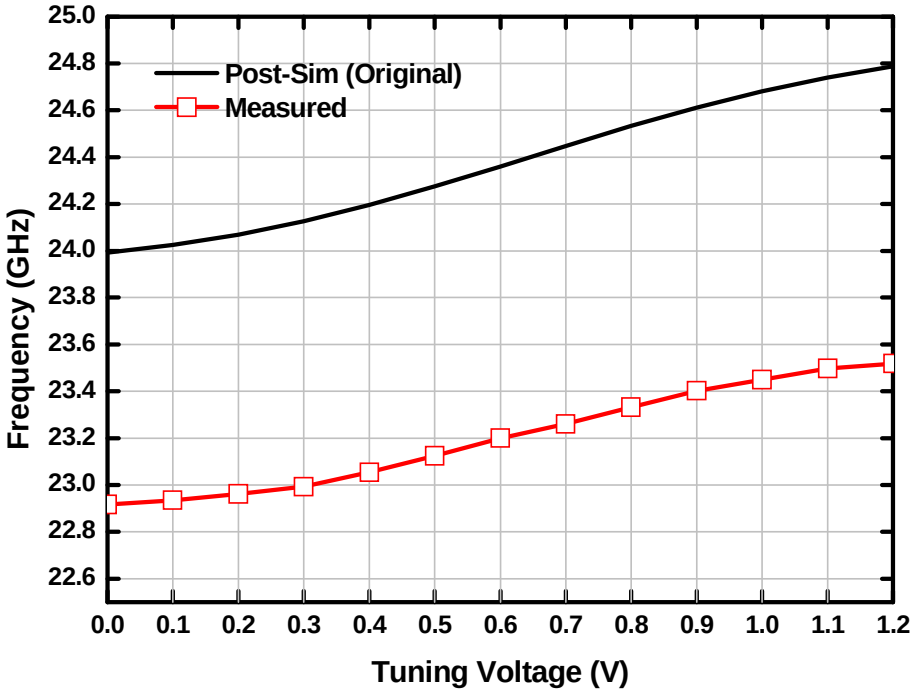


Fig. 3-3 Measured output frequency v.s. tuning voltage for proposed whole circuits

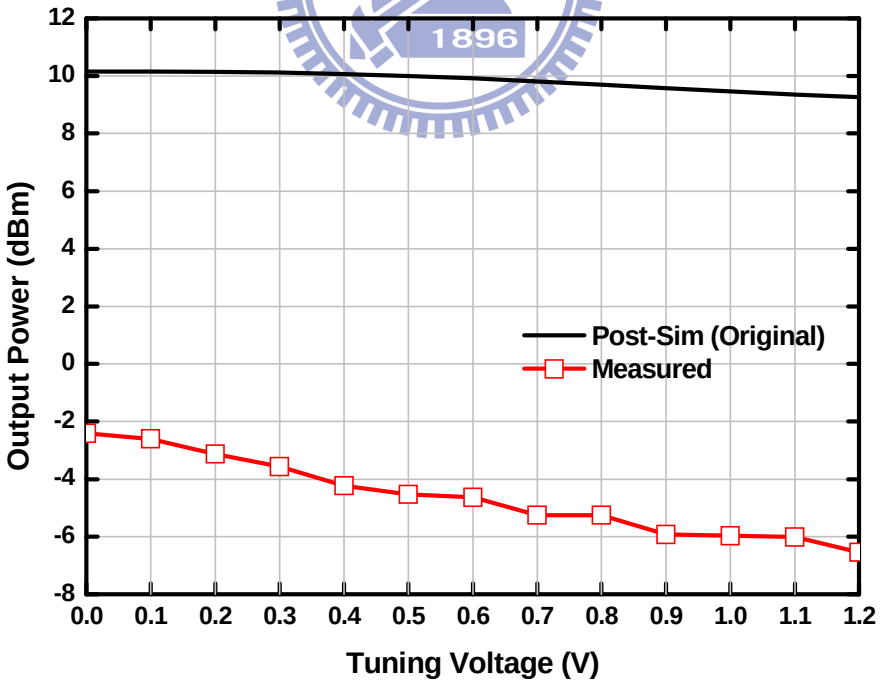


Fig. 3-4 Measured output power v.s. tuning voltage for proposed whole circuits

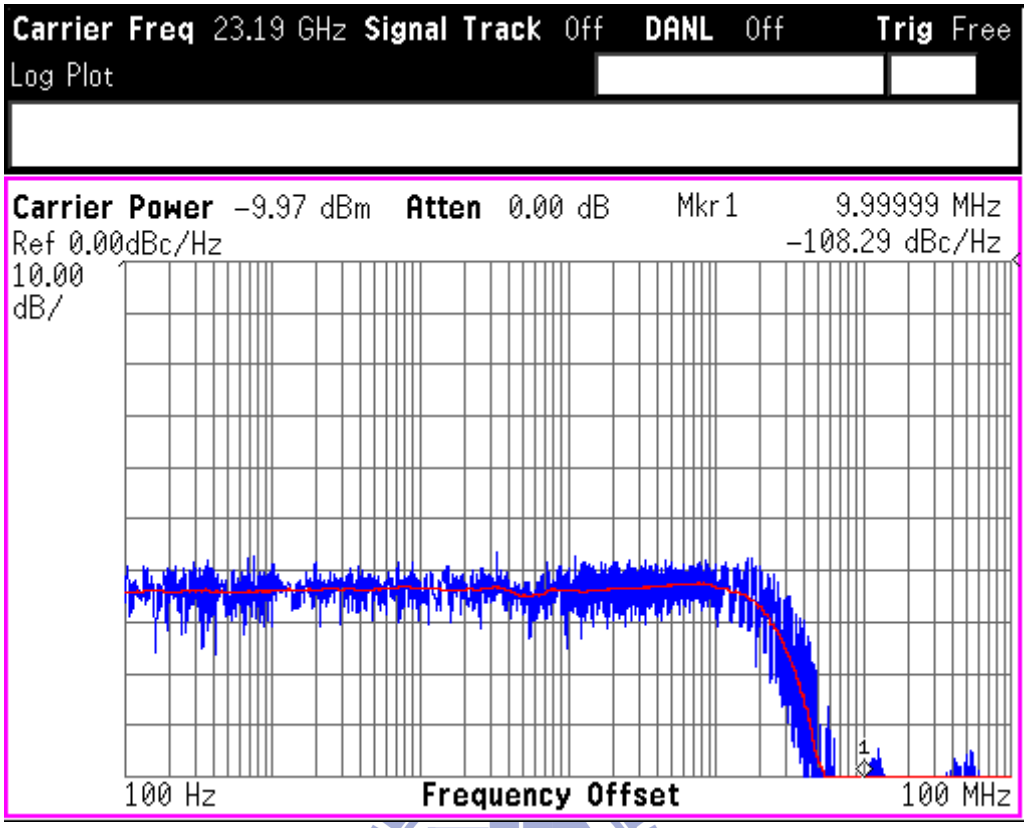


Fig. 3-5 Measured phase noise for proposed whole circuits

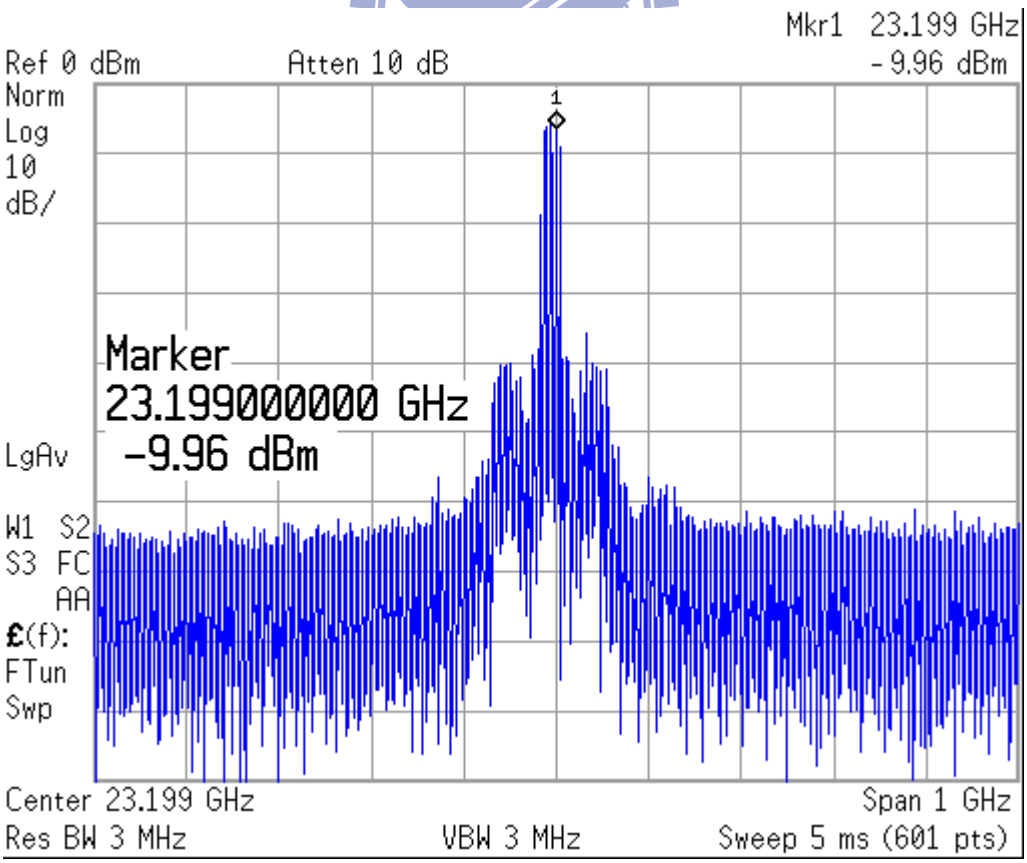


Fig. 3-6 Measured output power spectrum for proposed whole circuits

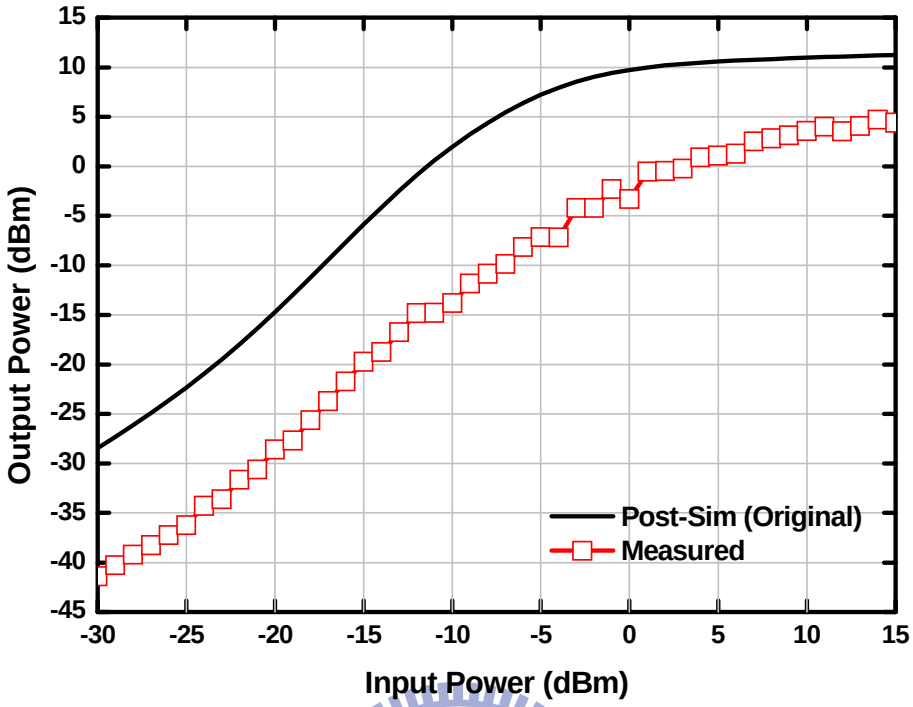


Fig. 3-7 P_{out} vs P_{in} for cascode buffer with power amplifier

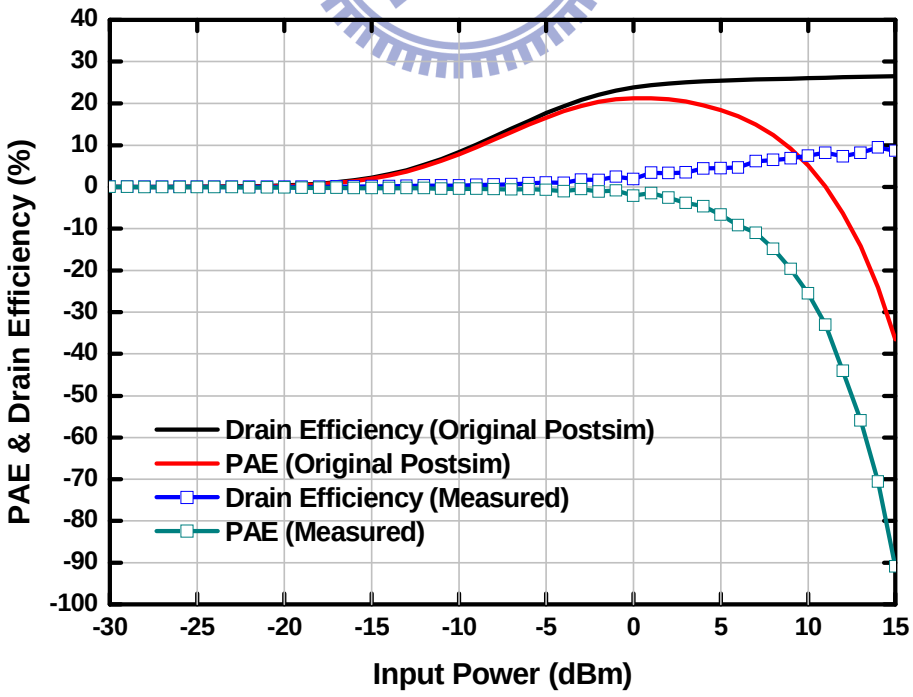


Fig. 3-8 PAE and drain efficiency vs P_{in} for cascode buffer with power amplifier

Table 3-1 Summaries of measurement results

		Post-Sim (Original)	Measurement	Spec.
Technology		0.13-μm CMOS		-
Supply Voltage (V)		1.2		-
RF (GHz)		24.4	23.2	24
Power (mW)	Voltage-Controlled Oscillator with Cascode Buffer	15.3	13.7	-
	Power Amplifier	31.1	15.7	-
	Total	46.4	29.4	-
Whole Circuits	Tuning Range (GHz)	0.795	0.602	-
	Phase Noise @ 10 MHz (dBc)	-117	-108	-
	Max. P_{out} (dBm)	10.15	–2.41	>10
	Overall Drain Efficiency (%)	22.31	1.95	-
Cascode Buffer with Power Amplifier	Peak PAE (%)	21.25	-	-
Chip Area (mm^2)		1.05		-

3.4. Discussion

It is obvious that the measured results are quite different from the results shown in post simulation. The performance degradation can be categorized into two parts. One is the degradation of the output power. Another is the drift of the center frequency. The detailed explanation will be introduced as follows.

3.4.1. The Degradation of Output Power

The gate waveforms of $M_{buffer4}$ given by original post-simulation and by revised post-simulation are given by Fig. 3-9. It is clear that the gate waveform given by post-simulation is biased to 1.2 V. However, the revised post-simulation result shows that the gate waveform of $M_{buffer4}$ is not exactly biased to 1.2 V. It has about 0.46 V swing on the 1.2 V DC level. After re-check the layout of the designing circuits, a mistake of crossover MOS line has been found. Because the crossover MOS line locates at the gate of $M_{buffer4}$, it may cause a big substrate coupling effect to let the gate waveform have about that kind of swing on the 1.2 V DC level. The original routing of the crossover MOS line in schematic and layout and the difference between the gate waveform of $M_{buffer4}$ with and without this crossover MOS line are shown in Fig. 3-9. In addition to that the source and body of $M_{buffer4}$ are connected together, the output power comes form voltage-controlled oscillator will be introduced to the gate of $M_{buffer4}$ by this substrate coupling effect. That is the reason why output power during the measurement is much lower than that in post-simulation.

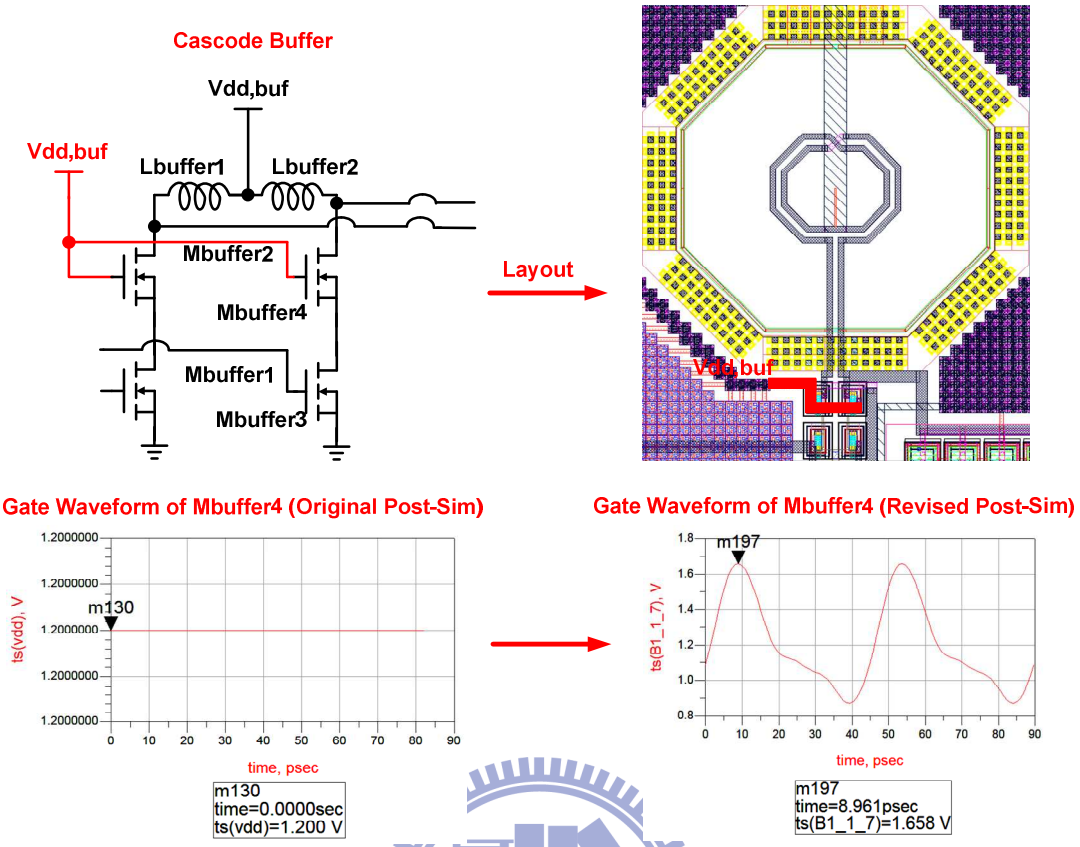


Fig. 3-9 The crossover MOS line and the effect in the gate waveforms of $M_{buffer4}$

3.4.2. The Degradation of the Frequency Drift

In general, the frequency drift comes from the parasitic effect. Because the parasitic effect had been considered for long metal line as shown in Fig. 2-22–Fig. 2-23, it is possible to underestimate the parasitic effect of other nodes. Therefore, the revised post-simulation has been done by considering full chip EM effect and re-simulated by HFSS. The layout view and 3-D model in HFSS are shown in Fig. 3-10.

Therefore, the revised post-simulation is done by replacing each SNP file produced by EM simulation in HFSS.

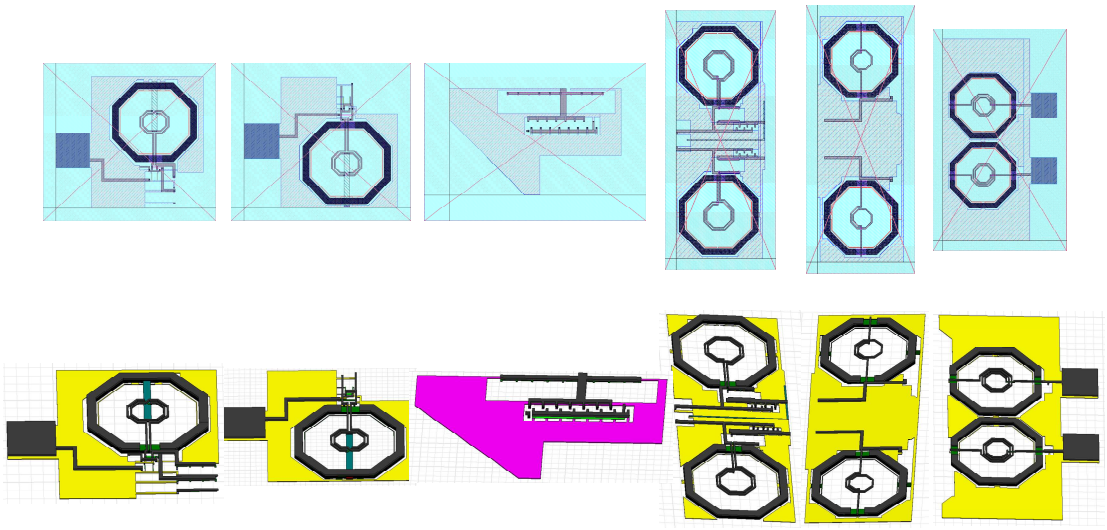


Fig. 3-10 Layout view and 3-D model in HFSS for revised post-simulation

3.4.3. Revised Post-Simulation Results

The revised simulation results, comparing with the original post-simulation results and measurement results, are shown in Fig. 3-11–Fig. 3-15. The sweep tuning voltage is shown in Fig. 3-11–Fig. 3-12. The center frequency drifts to 23.5 GHz which is similar to the measured results. Comparing to the original post-simulation, it is obvious that the phase noise and the testing cascode buffer with power amplifier case shown in Fig. 3-13–Fig. 3-15 of revised post-simulation results close to the measured results. The summaries and comparison table are given by Table 3-2

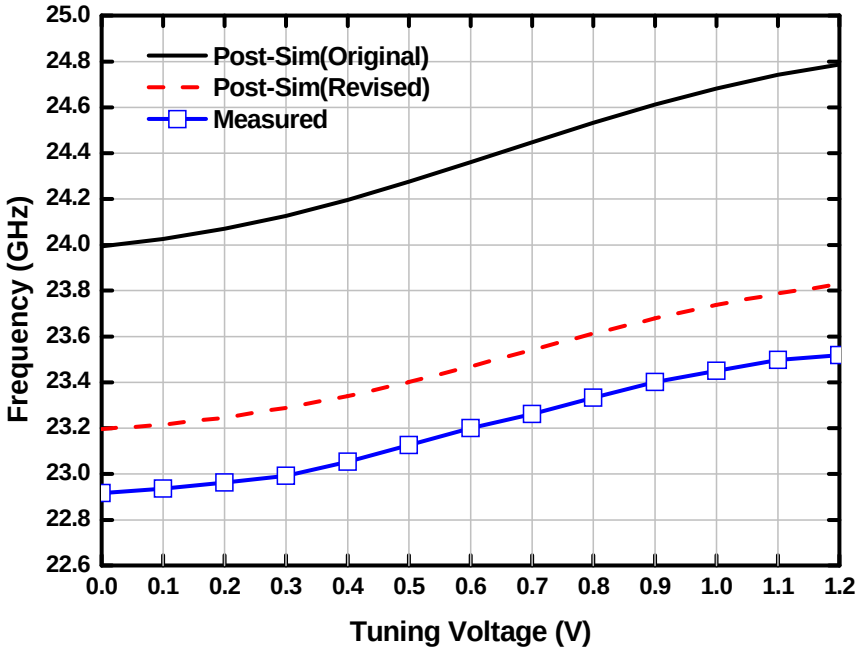


Fig. 3-11 Output frequency of revised post-sim comparing with original post-sim and measurement

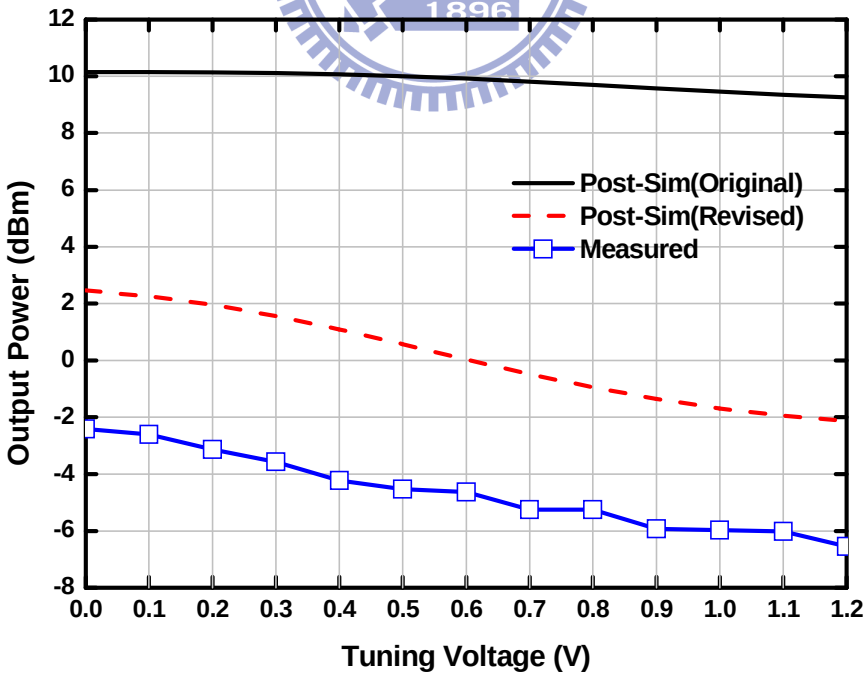


Fig. 3-12 Output power of revised post-sim comparing with original post-sim and measurement

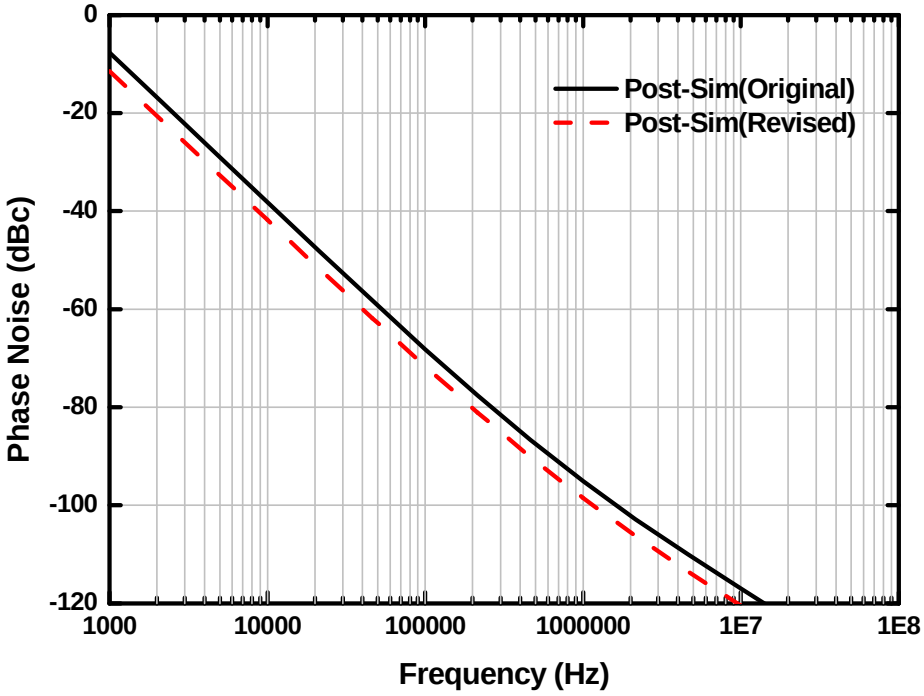


Fig. 3-13 Phase noise of revised post-sim comparing with original post-sim

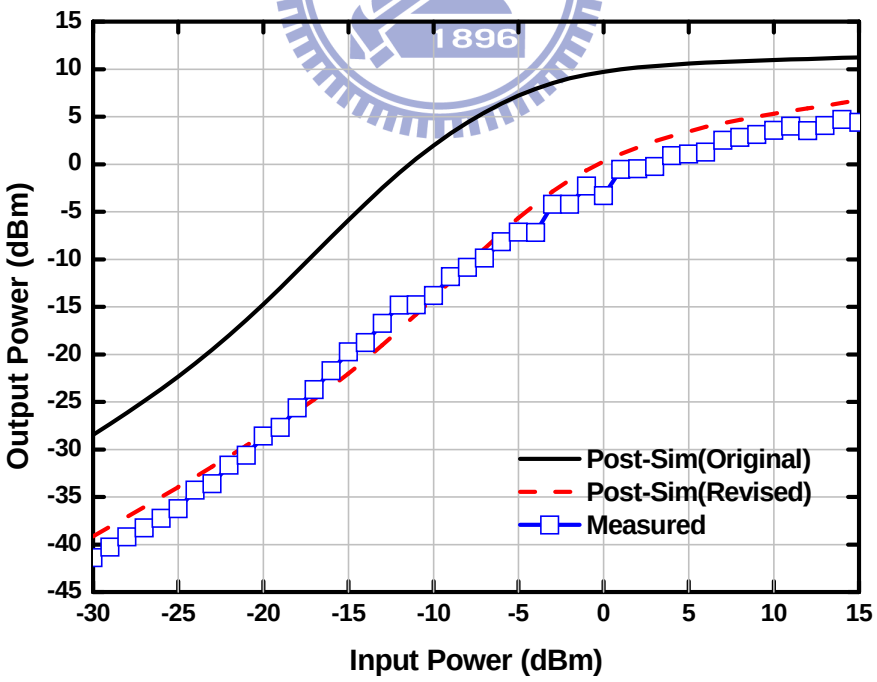


Fig. 3-14 P_{out} vs P_{in} of revised post-sim comparing with original post-sim and measurement

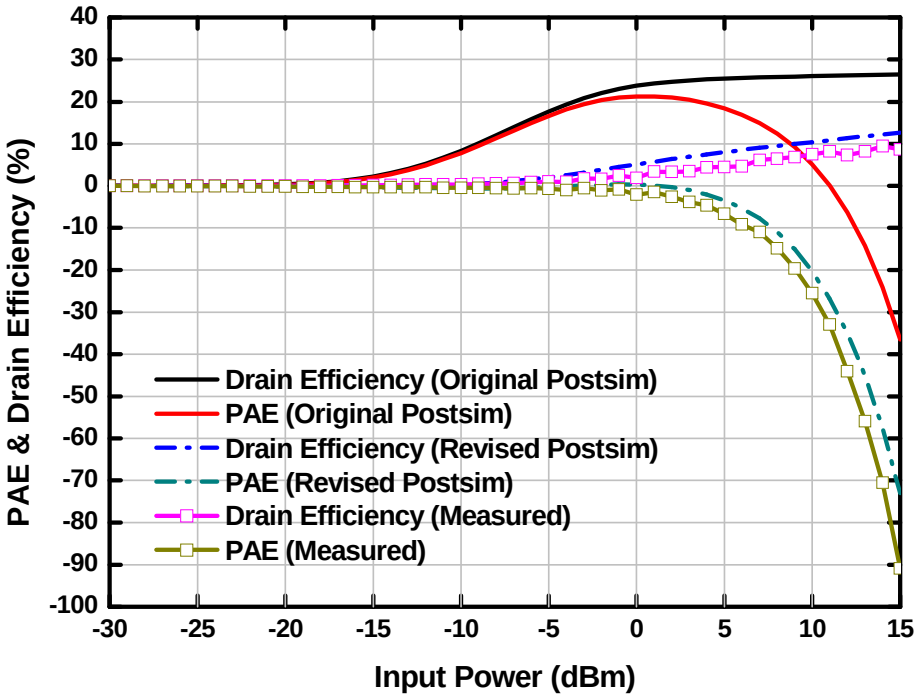


Fig. 3-15 PAE and drain efficiency vs P_{in} of revised post-sim comparing with original post-sim and measurement

Table 3-2 Summaries of revised post-sim results

		Post-Sim (Original)	Measurement	Post-Sim (Revised)	Spec.
RF (GHz)		24.4	23.2	23.5	24
Power (mW)	Voltage-Controlled Oscillator with Cascode Buffer	15.3	13.7	15.2	-
	Power Amplifier	31.1	15.7	10.9	-
	Total	46.4	29.4	26.1	-
Whole Circuits	Tuning Range (GHz)	0.795	0.602	0.632	-
	Phase Noise @ 10 MHz (dBc)	-117	-108	-120	-
	Max. P_{out} (dBm)	10.15	–2.41	2.47	>10
	Overall Drain Efficiency (%)	22.31	1.95	6.77	-
Cascode Buffer with Power Amplifier	Peak PAE (%)	21.25	-	-	-

3.5. Re-Design

Because some factor such as the parasitic effect simulated by Fig. 2-22–Fig. 2-23 is underestimated, the performance is quite degraded in measurement. Therefore, the purpose of the re-design is to match the original simulation performance but under the revised conditions. Under the worse conditions, the DC current, transistor's g_m, linearity, and power gain are degraded. Therefore, not only the passive components, the dimensions of active components have to be modified to improve the performance. In addition, the crossover MOS line (Metal 8) should be divided into two separate transmission lines (Metal 6, Metal 6). The components and transmission lines which have modified their dimensions are shown by red color in Fig. 3-16; the summaries of these dimensions are given by Table 3-3. The performance of the re-design version, including the detailed EM simulation of modified layout in Fig. 3-17 is simulated. The results of re-design version, comparing with original and revised post-sim, are shown in Fig. 3-18–Fig. 3-22. It is obvious that the output frequency and output power in Fig. 3-18–Fig. 3-19 are similar to the original design. The phase noise and the testing cascode buffer with power amplifier case, given by Fig. 3-20–Fig. 3-22, show that the phase noise and the testing cascode buffer with power amplifier case of the re-design are almost the same as the original. The summaries and the comparisons are given in Table 3-4–Table 3-7. It shows the proposed circuit has better PAE and drain efficiency under lower supply voltage. And the Ron case of re-design has better design results.

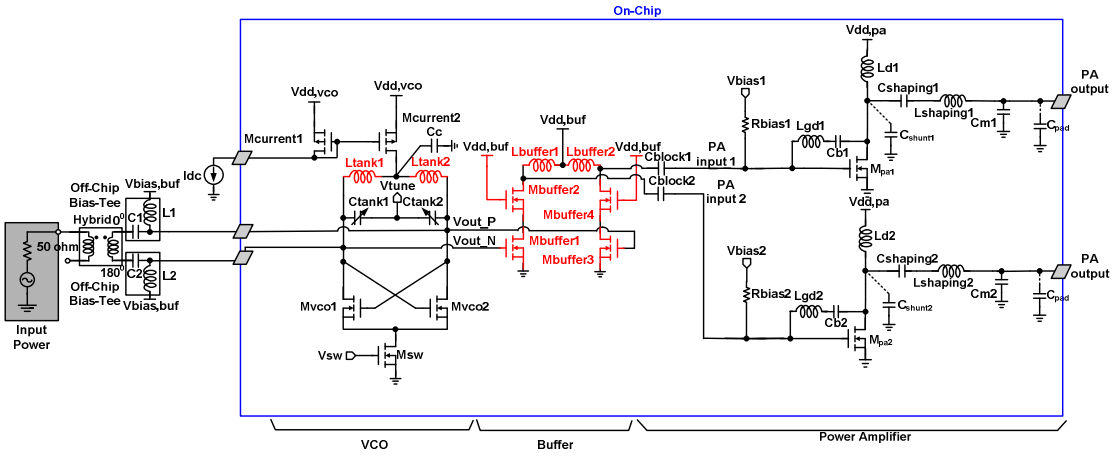


Fig. 3-16 Change components' dimensions for re-design

Table 3-3 Dimensions summaries of the re-design version

	Dimension (μm)
M_{pa1}	5*30/0.13
M_{pa2}	5*30/0.13
$M_{current1}$	3*20*1/0.35
$M_{current2}$	3*20*7/0.35
M_{vco1}	3*8/0.13
M_{vco2}	3*8/0.13
M_{sw}	3*40/0.13
*$M_{buffer1}$	6*11/0.13
*$M_{buffer2}$	6*16/0.13
*$M_{buffer3}$	6*11/0.13
*$M_{buffer4}$	6*16/0.13

	Value
L_1–L_2	off-chip
L_{gd1}–L_{gd2}	827.1 pH
L_{d1}–L_{d2}	395.9 pH
$L_{shaping1}$–$L_{shaping2}$	868.2 pH
*L_{tank1}–L_{tank2}	178 pH
*$L_{buffer1}$–$L_{buffer2}$	171 pH

	Value
R_{bias1}–R_{bias2}	10 Kohm
C_1–C_2	off-chip
C_{b1}–C_{b2}	1.38 pF
$C_{shaping1}$–$C_{shaping2}$	70.1 fF
C_{m1}–C_{m2}	109.1 fF
C_{pad}	30 fF
C_{block1}–C_{block2}	0.997 pF
C_c	2.5 pF
C_{tank1}–C_{tank2}	8-18 fF

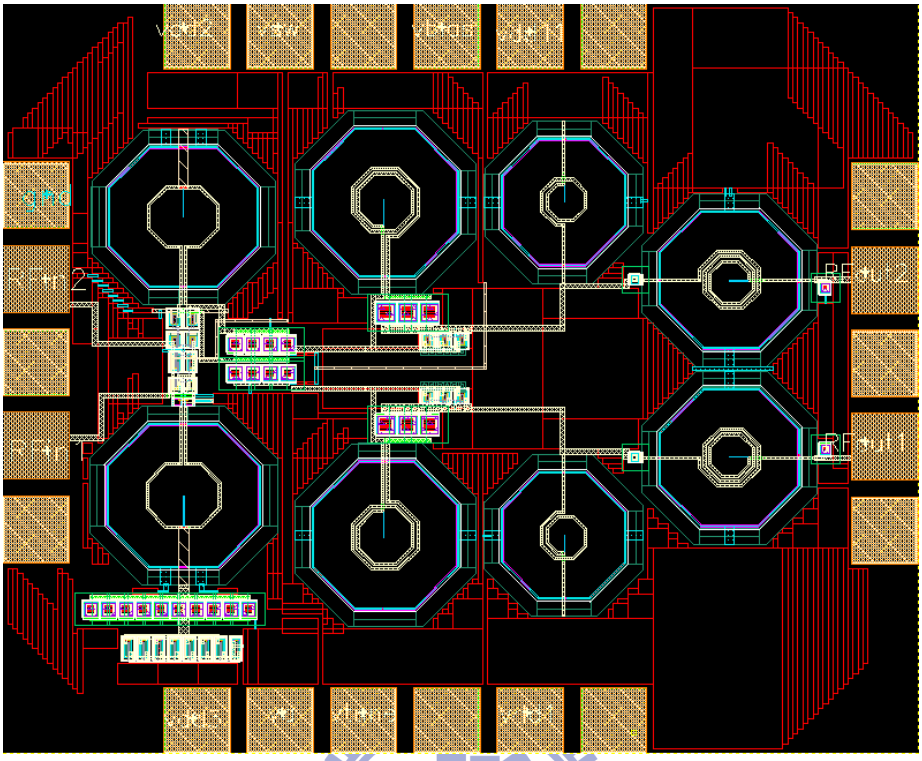


Fig. 3-17 The modified layout for re-design whole circuits

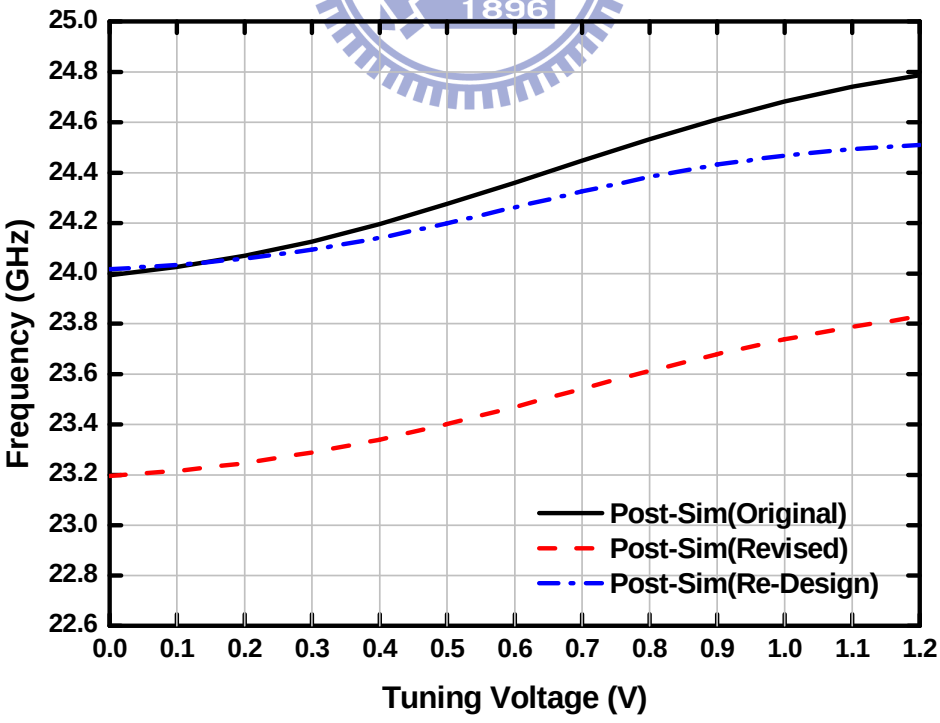


Fig. 3-18 Output frequency of re-design comparing with original and revised post-sim

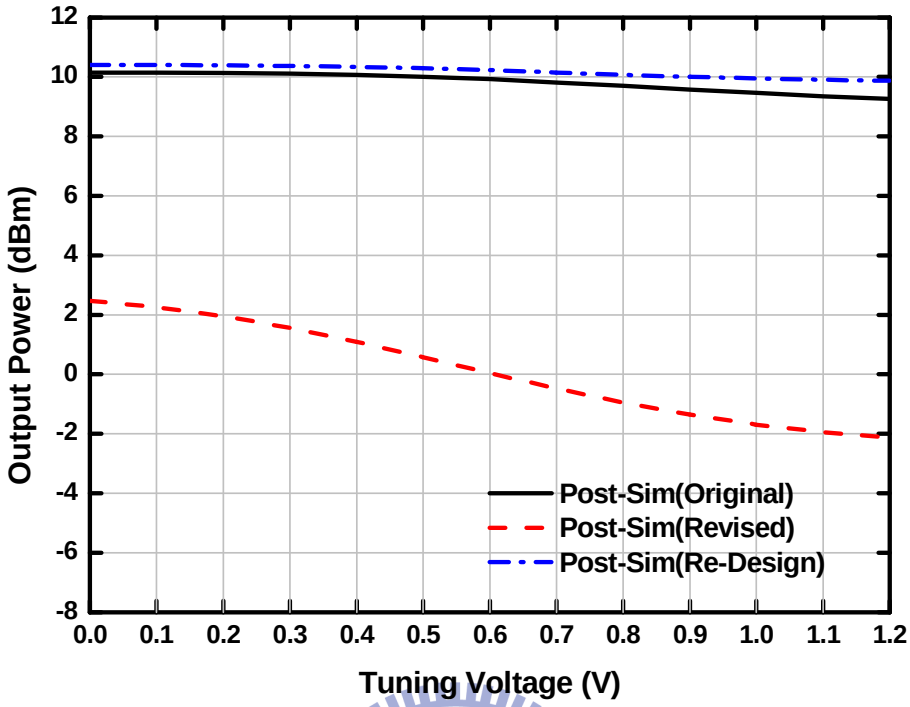


Fig. 3-19 Output power of re-design comparing with original and revised post-sim

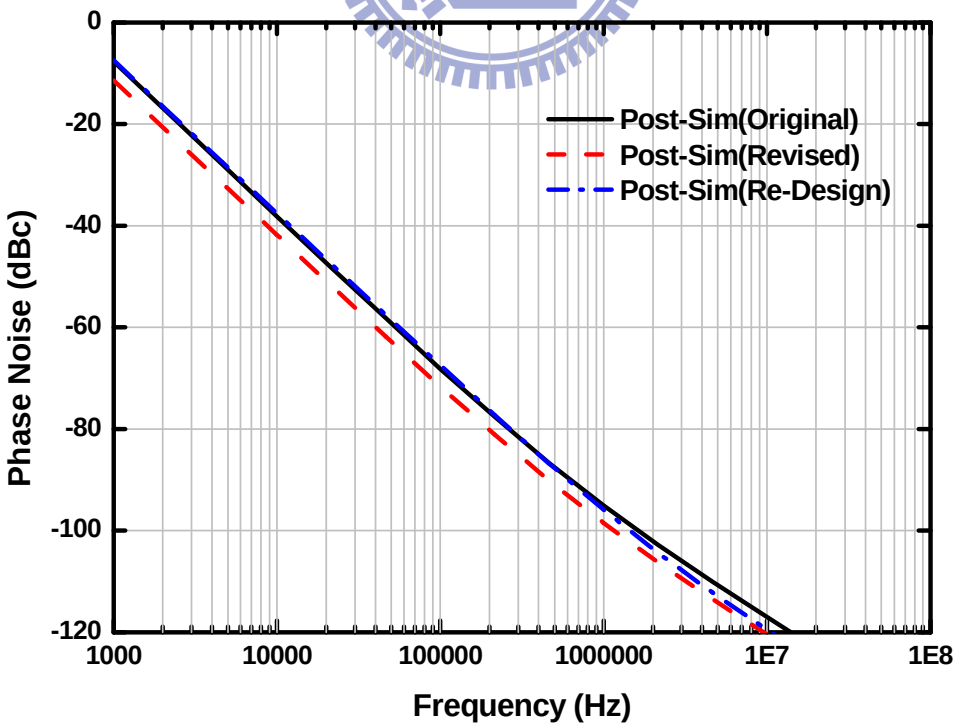


Fig. 3-20 Phase noise of re-design comparing with original and revised post-sim

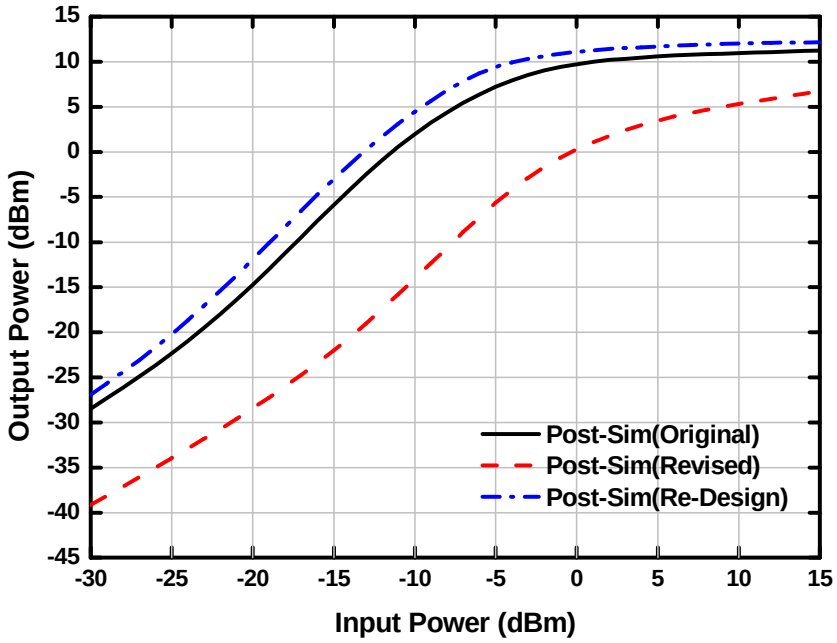


Fig. 3-21 P_{out} vs P_{in} of re-design comparing with original and revised post-sim

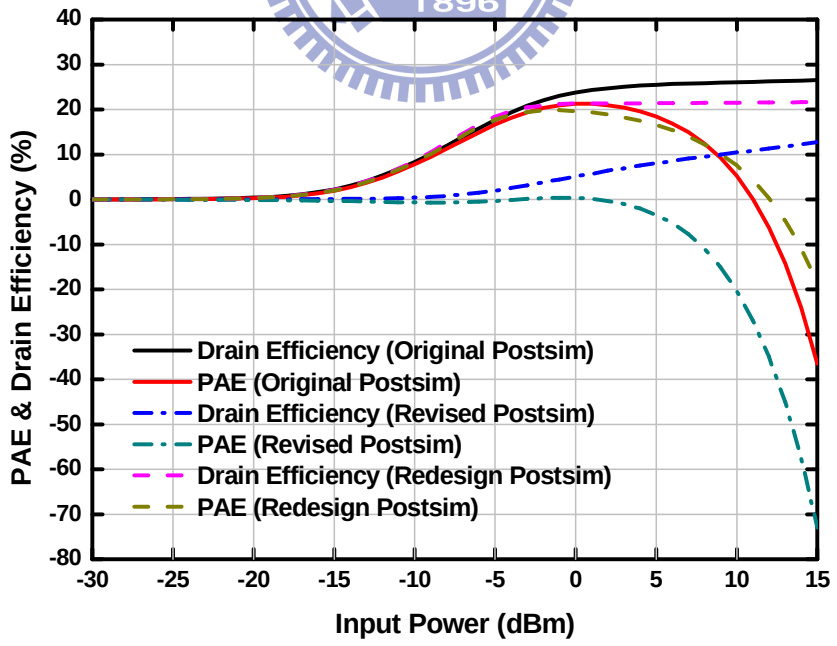


Fig. 3-22 PAE and drain efficiency vs P_{in} of re-design comparing with original and revised post-sim

Table 3-4 Comparison with other *K*-band power amplifiers

	Post-Sim (Re-Design)	[9]	[13]
Technology	0.13-μm CMOS	0.13-μm CMOS	0.18-μm CMOS
Topology	Class E Power Amplifier	Class E Power Amplifier	Class AB Power Amplifier
Supply Voltage (V)	1.2	1.5	2.5
Power Consumption (mW)	32.7	52.5	170
Frequency (GHz)	24.26	18	24
PAE (%)	27.82	23.5	6.5
Drain Efficiency (%)	32.91	23.43	14.78
Max. P_{out} (dBm)	10.41	10.9	14
Chip Area (mm^2)	1.05	0.78	14.28

Table 3-5 Comparison with other *K*-band power amplifiers

	Post-Sim (Re-Design)	*[10]	[11]	[12]
Technology	0.13-μm CMOS	0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Topology	Class E Power Amplifier	Class AB Power Amplifier	Class A Power Amplifier	Class A Power Amplifier
Supply Voltage (V)	1.2	1.2	3.6	3.6
Power Consumption (mW)	32.7	349.9	885.6	504
Frequency (GHz)	24.26	24	18-23	24
PAE (%)	27.82	23.9	9.3	20
Drain Efficiency (%)	32.91	29.3	11.55	31.45
Max. P_{out} (dBm)	10.41	17.1	20.1	22
Chip Area (mm^2)	1.05	1.05	0.79	0.42

*[10] : redesign post-sim results of proposed power amplifier in [10]

Table 3-6 Summaries of re-design post-sim results

		Post-Sim (Original)	Measurement	Post-Sim (Revised)	Post-Sim (Re-Design)	Spec.
RF (GHz)		24.4	23.2	23.5	24.26	24
Power (mW)	Voltage-Controlled Oscillator with Cascode Buffer	15.3	13.7	15.2	23.4	-
	Power Amplifier	31.1	15.7	10.9	32.7	-
	Total	46.4	29.4	26.1	56.1	-
Whole Circuits	Tuning Range (GHz)	0.795	0.602	0.632	0.492	-
	Phase Noise @ 10 MHz (dBc)	-117	-108	-120	-119.9	-
	Max. P_{out} (dBm)	10.15	-2.41	2.47	10.41	>10
	Overall Drain Efficiency (%)	22.31	1.95	6.77	19.59	-
Cascode Buffer with Power Amplifier	Peak PAE (%)	21.25	-	-	19.83	-

Table 3-7 Ron case comparisons

	Ron Case (Re-Design Postsim)	w/o Ron Case (Re-Design Postsim)
Technology	**0.13-μm CMOS**	**0.13-μm CMOS**
Topology	**Class E Power Amplifier**	**Class E Power Amplifier**
Supply Voltage (V)	**1.2**	**1.2**
Power Consumption (mW)	**32.7**	**21**
Frequency (GHz)	**24.26**	**24.26**
PAE (%)	**27.82**	**14.9**
Drain Efficiency (%)	**32.91**	**26.89**
Max. P_{out} (dBm)	**10.41**	**7.51**

Chapter 4

Conclusions and Future Work

4.1. Conclusions

In this research, 1.2-V *K*-band front-end circuits consisted of voltage-controlled oscillator and class E power amplifier are designed and measured. The power amplifier is realized by one-stage differential push-pull amplifier, and the voltage-controlled oscillator is realized by differential cross coupled LC tank voltage-controlled oscillator. This is the first work including a voltage-controlled oscillator and a power amplifier for *K*-band applications. A neutralization technique to improve isolation also has been developed instead of the cascode architecture.

Because of the layout mistake and incorrect post simulation procedure, the measured performance is seriously degraded. Measurement results show that the measured output center frequency and maximum output power are 23.2 GHz and –2.41 dBm, respectively. The measured phase noise is -108 dBc at 10 MHz. The measured output power of cascode buffer with power amplifier is lower than original post layout simulation about 13 dB. And the measured power consumption is 29.4 mW from 1.2 V power supply.

As after carefully considering these effects, the post layout simulation results of the re-design circuits show that the output center frequency and maximum output power are 24.26 GHz and 10.41 dBm, respectively. The phase noise is -119.9 dBc at 10 MHz. The output power of cascode buffer with power amplifier is almost the same to the original post layout simulation. And the total power consumption is 56.13 mW from 1.2 V power supply.

Even though the measured performance is seriously degraded, the advantages of

class E power amplifier approach can be noticed by post-sim results of the original or re-design circuits. Comparing to other works, this power amplifier has higher drain efficiency and PAE under lower supply voltage. Therefore, class E power amplifiers are suitable for high efficiency application, especially for advanced CMOS technology.

4.2. Future Work

Because the problem of frequency drift is occurred in measurement results, the re-design version is moved to 24.26 GHz by careful whole chip EM simulation. This re-design circuit will be tape-out and measured in the future. On-chip transformers at differential input and output will be integrated in next version. Polar loop structure will be designed in order to improve the linearity required of power amplifier in the future.

References

[1] ETSI EN 302 288-1 V1.1.1.

[2] Federal Communications Commission (FCC) 02-04, Section 15.249.

[3] Federal Communications Commission (FCC) 02-04, Section 15.515.

[4] Federal Communications Commission (FCC) website .(http://wireless.fcc.gov/auctions/default.htm?job=release&id=3578&y=2007), Auctions Datas, Band Plans, 24 GHz.

[5] E. Afshari, H. Bhat, X. Li, and A. Hajimiri, “Electrical funnel: a broadband signal combining method,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 206–207.

[6] A. Komijani and A. Hajimiri, “A 24 GHz, +14.5 dBm fully integrated power amplifier in 0.18 μm CMOS,” in *Proc. IEEE Custom Integrated Circuits Conf.*, Oct. 2004, pp. 561–564.

[7] Abbas Komijani, and Ali Hajimiri, “A Wideband 77-GHz, 17.5-dBm Fully Integrated Power Amplifier in Silicon,” in *IEEE Journal of Solid-State Circuits (JSSC)*, VOL. 41, NO. 8, AUGUST 2006, pp. 1749-1756.

[8] J.-L. Kuo, Z.-M. Tsai, and H. Wang, “A 19.1-dBm fully-integrated 24 GHz power amplifier using 0.18-μm CMOS technology,” in *Proc. EuMA*, Oct. 2008, pp. 1425–1428.

[9] C. Cao, H.-F. Xu, Y. Su, and K. K. O, “An 18-GHz, 10.9-dBm fully-integrated power amplifier with 23.5% PAE in 130-nm CMOS,” in *Proc. ESSCIRC*, Sep. 2005, pp. 137–140.

[10] C.-Y. Wu, S.-W. Hsu, and W.-C Wang, “A 24-GHz CMOS current-mode power amplifier with high PAE and output power,” in *Proc. IEEE ISCAS*, 2007, pp. 2866–2869.

[11] C.-C. Hung, J.-L. Kuo, K.-Y. Lin, and H. Wang, “A 22.5-dB gain, 20.1-dBm output power K-band power amplifier in 0.18-μm CMOS,” in *Proc. IEEE RFICS*, 2010, pp. 557–560.

[12] P.-C. Huang, J.-L. Kuo, Z.-M. Tsai, K.-Y. Lin and H. Wang, “A 22-dBm 24-GHz power amplifier using 0.18-μm CMOS technology,” in *Proc. IEEE IMS*, 2010, pp. 248–251.

[13] A. Komijani, A. Natarajan, and A. Hajimiri, “A 24-GHz, +14.5-dBm fully integrated power amplifier in 0.18-μm CMOS,” *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1901–1908, Sep. 2005.

[14] N.O. Sokal and A.D. Sokal. Class E-a new class of high efficiency tuned single-ended switching power amplifier. *Journal of Solid-State Circuits*, vol.sc-10, no. 3, Jun. 1975.

[15] Patrick Reynaert, Koen L. R. Mertens, and Michiel S. J. Steyaert, “A state-space behavioral model for CMOS class E power amplifiers,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 2, Feb. 2003

[16] Guillermo Gonzalez, “MICROWAVE TRANSISTOR AMPLIFIERS Analysis and Design,” SECOND EDITION.