國 立 交 通 大 學

電子工程學系 電子研究所 碩士班

碩 士 論 文

考量晶片封裝共同設計時的區域輸入輸出緩衝器

線路重佈繞線實作

An Implementation of Area-I/O RDL Routing for

Chip-Package Codesign

研 究 生：林昆生（Kun-Sheng Lin）

指導教授： 陳宏明 教授（Prof. Hung-Ming Chen）

中華民國九十九年三月

考量晶片封裝共同設計時的區域輸入輸出緩衝器線路重佈繞線實作

An Implementation of Area I/O RDL Routing for Chip-Package Codesign

研 究 生：林昆生　　Student：Kun-Sheng Lin

指導教授：陳宏明　教授　　Advisor：Professor Hung-Ming Chen

國 立 交 通 大 學

電 子 工 程 學 系　電 子 研 究 所 碩 士 班

碩 士 論 文

A Thesis

Submitted to Department of Electrical Engineering & Institute of Electronics

College of Electrical Engineering and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

March 2010

Hsinchu, Taiwan, Republic of China

中華民國九十九年三月

考量晶片封裝共同設計時的區域輸入輸出緩衝器線路重佈繞線實作

學生：林昆生　　指導教授：陳宏明　教授

國立交通大學　電子工程學系　電子研究所碩士班

摘　　要

覆晶封裝是由ＩＢＭ在６０年代所發展出來的，它提供一個高密度的解決方法給需求更多輸出入緩衝器的超大積體電路設計。線路重佈繞線問題是用來連接晶片以及封裝，這代表線路重佈繞線的結果將會影響晶片效能以及封裝效能。因此，近幾年來晶片－封裝－基板共同設計開始被提出並且逐漸受到重視。在這篇論文裡面我們提出一個考慮晶片－封裝共同設計時的區域輸入輸出緩衝器線路重佈繞線演算法。這個演算法包含晶片層級的分配以及線路重佈層級的繞線。我們在各個層級時不僅僅考量繞線長度還同時考量信號分配的影響。實驗數據顯示我們的方法可以在合理的接線長度內，大幅改善錫球分配並且達到百分之百的線路重佈繞線能力。

An Implementation of Area I/O RDL Routing for Chip-Package Codesign

Student: Kun-Sheng Lin **Advisor: Prof. Hung-Ming Chen**

Department of Electronic Engineering
Institute of Electronic
National Chiao Tung University

Abstract

The flip-chip package which was developed by IBM in the 60's provides a high chip-density solution to the demand of more I/O buffers in VLSI designs. The RDL routing problem is connected between chip domain and package domain, which means that the result of the RDL routing problem has strong influences on the chip performance and the package performance. Therefore, the concept of chip-package-board codesign is proposed and it is become more popular in recent years. In this thesis, we propose a routing algorithm for area-I/O RDL routing problem. Our algorithm contains chip-level assignment and RDL-level routing. In both chip-level assignment and RDL-level routing, we take not only wirelength but also signal influence into account. Experimental results have shown that our algorithm can improve bump assignment significantly with reasonable extra wirelength and it can achieve 100\% RDL routability.