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Process-variation- and random-dopants-induced threshold voltage fluctuations in nanoscale CMOS and SOI devices

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Abstract

In this paper, we investigate the threshold voltage fluctuation for nanoscale metal-oxide-semiconductor field effect transistor (MOSFET) and silicon-on-insulator (SOI) devices. The threshold voltage fluctuation comes from random dopant and short channel effects. The random-dopant-induced fluctuation is due to the random nature of ion implantation. The gate-length deviation and the line-edge roughness are mainly resulted from the short-channel effect. For the SOI devices, we should also consider the body thickness variation. In our investigation, the metal gate with high-κ material MOSFET is a good choice to reduce fluctuation of threshold voltage when comparing to the poly gate MOSFET and thin-body SOI devices.

Keywords: threshold voltage fluctuation; random dopant; process-variation; gate-length deviation; line-edge roughness; modeling and simulation

1. Introduction

As the dimension of complementary metal-oxide-semiconductor (CMOS) devices shrunk into sub-90nm scale, random-dopant-induced threshold voltage (Vt) fluctuations are pronounced [1-4, 6,7]. Fluctuation of threshold voltage is crucial for the design window, yield, noise margin, stability, and reliability of ultra large-scale integration circuits.

In this paper, we explore the threshold voltage fluctuation for planar metal-oxide-semiconductor field effect transistor (MOSFET) and silicon-on-insulator (SOI) devices. The fluctuation of threshold voltage comes from random dopant and short channel effects. The fluctuation of random effect derives mainly from the random nature of ion implantation. The fluctuation of short channel effect includes process-variation-induced gate length deviation and line edge roughness (as well as body thickness variation for SOI devices). The fluctuations are

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growing worse due to serious short-channel effect when the dimension of device is further scaled. The modeled threshold voltage fluctuation is firstly compared with the experimentally measured data for the 65nm high-performance and low-power devices, respectively. The investigation is advanced and finds that SOI device may suffer large body thickness variation and metal gate with high-κ material MOSFET [8,9] is a good choice to reduce fluctuation of threshold voltage.

This paper is organized as follows. In Sec. 2, we state the analyzing method used for the fluctuation of threshold voltage with respect to the random-dopant fluctuation, the gate-length deviation, and the-line edge roughness, respectively. In Sec. 3, we show the simulation results among devices. Finally, we draw conclusions.

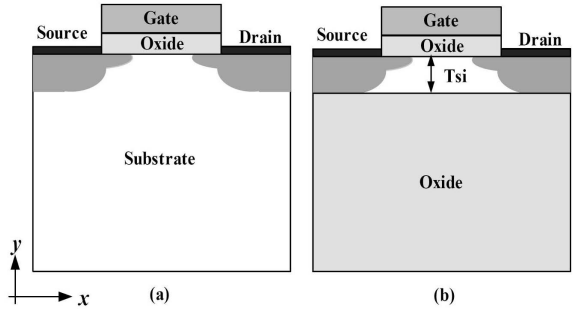


Fig. 1. A cross-sectional view of the simulated (a) planar MOSFET and (b) SOI device.

2. Computational approach

The fluctuation of threshold voltage is directly assumed to be contributed from the random dopant, the gate length deviation, and the line edge roughness. Therefore, the standard deviation of the total threshold voltage, $\sigma_{Vt,total}$, is

$$\sigma^2_{Vt,total} = \sigma^2_{Vt,RD} + \sigma^2_{Vt,Lg} + \sigma^2_{Vt,LER} \qquad (1)$$

where $\sigma_{Vt,RD}$ is the random-dopant-induced fluctuation, $\sigma_{Vt,Lg}$ and $\sigma_{Vt,LER}$ are fluctuations caused by the gate length deviation and line edge roughness. The $\sigma_{Vt,Tsi}$ of the body thickness variation is further considered for the SOI devices [1,7]. The random-dopant-induced threshold voltage fluctuation is calculated with a perturbed quantum correction approach, which was developed in our recent work [1,3,4]. Under the equilibrium condition, a two-dimensional quantum correction model together with the perturbation technique is firstly approximated by the finite volume method and then solved with the monotone iterative method for the explored devices. Thus, $\sigma_{Vt,RD}$ of device can be calculated in a cost-effective manner. Figure 1 shows the structures of the examined planar MOSFET and thin-body SOI devices.

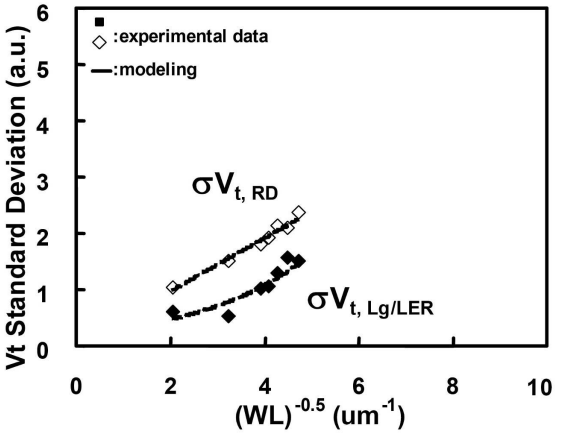


Fig. 2. The threshold voltage fluctuation comes from random-dopant and short channel effects for a 65nm high-performance device.

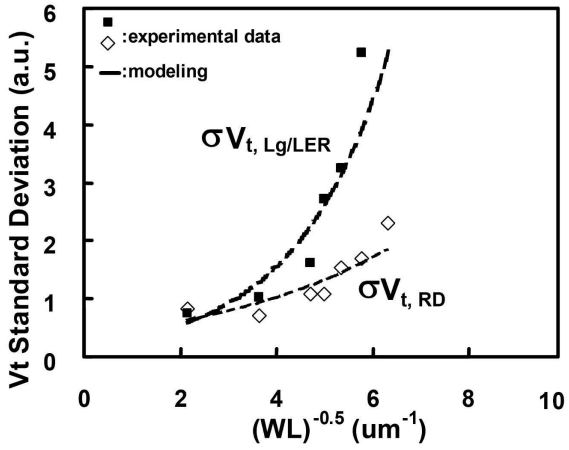


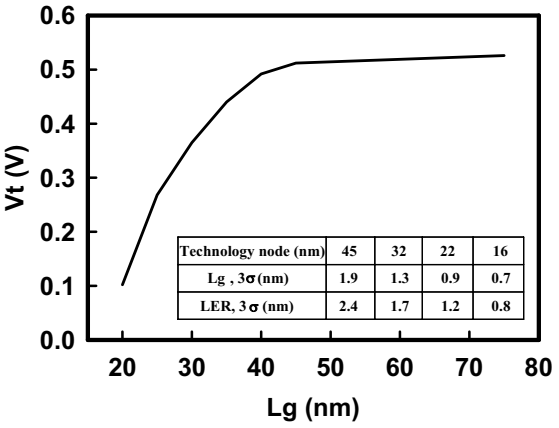
Fig. 3. The threshold voltage fluctuation comes from random-dopant and short channel effects for a 65nm lower-power device

Furthermore, we apply the statistical approach to evaluate the effect of $\sigma_{Vt,Lg}$ and $\sigma_{Vt,LER}$ [5]. The

magnitude of the gate length deviation and the line edge roughness are extracted from the projections of the ITRS 2005 for different technology nodes [1]. We establish a look-up table of the threshold voltage versus gate length firstly, as shown in Fig. 4. It enables us to evaluate the threshold voltage with respect to the deviation of gate length, which following the roadmap of ITRS that $3\sigma_{Lg}$ = 1.9 nm for the 45nm node and $3\sigma_{Lg}$ = 1.3nm for the 32nm technology node, as the inset table of Fig. 4. In a similar way, we calculate the effect of $\sigma_{Vt,LER}$ where the deviation of the line edge roughness following the rules, $3\sigma_{LER}$ = 2.4nm for the 45nm node and $3\sigma_{LER}$ = 1.7nm for the 32nm node. Thus, we can calculate the standard deviation of threshold voltage resulting from the deviation of gate length and the roughness of line edge.

3. Results and discussion

Figure 2 shows the different threshold voltage fluctuations for the 65nm high-performance MOSFET with varying device width. Figure 3 shows the result of the lower-power device. Our results have a good agreement with both the 65nm experiment data. We find that the threshold voltage fluctuations of the high-performance device are dominated by the short-channel effect; on the contrary, the Vt fluctuation of lower-power device are dominated by the random effect. The main difference of $\sigma_{Vt,RD}$ between the high-performance and low-power devices comes from different dopant materials. In addition, for the high-performance device, the $\sigma_{Vt,Lg}$ and $\sigma_{Vt,LER}$ are much more sensitive to device width than that of the low-power devices. Furthermore, Fig. 5 shows all fluctuation components of a 35nm planar MOSFET. In this case, the short-channel effects exceed the random-dopant-induced fluctuation when Lg < 25nm, and dominate the total fluctuations for device with a small Lg. Figure 6 shows a comparison among the poly-gate MOSFET, the metal-gate with high-κ material MOSFET, and the thin-body SOI device. In this work, the dielectric constant of the high-κ material is simply set to be 24, EOT of the high-κ gate dielectric is 1.4nm and the work function of metal-gate is 4.4 eV. We also consider that fluctuation comes from the variation of the body thickness in this comparison. The magnitude of body thickness deviation is $3\sigma_{Tsi}$ = 1.5nm. To be compared with Lg, the body thickness is Tsi = 5nm in this work [10,11]. The $\sigma_{Vt,Tsi}$ overwhelms all the other fluctuation factors in the thin-body SOI devices. Figures 7 and 8 show the comparisons of the total Vt fluctuation without and with considering $\sigma_{Vt,Tsi}$. When considering $\sigma_{Vt,Tsi}$, the metal gate with high-κ material MOSFET has smaller fluctuations compared with SOI devices.



Technology node (nm)	45	32	22	16
Lg , 3σ (nm)	1.9	1.3	0.9	0.7
LER, 3 σ (nm)	2.4	1.7	1.2	0.8

Fig. 4. The threshold voltage versus the gate length for a 35 nm planar MOSFET. The inset table is the magnitude of the gate length deviation and the line edge roughness.

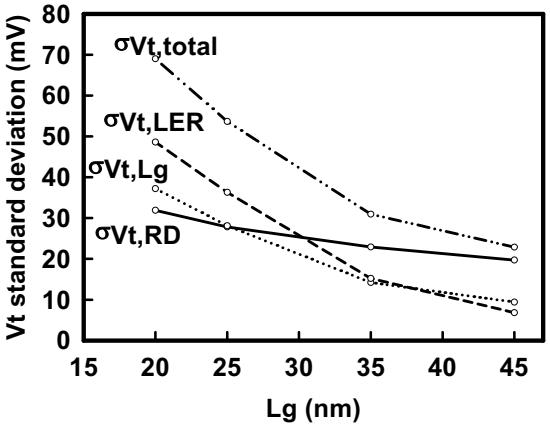


Fig. 5. Components of the threshold voltage fluctuation of the explored planar MOSFET, where the nominal Lg is 35nm and the oxide thickness is 1.7nm.

4. Conclusions

The threshold voltage fluctuation caused by the random dopant effect, the gate-length deviation, and the line-edge roughness are calculated and compared

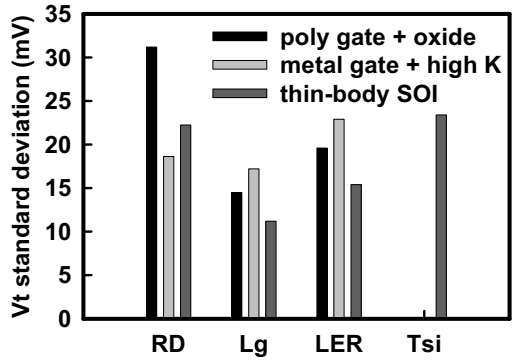


Fig. 6. Components of the threshold voltage fluctuation for the poly-gate MOSFET, the metal-gate, and high-κ materials MOSFET, and the thin-body SOI. The nominal Lg is 25nm.

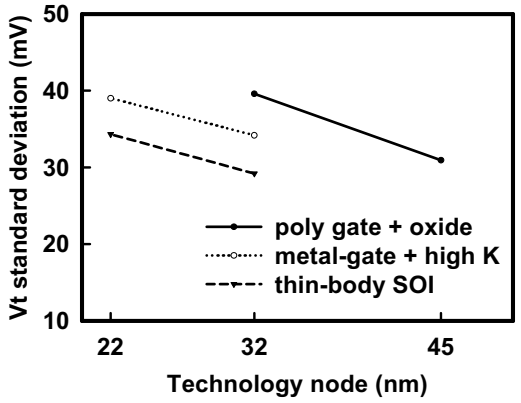


Fig. 7. The threshold voltage fluctuation versus different technology nodes without considering the $\sigma_{Vt,Tsi}$.

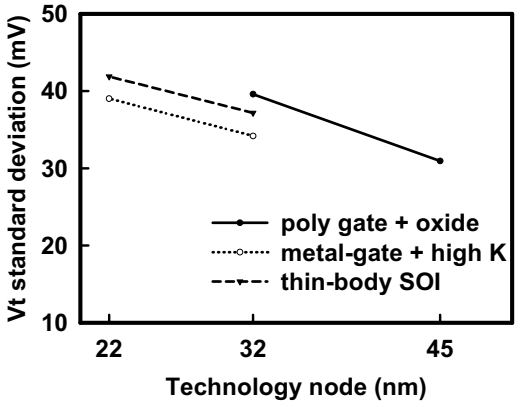


Fig. 8. The threshold voltage fluctuation versus different technology nodes including $\sigma_{Vt,Tsi}$.

the line-edge roughness are calculated and compared for the nanoscale CMOS and SOI devices. When ignoring the $\sigma_{Vt,Tsi}$, the SOI devices have the smaller Vt fluctuation. However the body thickness variation should be considered for the SOI devices; and it seems that the metal-gate with high-κ material MOSFET is a better solution for reducing Vt fluctuation.

Acknowledgements

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