國 立 交 通 大 學

電機與控制工程研究所

碩 士 論 文

一個 0.8-V 低功率類比前端積體電路應用於生醫訊號紀錄

A 0.8-V Low Power Analog Front-End IC for Biomedical Signal Recording

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指導教授：蘇朝琴　教授

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摘要

為了醫療上的用途，可攜帶的生醫訊號量測系統的需求越來越大。我們希望病人可以攜帶輕巧的監控裝置以做長時間的監控。本專案提出一個 0.8-V 低功率,可程式化的 CMOS 類比前端積體電路應用在生醫訊號測量。我們的設計能夠處理心電圖，肌電圖，以及腦波訊號，並且利用 chopper-stabilized 與交流回授電路技巧阻隔電極片的直流偏移，共模雜訊，以及 1/f 雜訊。儀表放大器的 input-referred noise floor 為 57 $nV/\sqrt{Hz}$ 以及 4.7 的 noise-efficient factor (NEF)。另外，可程式化放大器的電壓增益以及頻寬可以透過數位介面控制，實現上容易與 DSP 整合。考慮到放大器部分有 70dB 的動態範圍，因此整合一個低電壓低功率的連續近似暫存器類比數位轉換器。該類比數位轉換器有 0.09 $pJ/conv.step$，在取樣頻率為 2.67 KS/s 下有 63dB 的訊號對雜訊與失真比 (SNDR)，以及 0.31 μW 的功率消耗。工作電壓範圍 0.4-0.8V。前端放大器功率消耗是 1.84 μW。總功率消耗是 3.9 μW（不包含輸出緩衝器以及偏壓電路)。所提出的電路架構將被實現在 TSMC CMOS 0.18 μm 的製程，其晶片面積為 1.12mmX0.36mm（不包含 PAD）

索引詞彙—生物電位放大器，穩定截波，低電壓，低功率，數位類比轉換器，連續近似暫存器。

A 0.8-V Low Power Analog Front-End IC for Biomedical Signal Recording

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Institute of Electrical and Control Engineering

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Abstract

For medical purposes, there is a growing demand for portable bio-potentials signals systems. We hope that patients can wear the small-size and light-weight devices for long-term monitoring. A 0.8-V low power programmable CMOS analog front-end IC for biomedical signal acquisition is presented. Our design deal with Electrocardiogram (ECG), Electromyogram (EMG), and Electroencephalogram (EEG) signals, while reject DEO (Differential Electrode Offset), common-mode disturbance, and solve flicker noise by chopper-stabilized technique with an AC feedback circuit. The instrumentation amplifier achieves 57 $^{nV}/_{\sqrt{Hz}}$ input-referred noise floor and the noise-efficient factor (NEF) of 4.7. The programmable gain amplifier (PGA) sets voltage gain and bandwidth via digital interface, which could be integrated with DSP easily. Considering that the amplifier provides 70dB dynamic range (DR), a 11-b low-voltage low-power successive approximation register analog-to-digital converter (SAR ADC) is integrated. The SAR ADC circuit achieves Figure of Merit (FOM) of 0.09 $^{pJ}/_{conv.step}$, a signal-to-noise-and-distortion ratio (SNDR) of 63dB at sampling rate of 2.67KS/s and power consumptions of 0.31μW. The supply voltage range is from 0.4V to 0.8V. The power consumption of the front-end amplifiers is 1.84μW. The total power consumption is 3.9μW (output buffer and biasing circuits are excluded). The chip is realized in TSMC 1P6M 0.18μm CMOS process. The active die area is 1.12mmX0.36mm.

Index Terms – bio-potential amplifier, chopper-stabilized, low-voltage, low-power, analog-to-digital converters, successive approximation registers.

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最後感謝爸媽和哥哥這兩年給予我精神與物質上的支持，以及女友君寧的加油打氣，讓我能順利完成學業。

高碩廷

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Chapter 1

Introduction

1.1 Motivation

As the biomedical technology and IC processing technology grow rapidly, it is possible to realize a bio-potential read-out system on a single chip instead of the conventional one composed of many discrete components, which leads to large power consumption with extra costs. Furthermore, to reduce the patients' discomfort for long-term monitoring, it is encouraged to develop a small-size, light-weight and portable system. The challenges are low-noise, low-power and low-voltage circuits for battery-powered systems.

Generally, in order to read out the bio-potentials, two skin electrodes sticking on the body for improving common-mode noise immunity. However, bio-potential are commonly low frequency small signals, and there are three issues. First, the major one is the flicker noise. Due to low frequency signals, the charge carriers are trapped easily by dangling bonds, which appear at the interface between gate oxide and silicon substrate, and later released by the energy states, introducing flicker noise in the drain current. Second, another issue is power-line interference. Power line signal 50/60Hz coupled to the human body as the common-mode signal can be as high as 1mVpp. It

is not negligible compared to the bio-potential signals. Third, the other one is the differential electrode offset (DEO), which comes from the difference of two electrodes DC level. For conventional AgCl electrodes, the DEO can be as high as 50mv and the DEO changes with time slowly.

In this thesis, a 0.8-V low-power CMOS analog front-end integrated with 11-b SAR A/D converter is realized on a single chip. The front-end amplifier provides 70dB dynamic ranges and the programmable gain amplifier is capable of configuring the gain and bandwidth by digital interface. The power consumption of the chip is merely 3.9μW.

1.2 Basic Concepts of Biomedical Signal Recording

The Table 1-1 shows the common biomedical signals. It includes Electroencephalogram (EEG) shown in Figure 1-1, Electrocardiogram (ECG) shown in Figure 1-2, and Electromyogram (EMG) shown in Figure 1-3.

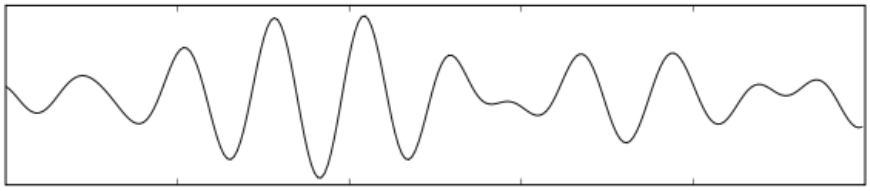


Figure 1-1 EEG alpha wave

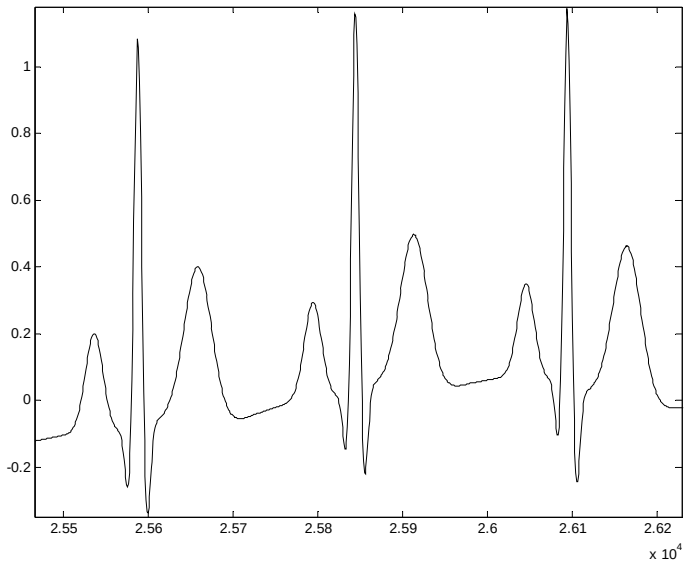


Figure 1-2 ECG signal

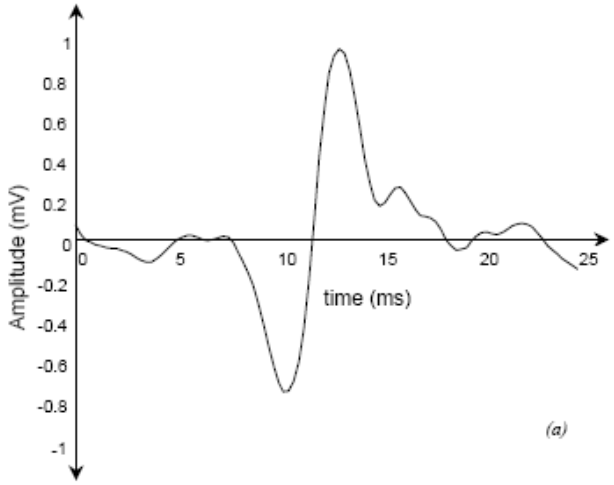


Figure 1-3 EMG signal

Table 1-1 Common biomedical signals

Biomedical signals	bandwidth	Amplitude (peak-to-peak)
EEG(Electroencephalogram)	0.5-100 Hz	100μV
ECG(Electrocardiogram)	0.5-100 Hz	5mV
EMG(Electromyogram)	10-1K Hz	2mV

The characteristics of these signals are low frequency small signals. The main issues in detecting them are flicker noise, common-mode noise, and differential electrode offset (DEO). On the subject of signal processing, the conventional solution is to use an instrumentation amplifier with very high CMRR to avoid flicker noise and suppress common-mode noise. As for DEO, it uses a high supply voltage or dual power supply to increase voltage headroom. According to the power consumption law, the power is proportion to the supply voltage. Thus, the conventional design has very high power consumption. Figure 1-1 shows a conventional bio-potential read-out system. Two skin electrodes are stuck on the human body, usually on two limbs, and pass the signals to the readout system. The system uses an instrumentation amplifier to amplify the signals, and filter out unwanted signals through analog filters, and then the filtered signals are converted to digital y an analog-to-digital converter.

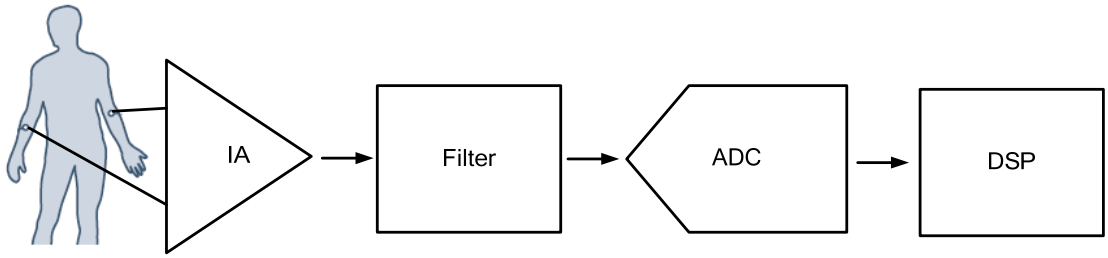


Figure 1-4 Conventional bio-potential readout system

1.3 Thesis Organization

This thesis describes a low-voltage low-power bio-potential readout analog front-end with configuration characteristics for different biomedical signals.

Chapter 2 gives a fundamental concepts and comparisons of dynamic offset cancelling techniques. A brief introduction and performance analysis on auto-zero amplifiers and chopper amplifiers. Besides, the chapter states the modern dynamic offset cancellation techniques and chopper-stabilized with AC feedback circuits.

Chapter 3 describes the fundamental principles of the charge redistribution successive approximation register A/D converter. The low-voltage circuits and the proposed design approach are presented.

Chapter 4 describes the proposed 0.8-V biomedical signal readout front-end IC. It includes IC design considerations, a front-end amplifier, a programmable gain amplifier, and a fully-differential boosted clock drivers. It also includes simulation results, the circuit layout and the measurement results.

Chapter 5 introduces the proposed 1.5-V bio-potential signal acquisition front-end. It includes the architecture, the simulated results, the layout, and measurement results. Chapter 6 states the conclusions.

Chapter 2

Dynamic Offset Cancellation Techniques

2.1 Introduction

The chapter states the details of bio-potential amplifiers. Section 2.2 introduces the noise in CMOS circuits. Section 2.3 describes the dynamic offset cancellation techniques, including auto-zero and chopping techniques. Section 2.4 presents AC coupled chopper-stabilized amplifiers with AC feedback circuits. Section 2.5 gives a brief summary.

2.2 Noise

In analog circuits design, there are two types of noises: the device electronic noise and environment noise. The former one could be categorized into flicker noise and thermal noise further. The latter one comes from the power supply noise or the substrates coupling noise. The following words focus on the electronic noise. The environment noise consideration is stated in Chapter 4.

Thermal Noise

Thermal noise is also called white noise because its noise power spectrum density is constant over a given frequency and the thermal noise comes from the random motion of electrons in conductors and the power spectrum density of the thermal noise is proportional to the absolute temperature. Figure 2-1 shows the thermal noise spectrum example and Figure 2-2 is the time domain example.

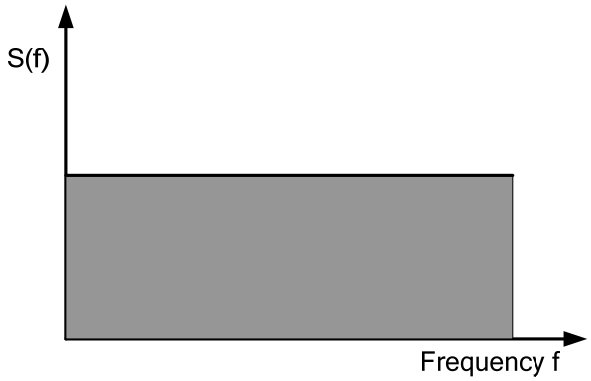


Figure 2-1 Thermal noise power spectrum density example

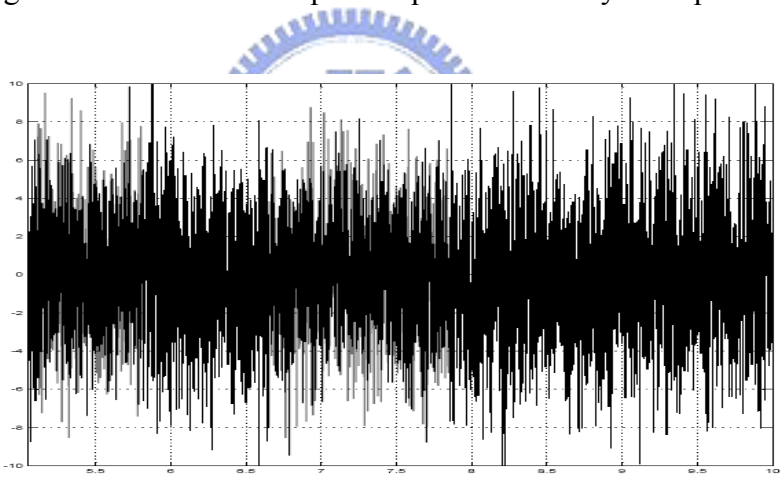


Figure 2-2 Thermal noise voltage signal in time domain

Different conductors have different noise models. For a resistor, the thermal noise could be modeled by a shunt current source or a series voltage source. Figure 2-3 illustrates the models. For a voltage source model, the thermal noise of a resistor could be represented as

$$S_R^2(f) = 4kTR. \tag{2.1}$$

Where k is the Boltzmann constant, $k = 1.38 \times 10^{-23}\, J/K$, T is the absolute temperature, and R is the resistance.

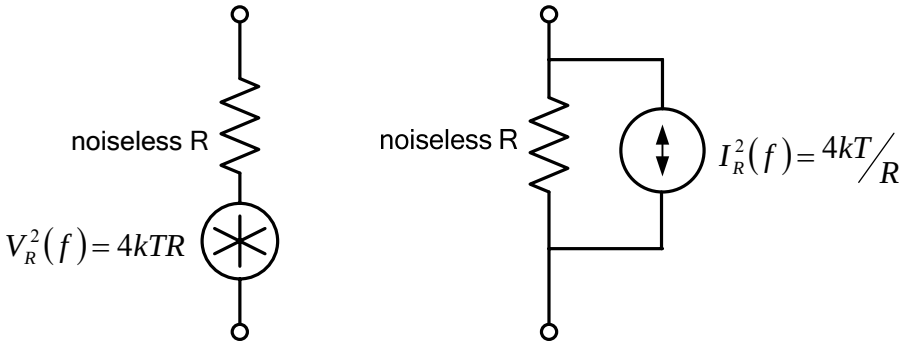


Figure 2-3 (a) A resistor thermal noise model with voltage source
(b) A resistor thermal noise model with current source

For a MOSFET, due to the resistive channel of a MOS transistor in active region, the thermal noise can be represented as

$$I_d^2(f)=4kT\gamma g_m. \tag{2.2}$$

Where γ is a constant. $\gamma=2/3$ for the long channel transistors.

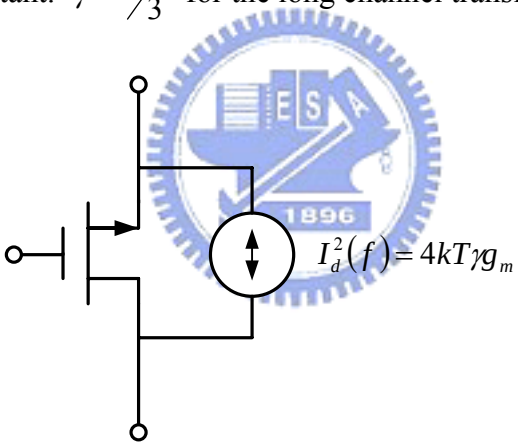


Figure 2-4 MOSFET thermal noise model

Flicker Noise

The flicker noise spectral density is inversely proportional to frequency, so it is also called “1/f noise”. The flicker noise in BJT is ignorable, but it is very high in MOSFET. Because there are dangling bonds at the interface between gate oxide and the silicon substrate, the charge carries can be trapped easily if the signal frequency is low. The phenomenon introduces the noise in the drain current and it can be modeled by a serial voltage source with the gate. Figure 2-5 shows the circuit model and (2.3) shows the model. Thus, larger device size introduces less flicker noise. It is common to use hundred or thousand micrometer square of devices in low-noise applications. Furthermore, it has a longer distance from channel to oxide-silicon interface for the

buried channel of PMOS. So, PMOS introduces less flicker noise than NMOS.

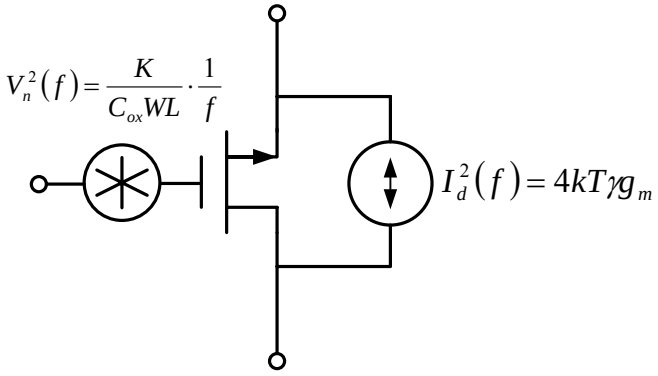


Figure 2-5 MOSFET noise model, including flicker noise voltage source and thermal noise current source.

$$\overline{V_n^2}=\frac{K}{C_{ox}WL}\cdot\frac{1}{f}. \tag{2.3}$$

Where C_{ox} is the gate capacitance per unit area, W is the width of the MOSFET, L is the length of the MOSFET, and K is the process-dependent constant on the order of $10^{-25}V^2F$.

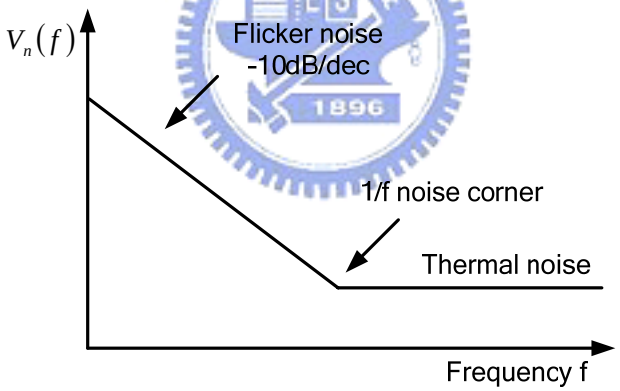


Figure 2-6 Noise spectrum of the MOSFET

The total noise voltage of the MOSFET can be written as

$$\overline{V_n^2}=\frac{K}{C_{ox}WL}\cdot\frac{1}{f}+4kT\left(\frac{2}{3}\cdot\frac{1}{g_m}\right). \tag{2.4}$$

Figure 2-6 shows the noise power spectrum. There is an intersection point between flicker noise and thermal noise. It is called “corner frequency” or “1/f noise corner”. It happens when the flicker noise power is equal to the thermal noise power. The equation can be derived as

$$\frac{K}{C_{ox}WL}\cdot\frac{1}{f_c}=4kT\left(\frac{2}{3}\cdot\frac{1}{g_m}\right). \tag{2.5}$$

The 1/f noise corner is derived as

$$f_c=\frac{K}{C_{ox}WL}\cdot\frac{3}{8kT}\cdot g_m. \tag{2.6}$$

2.3 Dynamic Offset Cancellation Techniques

Many bio-chips or sensor ICs deal with the signals in millivolt range. However, in CMOS IC technology, the offset of ordinary analog integrated circuits are also in millivolt range. Therefore, IC designers have developed many ways to reduce the offset. There are three common solutions. First, one can use larger devices with certain layout technique. The process variation and lithographic errors cause the mismatch of the differential pairs and introduce the offset. According to the mismatch model (2.7), the mismatch of the threshold voltage is inversely proportional to the device area.

$$\sigma(\Delta V_t)=\frac{A_{Vt}^2}{W\cdot L}. \tag{2.7}$$

Where A_{Vt} is the mismatch parameter (mV/μm).

Nevertheless, larger device area means higher cost. Second, one can use laser trimming. But, it needs extra test infrastructures. Third, one can use dynamic offset cancellation techniques. The last one is preferable to others for excellent long term stability and moderate costs. The following sections introduce auto-zeroing and chopping techniques.

Auto-zero Amplifier (AZA)

Figure 2-7 shows an auto-zeroing (AZ) example. There are two modes of operation: an auto-zero phase and an amplification phase. In the auto-zero phase (ϕ=1), the amplifier samples the offset and then store on the capacitor. After settling, the offset on the capacitor is $V_{OS}\cdot\frac{A}{A+1}$. In the amplification phase (ϕ=0), the output signal is available. Since the flicker noise and offset is highly correlated with the next sample, it can be subtracted from the amplified input signal. Finally, the offset at the output is $\frac{V_{OS}}{A+1}$.

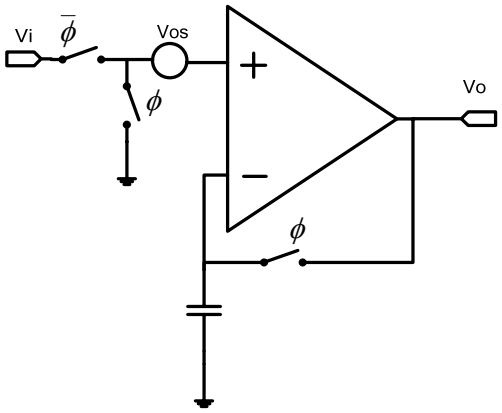


Figure 2-7 Auto-zeroing technique

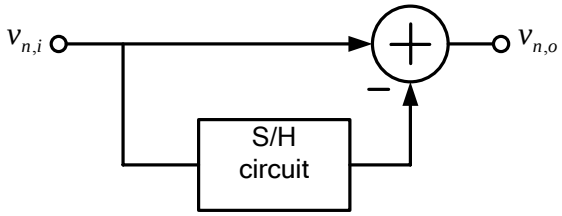


Figure 2-8 Auto-zeroing concepts

Conceptually, the system behavior is shown in Figure 2-8. Let H(f) be the transfer function of S/H circuit, and the noise transfer function is

$$v_{n,o}(f) = v_{n,i}(f) \cdot (1 - H(f)). \tag{2.8}$$

We know that

$$H(f) = \sin c(f). \tag{2.9}$$

Since $(1 - H(f))$ is a high-pass transfer function, the offset and 1/f noise can be reduced. However, the disadvantage of AZ is the noise fold-over. Figure 2-9 and 2-10 illustrate the phenomenon. If there is input noise frequency higher than Nyquist rate, the under-sampled output noise will be folded over to DC.

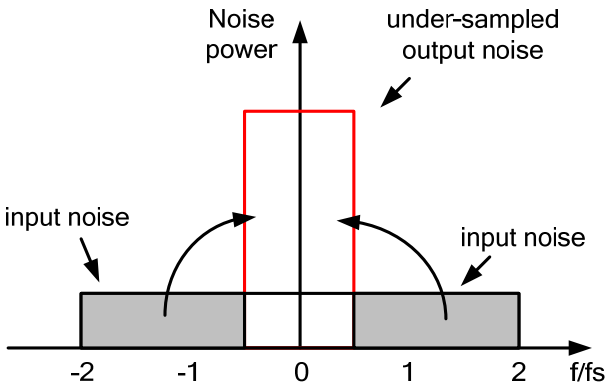


Figure 2-9 Out of band input noise is folded over to DC

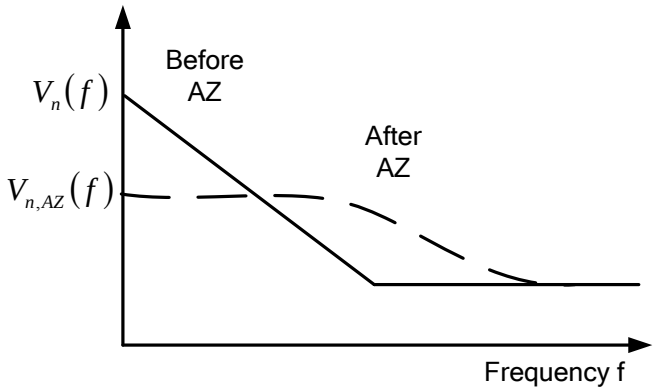


Figure 2-10 Residual noise of AZ impacts on the noise spectrum

Chopper-Stabilized (CHS) Amplifier

The chopper applies frequency modulation to the signals. Figure 2-11 shows the chopper modulation example and Figure 2-12 illustrates the chopping in frequency domain. The low frequency input signal is modulated, amplified and then demodulated back to DC while the offset and flicker noise is modulated to high frequency. Eventually, the high frequency component can be suppressed by a low-pass filter. Unlike discrete operation of AZA, the CHS output signal is continuously available.

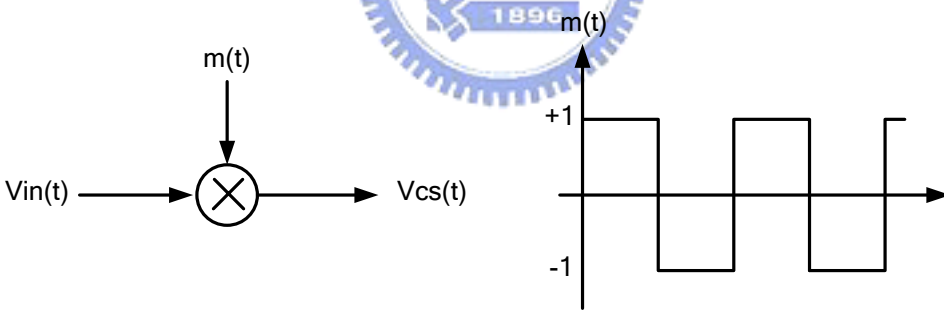
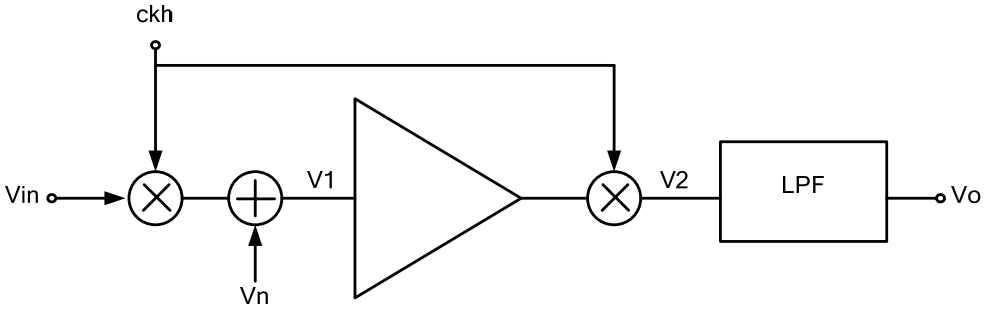


Figure 2-11 The input signal Vin(t) is multiplied by carrier signal m(t) and transposed to a higher frequency where is no flicker noise.



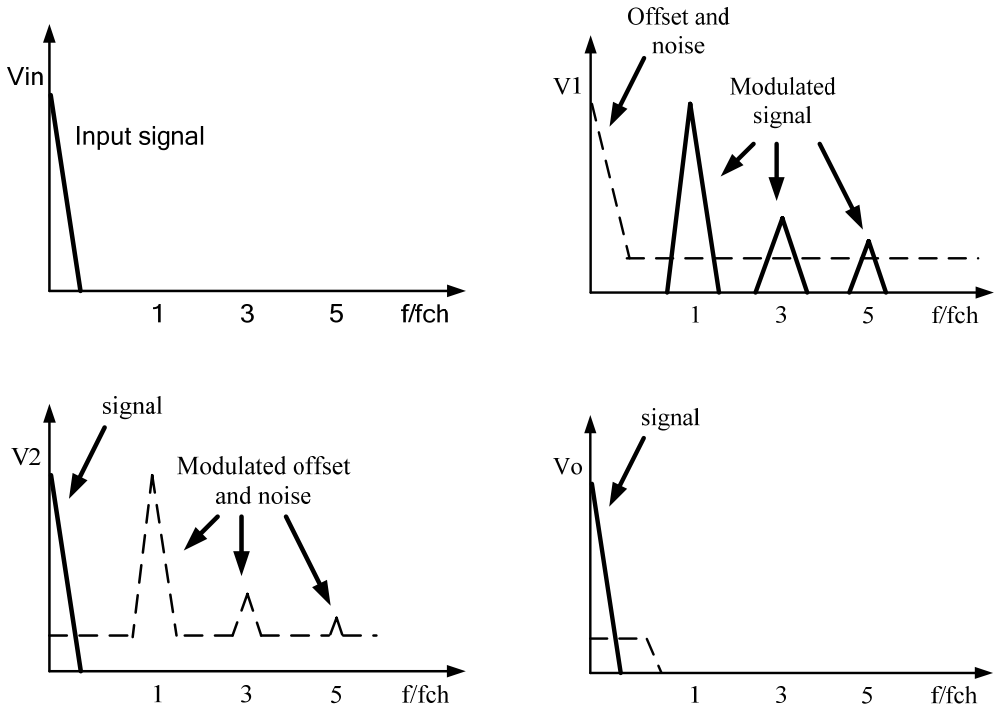


Figure 2-12 CHS in frequency domain

If the chopping frequency is much larger than corner frequency and the amplifier is ideal, the flicker noise is removed completely after chopping. Figure 2-13 shows the noise spectrum of CHS.

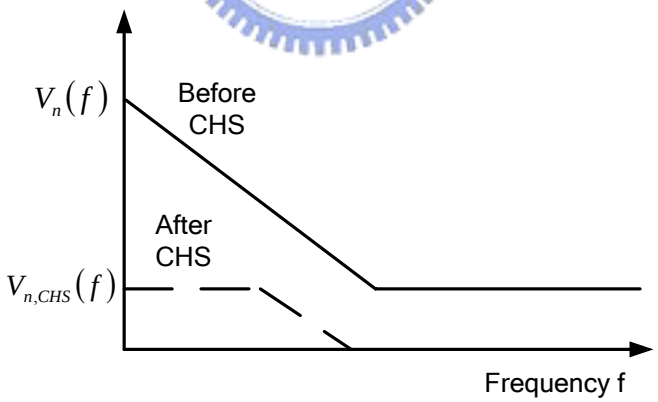


Figure 2-13 Residual noise of CHS

On the subject of time domain analysis, given a DC input signal and infinite amplifier bandwidth, the modulated signal is a square wave. In practical, the amplifier bandwidth is finite and it needs settling time. Figure 2-14 shows the difference. The actual demodulated DC signal is less than ideal one. Thus, the limited amplifier bandwidth reduces the effective gain (2.10).

$$A_{eff} = A_{nom}\left(1 - 4\tau/T\right) \tag{2.10}$$

Where $f_{ch} = 1/T$ and $\omega_{-3dB} = 1/\tau$. For example, if the amplifier bandwidth is ten times the chopping frequency, the gain error is about 6.37%

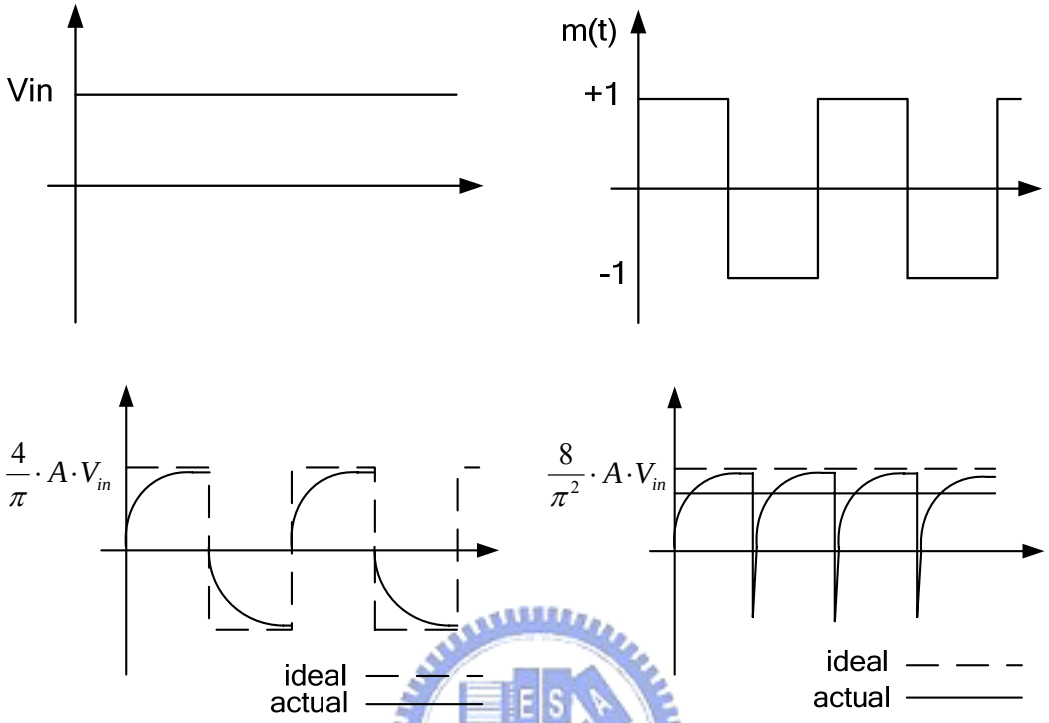


Figure 2-14 CHS in time domain

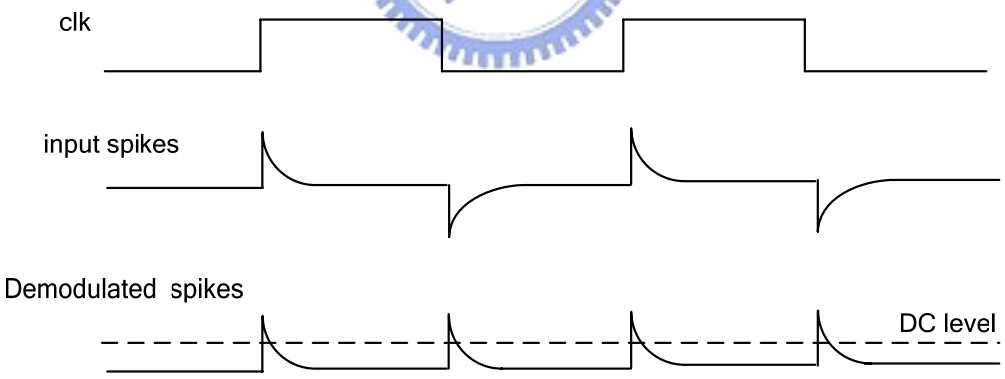


Figure 2-15 Spikes and the residual offset due to finite bandwidth

The charge injection of the switches at the input chopper introduces spikes. After filtering, the spikes become the DC component of the signal. It is residual offset of the chopper amplifier. The magnitude of the residual offset can be derived as

$$\text{Residual offset} = 2f_{ch}V_{spike}\tau. \tag{2.11}$$

Where f_{ch} is the chopping frequency, V_{spike} is the spike magnitude, and τ is the

settling time constant.

In a low supply voltage environment, the residual offset is crucial. To reduce the residual offset, the smaller settling time constant and low chopping frequency are preferred. However, at a given residual offset, the smaller settling time constant means more power consumption and low chopping frequency has more 1/f noise component. Thus, a trade-off between power and performance is required here.

2.4 AC Coupled Chopper-Stabilized Amplifier with AC feedback circuits

For biomedical applications, the conventional chopper-stabilized amplifiers or auto-zero amplifiers cannot satisfy the requirements. There are three problems. The first one is on the difference of the electrode common-mode voltage and the circuits input common-mode voltage. The electrodes common-mode voltage varies with time and is even lower than the earth ground. Using two chopper-stabilized amplifiers with nMOS and pMOS input pairs achieve rail-to-rail input stage [7]. However, it requires two power supply and extra area overhead. The modern solution is the one of AC coupled input stage. It blocks the common-mode signal and let differential signals go through. The second one is differential electrode offset (DEO) issue. For conventional Ag/AgCl electrodes, the DEO is as high as 50mV and varies with time. Because the chopper-stabilized amplifier is inherently DC coupled system, DEO may causes the amplifier to saturate and be out of operation point. Thus, a high-pass filter is required before amplification. Using external passive components before amplifier or differential difference amplifier with resistive feedback circuits are ways to solve DEO. However, the former degrades the signal-to-noise ratio (SNR) and the latter consumes excessive power. Here, an AC feedback circuits filters the DEO without extra costs.

Figure 2-16 shows the proposed architecture. It consists of a capacitive closed-loop chopper-stabilized amplifier with a DC gain A, a Gm-C filter, and an AC feedback circuits with a loop gain 1/K. Before going through the system, the input signal is modulated and transposed to high frequency before the 1/f noise is mixed. After amplification, the noise is modulated to high frequency. Since the signal is modulated twice, the output signal is demodulated back to low frequency signal. If there is a DEO at the input electrodes, the amplifier enters into the saturation region and output goes up to VDD or VSS. At the moment, the Gm-C filter integrates the output signal, extracts the DC component and then feedback to the system and cancel the DEO. Eventually, the system is back to the operation point.

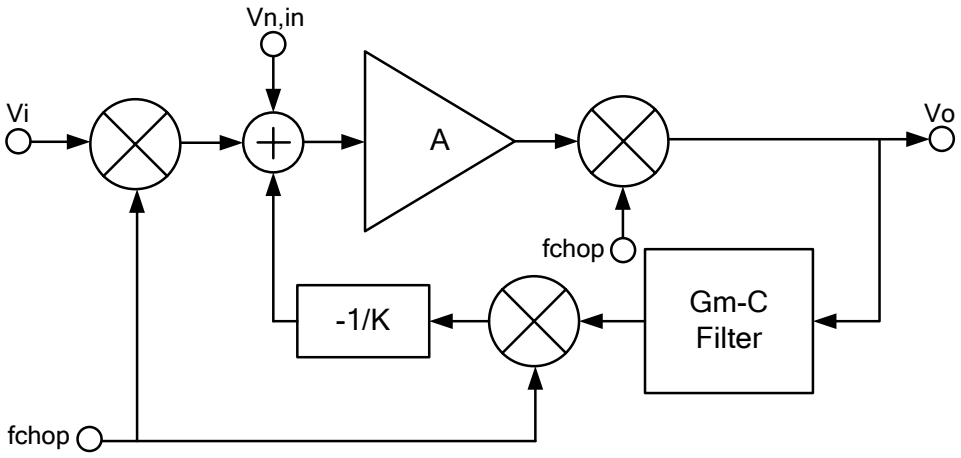


Figure 2-16 AC Coupled Chopper-Stabilized Amplifier with AC feedback circuits block diagrams.

The transfer function can be derived as

$$H(s)=V_o(s)/V_i(s)=A\cdot\frac{1}{1+s/\omega_{LP}}\cdot\frac{1}{1+\omega_{HP}/s}. \quad (2.12)$$

If 1/K is finite, the output offset to input offset transfer function is obtained as

$$V_{o,DC}=V_{i,DC}\cdot\frac{A}{1+A/K}. \quad (2.13)$$

The output noise is finally transposed to high frequency. It is derived as

$$S_{n,out}(f)=\left(\frac{2}{\pi}\right)^2\cdot\sum_{\substack{n=-\infty\\ n\,odd}}^{+\infty}\frac{1}{n^2}\left|A(f-n\cdot f_{chop})\right|^2\cdot S_{n,in}(f-n\cdot f_{chop}) \quad (2.14)$$

It is evident that the system has a band-pass characteristic. It blocks DEO and suppresses unwanted high frequency noise.

2.5 Summary

In order to deal with the bio-potentials, the low noise analog front-end amplifier plays an important role. Apparently, the AZA only reduces flicker noise, without limiting the amplifier bandwidth; the CHS eliminates the flicker noise, but limits the amplifier bandwidth. However, the conventional CHS is a DC coupled system and unable to handle the biomedical signals for DEO and different common-mode voltage issues. Thus, an AC coupled chopper-stabilized amplifier with AC feedback circuits is proposed. The architecture blocks a DEO and tolerates the electrodes common-mode voltage variance.

Chapter 3

Fundamentals of Low-Voltage Low-Power Successive Approximation Register Analog-to-Digital Converter

3.1 Introduction

In general, the signal process is preferred to be done with digital approaches than analog ones. Because digital signal processor (DSP) has large noise margin and is insensitive to circuit imperfection. Furthermore, powerful DSP is able to perform complex algorithms or execute programs. The natural signals are continuous-time analog, so an analog-to-digital converter (ADC) is essential. The quality of the digital signals depends on the ADC performance. Nevertheless, there are many non-ideal factors, such as quantization error, thermal noise and non-linearity, degrades the ADC performance. The design issues are more crucial for low voltage circuits. In this chapter, an low voltage low-power successive approximation register (SAR) analog-to-digital converter is stated. Section 3.2 introduces the SAR ADC based on charge redistribution approach. Section 3.3 describes the modern low-voltage design techniques. Section 3.4 presents the proposed SAR ADC circuits. Section 3.5 states the SAR implementation in CMOS technology. Section 3.6 makes a brief summary of this chapter.

3.2 Successive Approximation Register Analog-to-Digital Converter Based on a Charge Redistribution Principles

The major advantage of SAR ADC is simple and low power. Because the SAR ADC does not need opamp, it is a preferable architecture for low-speed medium-resolution application. Figure 3-1 describes the SAR ADC concepts. The conventional SAR ADC consists of a digital-to-analog converter (DAC), a comparator and a SAR. The basic principle is that the DAC produces a voltage and then does the binary search for the input voltage. Therefore, it requires at last N conversion cycles for N-bit resolutions.

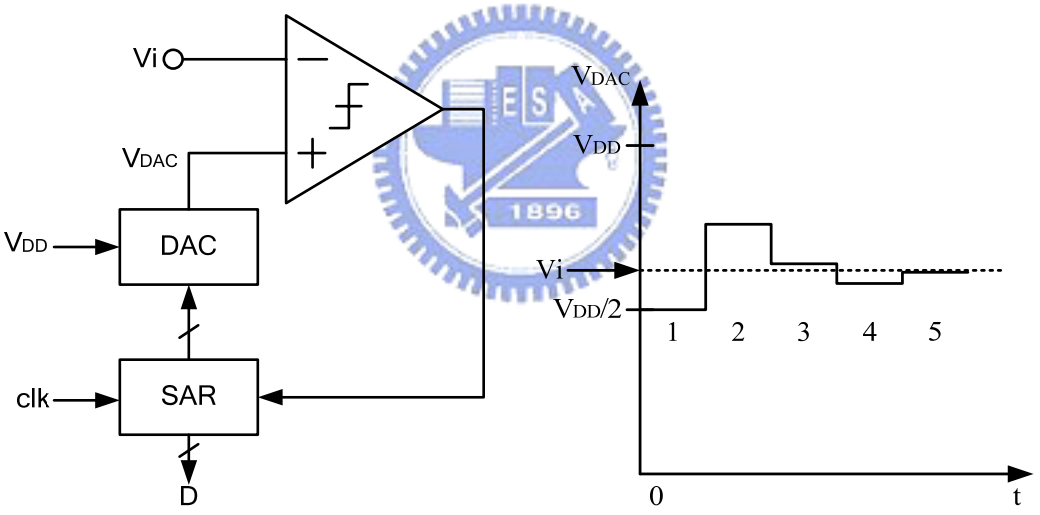


Figure 3-1 SAR ADC architecture

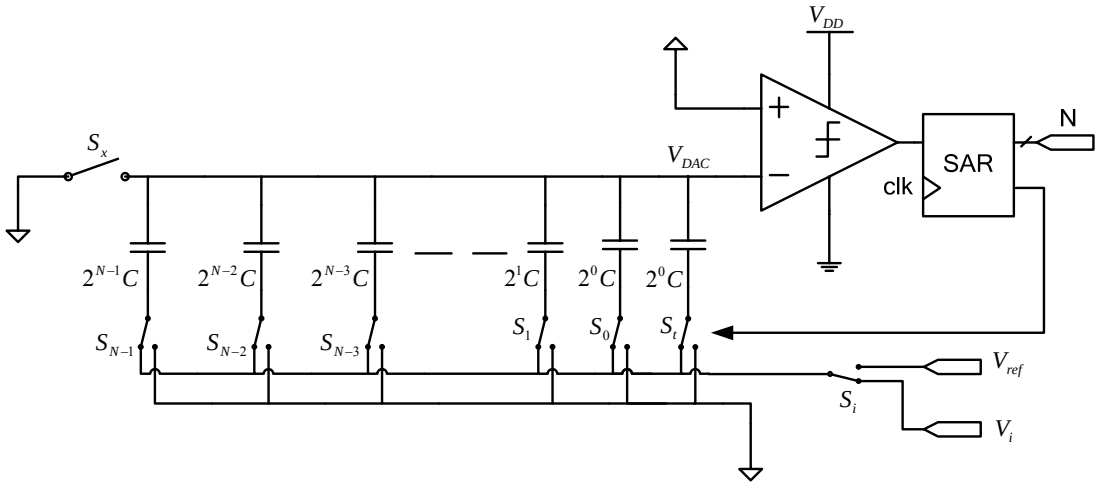


Figure 3-2 Charge-redistribution SAR ADC

Theoretically, it needs N+1 conversion cycles for N-bit resolutions. The additional conversion cycle initiates all registers and resets the comparators. Figure 3-2 shows the general SAR ADC based on charge-redistribution architecture.

The total capacitance for N-bit DAC is derived as

$$C_{total} = \sum_{i=0}^{N-1} 2^i \cdot C + 2^0 \cdot C = 2^N \cdot C. \quad (3.1)$$

Assume AGND stands for analog ground, V_i represents the input signal, and V_{ref} is the reference voltage. There are three modes of operations: Sample, hold and redistribution.

1. Sample Mode
   - S_x is switched to AGND
   - S_i is switched to V_i
   - S_t, S_0, S_1, S_{N-1} are switched to V_i
   - $V_{DAC} = 0$
2. Hold Mode
   - S_x open
   - S_t, S_0, S_1, S_{N-1} are switched to AGND

- $V_{DAC} = -V_i$

3. Redistribution Mode

- S_i is switched to V_{ref}
- Binary search, resolve one bit at a time. Starting with MSB b_{N-1}
- Bit b_{N-1} conversion
  - S_{N-1} is switched to V_{ref}
  - $V_{DAC} = -V_i + \frac{2^{N-1} \cdot C}{C_{total}} \cdot V_{ref} = -V_i + \frac{V_{ref}}{2}$
  - If V_{DAC}<0, b_{N-1}**=1,** $S_{N-1} \rightarrow V_{ref}$
  - If V_{DAC}>0, b_{N-1}**=0,** $S_{N-1} \rightarrow$AGND
- Bit b_j conversion, j=N-2, N-3,…,0
  - S_j is switched to V_{ref}
  - $V_{DAC} = -V_i + \frac{V_{ref}}{2^N} \cdot \sum_{k=j+1}^{N-1} b_k \cdot 2^k + \frac{2^j \cdot C}{C_{total}} \cdot V_{ref}$
  - If V_{DAC}<0, b_j**=1,** $S_j \rightarrow V_{ref}$
  - If V_{DAC}>0, b_j**=0,** $S_j \rightarrow$AGND

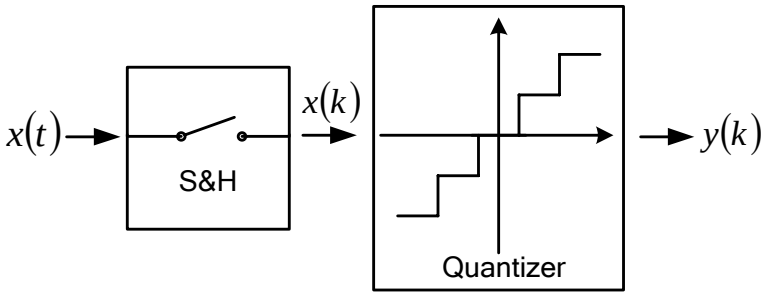
Eventually, V_{DAC} is represented as

$$V_{DAC} = -V_i + \frac{V_{ref}}{2^N} \cdot \sum_{i=0}^{N-1} b_i \cdot 2^i . \quad (3.2)$$

In order to avoid leakage of S_x, the analog ground is set to $V_{DD}/2$ and the input range is from $V_{DD}/2$ to V_{DD}. And switches are implemented as CMOS switches. After conversion, in ideal case, V_{DAC} is close to V_i and the difference should be smaller than half of the least significant bit (LSB). However, comparator's finite bandwidth, noise and the parasitic effect degrades the ADC performance. Next, the analyses of quantization noise and capacitor mismatch are stated.

Quantization Noise Analysis

The function of ADC is basically a quantization process. The continuous-time input signal $x(t)$ is converted to discrete-time signal $x(k)$ and then quantized to digital signal $y(k)$. Figure 3-3 describes the ADC quantization process model and its linear model.



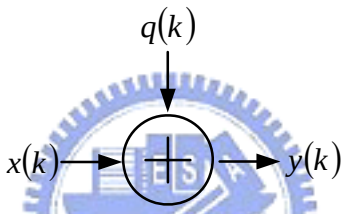


Figure 3-3 Quantizer linear model

The quantization noise is represented as

$$q(k) \equiv y(k) - x(k). \tag{3.3}$$

Noise power is derived as

$$P_n = \int q^2 \cdot pdf(e) \cdot dq = \frac{1}{12} \cdot \Delta^2. \tag{3.4}$$

Where pdf represents the probability density function, shown in Figure 3-4 and Δ is the difference between two adjacent quantization levels

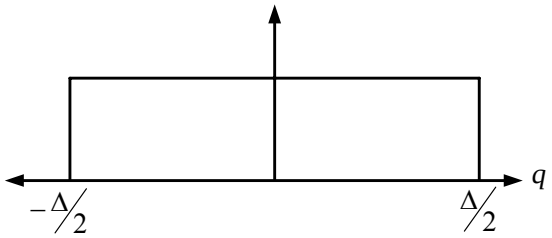


Figure 3-4 PSD of the quantization noise

Assume that the quantization noise $q(k)$ uniformly distributes within the Nyquist

frequency. Let f_s be the sampling frequency, f_i is the input signal frequency, input $x(k)$ is the sinusoidal wave with an amplitude A.

$$x(k) = A \cdot \sin\left(2\pi f_i k / f_s\right). \tag{3.5}$$

Signal power is derived as

$$P_s = \frac{1}{2} \cdot A^2. \tag{3.6}$$

(3.6) divided by (3.4), the signal-to-noise ratio (SNR) is obtained as

$$SNR = \frac{P_s}{P_n} = 6 \cdot \frac{A^2}{\Delta^2}. \tag{3.7}$$

If input signal amplitude A is the half of the full scale amplitude, SNR is rewritten as

$$SNR = \frac{3}{2} \cdot 2^{2N} = 6.02 \cdot N + 1.76dB. \tag{3.8}$$

Thus, in order to obtain the highest SNR, the input signal is demanded to be amplified as large as possible.

Capacitor Mismatch Analysis and Parasitic Effect

The performance depends on the accuracy of DAC. It is composed of passive components, such as capacitors or resistors. Unfortunately, metal or temperature gradient variation causes a component mismatch problem. According to the mismatch model (3.9), the mismatch of the capacitors is inversely proportional to the device area. Thus, there is a trade-off between cost and accuracy. In general, the charge-redistribution DAC with a resolution over 10bits requires calibrations or trimming.

$$\frac{\sigma(\Delta C)}{C} = \frac{A_C}{\sqrt{W \cdot L}}. \tag{3.9}$$

For a charge-redistribution DAC, the output voltage is

$$V_{DAC} = V_{ref} \cdot \frac{C}{2^N \cdot C + C_p} \cdot \sum_{i=0}^{N-1} b_i \cdot 2^i. \tag{3.10}$$

If there is a capacitor mismatch, the DAC output voltage has an error and

introduces differential non-linearity (DNL) and integral non-linearity (INL). INL is derived as

$$\left|INL\right|_{\max} = 2^{N-1} \cdot \left(C + \left|\Delta C\right|_{\max,INL}\right) - 2^{N-1} \cdot C = 2^{N-1} \cdot \left|\Delta C\right|_{\max,INL}. \quad (3.11)$$

Where C is the unit capacitance and the maximum ΔC that will result in an INL which is less than $1/2 \cdot LSB$ is

$$\left|\Delta C\right|_{\max,INL} = \frac{C}{2^N}. \quad (3.12)$$

DNL is defined by

$$DNL_{\max} = \left(2^N - 1\right) \cdot \left|\Delta C\right|_{\max,DNL}. \quad (3.13)$$

With the maximum ΔC, which leads to a DNL less than $1/2 \cdot LSB$ is

$$\left|\Delta C\right|_{\max,DNL} = \frac{C}{2^{N+1} - 2}. \quad (3.14)$$

Besides, the parasitic capacitance causes gain error. Higher resolution requires larger capacitance and more area to reduce the mismatch. It leads to more severe parasitic effect and requires higher comparator gain. Thus, there is a trade-off bewteen accuracy and power.

3.3 The Proposed 11-b Low-Voltage Low-Power SAR A/D converter

Under the low supply voltage environment ($\left|V_{thp}\right| + \left|V_{thn}\right| > V_{DD}$), there are many design challenges. For the conventional SAR ADC, there are two problems. First, CMOS switches cannot work efficiently. If input voltage is at the middle of the supply voltage, neither NMOS nor PMOS is unable to turn on. Second, input range is limited to half of the full scale voltage. In order to solve the problem, the novel low-voltage SAR ADC is presented.

The conventional successive approximation algorithm uses a DAC to binary search the input voltage. The proposed algorithm is adds or subtracts by the DAC voltage to binary search $V_{DD}/2$. It is shown in Figure 3-5. There are two advantages. First, it achieves rail-to-rail input range without a rail-to-rail comparator. Second, it adopts a grounded-switches technique. It means all switches are only switched to

V_{DD} or V_{SS}. Thus, it is easy to provide adequately low switch on-resistance.

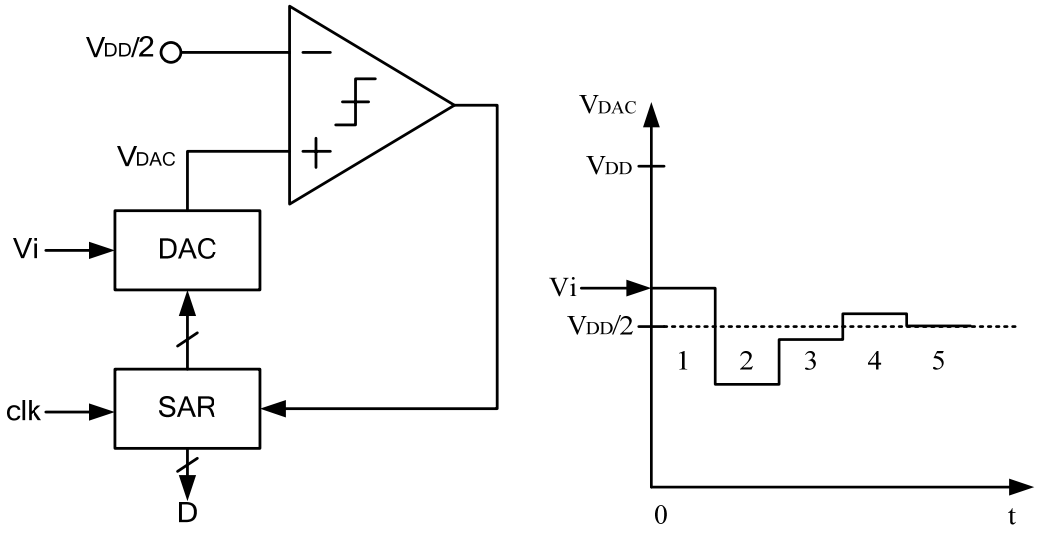


Figure 3-5 Proposed SAR ADC architecture

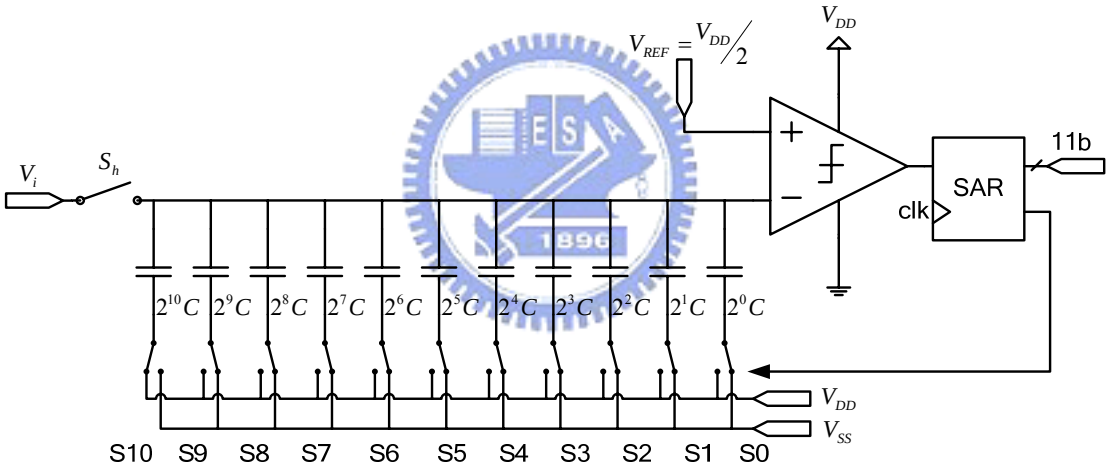


Figure 3-6 A 11-bit low-power and low-voltage SAR ADC

Because the front-end amplifier has a 70dB dynamic range (DR), a 11-bit SAR ADC is integrated. It is shown in Figure 3-6. The switch S_h is bootstrapped. It provides a rail-to-rail input range. And the others switches are grounded-switches. The switching operations are controlled by the successive approximation register (SAR). The whole operation is as follows.

Let N=10, i=0

- Sample mode
  - Sh close
  - S10 $\rightarrow V_{DD}$, S0-S9 $\rightarrow V_{SS}$

- Hold mode
  - Sh open
  - test b_N
  - Comparator activated and compared V_{DAC} with $V_{DD}/2$
- Redistribution mode (i conversion cycle)
  - As clk 0->1
    - If $V_{DAC} > V_{DD}/2$, $b_{N-i}=1$, $b_{N-i} \rightarrow V_{SS}$
    - If $V_{DAC} < V_{DD}/2$, $b_{N-i}=0$, $b_{N-i} \rightarrow V_{DD}$
    - Comparator reset
    - i=i+1, test $b_{N-i} \rightarrow V_{DD}$
  - As clk 1->0
    - Comparator activated and compared V_{DAC} with $V_{DD}/2$

Finally, the DAC output voltage V_{DAC} is close to $V_{DD}/2$. It is represented as.

$$V_{DAC} = V_{in} + \sum_{i=0}^{10} (-1)^{b_{N-i}} \cdot V_{DD}/2^{i+2}. \quad (3.15)$$

Comparator

The comparator plays an important role in SAR ADC. In order to minimize the power consumption, there is only one current branch in this design. The comparator is shown in Figure 3-7. It includes a preamplifier and a latch. The configuration has three advantages. First, a weak-inversion input pair maximize the g_m/I_D ratio. Second, PMOS input pairs have less flicker noise than NMOS. It is good for low-speed applications. Third, the source and the body of the PMOS is tied together to reduce threshold voltage mismatch and avoid body effect. It also enhances the common-mode immunity and input common-mode range.

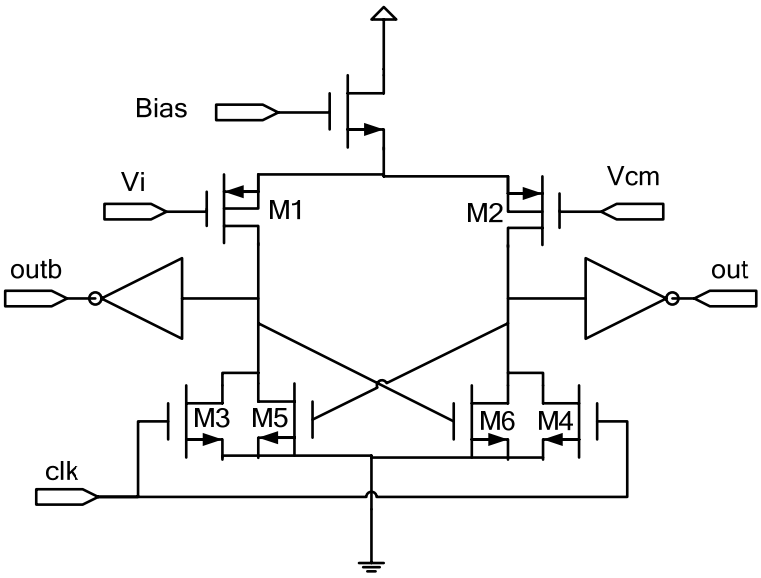


Figure 3-7 Latched comparator

The operation of the comparator is straightforward. There are two phases of operations. During the "reset" phase, M3 and M4 discharge the output nodes. In the phase, the comparator output is not available. The "compare" phase activates the latch and compares the difference. After settling, the comparator output is available. To determine current and transistor size, the analysis is as follows.

- In "compare" phase. Given a voltage difference ΔV, the ouptut function of time t is represented as

$$V_{out}(t) = \Delta V \cdot e^{t/\tau}. \tag{3.16}$$

Let t_a be the conversion period. The output is required to settle before the time ends.

$$V_{out}(t_a) = \Delta V \cdot e^{t_a/\tau} \geq V_{DD}. \tag{3.17}$$

Where the settling time constant $\tau = C/g_{m5}$ and it is has to be $(N+1)\cdot \ln 2$ times more than conversion period t_a

$$t_a/\tau = \ln\left(V_{DD}/\Delta V\right) = (N+1)\cdot \ln 2. \tag{3.18}$$

- In "reset" phase. The transistors M3 and M4 are fully turn on. Their resistance is represented as

$$R = 1/g_{m3}. \tag{3.19}$$

Considering the overdrive recovery issue. Assume the comparator is saturated and the

clock becomes high at t=0. If there is a input signal $\Delta V = {}^{1}\!/_{2} \cdot LSB$. The output function of time t is derived as

$$V_{out}(t) = (A \cdot \Delta V + I \cdot R) \cdot \left(1 - e^{-t/\tau}\right) - I \cdot R. \quad (3.20)$$

Where A is the comparator gain during "reset" phase, I represents the comparator tail current and τ stands for the ouput node time constant. The recovery time is defined by

$$V_{out}(t_{recovery}) = (A \cdot \Delta V + I \cdot R) \cdot \left(1 - e^{-t_{recovery}/\tau}\right) - I \cdot R = \Delta V. \quad (3.21)$$

$$\Rightarrow t_{recovery} = RC \cdot \ln\left[\frac{A \cdot \Delta V + I \cdot R}{(A-1) \cdot \Delta V}\right]. \quad (3.22)$$

In order to minimize the recovery time, it needs a high bandwidth and high gain comparator. However, higher bandwidth means more power consumption. Thus, there is a trade-off between speed and power.

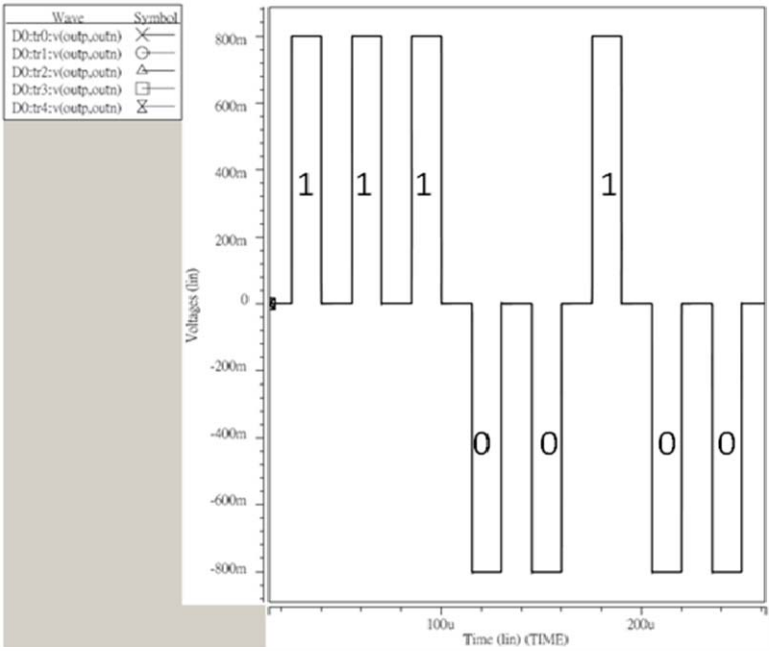


Figure 3-8 Given a input sequence {+0.5VDD, +0.25LSB, +0.5VDD, -0.25LSB, -0.5VDD, +0.25LSB, -0.5VDD, -0.25LSB }, the simulated output sequence={1, 1, 1, 0, 0, 1, 0, 0} under five corner cases (FF, FS, TT, SF, SS). Clock rate=32KHz

Thermal Noise

Due to the MOS resistance and parasitic resistance, there is a thermal noise at the DAC output during conversion. The resistive thermal noise can be modeled as a noiseless resistor series with a noise source. Thus, the equivalent model is shown in

Figure 3-9 for the MSB conversion cycle. Since MSB capacitor is connected to V_{DD} and the other capacitors are switched to V_{SS}, the equivalent capacitance is $2^9 \cdot C$. Thus, the thermal noise is derived as

$$\sqrt{\frac{KT}{2^9 \cdot C}} < \frac{1}{2} \cdot \Delta \tag{3.23}$$

Where K is the Boltzmann constant, T is the absolute temperature, and Δ represents a LSB.

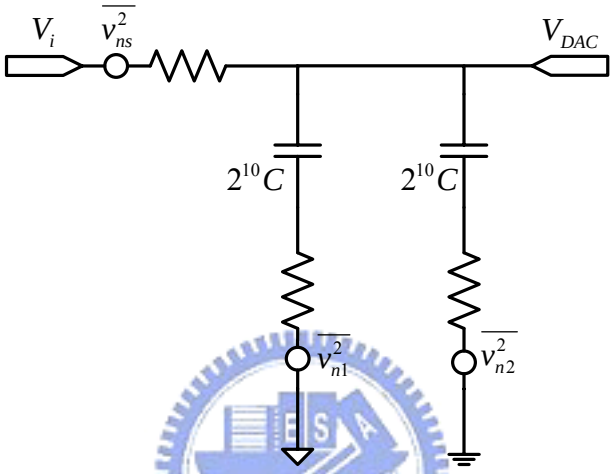


Figure 3-9 Thermal noise models as testing MSB

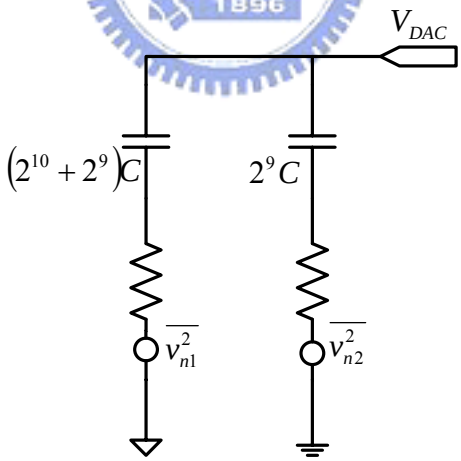


Figure 3-10 Thermal noise models during the next conversion after MSB

$$\sqrt{\frac{KT}{384 \cdot C}} < \Delta \tag{3.24}$$

In next conversion cycle, the thermal noise is modeled as shown in Figure 3-10. It shows the capacitance requirement is looser than the MSB. Thus, the thermal noise power is largest during MSB conversion. If it satisfies the requirement, the other bit

conversions will satisfy as well. In general, the thermal noise power should be less than the quantization noise power. Therefore, the unit-capacitance is known.

Voltage multiplier

For a low power supply, the conventional CMOS sampling switch is unable to offer adequate low switch-on resistance. In order to achieve the rail-to-rail input range, the bootstrapped technique is adopted. The sampling switch is implemented as NMOS switch. It is driven by the boosted clock driver shown in Figure 3-11. By the source and gate cross-coupled of M1 and M2 configuration, the capacitor C1 and C2 are charged alternatively. In steady state, the voltage drop across the capacitor C1 and C2 is V_{DD}. When the input clock becomes high, the output voltage is boosted to $2V_{DD}$. As the clock is low, M4 is turned on and the output is pull down to V_{SS}. Actually, the boosted output voltage cannot reach $2V_{DD}$ for the parasitic effect and charge sharing. In order to reduce the effect, capacitor C1 and C2 must be sufficiently large. Thanks for the light loading of the small sampling switch and the low speed clock rate, the power consumption of the boosted clock driver is as low as ten nano-watt of magnitude.

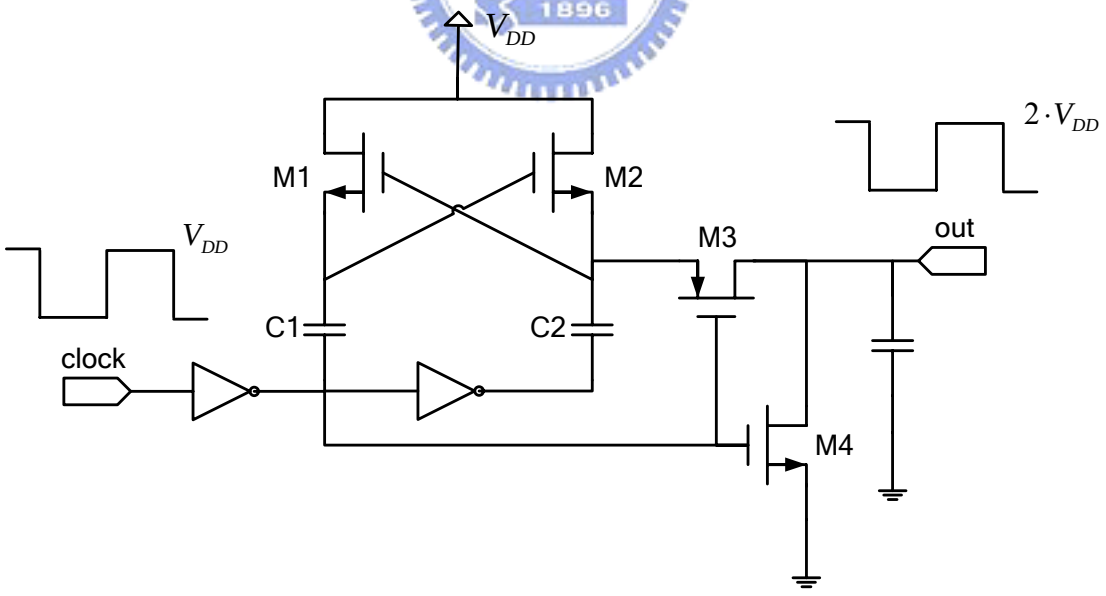


Figure 3-11 Boosted clock driver

3.4 Successive Approximation Register (SAR)

In this thesis, a CMOS successive approximation register is implemented. It is

composed of MUX, D flip-flop and simple logic circuits. In order to save the area, all transistors are of minimal size. All blocks are also implemented as standard cells. The sequential digital circuit is realized as a finite state machine shown in Table 3-1. A 11-bit SAR ADC requires 12 conversion cycles. During the first conversion cycle, SAR ADC samples the input signal and resets all registers. Note that the control signal S10 is reset to logic '1'. In second conversion cycle, the sampled signal is held. After settling, the comparator is activated and the first bit is extracted. The other conversion cycles are similar.

Table 3-1 SAR operation

Conversion Cycle	SAR output control signals											Cmp result
	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	
1	1	0	0	0	0	0	0	0	0	0	0	-
2	1	0	0	0	0	0	0	0	0	0	0	D10
3	D10	1	0	0	0	0	0	0	0	0	0	D9
4	D10	D9	1	0	0	0	0	0	0	0	0	D8
5	D10	D9	D8	1	0	0	0	0	0	0	0	D7
6	D10	D9	D8	D7	1	0	0	0	0	0	0	D6
7	D10	D9	D8	D7	D6	1	0	0	0	0	0	D5
8	D10	D9	D8	D7	D6	D5	1	0	0	0	0	D4
9	D10	D9	D8	D7	D6	D5	D4	1	0	0	0	D3
10	D10	D9	D8	D7	D6	D5	D4	D3	1	0	0	D2
11	D10	D9	D8	D7	D6	D5	D4	D3	D2	1	0	D1
12	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	1	D0

The whole block diagram of SAR is described in Figure 3-14 and the block details are shown in Figure 3-12 and Figure 3-13. It bahaves like a series shift register. When the global reset signal asserts, S10 is reset to '1' and S0-S9 are reset to '0'. As the conversion starts , the logic '1' is passed to the next block sequentially. After the conversion finishes, the global reset signal asserts again. All blocks and logic circuits are implemented as standard cells with minimial size.

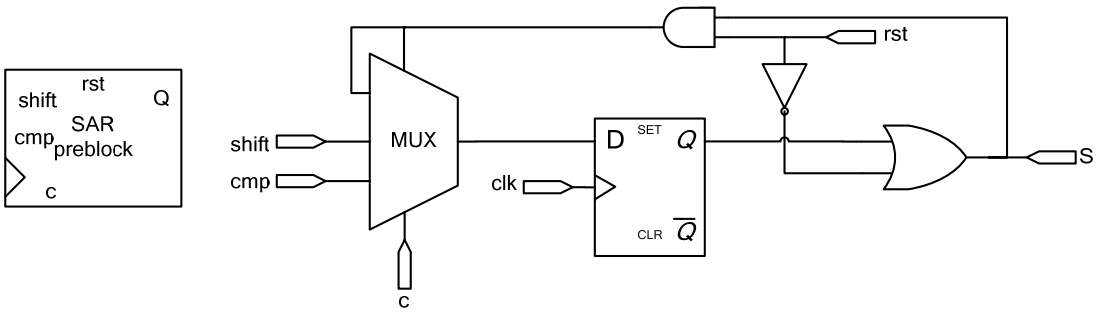


Figure 3-12 The first bit logic block of SAR

Table 3-2 The mux output versus the first control signal

S	c	Mux output
0	0	Shift
0	1	S
1	0	cmp
1	1	S

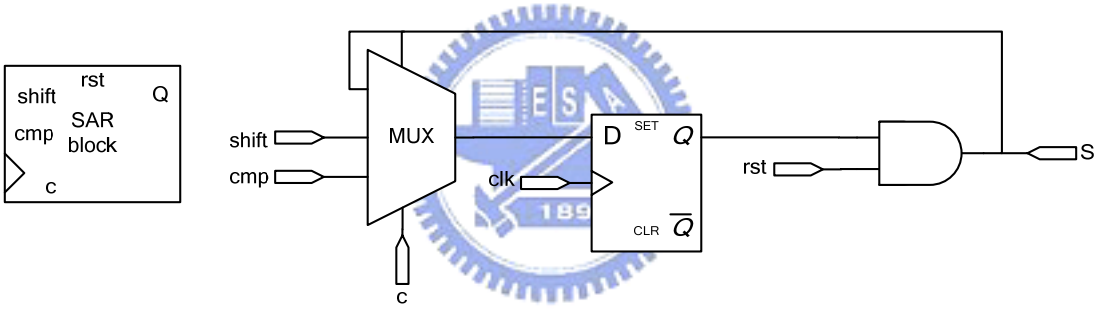


Figure 3-13 The other bit logic blocks of SAR

Table 3-3 The mux output versus the rest control signal

S	c	Mux output
0	0	Shift
0	1	S
1	0	cmp
1	1	S

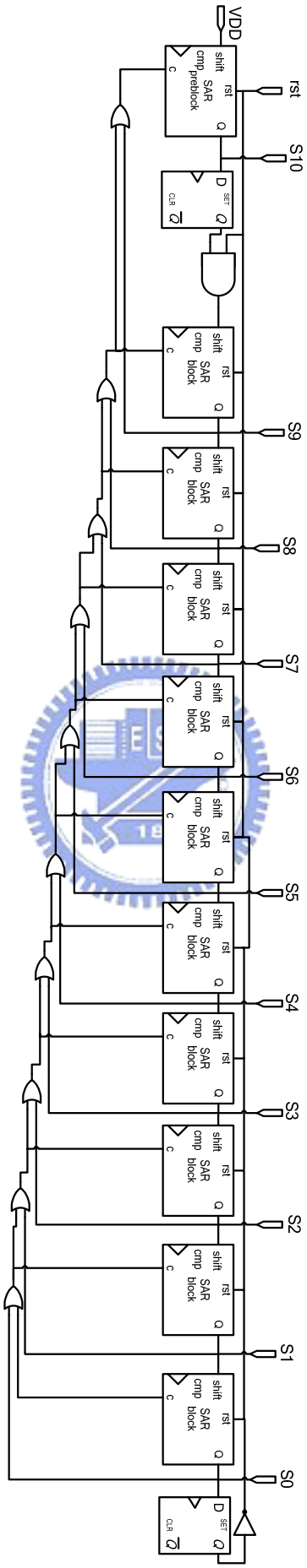


Figure 3-14 Successive approximation register architecture

Given an ideal comparator and capacitor array, the SAR simulation result is shown in Figure 3-15. The input signal 0 and V_{DD} are tested. Because the conversion results are the complements of the control signals in the thesis, the extracted bits are '000 0000 0000' and '111 1111 1111'.

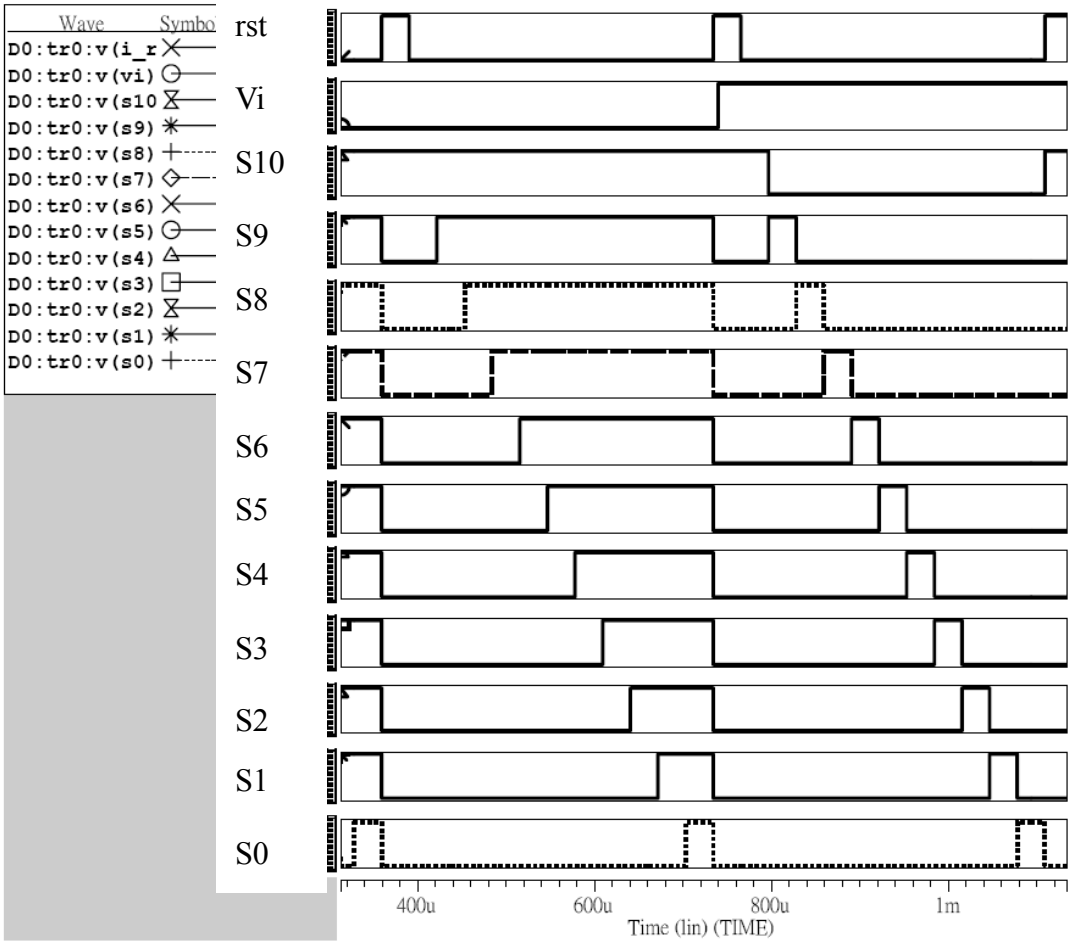


Figure 3-15 SAR simulation results

3.5 Simulation Results

Given a 402.7Hz 0.6Vp-p input sinusoidal signal, FFT simulation is shown in Figure 3-16. It has a SNR of 63.6dB, a SNDR of 63dB and a SFDR of 72.6dB. The power consumption is 0.31μW excluding the bias current. The clock rate is 32 KHz and the conversion rate is 2.67 KS/s. The supply voltage is 0.8V. Table 3-4 is the total corner simulation results. Because the threshold voltage is as high as 0.5V in the SS corner, it degrades the performance significantly. Figure 3-17 and Figure 3-18 are the simulated INL and DNL at the TT corner cases. Both of them are smaller than a LSB.

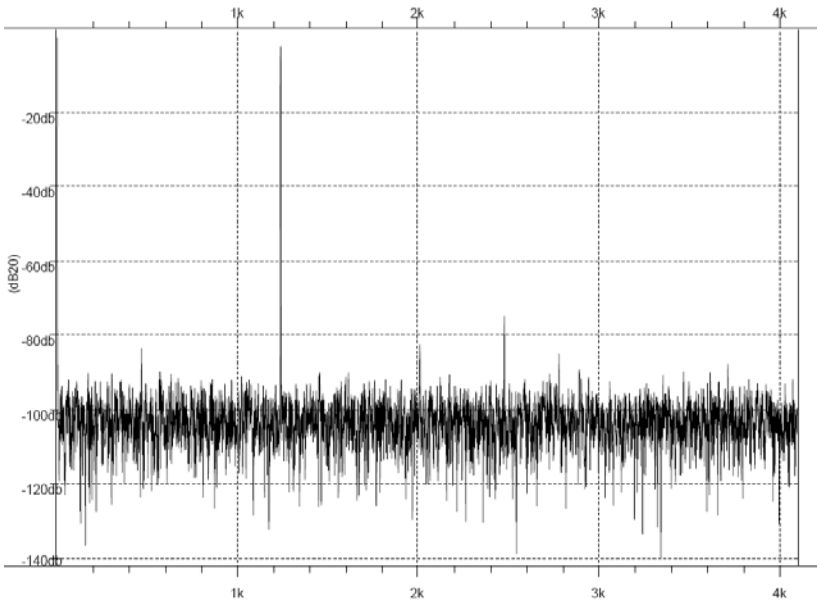


Figure 3-16 FFT simulation in TT corner @402.7Hz input signal and 0.6Vp-p swing

Table 3-4 SAR ADC performance versus different corner cases

Corner	TT	FF	SS
SNR	63.6dB	63.4dB	53.1dB
SNDR	63dB	62.4dB	52.6dB
ENOB	10.18b	10.08b	8.45b
SFDR	72.6dB	69.7dB	64. 7dB

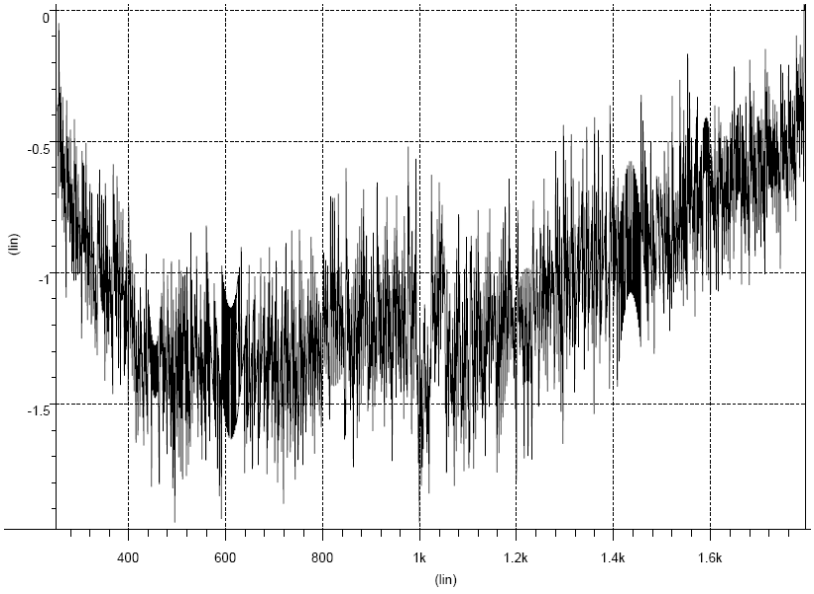


Figure 3-17 INL simulation in TT corner @402.7Hz input signal and 0.6Vp-p swing

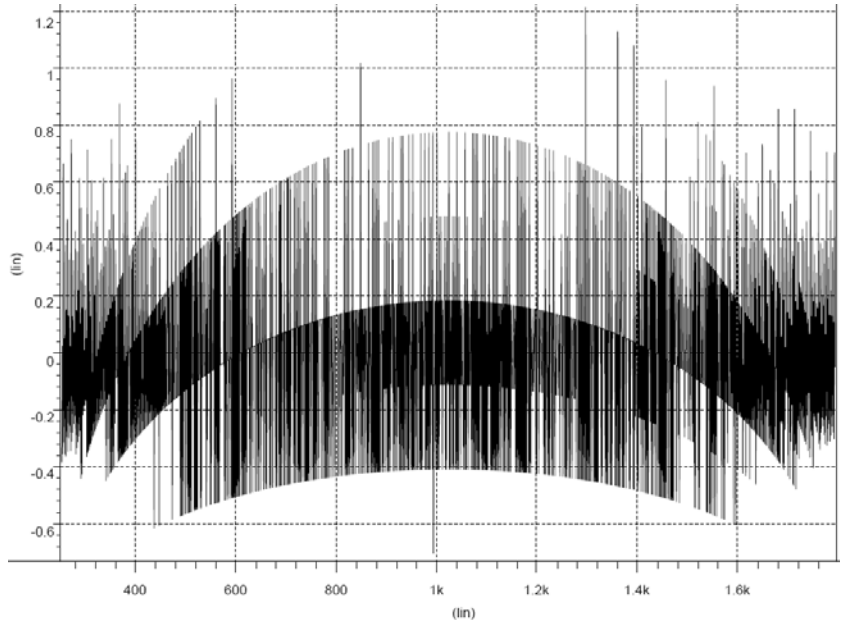


Figure 3-18 DNL simulation in TT corner @402.7Hz input signal and 0.6Vp-p swing

Given a capacitor mismatch 0.1% and 0.6Vpp sinusoidal input signal at 401.7Hz, the FFT simulation result is shown in Figure 3-19. It has a SNR of 65.27dB, SNDR of 66.83dB, THD of -70.5dB and ENOB of 10.55b. The INL and DNL simulations are shown in Figure 3-20 and Figure 3-21.

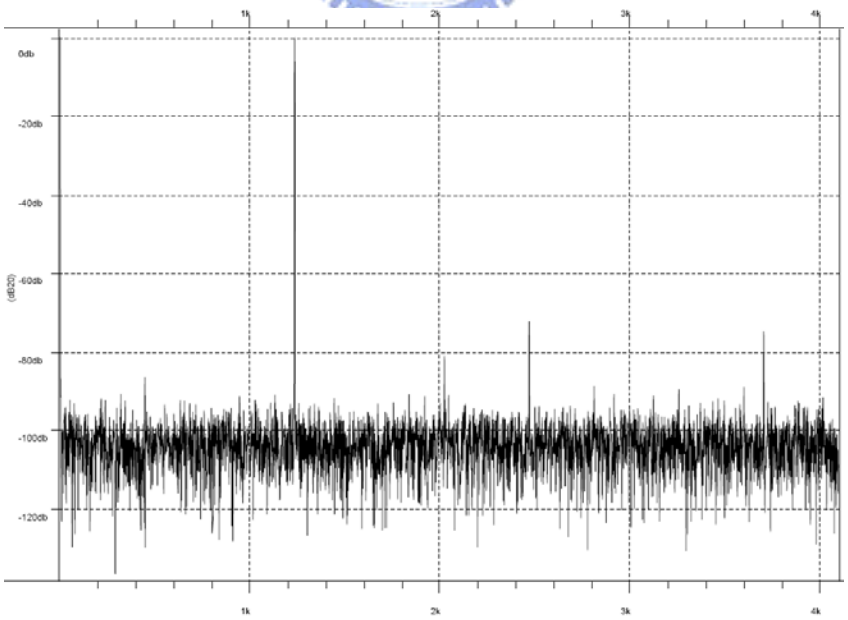


Figure 3-19 FFT simulation in TT corner @401.7Hz input signal and 0.6Vp-p swing with 0.1% capacitor mismatch

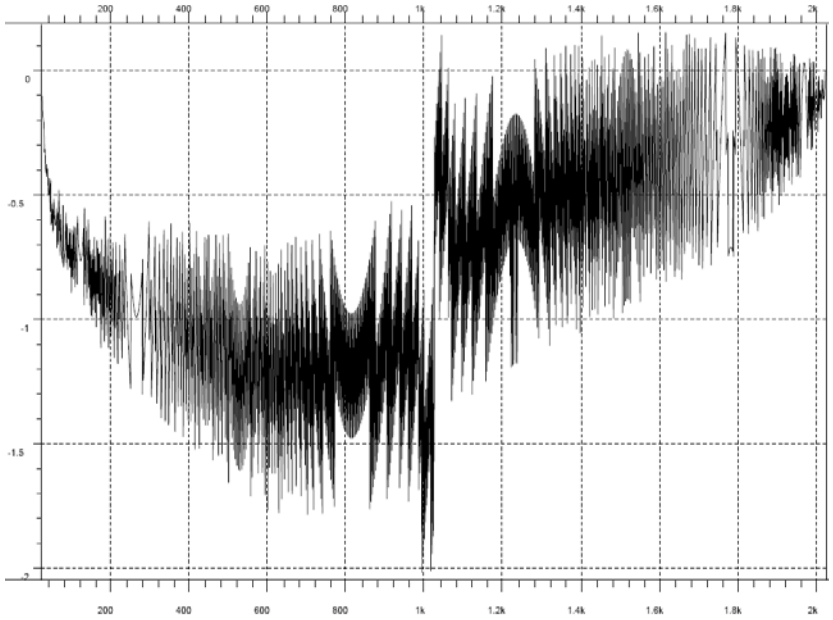


Figure 3-20 INL simulation in TT corner @401.7Hz input signal and 0.6Vp-p swing with 0.1% capacitor mismatch

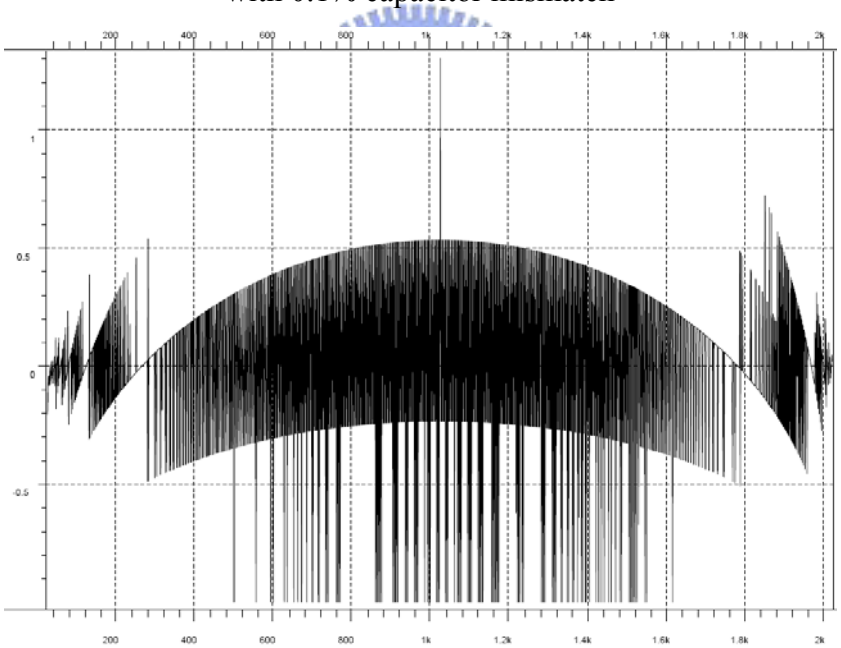
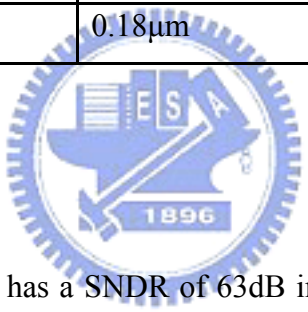


Figure 3-21 DNL simulation in TT corner @401.7Hz input signal and 0.6Vp-p swing with 0.1% capacitor mismatch

With a capacitor mismatch 0.1%, it leads to larger INL and DNL. It has a DNL of ± 1.15LSB and an INL of ± 1.085LSB. Nevertheless, the ENOB is above 10-b and satisfies the requirements.

Table 3-5 SAR ADC performance

Spec.	@fin=402.67Hz
# bits	11
VDD	0.8V
Pd (AVG)	0.31μW
SFDR	72.6 dB
SNR	63.6 dB
SNDR	63 dB
ENOB	10.18b
DNL	$< \pm 0.96 LSB$
INL	$< \pm 1 LSB$
Fs	2.67 KS/s
Input range	0.6V
Technology	0.18μm

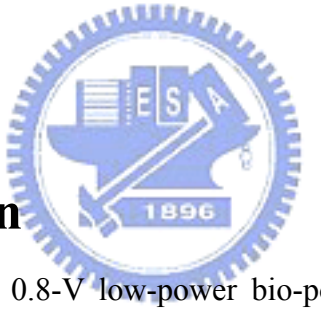


3.6 Summary

The proposed SAR ADC has a SNDR of 63dB in a low supply voltage of 0.8V and power consumption of 0.31μW. It adopts the novel successive approximation algorithm and grounded-switches techniques. The former achieves a rail-to-rail input common-mode range without a rail-to-rail input comparator. The latter provides sufficient low switch on-resistance. Besides, there is no opamp and only one current source in the whole architecture, so the power consumption is low.

Chapter 4

A 0.8-V Low-Power Analog Front-End IC for Biomedical Applications



4.1 Introduction

This chapter describes a 0.8-V low-power bio-potential readout front-end IC. Section 4.2 introduces the whole IC specification and design. Section 4.3 states the instrumentation amplifier and simulations. Section 4.4 presents the programmable gain amplifier and simulations. Section 4.5 includes the simulation results and the target spec. Section 4.6 states the measurement considerations. Section 4.7 presents the measurement results and the performance summary. Section 4.8 states the comparison with the state of the art.

4.2 AFE IC Design

The Proposed Digitally Programmable AFE IC

Figure 4-1 shows the proposed biomedical analog front-end (AFE). The skin electrodes Kendall H99SG provides the interface between body and the circuits. The instrumentation amplifier amplifies the signal while rejects common-mode noise. In order to accommodate different bio-potentials, the programmable gain amplifier offers

a variable gain controlled by digital interface. Finally, the 11-b SAR ADC converts the analog signal to digital signal.

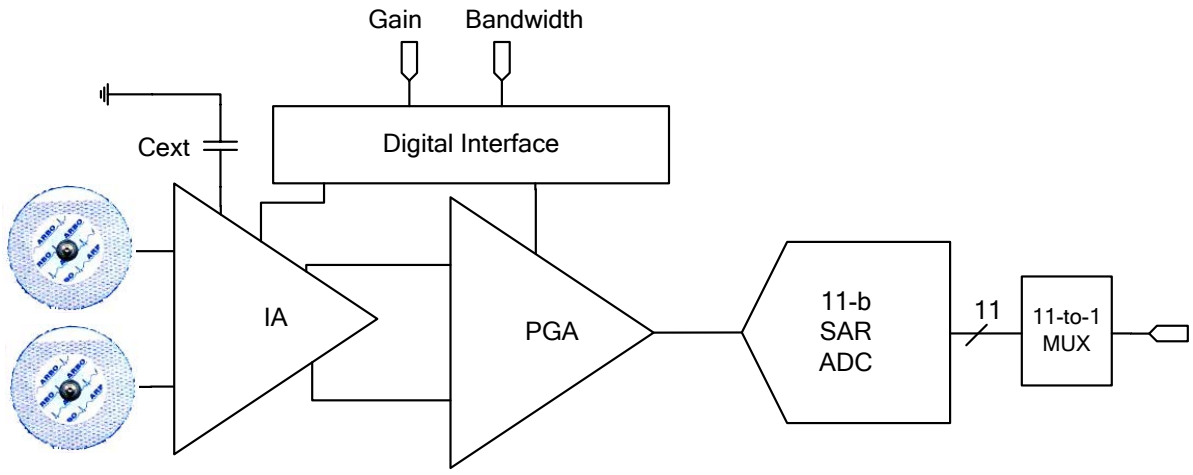


Figure 4-1 The proposed AFE IC

Design specifications

The specifications of the amplifier are listed in Table 4-1. In order to realize a long-term monitoring portable bio-potential acquisition IC, the supply voltage is chosen as low as 0.8V. It is low supply voltage poses lots of design challenges. Power budget upper bound is 5μW to ensure a lifetime of more than one year. The voltage gain has to be as large as possible for better data conversion. However, the limited voltage headroom in such low supply environment, the distortion issue is vital. Common-mode rejection ratio (CMRR) is the one of the most important issues in bio-potential acquisition analog front-end. Because a large 50/60Hz common-mode disturbance corrupts the signal quality, it needs a very high CMRR to purify the signal. According to International Federation of Clinical Neurophysiology (IFCN), CMRR must be at least 110dB for each channel. The total harmonic distortion (THD) must be less than 1%. According to dynamic range definition, the effective dynamic range is the largest input signal with THD<1% over the input-referred noise within the signal bandwidth. Thus, it is essential to make sure THD<1% for dealing with any biomedical signal. In order to obtain a 10-bit SNR, the dynamic range has to be over than 60dB. Besides, the noise performance is the key performance of the front-end amplifier. It determines the SNR. From Table 1-1, the input-referred noise should be less than 1μVrms for a 10-bit SNR.

Table 4-1 Specification of the front-end amplifier

Spec.	Value	Unit
Supply voltage	0.8	Volt
Power consumption	<5	μW
Gain	>40	dB
CMRR	110	dB
THD	<1	%
Dynamic range	>60	dB
Input-referred noise	1	μVrms (0.5Hz to 100Hz)
Bandwidth	0.5-100,400	Hz (programmable)

4.3 Instrumentation Amplifier

The concept of the AC coupled chopper-stabilized amplifier with AC feedback circuits is shown in Figure 2-16 and (2.12) derives the system transfer function. Figure 4-3 shows the simplified schematic. It includes a fully-differential folded-cascode opamp, a gm-c filter, three NMOS chopper and capacitors. Since the CMOS chopper is unable to work at a low supply voltage environment, the bootstrapped NMOS chopper is adopted without reliability issue. There are two feedback paths in the system. One is for setting the closed-loop gain and the other is for cancelling DEO. The capacitive closed-loop configuration dissipates less power than the resistive feedback one. Note that the demodulation of the signal is inside the opamp.

The transfer function is presented as

$$|H(s)| = v_o(s)/v_i(s) = \frac{C_i}{C_{fb}} \cdot \frac{1}{1+\frac{1}{A_o}\cdot\frac{C_i+C_{fb}+C_{hp}+C_p}{C_{fb}}} \cdot \frac{1}{1+s/\omega_{LP}} \cdot \frac{1}{1+\omega_{HP}/s}. \quad (4.1)$$

The low-pass cutoff frequency is derived as

$$\omega_{LP} = \omega_t \cdot C_{fb}/C_i. \quad (4.2)$$

And the high-pass cutoff frequency is derived as

$$\omega_{HP} = \frac{C_i}{C_{fb}} \cdot \frac{C_{hp}}{C_{fb}} \cdot \frac{G_m}{C}. \quad (4.3)$$

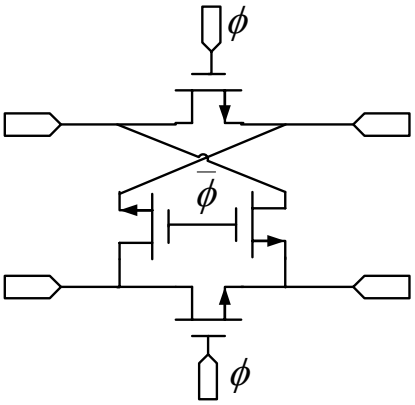


Figure 4-2 NMOS chopper

The midband gain is set by C_i/C_{fb} and the DEO cancelling loop gain is set by C_{hp}/C_{fb}. Let the amplifier thermal noise be $\overline{v_{ni}^2}$, the closed-loop input-referred noise is derived as

$$\overline{v_{ni,cl}^2} = \left(\frac{C_i + C_{fb} + C_{hp} + C_{p,i}}{C_i} \right)^2 \cdot \overline{v_{ni}^2}. \tag{4.4}$$

In order to reduce the thermal noise, the input capacitance C_i should be chosen as large as possible. But it increases the chip area and parasitic capacitance. Thus, there is a trade-off between the performance and area. In this thesis, the midband gain is set to be a little larger than 40dB to attenuate the parasitic effect. The input capacitance C_i is 16pF, the feedback capacitance C_{fb} is 0.15pF and the DEO feedback capacitance C_{hp} is 1pF. It is able to cancel a 50mV DEO which is the upper bounds of the common electrodes offset.

In DEO case, the operation of the amplifier can be described as follows: DC input voltage is modulated by the chopper Mi and transposed to a higher frequency. It causes the opamp to saturate and the output is driven to V_{DD} or V_{SS}. The operational transconductance amplifier (OTA) with low-pass cutoff frequency of 0.5Hz filters the DC component of the output and converts it to voltage drop on the capacitor C_{ext}. The chopper Mh modulates it and then feedbacks to the system. At steady state, the voltage drop on C_{ext} is converged to $\left(C_i/C_{hp}\right) \cdot V_{DC,OS}$.

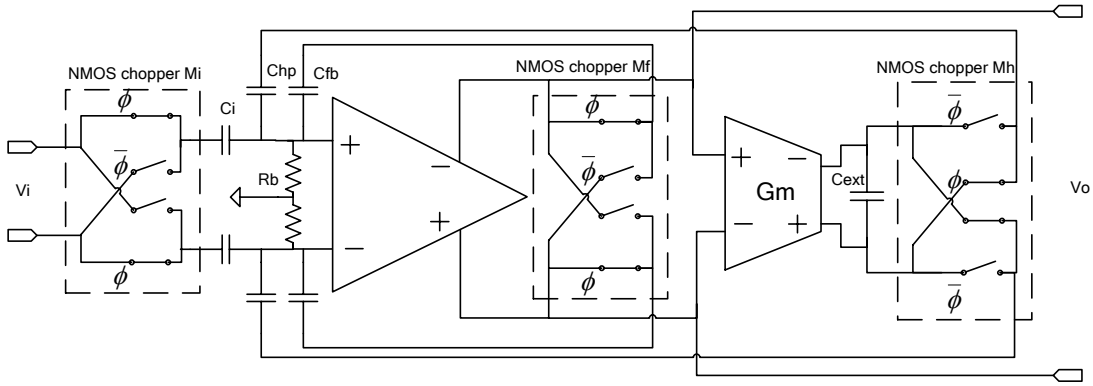


Figure 4-3 AC coupled chopper-stabilized amplifier with Gm-C filter

Opamp

Referencing Figure 4-4, the opamp is different from the conventional folded-cascode OTA. It includes two choppers and a fully-differential folded-cascode amplifier. It is also called "mixer amplifier". The architecture has three merits. First, the fully-differential configuration has better CMRR and dynamic range. It is good for bio-potential measurement. Second, the weak-inversion PMOS input pair has the best g_m/I_D ratio and less flicker noise than the NMOS. Besides, the source and body tied together improves the threshold voltage mismatch and the input common-mode range. Third, the mixer amplifier has less distortion and residual offset.

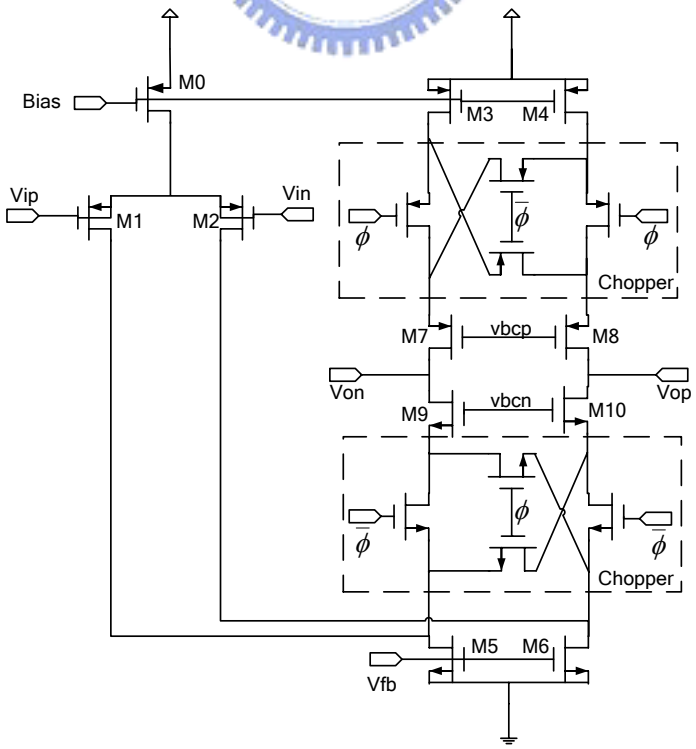


Figure 4-4 Folded-casocode mixer amplifier

Instead of the traditional chopper, the demodulation is done at the opamp output nodes. Mixer amplifier demodulates the AC signals inside the opamp. There are two advantages. First, the upper chopper can be implemented as a PMOS chopper while the lower one as a NMOS chopper. In low supply voltage circumstance, it works more efficient than traditional CMOS choppers at the output nodes. Second, the low impedance demodulation has very small settling time. It suppresses the even harmonics distortion significantly. Take the upper chopping node for example, the source of M7 is seen. The impedance is approximately $1/gm_7$. Thus, the settling time constant is derived as

$$\tau_u = \left(C_{GD4} + C_{DB4} + C_{GS7} + C_{BD7}\right)/gm_7. \tag{4.5}$$

While the output settling time constant is presented as

$$\tau_o = \left(C_{GD7} + C_{GD9} + C_L\right) \cdot g_{m7} \cdot r_o^{\,2}. \tag{4.6}$$

Where C_L is the output loading capacitance.

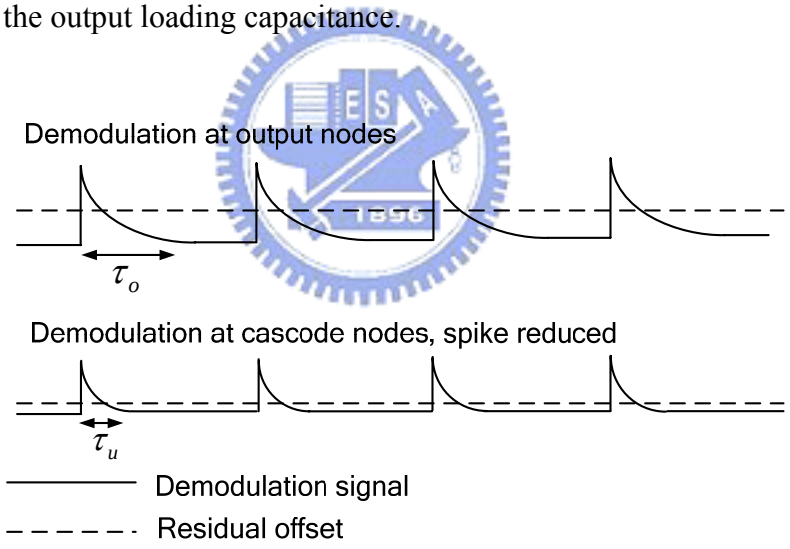


Figure 4-5 Residual offset of chopping

It is clear that the settling time constant τ_o is much larger than τ_u from the (4.5) and (4.6). Therefore, the architecture achieves very small residual offset according to the (2.11). Note that the chopper acts as a switch and the voltage drop of it is a few milli-volt. It doesn't reduce the voltage headroom. On the subject of the thermal noise, the equation can be written as

$$\overline{v_{ni}^2} = \frac{16kT}{3g_{m1}} \cdot \left(1 + g_{m3}/g_{m1} + g_{m5}/g_{m1}\right) \cdot \Delta f. \tag{4.7}$$

In bio-potential OTA, the aspect ratios of the output transistors are designed much

smaller than that of the input transistors. However, low aspect ratios of output transistors cause a high overdrive voltage for a given current. Thus, there is a trade-off between the output swing and thermal noise. In this thesis, the input pair M1 and M2 works in weak-inversion region to increase the transconductance. We choose $1+{g_{m3}}/{g_{m1}}+{g_{m5}}/{g_{m1}}=3$ for the area and noise trade-off. The equations of the open-loop gain, the unit-gain bandwidth, and the output swing and the slew rate are derived as follows:

$$\text{Open-loop gain}=g_{m1}\cdot g_{m7}\cdot r_{o7}\cdot r_{o3}. \tag{4.8}$$

$$\text{Unit-gain bandwidth}={g_{m1}}/{C_L}. \tag{4.9}$$

$$\text{Output swing}=2\cdot\left(V_{DD}-V_{od7}-V_{od3}-V_{od9}-V_{od5}\right). \tag{4.10}$$

$$\text{Slew rate}={I_{M0}}/{C_L}. \tag{4.11}$$

Figure 4-6 shows the simulated open-loop gain and phase-margin. The loading capacitance is implemented by a NMOS capacitor.

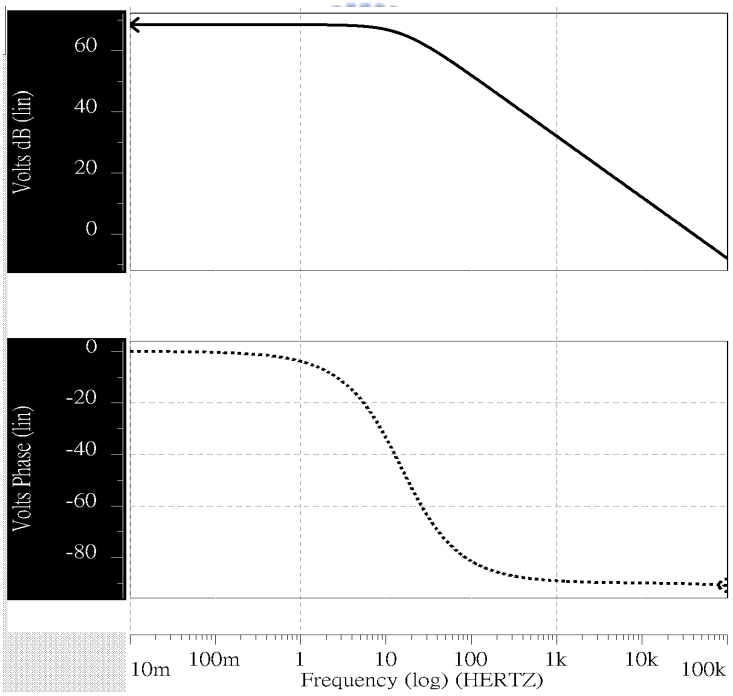


Figure 4-6 gain and phase margin simulation

Table 4-2 Opamp performance in 5 corner cases

	TT	FF	SS	SF	FS
Gain (dB)	68.4	66.9	68.8	68.3	67.4
PM(degree)	89.7	89.7	89.7	89.7	89.7

Common Mode Feedback

The fully-differential opamp needs a common-mode feedback circuit (CMFB) to bias M5 and M6 such that the common-mode output voltage is defined. There are two types of common-mode feedback. One is a continuous-time type shown in Figure 4-7, and another is a switched-capacitor type shown in Figure 4-8. The former senses the output common-mode voltage and amplifies the difference with the reference voltage V_{ref}. The feedback circuit applies the result to the NMOS current source M5 and M6. Finally, the output common-mode level is defined. For example, if the output common-mode voltage rises, so does the feedback voltage Vfb. The drain currents of M5 and M6 increase, so the output common-mode voltage falls. Thus, a feedback loop is formed. The accuracy of defining the output common-mode voltage depends on the loop gain. In other words, the larger loop gain makes the output common-mode voltage closer to the reference voltage V_{ref}. For SCMFB, it senses the output common-mode and feedbacks the difference to the system by charge transferring. In term of power consumption, the latter is preferred for no static current. However, there is a switching noise at the switching frequency. It needs a low-pass filter or higher ADC sampling rate. Figure 4-9 illustrates the phenomenon.

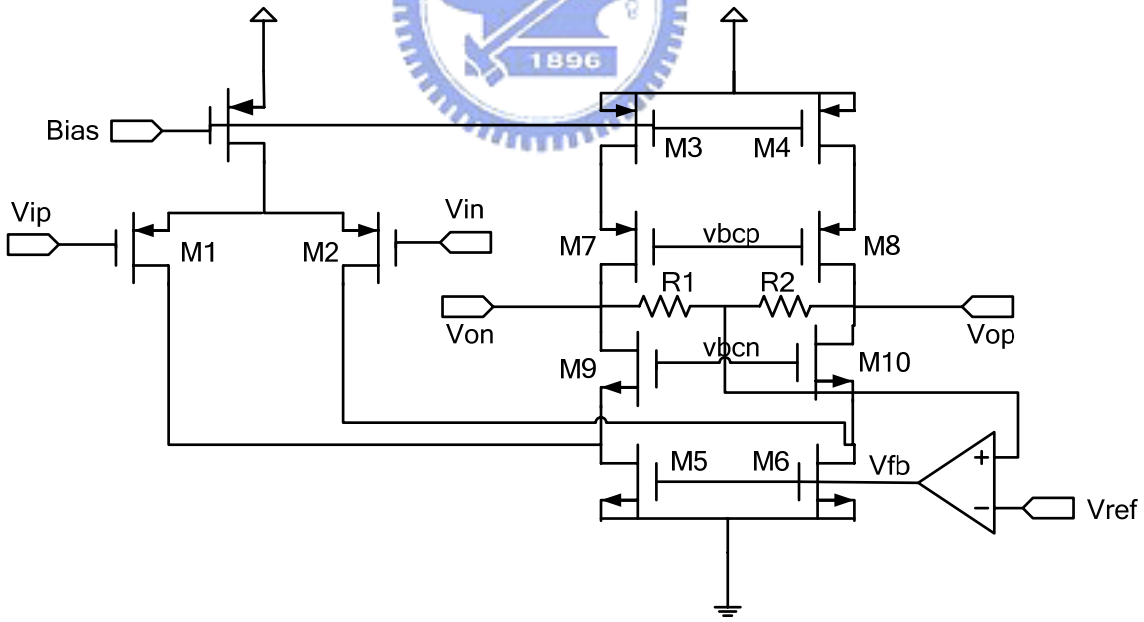


Figure 4-7 Continuous-time CMFB

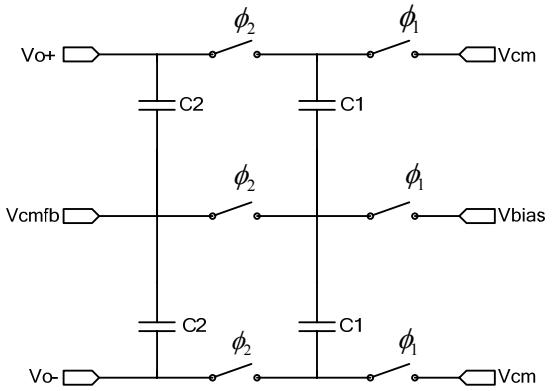


Figure 4-8 Switched-capacitor CMFB (SCMFB)

At the switching frequency (4 KHz), the SCMFB has much higher switching noise.

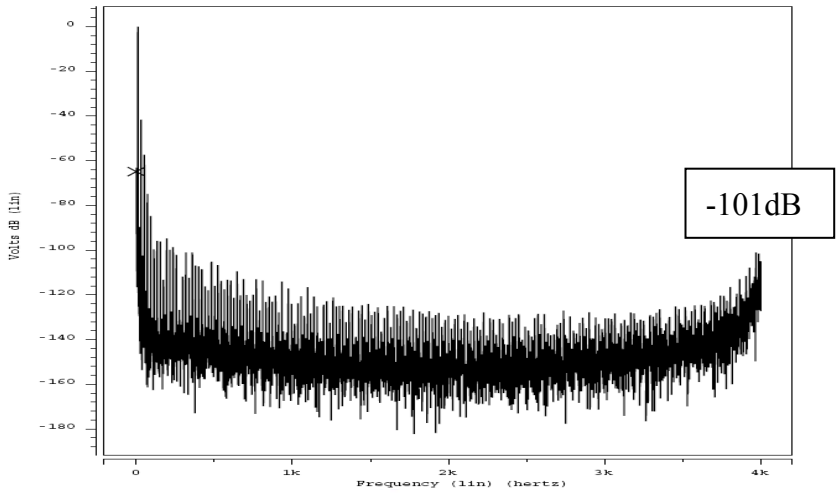


Figure 4-9 (a) Opamp with continuous-time CMFB FFT

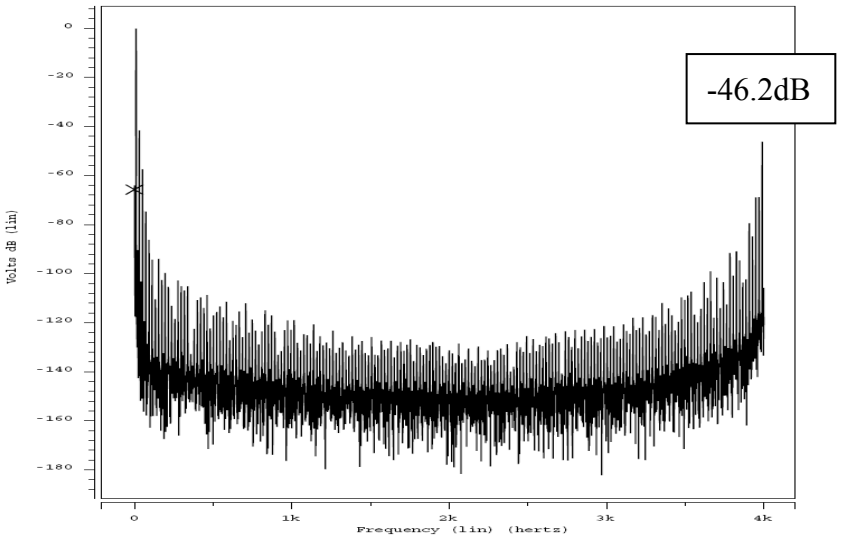


Figure 4-9 (b) Opamp with SCMFB FFT

Since the micro-power opamp output resistance is as high as hundreds of mega ohms, the resistive divider degrades the opamp voltage gain severely. Thus, a novel continuous-time CMFB is shown in Figure 4-10. The resistive divider is implemented as long channel PMOS pseudo-resistors. It has not only a light loading, but also does not affect the opamp swing. Besides, for the low speed input signal, the bias current is as low as 100nA. The input transistors M1 and M2 are operated in the weak-inversion region in order to maximize the loop gain. The CMFB gain is derived as

$$\left|A_{v,CMFB}\right| = g_{m1} / gm_{m4} . \tag{4.12}$$

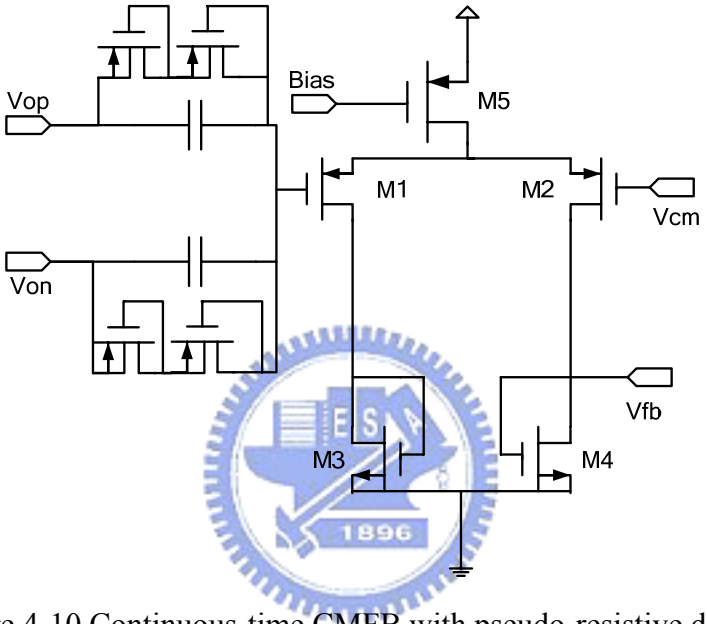


Figure 4-10 Continuous-time CMFB with pseudo-resistive divider

GM-C filter

The Gm-C filter integrated with instrumentation amplifier cancels the DEO from the electrodes DC offset. It needs an external capacitor as large as 1μF to set a very low high-pass cutoff frequency of 0.5Hz. Figure 4-11 shows the block diagram. The transconductance amplifier is implemented as a fully-differential current-mirror OTA shown in Figure 4-12. There are three advantages. First, the dominate pole is at the output node. Its time constant is very large, so the circuit is guaranteed to be stable. Second, the current-mirror architecture is less sensitive to the process variation. Third, the fully-differential OTA cancels twice more DEO than the single-end one. The cost is an additional CMFB circuit. The Gm-C filter does not use any source degeneration techniques. For DEO, Gm-C filter does its best effort to cancel it and the linearity is not an issue. Equations for the transfer function, bandwidth, and output swing are derived as follows:

$$\text{Transfer function} = g_{m1} / s \cdot C_{ext} . \tag{4.13}$$

$$\text{Unit-gain bandwidth} = g_{m1} / C_{ext} . \tag{4.14}$$

$$\text{Output swing} = 2 \cdot (V_{DD} - V_{od7} - V_{od5}). \tag{4.15}$$

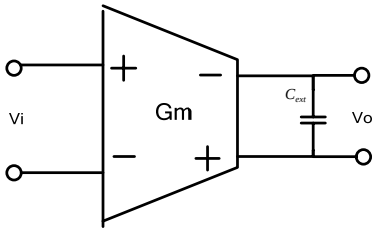


Figure 4-11 Gm-C filter

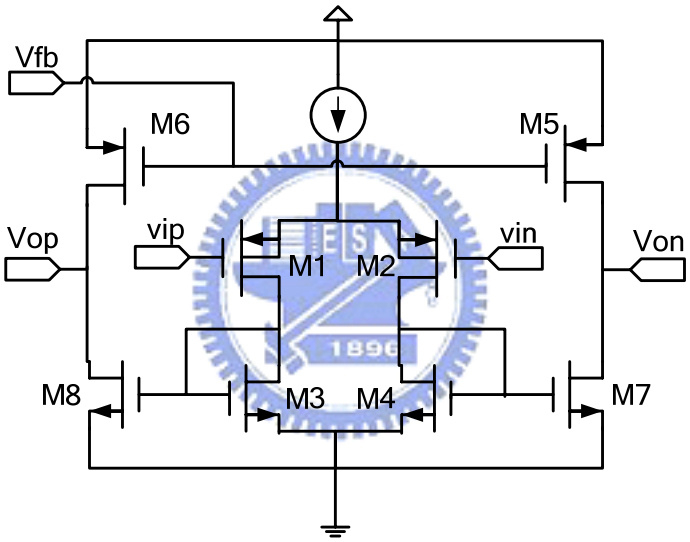


Figure 4-12 Fully-differential current-mirror OTA

Fully-differential boosted clock driver

The chopper is basically composed of two pairs of switches. They conduct in times. Therefore, one non-overlapping boosted clock driver is required. Figure 4-13 shows the proposed clock driver. It is similar to Figure 3-11. However, in order to prevent the charge leakage, it is driven by a non-overlapping clock generator.

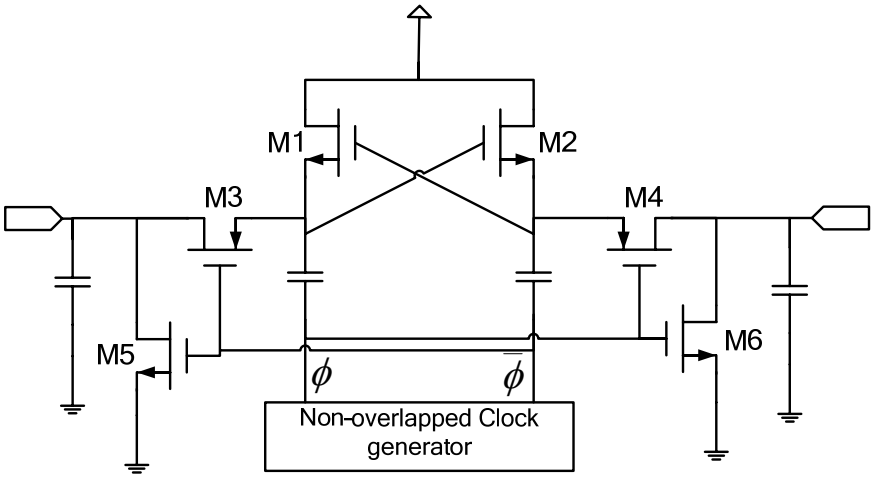


Figure 4-13 Fully-differential boosted clock driver

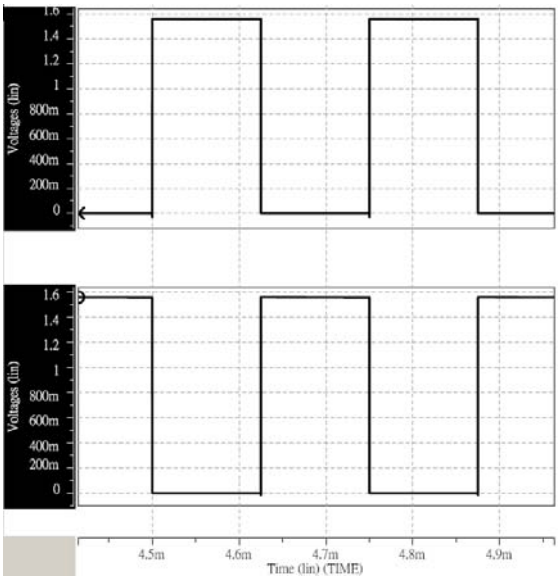


Figure 4-14 Simulated output waveforms

Non-Overlapping Clock Generator Circuit

The clock generator is implemented by NOR and Inverters. Because the clock rate is as low as 4 KHz, all the blocks are standard cells with minimal sizes. The digital circuits are surrounded by a guard-ring and an isolated power is given.

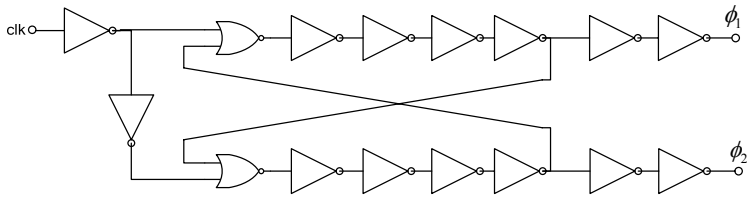


Figure 4-15 Non-overlapping clock generator

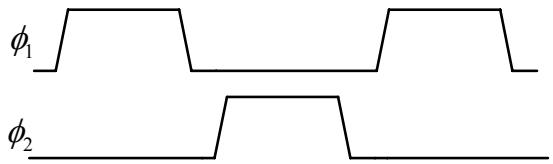


Figure 4-16 Output waveforms

4.4 Programmable Gain Amplifier

EEG has the smallest amplitude as low as 100μVpp in Table 1-1 ECG and EMG signals are much larger. To tolerate the gap, the programmable gain amplifier is presented. It consists of a single-end current-mirror OTA with capacitive feedbacks, pseudo resistors and some switches. Figure 4-17 shows the proposed architecture. The positive terminal feedback paths establish a high-pass filter with a very low cutoff frequency. It blocks the DC offset from the instrumentation amplifier. The midband gain is set to C_{in}/C_f. The input capacitors are selected by digital controls that define the closed-loop gain. The transfer function is written as

$$A(s) = -\frac{Cin}{Cf} \cdot \frac{1}{1 + s \cdot \frac{Cin}{Cf} \cdot \frac{C_L}{G_m}} \quad (4.16)$$

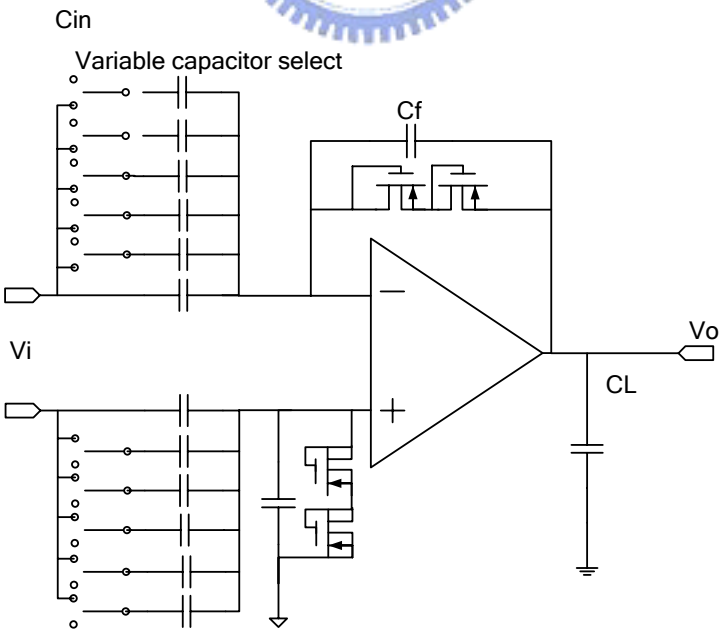


Figure 4-17 Digitally controlled amplifier

Figure 4-18 is the OTA used in PGA. Since the instrumentation amplifier

provides a 40 dB voltage gain, the noise requirement is much relaxed in the PGA. Although it does not require chopping in PGA, the input pair is implemented as PMOS in order to reduce flicker noise. The thermal noise of the OTA is derived as

$$\overline{v_{ni}^2} = \frac{16kT}{3g_{m1}} \cdot \left(1 + g_{m3}/g_{m1} + g_{m5}/g_{m1} + g_{m7}/g_{m1}\right) \cdot \Delta f. \tag{4.17}$$

Furthermore, the PMOS of the input pair have their bodies and sources tied together to obtain a better matching and a better input common-mode range.

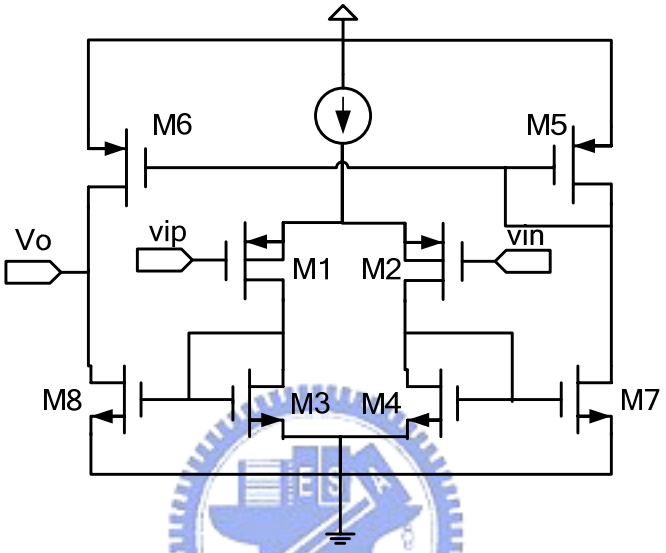


Figure 4-18 Single-end current-mirror OTA

4.5 Simulation Results and Layout

Given an ECG signal with a common-mode disturbance, the simulated results are shown in Figure 4-19. The horizontal-axis is the transient time and the vertical-axis is the voltage to ground. The upper waveform is the ADC output and the lower one is the single electrode input. The clear QRS-complex is obtained without 60Hz noise.

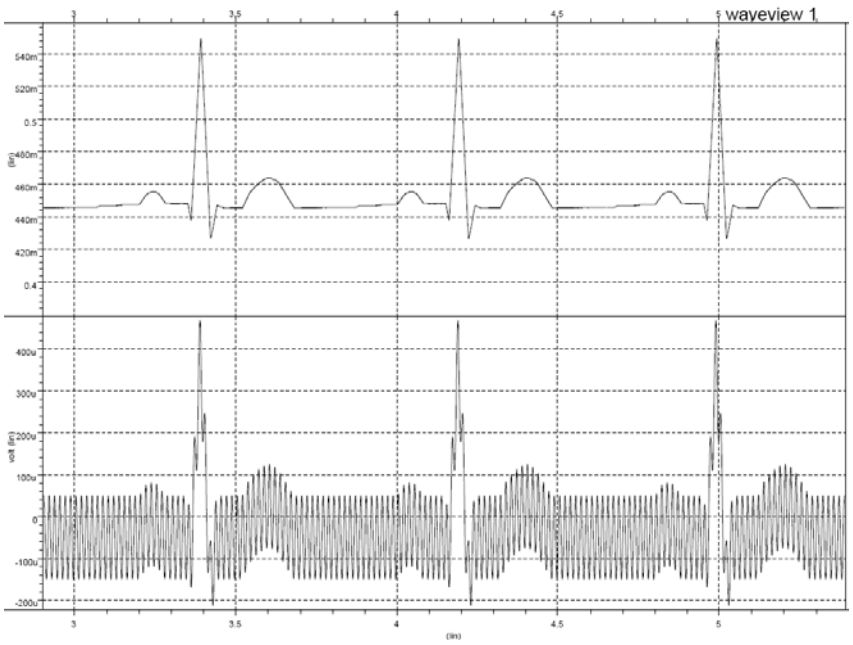


Figure 4-19 ECG signal simulation

Given a 1mVpp differential sine wave at 12.04Hz, the FFT simulation results of ADC are shown in Figure 4-20. The horizontal-axis is the frequency in log scale and the vertical-axis represents the power density. The SFDR is obtained as 54dB and the SNR is 54.13dB within DC to 100Hz.

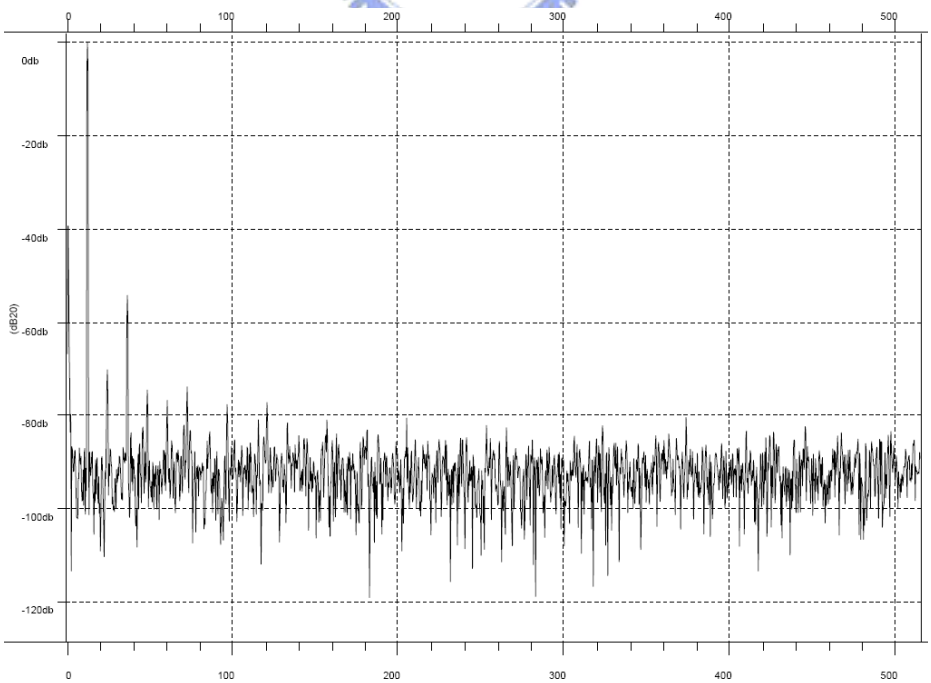


Figure 4-20 Proposed AFE IC FFT simulation

Given an ECG signal with a 60Hz common-mode disturbance, the PGA output waveform is shown in Figure 4-21. Figure 4-22 and 4-23 shows the simulation results at V_{DD}=0.6V and 0.4V. At V_{DD}=0.6V, all transistors operate in sub-threshold region. At V_{DD}=0.4V, all transistors work in deep sub-threshold region. Although the limited voltage headroom suppresses the dynamic range and causes nonlinearity, the QRS-complex is still able to be detected.

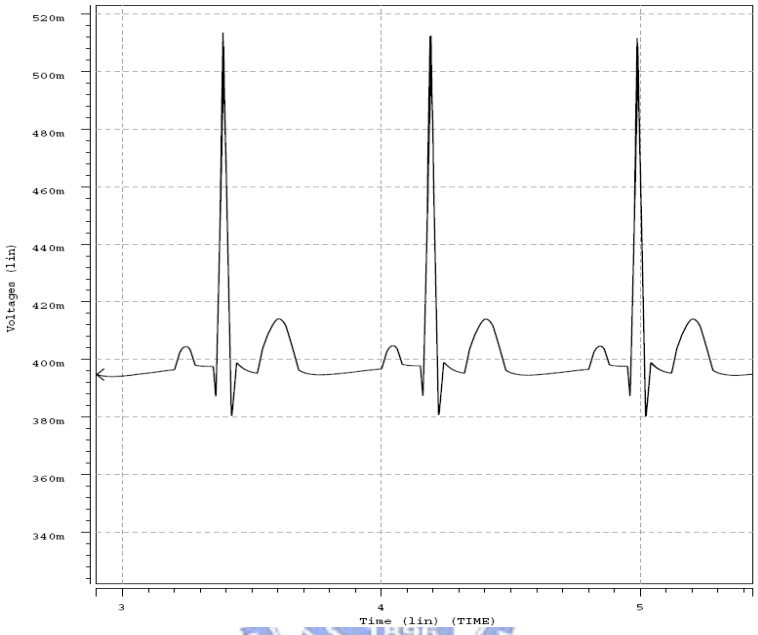


Figure 4-21 ECG signal simulation @V_{DD}=0.8V

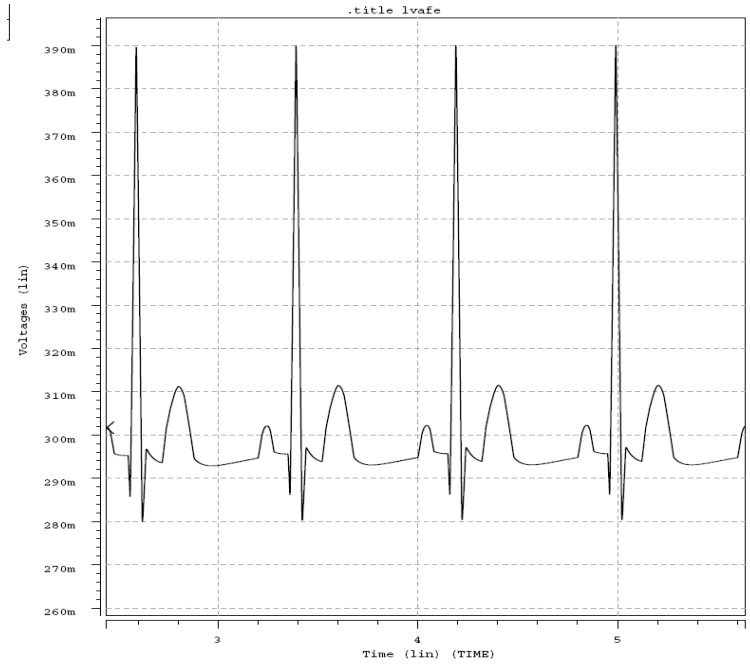


Figure 4-22 ECG signal simulation @V_{DD}=0.6V

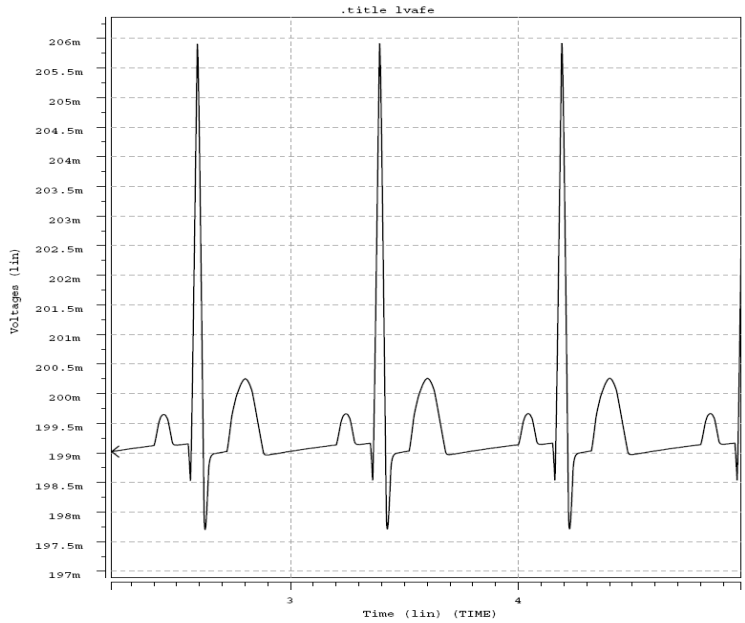


Figure 4-23 ECG signal simulation @V_{DD}=0.4V

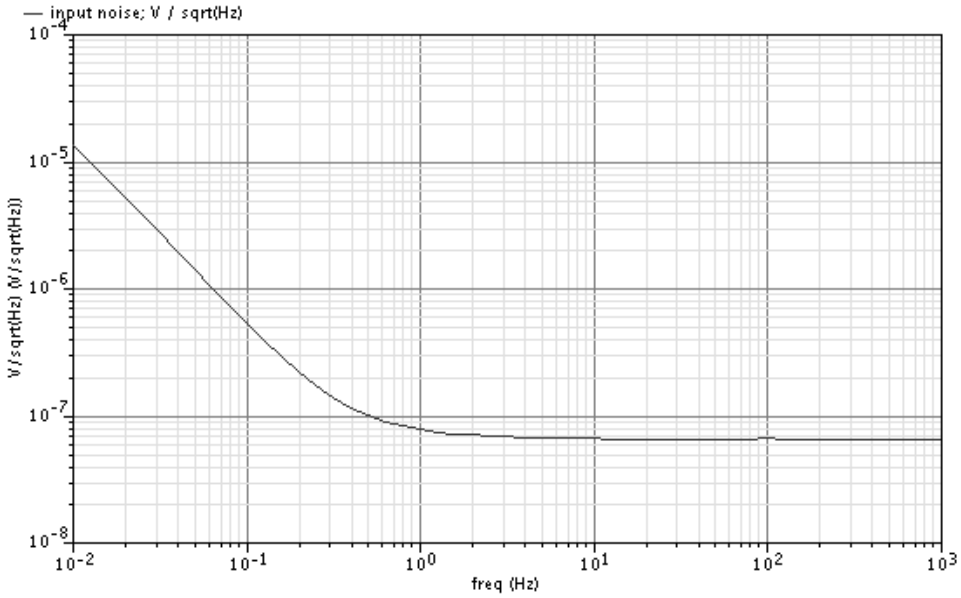


Figure 4-24 Front-end amplifier noise simulation

Table 4-3 Input-referred voltage noise density in 5 corner cases

Corner	TT	FF	SS	FS	SF
Noise Floor($nV/\sqrt{Hz}$)	59.7	59.2	64	61.6	61.4

Table 4-4 Input-referred noise for different applications

Application	Integrated bandwidth(Hz)	IRN(μVrms)
EEG	0.5-100	0.58
ECG	0.5-100	0.58
EMG	10-400	1.12

Figure 4-24 shows the simulated input-referred voltage noise density of the analog front-end. Because the chopping technique modulates the flicker noise and transposes to the chopping frequency at 4 KHz, there is only thermal noise within a signal bandwidth. The noise floor is about 60 $nV/\sqrt{Hz}$. Table 4-3 is the noise floor in five corner cases and Table 4-4 shows the input-referred noise for common applications. Considering the THD of the front-end amplifier, the simulation results are shown in Figure 4-25. Due to limited voltage headroom in a low supply voltage system, the distortion is severe as the front-end amplifier output amplitude goes high. In general, the dynamic range is defined as the largest input signal power magnitude over the input-referred noise power within the signal bandwidth under the condition that THD<1%. In the minimal gain case (100V/V), the largest input signal amplitude is 5.2mVpp such that THD=1%. Therefore, the front-end achieves a 70dB dynamic range.

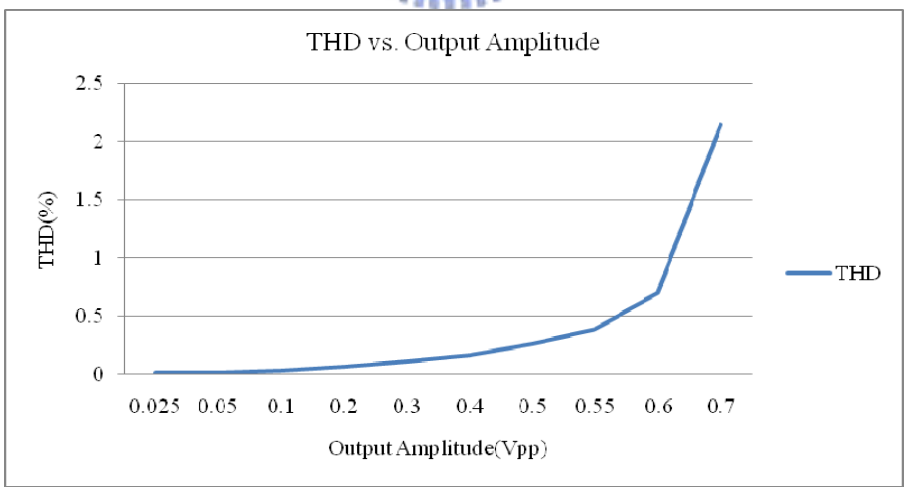


Figure 4-25 THD versus output swing simulation result (Gain=200V/V)

The overall transfer function versus bio-potential signals is shown in Figure 4-26. The AC coupled chopper-stabilized instrumentation amplifier offers 40dB voltage gain and the PGA provides the variable gain from 1V/V to 32V/V. The horizontal-axis is the frequency in log scale and the vertical-axis represents the magnitude in dB scale.

For EEG, it has the smallest signal amplitude, so the system gives a 70dB voltage gain. In ECG case, 40dB voltage gain is adequate. Table 4-5 shows the gain and bandwidth summary.

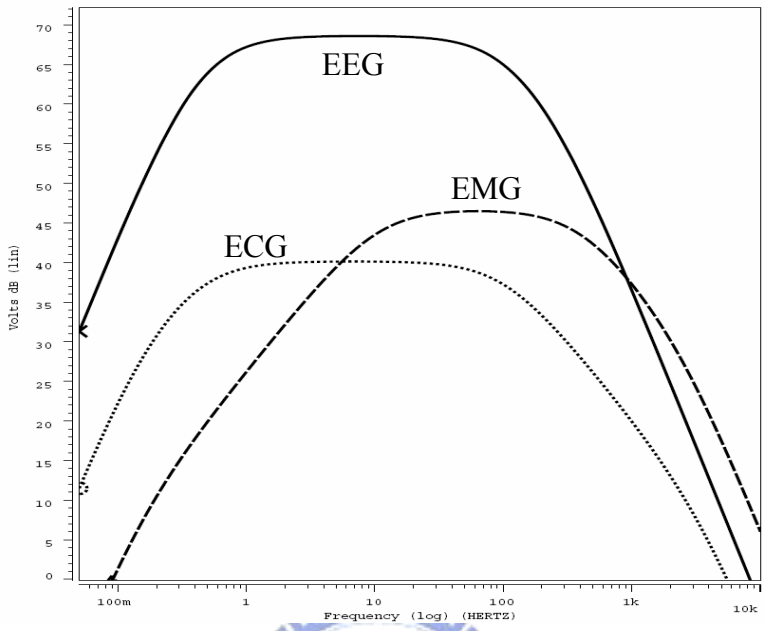


Figure 4-26 Output versus input transfer function for common biomedical signals

Table 4-5 Gain and bandwidth for common applications

Application	Gain	Bandwidth
EEG	70dB	0.5-100Hz
ECG	40dB	0.5-100Hz
EMG	46dB	10-400Hz

CMRR is the one of the most important issue in bio-potential acquisition IC. In order to satisfy IFCN standard, the fully-differential instrumentation amplifier achieves over 110dB CMRR is desired. Figure 4-27 is the CMRR simulation result. The horizontal-axis is the frequency in log scale and the vertical-axis is the magnitude in dB scale. Note that the simulation result is the differential gain over the single-end common-mode gain.

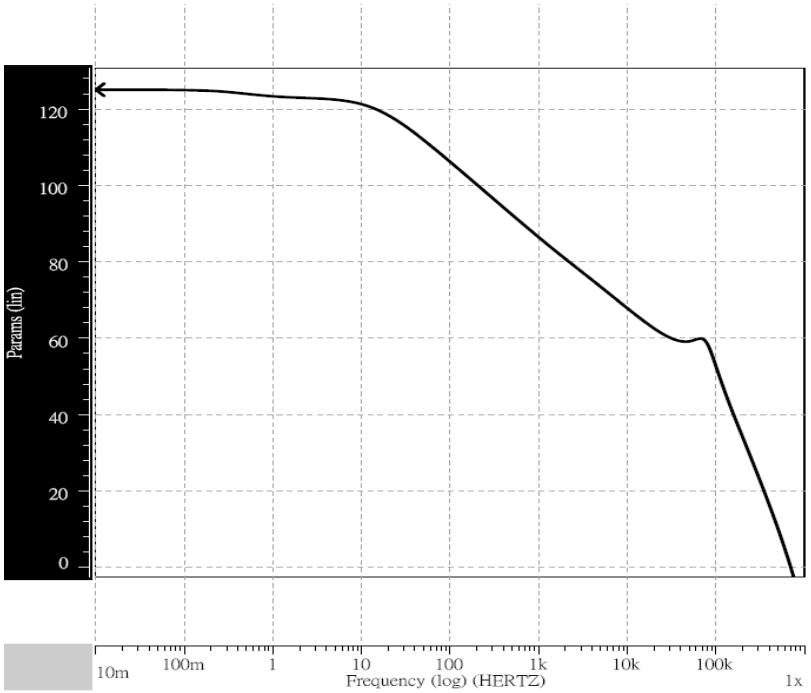


Figure 4-27 CMRR simulation. CMRR=110dB@60Hz

The proposed architecture is fabricated in TSMC 0.18μm CMOS technology. The chip micrograph is shown in Figure 4-28. It includes an instrumentation amplifier with a GM-C filter, a PGA, a SAR ADC, output buffers and MOS capacitors. The analog part and digital part are blocked by guard rings. The full chip area is 1.38x0.62 mm^2 and the core area is 1.12 x 0.36 mm^2. The performance summary is shown in Table 4-6.

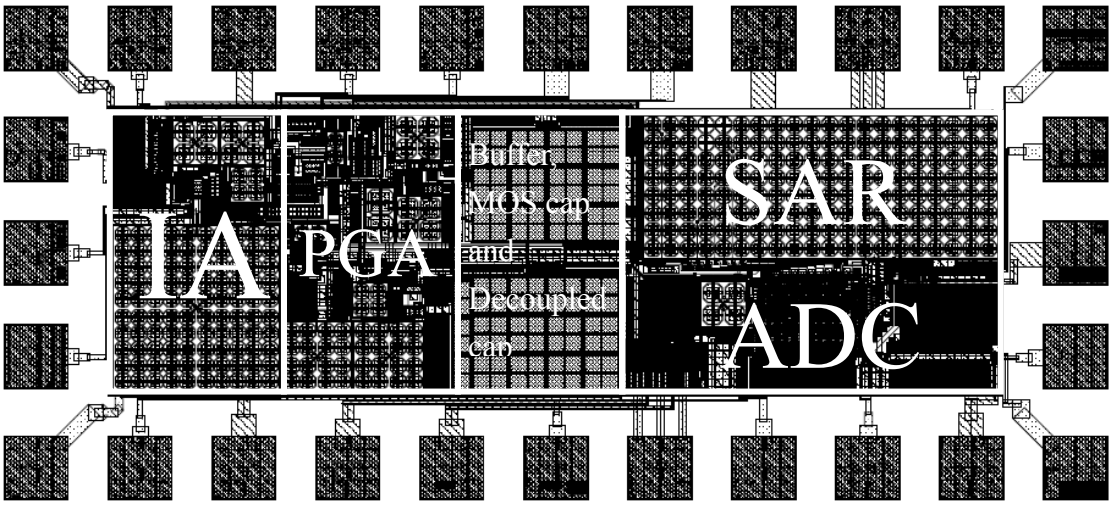


Figure 4-28 Layout of the proposed AFE IC

Table 4-6 The proposed AFE IC performance summary

Spec.	Performance Value	Unit
Supply Voltage	0.8	V
Supply Current	4.85	μA
NEF*	3.56	
Gain	40-70	dB
Input-referred Noise RMS	59.7	$nV/\sqrt{Hz}$
THD	<0.714	%
CMRR(50/60Hz)	>110	dB
High Pass -3dB Frequency	0.5, 10	Hz
Low Pass -3dB Frequency	100-400	Hz
AFE IC SFDR	54.2	dB
AFE IC SNR	54.1	dB
ADC sample rate	2.67	KS/s
ADC SNR	63.6	dB
ADC SNDR	63	dB
ADC ENOB	10.18	bit
ADC DNL	<± 0.96LSB	LSB
ADC INL	<± 1LSB	LSB
Chip core area	1380x618.585 1119.14x357.725	μm^2
Technology	0.18	μm

*NEF- Noise Efficient Factor.

$$NEF = V_{ni,rms} \cdot \sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot V_T \cdot 4kT \cdot BW}}$$

4.6 Measurement Consideration

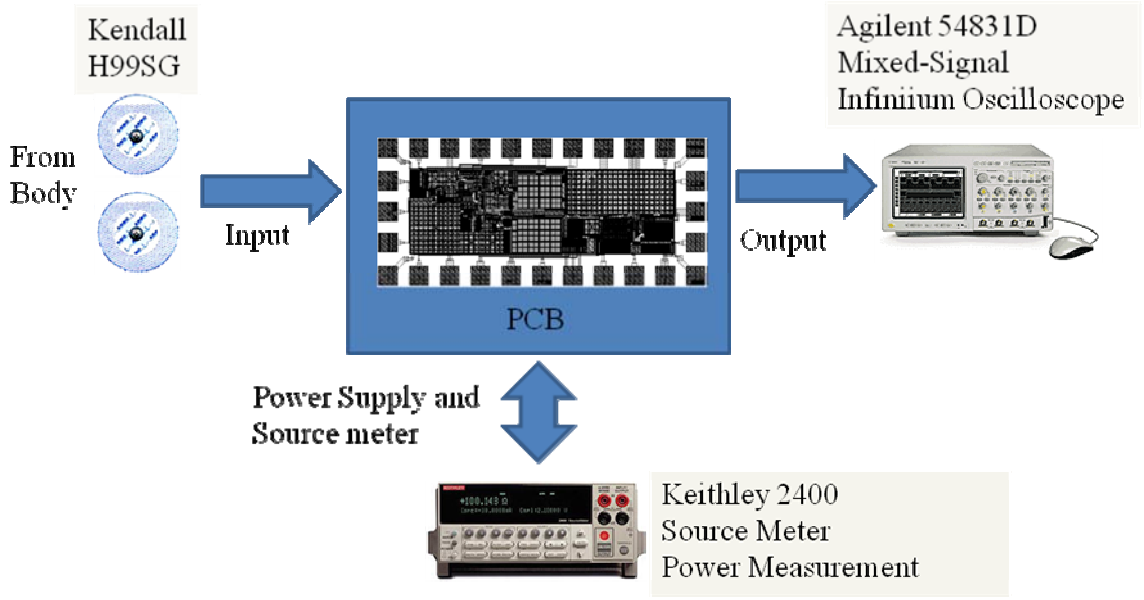


Figure 4-29 Measurement environments

The measurement environment is shown in Figure 4-29. The chip is located on the PCB board and the input/output pins are bounded by metal wires. The input signal is from the human body via Kendall H99SG skin electrodes. The power and reference voltage is supplied by Keithley 2400 general-purpose source meter with measurement. The output is analyzed by Aglient 54831D Mixed-Signal Infiniium Oscillioscope

4.7 Measurement Results

Before the experiment, it is essential to setup the measurement environment. Figure 4-30 shows the PCB photo. To measure the ECG signal, use two electrodes as differential inputs. The positive input terminal is connected to the venticulus sinister and the negative input terminal is connected to atrium dextrum. Two hands or right leg connected to the ground improve the 60Hz common-mode noise.

At the nominal bias current 500nA, the total supply current excluding ADC is 3.9μA. When the bias current is tuned as low as 276nA, the total supply current excluding ADC is 2.3μA. Figure 4-31 shows the measurement status.

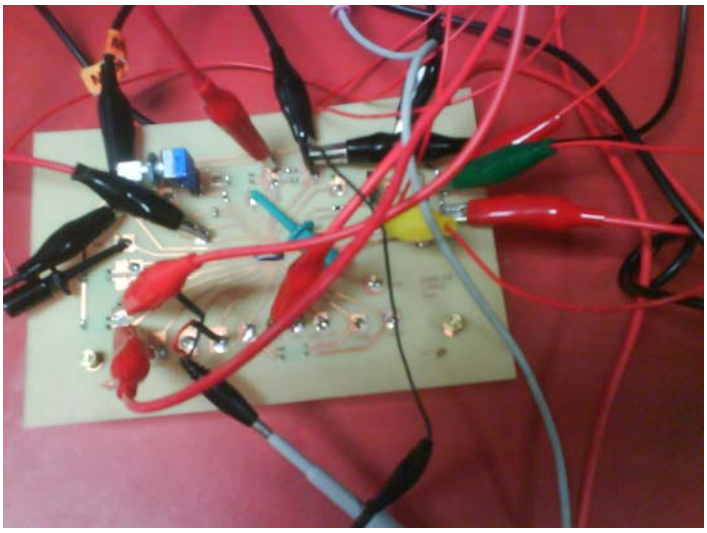


Figure 4-30 Setup the measurement environment

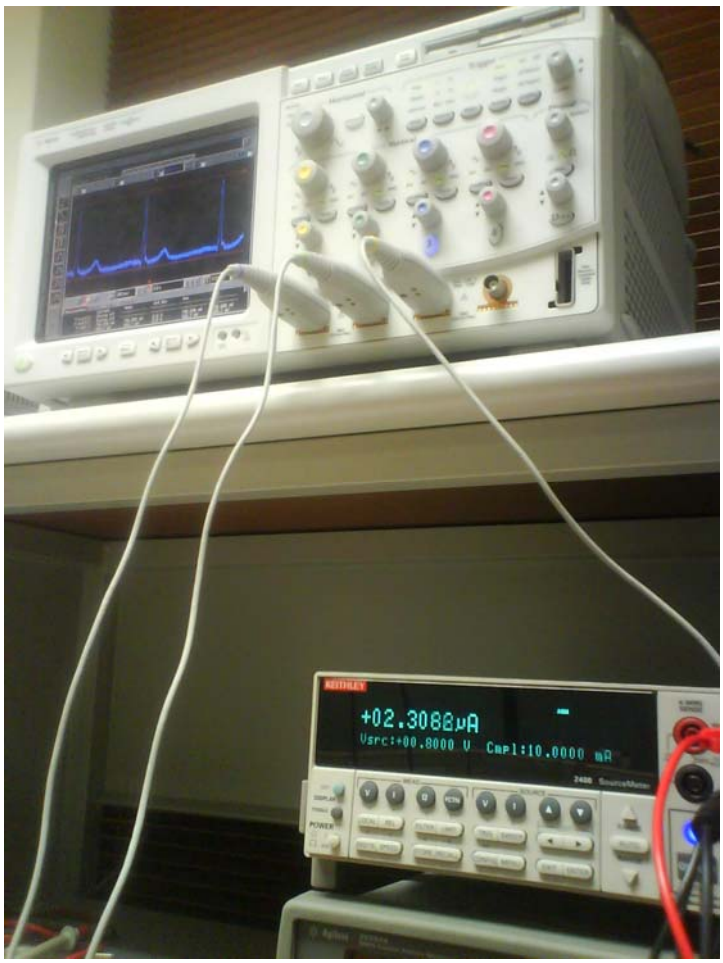


Figure 4-31 Measurement photo

The ECG output waveform measured at the PGA output is shown in Figure 4-32. The ECG output signal has high frequency modulated noise. After a second order low-pass filter with cutoff frequency 100Hz by Matlab, it is clear to see QRS-complex,

P wave and T wave shown in Figure 4-33. Here we set the voltage gain to 100V/V. The measured voltage gain is 107V/V. It has output amplitude of 268mVpp. Figure 4-34 shows the ECG output waveform at gain=200V/V. The measured voltage gain is 198V/V and the output amplitude is 495mVpp.

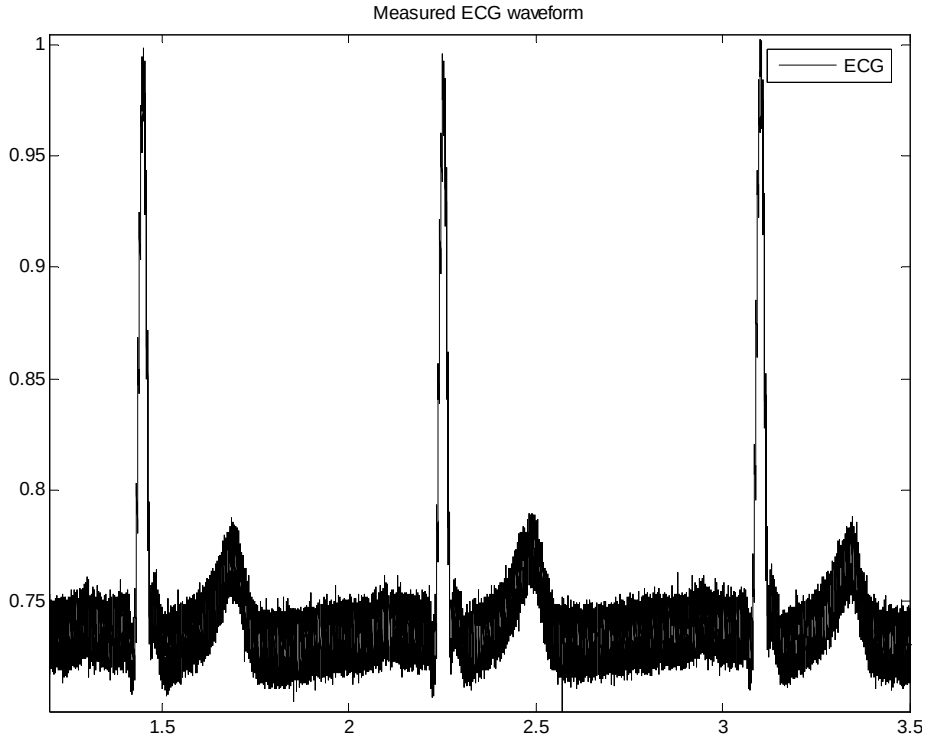


Figure 4-32 ECG measurement results (without DSP, Gain=100V/V)

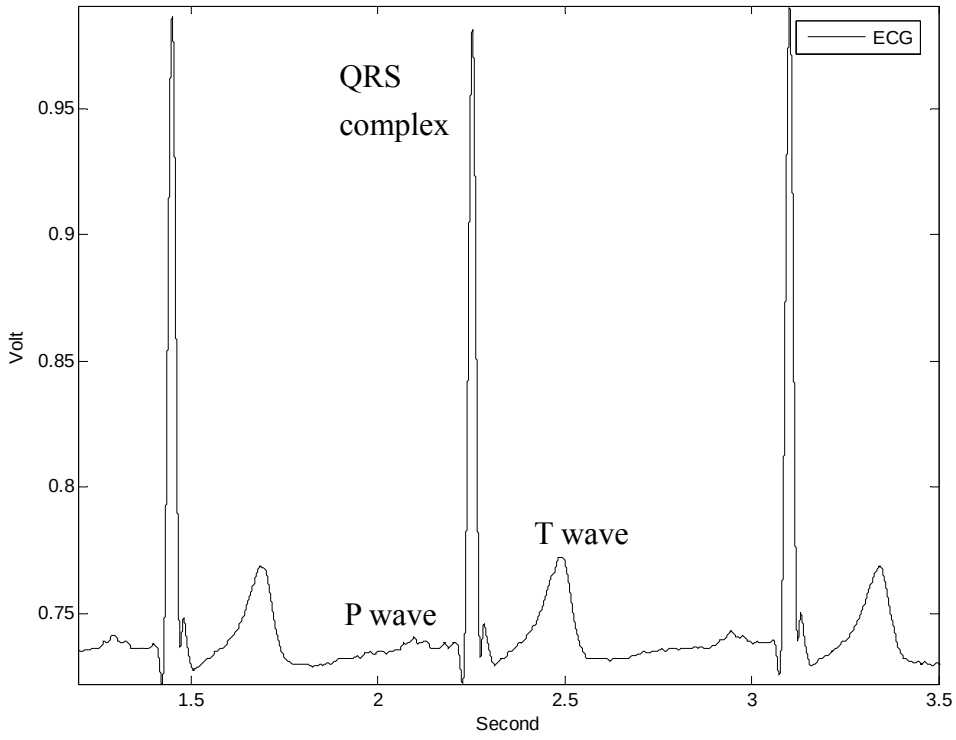


Figure 4-33 ECG measurement results (Gain=100V/V)

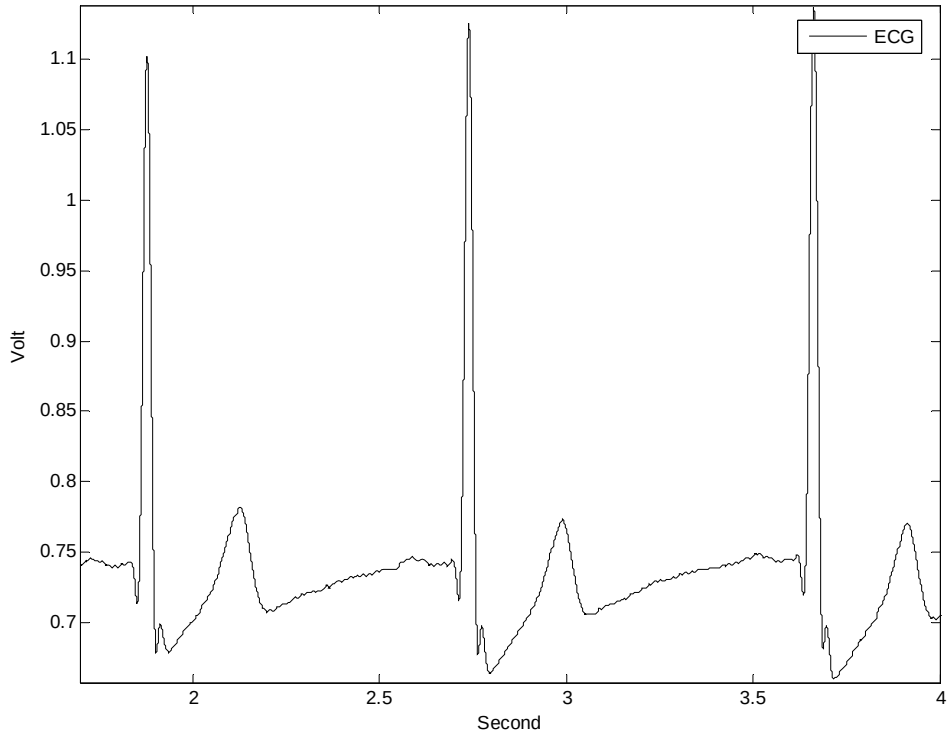


Figure 4-34 ECG measurement results (Gain=200V/V)

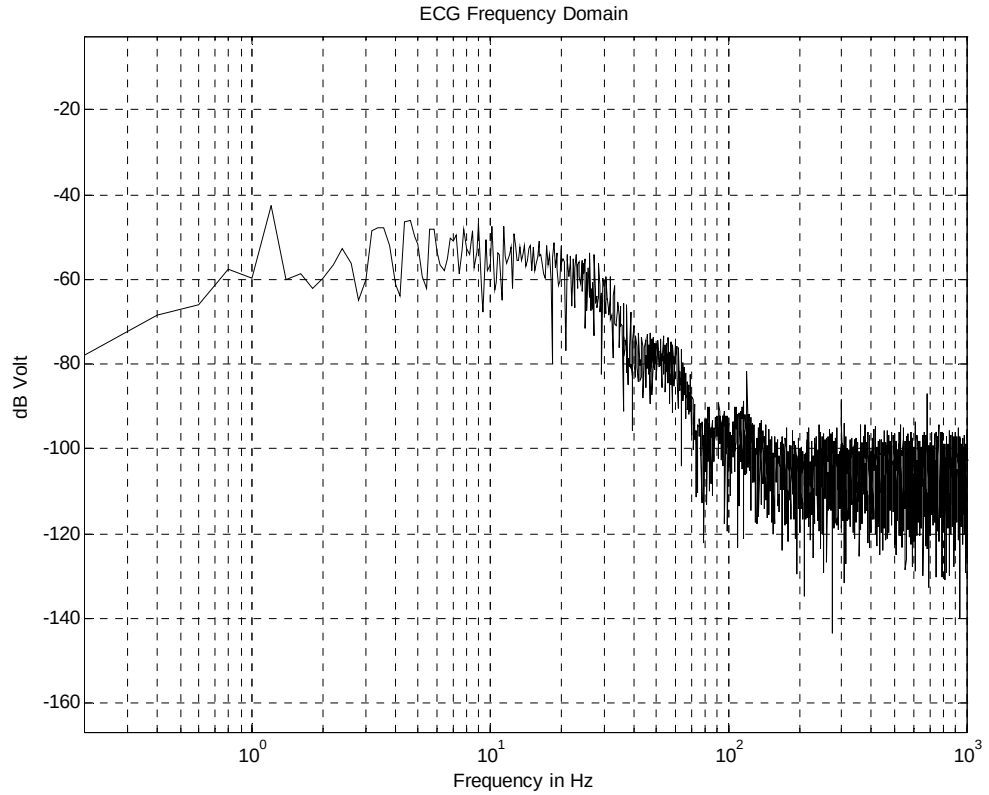


Figure 4-35 Measured ECG FFT spectrums

Figure 4-35 shows the FFT of the measured ECG signal. The ECG signal component is mostly around 10Hz.

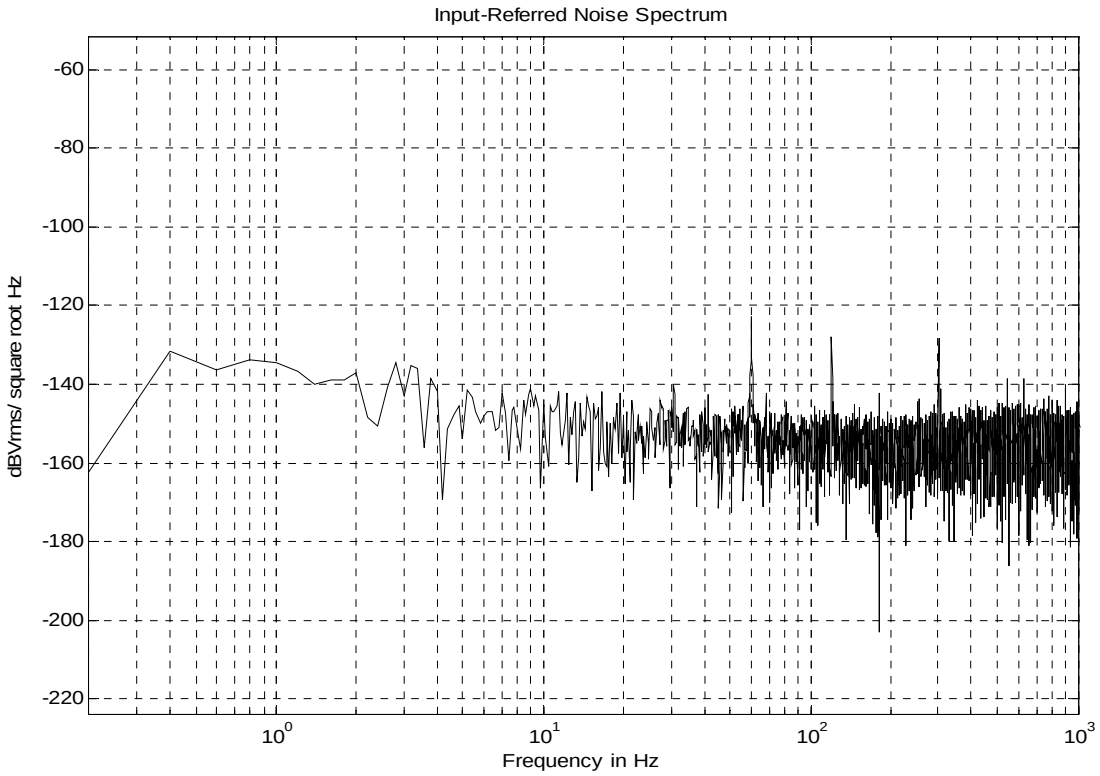


Figure 4-36 Input-referred noise spectrum density

To measure the input-referred noise, two input terminals are shorted to ground and measure the output noise. The output noise divided by the voltage gain equals the input-referred noise. Figure 4-36 shows the measurement result. The noise floor is about 57 $^{nV}/_{\sqrt{Hz}}$ and the input-referred noise voltage integrated from 0.5Hz to 100Hz is 0.88μV.

To verify the characteristic of the transistors in sub-threshold region, the supply voltage scales down and the voltage gain is set to 200V/V. Figure 4-37 shows the measured ECG output waveform at V_{DD}=0.7V. The output amplitude is 0.34Vpp and the voltage gain is 139V/V. Figure 4-38 shows the measured result at V_{DD}=0.6V. The output amplitude is decayed to 123.6mVpp and the voltage gain is 49.4V/V. Figure 4-39 shows the measured result at V_{DD}=0.5V. Here the gain is set to 100V/V. It has output amplitude of 11.8mV and the voltage gain of 4.72V/V. At V_{DD}=0.4V, the measured waveform is shown in Figure 4-40. The gain is set to 200V/V. The output amplitude is 25mVpp and the voltage gain is 10V/V.

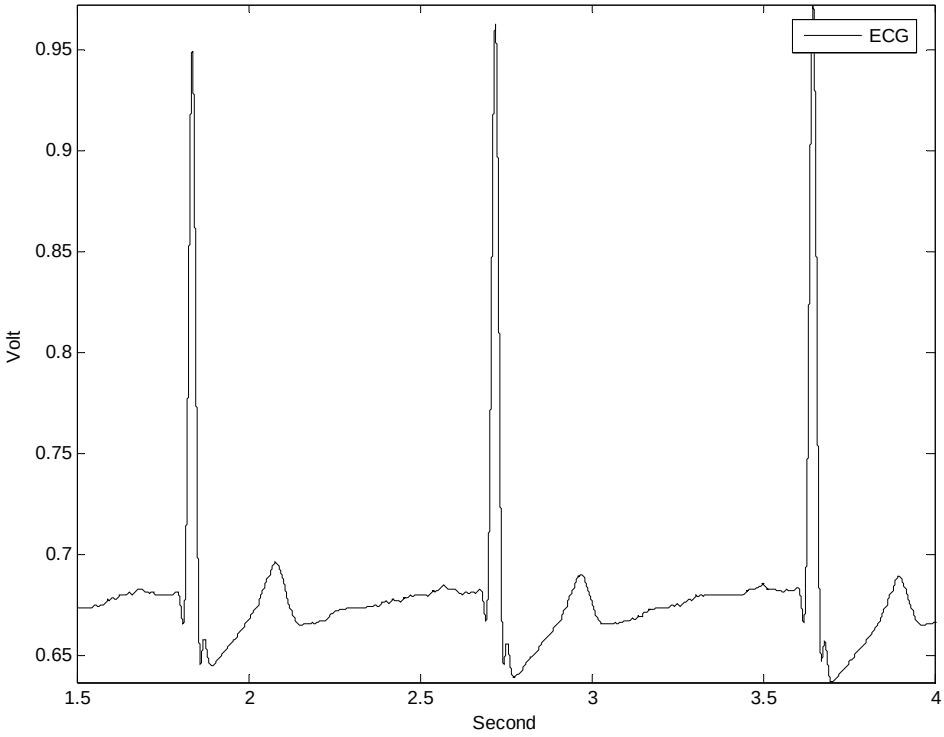


Figure 4-37 ECG measurement results at V_{DD}=0.7V

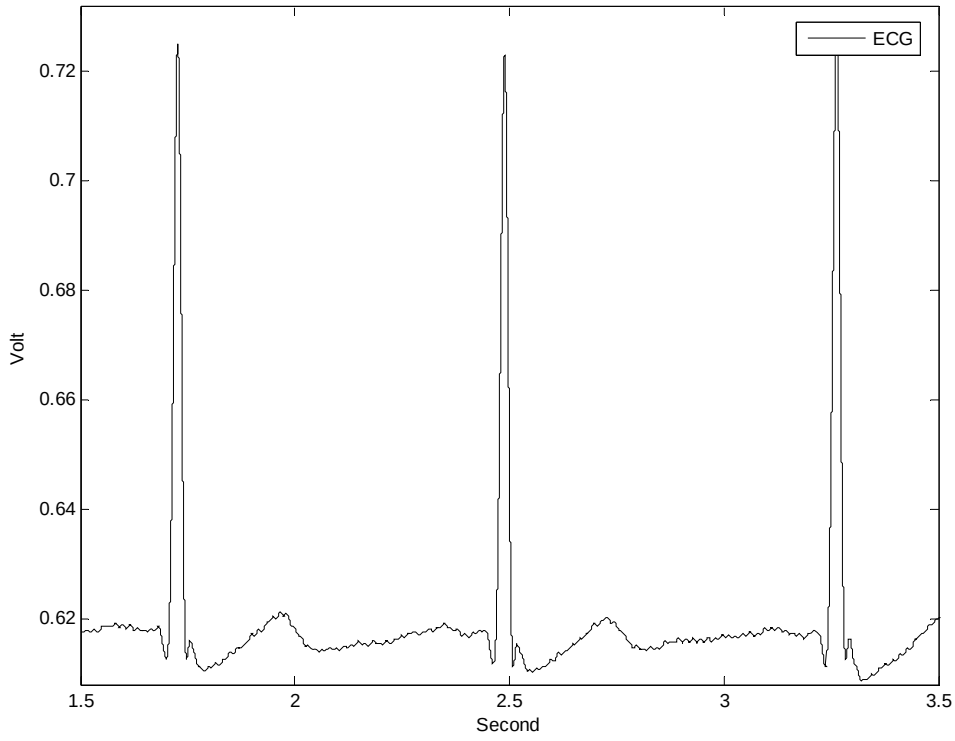


Figure 4-38 ECG measurement results at V_{DD}=0.6V

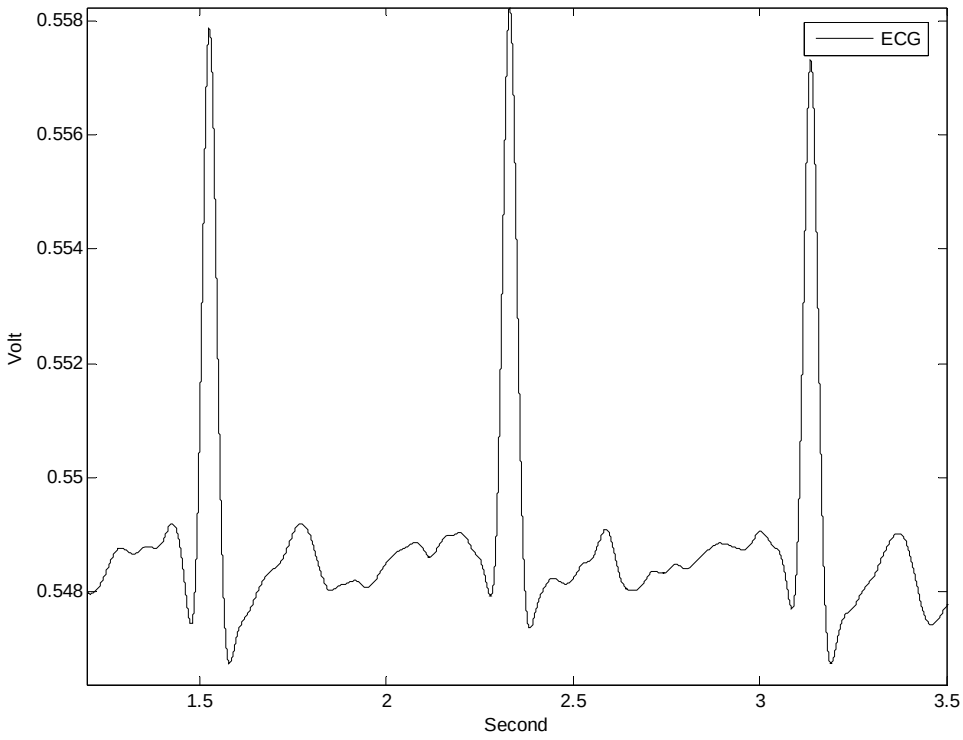


Figure 4-39 ECG measurement results at V_{DD}=0.5V

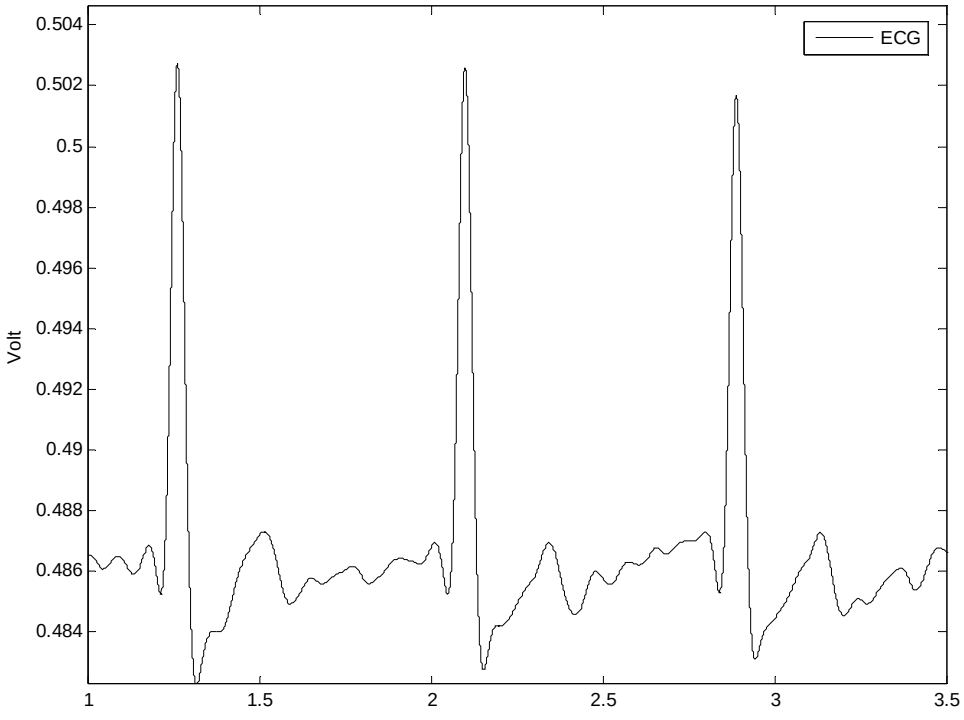


Figure 4-40 ECG measurement results at V_{DD}=0.4V

The table 4-7 shows the measurement results at the supply voltages from 0.4 to 0.8V. At V_{DD}=0.8V, it has an input-referred noise voltage of 0.88μV and power consumption of 1.84μW. It has the best NEF. At V_{DD}=0.4V, the circuit works and is still able to obtain QRS-complex with merely 119nW power dissipation. Because the bootstrapped NMOS choppers are sub-threshold turn-on, the choppers have insufficient low turn-on resistance, the noise increases.

Table 4-7 Measurement summaries

supply voltage	0.8V	0.7V	0.6V	0.5V	0.4V
supply current (by keithley 2400)	2.3μA	1.83μA	1.27μA	750nA	298nA
supply current (bias excluded)	1.86μA	1.48μA	1μA	598nA	226nA
noise floor@10Hz	57nV/sqHz	74.8nV/sqHz	129nV/sqHz	503nV/sqHz	1.76μV/sqHz
input referred noise (0.5-100HZ)	0.88μVrms	1.05μVrms	5.414μVrms	10.99μVrms	72.1μVrms
NEF (bias excluded)	4.7	5	21.2	33.4	134
External bias current	276nA	220nA	150nA	95nA	45nA
power	1960nW	1281nW	762nW	375nW	119nW

4.8 Comparison

The analog front-end amplifier performance comparisons are shown in Table 4-8. The chip is able to operate in the range of supply voltage from 0.4V to 0.8V. The total current of the amplifiers is 1.86μA. The work achieves an input-referred noise voltage of 0.88μV within 100Hz and a NEF of 4.7. In other words, it has the best power and noise trade-off. The gain and bandwidth are programmable via digital interface. It is realized in TSMC 0.18 μm with the core area of 0.4 mm^2

Table 4-8 Bio-potential front-end amplifier comparison

Amplifier	**This work simulation**	**This work Measured results**	Timothy Denison, ISSCC 07	R.F. Yazicioglu, ISSCC 06	K.A. Ng, JSSC 05	R. R. Harrison, JSSC 03
Supply Current	**4.5μA**	**1.86μA**	1.2μA	11.1μA	485μA	180nA
Supply Voltage	**0.4-0.8V**	**0.4-0.8V**	1.8V	3V	+/-1.5V	+/-2.5V
Power	**3.9μW**	**119nW-1.84μW**	2.16μW	33.3μW	1.455mW	0.9μW
NEF	**3.56**	**4.7**	4.9	7.8	59	4.8
Gain	**40-70dB**	**40-70dB**	45.5dB	>60dB	80dB	40dB
Input-referred Noise RMS	**0.58μV (100Hz)**	**0.88μV (100Hz)**	0.93μV (100Hz)	0.65μV (100Hz)	0.73μV (100Hz)	1.6μV (30Hz)
Dynamic Range	**70dB**	**58dB**	60dB	68dB	71dB	69dB
High Pass -3dB Frequency	**0.5Hz, 10Hz**	**0.5Hz, 10Hz**	0.5Hz	0.5Hz, 10Hz	0.3Hz	0.014Hz
Low Pass -3dB Frequency	**100-400Hz**	**100-400Hz**	250Hz	>150Hz	150HZ	30Hz
Core Area	**0.4** mm^2	**0.4** mm^2	NA	2 mm^2	4.81 mm^2	0.16 mm^2
Technology	**0.18μm**	**0.18μm**	0.8μm	0.5μm	0.5μm	1.5μm

Table 4-9 shows the ADC performance comparison. To compare the power efficiency, Figure-of-merit (FOM) is defined as

$$FOM = \frac{P}{2^{ENOB} \cdot f_s}. \tag{4.18}$$

where P is the power consumption, f_s represents the sampling rate, ENOB is effective number of a bit. This work has an ENOB of 10.3-b at Nyquist rate with a power consumption of 0.31μW excluding biasing circuits.

Table 4-9 ADC performance comparison

ADC	**This work**	Scott, JSSC03	Sauerbrey, JSSC03	Naveen Verma, JSSC07	Hao-Chiao Hong, JSSC07	Michiel van Elzakkerl, ISSCC08
# bits	**11**	8	9	12	8	10
V_{DD}(V)	**0.8**	1.4	0.8	1	0.83	1
Pd(μW)	**0.31**	4.2	11.4	25	1.16	1.9
ENOB @Nyquist rate	**10.3**	7	7.96	10.55	7.42	8
Fs(KS/s)	**2.67**	100	88	100	111	1000
FOM (fJ/Conv.)	**90**	330	520	165	60	4.4
Input swing/VDD	**0.75**	1	0.5	1	1	1
Technology	**0.18μm**	0.25μm	0.18μm	0.18μm	0.18μm	65nm

4.9 Summary

The proposed 0.8V analog front-end IC is presented in this chapter. The chip includes an instrumentation amplifier, a PGA and a SAR ADC. The instrumentation amplifier not only avoids flicker noise, but also handles DEO issue. PGA provides the reconfigure characteristic and interface with DSP. SAR ADC converts the analog signal to digital codes. The front-end amplifiers can operate at the supply voltage from 0.4V to 0.8V. At nominal supply voltage 0.8V, it has the best NEF of 4.7 with power consumption of 1.84μW. At ultralow voltage 0.4V, it is able to obtain QRS-complex with power consumption of 119nW. The chip is realized in TSMC 0.18μm.

Chapter 5

A 1.5-V Low-Power Bio-Potential Signal Acquisition Front-End IC

5.1 Architecture

Before the proposed analog front-end with SAR ADC is designed, we have implemented an analog front-end to explore the low power design technique. The proposed 1.5-V biomedical front-end IC is presented and shown in Figure 5-1. It includes an instrumentation amplifier, an Amp amplifier, and a PGA. All of the amplifiers are fully differential. There are switches to control the gain and bandwidth of the front-end.

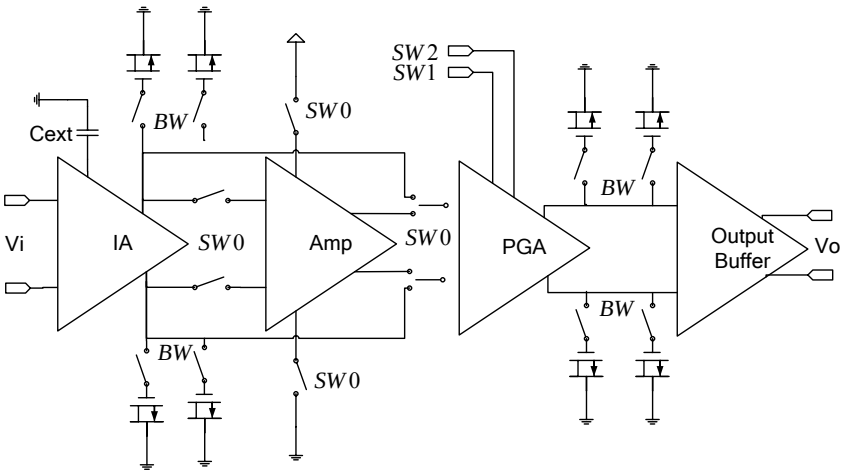


Figure 5-1 The 1.5-V biomedical signal readout analog front-end

IA

The instrumentation amplifier is similar to Figure 4-3. It is also an AC coupled chopper-stabilized amplifier with AC feedback circuits. The only difference is the opamp architecture shown in Figure 5-2 has CMOS chopper. Since the telescopic opamp has only one current branch, it has the best power efficiency. The thermal noise can be derived as

$$\overline{v_{ni}^2} = \frac{16kT}{3g_{m1}} \cdot \left(1 + g_{m7} / g_{m1}\right) \cdot \Delta f. \tag{5.1}$$

It is also less than that of a folded-cascode opamp. In other words, the telescopic opamp has better NEF. However, the drawback is that it is not suitable for low supply voltage. Compared to the proposed 0.8-V AFE IC, it is a low current and high voltage design.

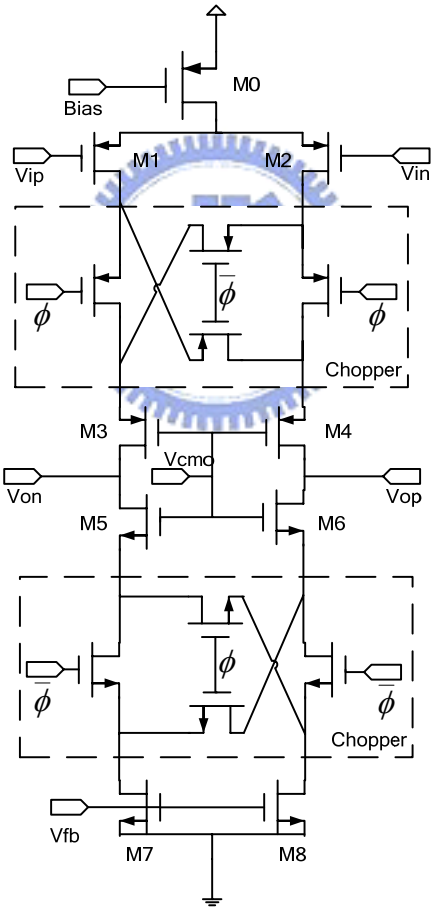


Figure 5-2 Telescopic mixer amplifier

The transistors M1 and M2 are operated in the sub-threshold region to have the highest tranconductance for a given current. The gain, bandwidth, output swing, and slew rate are derived as follows.

$$\text{Open-loop gain} = g_{m1} \cdot g_{m5} \cdot r_{o5} \cdot r_{o7}. \tag{5.2}$$

$$\text{Unit-gain bandwidth} = g_{m1} / C_L. \tag{5.3}$$

$$\text{Output swing} = 2 \cdot (V_{DD} - V_{od0} - V_{od1} - V_{od3} - V_{od5} - V_{od7}). \tag{5.4}$$

$$\text{Slew rate} = I_{M0} / C_L. \tag{5.5}$$

The simulation results of the opamp are shown in Figure 5-3. It has an open-loop gain of 90dB, a phase margin of 66 degree and an unit-gain bandwidth of 415KHz. The fully-differential OTA requires the common-mode feedback circuit shown in Figure 4-10.

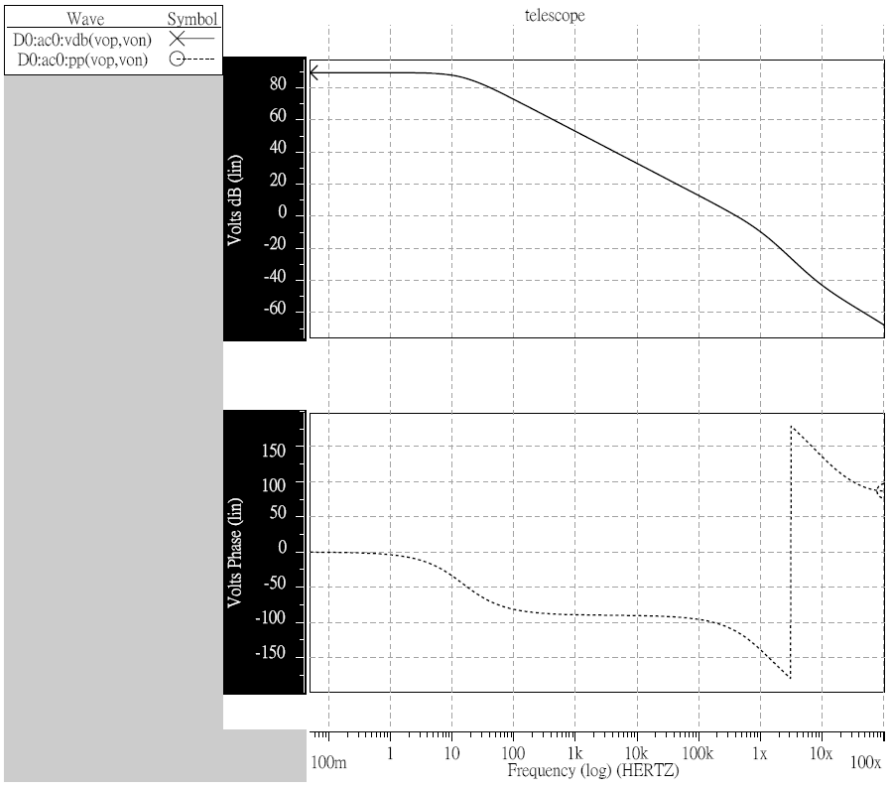


Figure 5-3 Gain and phase margin simulation

Amp Stage

The Amp stage is only activated when measuring EEG signal. The EEG has the smallest amplitude and the PGA is not able to offer enough voltage gain, so it requires Amp stage to do further amplification. It is a capacitive closed-loop amplifier. The input capacitance and the feedback capacitance set the closed-loop gain. The fully-differential OTA of the Amp stage is the same in Figure 4-12.

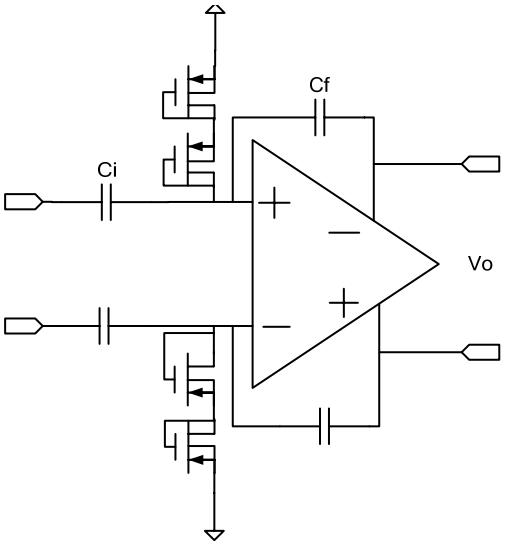


Figure 5-4 Amp stage

PGA

Figure 5-5 shows the programmable gain amplifier configuration. It includes a current-mirror OTA shown in Figure 4-12, capacitors, CMOS switches, and source-followers. It is similar to Figure 4-17, but a fully-differential architecture here. The midband gain is set by the input capacitance and feedback capacitance (5.6). Given a feedback capacitor Cf, we can select input capacitors Cin to set the PGA voltage gain. The source-followers cancel the parasitic resistance to ground.

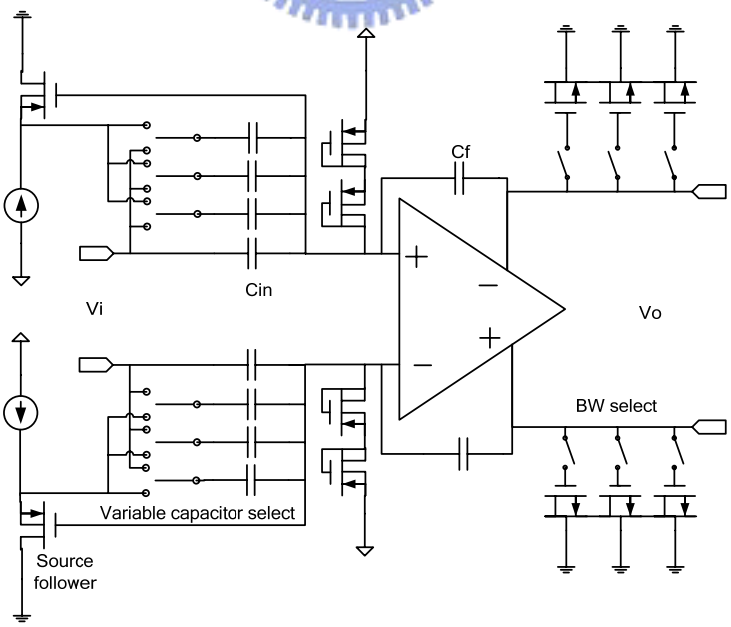


Figure 5-5 PGA

$$A(s) = -\frac{Cin}{Cf} \cdot \frac{s + \frac{1}{R_{par} \cdot Cin}}{s + \frac{1}{R_{par} \cdot Cf}} \cdot \frac{1}{1 + s \cdot \frac{Cin}{Cf} \cdot \frac{C_L}{G_m}}. \quad (5.6)$$

5.2 Simulation Results and Layout

Given a 5mVpp sine wave at 10.25Hz, the FFT simulation is shown in Figure 5-6. The horizontal axis is the frequency in linear scale and the vertical axis represents the magnitude in dB. The simulated THD is around 0.4%.

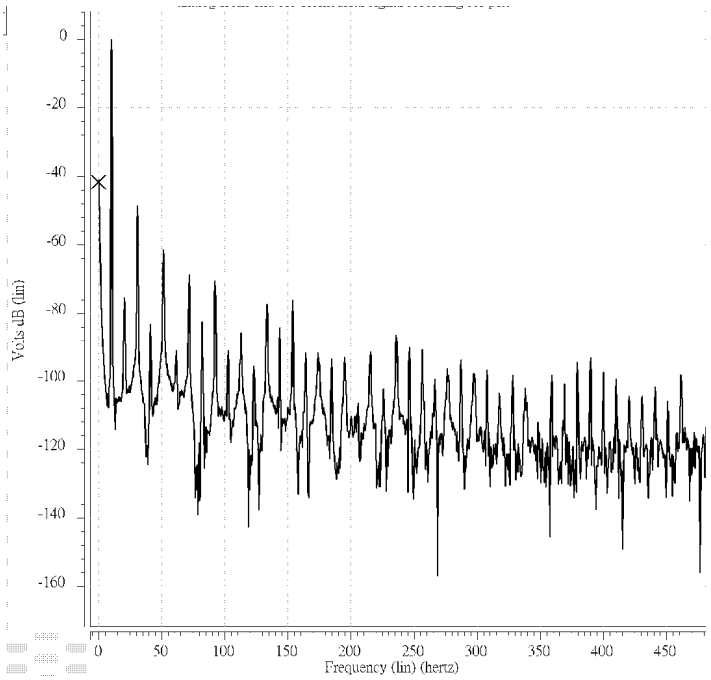


Figure 5-6 FFT simulation

Table 5-1 THD simulation in different corner cases

Corner	TT	SS	FF	FS	SF
THD (%)	0.402	0.482	0.359	0.362	0.387

Figure 5-7 shows the noise simulation results. There are two noise floors in Figure. The upper one is the input-referred noise without chopping. It is inversely proportional to the frequency evidently. The lower one activates the chopping technique and avoids the flicker noise within the signal bandwidth. The thermal noise

floor is 70 $nV/\sqrt{Hz}$.

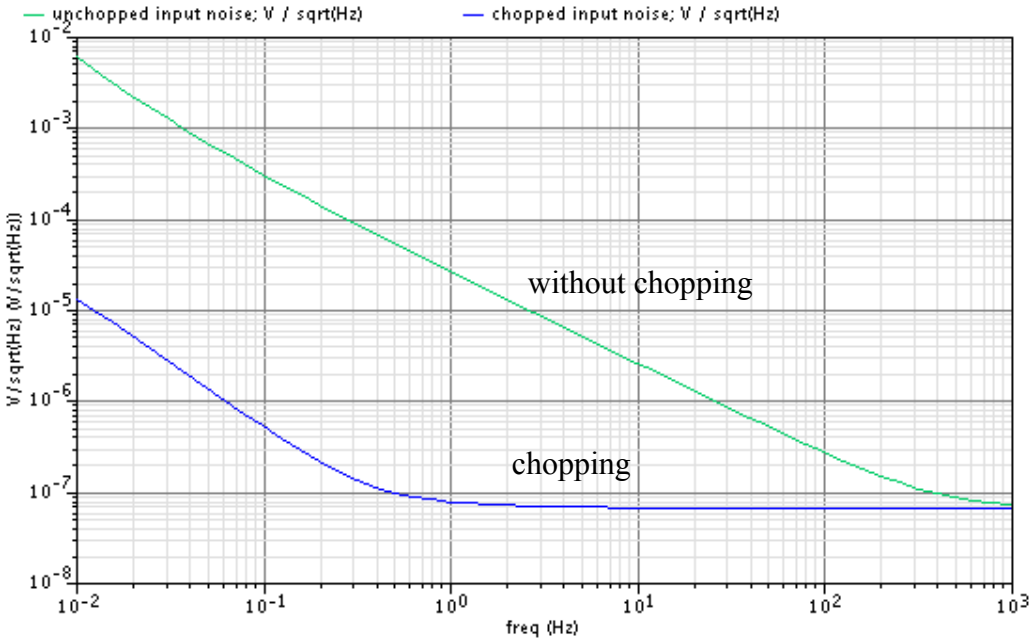


Figure 5-7 Input-referred noise density by Cadence Spectre

Table 5-2 Input-referred noise floor simulation in different corner cases

Corner	TT	SS	FF	FS	SF
Noise Floor ($nV/\sqrt{Hz}$)	70.7	73	69.2	70.6	72.4

Figure 5-8 is the transfer function of the front-end and Table 5-3 shows the voltage gain for each application. EEG has the smallest amplitude, so the Amp stage and the PGA offer the highest voltage gain at 50dB. Combined with the instrumentation amplifier, it has 88dB voltage gain. For ECG, 52dB voltage gain is sufficient. EMG has a higher frequency which requires a voltage gain of 58dB.

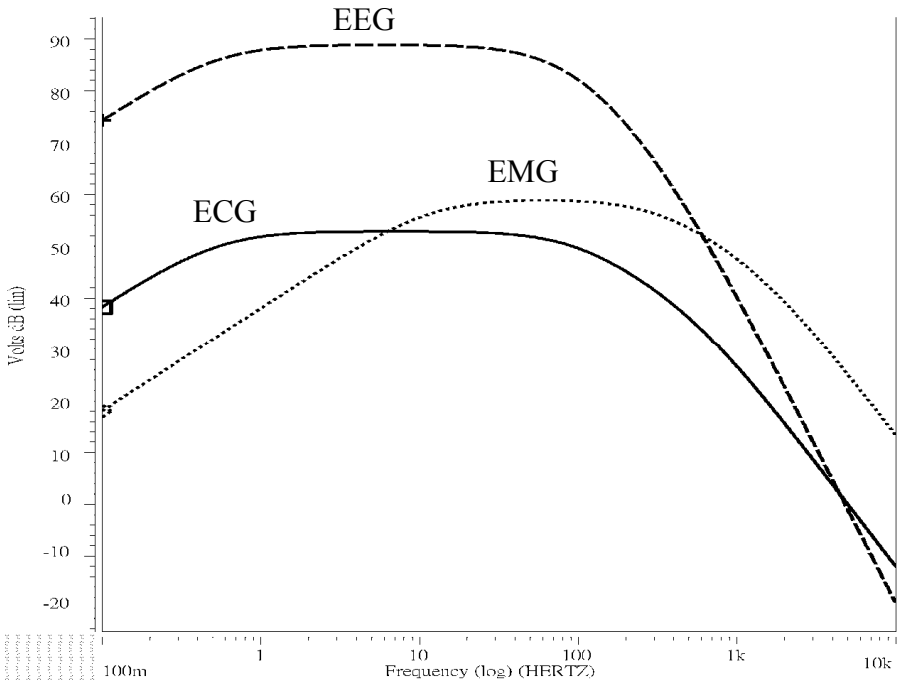


Figure 5-8 Overall transfer function

Table 5-3 Gain, bandwidth for biomedical applications

Application	Gain	Bandwidth
EEG	88dB	0.5-100Hz
ECG	52dB	0.5-150Hz
EMG	58dB	10-400Hz

From the specification in Table 5-4, the total supply current is merely 1.73μA and the supply voltage is 1.5V. Because the power efficiency of the telescopic opamp, it has a NEF of 3.6. The gain and bandwidth are digitally controlled. The chip is fabricated in TSMC 0.18μm. The layout of IC is shown in Figure 5-9. The core size is 0.6mm X0.63mm and the chip size is 0.86mm X0.89mm.

Table 5-4 A 1.5-V bio-potential signal acquisition analog front-end performance

Spec.	Performance Value
Supply Current	1.73μA
Supply Voltage	1.5V
NEF	3.6
Gain	46-88dB
Input-referred Noise RMS	0.7μV (100Hz)
CMRR(50/60Hz)	136dB
High Pass -3dB Frequency	0.5Hz
Low Pass -3dB Frequency	100-400Hz programmable
Core Area	0.38 mm^2
Technology	0.18μm

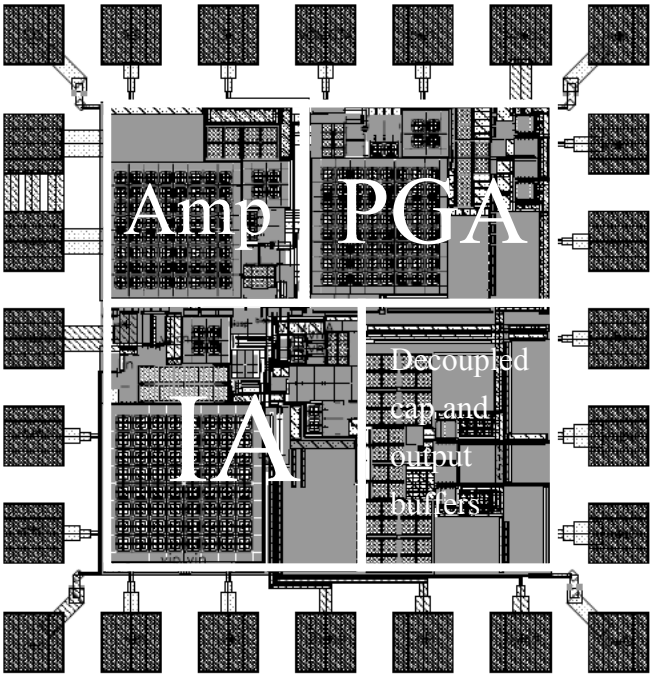


Figure 5-9 Layout of the AFE IC

5.3 Measurement Considerations

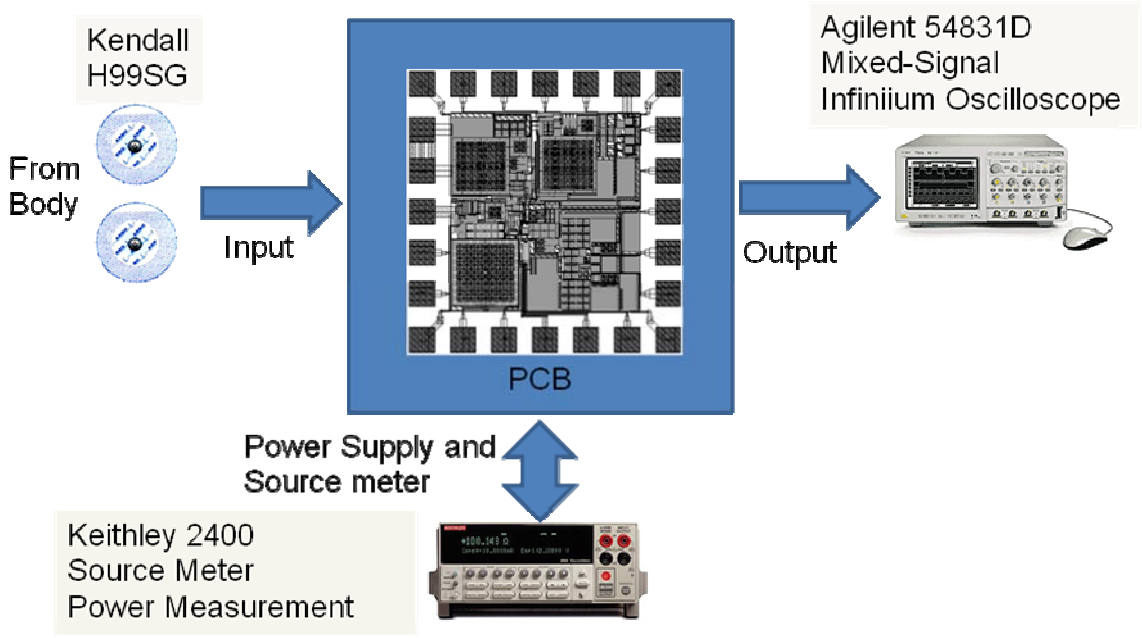


Figure 5-10 Measurement instruments

The measurement consideration is similar to the section 4.6. Locate the chip on the PCB board and bound the wires. To setup the environment, stick Kendall H99SG skin electrodes on the human body. The ECG signal is passed into the chip and the output waveform is analyzed by Agilent 54831D. Keithley 2400 general-purpose source meter supplies the voltage and measures the power consumption.

5.4 Measurement Results

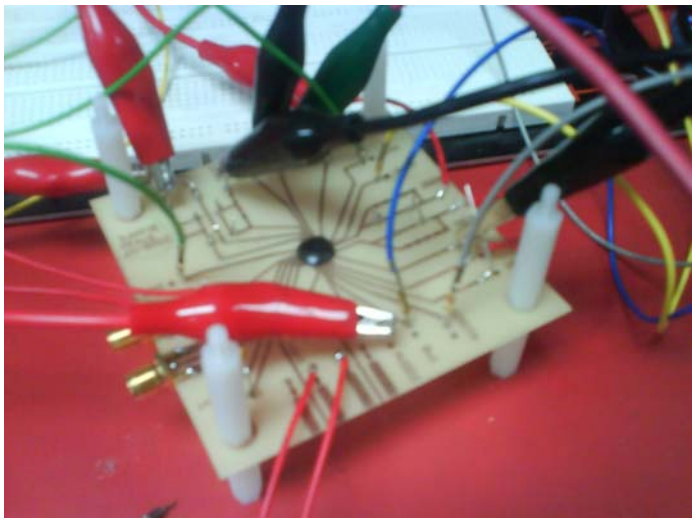


Figure 5-11 Setup the measurement environment

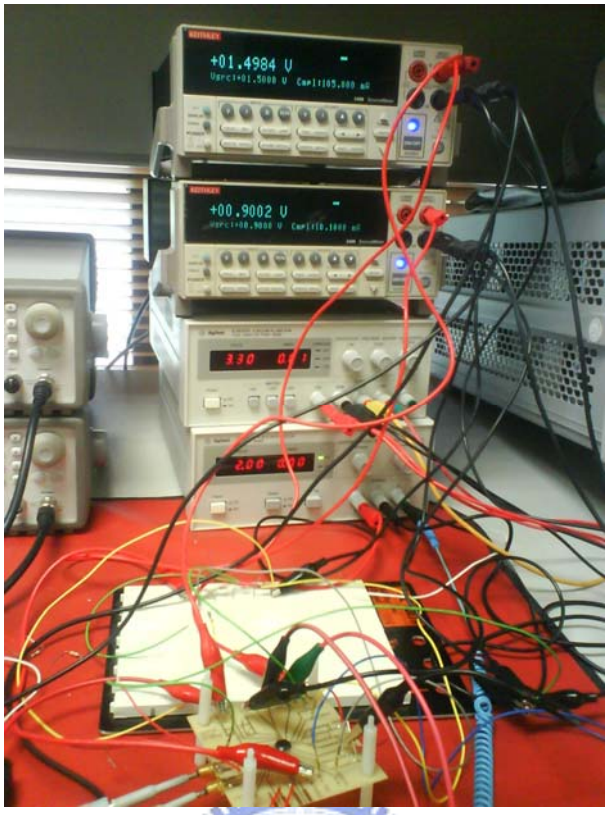


Figure 5-12 Measuring snap shot

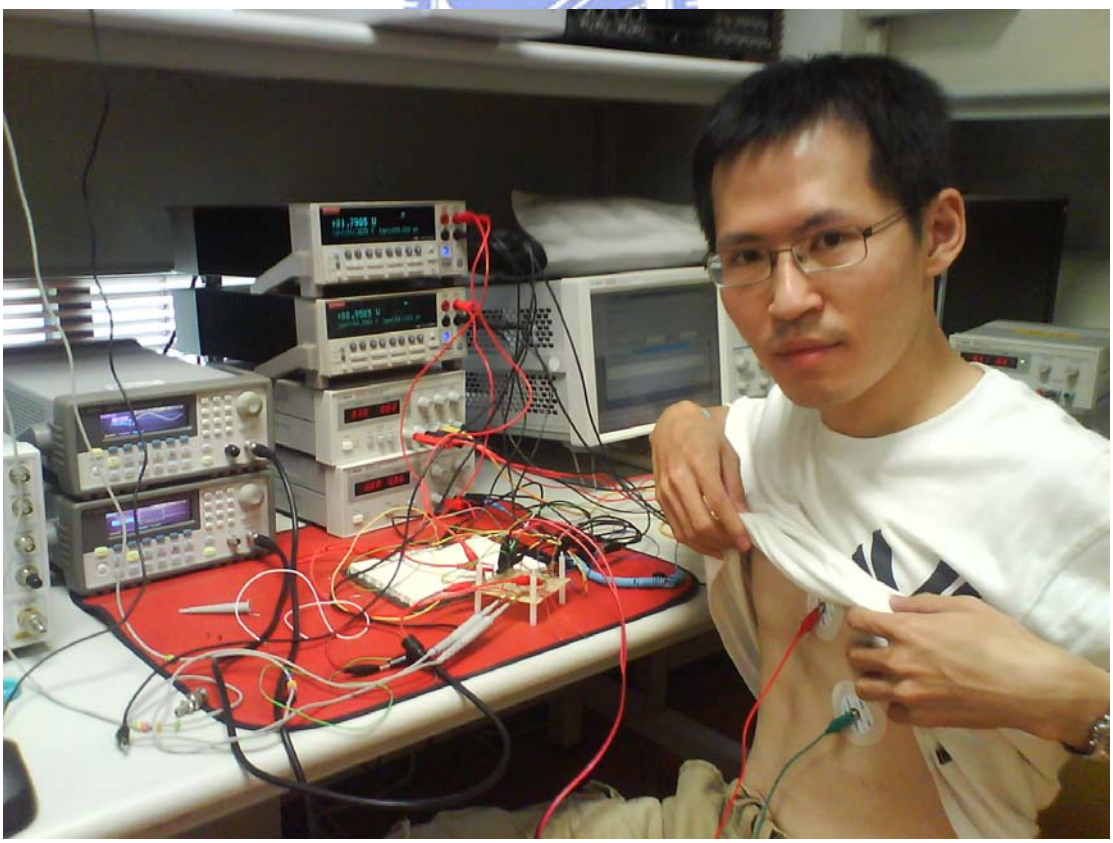


Figure 5-13 ECG measurement

The practical measurement photos are shown in Figure 5-12 and Figure 5-13. The positive input terminal is connected to the venticulus sinister and the negative input terminal is connected to atrium dextrum. The measured output waveform is shown in Figure 5-14. At the beginning, the electrodes offset causes the output to saturate and out of the operation point. The front-end circuit filters the output offset and cancels it. After less than one second, the front-end is back to the operation point. The clear QRS complex can be seen in the waveform. The distance of two R waves is about 0.85 second. Thus, there are 70 heart beats in a minute. Figure 5-15 shows the measured results for a longer time. The amplitude is 0.33Vpp and the R wave period is 0.833s. Figure 5-16 is the FFT result of Figure 5-15 by Matlab. The ECG signal component is mostly around 10Hz.

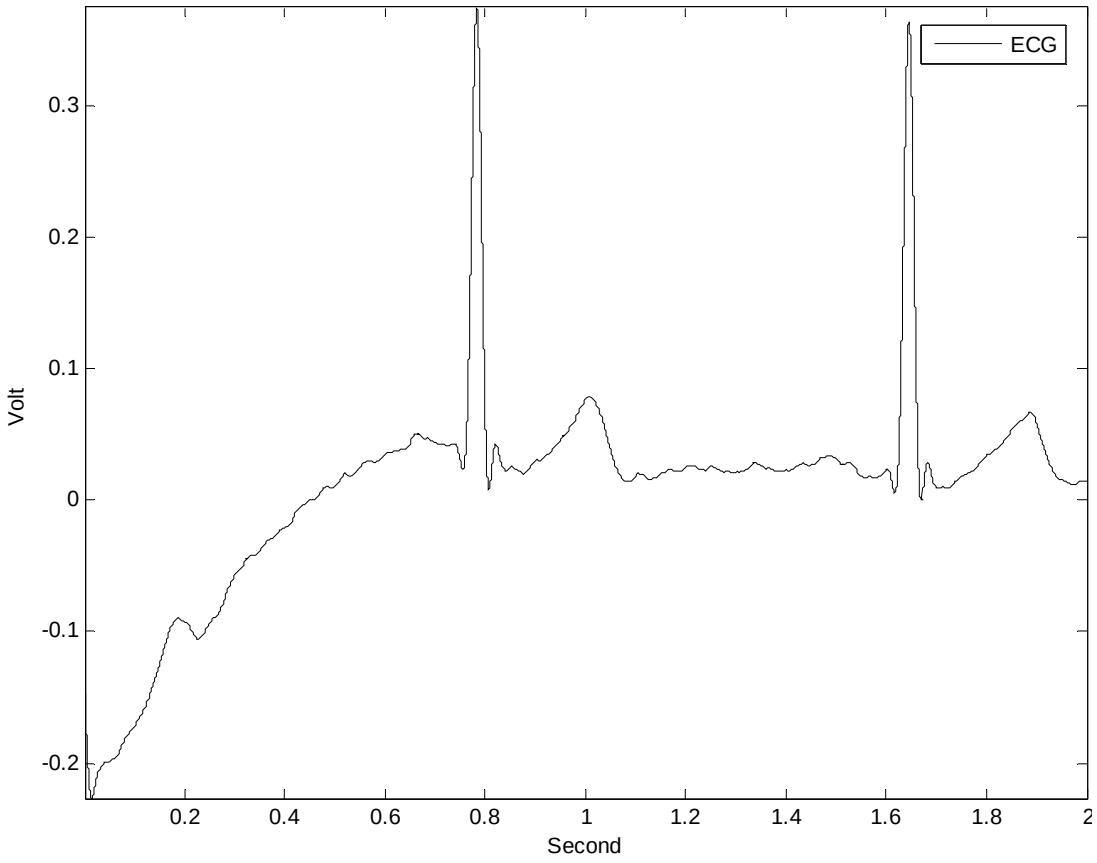


Figure 5-14 The output waveform. The electrode offset is cancelled and the output is back to the operation point.

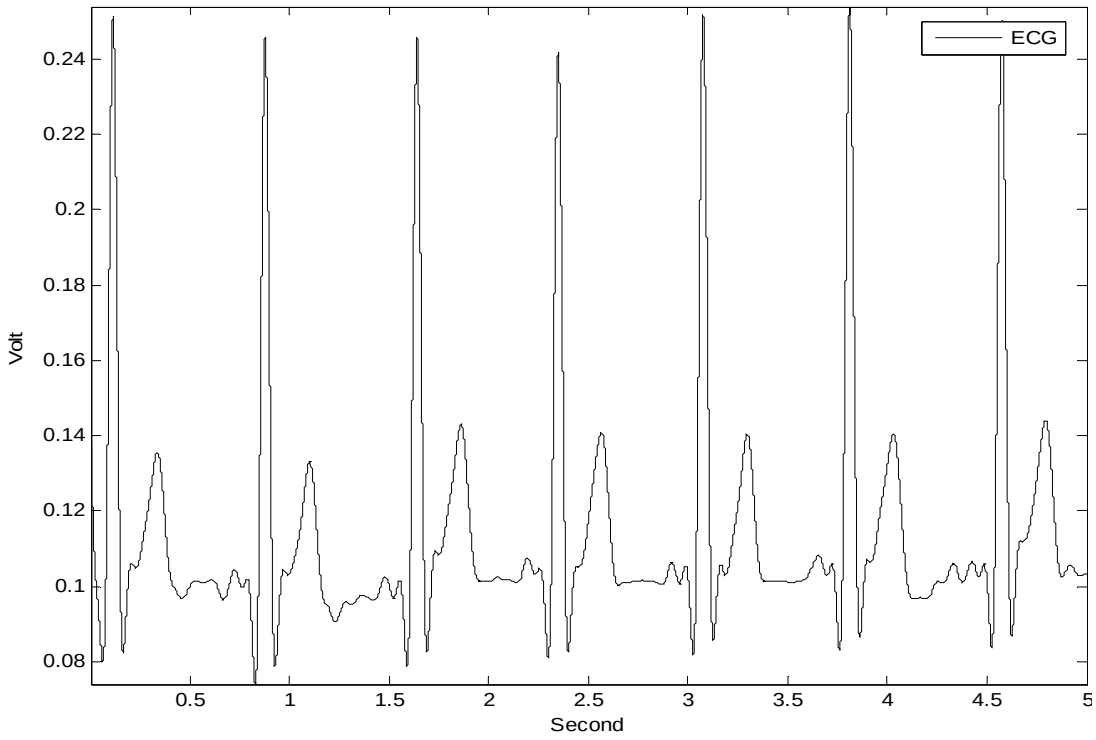


Figure 5-15 The Measured ECG output waveform.

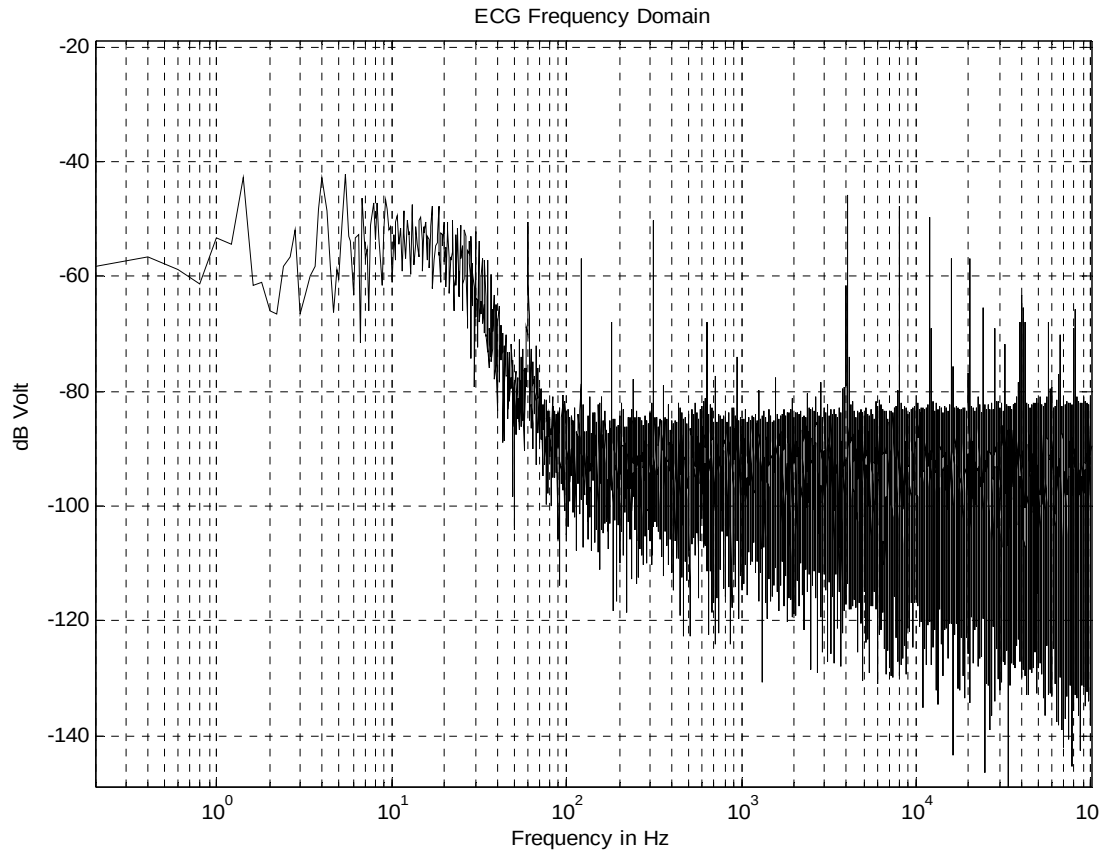


Figure 5-16 Measured ECG spectrums

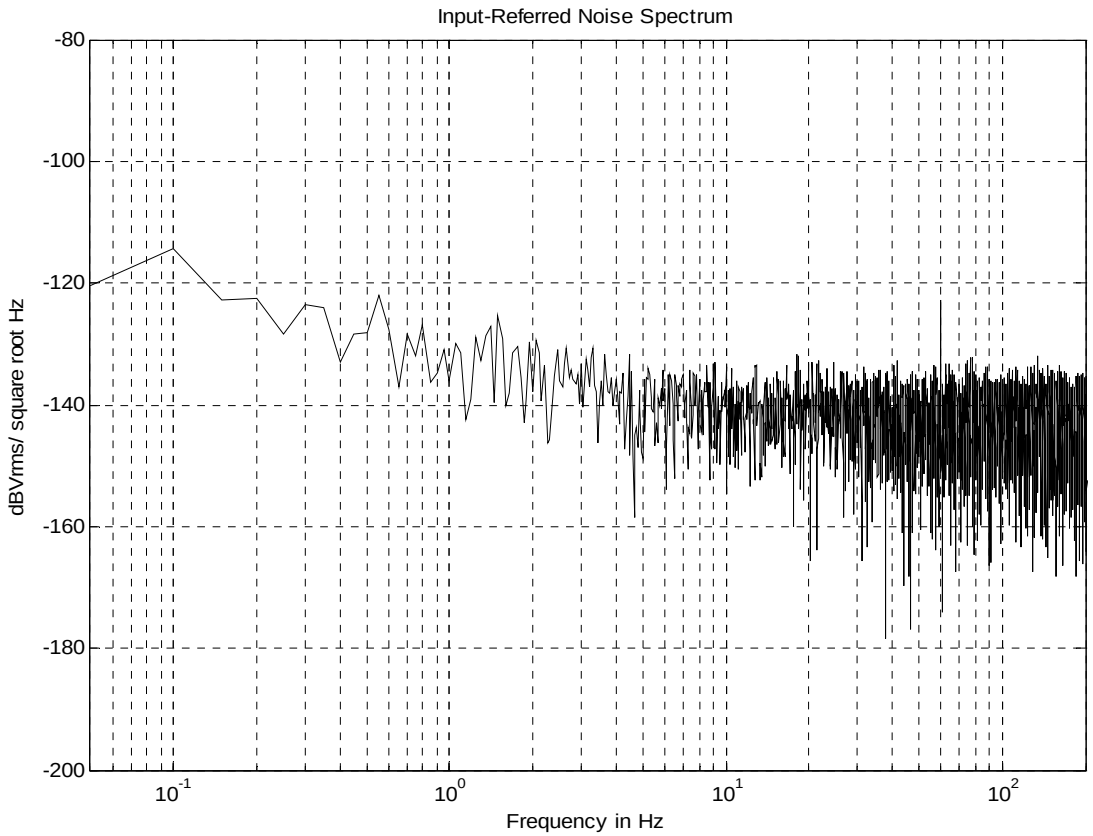


Figure 5-17 Input-referred noise spectrum density

To measure the input-referred noise, two input terminal are shorted to the ground. After settling, the output waveforms are captured and the output noise is obtained. Dividing the output noise by the voltage gain, the input-referred noise is obtained. The FFT results on the measured data are shown in Figure 5-17. The noise floor is $90\,nV/\sqrt{Hz}$ and the input-referred noise integrated from 0.5-100Hz is 1.27 μV. The chip achieves a dynamic range (1% THD) of 61dB with the total power current of 5μA.

5.5 Comparison

Table 5-5 shows the measured results of the chip. The total current is 5μA and the supply voltage is 1.5V. It has a voltage gain of 40.8dB, a NEF of 6.1, an input-referred noise of 1.27μV, and a dynamic range of 61dB. The active area is $0.4\,mm^2$ and it is realized in TSMC 0.18μm.

Table 5-5 Measurement performance comparison

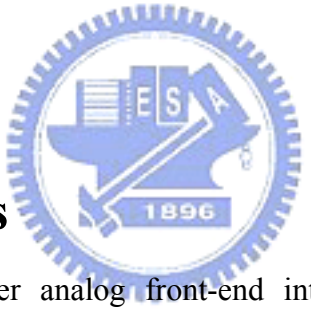
Amplifier	**This work simulation**	**This work measured**	Timothy Denison, ISSCC 07	R.F. Yazicioglu, ISSCC 06	K.A. Ng, JSSC 05	R. R. Harrison, JSSC 03
Supply Current	**1.73μA**	**5μA**	1.2μA	11.1μA	485μA	180nA
Supply Voltage	**1.5V**	**1.5V**	1.8V	3V	+/-1.5V	+/-2.5V
NEF	**3.61**	**6.1**	4.9	7.8	59	4.8
Gain	**40.8dB**	**40.8dB**	45.5dB	>60dB	80dB	40dB
Input-referred Noise RMS	**0.7μV (100Hz)**	**1.27μV (100Hz)**	0.93μV (100Hz)	0.65μV (100Hz)	0.73μV (100Hz)	1.6μV (30Hz)
Dynamic Range	**68dB**	**61dB**	60dB	68dB	71dB	69dB
High Pass -3dB Frequency	**0.5Hz, 10Hz**	**0.5Hz, 10Hz**	0.5Hz	0.5Hz, 10Hz	0.3Hz	0.014Hz
Low Pass -3dB Frequency	**400Hz**	**100-400Hz**	250Hz	>150Hz	150HZ	30Hz
Core Area	**0.4** mm^2	**0.4** mm^2	NA	2 mm^2	4.81 mm^2	0.16 mm^2
Technology	**0.18μm**	**0.18μm**	0.8μm	0.5μm	0.5μm	1.5μm

5.6 Summary

This chapter presents a 1.5-V analog front-end IC for biomedical applications. It includes an instrumentation amplifier integrated with Gm-C filter, an Amp stage and a PGA. The instrumentation amplifier uses the chopper-stabilized with AC feedback technique. It avoids the flicker noise and cancels the DEO. The Amp stage and PGA apply further amplification to the signal. The measurement results show the good ECG waveform. The chip achieves input-referred noise voltage density of 90 $nV/\sqrt{Hz}$ and the power consumption of 7.5μW.

Chapter 6

Conclusions



6.1 Conclusions

A low-voltage low-power analog front-end integrated with SAR ADC for biomedical signal acquisition is presented. It has configurable characteristic for common bio-potentials, including EEG, ECG and EMG. Furthermore, it is compatible with conventional AgCl electrodes. The whole system includes an AC coupled chopper-stabilized amplifier with an AC feedback circuits, a PGA, and an 11-b SAR ADC. The proposed front-end amplifier achieves an input-referred voltage noise density of 57 $nV/\sqrt{Hz}$ and a NEF of 4.7. It not only avoids the flicker noise and handles electrodes DC offset up to ± 50mV, but also rejects common-mode disturbance. Moreover, a digitally controllable PGA provides good compatibility with DSP. The proposed 11-b SAR ADC has a SFDR of 72.6dB, a SNDR of 63dB and a FOM of 0.09 $pJ/conv.step$. It is suitable for operation at a low supply voltage. The whole circuit has a SFDR of 54.2dB and a SNR of 54.1dB with a power consumption of 3.9μW. The chip is fabricated in TSMC 0.18μm.

6.2 Future Works

A bio-potential acquisition system includes analog front-end amplifiers, an ADC, and a DSP. To accomplish the system, the proposed analog front-end can be integrated with a DSP. Finally, the real product should be implemented for multi-channel biomedical signal acquisition in the future.

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