國立交通大學

電控工程研究所

博士論文

具有電荷儲存器和定電流機制的升壓電路用來改善 RGB 發光二極體背光模組效率

A Boost Converter with Charge-Reservoir Technique and Constant Current Regulator for Improving the Efficiency of RGB LED Backlight Module

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摘　要

目前色序法在液晶面版沒有濾光片的控制理論中可有效地減低色分離與運動模糊效應。由於 RGB LEDs 並非都是一直被開啟的，而是依序開啟紅、綠、藍 LED，再藉由混光的效果去實現 LCD 面版之影像色彩，可使電源消耗量降低，也因為其高色域和低電源消耗的特性，此項創新成為今日 LCD 顯示市場的潮流。因為藍光和綠光 LEDs 和紅光 LEDs 擁有不一樣的材料特性，所以紅光 LEDs 的順向電壓就有別於藍光和綠光 LED，因此在傳統紅綠藍三原色的背光模組會需要不同的直流對直流升壓轉換器去驅動不同顏色的 LED，

本篇論文提出只利用一個升壓轉換器以減少成本以及 PCB 佈局面積，具有快速轉換電壓技術，利用降壓-儲能與升壓-放能(Buck-store and Boost-Restore (BSBR))技術以及電荷回收(Charge Recycling(CR))技術，可快速的轉換輸出電壓以提供不同供給電壓來依序驅動串聯紅,綠,藍(RGB)發光二極體(LED)，來減低在定電流產生器上的電源損耗，在暫態的參考值追蹤時間之內，這一項創新的控制技術快速轉換電壓技術以及電荷回收技術，就被提出來增強追蹤參考電壓反應，當輸出電壓位準由低轉換至高供給電壓時，儲存在回收電容上的能量可以被用來對輸出電容充電，以將輸出電壓提升回高供給電壓位準。因此多餘的能量可被回收。實驗結果顯示出此技術的確可以有效的縮短追蹤參考電

壓的時間。此外，本項技術也另可提供一個調節電壓來驅動設立在液晶顯示器(LCD)系統上的副區塊。能源回收(CR)和降壓儲能升壓降能(BSBR)的最大效率分別可高達 90%和 94%，而本升壓 LED 驅動器的最大效率則為 94.5%。實驗結果證明了本篇提出的降壓-儲能與升壓-放能技術(BSBR)可達到快速且有效率的追蹤參考電壓效能。

關鍵字： 參考電壓追蹤，電荷回收，場色序法，發光二極體背光模組

A Boost Converter with Charge-Reservoir Technique and Constant Current Regulator for Improving the Efficiency of RGB LED Backlight Module

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Abstract

A Red, Green, and Blue (RGB) LED driver with the fast reference tracking (FRT) and charge-recycling (CR) techniques is proposed to implement a high efficiency and low cost RGB backlight module in color sequential notebook computers' display. The FRT technique can speed up the reference tracking performance and effectively improves the up-tracking performance. However, the down-reference tracking depends on the load current and output capacitor. Therefore, the charge-recycling and buck-store/boost-restore techniques are proposed to store extra energy on the re-cycling capacitor when the output voltage is switched from high- to low-voltage level and releases the reserved energy back to the output node at next period. Furthermore, the output voltage can be rapidly switched between two different voltage levels by FRT technique without consuming much power owing to the restored energy by the CR technique. The proposed BSBR technique not only stores and restores extra energy during the transient time of the reference tracking response to improve the efficiency but also enhances the reference tracking response to greatly reduce load transition time.

Experimental results show that the period of reference-tracking response can be improved. Furthermore, this BSBR technique also can provide a regulated voltage to drive the

sub-block implemented in the LCD system. The maximum efficiency of energy recycling with CR and BSBR technique is up to 90% and 94%, respectively. The total power consumption of a notebook computer's 15.4' LCD panel can be reduced from 5W in cold cathode fluorescent lamp (CCFL) backlight module to about 2-3W in RGB LED backlight module with the field color sequential (FCS) algorithm. Furthermore, after the implementation of the LED driver with the FRT and CR techniques, the power loss can be reduced to about 24% of that without the FRT and CR techniques,.

Keywords—Reference tracking, charge re-cycling, field color sequential, LCD, LED backlight, feedforward technique

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謝俊禹 謹誌

國立交通大學 電機與控制學系

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Chapter 1

Introduction

1.1 Background and the Backlight Module

For high-quality display in liquid crystal display (LCD) panels, the selection of the backlight module becomes more and more important. The selection of backlight system not only affects the power consumption but also determines display quality. The major light sources of LCD panel are cold-cathode fluorescent lamps (CCFL) and light-emitting-diode (LED). The structure of CCFL is shown in Figure 1. Currently, the CCFL light source is widely used in LCD TV because of the light-emitting principle and the physical structure. In addition, the LCD TV is very close to the fluorescent tubes used in our daily life. The outstanding features of this light source are simple structure, less temperature rise on the surface, high brightness, easy to be processed into various shapes.

But, there are also quite a few shortcomings as follows:

1. In general, the working life of CCFL backlight source is 15,000 ~ 25,000 hours. The longer the LCD using, the more of the decline in brightness. After being used for 2~3 years, LCD panel will be becoming dimmed and turning yellow, as the result of the defects owing to shorter working life of CCFL.

2. Each pixel of the LCD panel consists of three rectangular color blocks of R, G, B, while the color expression of LCD panel entirely depend on the performance of backlight module and color filter. The 3 primary colors of color filter are expected to

luminance a white light as homogeneous as the sun light, but the CCFL backlight module cannot actually meet the design requirements, only achieve 70% of the NTSC standard.

3. As the CCFL is not a flat light source, in order to output the backlight, LCD's backlight module needs to be collocated with diffuser plate, light guide plate, reflector, and many other auxiliary components. While the Raster Black or Raster White screen is displayed, the brightness difference between the panel edges and center is obviously significant.

4. As the CCFL backlight has to contain a diffuser plate, reflector and other complex optical components, the size of LCD is no longer further reduced. Furthermore, in the aspect of power consumption, the use of CCFL as a backlight source of the LCD is also unsatisfied.

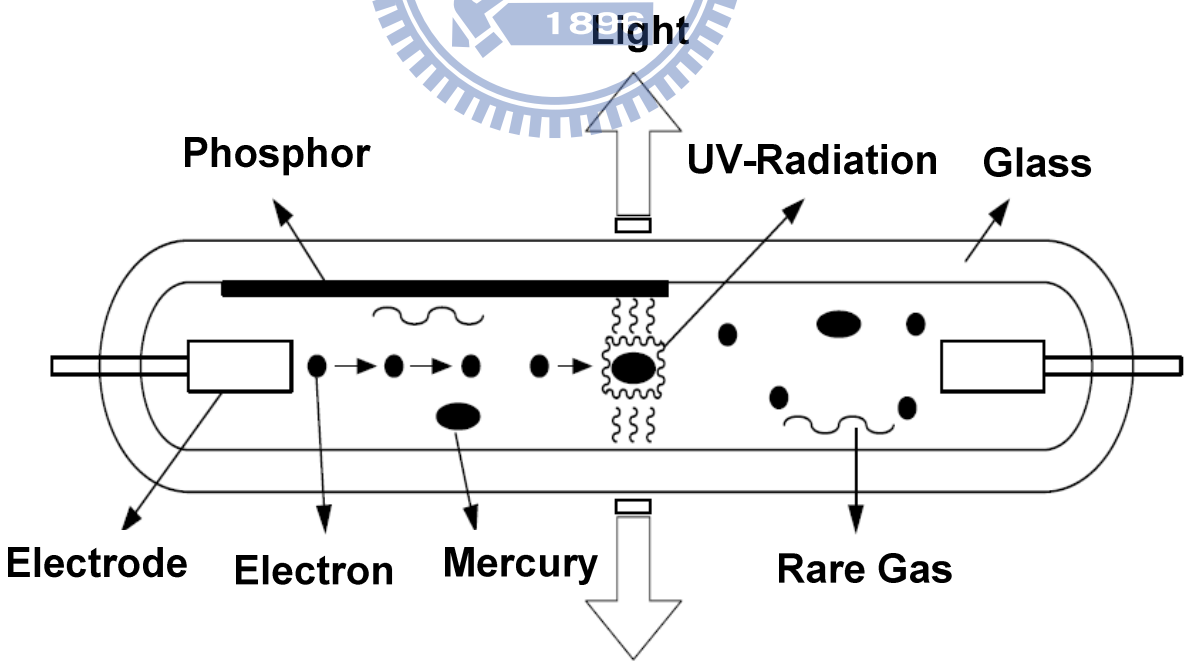


Figure 1. The structure of cold-cathode fluorescent lamps (CCFL) backlight source.

The other popular light source is LED which was invented in 1960. and the structure is shown in Figure 2. This light-emitting device can convert the electrical energy into light energy directly, with the outstanding features of low power consumption, high brightness and long working life. When LCD arrive in our world, it was recognized to be the terminator of CCFL, light bulbs and other lighting equipments, and have the opportunity to initiate a new era of lighting.

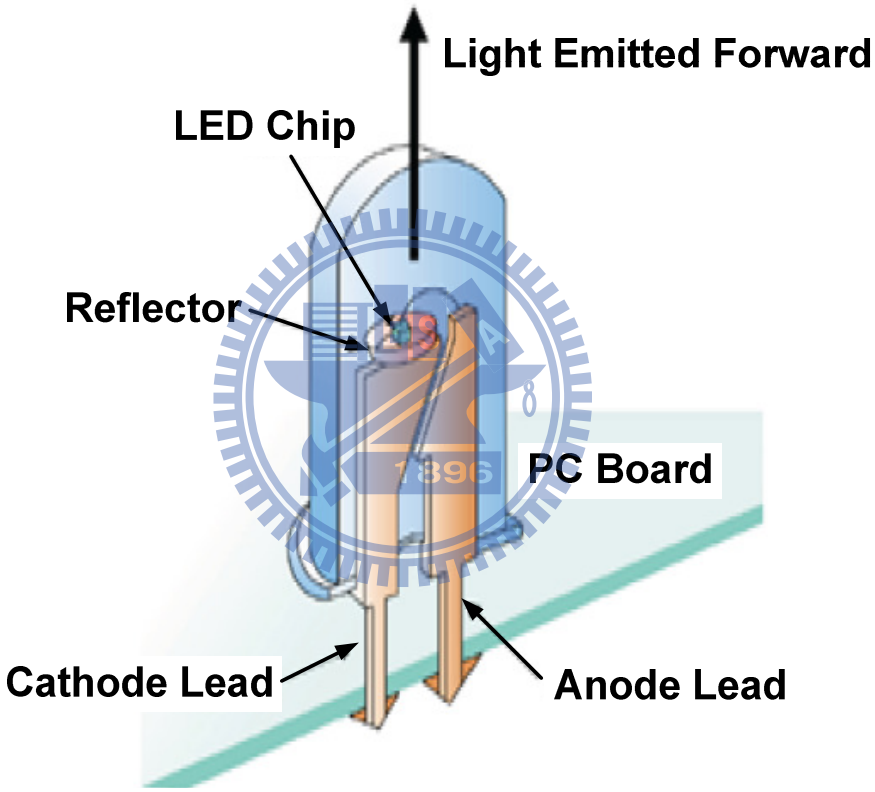


Figure 2. The structure of light-emitting-diode (LED) backlight source

Today's most popular and power-efficient backlight module is the white LED backlight in LCD panels since the power dissipation can be reduced about 40% compared to conventional CCFL backlight module. Moreover, since the backlight module will affect the color gamut, it is popular to make the use of LED backlight in the LCD panels for getting the higher color gamut. That is, the white-LED backlight has better color gamut than that of a

CCFL backlight. The disadvantage of the white-LED backlight is that it still needs the color filter to determine the color of the images since the operation of liquid crystal only determines the gray level of the image. In addition, the white-LED backlight generates only 70~80% National Television System Committee (NTSC) color gamut. Therefore, the color filter-less LCD panels with red, green, and blue (RGB) LED backlight can provide 110% NTSC color gamut as shown in Figure 3. Thus, the RGB LED backlight module becomes a trend of today's LCD display market to have better color gamut and low power consumption [1-2].

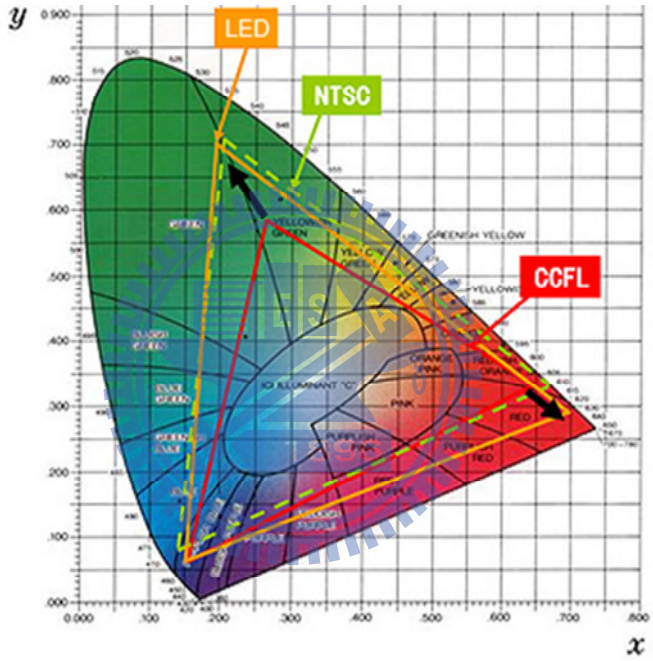


Figure 3. International Commission on Illumination (CIE) Chromacity Diagram

In addition to a good performance of color gamut, the adoption of the backlight source of RGB-LED can also enhance the contrast of LCD TV and HI-END display to achieve a more accurate gradation of gray level and layer sense of picture. LED backlight source is composed by a large number of tiny LED units that makes it successfully accomplishes the planarization of light source, any of them can attain an accurate LED brightness control, as well as the amendment of the brightness in the small region in accordance with the characteristics of the original image. The planarization of light source not only possesses excellent brightness uniformity, it does not

need a complex optical design. As a result, LCD can be made thinner, but also with a higher reliability and stability.

The ordinary working life of CCFL backlight source is about 25,000 hours, even a top-CCFL backlight source is nothing but 60,000 hours. At the end of working life, the LCD brightness will decrease significantly. However, there will be no such problem in using the panel of LED backlight source. The actual service life of a white LED backlight at this stage is 50,000~100,000 hours, which is basically the same as the life of LCD panel, but can be further enhanced potentially. Even if used 24-hours continuously, it still can work for 5 years.

In short, there are three main technical advantages for the LCD to use LED backlight source.

1. The planarization of light source.
2. In terms of color performance, the LED is far better than CCFL.
3. The luminous life of LED is far more than CCFL.

In theory, the cost of LED backlight module should be lower than the CCFL. However, the price of LEDli is still higher than the CCFL because the LED backlighting is still not mature enough, despite the LED manufacturers' great efforts, there are still a great price gap between CCFL and LED backlight module. Currently the price of LED backlight module components is about five times of the price of CCFL backlight. The larger panel size, the higher the costs of LED backlight technology. If without using the color filter and still can demonstrate the true colors, the cost of LED backlight module will be reduced by 30% and its popularity can then be speed up.

1.2 The Basic Theory of Field Color Sequential

According to the display method of the thin film transistor (TFT) LCD panel, the liquid crystal, which is functioned as a gate, is turned to the position determined by the content of the display data. Then, the light from backlight module only pass one of three color filters to

determine the correct color by the operation of the liquid crystal according to the image data. Therefore, the power loss due to the color filter is relatively large and the power consumption of the backlight module is difficult to be decreased because a lot of light is blocked by the color filter. Certainly, the best method is to remove the usage of the color filter.

Recently, the field color sequential (FCS) algorithm [3] that effectively reduced color breakup and motion blur effects can save much power consumption of the RGB LED backlight module without the requirement of color filter. The operation of the conventional FCS technique [3] shown in Figure 4. The frame per second (fps) for the FCS technique generally is 60Hz or 50Hz in the Europe. According to the FCS technique, one frame of data needs to be divided into three different color sub-frames, which are R_{scan}, G_{scan}, and B_{scan} as shown in Figure 4. Thus, the full color of one image can be constituted by the three sub-frames. As a result, the sub-frame rate of the three sub-frames is 180Hz. The operation of one sub-frame contains three basic steps. The first step is the operation of Thin Film Transistor (TFT) scanning in order to get the image color data. Secondly, according to the image color data, liquid crystal is rotated to the correct position within liquid crystal time t_{LC}. Finally, after liquid crystal is turned to the correct position, the LED backlight module emits correct light through the LCD panels to display the image colors at the rest of time, t_{BL}, which indicates the lighting time to determine the brightness of backlight module. Because the RGB LED are not turned on simultaneously but sequentially, the power consumption can be reduced. However, the value of time t_{BL} is too small to provide the rated brightness since one frame is divided into three sub-frames. In order to extend the lighting time of backlight module, there are many techniques proposed [2-5] in high-performance color sequential display. Persistence of vision can make the color image appear in human's eyes without sacrificing the color gamut compared to conventional CCFL backlight. For portable devices like notebook computers, the largest power consumption comes from the backlight module.

Therefore, it is important to decrease the power consumption in backlight module of the notebooks without sacrificing any image quality. As a matter of course, the color filter-less LCD panel with the FCS technique proves to be the best choice to reduce the power consumption of the display panels in the design of notebooks. Consequently, the RGB LED backlight module with the FCS technique becomes more and more popular owing to the characteristics of low power consumption and high image quality.

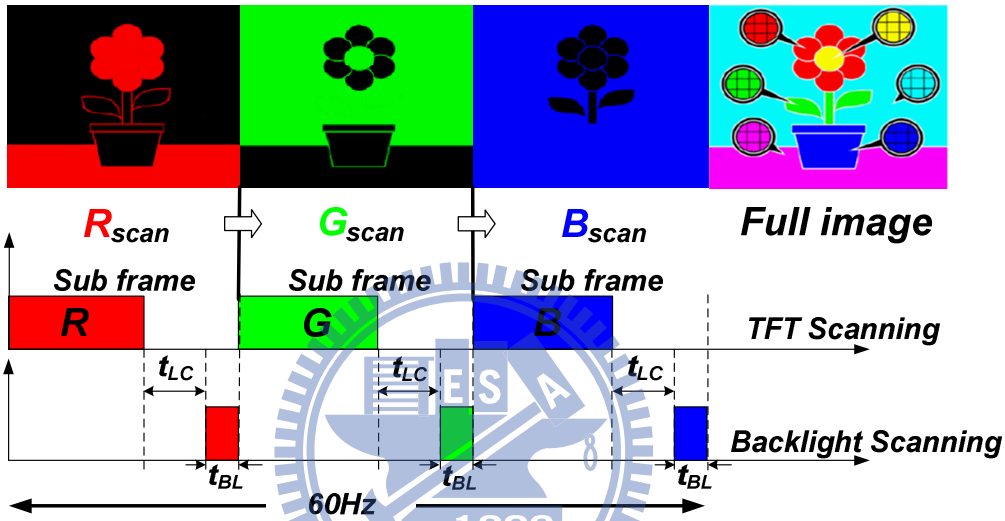


Figure 4. The timing diagram of color sequential technique for the color filter-less LCD panel.

The power consumptions in the recently LCD panels are reduced to 15W in white LED backlight and 5W in color sequential RGB LED backlight system, respectively, compared to 30W in CCFL backlight. However, there is the color breakup effect when the RGB LED emit light in sequence in the FCS technique. Thus, a modified FCS algorithm is utilized to generate the color breakup-fewer patterns for reducing the side effect of color breakup [1] as shown in Figure 5. For the implementation of modified FCS algorithm, the LCD panel is divided into three sections to display different colors owing to the small-size panel of the notebooks. Furthermore, the RGB backlight module employs impulse-type display method instead of the hold-type display by CCFL backlight technique for eliminating the motion blur [1]. The

disadvantages of the conventional FCS technique can be alleviated by the implementation of the modified FCS algorithm.

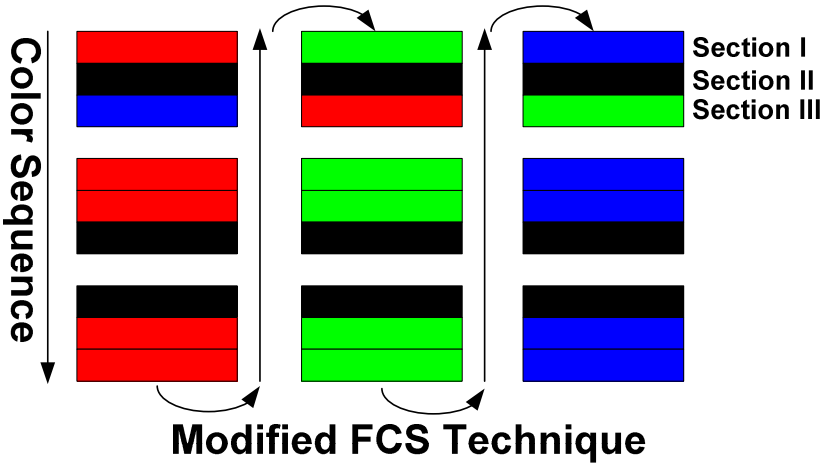


Figure 5. The implementation of modified FCS algorithm for reducing the color breakup and improving the efficiency.

1.3 The Analysis of Power Consumption and the Overall Efficiency in the RGB LED Driver

The comparison of power consumption between a conventional TFT-LCD with a white-LED backlight module and a FCS TFT-LCD with a RGB-LED backlight module is illustrated in Figure 6. Interestingly, the FCS technique can save 40% power compared to the conventional LCD display because there is no color filter that may reduce the brightness in the front of the LCD panel. Hence, the power consumption of the backlight module can be drastically minimized. Furthermore, this technique can be extended to contain the local blanking/dimming technique according to the locally averaged image data. That is, a higher power saving result can be achieved and thus the power reduction can be more than 60%. Actually, the minimum power consumption of the LCD display can be reduced to 20% of the conventional design when the backlight system is turned off. However, the image only contains gray levels at this moment. For portable devices like notebook computers, the largest

power consumption comes from the backlight module. The power consumptions in the recent LCD panels are reduced to 5W in white LED backlight and 3W in color sequential RGB backlight system, respectively, compared to 10W in CCFL backlight. Therefore, it is important to decrease the power consumption in backlight module of the notebooks without sacrificing any image quality.

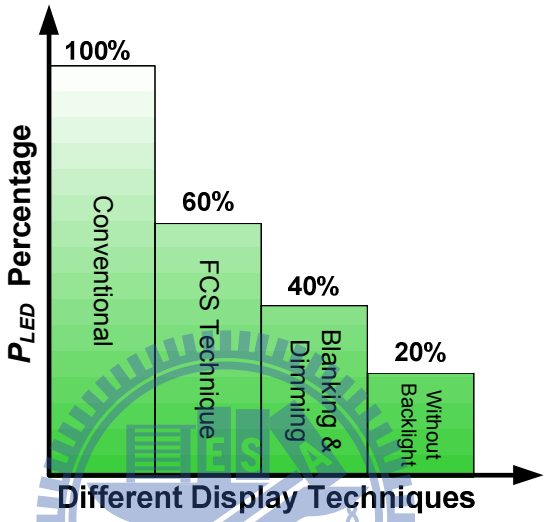


Figure 6. The current waveform of inductor, diode and power MOS(I_{Q1})

In addition, when the modified FCS technique is applied in the LCD panel, there is only one of three colors or black frame appearing in each section of the LCD panel. In general, the forward voltages of red, green, and blue LED are different to each other owing to the characteristic of material. Furthermore, the light illumination of LED is related to the amount of driving current and the forward voltage [6-7]. However, it is unreliable that the light illumination is controlled by utilizing the forward voltage when temperature and time is changed [8-9]. That is, it is inappropriate to make use of forward voltage to control the brightness of LED for getting high quality image of LCD panel. In order to get uniform and sufficient luminance, the LCD backlight module requires many LED to be series-and parallel-connection. The series connection ensures the series LED have the same conduction current. The parallel connection needs a constant current regulator circuit to maintain stable and

uniform light illumination in every series connection as shown in Figure 7. The Single Boost DC-DC converter is used to offer a sufficient voltage to overcome all the forward voltage V_{LED} of series LEDs. Owing to the great variation of LED material, each of the series LED forward voltage V_{LED} is different. Hence, the current balance circuit is designed as the current of LED I_{CC} that is independent of the voltage V_{CC}, which is the voltage across the current balance circuit. In general, the LED module will minimize the voltage V_{CC} [8-9] for reducing the power consumption because the power consumption is equal to the product of V_{CC} and I_{CC}. If the output voltage is larger than V_{LED}+$V_{CC(min)}$, the redundant voltage will be across the current balance circuit. Therefore, the power loss will be increased and the efficiency η_{LED} of the LED array, which depends on the ratio of the V_{LED} and the V_{out}, will be decreased. In order to improve the efficiency of LED backlight module, the value of the voltage V_{CB} must be minimized and the variation of the voltage V_{CB} will not affect the driving current I_{CB}.

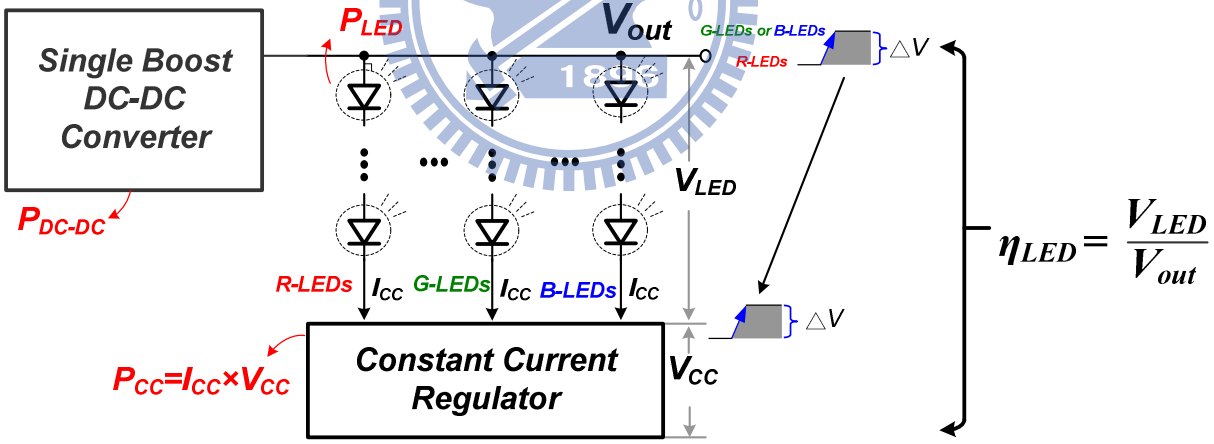


Figure 7. Inductor current are CCM operation at heavy and medium loads

The power dissipation P_{module} in LED backlight module for the FCS technique is composed of three parts as expressed in (1).

$$P_{module} = P_{LED} + P_{CC} + P_{DC-DC} \tag{1}$$

P_{LED} is the power consumption on the series-connected LED when the constant driving current flows through and forces the LED to emit light to the LCD panel. The constant driving current generated by the constant current generator consumes power dissipation P_{CC}, assuming the voltage across the constant current generator is V_{CC}. Besides, the power dissipation of the boost DC-DC converter is $P_{DC\text{-}DC}$. In the efficiency consideration of the backlight module, the power conversion efficiency of the switching DC-DC converter is higher than 90%. That is, the reduction of power loss $P_{DC\text{-}DC}$ in the DC-DC converter is much smaller than those of other power dissipations and cannot be decreased remarkably. Thus, in order to reduce the overall power consumption of the LED backlight module, the primary consideration of reducing power consumption is focused on the P_{LED} and P_{CC}.

When the power consumption of conventional LCDs with white-LED backlight and FCS LCDs with RGB-LED backlight are compared under the same light illumination condition, the FCS technique can save 40% power compared to the conventional LCD display since there is no color filter that reduces the brightness of the LCD panel. Hence, the power consumption P_{LED} of the backlight module can be drastically minimized. The power dissipation on the constant current regulator is proportional to the current I_{CC} and the headroom voltage V_{CC} as shown in Figure 7. According to the aforementioned statement, the I_{CC} is designed to define the brightness of LCD panel which should not be reduced arbitrarily. Therefore, the LED backlight module is designed to minimize the voltage V_{CC} for reducing the power consumption [10-11]. Generally speaking, since the material characteristic of blue and green LED is indium gallium nitride (InGaN) and the material characteristic of red LED is aluminum gallium indium phosphate (AlGaInP) [12], the forward voltages of red LED are different from that of green and blue LEDs. That is, the forward voltage of green and blue LED is approximately 2.8~3.3V, and the forward voltage of red LED is close to 2.2~2.8V. Moreover, LED drivers use constant current regulator to provide the constant current for

constant lumen. In general, the constant current generator occupied minimum about 0.4V to keep the characteristic of regular current and when the current is regulated to 25mA, the forward voltages of an R-LED and a G-LED (or B-LED) are close to 2.2V and 3V, respectively. As a result, the LED backlight driver would employ more DC-DC converter to provide different output voltage for overcoming the forward voltage of different color series-LEDs. Therefore, the LED with different colors require different supplying voltages [13]. That is, the implementation of the LED driver of the modified FCS algorithm needs nine DC-DC converters for driving the notebook's panel with the advantages of much power saving on the current balance circuit. However, the disadvantages are required the larger cost and the printed circuit board (PCB) area.

This thesis proposes two kinds implementations of the RGB backlight module for achieving the fast reference tracking. First method, the charge recycling (CR) technique and the fast reference tracking (FRT) are applied to a single boost converter. The other method is the buck-store and boost-store (BSBR) technique. The proposed fast reference tracking (FRT) can enhance the transient response of up- and down- reference tracking. The proposed CR and BSBR techniques can store extra charge and recycle it back to the output node when the backlight module switches between the R-LED and G-LED (or B-LEDs). The efficiency of CR and BSBR techniques can be up to about 90% and 94%, respectively, which is the common power efficiency in DC-DC converters. Moreover, the BSBR stage not only can operate the buck-store and boost-restore operations in order to achieve fast reference tracking performance but also can supply the regulated voltage V_{BSBR} by the Pulse Frequency Modulation (PFM) control when the stored charge needs to supply other sub-blocks of the system. The fast reference tracking performance can ensure the voltage across the constant current generator is minimized to achieve high efficiency. As a result, the equation of

luminance efficiency, which indicates the power transformation from the electric power to light luminance, can be written as (2).

$$\eta_{module} = \frac{K \times P_{LED}}{P_{LED} + P_{CC} + P_{DC-DC}} \tag{2}$$

K indicates the converting coefficient from electric power P_{LED} to luminance of light. This value of K depends on different display techniques and backlight characteristics. This thesis uses the FCS technique to enhance the value of K so that the backlight module can achieve better light luminance by means of smaller power dissipation P_{LED}. Furthermore, the DC-DC converter with the BSBR technique can efficiently store and recycle extra charge, and thereby reducing the value P_{CC} to improve the overall efficiency η_{module}. As a result, the proposed techniques can reduce the number of DC-DC converters and output component for reducing the cost and the printed circuit board (PCB) area. In addition, the high efficiency also can be acquired.

1.4 Prior Arts

The conventional RGB LED backlight module with conventional FCS algorithm, which utilizes many output components and DC-DC converters for providing the different output voltages, is illustrated in Figure 8 [14-16] because the forward voltages of red, green, and blue LED are different to each other from the characteristic of material. Therefore, the cost and footprint area is an drawback in the conventional LED backlight module system. In addition, when the modified FCS algorithm is applied in the LED backlight module, the LCD panel is divided into three sections to display different colors for the small-size panel of the notebooks. There is only one of three colors or black frame appearing in each section of the LCD panel as shown in Figure 4. As a result, the LED driver with the modified FCS algorithm requires nine

DC-DC converters for driving the notebook's panel with the advantages of much power saving on the current balance circuit.

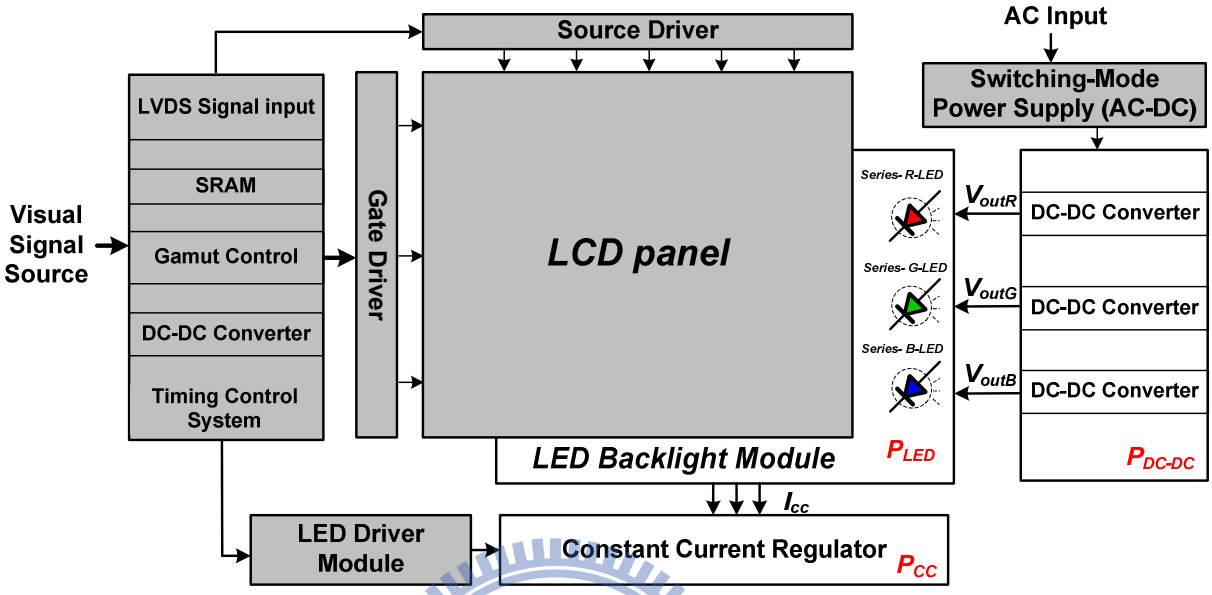


Figure 8. Conventional RGB LED backlight with three DC-DC converters.

In general, the six series LED are applied in the LED backlight module of notebook, and thus LED backlight module would supply 16 V and 21 V for 6 series R-LED and G- or B-LEDs, respectively. Since the bandwidth of the DC-DC converter is limited to the low-pass filter which is composed of the inductor and capacitor, the fast output voltage tracking between 16V and 21V is very difficult in the conventional DC-DC boost converters. Therefore, the LED with different colors require different supplying voltages [13]. That is, the implementation of the LED driver of the modified FCS algorithm needs nine DC-DC converters for driving the notebook's panel with the advantages of much power saving on the constant current regulator.

The conventional voltage-mode PWM buck converter is depicted in Figure 9 (a). The power stage is composed of power transistors M_P, M_N, and low-pass filter which is formed by inductor L and capacitor C_L. The error amplifier with compensated resistor and capacitor

compare the reference voltage V_{ref} with feedback voltage V_{fb} to generate the error signal V_c for determining the duty cycle of PWM signal V_{PWM}. In addition, the duty cycle of continuous-conduction mode (CCM) buck converter has a relationship with output voltage and input voltage (V_{out}/V_{in}). Thus, the conversion equation is given by

$$\frac{V_{out}}{V_{in}} = D = \frac{V_c - V_L}{V_H - V_L} \tag{3}$$

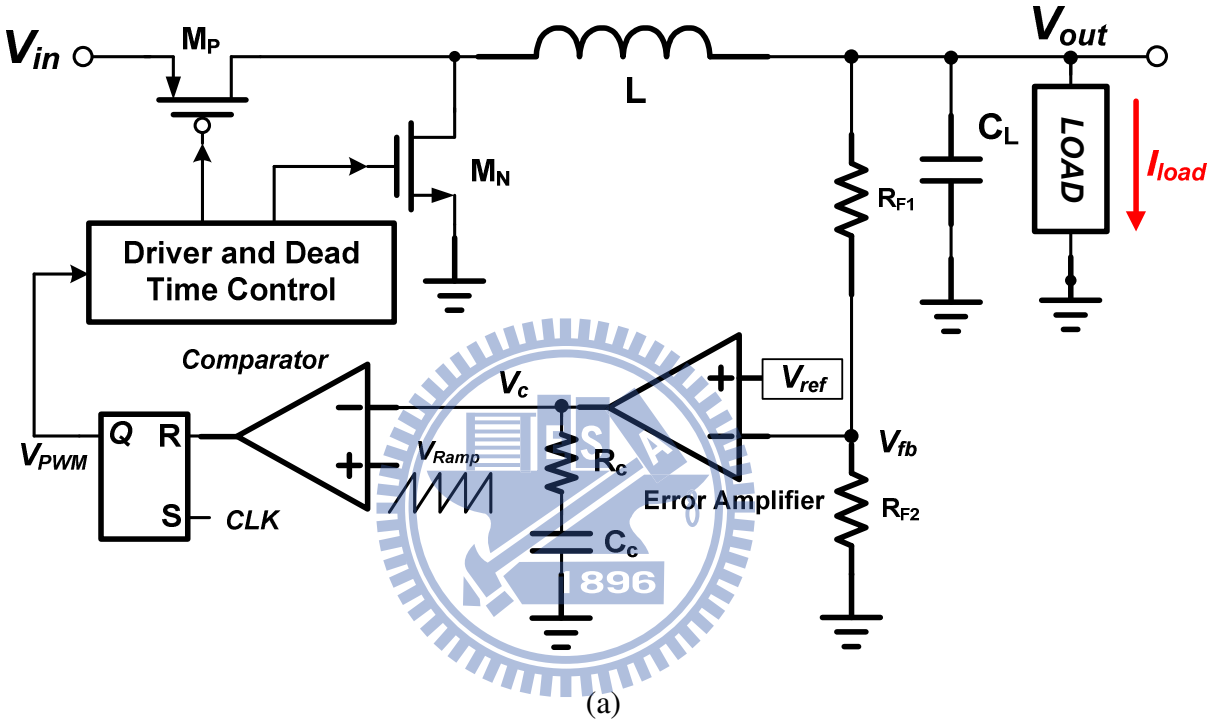
where V_H and V_L are upper and lower bounds of the ramp signal VRamp. When the reference voltage V_{ref} is changed, the output voltage V_{out} would be varied by changing the duty cycle of PWM signal V_{PWM} as shown in Figure 9 (b). Since a large compensator capacitor is utilized to provide the dominant-pole for compensating the power system. The signal V_c would slowly raise to the steady state and the tracking response of output voltage is slow.

This thesis proposes a DC-DC converter with fast reference tracking to provide the output voltage for overcoming the different color of series-LEDs. The new implementation of the RGB backlight module is depicted in Figure 10 for achieving low cost and high efficiency. It is obvious that only one DC-DC converters are employed. The hardware cost and volume can be effectively reduced.

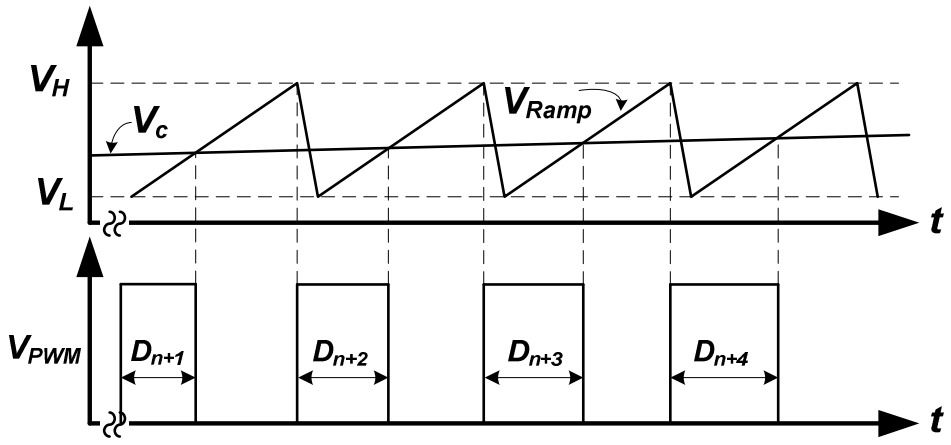
Several topologies and control techniques have been proposed to fast reference tracking output voltage. The reference tracking technique in [17] proposes the end-point prediction (EPP) for voltage-mode PWM buck regulator as shown in Figure 11. A voltage adder is required to sum the error signal V_{c1} and reference voltage V_{ref} to form the V_{c2} and generate the PWM signal. In addition, this technique design that the upper bound of ramp signal V_H is equal to

$$V_H = b \times V_{in} + V_L \tag{4}$$

where b is the ratio of feedback resistor (R_{F1} and R_{F2}). Therefore, the information of reference voltage and input voltage is acquired to generate the PWM signal for improving the transient response of reference tracking. However, the transient response of up-tracking still be clamped by the compensation capacitor.



(a)



(b)

Figure 9. (a)Conventional voltage-mode PWM buck converter. (b) The transient duty cycle of PWM signal V_{PWM} at reference tracking.

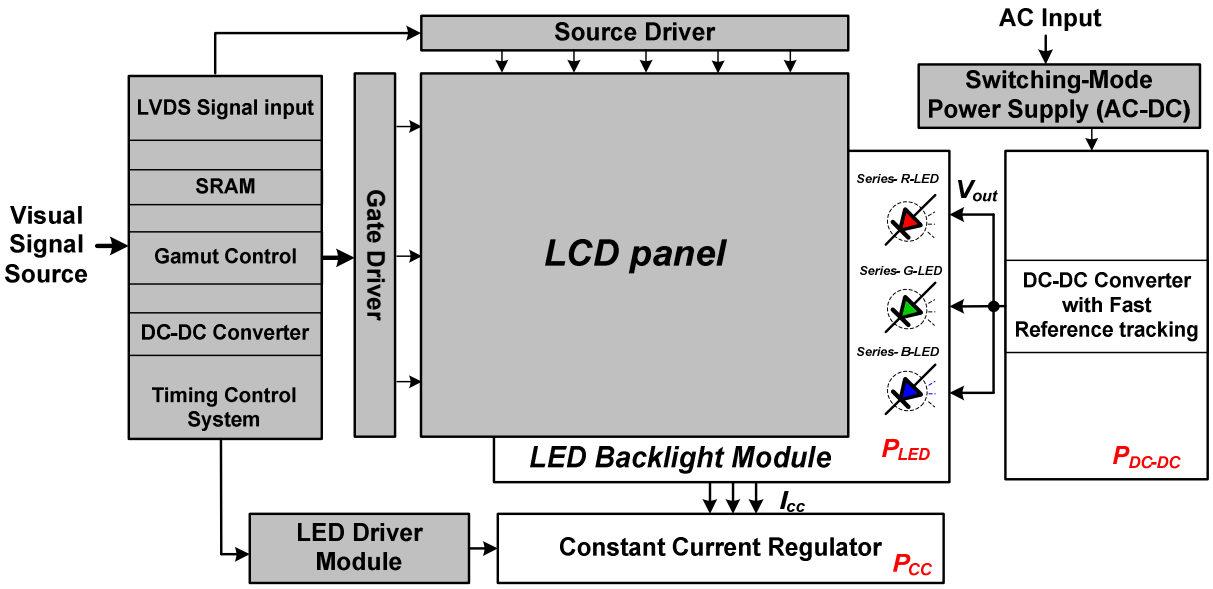


Figure 10. A high efficiency RGB LED backlight with one DC-DC converter for implementation of conventional FCS algorithm.

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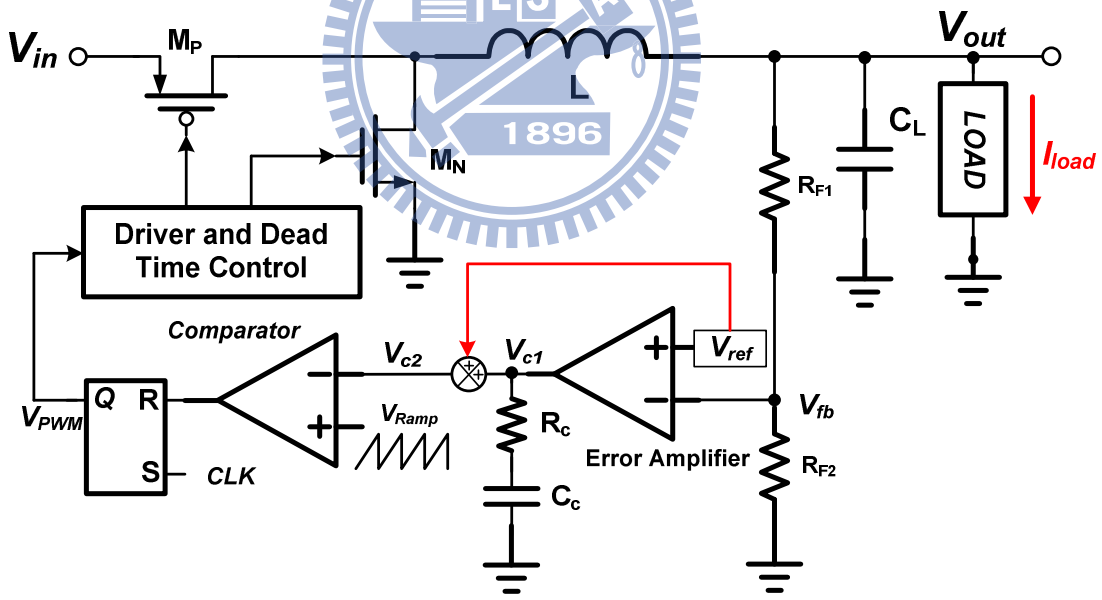

Figure 11. Voltage-mode PWM buck regulator with end-point prediction (EPP) technique

Another reference tracking technique in [18] is utilized by the hysteretic comparator and limiting current control to improve the transient response of reference tracking as shown in Figure 12.

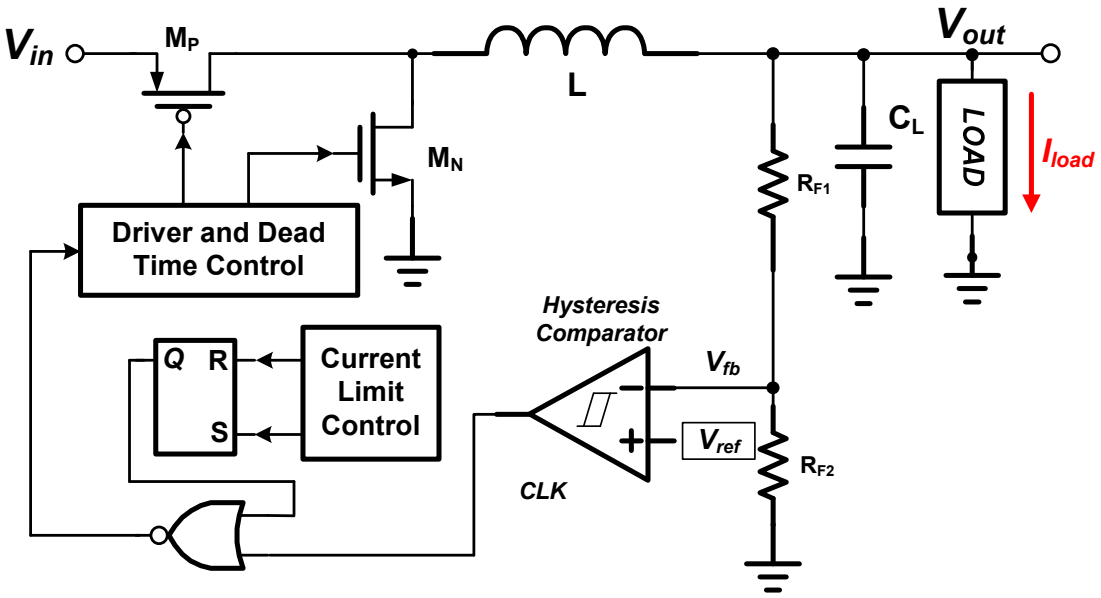

Figure 12. System architecture of hysteresis buck converter with current limit control for fast reference tracking.

The up-tracking process can be divided into the following three phases as shown in Figure 13.

1. Inductor current ramp up phase (T_1): During the period T_1, the average inductor current ramps up from the output (load) current to the maximum allowable current with full duty cycle. The Hysteresis buck converter can generate the full duty cycle. Thus, the inductor current can fast ramp up to maximum current.

2. Maximum current charging phase (T_2): During the period T_2, the inductor current switches between two predefined levels such that the average inductor current is kept at I_{max}. The maximum current is charging the output capacitor at full speed until the output voltage reaches the predefined value V_{out2}.

3. Inductor current ramp down phase (T_3): When the output voltage reaches the predefined value, the inductor current is then decreased to the new output load current. The load transient time depends on the control methodology of the converter. The total up-tracking time is T_1+ T_2+ T_3.

The down-tracking process also can be divided into the following three phases as shown in Figure 13.

1. Inductor current ramp down phase (T_4): During the period T_4, the average inductor current ramps down from the load current to the minimum current level which is close to zero. The Hysteresis buck converter would not turn on the Power MOSFET M_P. Thus, the inductor current can fast ramp down to minimum current.

2. Maximum current charging phase (T_5): During the period T_5, the output voltage is discharge by the load current and the down-tracking speed is dominated by the load resistor.

3. Inductor current ramp up phase (T_6): When the output voltage reaches the predefined value, the inductor current is then increased to the new output load current. The total down-tracking time is $T_4 + T_5 + T_6$.

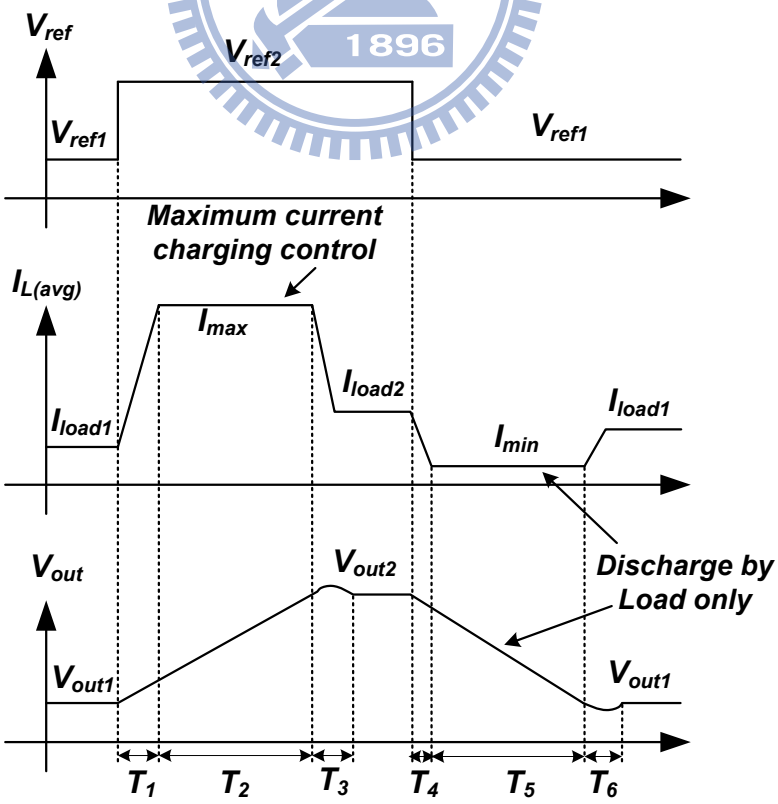

Figure 13. The up- and down- reference tracking process.

1.5 Motivation

In order to effectively reduce the chip cost and footprint area of the LED backlight module, the reference tracking process is required to turn on the RGB LED in sequential. The prior arts of reference tracking technique are well-design on the up-reference tracking response, however, the down-reference tracking are always depending on the load resistor or releasing the energy to ground. This thesis proposed the fast reference tracking (FRT) and charge recycle (CR) techniques to implement the up- and down- reference tracking with fast response and high efficiency. The FRT technique can make the LED driver drives more than 6-series R- and G-/B- LED by fast increasing or decreasing the output voltage to correct voltage level. Furthermore, the CR technique is presented to store the extra energy when the output voltage is decreased from high-supplying voltage level for 6-series G-/B- LED to low-supplying voltage level for 6-series R-LEDs. Therefore, the CR technique can quickly decrease the output voltage and the stored energy can be sent back to the output node for rapidly increasing the voltage level back to the high-supplying voltage level. Therefore, the proposed LED driver with FRT and CR techniques achieve high efficiency conversion and low cost performance compared to the conventional design. Moreover, three DC-DC converters can be decreased to only one DC-DC converter at the sacrifice of power consumption. In addition, this thesis also proposed charge recycling buck-store and boost-restore (BSBR) technique. This technique can be implemented as buck and boost converter on a single converter to store and recycle the extra energy for reducing the power dissipation on the LED driver circuit and applied on the boost converter to control the voltage.

1.6 Thesis Organization

In the following chapters, an integrated LED driver with fast reference tracking techniques including the CR and BSBR control mechanism are presented in this thesis. In

addition, the current regulator and current balance circuit are also discussed in this thesis. The Chapter 2 would describe the architecture of constant current regulator for LED Driver with the SAR-controlled adaptive off-time technique. The characteristics of LED backlight module and LCD panel are introduced in this chapter. In addition, the advantages and the disadvantages of these prior arts would be discussed in Chapter 2. In the Chapter 3, the analysis of the reference tracking procedure with FRT and CR technique is presented. The FRT technique is utilized for rapidly switching between two different output voltages and the CR technique is proposed for saving much power dissipation during the transition between two different output voltages. Furthermore, the stability and transient response of the LED driver with FRT technique is also discussed in this chapter. The circuit implementation composed of the voltage control current source (VCCS) compensator, the PWM generator, and the one-shot generator would be detailed illustrated in Chapter 3. In Chapter 4, a new charge recycling buck-store and boost-restore (BSBR) technique is proposed to reduce the power dissipation on the LED driver circuit and is applied on the boost converter to control the voltage, 9.3V for 4 series R-LED and 12.4V for G- or B- LED in the LED backlight module. The architecture of the proposed BSBR control, the BSBR tracking algorithm and the energy transforming efficiency are also discussed in detail. Experimental results shown in Chapter 5. Finally, conclusions are made in Chapter 6.

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Chapter 2

The Architecture of Constant Current Regulator for LED Driver

2.1 The Characteristic of LED

The LED I-V curve is shown in Figure 14. Because LED can be manufactured with smaller mismatch, the forward voltage variation of LED is expected. In addition, the forward voltage also varies with temperature and time. In order to get high quality image for LCD TV, it is impossible to regulate the forward voltage of LED to dimming the LED for changing the backlight brightness. In other words, the luminance is proportional to the level of driving current. The higher driving current will cause the higher brightness. As a result, by using the current to dimming the LED can prevent the variation of forward voltage and increase the brightness uniformity of LED backlight to get the high quality image of LCD TV.

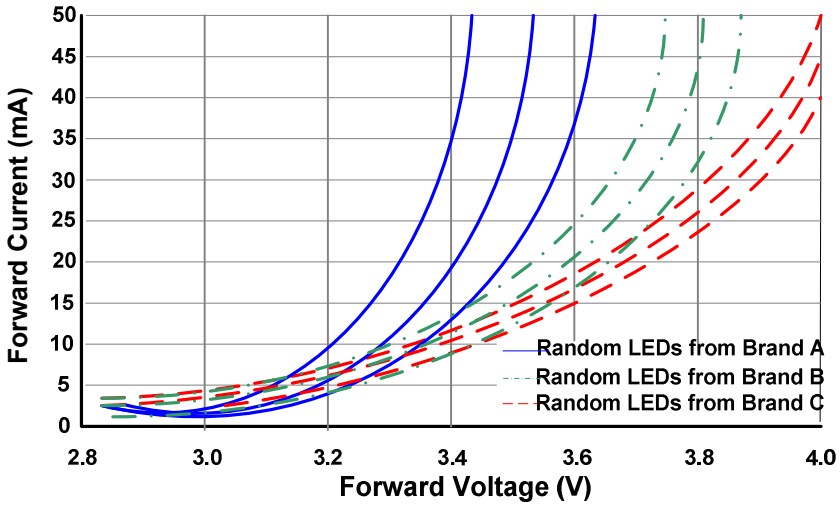


Figure 14 I-V curve characteristic of LED

2.2 The Basic LED Current Regulators

The most common method to drive LED current is shown in Figure 15. A simple current regulator is implemented for LED strings. This circuit includes operational amplifier, a reference voltage, V_{REF}, and the value of the external resistor, R_{EXT}, to determine the LED current. It is uses the constant-current source to regulate LED strings [19-20]. The constant-current source eliminates LED current changes due to variations in forward voltage. By using the constant-current source produces the constant LED brightness and strings uniformly. In Figure 15, LED can connect in a series and parallel to keep an identical current flowing in each LED, because the LED current I_{LED1}~ I_{LEDn} are produced by the value as V_{REF} /R_{EXT}. Therefore, if the external resistances are matched, this circuit can increase the current matching ability between channels.

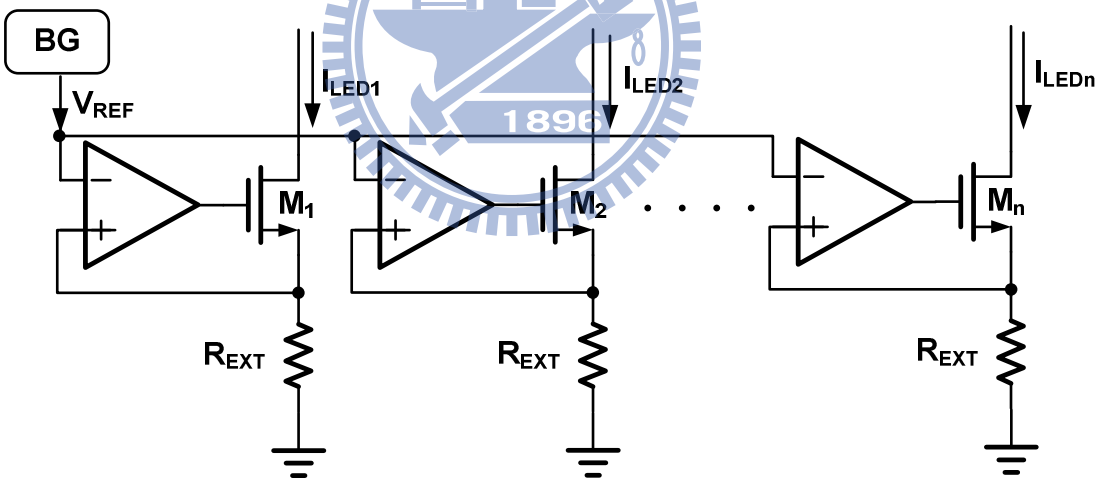


Figure 15. A simplified current regulator for LED driver.

Another important issue is LED dimming control. LED dimming control is needed in many applications. In applications as LCD backlighting, dimming provides brightness and contrast adjustment. In general, two types of dimming methods can be achieved, analog and pulse width modulation (PWM) [21]. In analog dimming, the changing of LED's forward current can change the brightness. For example, if an LED is at full brightness with 20 mA of

forward current, then 50% of the brightness is achieved by applying 50% of the maximum current to the LED. However, the drawback with analog dimming is that changes in forward current cause LED's color shift. This color shift may become unacceptable in displays requiring a true color representation. On the other hands, PWM dimming is achieved by applying full current to the LED at a modulated duty cycle. The LED brightness is controlled by adjusting the relative duty cycle. For example, 50% brightness level is achieved by turning the LED on time at full current for 50% of each period. The advantage of PWM dimming is that the forward current is always constant, so we just have to decide the maximum current for all the LED strings. Instead of analog dimming, by using this method, LED color does not vary with brightness. In order to keep the human eyes from seeing the LED turn on and off, the switching speed must be above 100 Hz. Therefore, the proposed method also includes the PWM dimming control circuit to maintain the benefits of PWM dimming. In order to eliminate the inrush current occurred at the instance of string turn on, we also proposed a delay method to reduce it. By using the delay method, the on time of all the strings will be split into several parts. In other words, turning on the strings gradually can reduce the charge current at the moment. The proposed circuit not only balances the current for LED strings but also is suitable for PWM dimming control.

2.3 The Structure of LED Lighting System with HCC and PCC Technique

There is another structure of LED driver for lighting system. The design of the LED lighting system needs the regulated driving current technique to flow through the LED for uniform brightness. The prior arts of the LED driver are the hysteretic current control (HCC) and peak current control (PCC) techniques. The PCC technique uses a constant off-time to reduce the need for the connection of the sensing resistor in series with the LEDs, sacrificing

the accuracy. The PCC technique connects the sensing resistor at the source node of the N-type power MOSFET. As a result, the PCC technique has the advantage of high efficiency but low accuracy. Therefore, how to get high efficiency and accuracy at the same time becomes an important design issue in an LED lighting system. The implementation of the conventional PCC technique is shown in Figure 16(a). It includes an oscillator to periodically turn on the N-type power MOSFET M_N. When the inductor current is increased to the predefined peak current level, the N-type power MOSFET M_N will be turned off. As a result, the inductor current is discharged by the freewheel-diode. The inductor current also flows through the LEDs; thus, the average inductor current will determine the brightness of the LEDs. Considering the inductor current waveform in the steady state as shown in Figure 16(b), the inductor current ripple ΔI_L can be expressed as (5).

$$\Delta I_L = \frac{V_{IN} - V_o}{L} t_{on} = \frac{V_o + V_D}{L} t_{off} \quad \text{where } V_o \approx nV_F \tag{5}$$

V_F and V_D are the forward voltages of the LED and the freewheel-diode, respectively. The V_o is equal to the summation of the total forward voltage of LED in series. The t_{on} and t_{off} are the on-time and off-time of the N-type power MOSFET M_N, respectively. Owing to the constant switching frequency, t_{on} and t_{off} can be approximately described as (6) and (7), respectively. The forward voltage of freewheel-diode is ignored in (6).

$$t_{on} = DT_s = \frac{V_o}{V_{IN}} T_s \tag{6}$$

$$t_{off} = (1 - D)T_s = \left(1 - \frac{V_o}{V_{IN}}\right) T_s \tag{7}$$

T_s and D are defined as the switching period and the duty cycle of the LED driver,

respectively [22]. Since the bottom current level is determined by the switching frequency, the average inductor current $I_{L(avg.)}$ can be calculated as (8).

$$I_{L(avg)} = I_{peak} - \frac{V_o}{2L} t_{OFF} = I_{peak} - \frac{V_o T_s}{2L}\left(1 - \frac{V_o}{V_{IN}}\right) \tag{8}$$

The value of the input voltage V_{IN} will affect the average inductor current. Moreover, the different numbers of LED in series which cause the different output voltage ($V_o \approx nV_F$) influence the average inductor current. Hence, the brightness of the LED is drastically influenced by the variation of the input voltage. Furthermore, as shown in Figure 16(a), the major power dissipation of the LED driver in the PCC technique is caused by the external sensing resistor R_s and the diode during phases I and II, respectively. In phase I, the inductor current passes through the external sensing resistor R_s and the equivalent resistance of the M_N (R_{on}) results in the energy consumption calculated as (9).

$$E_{phI(PCC)} = I_{L(avg)}{}^2 \times (R_{on} + R_s) \times t_{on} \tag{9}$$

Moreover, the inductor current flows through the freewheel-diode to decrease the inductor current during phase II. Therefore, the freewheel-diode also brings the energy dissipation described as (10).

$$E_{phII(PCC)} = I_{L(avg)} \times V_D \times t_{off} \tag{10}$$

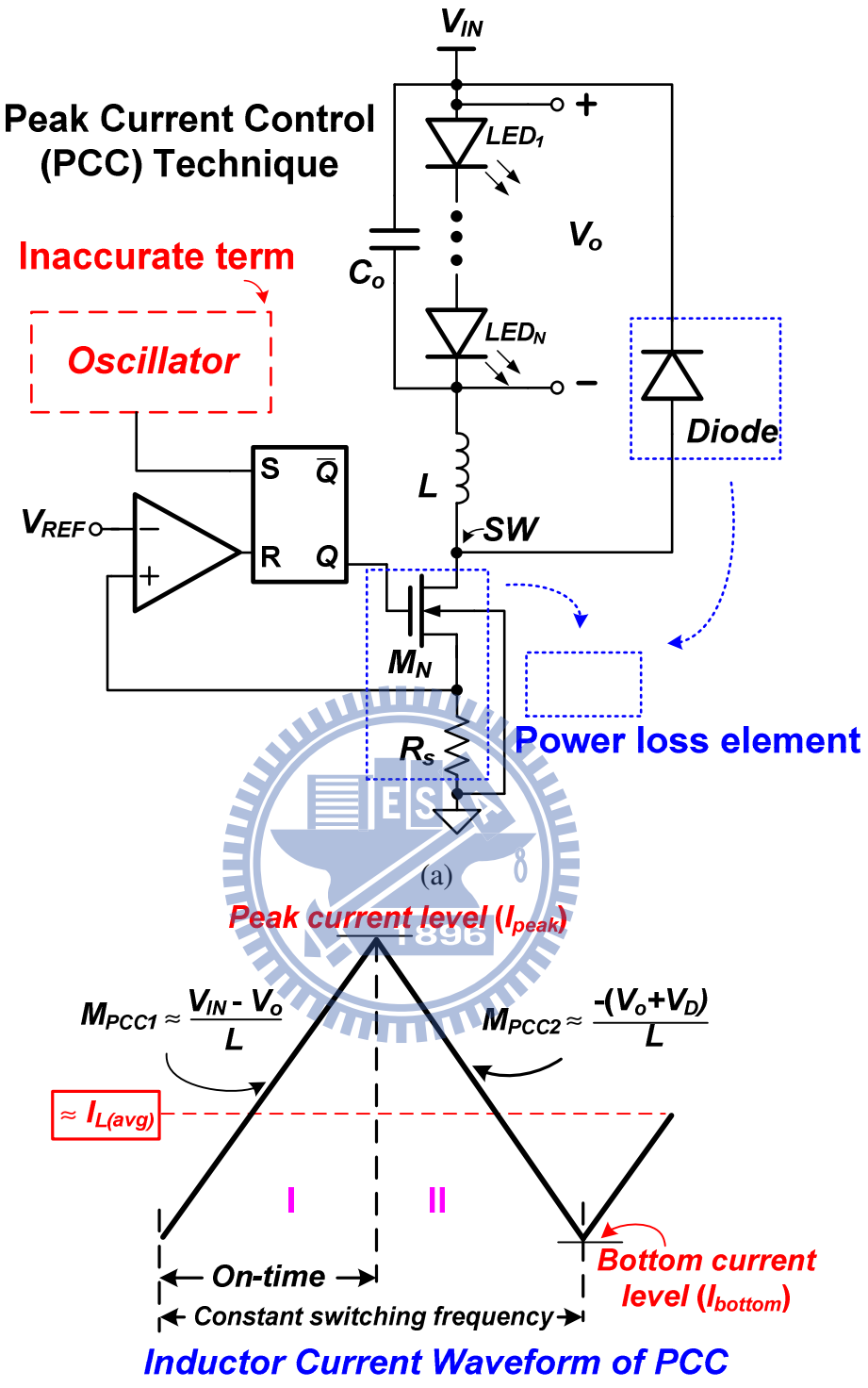


Figure 16. The prior art for LED lighting system. (a) The implementation of the LED driver with the PCC technique. (b) The inductor current waveform of the PCC technique.

The HCC technique utilizes two threshold current levels to accurately control the average inductor current $I_{L(avg)}$, thereby defining the switching frequency [22]. The

implementation of the fundamental HCC technique is shown in Figure 17(a). It includes the simplest implementation of the current sensing circuit composed of an external resistor, R_S. The inductor current waveform in the steady-state is shown in Figure 17(b). The two threshold current levels are defined as I_{Hth} and I_{Lth} indicating the high and low threshold current levels, respectively. When the switch M_S and the N-type power MOSFET M_N are turned on, the inductor current increases at a rate determined by $(V_{IN} - V_o)/L$. Thus, the current sensing circuit generates the sensing current via R_1 and the switch M_S to produce the ramp voltage V_s. When the voltage V_s is higher than the V_{REF}, the switch M_S and the N-type power MOSFET M_N are turned off by the output of the comparator. Therefore, V_s has a step variation since the sensing current passes through both the resistors R_1 and R_2, not only through R_1. In addition, the inductor current is discharged via the freewheel-diode back to V_{IN}, as such, V_s decays at a rate decided by the inductor current. The current ripple can be defined as (11):

$$\Delta I_L = I_{Hth} \times \frac{R_2}{R_1 + R_2} = I_{Lth} \times \frac{R_2}{R_1} \tag{11}$$

The HCC technique can accurately design the low threshold current I_{Lth} and the inductor current ripple by defining the high threshold current I_{Hth} and utilize the suitable resistors R_1 and R_2. Hence, the average inductor current can be accurately described as (12).

$$I_{L(avg)} = \frac{I_{Hth} + I_{Lth}}{2} \tag{12}$$

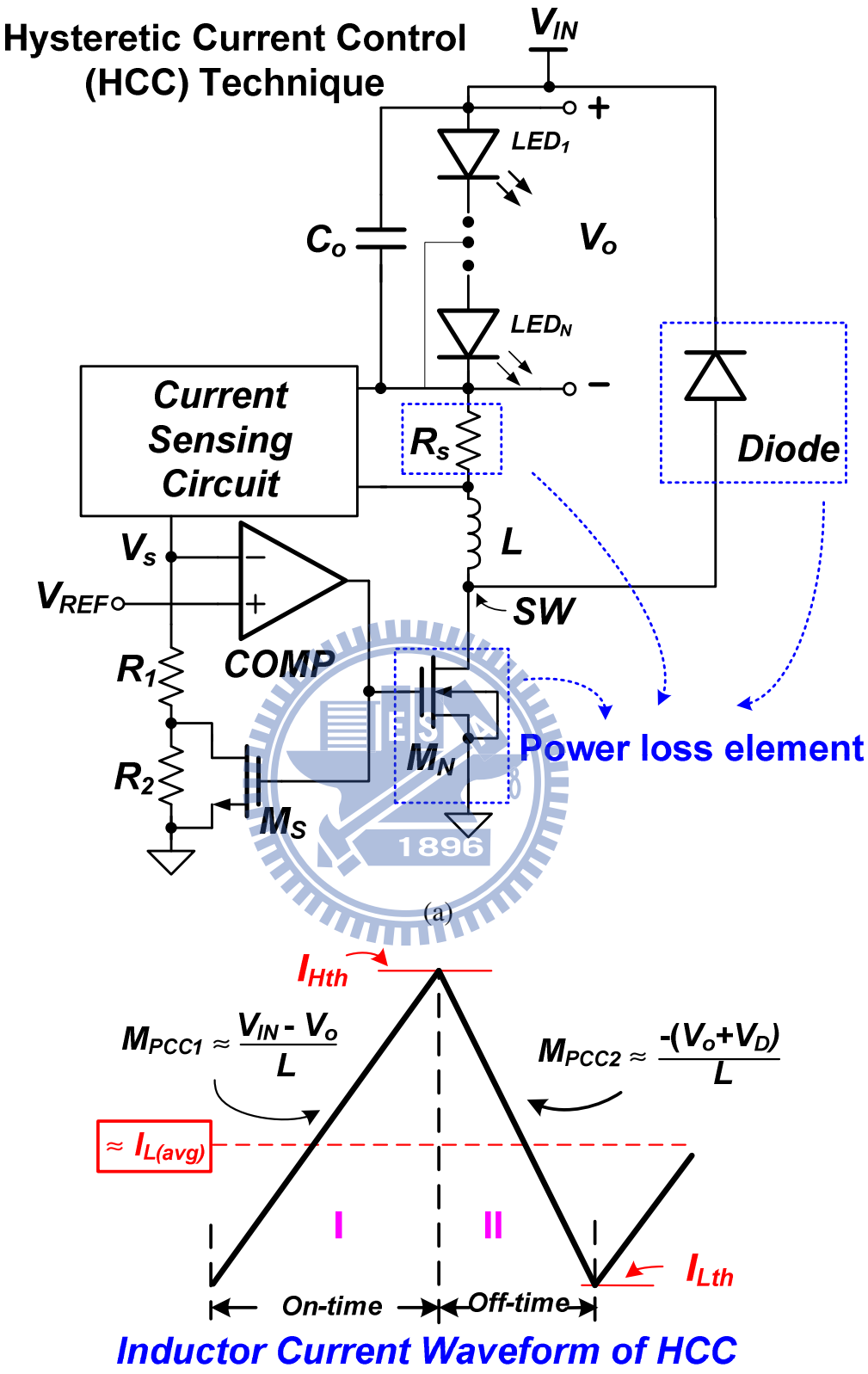
As a result, the HCC technique can achieve a more accurate average current than that of the PCC technique. Hence, the brightness of the LED can be effectively controlled by the HCC technique. However, the large inductor current flows through the sensing resistor R_s in the full period since the whole switching period needs the information of the inductor current

to compare it with the two threshold current levels. Thus, the energy dissipation by the conduction loss in phase I and phase II can be expressed as (13) and (14), respectively

$$E_{phI(HCC)} = I_{L(avg)}{}^2 \times (R_{on} + R_s) \times t_{on} \tag{13}$$

$$E_{phII(HCC)} = (I_{L(avg)} \times V_D + I_{L(avg)}{}^2 \times R_s) \times t_{off} \tag{14}$$

According to (9) and (10), the power consumption depends on the sensing resistor R_s and the forward voltage of freewheel-diode V_D because the R_s is much larger than R_{on}. However, comparing (10) and (14), the power efficiency of the PCC technique is generally higher than the HCC technique because the inductor current passes through the sensing resistor during phase I instead of the full period. Thus, the conduction loss of the HCC technique is larger than that of the PCC technique. There is a trade-off between accuracy and efficiency in the design of the LED driver. The HCC technique can have more accurate average current but larger conduction loss. On the other hand, the PCC technique can achieve higher efficiency at the expense of accuracy. To achieve higher accuracy and efficiency at the same time, the current regulator with the SAR-controlled adaptive off-time technique is proposed.



(b)

Figure 17. The prior art for LED lighting system. (a) The implementation of the LED driver with the HCC technique. (b) The inductor current waveform of the HCC technique.

2.4 The Successive Approximation Register (SAR) Design Methodology

The conduction loss of phase I due to the sensing resistor [7], [21] can be reduced by means of the on-chip low-side current sensing circuit that can accurately define the peak current level [23]. Additionally, the removal of the external sensing resistor can also save the cost and footprint area, but this causes an inability to sense inductor current during phase II [16]. Thereby, the average inductor current is difficult to accurately control because the bottom level of inductor current depend on the constant off-time or fixed frequency. Therefore, the accuracy of the LED lighting system is deteriorated. The value of the off-time needs to be adaptively adjusted to ensure the accurate inductor current that can be controlled between the peak and bottom current levels. As a result, the average inductor current can be independent of the variation of the input voltage and the numbers of LED in series. To adaptively adjust the value of the off-time [24], it is proposed that the SAR-controlled adaptive off-time calibrate the off-time value. That is, the duration of the off-time can be adjusted to regulate the bottom current level.

The flow chart of the SAR-controlled adaptive off-time technique is shown in Figure 18. The 8-bit SAR code A[7:0] is used to decide the duration of the off-time. At the beginning, the SAR code A[7:0] has an initial value of “1000,0000” and the gain code G[7:0] is set to “0100,0000”. Adding or subtracting the gain code G[7:0] leads to the accurate calibration values of the SAR code A[7:0] in the following eight switching cycles. When the duration of the off-time is too short, the current sensing signal V_{sense} at the beginning of the next switching cycle is larger than the expected value of VREF2 as shown in Figure 19. Thus, the average inductor current is larger than expected value to have an influence on the brightness of the LED. At this time, the gain codes G[7:0] would be added to the SAR code A[7:0] to

prolong the off-time. On the other hand, if the off-time is too long, the current sensing signal, Vsense, at the beginning of the next switching cycle will be smaller than the V_{REF2}. That is, the lumen of LED is relatively small due to the smaller average inductor current, and therefore, the SAR code A[7:0] will subtract the gain code G[7:0].

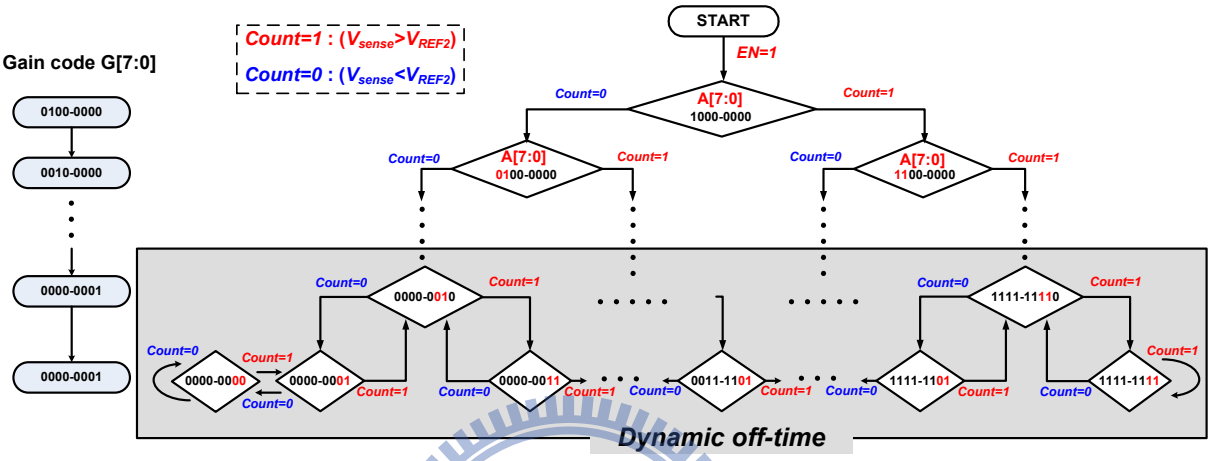


Figure 18. The inductor current waveform at different the off-time values.

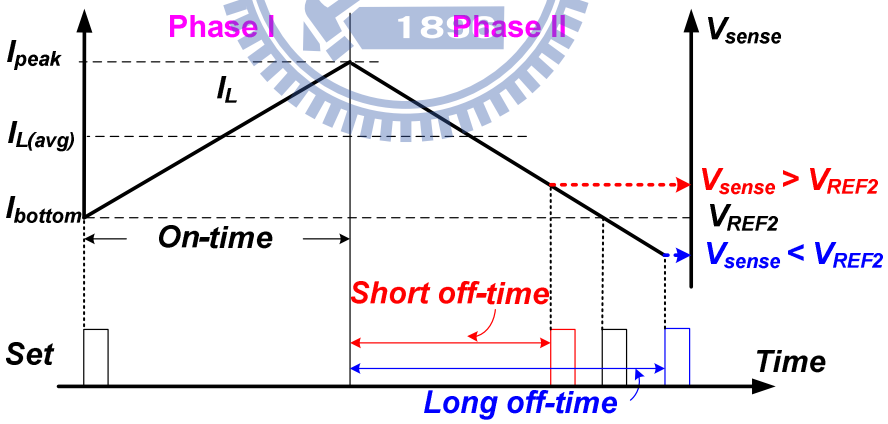


Figure 19. The inductor current waveform at different the off-time values.

After the eight switching cycles, the SAR code A[7:0] can be dynamically adjusted by a minimum value of the gain code G[7:0], which is “0000,0001” according to the value of the comparison result of the voltage V_{sense} and the reference voltage V_{REF2}. Consequently, after the calibration duration, the adaptive off-time can ensure that the bottom level of the inductor

current will be close to the expected value. That is, the average inductor current can be independent of the variation of the input voltage.

The external sensing resistor is not needed any more since the on-chip low-side current sensing circuit can detect the peak current level and the SAR code A[7:0] adaptively adjusts the off-time. Therefore, the efficiency can be improved owing to the removal of the conduction loss of the external sensing resistor. Simultaneously, the accuracy is also guaranteed because the adaptive off-time can ensure the average inductor is independent of the variation of the input voltage. In other words, the SAR-controlled adaptive off-time has the advantages of high efficiency like the PCC technique and high accuracy like the HCC technique.

2.5 The Successive Approximation Register (SAR) Circuit Implementations

The implementation of the SAR-controlled adaptive off-time technique is illustrated in Figure 20. The external sensing resistor is replaced by the on-chip low-side current sensing circuit. As a result, the power dissipation of the on-chip low-side current sensing circuit is much smaller than that of the external sensing resistor. Furthermore, the freewheel-diode [25] is substituted by the active diode, which is the P-type power MOSFET M_{Diode}, in order to reduce the power dissipation during phase II. The digital signals *EN* and *CLR* are used to enable the LED driver and reset the initial digital code. The digital signal, *Digital PWM*, is the dimming signal for adjusting the brightness of the LED.

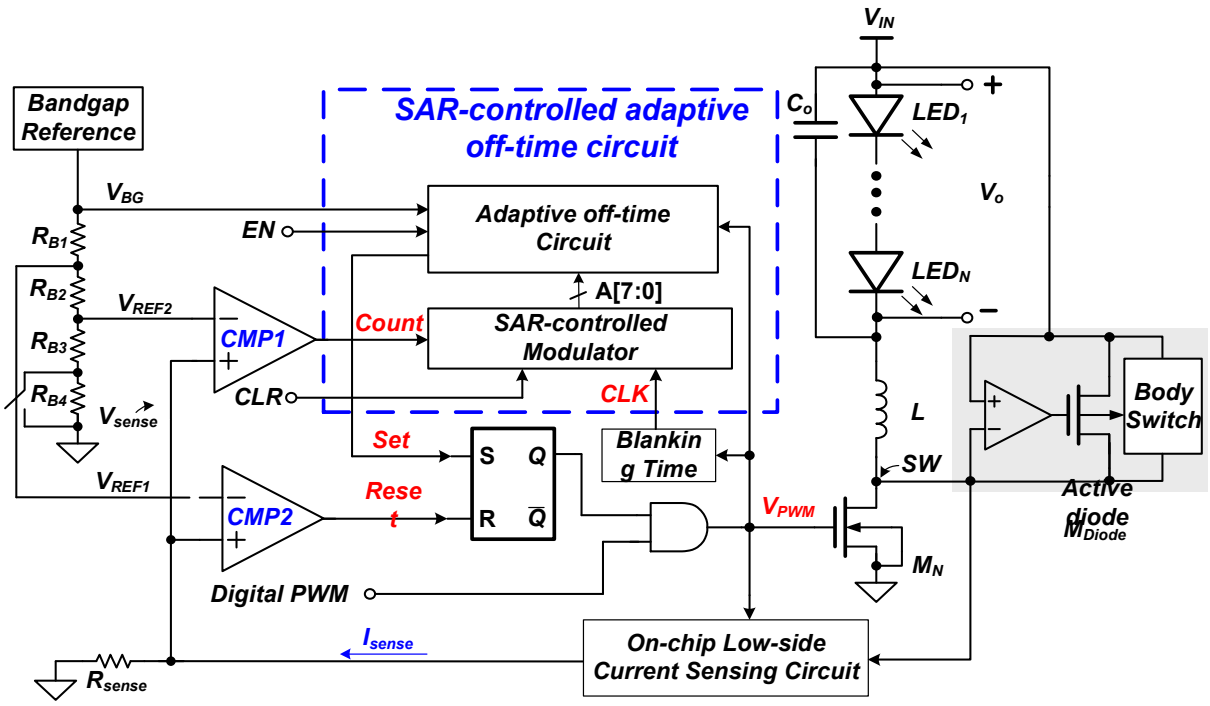


Figure 20. The proposed LED current driver uses the SAR-controlled adaptive off-time technique.

Two major circuits are used to enhance the accuracy of the LED driver. One is the SAR-controlled adaptive off-time control circuit and the other one is the on-chip low-side sensing circuit with the blanking time circuit. During phase I, the N-type power MOSFET is turned on to increase the inductor current. The current sensing circuit thus increases the sensing voltage V_{sense}. Once V_{sense} is larger than V_{REF1}, the output of the comparator '*CMP2*' triggers the signal *Reset* to turn off the N-type power MOSFET M_N. The on-time duration t_{on} is decided. The peak level of inductor current can be expressed as:

$$I_{peak} = \frac{K \times V_{REF1}}{R_{sense}} \tag{15}$$

K refers to the sensing ratio. At this particular time, the active diode M_{Diode} will be turned on to discharge the inductor current. The forward voltage of the active diode is the source-drain voltage V_{SD} of P-type power MOSFET. The off-time duration t_{off} is controlled by the 8-bit

SAR code A[7:0] from the SAR-controlled modulator. After the off-time duration, the adaptive off-time module sends a signal *Set* to turn on the N-type power MOSFET to charge the inductor current again.

At the beginning, the SAR-controlled adaptive off-time technique calibrates the off-time duration depending on the output '*Count*' of the comparator 'CMP1'. The signal '*Count*' equaled to '1' or '0' means that the sensing current signal V_{sense} is higher or lower than the reference voltage V_{ref2}. After the calibration process, the bottom level of inductor current can be determined by the voltage V_{REF2}. Thus, the bottom level of the inductor current can be formulated as:

$$I_{bottom} = \frac{K \times V_{REF2}}{R_{sense}} \tag{16}$$

Therefore, the current ripple divided by the average current can be calculated as:

$$\frac{I_{ripple}}{I_{avg}} = \frac{2 \times (V_{REF1} - V_{REF2})}{(V_{REF1} + V_{REF2})} \tag{17}$$

As a result, the current ripple ratio can be maintained by the reference voltages V_{ref1} and V_{ref2} and would not be influenced by the input voltage or the numbers of LED in series. Smaller current ripple has a more stable LED lumen. However, the ratio of the current ripple also defines the switching frequency as:

$$f_s = \frac{1}{L \times I_{ripple} \times (\frac{1}{V_o} + \frac{1}{V_{IN} - V_o})} \tag{18}$$

According to (18), a small inductor current ripple results in a faster switching frequency and increases power consumption. On the other hand, a high inductor current ripple results in

a slower switching frequency Therefore, power efficiency is increased because the switching loss is further reduced. However, the conduction power is increased due to large current ripple. Therefore, the inductor current ripple, which is about ±15% of the average inductor current has a better power conversion efficiency as shown in Figure 21. The power efficiency would be reduced while the current ripple is smaller than ±15%. Moreover, the current ripple can be increased to reduce the size of the inductor at the cost of reduced efficiency and, possibly, LED lifetime [26]. As a result, the suitable ratio of the inductor current ripple is ±15%. This is popularly used in today's LED lighting products.

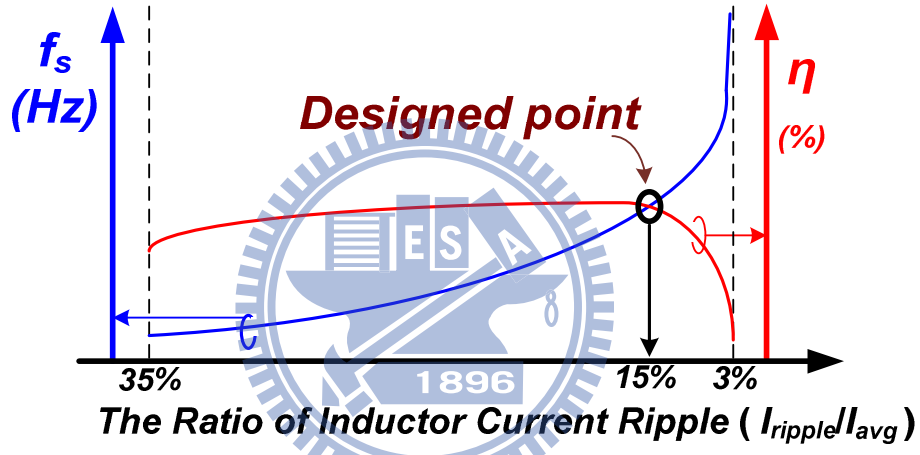


Figure 21. The relation of the ratio of inductor current ripple (I_{ripple} / I_{avg}), the power efficiency (η), and the switching frequency (f_s).

The LED driver needs to provide an accurate driving current for LED lighting systems. It should be noted that the SAR-controlled modulator can still dynamically adjust the off-time to rapidly react to the variations of the input voltage and the numbers of LED in series. In addition, the power dissipation during phases I and II can be reduced and expressed as (19) and (20), respectively.

$$E_{phI(SAR)} = I_{L(avg)}{}^2 \times R_{on} \times t_{on} \tag{19}$$

$$E_{phII(SAR)} = I_{L(avg)} \times V_{SD} \times t_{off} \tag{20}$$

According to (15), the power dissipation in phase I is much less than those in (9) and (13). During phase II, the power dissipation can also be reduced through the use of small V_{DS} because of the active diode. Hence, the technique can minimize the conduction power loss and improve the accuracy of the driving current. The following subsections will describe the implementations of the sub-modules.

2.5.1 The Implementation of the SAR-Controlled Modulator

The implementation of the SAR-controlled modulator is composed of three sub-modules as shown in Figure 22. The three sub-modules are the up-down 8-bit counter, the 8-bit SAR gain code generator, and the over-control logic circuit. The up-down 8-bit counter is used to calculate a new 8-bit SAR code A[7:0] and a gain code G[7:0] according to the digital signal *Count*. The 8-bit SAR gain code generator provides G[7:0] to the up-down 8-bit counter to calculate the precise A[7:0]. The over-control logic circuit detects A[7:0] and generates C[7:0] to avoid the overflow issue.

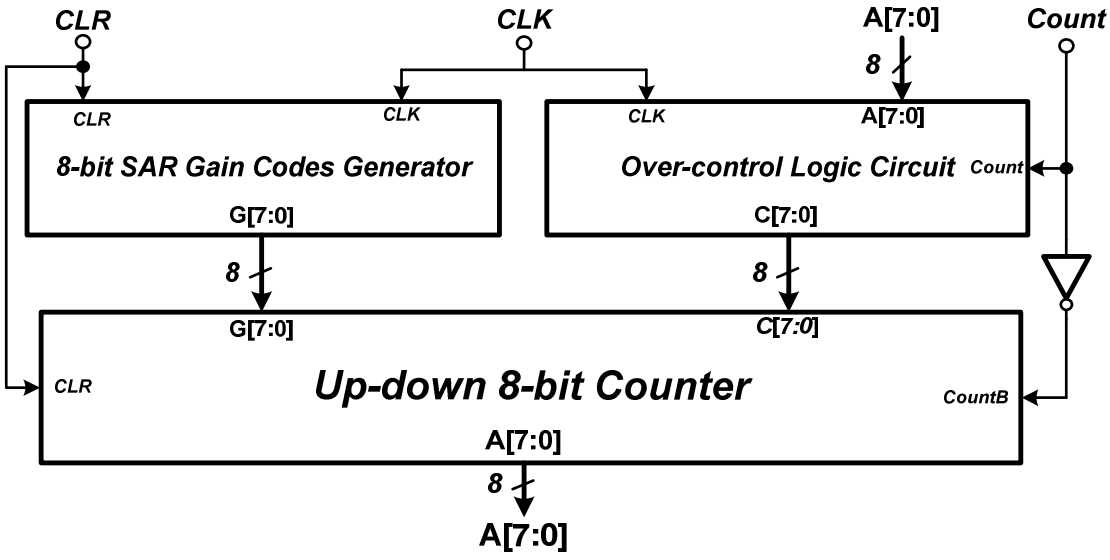


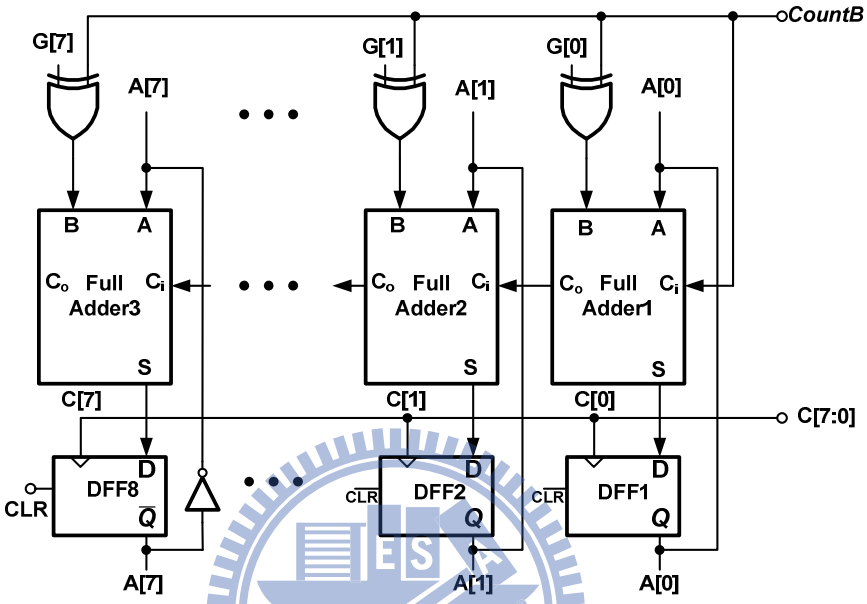
Figure 22. The structure of the SAR-controlled modulator.

The circuit of the up-down 8-bit counter is the main module shown in Figure 23(a). Since A[7:0] starts from '10000000', the gate DFF8 utilizes the complement of the *Q* signal when the signal *CLR* is high. Therefore, A[7:0] starts from '10000000' after the clear state. The eight XOR gates and the signal *CountB* are used to decide if the operation is an addition or a subtraction. Additionally, *CountB* is also used as the carry-in signal of the first full-adder to achieve the correct calculation. When *CountB* is '1', G[7:0] will be converted into its 2's complement value. Hence, A[7:0] subtracts G[7:0] to prolong the off-time duration. On other hand, if *CountB* is '0', G[7:0] is not complemented. That is, the addition is proceeded by the SAR-controlled modulator and A[7:0] is equal to the sum of the previous value and G[7:0].

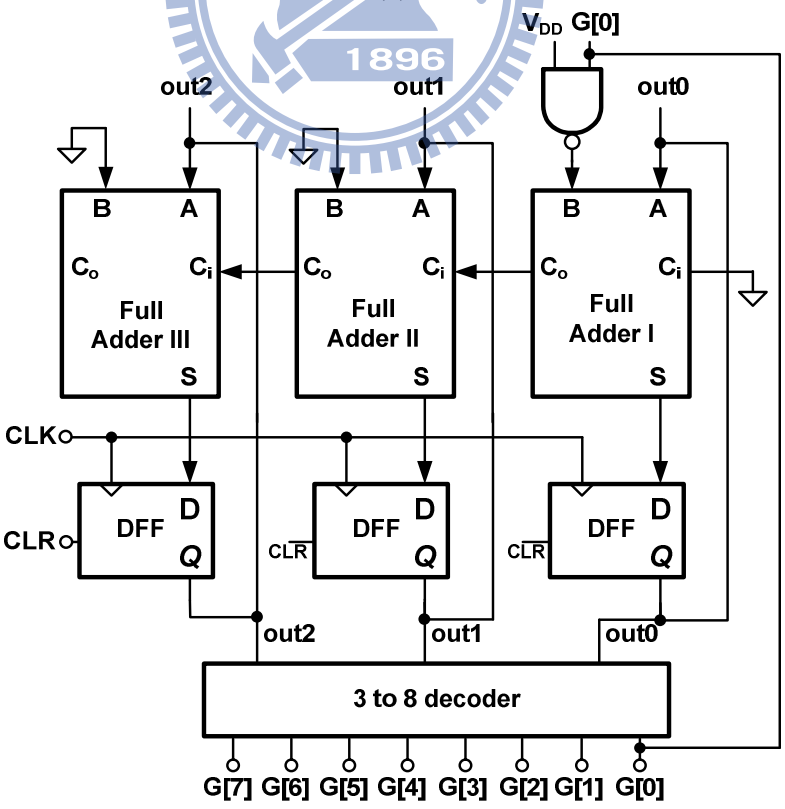
The 8-bit gain code generator is shown in Figure 23(b). G[7:0] starts from '01000000' to '00000001'. At the beginning, the binary code [out2, out1, out0] is set to '000' and converted by the 3-to-8 decoder so that G[7:0] can be set as '01000000.' Three full adders are used to generate the increasing binary code [out2, out1, out0] from '000' and G[7:0] is converted from '01000000' to '00000001' by the 3-to-8 decoder. Until G[0] is changed from '0' to '1', the input B of the full adder I becomes '0' and the binary code [out2, out1, out0] will be settled. This indicates the end point of the calibration of the SAR operation. Then, the SAR-controlled modulator starts to slightly adjust A[7:0] by setting the minimum G[7:0] as '00000001.'

The over-control logic circuit is depicted in Figure 23(c). The AND gate array is used to block the clock *CLK* when the overflow issue happens. When the value of the signal *CountB* is '1', the operation of the up-down 8-bit counter is the addition function. If A[*7:0*] is '11111111,' the output of the XOR gate array is '0' to block the clock signal *CLK*. Thus the over-control signal C[7:0] holds to '00000000.' For the subtraction function, the up-down 8-bit counter needs to prevent the value of the SAR code A[7:0] from continuously decreasing when A[7:0] is '00000000.' When the function of subtraction is enabled by the *CountB*, it

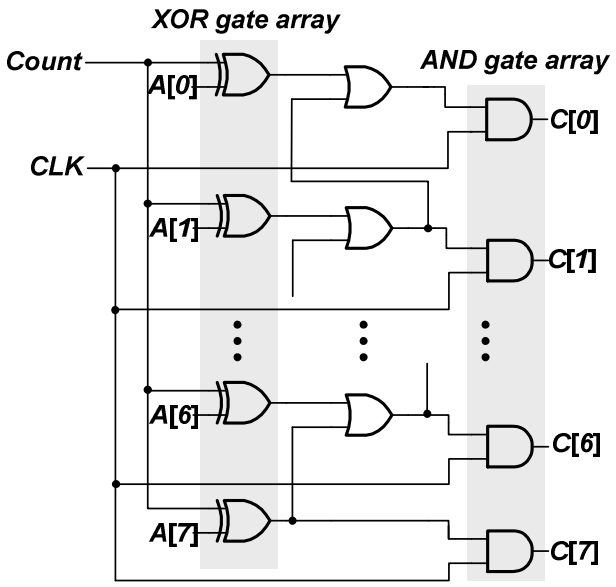
also prevents the overflow issue from happening through the XOR gate array. The SAR-controlled modulator with three sub-modules can generate A[7:0] through the digital signal *Count* to adjust the dynamic off-time. When *Count* is '0' or '1', the SAR code will subtract or add G[7:0] as '00000001.'



(a)



(b)



(c)

Figure 23. The three sub-modules in the implementation of the SAR-controlled modulator. (a) The up-down 8-bit counter. (b) The 8-bit SAR gain code generator. (c) The over-control logic circuit.

2.5.2 The Implementation of the Adaptive Off-time Circuit

The simple implementation of the constant off-time circuit is depicted in Figure 24(a). When the signal *control* is high, the non-inverting input of comparator V_{ca} is discharged to ground and the output of comparator *Set* is zero. When the signal *control* is changed to low, the constant biasing current I_B will flow into the capacitor C_{off} to increase V_{ca}. Once V_{ca} is larger than the voltage V_{BG}, the signal *Set* is changed to high to start the next switching cycle. Thus, the off-time duration can be expressed as (21).

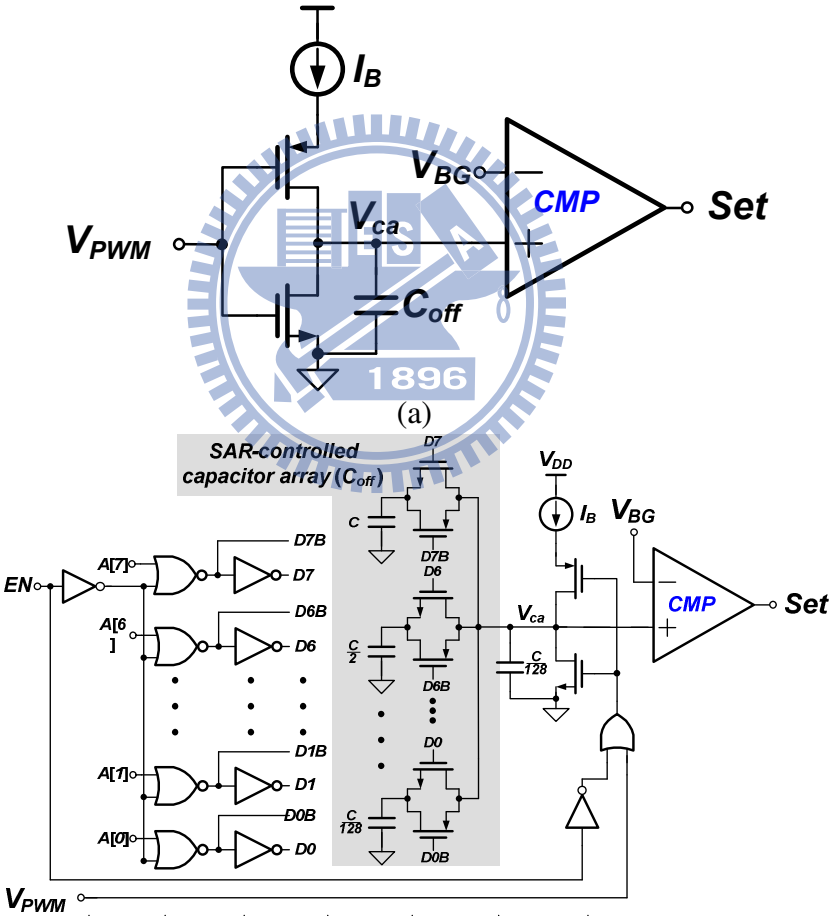
$$t_{off} = \frac{C_{off} V_{BG}}{I_B} \tag{21}$$

where t_{off} is proportional to the value of the capacitor C_{off}. Therefore, the adaptive off-time circuit as illustrated in Figure 24(b) utilizes the SAR codes to adjust the value of the capacitor

for the suitable off-time t_{off}. A[7:0] turns on/off the switches in the SAR-controlled capacitor array to decide the total value of C_{off} when the input enable signal *EN* is high. Each bit in A[7:0] indicates the additional capacitor. As such, C_{off} can be expressed as (22):

$$C_{off} = C \times (2^{0} \cdot A_7 + 2^{-1} \cdot A_6 + ... + 2^{-7} \cdot A_0 + 2^{-7}) \tag{22}$$

Thus, the maximum and minimum values of the capacitor are *2C* and *C/128*, respectively. As a result, the off-time t_{off} can be dynamically adjusted to get the accurate average inductor current.



A[7]	A[6]	A5]	A[4]	A[3]	A[2]	A[1]	A[0]
C	C/2	C/4	C/8	C/16	C/32	C/64	C/128

(b)

Figure 24. (a) The implementation of a simple off-time circuit (b) The schematic of the adaptive off-time circuit and the corresponding capacitor according to each bit of the SAR code A[7:0].

2.5.3 The Implementation of the On-chip Low-side Current Sensing and the Blanking Time Circuits

The on-chip low-side current sensing circuit is shown in Figure 25. The switches M_{s1}-M_{s3} are used to control the turning on/off the current sensing mechanism. When the V_{PWM} changes to high to turn on the N-type power MOSFET M_N, the sensing MOSFET M_{sense}, and the switch M_{s1}, the voltage at node *SW* will pass to V_B through the M_{s1} and voltage V_A will be equal to the voltage at node *SW* due to the close-loop of the amplifier. Thus, the transistors M_N and M_{sense} will have the same drain, gate, source, and bulk voltages. The *W/L* ratio of M_N to M_{sense} is about K. In this design, the value of K is 3000. The current I_s is approximately equal to (1/3000)×I_L. The inductor current information passes through the current mirror pair, composed of transistors M_{R1} and M_{R2}, to generate the sensing signal V_{sense}, which is used to compare two reference voltages, V_{REF1} and V_{REF2}, to decide the values of t_{on} and t_{off}.

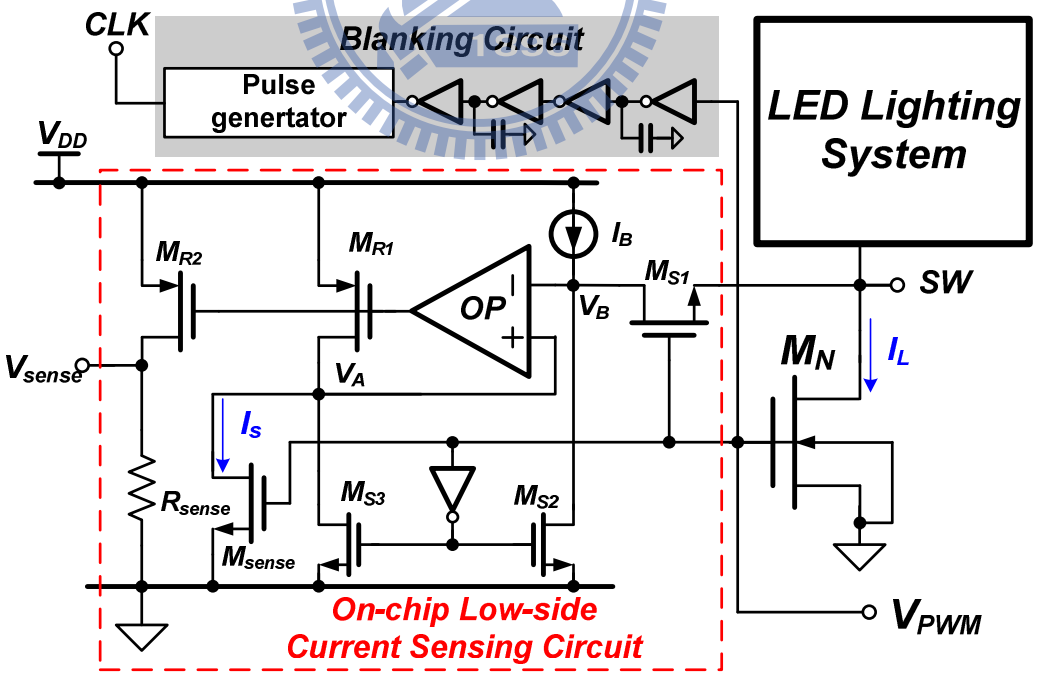


Figure 25. The design of the on-chip low-side current sensing circuit with the blanking time circuit.

At the beginning of every switching cycle, the current sensing signal V_{sense} is utilized to

determine whether the digital *Count* is '1' or '0'. Since the clock signal *CLK* in the SAR-controlled modulator can trigger the calibration of the off-time duration, V_{sense} needs to correctly present the inductor current information before the clock signal *CLK* changes from low to high. Thus, the blanking time circuit is used to delay the signal V_{PWM} to generate the clock signal *CLK*. That is, the blanking time circuit provides enough time for V_{sense} to track the variation of the load current. Therefore, A[7:0] can accurately decide the value of the capacitor.

Chapter 3

The Proposed FRT Technique and CR Technique

3.1 The Analysis of FRT Technique and CR Technique

The LED driver for modified FCS algorithm needs two characteristics to meet the requirements of the LCD response time. One is the fast reference voltage tracking [17], [27] for rapidly switching output voltage to meet the requirement of three colors LED and the other one is the charge-recycling [28-29] for reducing power consumption. The schematic of the proposed RGB driver is shown in Figure 26. The main blocks contain the PWM generator with FRT technique, the CR circuit, the CB circuit, and the timing controller implemented by FPGA.

3.1.1 The Operation Principle of the FRT Technique

The function blocks of PWM generator with FRT technique is shown in Figure 27 (a). The correction current I_c generated by the G_m amplifier represents the output voltage condition of the LED driver. Owing to the usage of the G_m amplifier, the characteristic of high bandwidth can result in fast load/line transient response and reference tracking. However, the static error is worse since the characteristic of low gain of the G_m amplifier. Therefore, the FRT technique utilizes the feedforward current I_{feed} to minimize the effect of I_c for improving

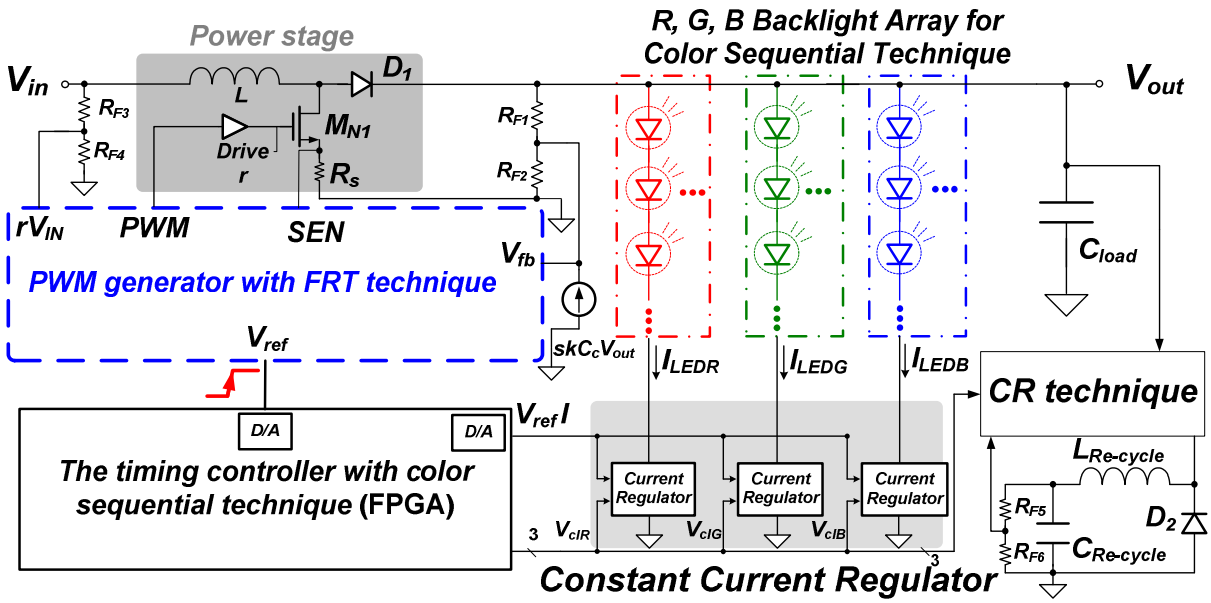


Figure 26. The proposed LED driver contains the FRT, CR techniques, and the current balance (CB) circuit.

the static performance. Furthermore, the feedforward current I_{feed} standing for the input voltage information also can improve line transient performance. The output of the saw-tooth generator is a saw-tooth waveform I_a with a high threshold current I_H defined as $V_{ref} \times G_m$ and a low threshold current defined as "0". Therefore, the saw-tooth signal with reference voltage information can rapidly determine the value of the duty cycle, thereby regulating the output voltage to quickly track the variations of the reference voltage V_{ref}.

The duty cycle of a voltage-mode LED driver operated in continuous current mode (CCM) is defined as (23) and depicted in Figure 27 (b). At steady state, the correction current I_c can be neglected because the feedforward current I_{feed} is used to minimize the value of correction current I_c. The static performance can be improved since the duty cycle of LED driver with FRT technique can be simplified as (24).

$$D = \frac{V_o - V_{in}}{V_0} = \frac{I_H - (I_{feed} - I_c)}{I_H} \tag{23}$$

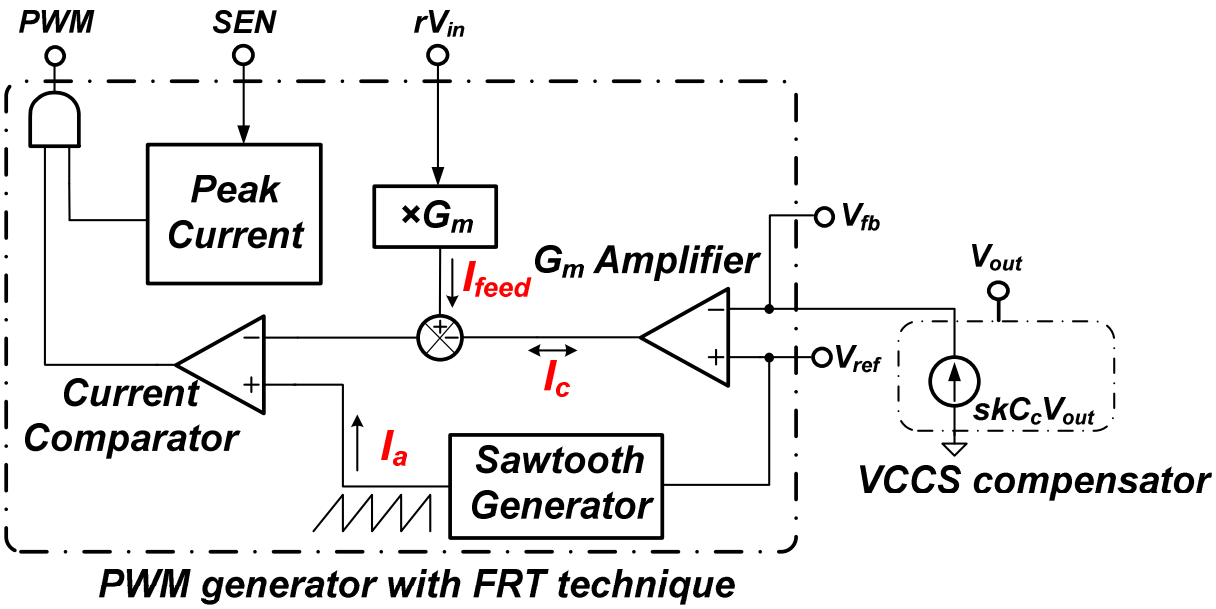
$$D \approx \frac{V_{ref} \times G_m - I_{feed}}{V_{ref} \times G_m}, \text{ where } I_H = V_{ref} \times G_m \tag{24}$$

When the LED driver is well-designed, the feedback voltage V_{fb} is equal to the reference voltage V_{ref} as shown in (25). According to (24) and (25), the expression of the duty cycle is rewritten as (26). It is obvious that the transient response of line/load can effectively improved due to the appearance of the input and output information in (26). Therefore, the FRT technique not only has fast line/load transient response with a minimized static error but also has fast reference tracking since the variation of I_H is proportional to the variation of the reference voltage.

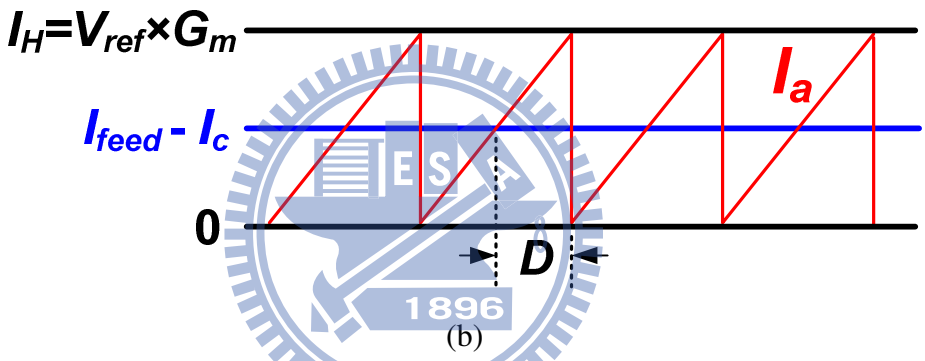
$$V_{ref} = V_{fb} = \frac{R_{F2}}{R_{F1} + R_{F2}} V_o = rV_o \quad \text{where } r = \frac{R_{F2}}{R_{F1} + R_{F2}} \tag{25}$$

$$D = \frac{V_o - V_{in}}{V_o} = \frac{rV_o \times G_m - I_{feed}}{rV_o \times G_m} \quad \text{where } I_{feed} = rV_{in} \times G_m \tag{26}$$

When output voltage is changed from low- to high-supplying voltage level, the output voltage can quickly increase by peak current level owing to the high bandwidth of G_m amplifier and FRT technique. However, when output voltage is changed from high- to low-supplying voltage level, the duty cycle of PWM generator can be decreased by fast response of G_m amplifier and FRT technique. Nevertheless, the drop of output voltage still depends on the load current and output capacitor. If the value of the load current is small [30], the recovery time of the regulated output voltage is prolonged. There is not any high efficiency method proposed to solve this problem [18]. Thus, the CR technique is presented to speed up the recovery time, thereby enhancing the power conversion efficiency due to the energy recycling.



(a)



(b)

Figure 27. (a) The PWM generator with FRT technique. (b) The determination of duty waveform in the PWM generator with FRT technique.

3.1.2 The Operation Principle of the CR Technique

The low-supplying voltage level can be quickly raised to the high-supplying voltage level by the proposed FRT technique. However, the pulling down response time of the output voltage from high- to low-supplying voltage level depends on the values of the output capacitor and load current. The CR technique stores the extra charge from the output capacitor C_{load} to the re-cycling capacitor $C_{Re\text{-}cycle}$ and thus rapidly pulls down the output voltage to the low-supplying voltage level for driving R-LEDs. Hence, the LED diver can maintain high

efficiency due to the minimized power consumption on the current balance circuits. The implementation of the CR technique is conceptually illustrated in Figure 28.

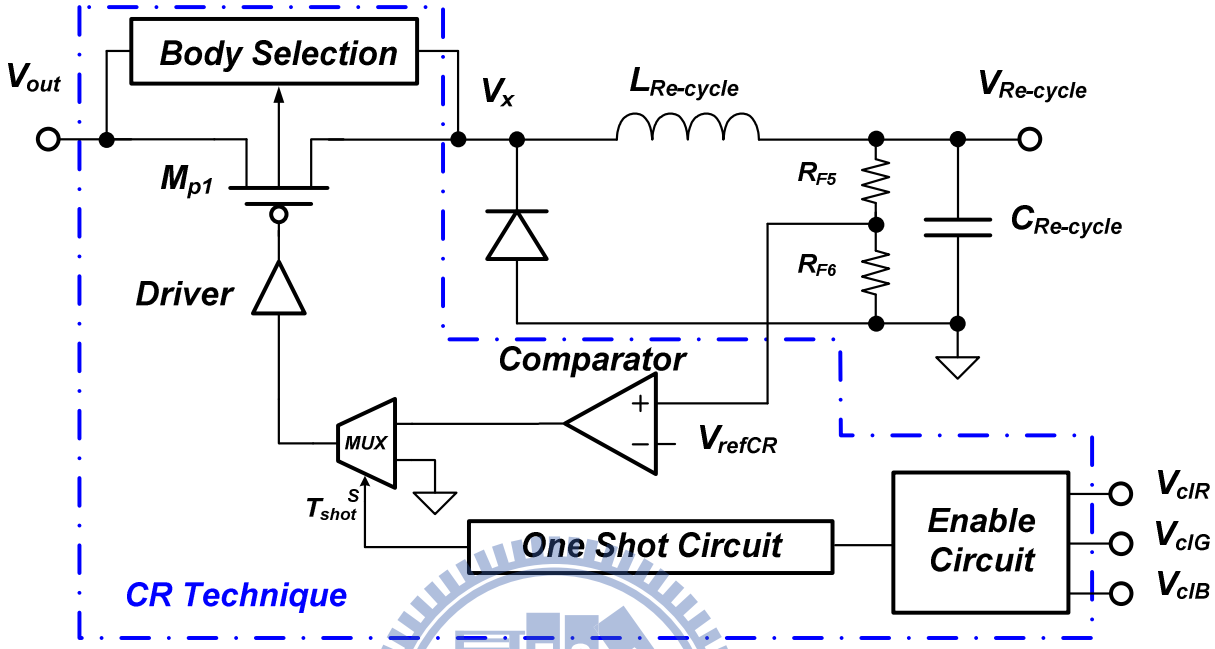


Figure 28. The schematic of the charging-recycling technique.

At the beginning of the operation of the LED driver, the LED backlight module enters the soft-start period. The output voltage of the LED driver is slowly and smoothly raised to the low output voltage for driving R-LEDs. Simultaneously, the comparator turn on the power transistors M_{p1} and the voltage $V_{Re\text{-}cycle}$ followed the output voltage V_{out} is also slowly pulled up to low-supplying voltage level in the CR technique. After the soft-start period, the LED driver enters the normal operation for the modified FCS algorithm. In addition, the FCS algorithm begins to display different color LED in sequence for the reducing the effect of the color breakup. Therefore, three signals (V_{clR}, V_{clG}, V_{clB}) are enabled to turn on/off three different color LEDs. The LED driver needs to switch the output voltage between the high- and low-supplying voltage levels for minimizing the power consumption because the high-supplying voltage level for 6-series R-LED consumes much power due to the large voltage across the current balance circuit compared to G- or B- LEDs.

When the LED backlight module changes from G- or B- LED to R- LEDs, the signal V_{clR} is switched to low and the voltage V_{out} will be decreased from high- to low-supplying voltage levels. In the meanwhile, the one-shot circuit will generate the signal T_{shot} to turn on the power transistor M_{P1} and decide the duration of the storing period. Therefore, the CR technique is activated and the extra charge on the output capacitor is delivered to the re-cycling capacitor $C_{Re\text{-}cycle}$ via the inductor and power transistor M_{p1}. Owing to the current continuity of the inductor, the CR technique can continuously deliver extra charge to the re-cycling capacitor $C_{Re\text{-}cycle}$ even that the output voltage V_{out} is smaller than the voltage $V_{Re\text{-}cycle}$. Therefore, the high-supplying voltage level can be rapidly pulled down due to the charge storage on the re-cycling capacitor. Therefore, the CR technique can totally deliver the extra charge from the output capacitor C_{Load} to the external capacitor $C_{Re\text{-}cycle}$ if the $C_{Re\text{-}cycle}$ is chosen with a value similar to that of the C_{Load}. Therefore, the output voltage is rapidly pulled down to the lower regulation voltage for driving R-LED and the LED driver effectively stores the charge on the re-cycling capacitor $C_{Re\text{-}cycle}$. And the one-shot time is defined as (27) by the laws of conservation of energy.

$$T_{shot} = \frac{(C_{Load} \text{ or } C_{Re-cycle}) \times V_{diff}}{I_{LRe\text{-}cycle(avg.)}} \tag{27}$$

The difference voltage V_{diff} is defined as the difference between the high- and low-supplying voltage levels for controlling the charge storing or restoring procedure. $I_{LRe\text{-}cycle(avg.)}$ is an average inductor current in the charge storing procedure. Therefore, the period of CR technique is inversely proportional to the value of the inductor current $I_{LRe\text{-}cycle}$ according to (27). During the charge-recycling procedure, the peak value of inductor current I_{peak} is approximated to $2 \times I_{LRe\text{-}cycle(avg.)}$ and the slope of inductor current is defined as $\Delta V / L_{Re-cycle}$. In addition, the value of ΔV is nearly equal to $V_{diff} / 2$ and the peak current appears at time

$t = T_{shot}/2$. Therefore, based on (27), the period of charge-recycling process T_{shot} can be derived as (28).

$$I_{peak} = \frac{\Delta V}{L} \cdot t \;\Rightarrow\; (I_{LRe\text{-}cycle})_{avg} = \frac{V_{diff} \times T_{shot}}{8L_{Re-cycle}}$$

$$\Rightarrow\; T_{shot} = \sqrt{8L_{Re-cycle}(C_{Load} \text{ or } C_{Re-cycle})} \tag{28}$$

According to (28), the value of T_{shot} is proportional to square of the product of the values of inductor and capacitor. It means the larger the values of inductor and capacitor need more storing/restoring time. Furthermore, it is also important to limit the peak inductor current to prevent the circuit from being damaged by the large inductor current. Thus, the boundary of the peak current is expressed as (29).

$$I_{peak} \le \sqrt{\frac{2(C_{load} \text{ or } C_{Re-cycle})}{L_{Re-cycle}}} V_{diff} \tag{29}$$

According to (28)-(29), the CR technique can utilize the larger inductor to decrease the peak inductor current and extend the period T_{shot} to accomplish the charge-recycling procedure. On other hand, when the one of the signals V_{clG} and V_{clB} is switched to low and the signals V_{clR} is switched to high, it means that the output voltage will be raised from low- to high-supplying voltage level for turning on the G-/B- LEDs. Therefore, the signal T_{shot} is generated by the one-shot circuit and the restoring period is started to restore the charge from the re-cycling capacitor to the output capacitor, thereby rapidly raising the output voltage back to its high-supplying voltage level. Hence, that means the restored charge can rapidly raise the output voltage back to it regulated voltage level and the rising recovery time is effectively decreased to extend the emission of the LED for ensuring the brightness. The

timing diagram of charge-recycling procedure is conceptually depicted in Figure 29. Moreover, since the recycling voltage $V_{Re\text{-}cycle}$ switches between high- and low-supplying voltage levels, the body selection circuit is needed to avoid the forward biasing current for improving power efficiency.

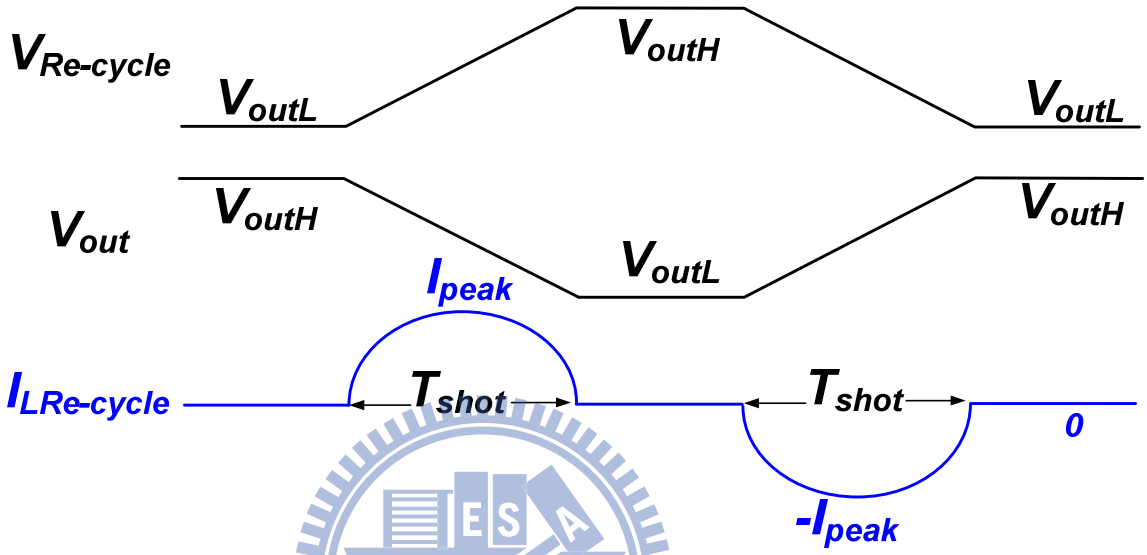


Figure 29. The timing diagram of the proposed charge-recycling technique.

The selection of the inductor and capacitor can ensure the CR technique smoothly transfers energy between two external capacitors depend on the equation (27)-(29). According to the previous designs, the pulling down response time depends on the load current and output capacitor. It is very hard to speed up the response time. However, due to the existence of the CR technique, the response time can be effectively reduced. Furthermore, when the output voltage V_{out} is needed to switch from low- to high-supplying voltage level, the stored energy is restored back to the output capacitor C_{Load}. Considering another condition that G-LED changes to B- LED or vice versa, the CR technique is not activated due to the same output voltage level for driving G- or B- LEDs. The CR technique not only saves much power when the backlight module changes from G- or B-LED to R-LED but also speeds up the transient response time.

3.1.3 Reference Tracking Procedure

The FRT and CR techniques can speed up the transient response of tracking response. Therefore, the reference tracking process of LED driver with mixed color sequential can be divided into four stages, which are described as follows.

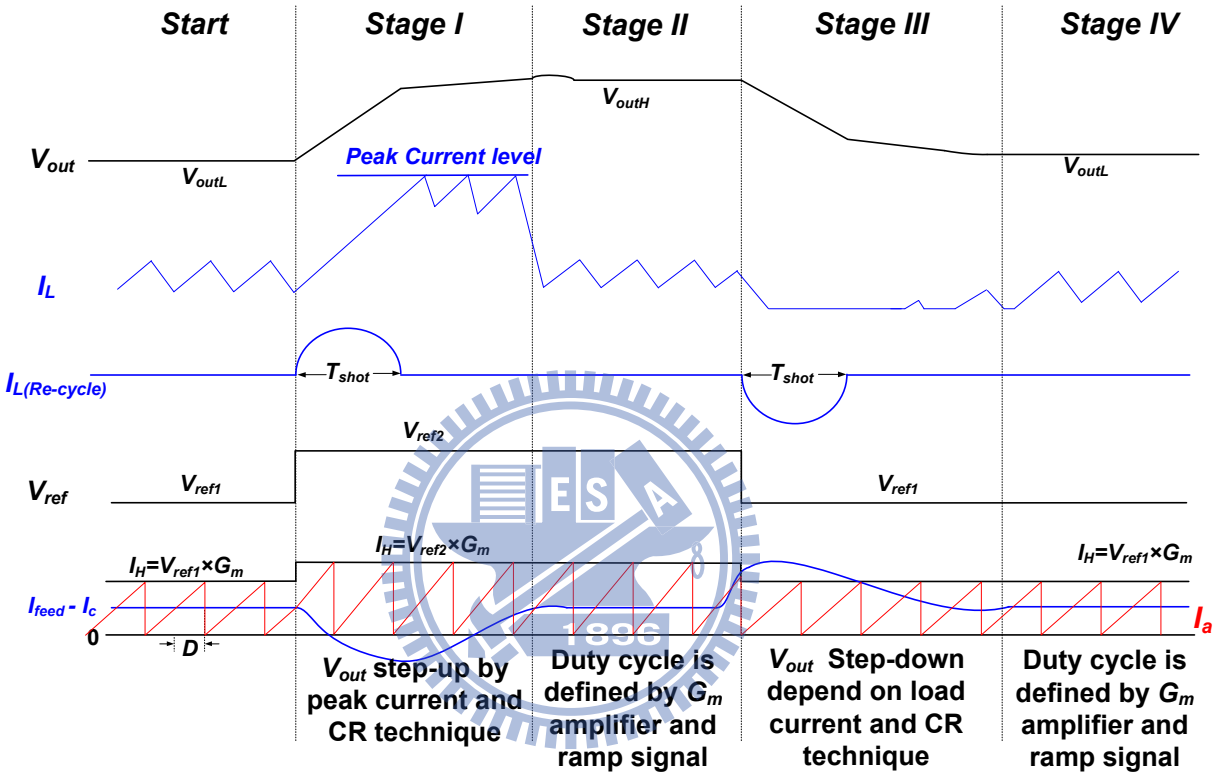


Figure 30. The timing diagram of the proposed charge-recycling technique.

Stage I: When the reference voltage V_{ref} steps from V_{ref1} to V_{ref2}, the peak value I_H of the saw-tooth current I_a is increased instantly due to reference tracking mechanism. The correction current I_c, which is the output of G_m amplifier, is also increased owing to a larger difference voltage between V_{ref} to V_{fb}. A feedforward current I_{feed} is determined by input voltage V_{in}. The difference current between I_{feed} and I_c is compared to the saw-tooth current I_a for determining duty cycle. Therefore, the current of I_{feed} - I_c is decreased instantly as a result that reference voltage V_{ref} is increased. Thus, by comparing I_a and I_{feed} - I_c, the control signal V_{PWM} is switched to a high level and the turn-on time of power transistor MN_1 in Figure 5 is limited to a predefined maximum duty that represents a peak current level. Thus, the boost

converter is controlled by the peak current loop. At this time, the CR technique also conveys the energy from the capacitor $C_{Re\text{-}cycle}$ to output capacitor C_{load}. Therefore, the voltage $V_{Re\text{-}cycle}$ is decreased by CR technique and the output voltage can be quickly increased. The output voltage is raised to a high-supplying voltage level for a forward conduction voltage of 6-series green or blue LED within a short time.

Stage II: When the output voltage V_{out} approaches the high-supplying voltage level V_{outH}, the correction current I_c is gradually decrease because the difference voltage between V_{fb} and V_{ref} is decreased and the characteristic of fast response of the G_m amplifier [31-32]. Hence, the current of I_{feed} - I_c is increased rapidly and then the outputs of the PWM generator can substitute for the peak current control to regulate the output voltage of the LED driver. Certainly, the static error is minimized due to the insertion of feedforward current I_{feed} compared to the current-mode boost converter with current-domain control.

Stage III: When the reference voltage V_{ref} is decreased instantly from V_{ref2} to V_{ref1}, the correction current I_c by the G_m amplifier is instantly decreased owing to a larger difference voltage between V_{ref} and V_{fb}. Furthermore, due to the reference tracking mechanism, the peak value of the saw-tooth current I_a is decreased instantly. Thus, the current I_a is decreased and the value of I_{feed} - I_c is increased instantly as well. By comparing the values of I_a and I_{feed} - I_c, the control signal V_{PWM} can be adjusted to a lowest level to turn off power transistor M_{N1} illustrated in Figure 6. In addition, the CR technique is activated and stores extra energy on the capacitor $C_{Re\text{-}cycle}$ at this time. Therefore, the output voltage of proposed LED driver is decreased according to load current and the CR technique. And the down tracking can be quickly achieved compared to conventional converter after the implementation of the CR technique.

Stage IV: When the output voltage is decreased to the low-supplying voltage level V_{outL}, the correction current I_c is gradually increased. Due to the fast response of the G_m amplifier,

the current of I_{feed} - I_c is decreased instantly. The fast and stable pulse width control is guaranteed and the timing diagram of the LED driver is shown in Figure 30.

3.1.4 The stability of the LED driver with the FRT and CR techniques

After the description of the FRT and CR techniques, the stability of the whole system must be guaranteed to ensure the stable operation. Because the CR technique is enabled in the transient time of reference tracking procedure, the stability analysis of LED driver can ignore the effect from the CR technique. Since the design of the LED driver is based on the voltage-mode boost converter design, the LED driver with FRT techniques is needed to be analyzed and compensated. The transfer function of a voltage-mode boost converter in CCM [33-35] is defined as (30).

$$T(s) = G_m(s) \times \frac{V_{out} r}{V_H D'} \times \frac{\left(1 - \frac{s}{\omega_z}\right)}{\left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right]} \tag{30}$$

where $\omega_0 = \frac{D'}{\sqrt{LC}}$, $Q = D'R\sqrt{\frac{C}{L}}$, and $\omega_z = \frac{(D')^2 R_{Load}}{L}$

r is feedback resistor ratio defined by (25). V_H is the amplitude of the saw-tooth signal. ω_0 is the double poles due to the output LC filter. The parameter Q is called the quality factor. ω_z is the right-half plane (RHP) zero of the boost converter in CCM operation. R_{Load} is the output equivalent load resistance. Instead of the error amplifier, the FRT technique uses the low-gain and high-bandwidth G_m amplifier to speed up the reference tracking time. $G_m(s)$ is used to stand for the transfer function of the G_m amplifier and can be treated as a low-gain amplifier

with having a high-frequency pole. As illustrated in Figure 27(a), in order to stabilize the whole system, a left-half plane (LHP) zero is inserted by the voltage-control current source (VCCS) compensator [36-37] to enhance the phase margin. Then, the system transfer function of the proposed structure is modified as (31).

$$T(s)=G_m(s)\cdot\frac{V_{out}r}{V_H D'}\cdot\frac{\left(1+\frac{s}{\omega_{z(VCCS)}}\right)\left(1-\frac{s}{\omega_z}\right)}{\left[1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2\right]},\ \text{where}\ \omega_{z(VCCS)}=\frac{-1}{kC_cR_{F1}} \tag{31}$$

$\omega_{z(VCCS)}$ is an low-frequency LHP zero generated by the VCCS compensator. The parameter k is the amplified factor of the compensation capacitor C_c and is determined by the VCCS compensator. The stability of the proposed boost converter can easily promised by using a G_m amplifier with a high-frequency pole above the crossover frequency and a low-frequency zero $\omega_{z(VCCS)}$. The Bode plot of the converter as illustrated in Figure 31 show the adequate phase margin [38].

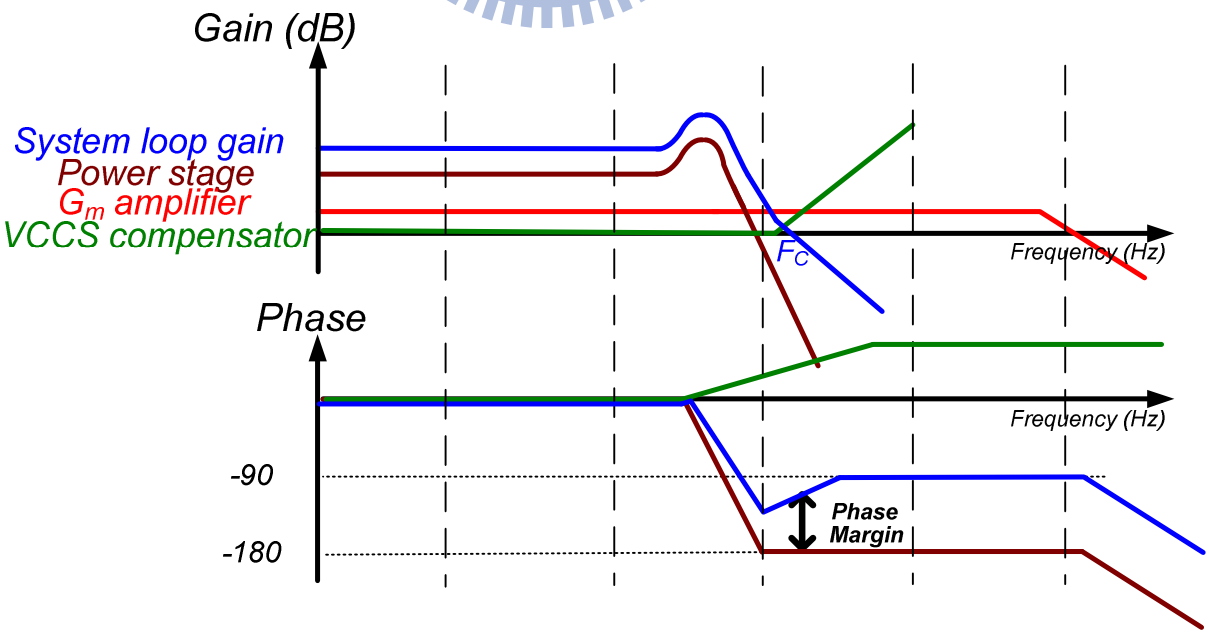


Figure 31. The Bode plot of the proposed boost converter.

3.2 Current Sensor and Charge Reservation Circuits

3.2.1 The Design of the Voltage Control Current Source Compensator

The purpose of the voltage control current source (VCCS) compensator is to generate a low-frequency zero to extend phase margin. The design of the VCCS compensator is depicted in Figure 32. Due to the variations of the output voltage, the small-signal current I_1 can be expressed as (10) by using small integrated capacitors C_{c1} and C_{c2}. In addition, the resistors R_1 and R_2 must be used to reduce the DC level of output voltage for avoiding that the capacitor C_{c1} is damaged by higher voltage.

$$I_1 = \frac{aV_{out}}{1/sC_{c1} + Z_x} \quad \text{where } a = \frac{R_2}{R_1 + R_2} \tag{32}$$

Z_x is output impedance seen at node X. The value of Z_x is low enough to be ignored since there is a negative feedback loop that is composed of transistors M_1 and M_3 [37]. Ideally, the small-signal current I_1 flows through transistor M_1 because the impedance at the source of transistor M_1 is much smaller than that of the bias current source. Thus, the small-signal voltage at node Y is equal to (33).

$$V_Y = I_1 \times R_o \tag{33}$$

R_o is the output resistance seen at node Y. In order to convert the small-signal voltage to current signal, a transconductance amplifier g_m is used and thus the output current of the VCCS circuit I_{out} is defined as (34).

$$I_{out} = g_m \times V_Y = \frac{g_m R_o V_{out}}{\frac{1}{sC_{c1}} + Z_x} = \frac{sC_C g_m R_o a V_{out}}{1 + sC_{c1} Z_x} \approx sC_{c1} g_m R_o a V_{out} = skC_{c1} V_{out} \quad (34)$$

where $k=g_m R_o(R_1/(R_1+R_2))$ is the multiplication factor to amplify the effective value the small compensation capacitor C_c. That is only a small capacitor is needed to generate a LHP zero near the crossover frequency. Besides, the other parasitic poles in the VCCS compensator locate at higher frequency because the value of impedance Z_x is small. Therefore, these poles have no effect on the stability of the system. Therefore, a low-frequency zero is generated by the VCCS circuit without inserting any low-frequency pole.

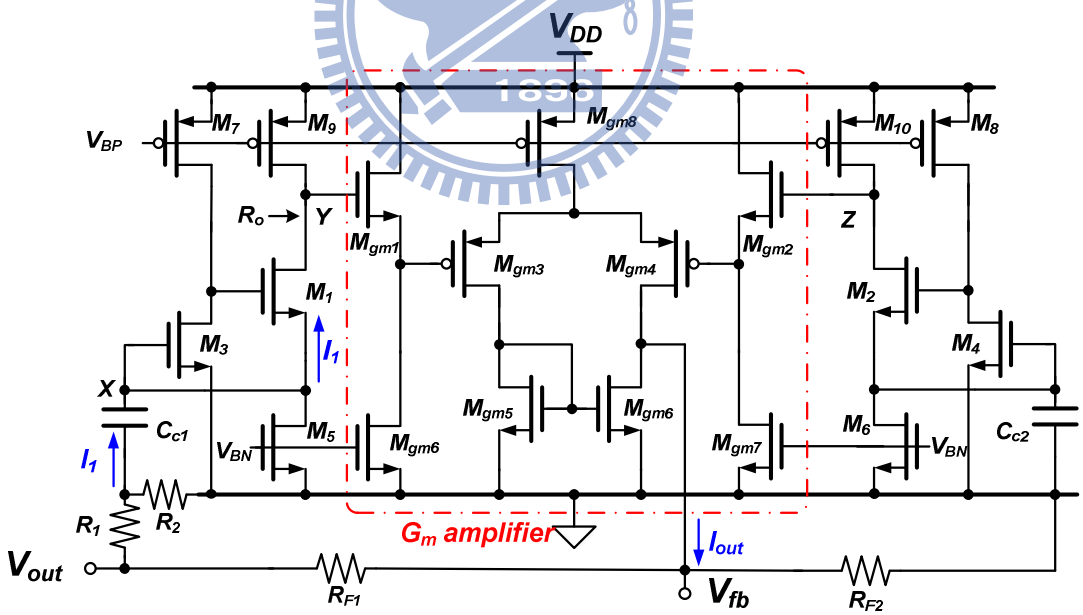


Figure 32. The circuit of the VCCS compensator.

3.2.2 The Implementation of the PWM Generator

with FRT Technique

The circuit implementation of the PWM generator with FRT technique is shown in Figure 33. The circuit is used to generate the prediction PWM control signal and consists of two voltage-to-current circuits, a G_m amplifier, and a current comparator. In order to have the same transconductance of the two voltage-to-current converters, the resistors R_1 and R_2 of the two voltage-to-current converters are designed to have the same value. The upper bond of the voltage V_{ramp} is defined as V_{ref} and the low bond of the voltage V_{ramp} is defined as ground. Therefore, the voltages V_{ramp} and rV_{in} are converted into current signals I_a and I_{feed} to implement the equations (24)-(26) by the two voltage-to-current converters with the same transconductance. The matching methods of layout technique are carefully used to reduce the process variation between the two resistors. The G_m amplifier [31] is used to convert the difference voltage between V_{fb} and V_{ref} to a current signal I_c. That is the signals V_{fb} and V_{ref} are applied to the gates of transistor M_1 and M_2, respectively. The output current I_c is injected to the input of the current comparator. The flipped-voltage-follower (FVF) is used to minimize the resistance seen at node X and Y for improving the linearity of the transconductance of the G_m amplifier. Obviously, the reduction of the impedance at node X or Y can be found as (35).

$$Z_x \approx \frac{1}{g_{m1}} \frac{1}{g_{m5} r_{o5}} \frac{1}{g_{m3} r_{o1}} \tag{35}$$

Therefore, the transconductance of the G_m amplifier is approximated to $1/R$ due to the low impedance at node X and Y. After the operation of the three current mirrors, which are (M_3, M_7), (M_4, M_8), and (M_9, M_{10}), the correction current I_c is defined as (36).

$$I_c = 2N \frac{V_{ref} - V_{fb}}{R} \tag{36}$$

The current I_{PWM} is the summation of the ramp current I_a, the feedforward current I_{feed}, and the correction current I_c at the input of the current comparator. Thereby, the value of the current I_{PWM} decides the duty of the PWM signal. Moreover, not only the prediction duty cycle can be decided by I_a and I_{feed} but also the correction current can adjust the duty cycle to regulate the output voltage.

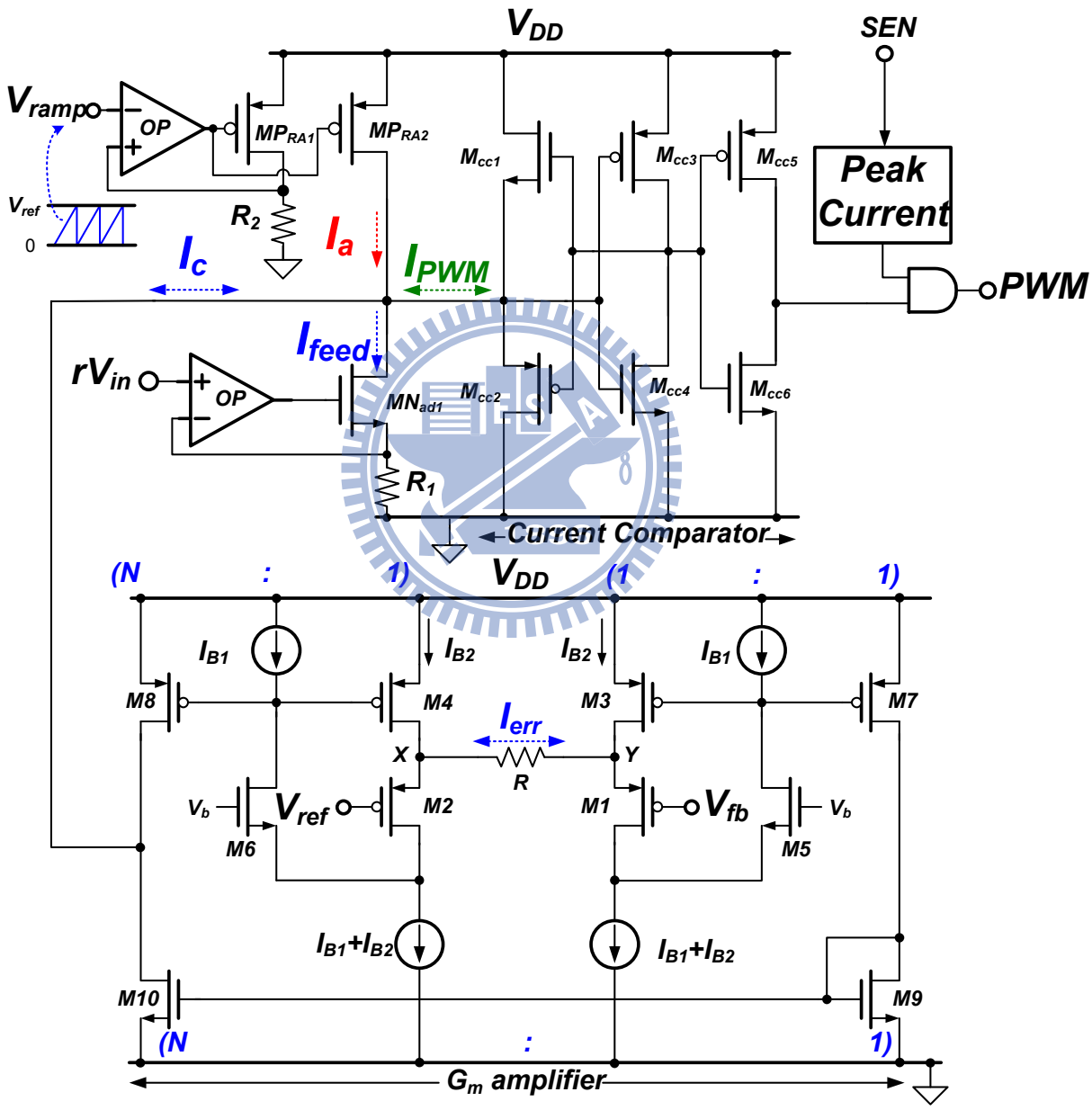


Figure 33. The PWM generator with FRT technique consists of voltage-to-current converters, G_m amplifier, and current comparator.

3.2.3 The Proposed One-Shot Generator for Charge Recycling Technique

The FCS algorithm implemented by FPGA send the controlling signals (V_{clR}, V_{clG}, and V_{clB}) to turn on/off the different color LED in sequence as shown in Figure1. In addition, the LED driver not only supplies 16V to supply 6-series R- LED but also supplies 21V to 6-series G- or B- LED for minimizing the voltage across the current balance circuit to maintain high efficiency [8-9]. According to the color of the backlight module in the section I of the notebook with FCS algorithm as illustrated in Figure3, the controlling signals V_{clR}, V_{clG}, and V_{clB} are turned on/off in sequence and can define the output voltage level as depicted in Figure 34. The black (K) frame means that all the LED are turned off to reduce the effect of color breakup. Furthermore, the output voltage is kept constant when the black frame is inserted to the FCS algorithm. Until one of the controlling signals which need different output voltage level is switched to the low level, the output voltage will be changed to the appreciate voltage for reducing power consumption on the current balance circuit. Therefore, when the output voltage switches from high- to low-supplying voltage level or low- to high-supplying voltage level, the LED driver will start the CR technique to transmit the charge for speeding the reference tracking procedure.

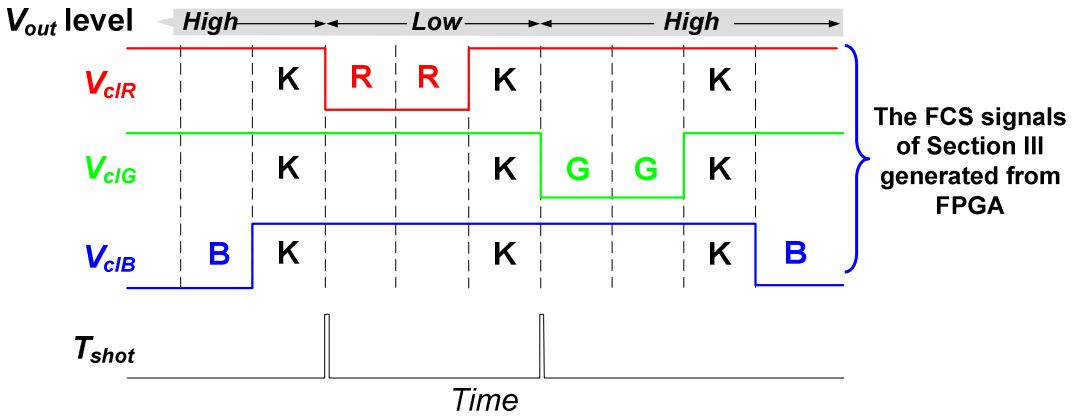


Figure 34. The timing diagram of modifier FCS signal in Section I of the notebook and the one shot signal T_{shot}.

These signals (V_{clR}, V_{clG}, and V_{clB}) used to generate the one-shot signal T_{shot} are shown in Figure 34 to decide the turning on/off the power transistor M_{p1} of the CR technique in Figure 8. Therefore, the one-shot generator, which is composed of the enable circuit and two one-shot circuits, utilizes the three signals (V_{clR}, V_{clG}, and V_{clB}) to start the CR technique as shown in Figure 35. The enable circuit uses three input signals (V_{clR}, V_{clG}, and V_{clB}) to generate two signals V_{s1} and V_{s2}. The one-shot circuit produces the one-shot signal T_{shot} when one of the signals V_{s1} and V_{s2} is instantly pulled to high. Furthermore, the one-shot circuit I will be reset until the signal V_{s1} is switched to low and so does the one-shot circuit II. When the LED backlight module turns off the G- and B- LEDs, the controlling signals V_{clG} and V_{clB} reset the signal V_{s1} to low. Therefore, when the signal V_{clR} is switched from high to low means that the R-LED will be turned on, the signal V_{s1} will be instantly pulled to high and the output voltage should change from high- to low-supplying voltage level. Therefore, when the signal V_{s1} is pulled to high, the capacitor C_{p1} is discharged by biasing current I_{B1} to generate the one-shot signal T_{shot}. Therefore, the signal T_{shot} is utilized to turn on the power transistor M_{p1} in Figure 8 and thereby the CR technique is activated to store the energy on the re-cycling capacitor $C_{Re\text{-}cycle}$. The length of the one-shot signal T_{shot} can be calculated as (37).

$$T_{shot} = \frac{(V_{DD} - V_H)C}{I_B} \tag{37}$$

Therefore, the one shot circuit can modulate the length of one-shot time by adjusting the capacitor and biasing current for achieving the preferable CR technique. In practice, the length of the one-shot time may be varied by the process variation. The value of the capacitor is trimmed to finely adjust the value of switching frequency [39]. Similarly, when the R-LED are turned off by the controlling signal V_{clR}, the SR-latch will reset the signal V_{s2} to low. Until one of the signals V_{clG} and V_{clB} is pulled to low, the signal V_{s2} will be switched to high and it

represents that the LED driver should supply high-supplying voltage level to turn on the G- or B- LEDs. Therefore, the signal will enable the one-shot circuit to start the CR technique to restore the energy back to the capacitor C_{load}. Thus, the CR technique can achieve the fast up- and down- reference tracking procedure and high efficiency without consuming much power.

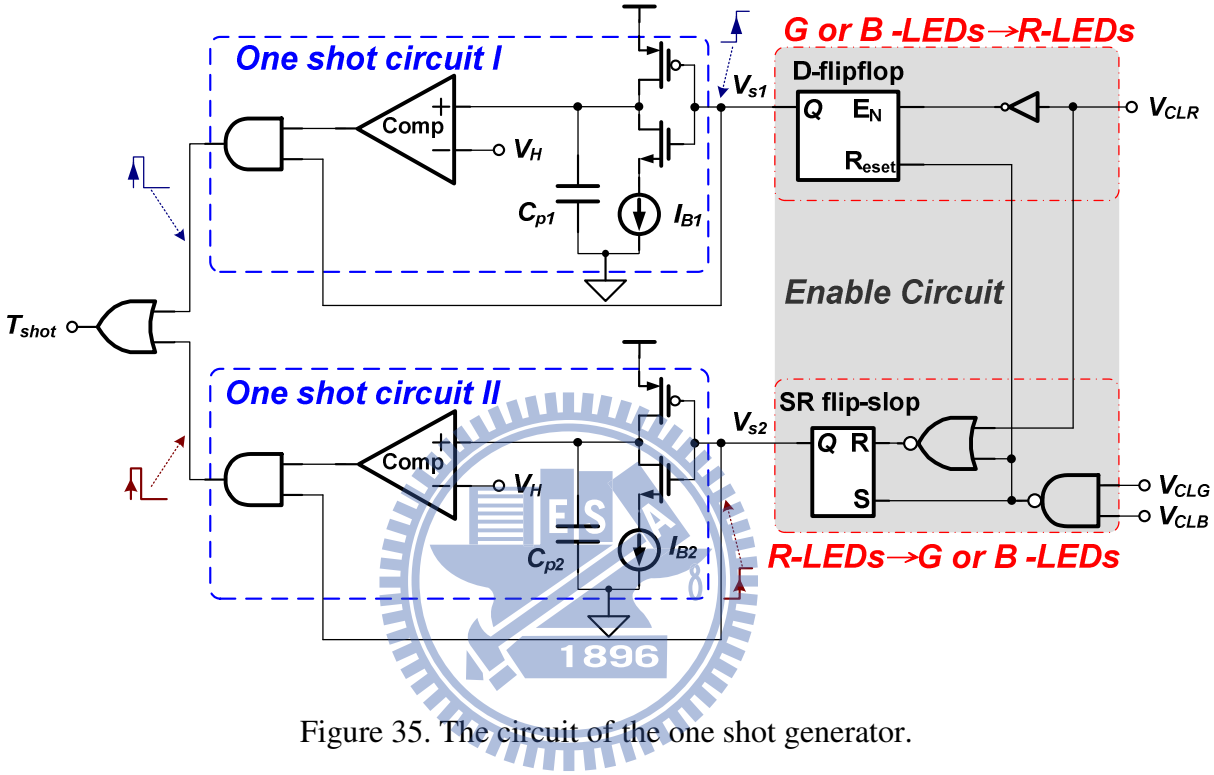


Figure 35. The circuit of the one shot generator.

3.2.4 Proposed Constant Current Regulator

In generally, the light luminance of LED is controlled by the driving current [8-9]. Therefore, the LED backlight module utilizes the current balance circuit to control the amount of driving current for regulating the constant light luminance of LEDs. The current balance circuit composed of three current regulators is controlled by the signals V_{refI}, V_{clR}, V_{clG}, and V_{clB} from the FPGA as shown in Figure 36. The current regulator utilizes the operation amplifier (OP) and the resistor R to operate as a voltage-to-current converter. Furthermore, the input signals V_{refI}, which is converted by the digital-to-analog (D/A) converter in the FPGA, determines the value of the driving current in the series connection LEDs. Thus, the voltage

signal V_{refI} is used to generate the constant current. After the two current mirrors pairs, which are (M_{P1}, M_{P2}), (M_{N1} - M_{N5}), the current I_{LEDR} can be used to drive the 4 brunches of LED and thus the variation of drain-source voltage of these transistors (M_{N1} - M_{N5}) will not have large influence on the value of current I_{LEDR}. Moreover, the FPGA uses the three signals V_{clR}, V_{clG}, and V_{clB} to turn on/off the R-, G-, and B- LED for achieving the FCS algorithm as shown in Figure 3. Using the R-LED as an example, the transistor M_{C1} operates in the cut-off region when the signal V_{clR} is pulled to high level. Thus, the current I_{LEDR} is equal to zero and unable to drive the R-LEDs. In other words, when the V_{clR} is pulled to low and the transistor M_{SR} operates in cut-off region, the voltage-to-current converter will start to convert the reference voltage V_{refI} to current signal I_{LEDR} for driving the R-LEDs. Therefore, the current balance circuit is used to generate the constant current to drive the LED for constant light luminance. The FCS algorithm can be achieved by turning on/off the LED according the values of signals V_{clR}, V_{clG}, and V_{clB}. When the current regulator is activated to convert the current, the transistors (M_{N1} - M_{N5}) operated in the saturation region generally stress the drain-source voltage for reducing the power consumption.

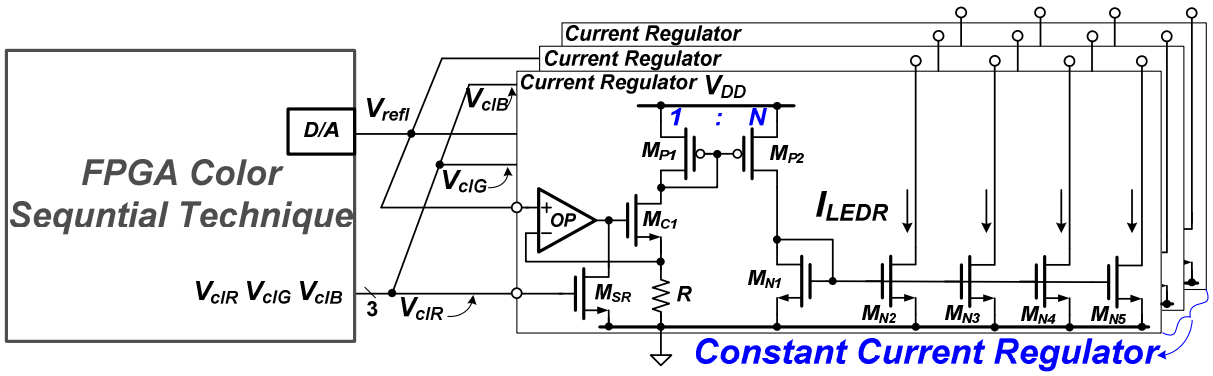


Figure 36. The constant current regulator.

Chapter 4

The Proposed Buck-Store Boost-Restore (BSBR) Technique

4.1 The Buck-Store and Boost-Restore Technique

The output voltage for driving the series-connected R-LED is smaller than that for driving G-LED and B-LEDs. Thus, the output voltage of the boost DC-DC converter needs to switch between two output voltages, which are 9.3V and 12.4V. In order to switch the output voltage between the two values, the reference voltage integrated in the chip needs to switch between 0.92V and 1.22V. The proposal BSBR technique is applied to the boost DC-DC converter for achieving fast and efficient reference tracking performance. The function blocks and waveforms are illustrated in Figure 37 (a). The BSBR technique delivers extra charge and stores it on the capacitor C_{BSBR} once the output voltage V_{out} expresses much voltage stress on the constant current generator. As a result, the reference down tracking is sped up and more charge is saved to achieve high efficiency compared to the conventional structure [40]. In other words, the LED backlight module can get higher efficiency due to low voltage headroom of the constant current generator. Furthermore, the BSBR technique recycles the stored charge back to the capacitor C_{Load} when the FCS technique changes the color of LED from red to green or blue. Therefore, the BSBR technique can efficiently recycle extra charge [33] and enhance the transient response of reference tracking. When the BSBR technique is enabled to store or restore extra charge, the boost converter is disabled to prevent the two

power stages from being influenced by each other. That is, the boost converter is shutdown when the BSBR technique efficiently transfers the charge between the two capacitors C_{Load} and C_{BSBR}. The architecture of the BSBR technique contains one BSBR power stage and one BSBR controller. The input node of the BSBR power stage is connected to the output node of the boost DC-DC converter. The output node of the BSBR power stage is named as V_{BSBR}. There is a large capacitor C_{BSBR} connected at the node V_{BSBR} in order to store extra charge from the output node of the boost DC-DC converter. The stored charge can be utilized to pull the voltage V_{out} back to a higher level or to drive another sub-block in the LCD system. Furthermore, the BSBR power stage can regulate the steady output voltage for the sub-block of LCD system when the digital signal *EN* is triggered from high to low level.

The signal E_{ref} generated by the LCD timing control system can indicate the display color is. That is, the high- or low-level of this signal represent the output voltage of the boost converter as high- or low-supplying voltage, respectively. The transition of the signal E_{ref} from low to high indicates the output voltage V_{out} needs to be raised to high-supplying voltage level. The stored charge should be restored back to the output voltage V_{out}. On other hand, the transition of the signal E_{ref} from high to low indicates the output voltage V_{out} needs to be reduced to the low-supplying voltage level. As a result, extra charge should be stored in the BSBR capacitor C_{BSBR}. The signal E_{ref} can be used to determine whether it is the buck-store or boost-restore operation. The signal E_{BSBR} is a signal to coordinate the two power stages, which are the boost converter and the BSBR power stage, in order to correctly control the two closed loops. The digital signal V_{PWM} indicates the current comparator output of the PWM generator and it reflects the output voltage information. The signal V_{sen} is the sensing information of the inductor L current. The signals V_P and V_N indicate the sensing information of the inductor L_{BSBR} current.

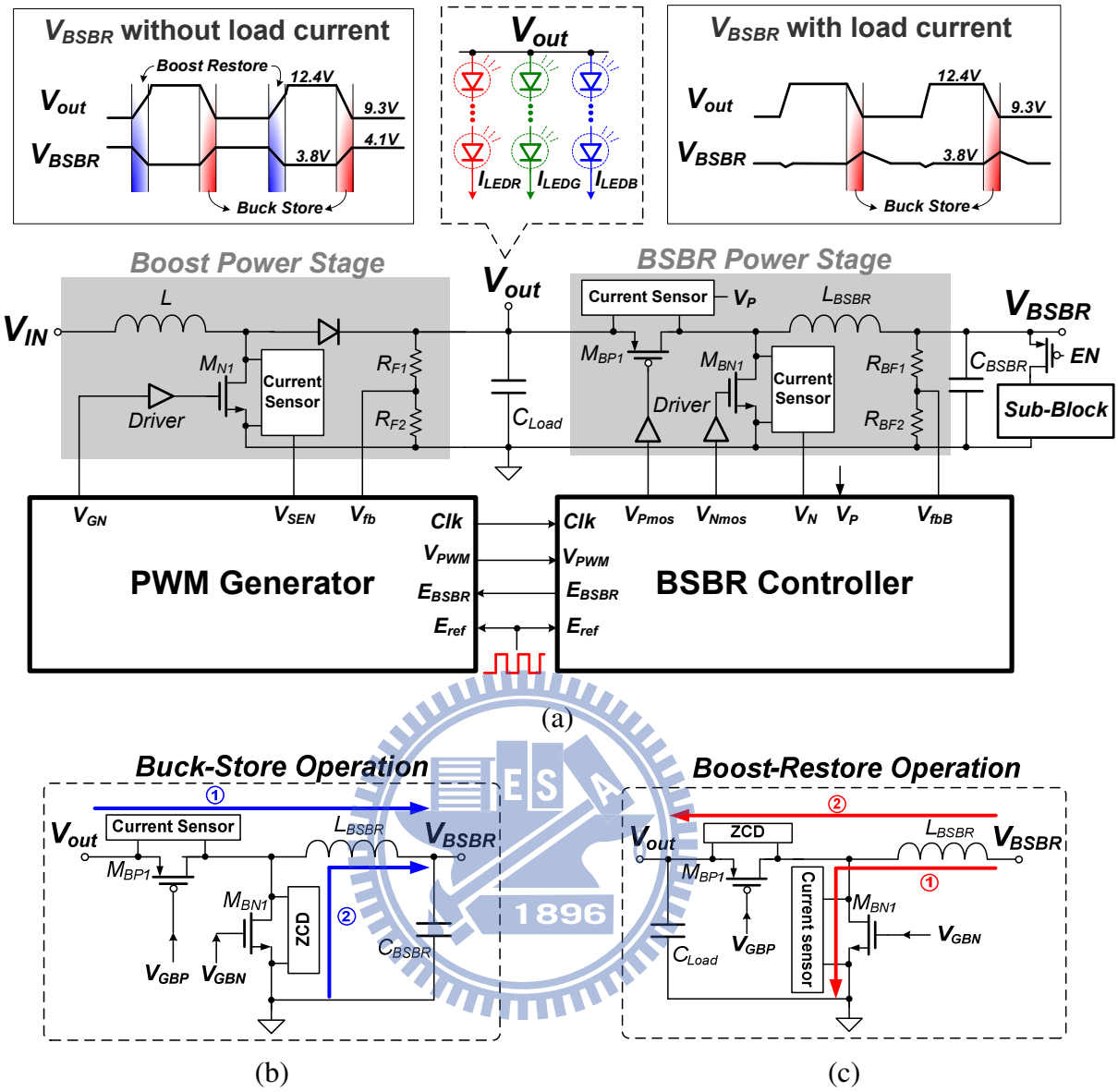


Figure 37. (a)The proposed boost converter with BSBR technique and the timing diagram of the voltage V_{BSBR} with/without load current requested from another sub-block in the LCD driving system. The BSBR power stage can be simplified as (b) buck-store operation and (c) boost-restore operation.

4.1.1 Architecture of the BSBR Power Stage and Controller

The BSBR technique is composed of the buck-store and boost-restore operations. Extra charge is transferred from the output capacitor C_{Load} to the capacitor C_{BSBR} by the buck-store

operation and restored from C_{BSBR} back to C_{Load} by the boost operation. The reference down-tracking utilizes the buck-store operation to rapidly reduce the output voltage of the boost converter from the high- to low-supplying voltage level. The BSBR controller is enabled to turn on the P-type power transistor M_{BP1} first to increase the inductor current. The duty cycle is determined by the closed loop of the BSBR controller. After turning off the M_{BP1}, the BSBR controller turns on the N-type power transistor M_{BN1} to decrease the inductor current. In addition, the current-sensing circuit of p-type power transistor M_{BP1} is utilized to set the maximum delivering current and the current sensing circuit of n-type power transistor M_{BN1} is used as the zero-current-detector (ZCD) mechanism for avoiding the reversal inductor current releasing to ground. The procedure that the output voltage V_{out} delivers charge to the capacitor C_{BSBR} for storing extra charge is similar to the operation of a buck converter [28] that steps down the output voltage V_{out} to the voltage V_{BSBR} and the BSBR power stage can be simplified as the buck-store operation illustrated in Figure 37(b). For the reference up-tracking operation, the system turns on the n-type power MOSFET M_{BN1} to increase the inductor current at first and then turns on the p-type power transistor M_{BP1} to decrease the inductor current after the power MOSFET M_{BN1} is turned off.. The charge stored on the capacitor C_{BSBR} can be restored back to the capacitor C_{Load}. Similarly, the current-sensing circuits of p-type and n-type power transistors are operated for ZCD and current-limiting mechanism, respectively. Thus, V_{BSBR} steps up the output voltage V_{out} through the operation of the boost converter as shown in Figure 37(c). Therefore, the BSBR technique can rapidly pull down the output voltage V_{out} from 12.4V to 9.3V and raise V_{out} back to 12.4V from 9.3V when driving the G-LED and B-LEDs. Furthermore, the BSBR power stage is also designed as a switching converter to regulate a steady voltage at node V_{BSBR} by the simple PFM control when the BSBR technique is disabled.

4.1.2 The Tracking Algorithm of the BSBR

Technique

The BSBR power stage is controlled by the three operation loops (buck-store operation, boost-restore operation, and PFM) to pull down/up the output voltage or regulate the BSBR voltage V_{BSBR}. Therefore, the tracking algorithm of the BSBR technique is necessary to choose the appropriate operation loops for avoiding incorrect switching sequences. The algorithm is described by the flowchart in Figure 38 starting from the transition of the signal E_{ref} from high to low or low to high. For the buck-store operation, this algorithm estimates the values of the voltage V_{BSBR} and the PWM signal V_{PWM} to decide whether the charge needs to store in the BSBR capacitor C_{BSBR} or not. When all of the controller signals are in the correct state, the BSBR power stage increases the inductor current by means of energy delivering from the output voltage V_{out}. Hence, the charge is transferred to the capacitor C_{BSBR} every switching cycle. The boost converter is disabled in the meantime in order not to disturb the closed loop of the BSBR power stage.

When the output voltage V_{out} approaches to the low-supplying voltage (V_{Low}) or the voltage V_{BSBR} exceeds the predefined voltage V_{max}, the algorithm ends the buck-store operation loop and the BSBR power stage is controlled by the PFM operation. In succession, the boost converter is enabled to regulate the output voltage V_{out}. Consequently, the voltage V_{BSBR} is increased due to extra charge stored on the BSBR capacitor C_{BSBR}.

For reference up-tracking response, the algorithm will enable the boost-restore operation loop if the signals V_{BSBR} and V_{PWM} are set by the correct values. The stored charge is transferred from the BSBR capacitor C_{BSBR} to the output load capacitor C_{Load} and thereby steps up the output voltage. Until the voltage V_{BSBR} is lower than the predefined minimum voltage V_{min} or the output voltage V_{out} approaches to the high-supplying voltage V_{High}, the boost-store operation loop is ended and then the output voltage will be regulated by the boost

converter. Furthermore, the algorithm also determines the function of current-sensing circuit in the different power transistors M_{BN1} and M_{BP1} as ZCD or current limiting mechanism.

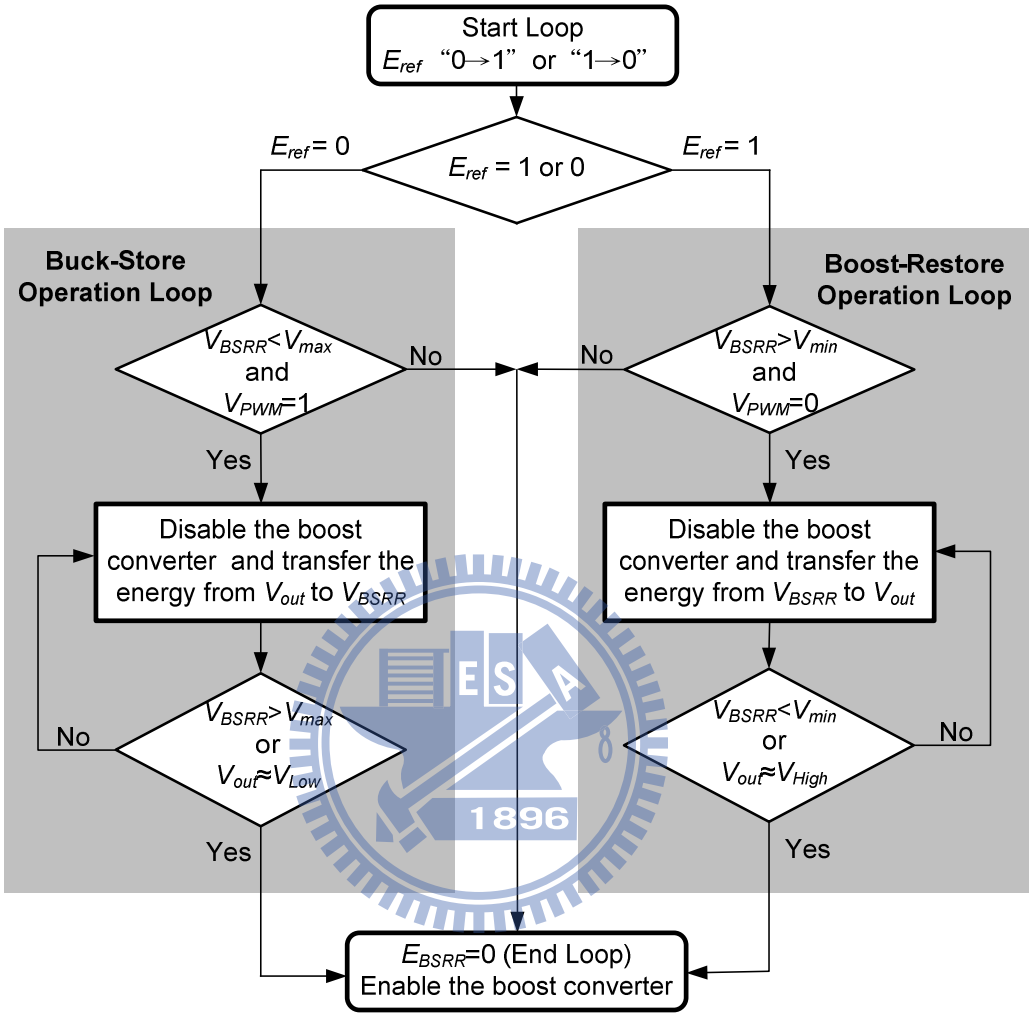


Figure 38. The flowchart of the BSBR tracking algorithm.

When the BSBR technique is disabled by the tracking algorithm, the voltage V_{BSBR} is also designed to supply a regulated voltage by PFM operation for another sub-block in the LCD system. Therefore, this voltage should be kept constant to prevent the sub-block in this system from being affected by the voltage variation [8-9]. Therefore, the C_{BSBR} (10μF) is designed larger than the C_{load} (1μF) and the voltage V_{BSBR} only rises one-tenth of the output voltage due to the law of the charge conservation ($Q \equiv C \times V$). In this design, the V_{BSBR} is used to turn on white LEDs. Furthermore, the maximum current supplied by the PFM operation of BSBR controller is about 100mA in this design.

4.1.3 The Efficiency of Charge Transition

The BSBR technique is utilized to transfer extra charge between the capacitors C_{Load} and C_{BSBR}. The extra charge energy can be expressed as (38).

$$W_{cap} = \frac{1}{2} C_{Load} \Delta V^2 \tag{38}$$

The ΔV is the different voltage between high- and low- supplying voltage. During the transforming procedure, part of the energy is consumed by the equivalent on-resistance of power transistors (M_{BN1} and M_{BP1}). The energy stored on the capacitor is also wasted on the feedback resistors (R_{BF1} and R_{BF2}) during the transition period depending on the FCS frequency. Therefore, the transforming efficiency can be approximated by (39).

$$\eta_{tran} = \frac{W_{cap} - W_{R\_on} - W_{VBSBR}}{W_{cap}} \tag{39}$$

The W_{R_on} and W_{VBSBR} represent the energy consumption on the power transistor and feedback resistor as shown in (40) and (41), respectively.

$$W_{R\_on} = I_{avg}{}^2 R_{ds\_on}(T_{up} + T_{down}) = 2 I_{avg} R_{ds\_on} C_{Load} \Delta V \tag{40}$$

$$W_{VBSBR} = \frac{V_{BSBR}{}^2}{R_{BF1} + R_{BF2}} T_{FCS} = \frac{V_{BSBR}{}^2}{(R_{BF1} + R_{BF2}) f_{FCS}} \tag{41}$$

R_{ds_on} is the equivalent on-resistance of power transistors. I_{avg} is the average transforming current during up- or down-reference tracking, C_{Load} is the output capacitance, T_{FCS} is the period of the FCS technique. T_{up} and T_{down} are the transient time of up- and down-reference tracking, respectively. According to (40), small R_{ds_on} and I_{avg} can reduce the energy

consumption of W_{R_on}. However, small R_{ds_on} leads to larger chip area due to large power transistors and thus the value of R_{ds_on} can be decreased depending on the chip area limitation. On the other hand, small average current I_{avg} results in longer transient time. Thus, in this proposed design, the maximum transforming current is designed to about 0.5A which is smaller than conventional current-limiting mechanism. In addition, according to (41), large feedback resistors (R_{BF1} and R_{BF2}) and small T_{FCS} can reduce the value of energy W_{VBSBR}. However, the period of T_{FCS} depends on the speed of liquid crystal rotation. As a result, a large resistor is chosen to improve the transforming efficiency.

4.2 The Circuit Implementation

4.2.1 The Implementation of the Proposed BSBR Controller

The proposed BSBR controller and its control signal timing diagram are shown in Figure 39. Basically, the operation mode of BSBR power stage can be divided into two parts, which are the PFM operation and the BSBR technique. The BSBR enable circuit is designed to implement the BSBR tracking algorithm as shown in Figure 40. This algorithm utilizes these signals V_{fbB} and V_{PWM} to appraise whether the system is suitable for transforming extra charge or not. Therefore, when these two conditions are suitable to enable the BSBR technique, this circuit will generate the signal E_{BSBR} to enable or disable the boost converter and the PFM operation of BSBR controller. Moreover, the signals Clk and E_{BSBR} produce the signal Clk_{BSBR} to increase the inductor current of the BSBR power stage for transferring the energy at a fixed frequency. Furthermore, the signal selector utilizes these two signals E_{BSBR} and E_{ref} to determine the operation mode and disable either the ZCD_{PMOS} or ZCD_{NMOS} mechanism for avoid incorrect switching. Therefore, this proposed BSBR technique uses these digital signals to determine the function of the BSBR power stage as buck-store (down-reference tracking)

or boost-restore (up-reference tracking) operation. Moreover, V_N and V_P are sensing signals of power transistor current (M_{BN1} and M_{BP1}). The BSBR technique uses these two signals V_N and V_P to decide the maximum delivering current. In normal condition, the voltage V_{BSBR} is regulated by the PFM controller. When the signal V_{BSBR} is lower than 3.8V, the PFM controller turns on the power transistor M_{BP1} at a fixed duty to provide energy for regulating the voltage V_{BSBR}. As a result, the PFM operation can regulate the voltage V_{BSBR} according to load current condition. On the other hand, the BSBR technique is utilized to transfer the charge between the two capacitors C_{Load} and C_{BSBR}. The signal E_{ref} generated by the timing control system defines output voltage level of boost converter as described in Section III. Additionally, when the BSBR power stage is controlled by the BSBR technique, the PFM operation will be disabled until the BSBR tracking algorithm ends the loop.

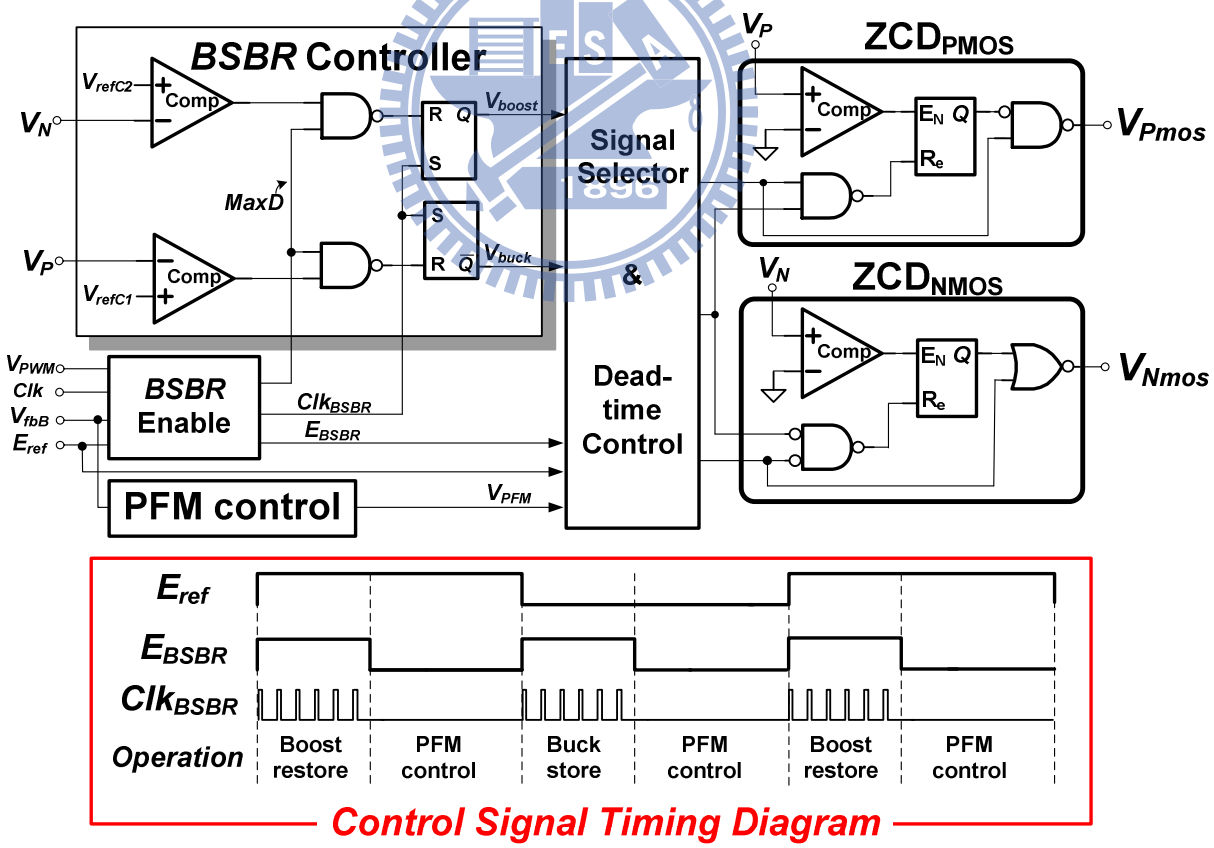


Figure 39. The implementation of the proposed BSBR controller and the control signal timing diagram.

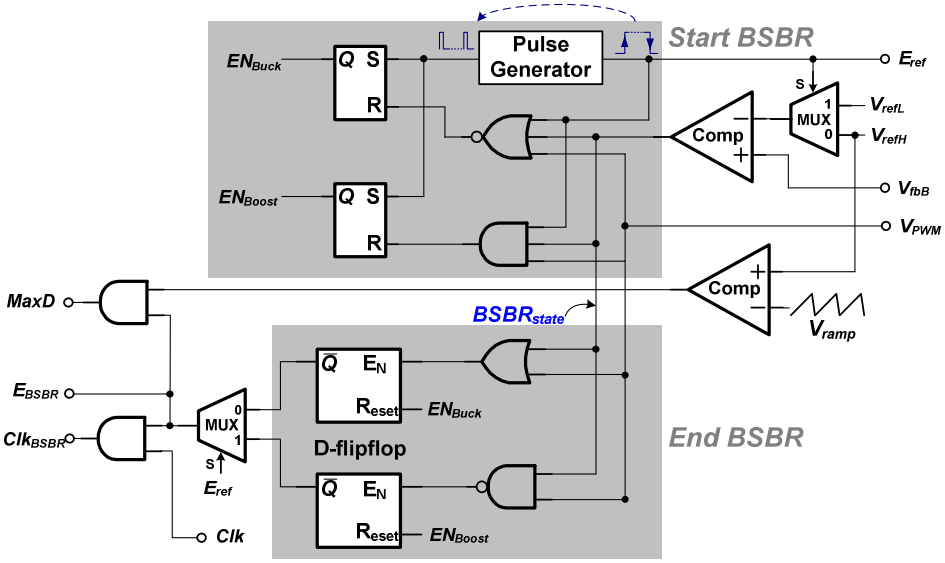


Figure 40. The function block of proposed BSBR Enable circuit.

For the buck-store (down-reference tracking) case, the current-sensing circuits of power transistors M_{BP1} and M_{BN1} illustrated in Figure 37(a) are utilized to act as current limiting and ZCD mechanism, respectively. The transistor M_{BP1} is turned on and then the inductor current is increased to ramp up. The transistor M_{BP1} is turned off when the inductor current exceeds the predefined maximum current. After the dead-time period, the transistor M_{BN1} is turned on to decrease the inductor current. In succession, the BSBR power stage undergoes the switching activities, turning on and off the transistors M_{BP1} and M_{NB1} alternately. Hence, extra charge can be safely and quickly transferred to the BSBR capacitor C_{BSBR}. When the signal V_{PWM} transits from low to high or the V_{BSBR} is higher than the V_{max}, the buck-store algorithm loop is ended. The signal Clk_{BSBR} is disabled and the inductor current will not be increased to ramp up anymore. The remaining inductor current is decreased through the power transistor M_{BN1} to the capacitor. When the reversal of the inductor current happens, the ZCD_{NMOS} is used to turn off the transistor M_{BN1} for alleviating the problem of the reverse inductor current flowing to ground. On the contrary, the function of the ZCD_{PMOS} is disabled to avoid the error digital control signal. For the reference up-tracking case, the boost-restore operation is

selected by the BSBR Enable circuit according to the BSBR algorithm. At first, the BSBR turns on the power transistor M_{BN1} to increase the inductor and then transfers extra charge to the capacitor C_{Load}. Hence, the boost-restore technique senses the n-type power transistor M_{BN1} to decide the discharging time and uses the ZCD_{PMOS} to alleviate the boost converter to provide the unnecessary energy to the capacitor C_{BSBR}. When the signal V_{PWM} is triggered to low or the V_{BSBR} is lower than the voltage V_{min}, the boost-restore operation is completed.

4.2.2 The PWM Generator of the Boost Converter

The PWM generator is the main circuit of the boost converter as shown in Figure 41. The LED backlight driver uses the boost converter to provide enough voltage and current to overcome the forward voltage of series-LEDs. This PWM generator translates all signals to current domain [27] in order to compensate the system without any large external compensation capacitors [34], [41]. The G_m amplifier [29] with high bandwidth characteristic is used to convert the voltage difference between V_{fb} and V_{ref} to a correct current signal according to the output voltage condition. Therefore, the response of this converter can result in fast load/line transient [32] and reference tracking.

Since the LED driver turns on the series-LED after the liquid crystal being rotated to the correct position according to the image data as discussed in Section I, the PWM generator needn't increase the inductor current every switching period. Hence, when the timing control system turns on the LED driver and leads to V_{fb} drop below the reference voltage V_H or V_L, the signal V_{PWM} instead of the clock signal enables the pulse control circuit to turn on the power transistor M_{N1} as described in Figure 37(a).

The reset signal of the PWM signal is determined by three loops. In the normal condition, the current-domain control forms the linear loop composed of G_m amplifier and current comparator to determine the duty ratio. The peak current control uses the current information

of M_{N1} to turn off the M_{N1} preventing the chip from being damaged by large current. Besides, the PWM system applies the maximum duty loop to ensure that the inductor current is transferred to the output during a period. In this proposal, the maximum duty is set as high as 80%. Hence, this three control loops can effectively regulate the boost converter. During the BSBR technique operation, the digital signal E_{BSBR} transits to high and prevents the boost converter from being enabled by the pulse signal of the pulse control. There are two conditions that decide the end of the buck-store algorithm loop.

One condition occurs when V_{BSBR} is higher than the predefined maximum voltage. That is, no extra charge on C_{Load} needing to be transferred to the capacitor C_{BSBR}. The signal V_{PWM} indicates the output voltage information is still in the low level to keep the power transistor M_{N1} off. Once the output voltage drops below the reference voltage V_L, the boost converter starts switching activities to regulate the output voltage. This condition is designed to prevent the chip from being damaged by excess voltage V_{BSBR}. In general, the buck-store algorithm is ended when the signal V_{PWM} transits from low to high to end the buck-store algorithm. Accordingly, E_{BSBR} instantly transits from high to low level to generate the pulse signal V_{pulse} as depicted in Figure 41 and the sequence is shown in Figure 42(a).

Therefore, the boost converter can be immediately controlled by the PWM generator. Similarly, the BSBR technique ends the boost-restore algorithm loop when the output voltage exceeds the high-supplying voltage or the V_{BSBR} is lower than the predefined minimum voltage V_{min}. Nevertheless, some power loss occurs in the procedure of transforming energy. Thus, the boost-restore algorithm loop is usually ended once the V_{BSBR} is lower than V_{min}. In the meanwhile, the signal $BSBR_{state}$ described in Figure 40 transits from high to low level and V_{PWM} is still in the high level. Therefore, the pulse signal from one-shot circuit is immediately generated to turn on the transistor M_{N1} for increasing the inductor current and stepping up the output voltage and the signal sequence is shown in Figure 42(b). As the BSBR technique ends,

the PWM generator can be activated without any delay to avoid the voltage drop and use the peak current control loop to rapidly pull up the output voltage. Therefore, this converter with BSBR technique can quickly track the output voltage that the series-LED need.

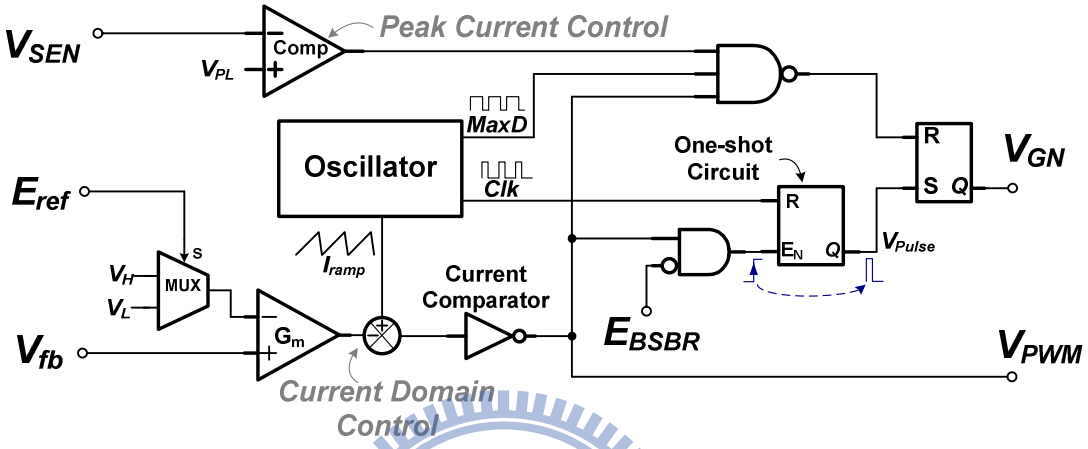
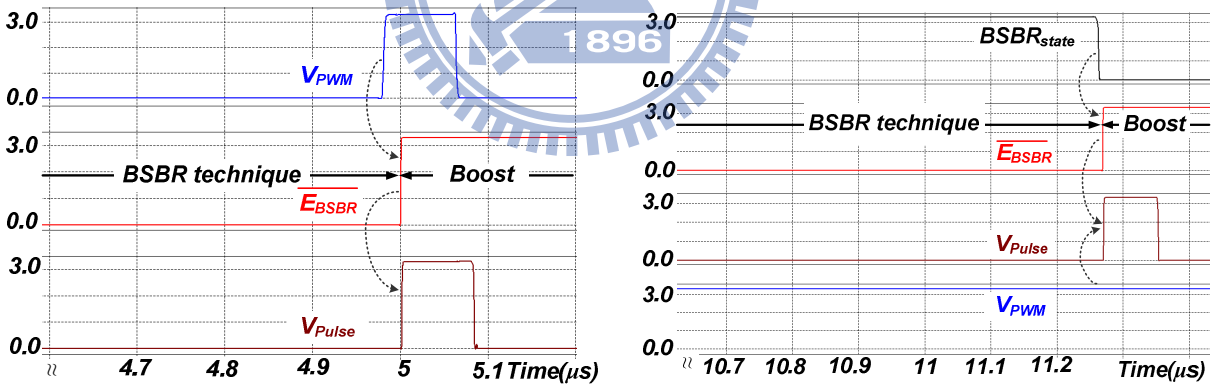


Figure 41. The schematic of the PWM generator with characteristic of fast response and stability.



(a) (b)

Figure 42. The enable sequence of boost converter resulted from the end of BSBR tracking algorithm. (a) The buck-store operation is ended by the signal V_{PWM} . (b) The boost–restore operation is ended by the signal $BSBR_{state}$.

Chapter 5

Measurement Results

5.1 The Measure Result of SAR Methodology

The proposed SAR-controlled adaptive off-time technique for the LED lighting systems was fabricated by the UMC 0.35μm high voltage process. The threshold voltages of n-type and p-type low voltage MOSFET are 0.56 V and 0.79V, respectively. The chip micrograph is shown in Figure 43. The total silicon area including the testing pad is about 1100 μm × 1000 μm. The LED current driver in this technique can operate from 8 V to 40 V and the regulated driving current can be higher at about 1 A. The detailed specifications are listed in Table I.

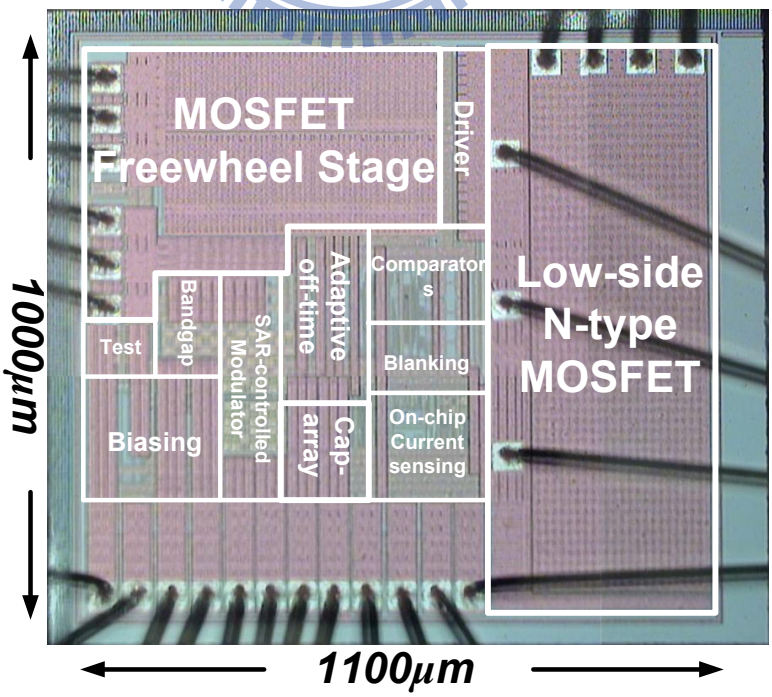
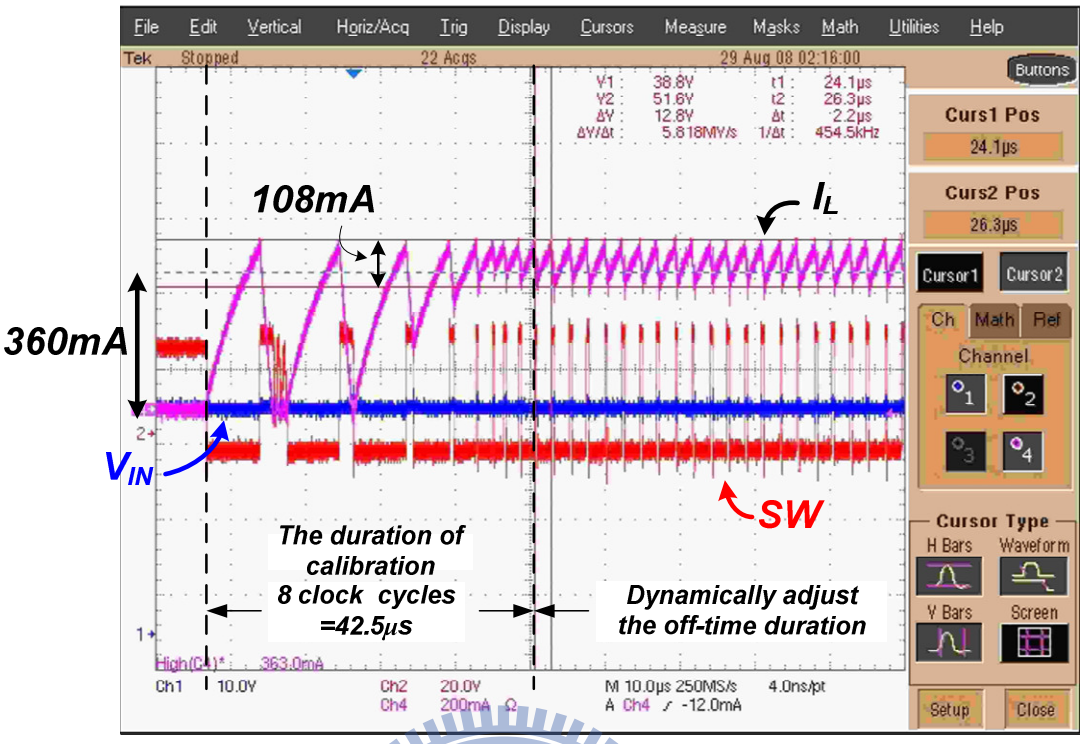


Figure 43. Chip micrograph.

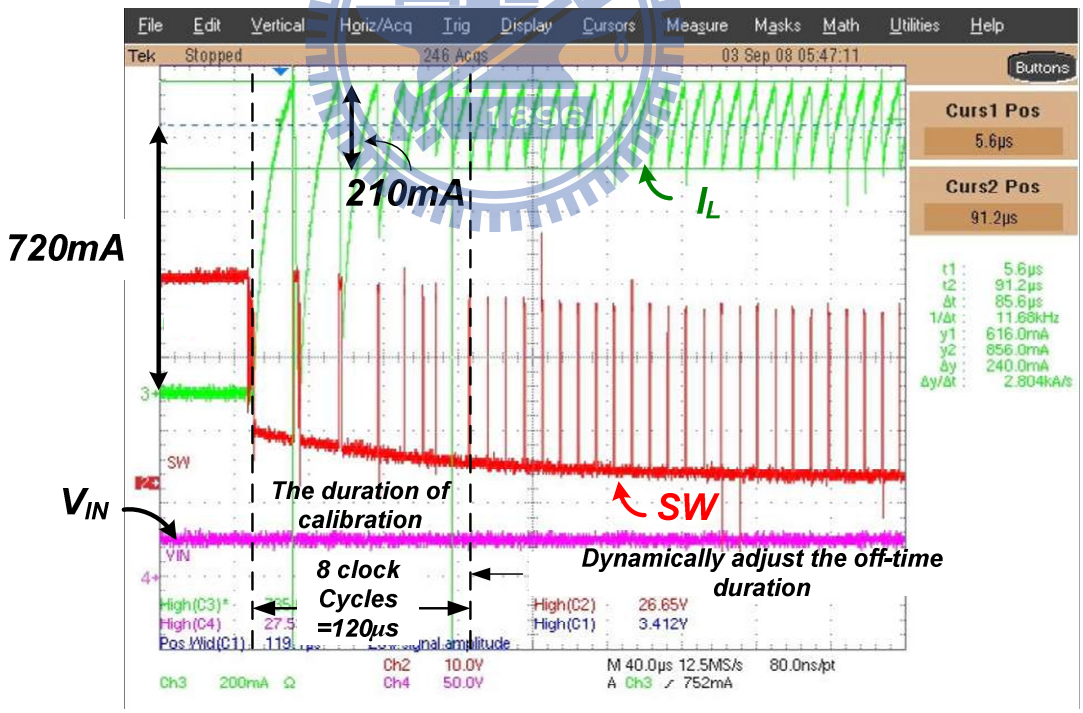
Table I: The Specifications of SAR Methodology

Fabrication Process	UMC 0.35μm high voltage process
Chip area	1100 μm*1000 μm
V_{IN}	8 V to 40 V
Supply Voltage	4V
Quiescent current	0.5 mA
Maximum adaptive off-time	2.5 μs
SW	8 V to 40 V
Inductor	33 μH
Maximum LED Current	1.5A

The on-chip reference voltage can be adjusted to 360 mA and 720 mA and the experimental results are shown in Figure 44 (a) and (b), respectively. The SAR-controlled adaptive off-time technique starts to calibrate the off-time duration once the LED driver is enabled. After eight switching clock cycles, the off-time value is determined and this technique enters the dynamic adjustment stage through the up-down converter. In particular, t_{off} is finely and adaptively adjusted for the variation of the environment after the calibration stage. The calibration times are 42.5 μs and 120 μs when the LED driving currents are 360 mA and 720 mA, respectively. The average inductor currents are adjusted to the predefined values of 360 mA and 720 mA. After the calibration, the ripples of the inductor current (I_L) are adjusted to 108 mA and 210mA peak-to-peak when the LED driving currents are 360mA and 720mA, respectively. The inductor current ripple is approximated to within ±15% of the average inductor current. The switching frequencies of the two load conditions are different because of the adaptive off-time.

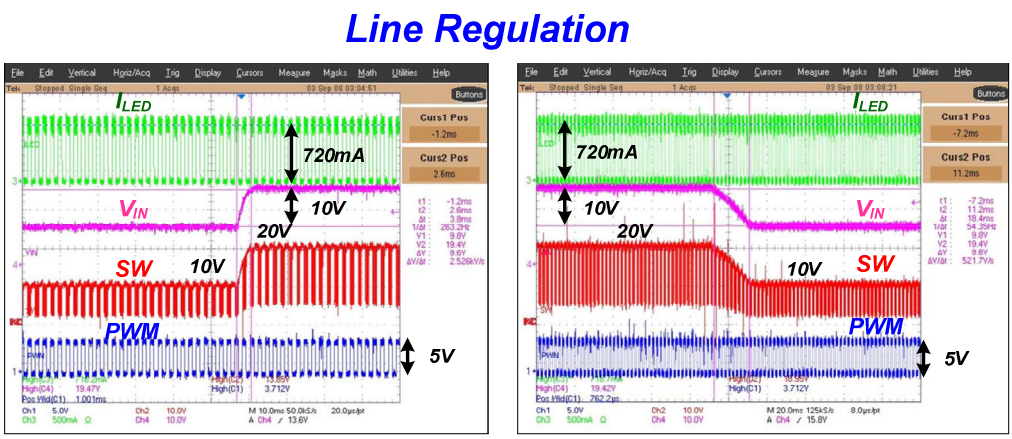


(a)

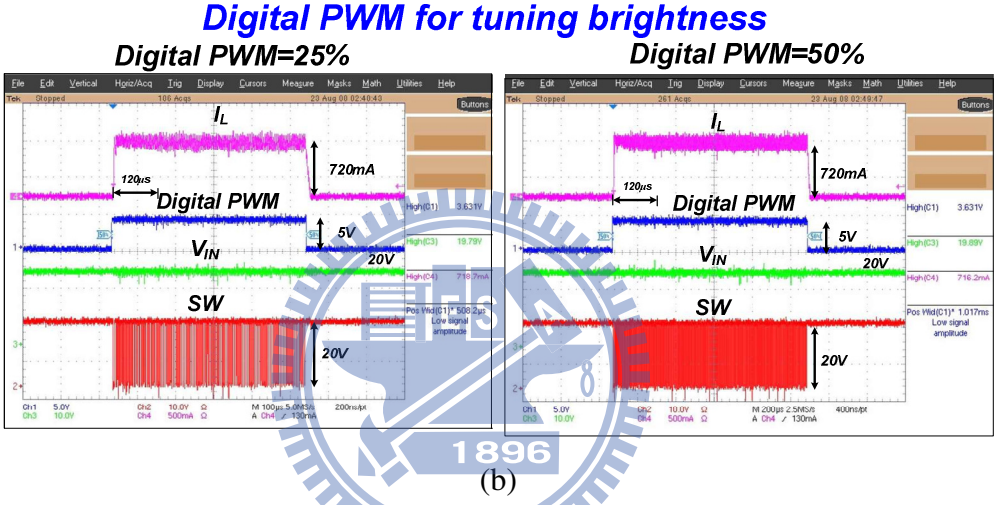


(b)

Figure 44. Experimental results when the LED driving currents are (a) 360mA and (b) 720mA.



(a)

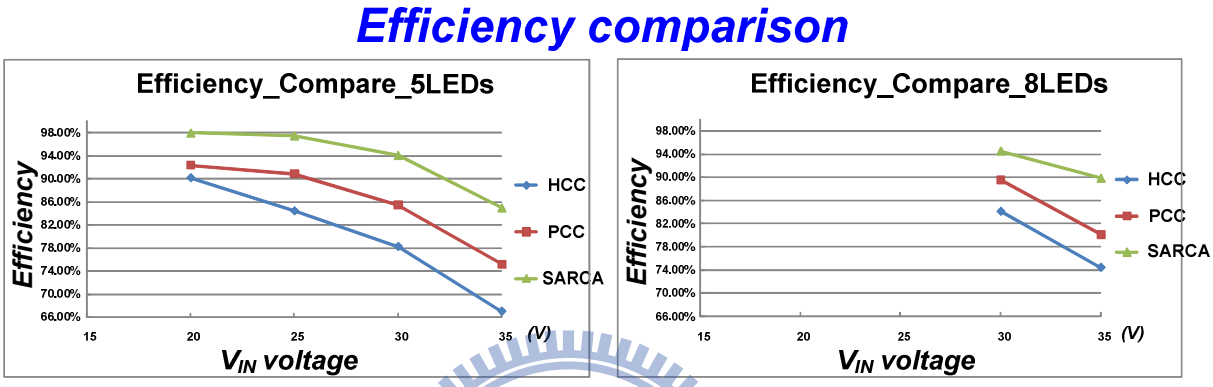


(b)

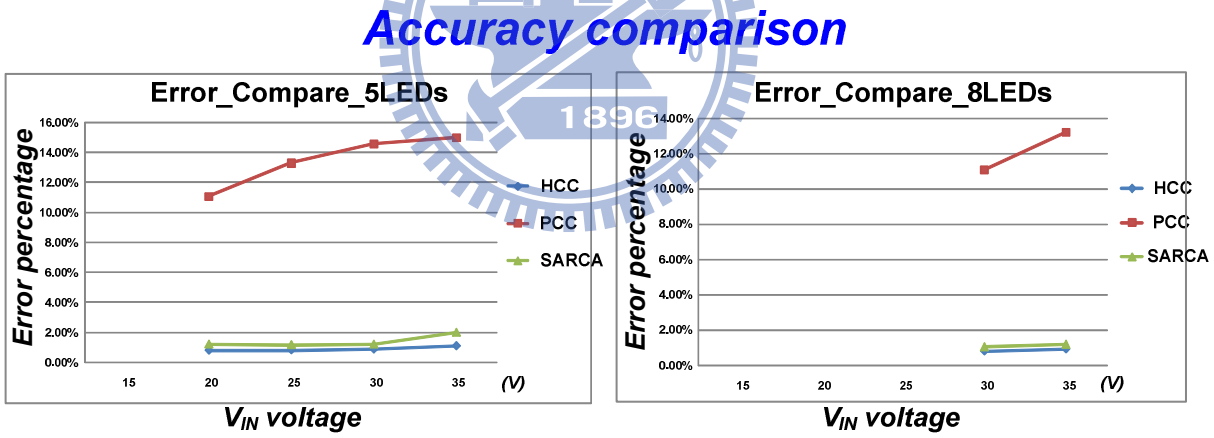
Figure 45. Experimental results. (a) When the duty of the PWM dimming is 50 % and the input supply voltage changes from 10V to 20V or vice versa. (b) The waveforms of the SAR technique when the duties of the digital PWM signal are 25% and 50%.

Fig. 45(a) demonstrates that this technique can rapidly adjust the off-time t_{off} to maintain the LED driving current when the input voltage is increased from 10V to 20V and vice versa. Furthermore, the digital PWM signal is used to adjust the brightness of the LED lighting system at different duties of the digital PWM. The inductor current operates at the defined value when the digital PWM signal is high. In addition, the inductor current is zero when the digital PWM signal is low. Thus, the average output current can be adjusted between 0% and 100% by adjusting the duty ratio of the digital PWM signal. Similarly, when the number of LED is changed, the condition is the same as the test of line transient regulation because the voltage across the inductor is changed and the LED current is kept constant. Fig. 15(b) shows

the experimental results of the inductor current waveforms when the duties of the digital PWM signal are 25% and 50%. The average inductor current is adjusted back to the predefined 720mA after eight switching cycles at the beginning of the digital PWM signal. This technique can effectively adjust the off-time t_{off} back to its accurate value every time when the LED lighting system is turned on.



(a)



(b)

Figure 46. Experiment results (a) The efficiency comparison between the HCC, PCC and SAR techniques. (b) The accuracy comparison between the HCC, PCC and SAR techniques at different input supply voltages.

Figure 46 (a) demonstrates the improvement of the power conversion efficiency compared with the previous designs. The power conversion efficiency is increased by about 8%~15% compared to the HCC method, and by about 5%~8% compared to the PCC method when the LED driver is used to drive 5 to 8 series-LEDs. As shown in Figure 46 (b), the

accuracy of this proposed technique can only keep 1% error percentage compared to that of the HCC technique. However, the error percentage of the PCC method may be larger than 15% under different input supply voltages. In other words, the SAR-controlled adaptive off-time technique can effectively enhance the power conversion efficiency and, at the same time, provide accurate driving current.

5.2 The Measured Result of FRT and CR Technique

The proposed LED driver with CR and FRT techniques was fabricated in 0.25μm TSMC BCD 40V technology and the micrograph of the chip is shown in Figure 47.

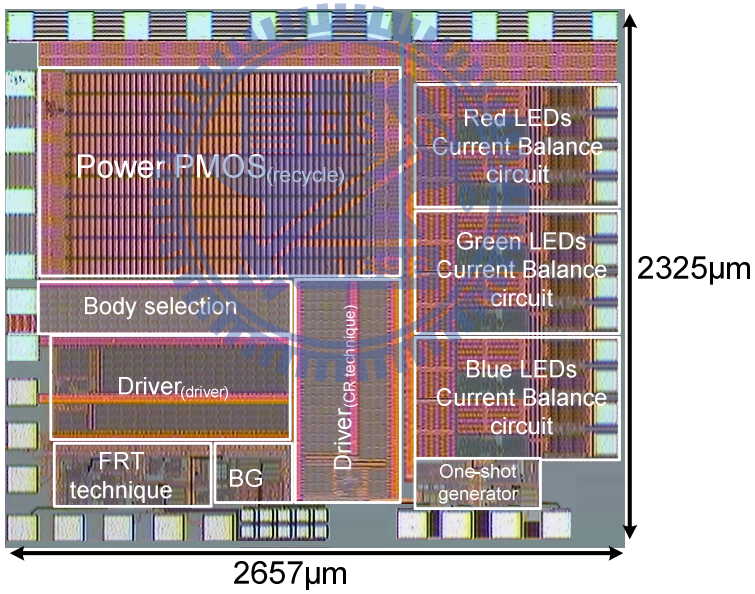


Figure 47. The chip micrograph.

Figure 48(a) shows the one DC-DC converter without the reference tracking technique supply only high-supplying voltage level as 21V to drive all of the R-, G-, and B- LEDs. However, when the backlight module drives the R-LED by such high supplying voltage level, the voltage across the current balance circuit is larger than that during driving the G-/B- LEDs. Therefore, the efficiency of the LED backlight module is deteriorated. The LED driver with

the FRT technique can speed the transient performance of reference tracking, and thereby reducing the power dissipation. However, the up-reference tracking procedure can be quickly achieved due to the FRT technique and the down-reference tracking depends on the output capacitor and load current. Unfortunately, when the value of the load current is small, the output voltage is slowly decreased by the small load current as shown in Figure 48(b), which shows the signal V_{clR} decides the turning on/off of the R-LEDs. The low value of the signal V_{clR} means the output voltage needs to be low-supplying voltage level as 16V. On other hand, the high value of the signal V_{clR} means the output voltage needs to be high-supplying voltage level as 21V. Therefore, when the LED driver operates at light loads, large output voltage across the current balance circuit causes much power dissipated in the constant current regulator. Certainly, the extra energy is always dissipated on the current balance circuit at any load condition.

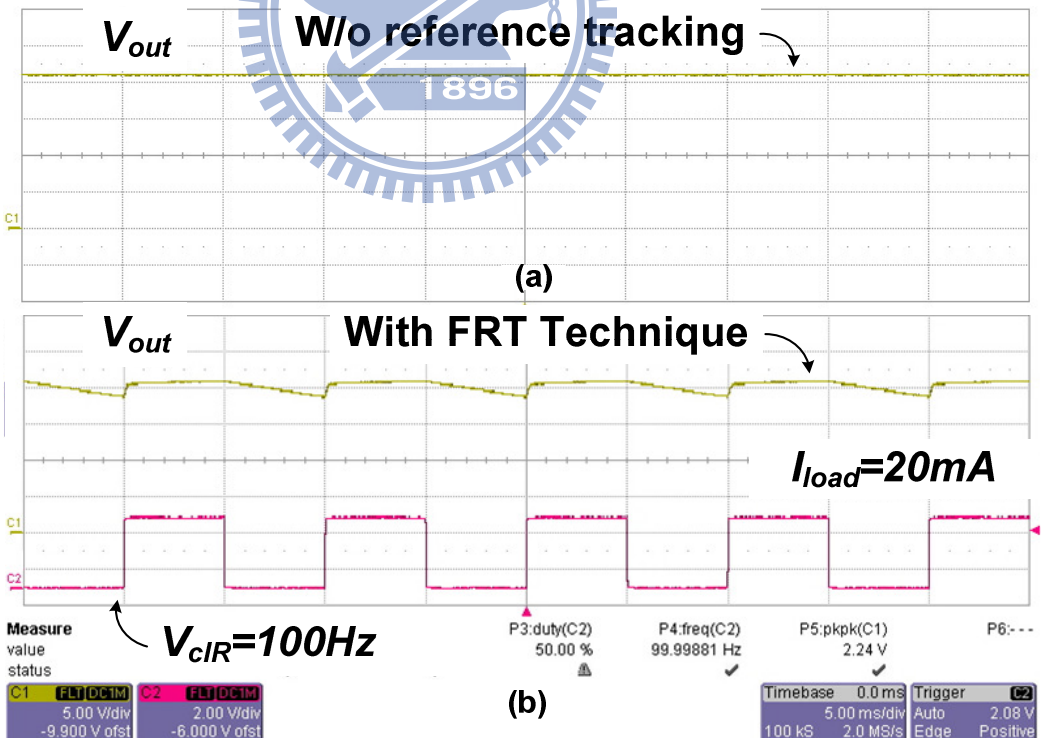


Figure 48. (a) The waveforms of the LED driver without reference tracking technique. (b) The waveforms of the LED driver with the FRT Technique.

The proposed CR technique can reduce the power consumption on the constant current regulator circuit and increase the efficiency of the LED driver. The waveforms of LED driver with CR and FRT techniques can effectively speed the up- and down- reference tracking procedures as shown in Figure 49. Therefore, the CR technique can save much extra energy on the recycling capacitor $C_{Recycle}$ and the detail waveform of CR and FRT techniques is shown in Figure 50.

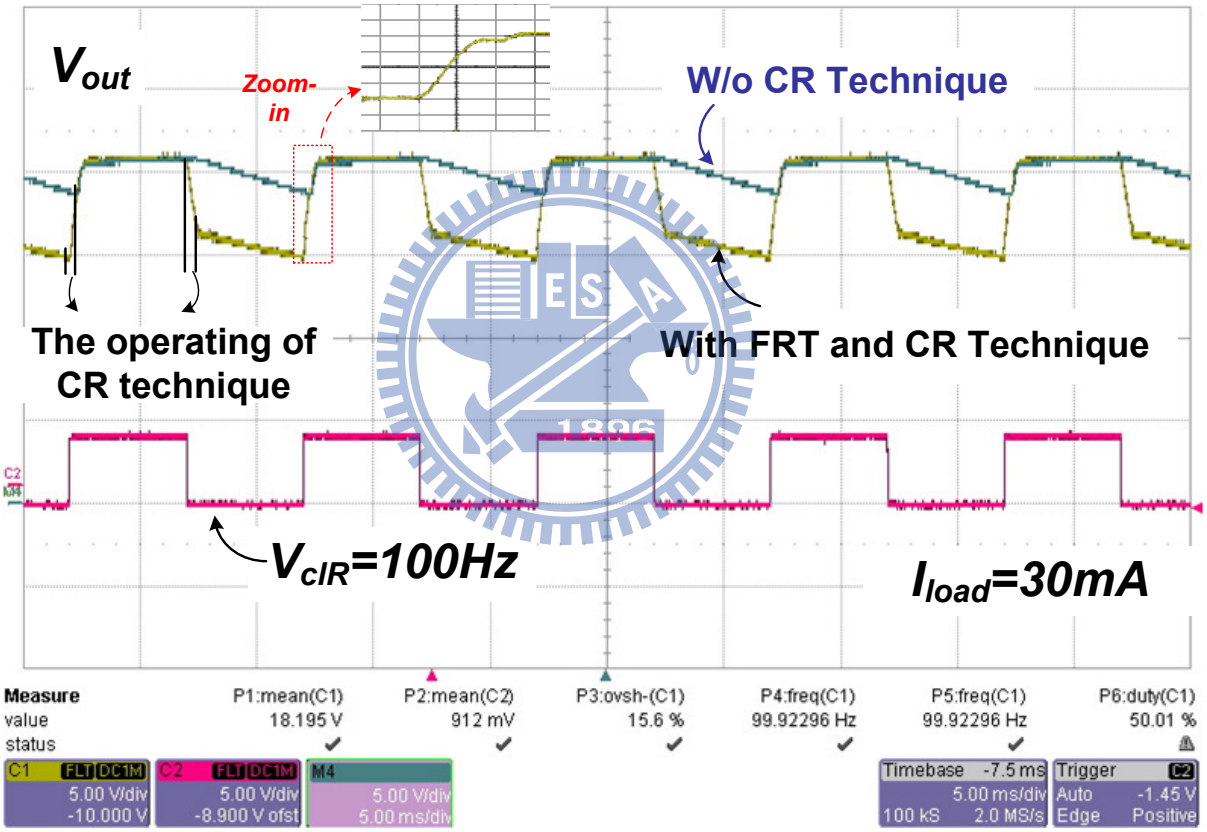
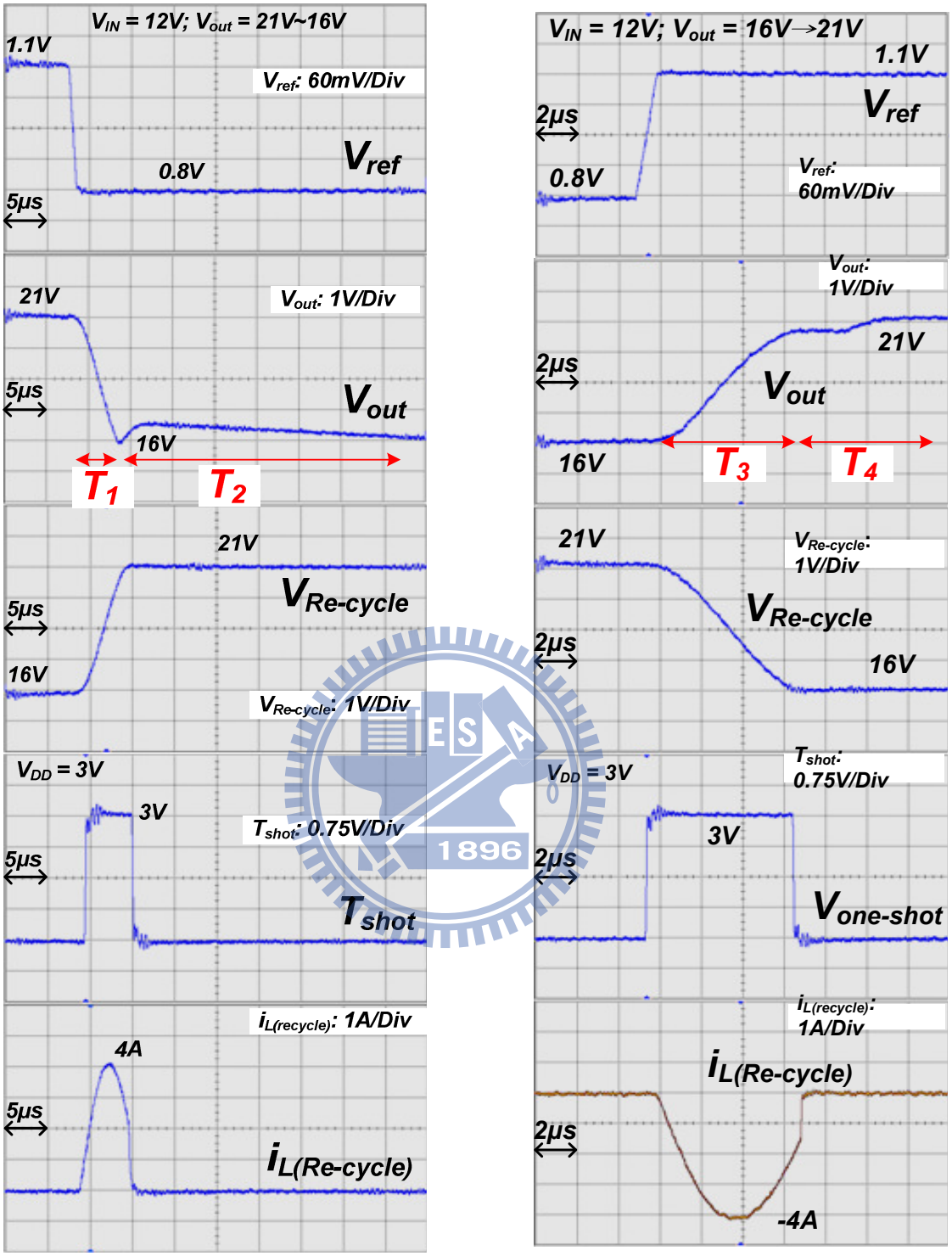


Figure 49. The waveforms of the LED driver with or without the FRT and CR techniques.

When the output voltage changes from high-supplying voltage level for G- or B- LED to low-supplying voltage level for R- LEDs, the one-shot generator sends the signal T_{shot} to turn on the power transistor M_{p1} for transmitting energy from C_{load} to $C_{Re\text{-}cycle}$. The duration of the signal T_{shot} is approximated to 7μs as shown in Figure 21(a). Simultaneously, the $I_{L(Re\text{-}cycle)}$

transmits energy from the output capacitor C_{load} to the re-cycling capacitor $C_{Re\text{-}cycle}$ at time T_1. Thus, the output voltage V_{out} can be rapidly decreased from 21V to 17V within time T_1. The value of T_1 about 7μs is faster than other conventional structure. Furthermore, the recycling voltage $V_{Re\text{-}cycle}$ is also raised from 17V to 21V because the extra charge is high efficiency to store on re-cycling capacitor $C_{Re\text{-}cycle}$. Thus, the fast response from high- to low-supplying voltage level is demanded for achieving high performance of the FCS technique. And then the settling time T_2 depends on the value of the output capacitor C_{load} and load current. The output voltage is pulled down to near 17V after the period T_1. This voltage level is enough to drive the 6 series R-LED with minimized power loss since the voltage stress across the current balance unit is smaller that of the high supplying level as 21V. But the CR technique also dissipates power due to the conduction loss. However, the efficiency still can be improved due to low conduction loss during the short storing/restoring time. When the low-supplying voltage level steps to high-supplying voltage level, the signal T_{shot} is sent to transferred the re-cycling energy on the $C_{Re\text{-}cycle}$ back to the output capacitor C_{load} for rapidly raising the output voltage V_{out} to the regulated voltage. Thus, Figure 21(b) shows the reversing current $I_{L(Re\text{-}cycle)}$ from $V_{Re\text{-}cycle}$ to V_{out} at time T_3. The output voltage V_{out} gets stored energy from the CR technique of the LED driver at time T_3 about 7μs. Thus, the extra energy stored on the re-cycling capacitor $C_{Re\text{-}cycle}$ is efficiently used to speed the up-reference tracking procedure. After the period T_3, the FRT technique is used to regulate the output voltage V_{out} to the high-supplying voltage level, which is 21V, within time T_4.

The load regulation is shown in Figure 51, the value of load regulation is 0.5mV/mA when input voltage V_{in} is 12V and the output voltage V_{out} is 21V. The load transient time is only 10μs when variation of load current is about 80mA. It is obvious to find that the load regulation is improved [18] and the transient response time is short due to the FRT technique. The line regulation is shown in Figure 52, the value of line regulation is 1.36mV/V when the



(a) (b)

Figure 50. (a) When V_{ref} changes from 1.1V for G- or B- LED to 0.8V for R-LEDs, the extra energy is stored in the auxiliary inductor $L_{(Re\text{-}cycle)}$ and capacitor $C_{Re\text{-}cycle}$, which is triggered by the one-shot generator. (b) When V_{ref} changes from 0.8V for R-LED to 1.1V for G- or B-LEDs, the extra energy stored in the auxiliary inductor $L_{(Re\text{-}cycle)}$ and capacitor $C_{Re\text{-}cycle}$ is released to the output node V_{out}, which is also triggered by the one-shot generator.

output voltage V_{out} is 21V and load current I_{load} is 100mA. Similarly, the recovery time of the line transient response is decreased within 10μs. The For a conventional boost converter design with PI compensation, it is very hard to decrease the line/load transient response time within 10μs. Figure 53 shows comparison of the power consumption between LED driver with or without CR and FRT technique. The LED driver without FRT and CR techniques always supplies 21V and thereby the power still waste on the current balance circuit when the backlight module turn on the R-LEDs. However, the driver with FRT technique can reduce the power loss due to the small voltage across the current balance circuit. Furthermore, the proposed driver with FRT and CR techniques can reduce the power consumption and efficiently enhance reference tracking performance. When the RGB LED backlight module with FCS algorithm drives 12-branches LED and each branch consumes 20mA, the LED driver without FRT and CR techniques consumes 1.04W. However, the LED driver with the FRT and CR techniques switches different voltage level and consumes only 0.252W. The power saving can achieve 0.788W if the LED driver utilizes the proposed CR and FRT techniques. In addition, when the LED driver drives the one branch of the LED array, the current balance circuit consumes a little power. That is, the difference power consumption with or without CR and FRT technique is smaller than that of driving many branches of the LED array. The reason is the quiescent current of the LED driver dominates most of the power loss in driving one branch of the LED array. However, after the implementation of the CR and FRT techniques, the power consumption on the current balance circuit still can be reduced. Furthermore, the transient response is also speeded up due to the restored charge by the CR technique. The performance summary of FRT and CR technique is listed in Table II.

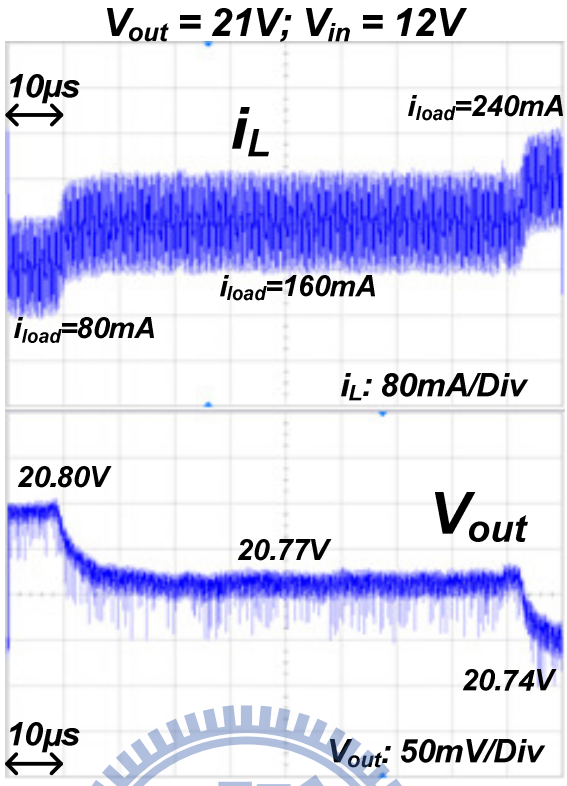


Figure 51. Load regulation when load current changes from 80mA to 240mA.

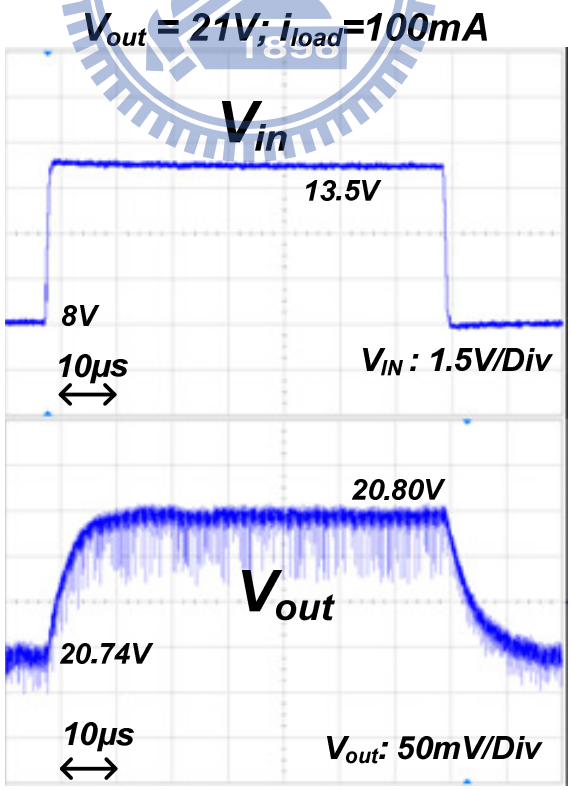


Figure 52. Line regulation when input voltage changes from 8V to 13.5V and back to 8V when load current is 80mA.

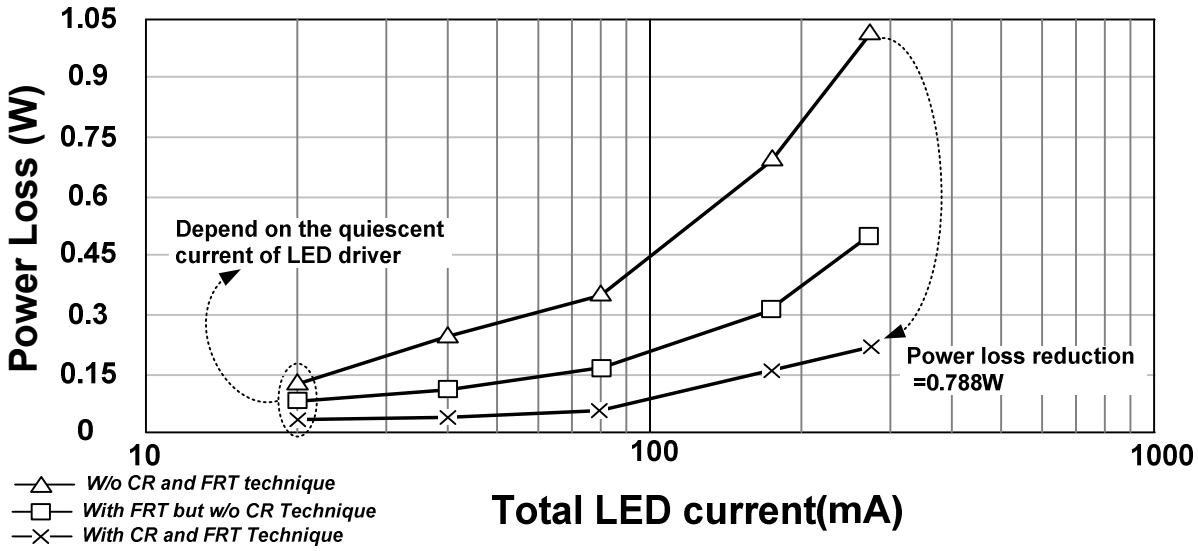


Figure 53. Measured power loss of the LED driver with or without the FRT and CR techniques.

Table II: Performance Summary of FRT and CR Technique

Fabrication Process	TSMC 0.25μm BCD 40V 1P5M
Chip Area	6.178 mm^2(2325μm*2657μm)
Supply Voltage (V_{in})	8-13.5 V
Output Voltage (V_{out})	16-30 V
Switching Frequency	1.5 MHz
Maximum Load Current	300 mA
Inductor / Capacitor	L=10 μH, $L_{Re\text{-}cycle}$=2.2 μH / C_{load}=4.7 μF, $C_{Re\text{-}cycle}$=4.7μF
Load Regulation	0.5mV/mA@V_{in}=12V, V_{out}=21V
Line Regulation	1.36mV/V@V_{out}=30V, I_{out}=80mA
Maximum CR Current	4A
Reference Tracking Speed	12us for 17V → 21V with I_{load} = 20mA 1ms for 21V → 17V with I_{load} = 20mA

5.3 The Measure Result of BSBR Technique

The chip containing the boost converter and BSBR technique was fabricated in a 0.25μm BCD process and Figure 54 shows a die micrograph of the implement with the die area is 4.03mm^2 which the BSBR controller only occupies 0.072 mm^2. The maximum allowable voltages for drain-source voltage and gate-source voltage are 40V and 12V, respectively. The developed prototype is shown in Figure 55. Table III summarizes the design parameters and the measurement results.

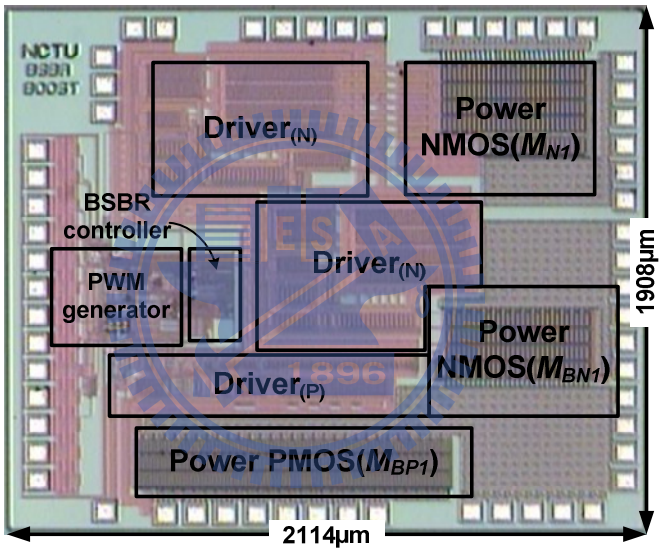


Figure 54. Chip micrograph.

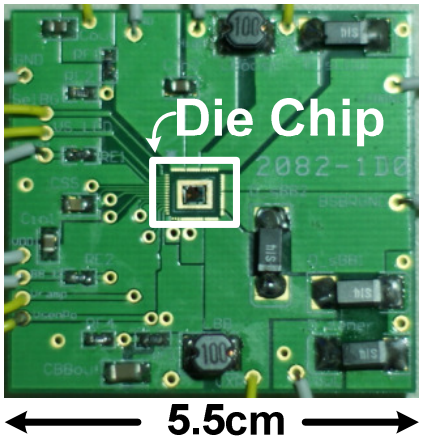


Figure 55. The prototype for testing the RGB LED driver with the BSBR technique.

Table III: Chip Features of BSBR Technique

Fabrication Process	0.25μm BCD 40V 1P5M (Maximum V_{DS} = 40 V and V_{GS} = 12 V)
Chip Area	4.03 mm^2(1908 μm×2114 μm)
Supply Voltage (V_{in})	3.3-6 V
Output Voltage (V_{out})	9-15 V
Control Voltage (V_{DD})	3.3 V
Switching Frequency	1 MHz
Maximum Load Current	300 mA
Inductor	L=10 μH, L_{BSBR}=10 μH
Capacitor	C_{Load}=1 μF, C_{BSBR}=10 μF
Maximum Efficiency of Charge Recycling	94%
Maximum Efficiency of Boost Converter	94.5%
Reference Tracking Speed	20 μs for 9.3V→12.4V with I_{Load}=100mA 10 μs for 12.4V→9.3V with I_{Load}=100mA

The prototype working with input voltage ranging from 3.3~6 V is applied to the RGB LED backlight module with FCS technique and thus the boost converter steps up the output voltage to 9.3 V for 4 series R-LED and 12.4 V for 4 series G- or B-LEDs. The values of the inductors L and L_{BSBR} are both chosen as 10μH. The values of the capacitors C_{Load} and C_{BSBR} are chosen as 1 μF and 10 μF in this proposal. Besides, the voltage V_{BSBR} is regulated around 3.8 V to turn on white-LED implemented on the flashlight of the portable device. However, the capacitor C_{BSBR} can be chosen to be any types of capacitors according to different applications. The frequency of the FCS technique usually utilizes the 60 Hz or 50 Hz switching frequency to switch different color LEDs. Nevertheless, in order to ensure the functionality and reliability of the developed prototype, a higher switching frequency (3 kHz) is utilized to test the performance and observe the response of the reference tracking procedure as shown in Figure 56. The output voltage is dynamically stepped up to 9.3 V and 12.4 V according to the digital signal E_{ref} from the FCS technique when the load current is 100mA. For reference down-tracking response, the output voltage without BSBR technique drops slowly and causes large power consumption on the constant current generator. However,

the output voltage with BSBR technique can transfer extra charge to the capacitor C_{BSBR} so that the period of reference down-tracking is smaller than 10 μs and 5X faster than that of the traditional converter when load current is 100mA. Furthermore, extra charge stored on the capacitor C_{BSBR} is more efficient than prior art [18], [40], and [42]. Therefore, the voltage V_{BSBR} is raised from 3.8 V to 4.09 V under no-load situation when the boost converter changes the output voltage level to turn on the R-LEDs. On the contrary, when the output voltage is raised from 9.3 V to 12.4 V, the boost-restore technique is enabled to transfer the stored charge back to the capacitor C_{load}. Until the voltage V_{BSBR} is smaller than 3.8 V, the boost-restore technique is disabled. In succession, the boost converter continues to step up the output voltage to the desired voltage, 12.4V. As shown in Figure 56, the output voltage has two different rising slopes when the output voltage is stepping up from 9.3V to 12.4V. The first slope is controlled by the BSBR technique and the second one is by the boost converter. Since the BSBR technique uses the smaller transforming current for reducing the power consumption, the first slope is smaller than the second one. However, the up-tracking response is smaller than 20 μs and fast enough for the FCS technique. Furthermore, the maximum efficiency of the extra charge recycling can be up to 94%.

Figure 57 shows the measured waveforms of the BSBR power stage with 80mA load current. Because the forwarding voltage of white-LED is close to 3.5V, the voltage V_{BSBR} must be set above 3.7V. Therefore, the PFM control and BSBR techniques are used to regulate V_{BSBR} to be 3.8V in this application. When the output voltage drops from 12.4V to 9.3V, the BSBR technique is enabled to transfer the extra charge and thus the voltage V_{BSBR} is instantly increased owing to buck-store technique. When the buck-store technique is disabled, the PFM control technique continues to regulate the voltage V_{BSBR}. However, when the output voltage rises from 9.3V to 12.4V, the boost restore technique is still enabled at first. As mentioned before, the technique is disabled when the voltage V_{BSBR} is lower than 3.8V and

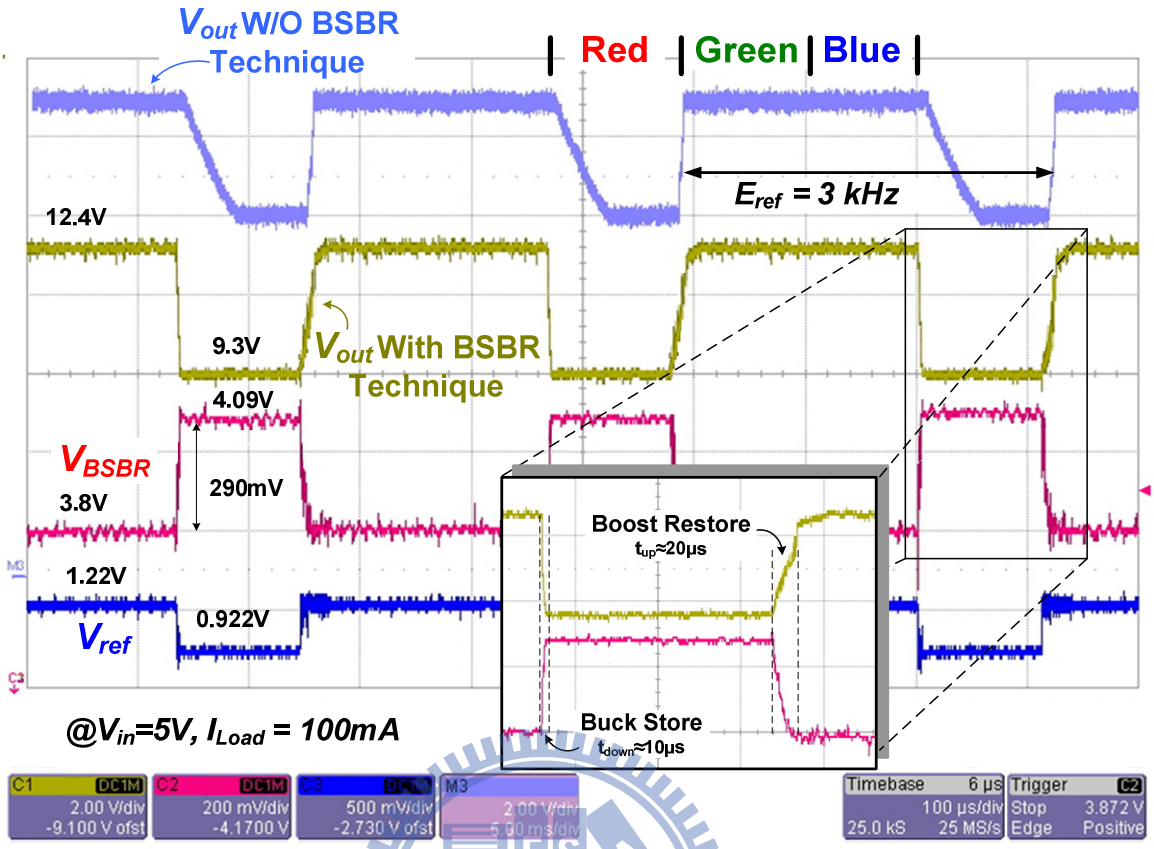


Figure 56. Measured waveforms for reference tracking response with/without BSBR technique.

then the BSBR power stage is controlled by the PFM operation. Figure 58 shows the measured efficiency of boost converter under different load current with and without BSBR technique when input voltage is 5V. The effective efficiency of LED backlight driver composed of boost converter and constant current generator is calculated as (42).

$$\eta_{LED\_driver} = \eta_{boost} \times \frac{V_{LED}}{V_{out}} \tag{42}$$

The V_{LED} is the total voltage of the string LED and the V_{out} is the output voltage of the boost converter as illustrated in Figure 7. The η_{LED_drver} indicates the efficiency of the LED driver. In addition, the η_{boost} indicates the efficiency of the boost converter. Thus, the efficiency of LED backlight module with BSBR technique can be improved by 8%. Figure 59 (a) and (b) show the measured efficiency the boost converter versus load current under different input voltages when output voltages are 9.3V and 12.4V, respectively. The efficiency

measurement is setup by the power supply and electron load. When the electron load is connected with the prototype, the power supply would show the input voltage and input power. The input power P_{in} can be calculated by multiplying the input current and input voltage. And the electron load also show the output current and output voltage. The output power P_{out} also can be calculated by the output current and output voltage. Thus, the efficiency of boost converter can be measured through output power P_{out} divided input power P_{in}. The charge recycling efficiency is calculated by the transmission ratio. The output of CR power stage should be pulled up about 5 V. The measured result is about 4.5 V. The efficiency of CR technique is about 90%. And the output of BSBR power stage should be pulled up 310 mV and measured result are about 290 mV. Thus, the efficiency is about 94%. Moreover, the BSBR power stage not only can operate the buck-store and boost-restore techniques for reference tracking performance but also can supply the regulated voltage V_{BSBR} by the PFM operation technique.

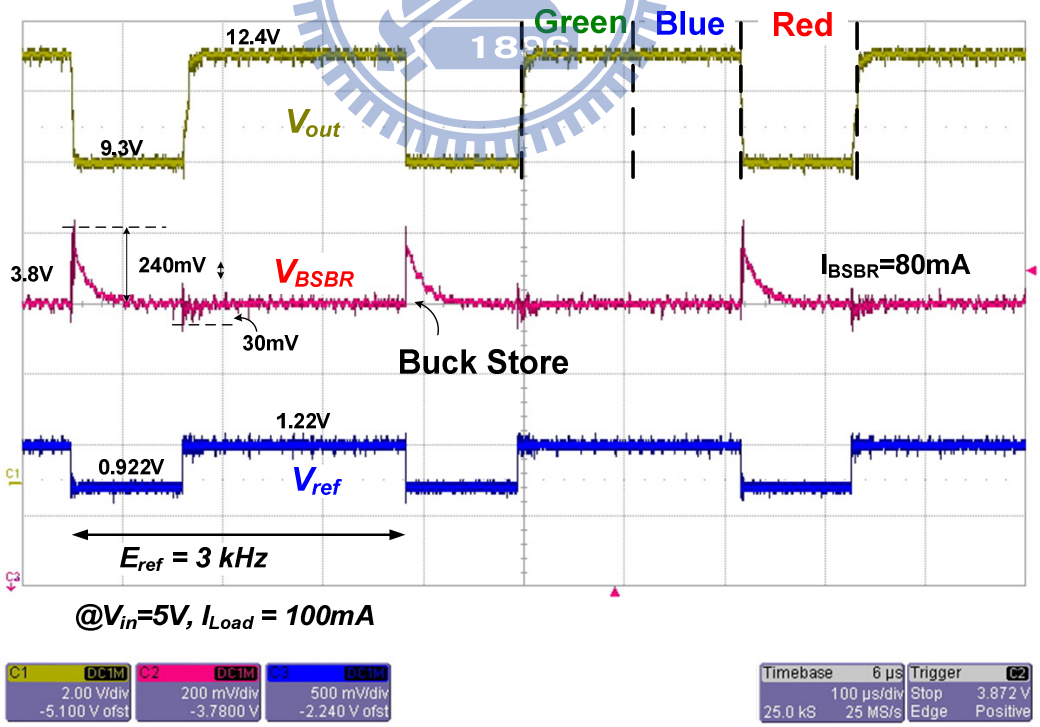


Figure 57. Measured waveforms showing the BSBR power stage with 80mA load current (I_{BSBR}) for forwarding white-LED. The PFM control and BSBR techniques are used to maintain the voltage V_{BSBR} above 3.8V.

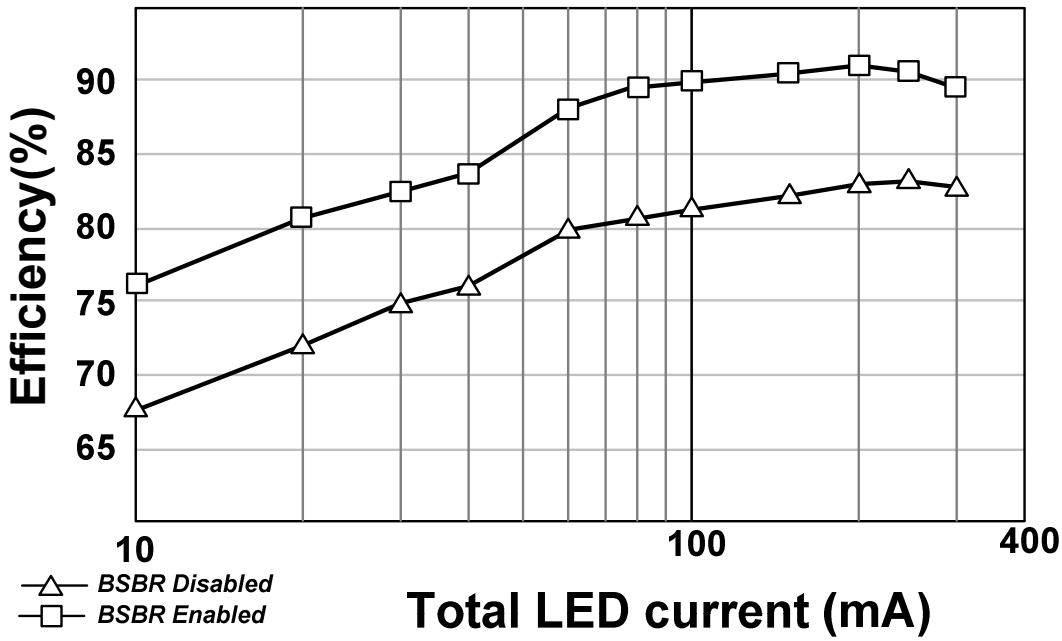
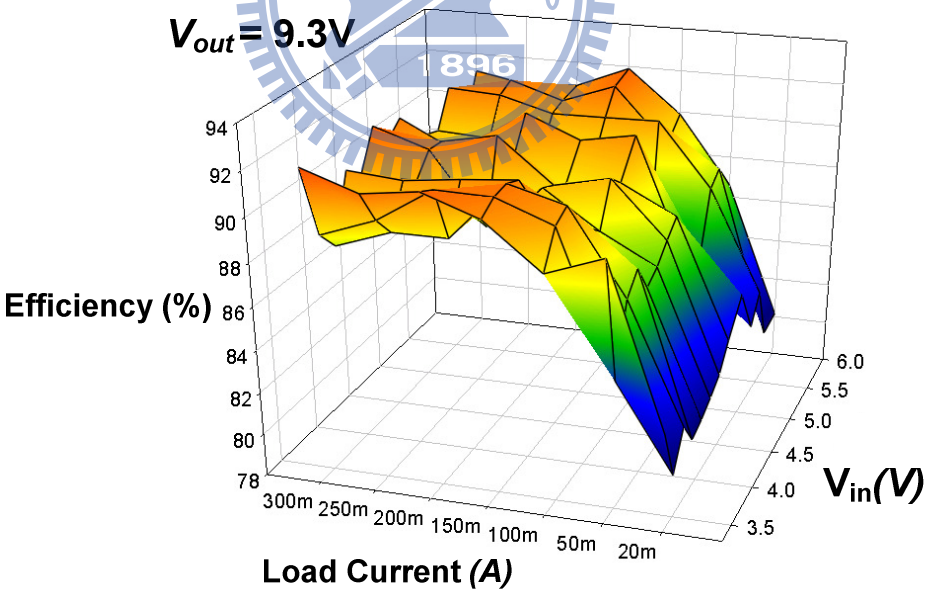
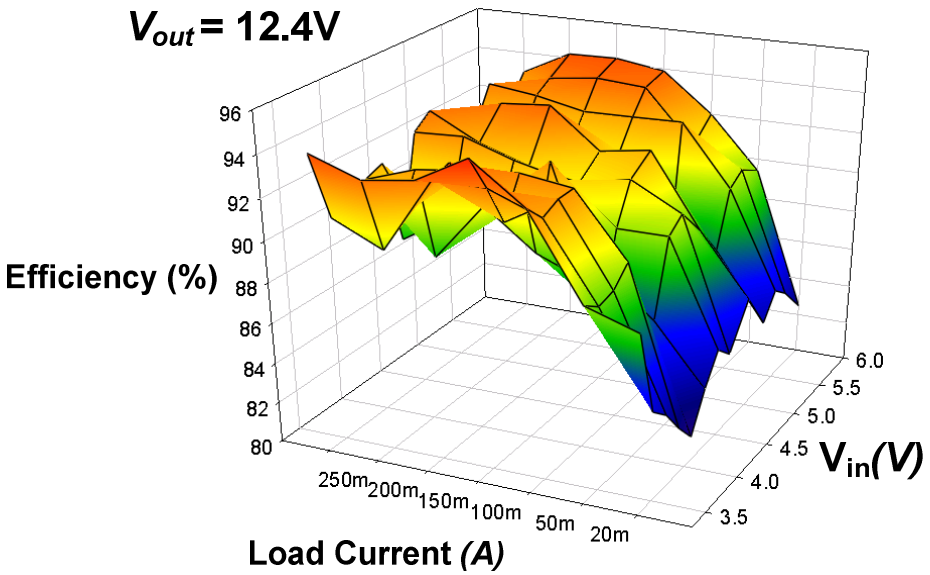


Figure 58. Measured efficiency of the boost converter with and without BSBR technique enabled under different load current when input voltage is 5V.



(a)



(b)

Figure 59. Measured efficiency of the boost converter versus load current under different input voltages are illustrated (a) when output voltage is 9.3V and (b) when output voltage is 12.4V.

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Chapter 6

Conclusions and Future Works

6.1 Conclusions

The prior arts of the LED drivers such as the PCC and HCC methods have shown a trade-off between efficiency and accuracy. In this thesis, the LED driver with the SAR-controlled adaptive off-time technique is proposed to achieve high accuracy and efficiency at the same time. According to the operation of this technique, the average inductor current can be adjusted to a constant value. The on-chip low-side current sensing method and the active diode can greatly improve efficiency. Thus, this topology achieves 94% efficiency and 98% accuracy. The power efficiency is increased to about 8%~15% compared to the HCC method and to about 5%~8% compared to the PCC method. The SAR-controlled adaptive off-time technique can be widely used in LED lighting systems with PWM dimming control.

Moreover, the constant current regulator for the RGB backlight module requires the DC-DC converter with fast reference tracking technique. A RGB LED backlight driver is proposed for rapidly switching between driving 6-series R (about 16V) and 6-series G/B LED (about 21V). Owing to voltage difference about 5V between driving series-R and series-G/B LEDs, the FRT technique is presented to enhance line and load regulations. Besides, the CR technique stores extra energy on the re-cycling capacitor at the transition from high-suuplying voltage (21V) to low-supplying voltage (16V). On other hand, it can restore the energy back to output node to speed up the raising of voltage back to 21V at the stage of driving G/B LEDs. Both the transient response time and efficiency are enhanced. The proposed LED

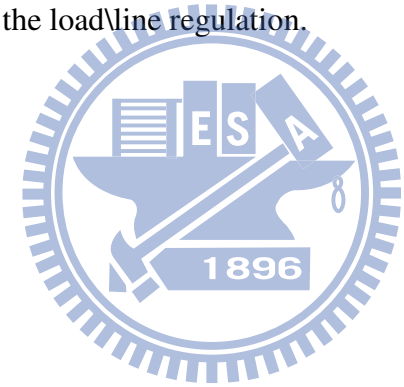
driver with the FRT and CR techniques was implemented in 0.25μm TSMC BCD 40V technology. Experimental results show that the load transition time can be reduced within 10μs and the line transient response time can be reduced within 10μs. It demonstrates the fast reference tracking performance achieved by the proposed FRT technique. The power consumption of the backlight module in the implementation of the field color sequential (FCS) algorithm is smaller than 3W. Furthermore, the power loss due to the LED driver can be effectively reduced to about 24% of the LED driver without CR and FRT techniques. The proposed LED driver with the FRT and CR techniques can improve the reference tracking performance and reduce the power loss.

In addition, another innovative control mechanism, the BSBR technique, is proposed to enhance the reference-tracking response and reduce the power consumption of the LED backlight module. The proposed BSBR technique can store extra charge on the output capacitor to the recycling capacitor when the output voltage transits from high-supplying voltage (12.4V) to low-supplying voltage (9.3V). As a result, the power dissipation on constant current generator can be considerably improved. On the other hand, when the output voltage level is changed from low- to high-supplying voltage, the charge stored on the recycling capacitor can be used for raising the output voltage back to the high-supplying voltage level. Therefore, extra charge can be recycled and the overall power consumption of the backlight module can also be reduced. In addition, the regulated voltage can be utilized to implement other applications such as turning on white-LED on the portable devices.

6.2 Future Works

The proposed charge-recycling (CR) and buck-store/boost-restore (BSBR) technique can store extra charge on the output capacitor to the recycling capacitor when the output voltage transits from high-supplying voltage for turning on the G- B-LED to low-supplying voltage

for turning on the R-LEDs. As a result, the power dissipation on constant current generator can be considerably improved. In addition, these techniques also can reduce the numbers of output component to improve the PCB area. However, these two techniques still require the external large capacitor and inductor to achieve the performance of fast reference tracking. In order to have future works on the reference tracking, furthermore simplify the driving module and reduce more power consumption of the FCS-LCD backlight module can be continuously studied. The BSBR and CR technique can be based on a synchronous boost DC-DC converter. In addition, there are many challenges on the studies of reference tracking technique. Such as that the new control algorithm for reducing chip area and power consumption, the fast transient technique for stepping load transition, a new controlling error amplifier or compensator for improving the load\line regulation.



References

[1] Yi-Fu Chen, Che-Chin Chen, and Ke-Horng Chen, "Mixed Color Sequential Technique for Reducing Color Breakup and Motion Blur Effects," *IEEE/OSA Journal of Display Technology*, pp. 377-385, Dec. 2007.

[2] T. Shirai, S. Shimizukawa, T. .Shiga, S. Mikoshiba, and K. Kalantar, "RGB-LED Backlights for LCD-TVs with 0D, 1D, and 2D Adaptive Dimming," *Society of Information Display,* 2006 Dig. 44.4, pp. 1520–1523.

[3] K. Käläntär, T. Kishimoto, K. Sekiya, T. Miyashita, and T. Uchida, "Spatio-Temporal Scanning Backlight for Color-Field Sequential Optically Compensated Bend Liquid-Crystal Display," *Society of Information Display,* 2005 Dig. 36.3, pp. 1316–1319.

[4] A. Yohso and K. Ukai, "How Color Break-up Occurs in the Human Visual System: Mechanism of Color Break-up Phenomenon," *Society of Information Display,* 2006 Dig. 25.2, pp. 1223–1228.

[5] R. Van Dijk and J. A. Shimizu, "A System and Method for Motion Compensation Image Planes in Color Sequential Displays," U.S. Patent 6 831 948, Dec. 14, 2004.

[6] Datasheet "3508 White SMD LED," Light House Technology Co., LTD.

[7] Datasheet "MAX16807/MAX16808: Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller," Maxim Integrated Products, Inc.

[8] O. Ronat, P. Green and S. Ragona, "Accurate Current Control to Drive High Power LED Strings," *IEEE Applied Power Electronics Conference*, 2006, pp.376-380.

[9] Doshi, Montu, Zane, and Regan, “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM” *IEEE Applied Power Electronics Conference,* 2007, pp.287-393.

[10] C.-C. Chen, C.-Y. Wu and T.-F. Wu, “LED Back-Light Driving System for LCD Panels,” in *Proc. IEEE Applied Power Electronics Conference*, 2006, pp.381-385.

[11] Yogesh K. Ramadass and Anantha P. Chandrakasan, “Minimum Energy Tracking Loop with Embedded DC-DC Converter Enabling Ultra-Low-Voltage Operation Down to 250 mV in 65 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1,pp. 256-265, January 2008.

[12] Datasheet “1206 RGB SMD LED,” Light House Technology Co., LTD.

[13] Baddela, S.M., and Zinger, D.S, “Parallel Connected LED Operated at High Frequency to Improve Current Sharing,” *IEEE Industrial Application Society*, 2004, vol. 3, pp.1677- 1681.

[14] In-Hwan Oh, “A Single-Stage Power Converter for a Large Screen LCD Back-Lighting,” in *Proc. IEEE Applied Power Electronics Conference*, 2006, pp.1058-1063.

[15] Huang-Jen Chiu and Shih-Jen Cheng, “LED Backlight Driving System for Large-Scale LCD Panels,” *IEEE Transaction on Industrial Electronics*, vol. 54, pp. 2751-2760. Oct. 2007

[16] Heinz van der Broect, Georg Sauerlander, and Matthias Went, ”Power Driver Topologies and Control Schemes for LEDs,” *IEEE Applied Power Electronics Conference*, 2007, pp. 1319~1325

[17] Man Siu, Philip K.T. Mok, Ka Nang Leung, Yat-Hei Lam, and Wing-Hung Ki, "A Voltage-Mode PWM Buck Regulator with End-Point Prediction," *IEEE Transaction on Circuits and Systems II*, vol. 53, no. 4, pp. 294-298, April 2006.

[18] Feng Su, Wing-Hung Ki, and Chi-Ying Tsui, "Ultra Fast Fixed-Frequency Hysteretic Buck Converter with Maximum Charging Current Control and Adaptive Delay Compensation for DVS Application", *IEEE Journal of Solid-State Circuits*, pp. 805-814, Apr. 2008

[19] Datasheet "DD311: High Constant Current LED Driver," Silicon touch technology inc

[20] Application Note "EL7801: Powering LED Strings and Arrays in Backlight Applications," Intersil Corp.

[21] Application Note "TLC5940: PWM Dimming Provides Superiorcolor Quality in LED video displays," Texas Instruments Incorporated.

[22] R. D. Middlebrook, "Modeling Current-Programmed Buck and Boost Regulators," *IEEE Transaction on Power Electronics*, vol. 4, pp. 36-52, Jan. 1989.

[23] Chi Yat Leung, P. K. T. Mok, and Ka Nang Leung, "A 1-V Integrated Current-Mode Boost Converter in Standard 3.3/5-V CMOS Technologies," *IEEE Journal of Solid-State Circuits*, pp. 2265-2274, Nov. 2005.

[24] Guangbin Zhang, Sooping Saw, Jin Liu, Scott Sterrantino, David K. Johnson, and Sungyong Jung, "An Accurate Current Source With On-Chip Self-Calibration Circuits for Low-Voltage Current-Mode Differential Drivers" *IEEE Transaction on Circuits and System I,* vol. 53, pp. 40-47, Jan. 2006.

[25] Kihyuk Sung and Lee-Sup Kim, "A High-Resolution Synchronous Mirror Delay Using Successive Approximation Register," *IEEE Journal of Solid-State Circuits*, pp. 1997-2004, Nov. 2004.

[26] Application Note "Buck-Based LED Drivers Using the HV9910B," Supertex Inc.

[27] Chun-Yu Hsieh, Shih-Jung Wang; Yu-Huei Lee, and Ke-Horng Chen, "LED Drivers with PPD Compensation for Achieving Fast Transient Response" *IEEE International Symposium on Circuits and Systems*, 2008, pp.2202-2205.

[28] Michel D. Mulligan, Bill Broach, Thomas H. Lee "A 3MHz Low-Voltage Buck Converter with Improved Light Load Efficiency" *IEEE Solid-State Circuits Conference*, 2007, pp. 528-529.

[29] Chun-Yu Hsieh and Ke-Horng Chen, "Boost DC-DC Converter with Charge-Recycling (CR) and Fast Reference Tracking (FRT) Techniques for High-Efficiency and Low-cost LED Driver" *IEEE European Solid-State Circuits Conference*, pp.358-361. 2008.

[30] Hong-Wei Huang, Ke-Horng Chen, and Sy-Yen Kuo, "Dithering Skip Modulation, Width and Dead Time Controllers in Highly Efficient DC-DC Converters for System-on-chip Applications," *IEEE Journal of Solid-State Circuits,* pp. 2451-2465, Nov. 2007.

[31] Werner Hollinger, Manfred Punzenberger, "An Asynchronous 1.8MHz DC/DC Boost Converter Implemented in the Current Domain for Cellular Phone Lighting Management," *IEEE European Solid-State Circuits Conference*, 2006, pp. 528-531.

[32] Ke-Horng Chen, Hong-Wei Huang, and Sy-Yen Kuo, "Fast Transient DC-DC Converter with On-Chip Compensated Error Amplifier," *IEEE Transaction on Circuits and Systems II,* pp. 1150-1154, Dec. 2007.

[33] Robert W. Erickson and Dragon Maksimović, *Fundamentals of Power Electronics, 2nd ed*. Noirwell, MA: Kluwer, 2000.

[34] Ke-Horng Chen, Chia-Jung Chang, and Ter-Hsing Liu, "Bidirectional Current-Mode Capacitor Multipliers for On-Chip Compensation," in *IEEE Transaction on Power Electronics*, pp. 180-188, Jan. 2008.

[35] Wing Hung Ki, "Signal Flow Graph in Loop Gain Analysis of DC-DC PWM CCM Switching Converters," *IEEE Transaction on Circuits and Systems I*, vol. 45, pp. 644-655, July 1998

[36] Chaitanya K. Chava, José Silva-Martínes, "A Frequency Compensation Scheme for LDO Voltage Regulators" *IEEE Transaction on Circuits and Systems I*, vol. 51, pp. 1041-1050, June 2004

[37] Qiang Bian, Zushu Yan, Yuanfu Zhao, and Suge Yue, "Analysis and Design of Voltage Controlled Current Source for LDO Frequency Compensation", *IEEE Conference on Electron Devices and Solid-State Circuits*, 2005, pp.363-366.

[38] Hong-Wei Huang, Chun-Yu Hsieh, Ke-Horng Chen, and Sy-Yen Kuo, "Adaptive Frequency Control Technique for Enhancing Transient Performance of DC-DC Converters," *IEEE European Solid-State Circuits Conference*, Sep. 2007, pp. 174-177.

[39] Hong-Wei Huang, Chun-Yu Hsieh, and Ke-Horng Chen, "A 1V 16.9ppm/°C 250nA Switched-Capacitor CMOS Voltage Reference" *IEEE Solid-State Circuits Conference*, 2008, pp. 438-439.

[40] Patrick Y. Wu and Philip K. T. Mok, "A Monolithic Buck Converter With Near-Optimum Reference Tracking Response Using Adaptive-Output-Feedback," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11,pp. 2441-2450, November 2007.

[41] Chun-Yu Hsieh and Ke-Horng Chen, "Adaptive Pole-Zero Position (APZP) Technique of Regulated Power Supply for Improving SNR," in *IEEE Transaction on Power Electronics,* pp. 2949-2963, Nov. 2008.

[42] Osama Abdel-Rahman and Issa Batarseh, “Transient Response Improvement in DC-DC Converters Using Output Current for Faster Transient Detection,” *IEEE Annual Power Electronics Specialists Conference*, 2007, pp. 157-160.

Published Paper

◆ *International Journal Paper：*

● 2010

1. **(SCI)** Chia-Hsiang Lin, **Chun-Yu Hsieh**, and Ke-Horng Chen, "A Li-Ion Battery Charger with Smooth Control Circuit (SCC) and Built-in Resistance Compensator (BRC) for Achieving Stable and Fast Charging," in *IEEE Transaction on Circuit and System I,* pp. 506-517, Feb., 2010.
2. **(SCI)** Chao-Hsuan Liu, **Chun-Yu Hsieh**, Yu-Chiao Hsieh, Ting-Jung Tai, and Ke-Horng Chen, "SAR-controlled Adaptive Off-time Technique without Sensing Resistor for Achieving High Efficiency and Accuracy LED Lighting System," in *IEEE Transaction on Circuit and System I,* pp. 1384-1394, June, 2010.
3. **(SCI) Chun-Yu Hsieh**, Chih-Yu Yang, and Ke-Horng Chen, "A Low-Dropout Regulator with Smooth Peak Current Control (SPCC) Topology for Over-Current Protection," in *IEEE Transaction on Power Electronics,* pp. 1386-1394, June, 2010.
4. **(SCI) Chun-Yu Hsieh**, Hong-wei Huang, and Ke-Horng Chen, "A 1 -V, 16.9 ppm/ °C, 250 nA Switched-Capacitor CMOS Voltage Reference," in *IEEE Transaction on Very Large Scale Integration System, accept to be published.*

● 2009

5. **(SCI) Chun Yu Hsieh** and Ke Horng Chen, "Boost DC-DC Converter With Fast Reference Tracking (FRT) and Charge-Recycling (CR) Techniques for High-Efficiency and Low-Cost LED Driver", *IEEE Journal of Solid-State Circuits*, pp. 2568-2580, Sep., 2009.
6. **(SCI) Chun-Yu Hsieh**, Chih-Yu Yang, and Ke-Horng Chen, "A Charge-Recycling Buck-store and Boost-Restore (BSBR) Technique with Dual Outputs for RGB LED Backlight and Flashlight Module," in *IEEE Transaction on Power Electronics,* pp.

1914-1925, Aug., 2009.

- **2008**

7. **(SCI) Chun-Yu Hsieh** and Ke-Horng Chen, "Adaptive Pole-Zero Position (APZP) Technique of Regulated Power Supply for Improving SNR," in *IEEE Transaction on Power Electronics,* pp. 2949-2963, Nov. 2008.

◆ ***International Conference Paper：***

- **2010**

1. Chen-Li Chu, **Chun-Yu Hsieh**, Da-Liang Chiu, and Ke-Horng Chen, "Multi-LC/BL Algorithmic Technique in Field Color Sequential LCD for Color Breakup Suppression," *Society for Information Display*, 2010 Digest 12.3, pp 159-162.
2. **Chun-Yu Hsieh**, Chih-Yu Yang, Fu-Kuei Feng, and Ke-Horng Chen, "A Photovoltaic System with an Analog Maximum Power Point Tracking Technique for 97.3% High Effectiveness," *Society for Information Display*, 2009 Digest 43.2, pp640-643.

- **2009**

3. **Chun-Yu Hsieh**, Chih-Yu Yang, Ming-Hsin Huang, Don-Hwan Li, Chi-Lin Chen, and Ke-Horng Chen, "A Charge-Reservoir with Buck-Store and Boost-Restore (BSBR) Technique for High Efficient Conversion and Low Cost Solution of RGB LED Display Panels," *Society for Information Display*, 2009 Digest 43.2, pp640-643.

- **2008**

4. **Chun-Yu Hsieh** and Ke-Horng Chen, "Boost DC-DC Converter with Charge-Recycling (CR) and Fast Reference Tracking (FRT) Techniques for High-Efficiency and Low-cost LED Driver," *IEEE European Solid-State Circuits Conference*, 2008, pp.358-361.

5. **Chun-Yu Hsieh**, Shih-Jung Wang, Yu-Huei Lee and Ke-Horng Chen, "High Efficiency and/or Low Cost LED Backlight System for Color Sequential Technique in Color Filter-less LCD System," *Society for Information Display*, 2008 Digest 71.4, pp1104-1107.
6. **Chun-Yu Hsieh**, Shih-Jung Wang, Yu-Huei Lee, and Ke-Horng Chen, "High Efficiency and/or Low Cost LED Backlight System for Color Sequential Technique in Color Filter-less LCD System" *Society for Information Display* , Los Angel, May 18-23 2008
7. **Chun-Yu Hsieh**, Shih-Jung Wang, Yu-Huei Lee, and Ke-Horng Chen, "LED Drivers with PPD Compensation for Achieving Fast Transient Response" *International Symposium on Circuits and Systems*, Seattle, May 18-21 2008
8. Hong-wei Huang, **Chun-Yu Hsieh**, Ke-Horng Chen, and Sy-Yen Kuo, " A 1-V, 16.9 ppm/°C, 250 nA Switched- Capacitor CMOS Voltage Reference", *International Solid State Circuit Conference*, San Francisco, USA, Feb. 3-7 2008

- **2007**

9. **Chun-Yu Hsieh**, Yung-Chun Chuang, and Ke-Horng Chen," A Novel Precise Step-Shaped Soft-Start Technique for Integrated DC-DC Converter" *International Conference on Electronics, Circuits, and Systems*, Dec. 11-14 2007, Morocco Marrakech
10. **Chun-Yu Hsieh**, Po-Chin Fan, and Ke-Horng Chen, "A Dual Phase Charge Pump with Compact Size" *International Conference on Electronics, Circuits, and Systems*, Dec. 11-14 2007, Morocco Marrakech
11. Hong-wei Huang, **Chun-Yu Hsieh**, Ke-Horng Chen, and Sy-Yen Kuo, "Adaptive Frequency Control Technique for Enhancing Transient Performance of DC-DC converters", *IEEE European Solid-State Circuit Conference*, Munich, Germany, Sep. 11-13 2007

12. Hong-wei Huang, **Chun-Yu Hsieh**, Ke-Horng Chen, "Load Dependent Dead-Times Controller Based on Minimized Duty Cycle Technique for DC-DC Buck Converters", *IEEE Power Electronics Specialist Conference*, Orlando, Florida, USA, June 17-21 2007
13. Shih-Min Chen, **Chun-Yu Hsieh**, Ke-Horng Chen, "Challenge on Compact Size DC-DC Buck Converters with High-Speed Current Sensor and On-Chip Inductors", *IEEE Midwest Symposium on Circuits and Systems*, Montréal, Canada, Aug. 5-8 2007

◆ ***National Conference Paper*：**

1. **(SCI) Chun-Yu Hsieh**, Chih-Yu Yang, and Ke-Horng Chen, "An Energy-Recycling Buck-Store and Boost-Restore (BSBR) Technique with Dual Outputs for RGB LED Backlight and Flashlight Module," in *Electronic Technology Symposium,* June, 2009.
2. **(SCI) Chun-Yu Hsieh**, Chih-Yu Yang, and Ke-Horng Chen, "A Low-Dropout Regulator with Smooth Peak Current Control (SPCC) Topology for Over-Current Protection," in *VLSI/CAD,* July, 2009.

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