國 立 交 通 大 學

電信工程研究所

博 士 論 文

應用於解決 CMOS 閃爍雜訊之低中頻接收機架構和深 N 型井雙極性接面電晶體直接降頻接收機

CMOS Flicker Noise Solutions by Low-IF Receiver Architecture and Deep-N-Well BJT Direct-Conversion Receiver

研 究 生：徐金詳

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中 華 民 國 一百 年 六 月

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研究生：徐金詳　　Student: Jin-Siang Syu

指導教授：孟慶宗　博士　　Advisor: Dr. Chinchun Meng

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一、 事由：本校電信研究所博士班研究生 徐金詳 提出論文以參加國立交通大學博士班論文口試。

二、 說明：本校電信研究所博士班研究生 徐金詳 已完成本校電信研究所規定之學科課程及論文研究之訓練。

有關學科部分，徐君已修滿三十六學分之規定（請查閱學籍資料）並通過資格考試。

有關論文部分，徐君已完成其論文初稿，相關之論文亦分別發表或即將發表於國際期刊（請查閱附件）並滿足論文計點之要求。

總而言之，徐君已具備國立交通大學電信研究所應有之教育及訓練水準，因此特推薦

徐君參加國立交通大學電信工程研究所博士班論文口試。

孟慶宗

交通大學電信工程研究所教授　孟　慶　宗

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學生:徐金詳　　指導教授:孟慶宗博士

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電信工程研究所博士班

摘　　要

本論文中分作五個章節，包含了各式混頻器和接收機之效能改善。在第二章中提出單頻帶和雙頻帶之高線性度吉伯特升頻器。利用輸入端之偏壓偏移交錯耦合對與輸出端之並聯回授緩衝放大器，使升頻器之輸出端三階交調截點與輸出端 1-dB 壓縮點差距高達 22 dB。

第三章利用相量表示方式完整地分析和比較各式被動正交信號產生器，包含了振幅和相位與頻寬的關聯。此外，雙極性接面電晶體之主動混頻器比互補式金氧半導體之主動或被動混頻器擁有更寬的轉換增益平坦區，因此有著更佳的正交本地振幅不平衡之容忍度。應用於吉伯特混頻器本地振盪源埠之正交耦合器若直接在高損耗矽基板上製作，可縮小面積但會有輸出振幅不相等的特性，正好可以利用選取適當之本地振幅而改善。另一方面，利用 LR-CR 正交相位產生器並配合雙極性接面電晶體主動混頻器成功地實現一接收機，並且在超寬頻應用頻帶中輸出端之信號振幅與相位誤差分別低於±1dB 和±2°。

在第四章中，於 0.35 毫米矽鍺異質接面電晶體製程中利用補償相位延遲技術實作一個高隔離度之次諧波降頻器。在相同偏壓條件、電晶體大小和操作頻率

下，使用補償相位延遲技術與傳統無使用此技術之電路可得到相似之轉換增益、雜訊指數和線性度，卻額外改善了 34/35 dB 的 2LO 至 RF/IF 埠隔離度，8/9 dB 的 LO 至 RF/IF 埠隔離度和 22 dB 的 RF 至 IF 埠隔離度。

第五章則利用了相量分析方式來討論在雙降頻低中頻接收機中鏡像抑制效能衰減之原因。因此，分別在射頻輸入端或兩級混頻器中間適當地擺放額外的多相位濾波器均可以大大地改善鏡像抑制效能，使得在本地振盪源之正交信號誤差和元件不匹配仍然存在的情況下，達到接近中頻多相位濾波器之鏡像抑制比的理論極值。

第六章則介紹了在低成本 0.18 毫米互補式金氧半導體製程下應用於低功率低雜訊直接降頻接收機。在標準互補式金氧半導體製程中，深 N 型井雙極性接面電晶體因為其超低之閃爍雜訊和較佳之轉導而被有效地應用於混頻器和基頻放大器中，然而其相對低的截止頻率在混頻器的應用上也造成了額外的挑戰。因此，透過詳盡地分析操作在低截止頻率之吉伯特混頻器，電感式突起技術被用以降低本地振盪輸出之損耗和增加混頻器之轉換增益。另一方面，次諧波混頻機制為另一解決低截止頻率之方式並搭配低損耗的八相位多相位濾波器實作一低功率低雜訊次諧波直接降頻接收機。最後，利用可調頻式雙級低雜訊放大器和寬頻之八相位本地振盪產生器，實作了一涵蓋完整 U-NII 頻段之低功率低雜訊接收機，其中同時利用電感式突起和次諧波混頻機制成功讓接收機之射頻頻率可以為深 N 型井雙極性接面電晶體之三倍截止頻率。

關鍵字：互補式金氧半導體、矽鍺異質接面電晶體、吉伯特混頻器、雙頻帶、次諧波混頻器、隔離度、低中頻接收機、鏡像抑制、直接降頻接收機、深 N 型井雙極性電晶體、閃爍雜訊。

CMOS Flicker Noise Solutions by Low-IF Receiver Architecture and Deep-N-Well BJT Direct-Conversion Receiver

Student: Jin-Siang Syu Advisor: Chinchun Meng

Institute of Communication Engineering

National Chiao Tung University

Abstract

This dissertation consists of five chapters, including performance improvements of various mixer topologies and receivers. Chapter 2 introduces single-/dual-band highly linear Gilbert upconverters. The difference of OIP_3 and OP_{1dB}, widely used as a criterion for mixer linearity, is over 22 dB by using an input bias-offset cross-coupled pair and output shunt-shunt feedback buffer amplifier.

In Chapter 3, passive quadrature signal generators are deeply discussed, including amplitude/phase relations by using phasor analyses. Further, a bipolar-juncion-transistor (BJT)-based Gilbert mixer inherently has a wider flat-gain region and more toleration of LO amplitude imbalance than MOS active/passive mixers. Thus, the loss imbalance of the LO quadrature coupled-line coupler directly implemented on a lossy silicon substrate can be simply solved by choosing proper LO power in the common flat-gain region. On the other hand, an ultra-wideband (UWB) Gilbert downconverter using an LR-CR quadrature generator, which has always perfect quadrature phase but balanced amplitudes only at the center frequency. However, the BJT mixer successfully compensates this drawback and achieves amplitude/phase imbalance

below ±1dB/±2° covering whole UWB bands, respectively.

In Chapter 4, a 0.35-μm SiGe heterojunction bipolar transistor (HBT) high-isolation sub-harmonic mixer is proposed using a delay compensation technique. The sub-harmonic mixers with and without delay compensation are demonstrated at the same bias condition, device sizes and operating frequency. As a result, similar conversion gain, noise figure and linearity are achieved. However, the 2LO-to-RF/IF isolation is improved by 34/35 dB, the LO-to-RF/IF isolation by 8/9 dB and the RF-to-IF isolation by 22 dB.

Chapter 5 fully discusses the reasons for the degradation of the image rejection performance in a dual-conversion low-IF receiver by using phasor analyses. By inserting the poly-phase filters (PPFs) at proper positions (RF stage or inter-stage between two downconversions), the image-rejection ratio (IRR) can nearly reach the theoretical limit of the IF PPF even if the LO quadrature imbalance and device mismatches still exist.

Finally, Chapter 6 introduces various techniques in designing a low-power low-noise direct-conversion receiver (DCR) in a low-cost 0.18-μm CMOS technology. Deep-n-well (DNW) BJTs in standard 0.18-μm CMOS process are used for lower flicker noise and higher transconductance than standard NMOS devices. But the relatively low cut-off frequency (f_T) becomes a big challenge for the mixer application. Thus, the current switching operation of the BJT switching function operating near or even higher than the device f_T is fully analyzed. An inductive peaking technique is then used to compensate the loss of the LO generator and the mixer conversion loss. On the other hand, a sub-harmonic mixing is another straightforward solution for the low-f_T operation, but a low-loss octet-phase PPF is analyzed and employed to generate well-balanced octet LO signals. Furthermore, a low-power sub-harmonic DCR

covering whole U-NII bands is also demonstrated in this chapter by using a two-stage tunable-band RF low-noise amplifier (LNA) and a wideband octet-phase generator.

Keywords: CMOS, SiGe heterojunction bipolar transistor (HBT), Gilbert mixer, dual-band, sub-harmonic mixer, isolation, low-IF receiver, image rejection, direct-conversion receiver (DCR), deep n-well (DNW), bipolar junction transistor (BJT), flicker noise.

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Jin-Siang Syu

NCTU, June 2011

Table of Contents

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter4

Chapter 5

Chapter 6

Chapter 7

List of Tables

List of Abbreviations

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CG	Conversion Gain
DCR	Direct-Conversion Receiver
HBT	Heterojunction Bipolar Transistor
I/OP_{1dB}	Input/Output 1-dB Gain Compression Point
I/OIP_3	Input/Output Third-Order Intercept Point
I/OIP_2	Input/Output Second-Order Intercept Point
I/Q	In-Phase/Quadrature
IRR	Image-Rejection Ratio
LO	Local Oscillator
NF	Noise Figure
PPF	Poly-Phase Filter
SH-DCR	Sub-Harmonic Direct-Conversion Receiver
SHM	Sub-Harmonic Mixer
SiGe	Silicon-Germanium
SSB	Single Side-Band
TCA	Transconductance Amplifier
TIA	Transimpedance Amplifier
UWB	Ultra-Wideband
VGA	Variable-Gain Amplifier
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

Chapter 1 Introduction

1.1 COMMERCIAL FREQUENCY BANDS AND APPLICATIONS

The industrial, scientific and medical (ISM) bands and Unlicensed National Information Infrastructure (U-NII) bands are two main unliscensed bands. Thus, they are widely used for wireless communication systems.

The ISM bands were originally reserved internationally for the use of RF energy for industrial, scientific and medical purposes, not for communications. For examples, microwave ovens, and medical diathermy machines. Thus, in general, communication equipments operating in these bands must accept any interference generated by ISM equipments. The ISM bands defined by the International Telecommunication Union Radiocommunication Sector (ITU-R) are listed with the main applications as listed in TABLE. 1.1.

TABLE. 1.1 ISM BAND

Frequency Band	Applications	Frequency Band	Applications
6.765–6.795 MHz		2.400–2.500 GHz	Bluetooth, ZigBee, WLAN (802.11b/g/n)
13.553–13.567 MHz	RFID, NFC	5.725–5.875 GHz	HyperLAN, Wi-Fi
26.957–27.283 MHz		24–24.25 GHz	
40.66–40.70 MHz		61–61.5 GHz	
433.05–434.79 MHz		122–123 GHz	
902–928 MHz	ZigBee	244–246 GHz	

On the other hand, the U-NII band is part of the radio frequency spectrum used by IEEE 802.11a devices and by many wireless internet service providers (ISPs). It operates over the following ranges:

- U-NII Low (U-NII-1): 5.15-5.25 GHz.
- U-NII Mid (U-NII-2): 5.25-5.35 GHz.
- U-NII Worldwide: 5.47-5.725 GHz. Added by Federal Communications Commission (FCC) in 2003.
- U-NII Upper (U-NII-3): 5.725-5.825 GHz. Sometimes referred to as *U-NII/ISM* due to overlap with the ISM band.

Fig. 1-1 shows the comparisons by data rate and distance for different communication technologies, including wireless personal area network (WPAN) and wireless local area network (WLAN). The size of the block represents the costs, *i.e.*, a small block means a lower price. TABLE. 1.2 lists the comparisons for popular WPAN systems. The UWB technology has the highest data transmission rate and NFC has the lowest. However, the ZigBee has the longest transceiving distance but relatively low data rate. Based on data rate and transceiving distance of each application, a proper protocol can be chosen. Besides, NFC operates at slower speeds than Bluetooth, but consumes far less power and requires no pairing. NFC sets up faster than standard Bluetooth, but is not much faster than Bluetooth low energy.

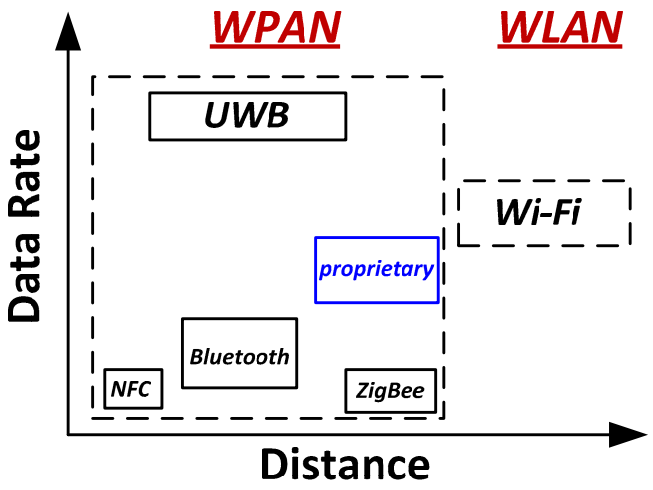


Fig. 1-1 Comparisons for WPAN and WLAN by data rate and distance.

TABLE. 1.2 COMPARISONS FOR WIRELESS PERSONAL AREA NETWORK

WPAN	UWB	Bluetooth	ZigBee	NFC	**Proprietary**
Frequency	3.1~10.6 GHz	2.4GHz (ISM)	2.4GHz/898 MHz/915MHz	13.56 MHz	**Single-/ Dual-Band**
Distance	0~10m	0~10m	0~75m	<50cm	**0~75m**
Data Rate	Very High	Low	Very Low	Very Low	**Medium**
Safety	High	High	Medium	Very High	**High**
Price	High	Medium	Low	Very Low	**Low**
Standard	802.15.3	802.15.1	802.15.4	IEC 18092/21481	**N.A.**

As shown in TABLE. 1.2, the proposed low-power transceiver in this dissertation does not focus on any specific standard. Contrarily, long distance, high data rate (for high quality and accurate control) but still low cost are the main goals for implementations. All the proposed techniques and demonstrations are based on these goals. Moreover, a multi-band/multi-standard integration can even be achieved in the future.

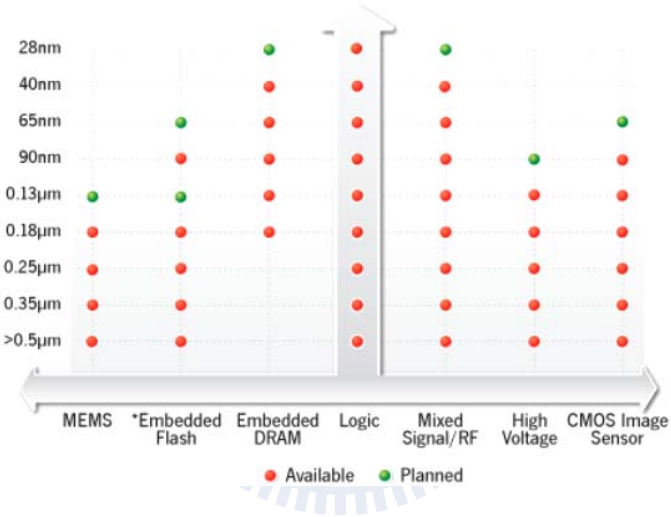
1.2 PROCESS CHOSEN

1.2.1 Cost vs. Performance

Since the operating frequency of these short-range application is not high (except for the emerging 60-GHz high-data-rate application), various technologies can be chosen to achieve required functions and specifications. Fig. 1-2 shows the technology development in TSMC. The 28nm logic circuits are now available but the mixed-signal/radio-frequency (MS/RF) circuits are still developing. On the other hand, the 40 nm process is available for MS/RF circuits. However, 0.18-μm CMOS is still the mainstream technology.

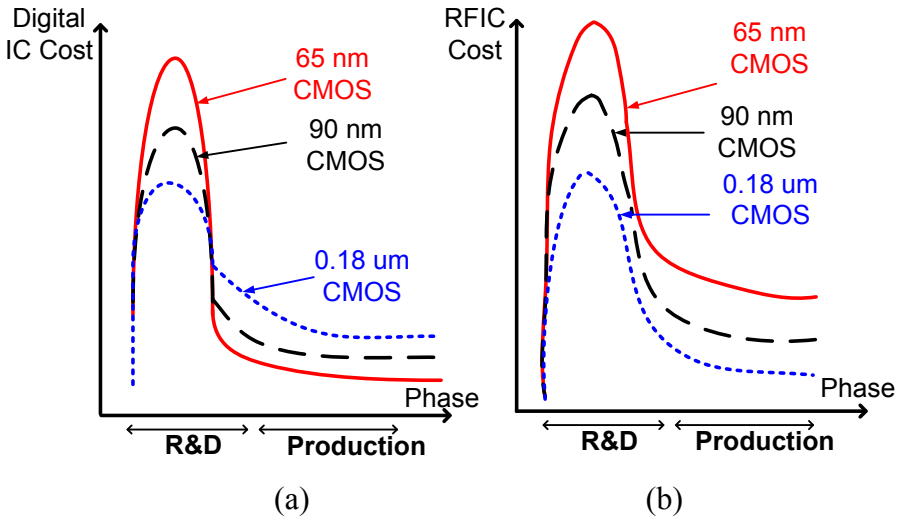
Although it is believed that the cost can be much lower down when the final

product is entering mass production, the barrier for research and development (R&D) makes it very hard to finish a final product. The concept of the barrier for the CMOS R&D cost for digital and RF ICs is illustrated in Fig. 1-3(a) and (b), respectively. The Y-axis is the cost and the X-axis is the production phase. Fig. 1-3(a) shows the cost reduction of the digital circuit as CMOS scaling although the R&D cost is high. It is noteworthy that Fig. 1-3(a) is similar to a conventional diagram of the activation energy. TABLE. 1.3 also lists the R&D cost of every technology, pronounced by Chang, ISSCC 2007.



*0.13 µm embedded flash is actually shrunk to 0.11 µm

Fig. 1-2 TSMC Technology Development



(a) (b)

Fig. 1-3 R&D and production cost of CMOS technology for (a)digital IC(b)RFIC.

TABLE. 1.3 R&D COST FOR DEEP SUBMICRON CMOS

Technology	Cost (Wafer/Mask set)
0.18 um	1.4K/120K
0.13 um	1.8K/300K
90 nm	2.5K/900K
65 nm	3.8K/1400K

On the other hand, because the operating frequency is relatively low, the passive components limit the size reduction. This is the biggest difference from the digital circuits, as shown in Fig. 1-3 (b). Thus, choosing a proper, not always the most advanced, technology can save significant cost.

1.2.2 Flicker Noise

However, a CMOS process has severe flicker noise problems. The dangling bonds, appearing at the interface between the gate oxide and the silicon substrate in a MOSFET, give rise to extra energy states. Thus, when charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing the flicker noise in the drain current. Typically, the noise spectral density of the flicker noise is inverse proportional to frequency and thus the flicker noise is also called 1/*f* noise.

In this dissertation, various solutions for flicker noise problems are provided. Direct-conversion receivers (DCRs) with fundamnetal mixer (in Chapter 3) or sub-harmonic mixers (in Chapter 4) are demonstrate using silicon germanium (SiGe) heterojunction bipolar transistor (HBT) technology for good gain/noise performance and flicker noise free property at a higher cost. A low-IF architecutre with IF frequency set over the flicker noise corner (discussed in Chapter 5) is another straightforward flicker noise solution. However, a higher power consumption is

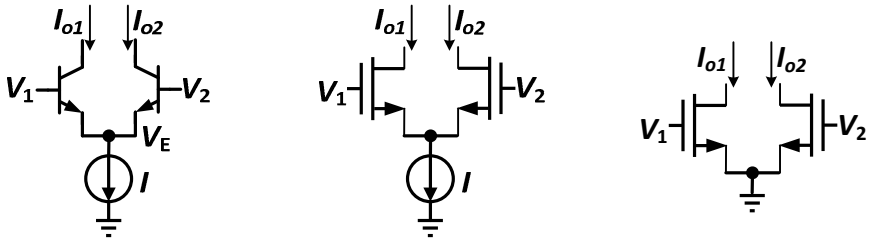
required for both RF and analog to digital converter (ADC) circuits. On the other hand, the parasitic deep-n-well (DNW) bipolar junction transistor (BJT), which has an ultra-low flicker noise, is available in standard CMOS process without extra cost. However, the low transistor cut-off freuqency (f_T) of the parasitic BJT devices becomes another challenge for designers and is deeply analysis and then solved in Chapter 6.

Chapter 2 High Linearity Gilbert Upconversion Mixer

2.1 HIGH-LINEARITY BIAS-OFFSET TCA

2.1.1 Introduction

Linearity is an important issue in communication systems, especially in transmitters. The passive mixers, *e.g.*, the resistive mixers [1] or the diode mixers [2], are demonstrated with high linearity but severe loss. On the other hand, a Gilbert mixer topology is widely used in a wireless transceiver to avoid the severe loss at high frequencies. However, a conventional Gilbert mixer with emitter-coupled (source-coupled) differential pair input stage suffers from a poor linearity and therefore the signals of adjacent channels easily interfere with the desired channel. Note that, a differential topology, either with a tail current source at low frequency or an parallel LC tank at high frequencies, has a better common-mode rejection and also a higher second-order input-referred intercept point (IIP_2).



(a) (b) (c)

Fig. 2-1 (a) BJT differential amplifier (b) MOS differential amplifier (c) MOS pseudo-differential pair.

The transfer function of a BJT differential pair with an ideal current source, as shown in Fig. 2-1(a), is $\Delta i_c = \tanh(\frac{v_{id}}{2V_T})$ [3], which is obtained from the I-V exponential transfer function of a BJT device. Thus, the linearity is inherently poor.

On the other hand, the transfer function of a MOS differential pair [in Fig. 2-1(b)] is

$$\begin{aligned}\Delta i_d &= v_{id}\left(\frac{I}{V_{OV}}\right)\sqrt{1-\left(\frac{v_{id}/2}{V_{OV}}\right)^2} \\ &\approx v_{id}\left(\frac{I}{V_{OV}}\right)\left[1-\frac{1}{8}\left(\frac{v_{id}}{V_{OV}}\right)^2\right] \\ &= \left(\frac{I}{V_{OV}}\right)v_{id}-\frac{I}{8V_{OV}^3}v_{id}^3\end{aligned} \tag{2.1}$$

and the third order term cannot be omitted [4] even without considering the short-channel effect. The MOS pseudo-differential topology [in Fig. 2-1(c)] has much better IIP_3 but a worse IIP_2.

Many ideas are utilized to improve linearity. For example, a multi-*tanh* approach [5] and a class-AB transconductance [6] are designed to provide more linear transfer function of the transconductor by eliminating high order terms of the exponential function of bipolar junction transistors (BJTs) or the short channel effect of the MOS transistors. A feedback technique is also widely employed by strongly suppressing the high-order distortion at the cost of gain [7], e.g., emitter (source) degeneration.

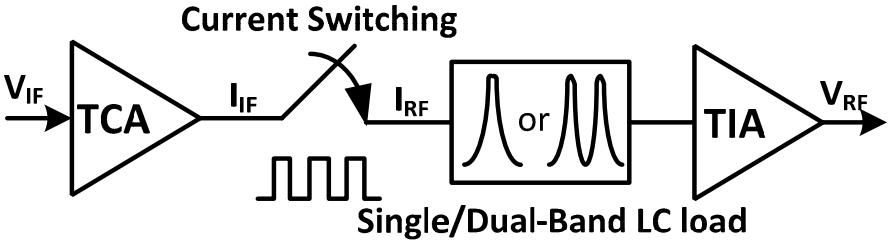


Fig. 2-2 Block diagram of the single-/dual-band Gilbert upconverter.

The block diagram of a single-/dual-band Gilbert upconversion mixer is illustrated in Fig. 2-2. A Gilbert mixer core is employed to commutate I_{IF} with LO frequency to produce I_{RF} while I_{IF} is generated by a transconductance amplifier (TCA) input stage. The differential I_{RF} current passes through a passive single/dual-band LC

current combiner with extra gain improvement [8] and then a transimpedance amplifier (TIA) translates the output current (I_{RF}) to the voltage signal (V_{RF}) and achieves output matching simultaneously.

The current commutation is a highly linear process and only translates the IF signal to the RF signal with every odd order LO frequencies. Besides, the passive resonator is inherently linear. Consequently, the input TCA and output TIA play important roles for the linearity issue.

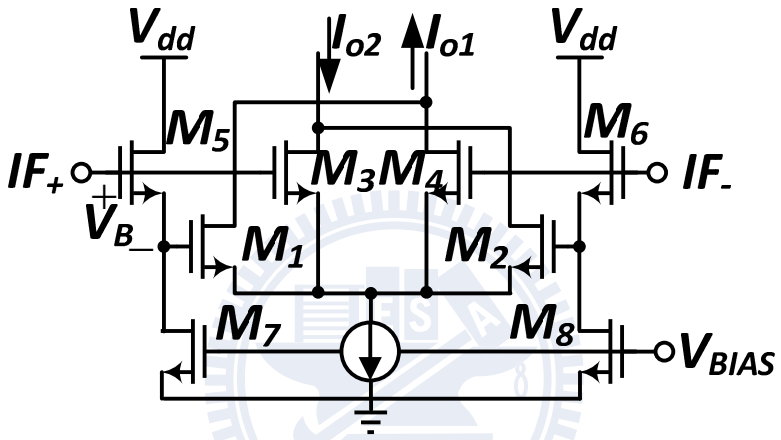


Fig. 2-3 Bias-offset transconductance amplifier.

In this chapter, a bias-offset cross-coupled TCA [9] is employed at the IF port for linearity improvement. The TCA consists of two differential pairs with a constant bias offset (V_B), as shown in Fig. 2-3. The transconductance (g_m) of the TCA is derived as follows, assuming all transistors are in a square-law region.

$$\begin{cases} i_{o1} = i_{M1} + i_{M4} = k_1(V_{IF+} - V_x - V_{Tn})^2 + k_4(V_{IF-} - V_B - V_x - V_{Tn})^2 \\ i_{o2} = i_{M2} + i_{M3} = k_2(V_{IF-} - V_x - V_{Tn})^2 + k_3(V_{IF+} - V_B - V_x - V_{Tn})^2 \end{cases}, \quad (2.2)$$

where $k_i = \frac{1}{2}\mu_n C_{ox}\frac{W_i}{L_i}, i = 1,2,3,4 \quad k_1 = k_2, k_3 = k_4$ and V_B is the gate-to-source voltage drop of M_5-M_6 which provides a constant dc offset voltage for the two differential pairs of M_1-M_2 and M_3-M_4.

$$i_{o1}-i_{o2}=k_1(V_{IF+}-V_{IF-})(V_{IF+}+V_{IF-}-2V_x-2V_{tn}) \\ -k_3(V_{IF+}-V_{IF-})(V_{IF+}+V_{IF-}-2V_x-2V_{Tn}-2V_B) \tag{2.3}$$

because $V_{IF+}+V_{IF-}=2V_{CM}$ is a constant dc,

$$i_{o1}-i_{o2}=(V_{IF+}-V_{IF-})\left[2(k_1-k_3)(V_{CM}-V_x-V_{Tn})+2k_3V_B\right]. \tag{2.4}$$

Thus, $g_m=2kV_B$, *if* $k=k_1=k_3$. The g_m is a constant and no third-order inter-modulation occurs ideally. However, the short-channel effect degrades the linearity, especially when a large gate-to-source voltage is applied on the device with a shorter gate length in an advanced CMOS technology.

Gilbert upconversion mixers with NMOS/PMOS bias-offset TCAs are implemented, respectively, and fully compared in next section.

2.1.2 Gilbert Upconversion Mixers With NMOS/PMOS Bias-Offset TCA

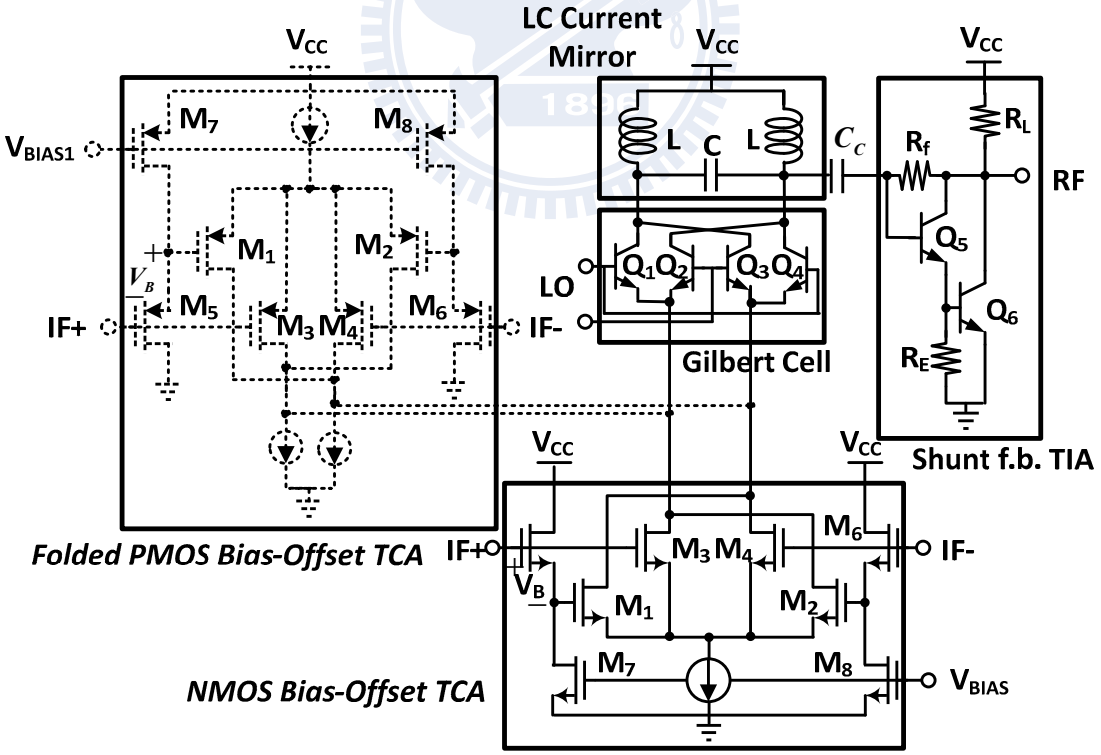
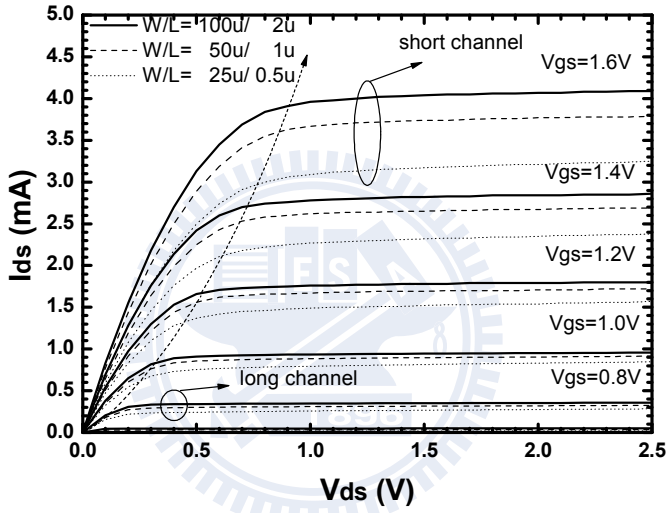


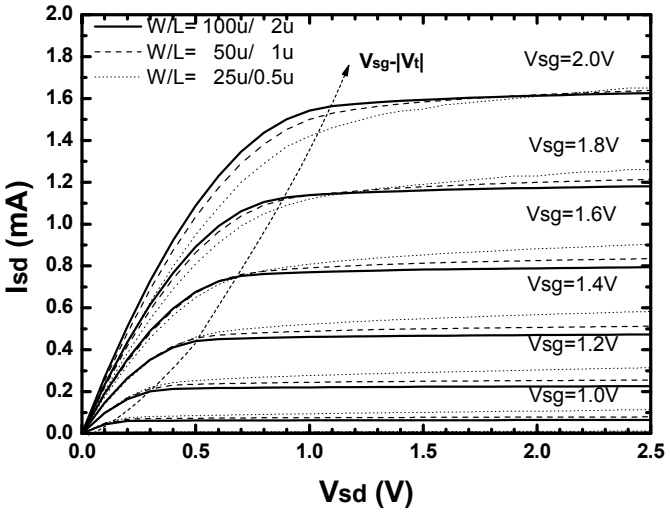
Fig. 2-4 Schematic of the Gilbert upconverters with NMOS/PMOS-type bias-offset TCAs and a single-band LC current combiner.

The schematics of the Gilbert upconversion mixers with NMOS-type and folded PMOS-type input stages are shown in Fig. 2-4. The bias-offset differential pair employed in the input stage has the transconductance of $2kV_B$ if the MOS characteristic is still in a square-law region with a long channel transfer function, as introduced in Section 2.1.1.

The NMOS and PMOS I-V characteristics are shown in Fig. 2-5(a) and (b) with the gate lengths of 0.5 μm, 1 μm, and 2 μm and the correspondent widths of 25 μm, 50 μm, and 100 μm, respectively.



(a)



(b)

Fig. 2-5 (a)NMOS (b) PMOS I-V characteristics with different gate lengths.

The drain saturation voltage, V_{dsat}, is less than the gate-overdrive voltage, $V_{gs}-V_T=V_{OV}$, if the short channel effect takes place. However, if V_{OV} is still small, the transistors are still in the long channel region because the electric field is not large enough to saturate the velocity of the electrons as depicted in Fig. 2-5(a). Contrarily, the PMOS is almost in the long channel region even if the gate-overdrive voltage is large as shown in Fig. 2-5(b). Moreover, if the device is still in the long channel region, the drain saturation currents are almost the same if the W/L ratio is kept at a constant as shown in Fig. 2-5(b). On the other hand, the saturation current of a short channel device is lower than that of the long channel device when the W/L ratio is kept the same as shown in Fig. 2-5(a). In addition, a shorter gate length results in a smaller output resistance of the MOS transistor.

The gate length of the NMOS transistors, M_1-M_4, in the input stage of the first chip is 0.5 μm while the gate length of the PMOS transistors, M_1-M_4, of the other chip is 1 μm. For the lower mobility of PMOS transistors, the widths of the PMOS transistors are designed much wider to achieve similar transconductance gain when compared to the upconverter with the NMOS TCA. As a result, the IF bandwidth of the upconverter with the PMOS TCA is much narrower than that with the NMOS TCA.

Instead of using the MOS transistors in the Gilbert switching quad with a large LO switching voltage requirement of $\sqrt{2}V_{OV}$ (gate-overdrive voltage), the bipolar transistors Q_1-Q_4 are utilized in this work with only about 0.1-V LO voltage swing requirement to make the current fully switch. The current commutation mechanism is highly linear and only performs the frequency translation. A single band current combiner with a π-shape is shown in Fig. 2-6 with the differential input current I_+ and I_-. The combination of the LC current combiner and the current source I_+ can be

represented by its Norton equivalence I_{out} and Z_{out} as shown in Fig. 2-6. The equivalent current source (I_{out}) and the output equivalent impedance (Z_{out}) can be obtained by of the ABCD matrix

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{bmatrix} \mathrm{A} & \mathrm{B} \\ \mathrm{C} & \mathrm{D} \end{bmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix}. \tag{2.5}$$

That is, $I_{out} = \frac{1}{D} I_+$ and $Z_{out} = \frac{D}{C}$, where

$$D = 1 - \frac{1}{\omega^2 LC} \tag{2.6}$$

and

$$C = \frac{1}{j\omega L}\left[2 - \frac{1}{\omega^2 LC}\right]. \tag{2.7}$$

At the resonant frequency of $\omega_0 = 1/\sqrt{2LC}$, D=−1, and C=0. That is, input current I_+ reverses and thus the total output current doubles (i.e., I_{total}=I_-−I_{out}= I_-+I_+=2I) when compared to the single-ended output current of each path [8].

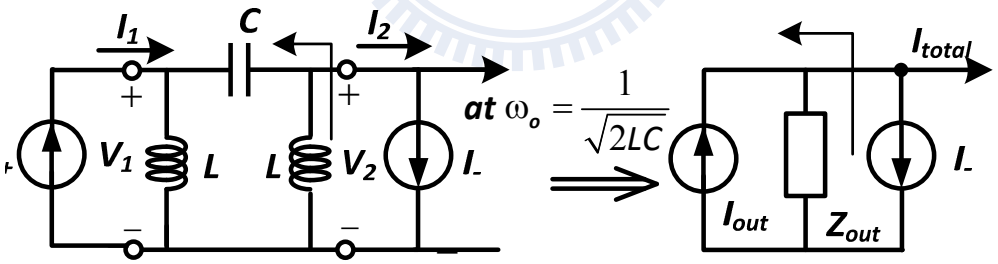
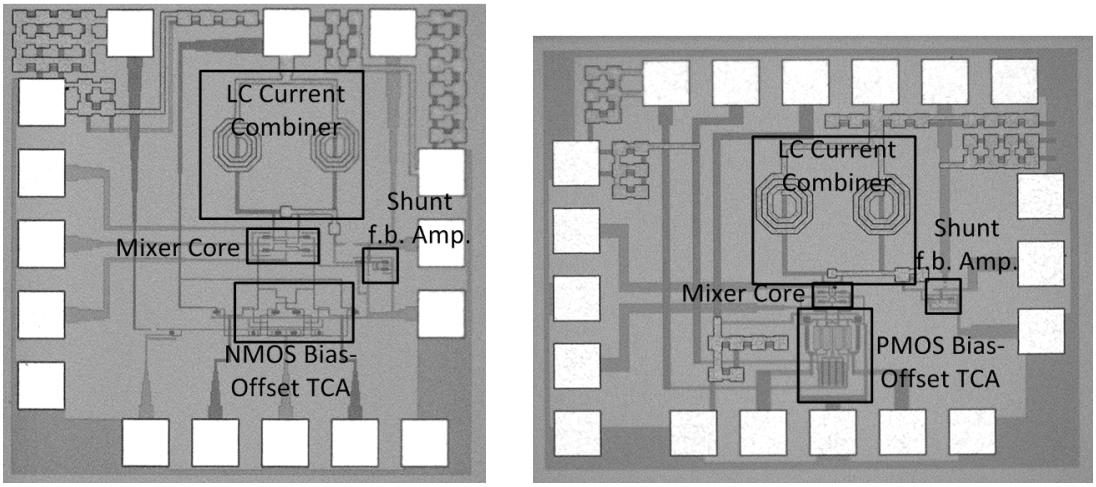


Fig. 2-6 Block diagram of the LC current combiner and its equivalent circuit at the resonant frequency.

The output shunt-shunt feedback TIA is employed to translate the combined current output I_{tot} to the voltage signal. Moreover, the output impedance is reduced by the factor of (1+$A\beta$) for the shunt-type feedback and thus the output matching is easily achieved. The 20-GHz bandwidth of the feedback TIA is designed with strong feedback to reduce the nonlinearity effect.

The die photo of the high linearity Gilbert upconverters are demonstrated by

utilizing NMOS and PMOS TCAs are shown in Fig. 2-7(a) and (b), respectively. On-wafer measurement facilitates the RF performance.



(a) (b)

Fig. 2-7 Die photo of the Gilbert upconverter (a) using an NMOS TCA (b) using a PMOS TCA.

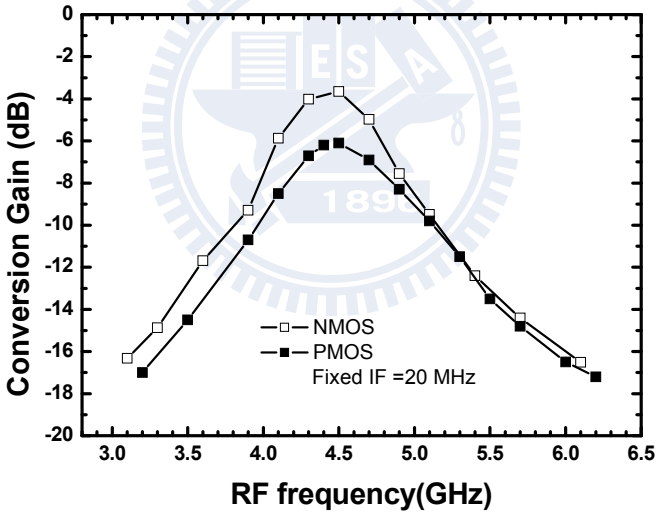


Fig. 2-8 Conversion gain with respect to RF frequency.

The peak conversion gain of the upconverters with NMOS/PMOS input TCAs occurs at both RF=4.4 GHz, IF=20 MHz and the LO power is −5 dBm as shown in Fig. 2-8. The power performance of the upconverters with NMOS/PMOS TCAs is shown in Fig. 2-9. The OP_{1dB} and OIP_3 are −11/−11 dBm and 5.5/9.5 dBm for the upconverters with NMOS and folded PMOS TCAs, respectively.

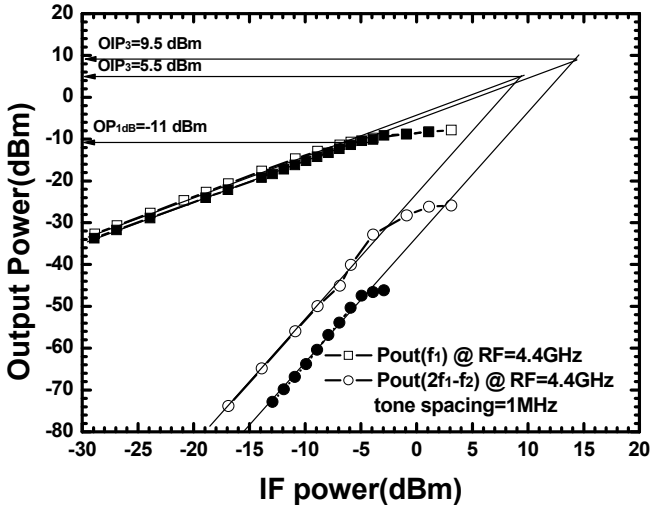


Fig. 2-9 Power performance.

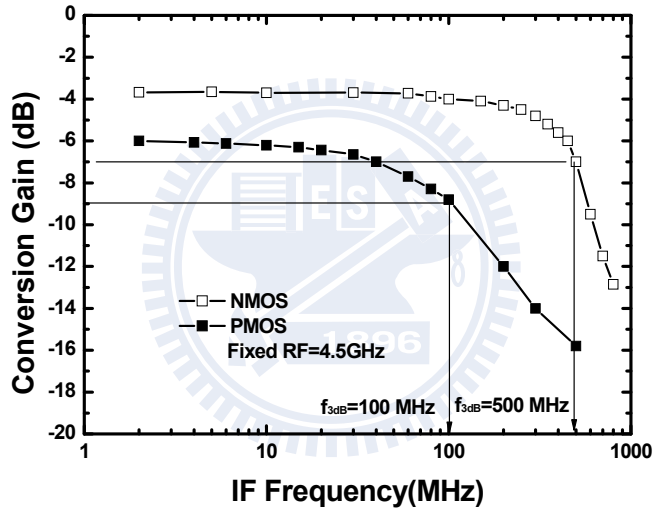


Fig. 2-10 IF bandwidth.

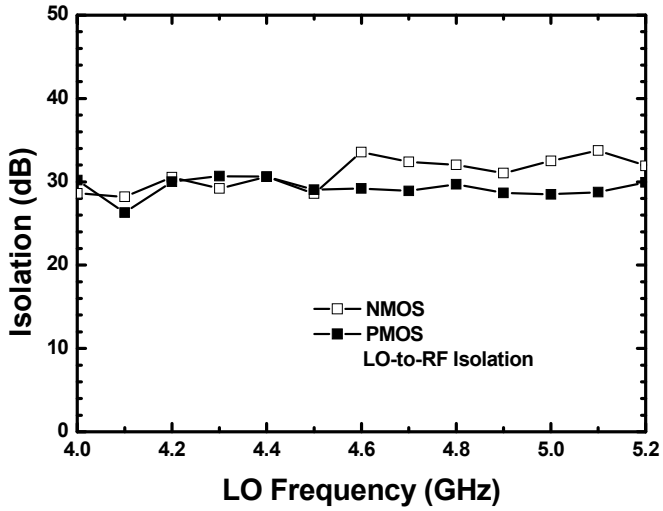


Fig. 2-11 LO-to-RF isolation.

The IF bandwidth of the upconverters with NMOS and PMOS TCAs are 500 MHz and 100 MHz, respectively, as shown in Fig. 2-10. The upconverter with a PMOS TCA has a 20.5-dB difference between the OIP_3 and OP_{1dB} which is larger than a 16.5-dB difference for the upconverter with an NMOS TCA at the cost of a narrower IF bandwidth for a similar gain design purpose. However, both designs are much more linear than a conventional Gilbert upconverter. The output RF return loss is better than 16 dB for both circuits over 20 GHz. The LO-to-RF isolation of each upconverter is better than 28/26 dB when LO frequency ranging from 4-5.2 GHz as shown in Fig. 2-11. The power consumption of each circuit is 40/46 mW, respectively. TABLE. 2.1 compares the proposed high-linearity Gilbert upconversion mixers using NMOS/PMOS TCA to the state-of-the-art circuits in literatures [8], [10]-[12].

TABLE. 2.1 PERFORMANCE COMPARISON OF THE GILBERT UPCONVERSION MIXERS

	w/ NMOS TCA	w/ PMOS TCA	[8]	[10]	[11]	[12]
RF (GHz)	4.4	4.4	5.2	5.8	5.8	5.2
Gain (dB)	−4	−6	1	−2.9	−2.9	−1
LO-to-RF Isolation (dB)	28	26	38	NR	NR	39
OP_{1dB} (dBm)	−11	−11	−10	−3.4	−3.4	−10
OIP_3 (dBm)	5.5	9.5	2	4.6	4.6	6
Supply Voltage (V)	3.5	3.3	5	V_{EE}= −2.7	V_{EE}= −2.7	3.3
Power Consumption (mW)	40	46	32.5	40.5	40.5	37.95
Technology	0.35μm SiGe HBT	0.35μm SiGe HBT	2μm GaInP/GaAs HBT	0.8μm SiGe HBT	0.8μm SiGe HBT	0.35μm SiGe HBT

2.2 DUAL-BAND HIGH-LINEARITY GILBERT UPCONVERSION MIXER

2.2.1 Dual-Band LC Current Combiner

For wireless communication systems, the current trend is toward multi-standards/multi-services, and thus it brings multi-band circuit design on a single chip, especially for dual-band (wireless local area network) WLAN applications [13]-[16]. Traditionally, it can be procured by using a dual-band filter cascaded after RF output stage at the cost of extra loss. However, in this section, a dual-band LC current combiner is introduced and applied at the load of the Gilbert upconversion mixers for a 2.4/5.7 GHz dual-band operation.

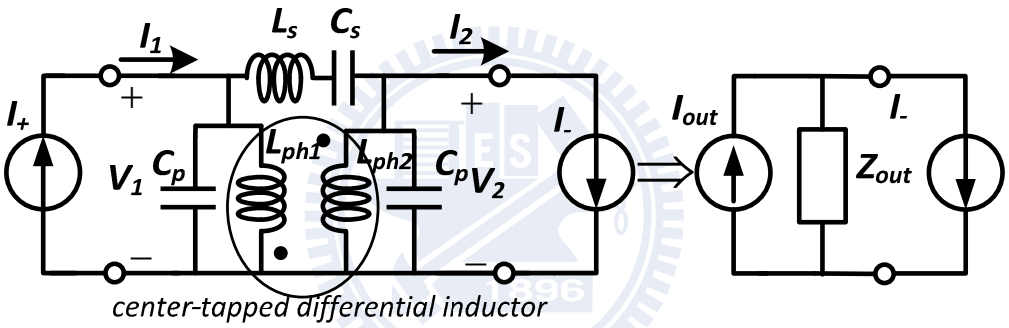


Fig. 2-12 Operational principle of the dual-band LC current combiner.

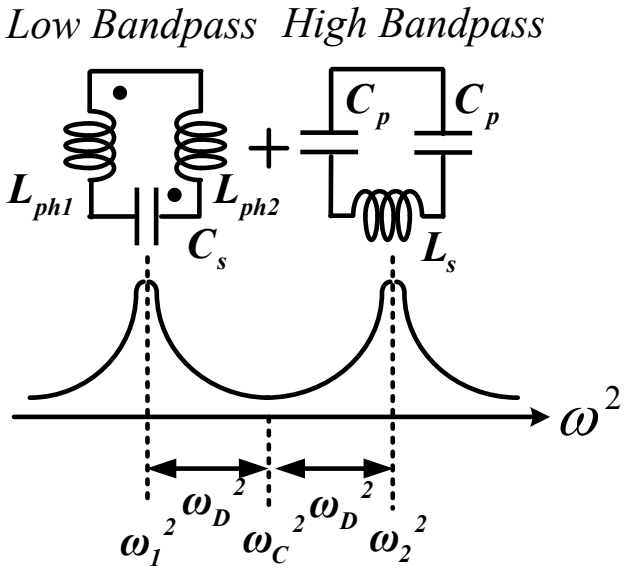


Fig. 2-13 Frequency response of a dual-band LC current combiner.

A single-band LC current combiner is introduced in Section 2.1.2. The dual-band version of the π-shaped LC current combiner is illustrated in Fig. 2-12. At low frequencies, the series branch is dominated by $1/j\omega C_S$ while the shunt branch is dominated by $1/j\omega L_{Ph1,2}$. On the other hand, the series and shunt branches are dominated by $j\omega L_S$ and $j\omega C_P$ at high frequencies, respectively. Therefore, the π-shaped dual-band LC current combiner can be treated implicitly as a combination of a low-frequency band-pass (L_{Ph1}, L_{Ph2}, and C_S) resonator and a high-frequency band-pass (L_S, C_P) resonator as shown in Fig. 2-13.

Using the same method applied to a single-band LC current combiner, the target frequency of current reversion can be obtained by letting $D=-1$,

where

$$D \equiv \left.\frac{I_2}{I_1}\right|_{V_1=0} = 1+\frac{L_S}{L_P}+\frac{C_P}{C_S}-\omega^2\left(C_P L_S\right)-\frac{1}{\omega^2 C_S L_P}. \tag{2.8}$$

At that frequency, $I_{total}=I_- - I_{out}= I_- + I_+ = 2I$ and ideally 6 dB gain improvement is obtained when compared to each output node of the Gilbert mixer.

When the element D of the ABCD matrix equals −1, *i.e.*,

$$\omega^4 L_P C_P L_S C_S - \left(L_P C_P + L_S C_S + 2L_P C_S\right)\omega^2 + 1 = 0. \tag{2.9}$$

$I_{out}=I_+$ is achieved, and therefore the equivalent total output current doubles. The roots of Eqn. (2.9) are ω_1 and ω_2, which can be found as

$$\omega = \sqrt{{\omega_C}^2 \pm {\omega_D}^2} \tag{2.10}$$

where

$${\omega_C}^2 \equiv \frac{{\omega_1}^2 + {\omega_2}^2}{2} = \frac{(L_P C_P + L_S C_S + 2L_P C_S)}{2L_P C_P L_S C_S} \tag{2.11}$$

and

$$\omega_D{}^2 \equiv \frac{\omega_2{}^2 - \omega_1{}^2}{2} = \frac{\sqrt{(L_P C_P + L_S C_S + 2L_P C_S)^2 - 4L_P C_P L_S C_S}}{2L_P C_P L_S C_S} \quad . \qquad (2.12)$$

The design procedure of the dual-band LC current combiner is as follows:

a) Define the dual-band frequencies ω_1 and ω_2. Thus the center frequency ω_C and difference frequency ω_D are specified by Eqns. (2.11) and (2.12).

b) Choose proper inductors (L_S and L_P) with high qualify factors at the desired frequencies.

c) Calculate the value of C_S and C_P by known ω_C and ω_D.

For the application on WLAN 802.11a/g, the two frequencies are specified as f_1= 2.4 GHz and f_2=5.7 GHz, respectively. The series capacitor C_S is decomposed into two capacitors with capacitance of $2C_S$ and these two capacitors are connected to each end of the floating inductor L_S for fully symmetric layout design. The lower limitation of inductances L_S and L_P are constraint by the achievable f_{Qmax} in practice while the capacitances of C_S and C_P are restricted by the severe parasitic effects. Consequently, $2C_S$=0.8 pF and C_P=1 pF and the inductances of L_P and L_S are 1.85 nH and 4.6 nH, respectively. In the dual-band LC current combiner, a 5-square-turn symmetric inductor (L_S) is 3 μm line width, 3 μm line spacing and outer diameter of 120 μm while a center-tapped symmetric differential inductor, L_P (consisting of L_{Ph1} and L_{Ph2}), is composed of a 5-square-turn with line width, spacing and outer diameter of 4, 2.5, and 120 μm, respectively. In real implementation of on-chip inductors, the output impedance of the dual-band resonator at resonance frequency of 2.4 GHz and 5.7 GHz are both 120 Ω, by Agilent Advanced Design System (ADS) simulation.

The following sections introduce two implementations using the proposed dual-band current combiner. Section 2.2.2 describes a dual-band upconverter with a conventional BJT differential amplifier as an input TCA while a bias-offset TCA

introduced in Section 2.1.1 is further applied in the dual-band upconverter with linearity improvement in Section 2.2.3.

2.2.2 Dual-Band Upconversion Mixer With a Dual-Band LC Current Combiner

The schematic of the 2.4/5.7-GHz dual-band Gilbert upconverter using 0.35-μm SiGe HBT technology is shown in Fig. 2-14. The proposed dual-band LC current combiner is applied at the output of the Gilbert mixer. The chosen of inductance, capacitance and the real geometric size of real implementations in the dual-band current combiner are introduced in Section 2.2.1. Moreover, the power improvement of the Gilbert upconverter is achieved by using the active matching network, the Darlington voltage buffer, in the output stage when compared to using a passive matching network [17].

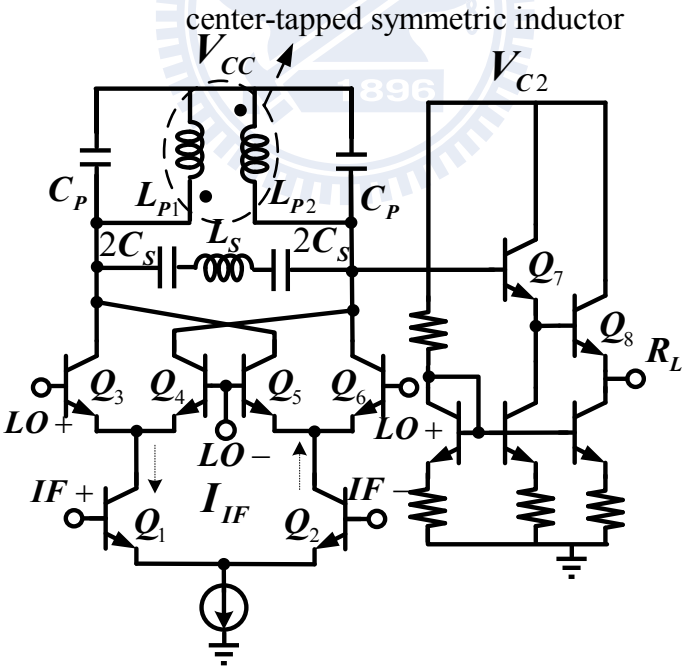


Fig. 2-14 Schematic of the 2.4/5.7 GHz Gilbert upconverter with a dual-band LC current combiner.

The die photo of the dual-band upconverter is shown in Fig. 2-15 and the die size is 1×1 mm^2.

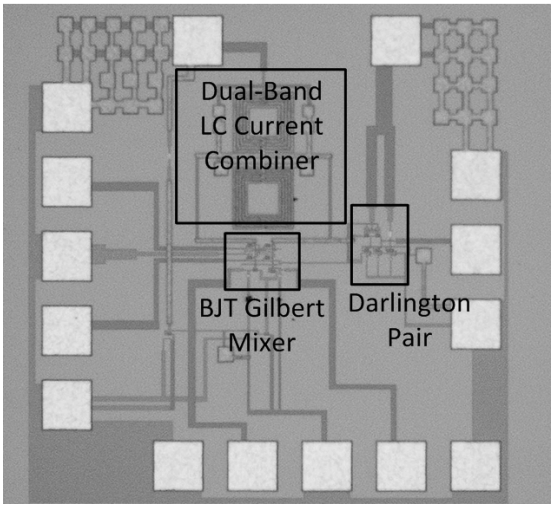


Fig. 2-15 Die photo.

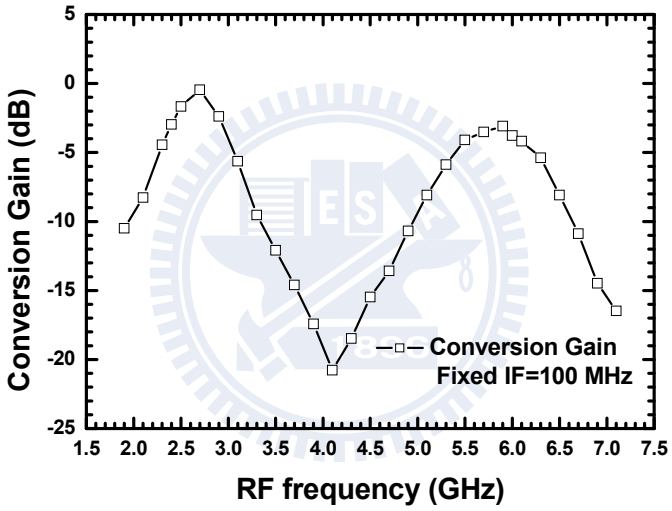


Fig. 2-16 Conversion gain with respect to RF frequency.

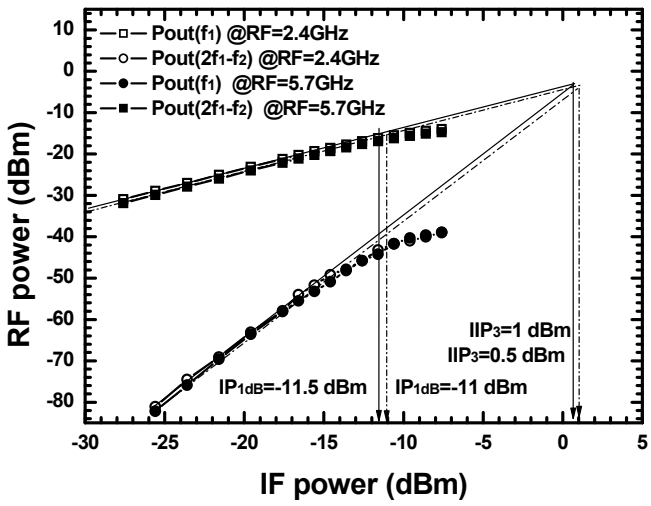


Fig. 2-17 Power performance.

Fig. 2-16 shows the conversion gain with respect to *RF* output frequency when *IF*=100 MHz. The measured conversion gain at desired frequencies of 2.4/5.7 GHz is −3/−3.5 dB with the *LO* input power of −4 dBm. However, the peak conversion gain is 0/−3 dB at 2.7/5.9 GHz due to the process variation. As shown in Fig. 2-17, the dual-band upconverter has the IP_{1dB} of −11.5/−11 dBm, and the IIP_3 of 0.5/1 dBm when IF=100 MHz, RF=2.4 GHz and 5.7 GHz, respectively. The power consumption is 49.5 mW at a 3.3-V supply.

2.2.3 2.4/5.7 GHz High-Linearity Gilbert Upconversion Mixer

The schematic of the 2.4/5.7 GHz dual-band SiGe BiCMOS Gilbert upconversion mixer is shown in Fig. 2-18. The upconverter in Fig. 2-18 consists of a SiGe HBT LO Gilbert mixer core (Q_1-Q_4), an IF bias-offset CMOS TCA (M_1-M_4), and an RF output dual-band LC current combiner with a SiGe HBT TIA output buffer (Q_5-Q_6).

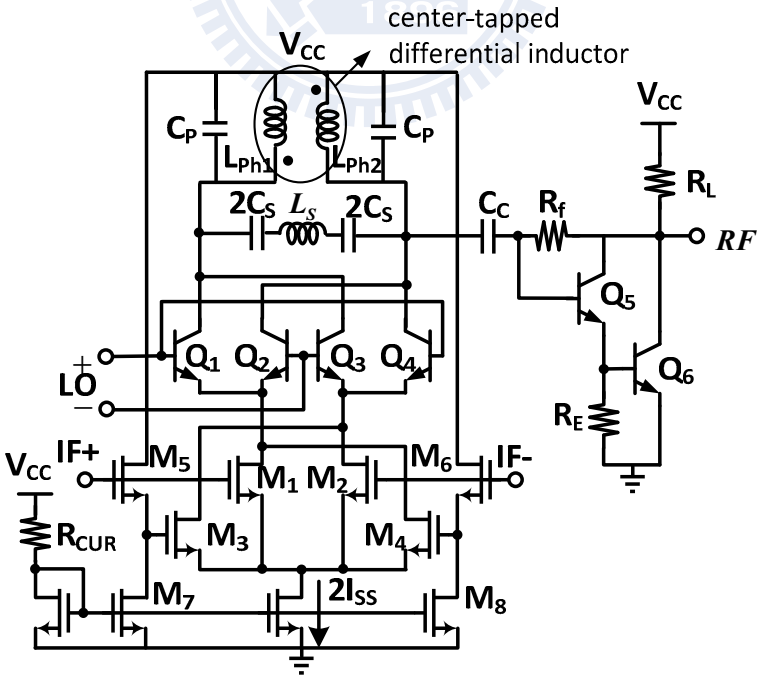


Fig. 2-18 Schematic of the SiGe BiCMOS dual-band Gilbert upconverter with the bias-offset TCA and dual-band LC current combiner.

As mentioned in Section 2.1.1, the transconductance of the TCA equals to $2kV_B$ as long as the NMOS I-V characteristics is in the square-law long channel region. The NMOS devices M_1-M_4 are biased at a small gate overdrive voltage and the gate lengths of the MOS transistors are 0.5 μm to mitigate the short channel effect. A shunt-shunt feedback TIA is employed in the output stage to achieve output matching. A wideband TIA with a 3dB bandwidth of 20 GHz is designed because strong feedback results in high linearity improvement. Passive matching output network is another choice [18].

The SiGe BiCMOS 2.4/5.7 GHz dual-band upconverter facilitates on-wafer rf measurements. Fig. 2-19 shows the die photo of the dual-band upconverter and the die size is 1.13×0.97 mm^2. The supply voltage is 3.5 V and the current consumption of the mixer core with the common-drain-configured M_5 and M_6 input buffers is 6.95 mA.

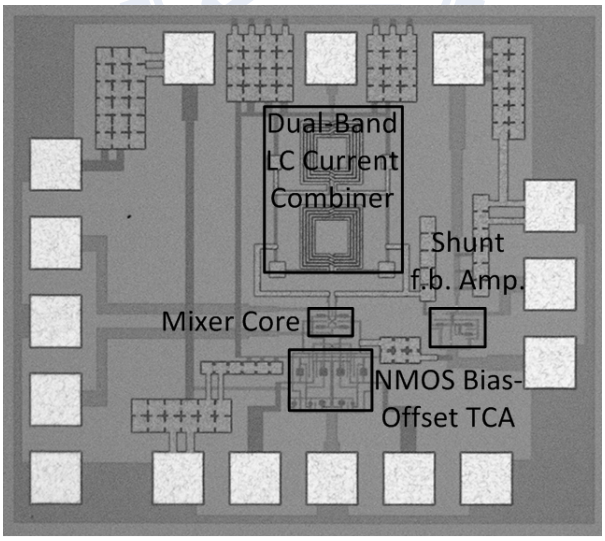


Fig. 2-19 Die photo.

In Fig. 2-20, the measured peak conversion gain at 2.4 GHz and 5.7 GHz is 1.5 and −0.2 dB, respectively, with 3dB bandwidth of 750 MHz when LO power is −5 dBm.

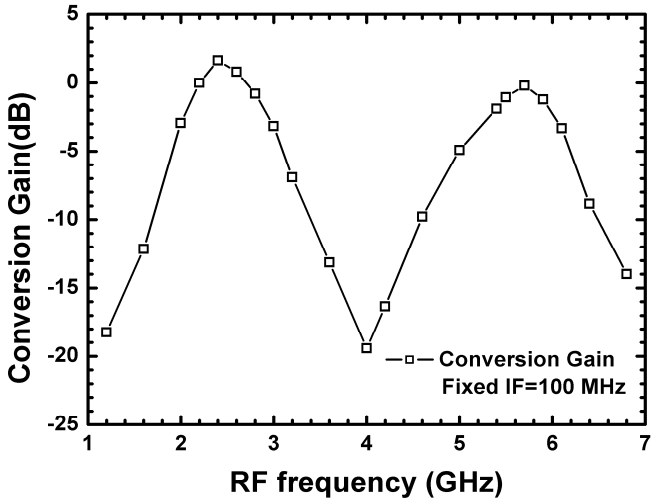


Fig. 2-20 Conversion gain as a function of RF frequency.

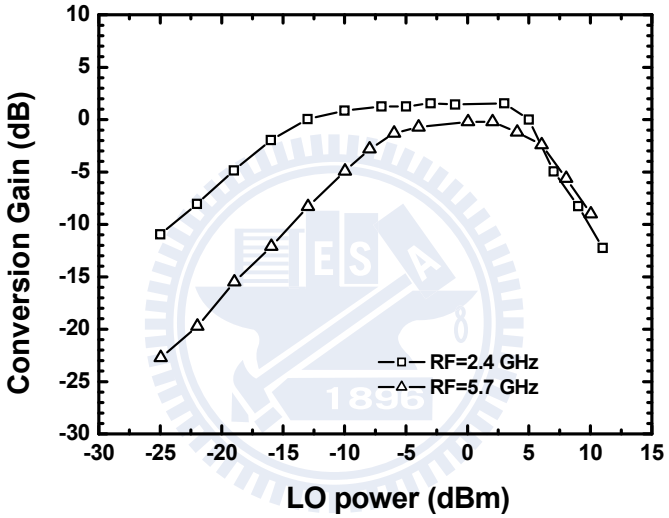


Fig. 2-21 Conversion gain with respect to LO power at RF=2.4 and 5.7 GHz.

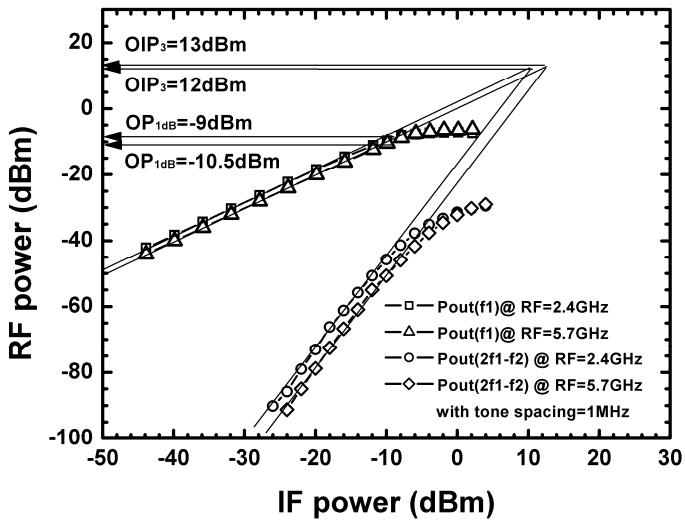


Fig. 2-22 Power Performance.

The measured conversion gain varies within 1 dB when LO power changes from –12 dBm to 4 dBm with RF=2.4 GHz, LO=2.3 GHz and IF=100 MHz while it changes from −6 dBm to 5 dBm with RF=5.7 GHz, LO=5.6 GHz and IF=100 MHz, as shown in Fig. 2-21. The output RF return loss is better than 13 dB at both 2.4/5.7 GHz. The power performance of the dual-band upconverter is illustrated in Fig. 2-22. It has OP_{1dB} of −10.5/−9 dBm, and OIP_3 of 12/13 dBm when input IF=100 MHz, RF=2.4 GHz and 5.7 GHz respectively. The measured LO-to-RF isolation is 38/43 dB when LO=2.3 GHz and 5.6 GHz, respectively. The difference between OIP_3 and OP_{1dB} can be used to indicate the linearity and our work shows excellent linearity of 22 dB difference between OIP_3 and OP_{1dB}.

TABLE. 2.2 summarizes the comparison of the proposed Gilbert upconversion mixer using bias-offset TCA in this section and that using conventional BJT differential pair introduced in Section 2.2.2. It is obvious that the difference between OIP_3 and OP_{1dB} is improved by around 9 dB when using a bias-offset TCA to replace the conventional BJT differential pair.

TABLE. 2.2 PERFORMANCE COMPARISON OF THE DUAL-BAND UPCONVERTERS WITH/WITHOUT BIAS-OFFSET TCA

	w/ Bias-Offset TCA	w/ BJT Differential Pair TCA
RF (GHz)	2.4/5.7	2.4/5.7
Gain (dB)	1.5/−0.2	−3/−3.5
LO-to-RF Isolation (dB)	38/43	30/32
OP_{1dB} (dBm)	−10.5/−9	−15.5/−15.5
OIP_3 (dBm)	12/13	−2.5/−2.5
Supply Voltage (V)	3.5	3.3
Power Consumption (mW)	45	49.5
Technology	0.35μm SiGe HBT	0.35μm SiGe HBT

Chapter 3 Passive Quadrature Signal Generations and Their Applications on BJT-based Gilbert Mixers

3.1 Passive Quadrature Signal Generation

A quadrature signal generation with accurate amplitude and phase is always an important issue for communication systems, *e.g.*, quadrature up/down conversion mixers [19] and sub-harmonic mixers (SHMs) [20], because the quadrature accuracy determines the bit-error rate (BER) performance.

Typically, there are four main methods for generating quadrature signals:

1) A frequency divider,
2) a quadrature voltage-controlled oscillator (QVCO),
3) distributed elements, *e.g.*, a quarter-wavelength coupler or a branch-line coupler,
4) lumped elements, *e.g.*, an RC-CR, LR-CR phase shifter and even a poly-phase filter (PPF).

An even-modulus divider, *e.g.*, a divide-by-two divider, can generate accurate quadrature signals but it requires an input signal with twice the *RF* frequency and an extra dc power consumption. However, its wideband performance and excellent accuracy are very attractive and thus is widely used in real applications [14], [21]. On the other hand, a QVCO suffers from a strong trade-offs between quadrature phase accuracy and phase noise performance. Thus, it is difficult to achieve both of them at the same time [22]-[24]. A passive coupler has an advantage over the lumped circuits especially at high frequencies; however, it occupies a bulky area at low frequencies [25], *e.g.*, below 10 GHz. Passive realizations using either distributed or lumped components have unavoidable power loss. However, when applying to low-frequency

circuits, the voltage relation is more important than the power relation because the input/output terminals no longer need to be 50 Ω. When considering the impedance transformation, the PPF may even has voltage gain [26]. This chapter focuses on the passive quadrature signal generation including both distributed and lumped realizations. To further analyze the quadrature signal accuracy, phasor and complex representations of real signals are introduced in Section 3.1.1 while Section 3.1.2 and Section 3.1.3 describe the distributed and lumped passive quadrature generators, respectively. In Section 3.2, passive quadrature generators are applied to BJT Gilbert mixers, which have a wide flat-gain region and provide additional tolerance on LO amplitude imbalance. Thus, 5.7-GHz I/Q downconversion mixers with LO quadrature couplers are implemented in Section 3.2.1 while Section 3.2.2 introduces UWB I/Q downconversion mixers using LR-CR LO quadrature generators.

3.1.1 Phasor and Complex Representations for Real Signals

A phasor ($\vec{v} = Ae^{j\theta}$) includes the information of amplitude (A) and phase (θ) of a real signal. As indicated in Fig. 3-1(a), an arbitrary phasor sequence (four vectors) can be decomposed into four balanced sequences [26]-[27]:

1) quadrature counterclockwise (right-handed) sequence $\vec{R}$,

2) quadrature clockwise (left-handed) sequence $\vec{L}$,

3) collinear differential sequence $\vec{D}$, and

4) collinear in-phase sequence $\vec{I}$.

A differential amplitude/phase imbalance affects the isolation and second-order nonlinearity significantly, but not gain or image rejection [26]. Therefore, assuming a phasor sequence is fully differential for simplicity, the phasor sequence is simply a linear combination of a right-handed sequence $\vec{R}$ and a left-handed sequence $\vec{L}$. The right-handed sequence $\vec{R}$ (0°,90°,180°,270°) can be denoted as a complex signal

exp(*j*ωt), while the left-handed sequence $\vec{L}$ (0°,270°,180°,90°) represents exp(-*j*ωt) [28].

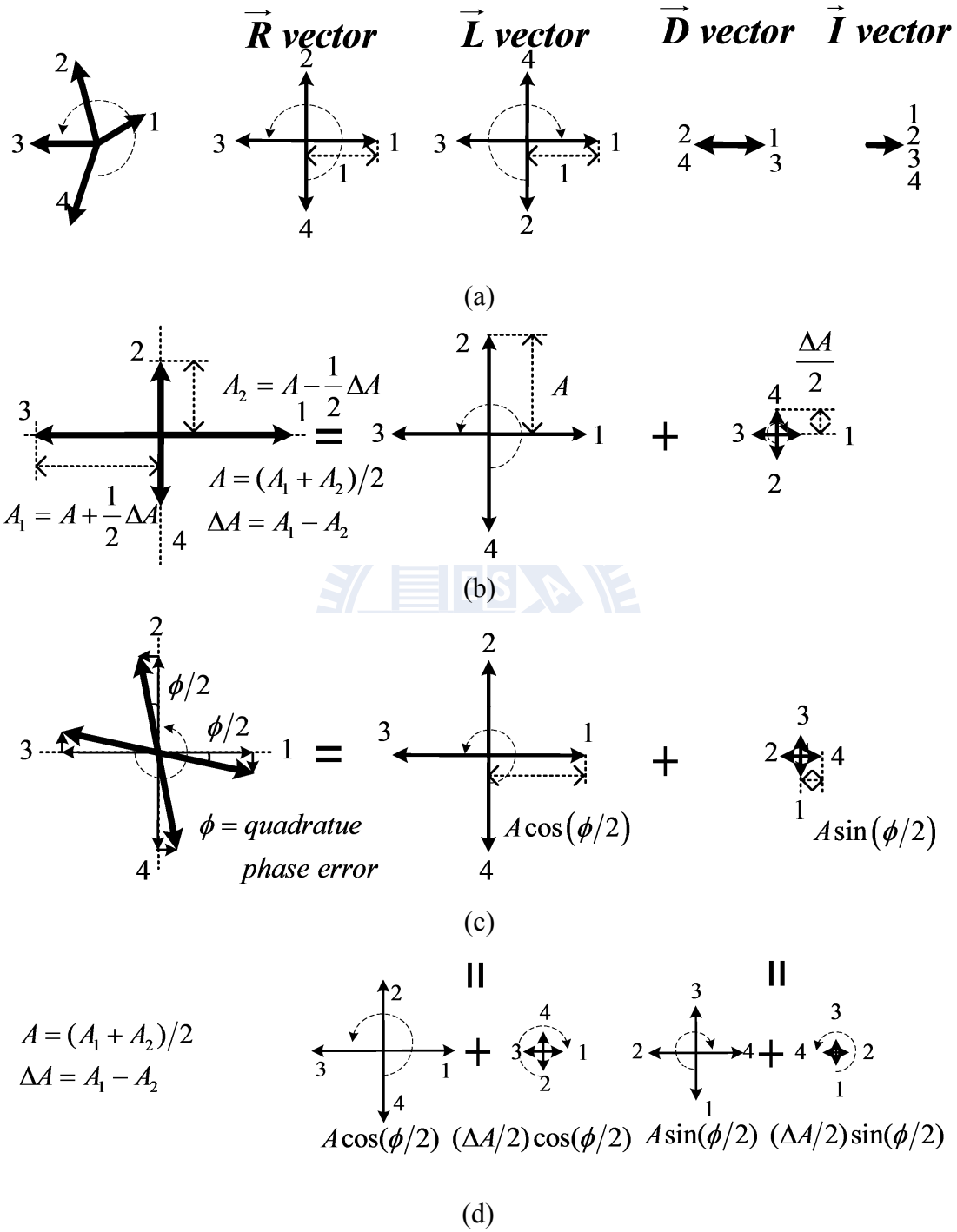


Fig. 3-1 (a)Balanced phasor sets $\vec{R}, \vec{L}, \vec{D}$ and $\vec{I}$ (b) phasor set with amplitude imbalance (ΔA) (c) phasor set with quadrature phase error (ϕ) (d) phasor set with both phase and amplitude imbalance.

In addition, an error function (ε) is defined as an amplitude ratio of $\vec{L}$ and $\vec{R}$ to

facilitate the analysis throughout the paper. Since a downconverted image signal is at the opposite spectrum of a desired signal, the reciprocal of the error function is equal to the image-rejection ratio (IRR).

For example, a phasor sequence with unbalanced amplitudes ($A_1 = A + \Delta A/2$ and $A_2 = A - \Delta A/2$) as shown in Fig. 3-1(b) can be decomposed into

$$\vec{V} = A\vec{R} + \Delta A/2\,\vec{L} \tag{3.1}$$

with an error function

$$\varepsilon_r = \left|\frac{\Delta A}{2A}\right| = \left|\frac{A_1 - A_2}{A_1 + A_2}\right|. \tag{3.2}$$

Similarly, a phasor sequence with a balanced amplitude (A) but a quadrature phase error (ϕ) as shown in Fig. 3-1(c) can be decomposed into

$$\vec{V} = A\cos(\phi/2)\vec{R} - jA\sin(\phi/2)\vec{L} \tag{3.3}$$

with an error function

$$\varepsilon_\phi = \left|\tan(\phi/2)\right|. \tag{3.4}$$

Generally, a phasor sequence with both amplitude imbalance and phase error as shown in Fig. 3-1(d) can be decomposed into

$$\vec{V} = \left[\cos(\phi/2)A - j\sin(\phi/2)(\Delta A/2)\right]\vec{R} + \left[\cos(\phi/2)(\Delta A/2) - j\sin(\phi/2)A\right]\vec{L} \tag{3.5}$$

Hence, an overall error function becomes

$$\varepsilon_{r,\phi} = \left|\frac{\varepsilon_r - j\varepsilon_\phi}{1 - j\varepsilon_\phi\varepsilon_r}\right| = \sqrt{\frac{\varepsilon_r^2 + \varepsilon_\phi^2}{1 + \varepsilon_r^2\varepsilon_\phi^2}}\,. \tag{3.6}$$

It is evident that either a phase error or an amplitude imbalance produces an opposite phasor sequence. It is worthwhile to mention that the reciprocal of calculated result $\left|\varepsilon_{r,\phi}\right|^2$ is the IRR in an image-rejection receiver described in Eqn. (5.15) [29] with LO quadrature amplitude/phase mismatches

$$IRR = \frac{A_1^2 + 2A_1A_2\cos\phi + A_2^2}{A_1^2 - 2A_1A_2\cos\phi + A_2^2} \tag{3.7}$$

where $(A_1^2 + A_2^2) = 2A^2(1+\varepsilon_r^2)$, $2A_1A_2 = 2A^2(1-\varepsilon_r^2)$, and $\cos\phi = (1-\varepsilon_\phi^2)/(1+\varepsilon_\phi^2)$.

3.1.2 Distributed Quadrature Signal Generation Method(Quadrature Coupler)

S parameters of a quarter-wavelength (λ/4) coupler indicate a voltage gain from the input port to the through port (S_{21}) and to the coupled port (S_{31}), respectively. By dividing the two outputs,

$$\begin{aligned}\frac{S_{21}}{S_{31}} = \frac{Q}{I} &= \sinh\gamma\frac{k}{\sqrt{1-k^2}} \\ &= \frac{k}{\sqrt{1-k^2}}\frac{\sin(\beta l)}{\cosh(\alpha l)}\sqrt{1+\frac{\tanh^2(\alpha l)}{\tan^2(\beta l)}}e^{j\tan^{-1}\left[\tan(\beta l)/\tanh(\alpha l)\right]} \\ &= j\frac{k}{\sqrt{1-k^2}}\sin(\beta l)\ (if\ \alpha = 0)\end{aligned} \tag{3.8}$$

where $r=\alpha+j\beta$, $\beta l = \frac{2\pi}{\lambda}l = \frac{\pi}{2}\frac{\lambda_0}{\lambda} = \frac{\pi}{2}\frac{f}{f_0}$ with $l=\lambda_o/4$.

Thus, the phase difference is always 90° on a lossless condition; however, the amplitude is determined by the operating frequency (*f*) and the coupling factor $k=(Z_{0e}-Z_{0o})/(Z_{0e}+Z_{0o})$, where Z_{oe} and Z_{oo} are the even-mode and odd-mode characteristic impedances, respectively. Thus, the equivalent error function is

$$\varepsilon = \left|\frac{x-1}{x+1}\right| \tag{3.9}$$

where $x = \frac{k}{\sqrt{1-k^2}}\sin(\frac{\pi}{2}\frac{f}{f_0})$.

The quadrature phase maintains with arbitrary output loadings for *C* and *T* ports if and only if the characteristic impedance (Z_o) of the coupler is 50 Ω=Z_{inc}=Z_{iso}.

A λ/4 coupled-line coupler with different coupling factor *k* has different bandwidth on the same image-rejection criterion (*e.g.*, 40 dB IRR; ε=0.01). Since the

maximum amplitude imbalance occurs at the center frequency. Thus, the maximum ε equals to

$$\varepsilon_{\max} = \left| \frac{k - \sqrt{1-k^2}}{k + \sqrt{1-k^2}} \right| , \tag{3.10}$$

and thus, for the criterion of $\varepsilon_{\max}$, the required coupling coefficient will be

$$k_{\max} = \frac{1+\varepsilon}{\sqrt{2(1+\varepsilon^2)}} . \tag{3.11}$$

For example, a 3-dB coupler without amplitude imbalance (i.e., $\varepsilon_{\max}$=0), the $k_{\max}$ should be $1/\sqrt{2}\,(=0.707)$ but the perfect balanced amplitude and phase only occur at the center frequency. A higher coupling results in a wider bandwidth under a given tolerable $\varepsilon_{\max}$. To achieve a higher coupling, a broadside-coupled coupler or an Lange coupler can be utilized [30]. Moreover, multiple sections of λ/4 coupled-line couplers with a properly designed characteristic impedance of each section are cascaded to cover a much wider bandwidth [30]. However, the huge area arises much production cost for chip implementation.

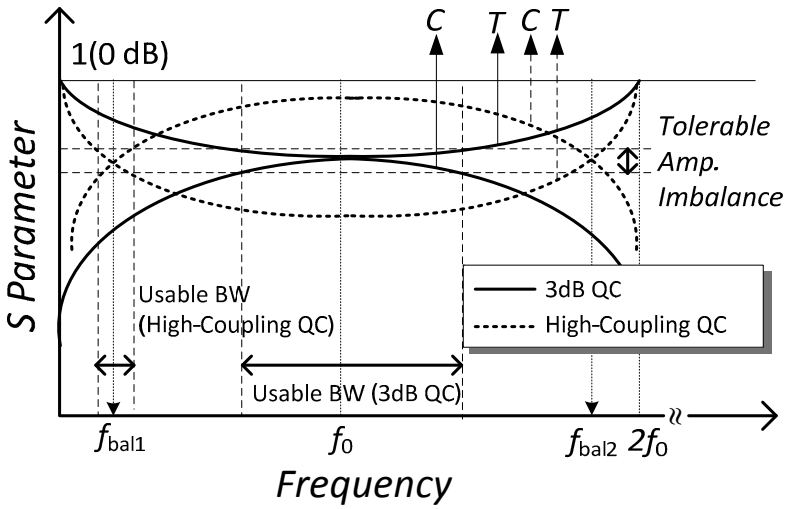


Fig. 3-2 Description of the S parameters for a 3-dB quadrature coupler and a high-coupling quadrature coupler.

As mentioned earlier, the conventional quadrature coupler is implemented by a

quarter-wavelength coupled line [68]. As a result, the 3-dB quadrature coupler is realized with a coupling factor of $1/\sqrt{2}$ and the description of the S parameters is shown in Fig. 3-2. To widen the bandwidth, the coupling factor can be chosen larger if the amplitude imbalance between the coupled and through ports is still tolerable. It is noteworthy that the phase difference between these two ports of a quarter-wavelength quadrature coupler under the lossless condition is always 90° [68].

However, another design concept is proposed for miniaturization. A high coupling factor (~0.85) results in a significant amplitude difference at the center frequency (f_0) and the perfect balanced amplitudes occur at two frequencies, f_{bal1} and f_{bal2}, as shown in Fig. 3-2. If the f_{bal1} is chosen for the usage frequency, the coupler can be very compact since the center frequency of the coupler is several times the operating frequency. However, the bandwidth is relatively narrow. The high coupling factor can be achieved by using a broadside-coupled quadrature coupler, consisting of two spiral inductors using metal 6 and metal 5 (in 0.18-μm CMOS technology). The dielectric thickness between metal 6 and metal 5 is 0.8 μm, which is much less than the 3-μm line spacing of the inductor; thus, the broadside-coupling is dominant.

When considering metal loss or substrate loss, *i.e.*, α=attenuation constant≠0 in practice, the perfectly quadrature phase no longer maintains and thus the amplitude/phase accuracy trade-offs increase. However, a BJT mixer can tolerate the LO amplitude imbalance and thus the lossy quadrature coupler can be designed for perfect quadrature phase, which will be introduced in Section 3.2.1.

3.1.3 Lumped Quadrature Signal Generation Methods

Instead of the microwave realizations, lumped quadrature signal generators are widely used at low frequencies. Traditionally, there are two primary kinds of methods for a quadrature signal generation:

1) constant quadrature phase architecture,

2) balanced amplitude architecture.

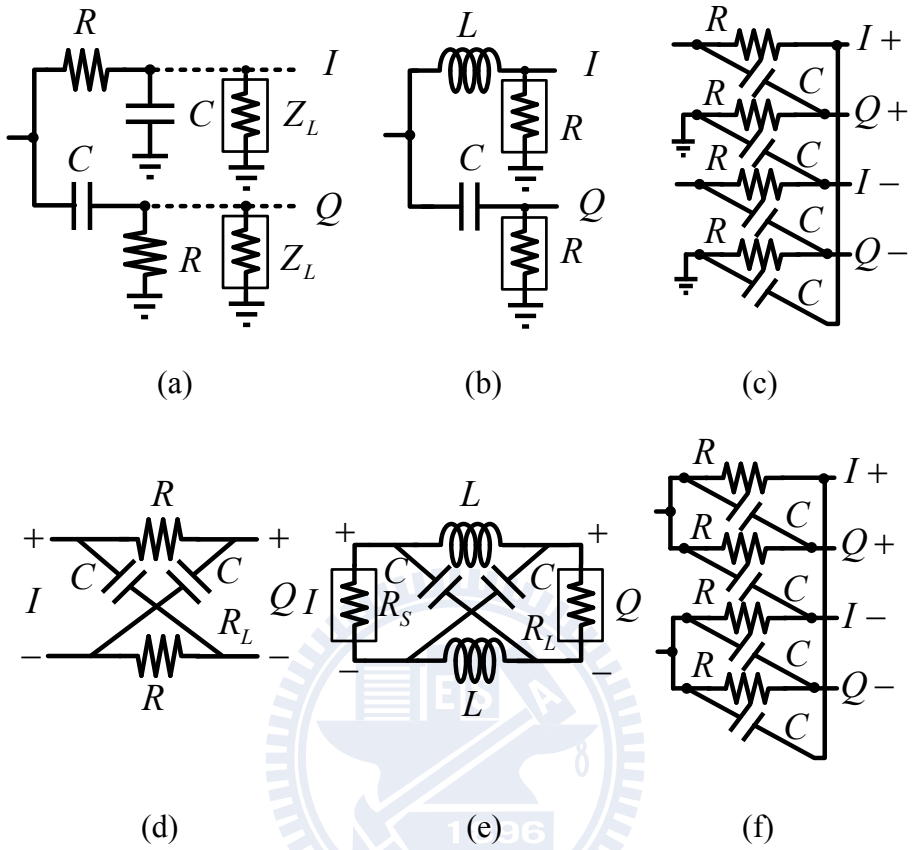


Fig. 3-3 (a) RC-CR phase shifter (b) LR-CR phase shifter (c) PPF with Q input shorted to ground (d) RC-CR all-pass filter (APF) topology (e) LR-CR APF topology and (f) a PPF with I/Q input connected together.

An RC-CR phase shifter [Fig. 3-3(a)], an LR-CR phase shifter [Fig. 3-3(b)], and a PPF with Q input shorted to ground [Fig. 3-3(c)] belong to the former type while the latter type includes an RC-CR all-pass filter (APF) topology [Fig. 3-3(d)], an LR-CR APF topology [Fig. 3-3(e)], and a PPF with I/Q input connected together [Fig. 3-3(f)].

An RC-CR phase shifter and an LR-CR phase shifter have the same quadrature output ratio

$$\frac{Q(\omega)}{I(\omega)} = j\frac{\omega}{\omega_0} = \left|\frac{\omega}{\omega_0}\right| e^{j90^\circ} . \tag{3.12}$$

The output phasor sequence belongs to a constant-quadrature-phase sequence,

illustrated in Fig. 3-1(b); thus, by Eqn. (3.2), the error function becomes

$$\varepsilon_0(\omega) = \left|\frac{\Delta A}{2A}\right| = \left|\frac{|Q|-|I|}{|Q|+|I|}\right| = \left|\frac{\omega-\omega_0}{\omega+\omega_0}\right| \tag{3.13}$$

where $\omega_0 = 1/RC$ for the RC-CR topology but $\omega_0 = 1/\sqrt{LC}$ for the LR-CR topology.

For an RC-CR phase shifter, the output quadrature phase maintains at every frequency with arbitrary loadings if the two loadings are the same, but the result holds for an LR-CR topology only when the load impedance equals $\sqrt{L/C}$.

The ratio of V_Q (*CR*-path) and V_I (*LR*-path) can be described as

$$\frac{V_Q}{V_I} = \frac{R+j\omega L}{R+1/j\omega C} = \frac{1+j\dfrac{\omega}{\omega_o}}{1-j\dfrac{\omega_o}{\omega}} = j\frac{\omega}{\omega_o} \tag{3.14}$$

where $L=R/\omega_0$ and $C=1/(\omega_0 R)$. That is $\omega_0 = 1/\sqrt{LC}$, $R=\sqrt{L/C}$.

Besides, the input impedance of the *LR-CR* quadrature generator is

$$Z_{inLO} = (R+j\omega L)//\left(R+1/j\omega C\right) = R\left[(1+j\frac{\omega}{\omega_o})//(1-j\frac{\omega_o}{\omega})\right] = R \ , \tag{3.15}$$

which is always equals to the load impedance (R) under the balanced condition.
Note that, no power loss is necessary for the LR-CR topology since all reactive components are used when compared with the lossy RC-CR phase shifter.

A single-stage PPF with Q input shorted to the ground is a differential variant of an RC-CR phase shifter; thus the same quadrature output ratio $Q/I=j\omega/\omega_0$ and error function $|\varepsilon|=|(\omega-\omega_0)/(\omega+\omega_0)|$ can be obtained straightforwardly.

On the other hand, the APF variant for an RC-CR topology and its differential type (PPF with I/Q input connected) have a quadrature output ratio of

$$\frac{Q(\omega)}{I(\omega)} = \frac{1+sRC}{1-sRC} = \frac{1+j\,\omega/\omega_0}{1-j\omega/\omega_0} = e^{j\left[2\tan^{-1}(\omega/\omega_0)\right]} = e^{j(90°+\phi)} \tag{3.16}$$

where $\phi/2 = \tan^{-1}(\omega/\omega_0) - 45°$.

Therefore, output phasor sequence has balanced amplitudes but a phase error the same as Fig. 3-1(c). By Eqn. (3.4), the error function becomes

$$\varepsilon_0(\omega) = \left|\tan(\phi/2)\right| = \left|\frac{\omega - \omega_0}{\omega + \omega_0}\right|. \tag{3.17}$$

By the same token, an LR-CR APF topology has the same quadrature output ratio and error function as the RC-CR APF topology on an additional condition that the source/load impedances are equal to $\sqrt{L/C}$.

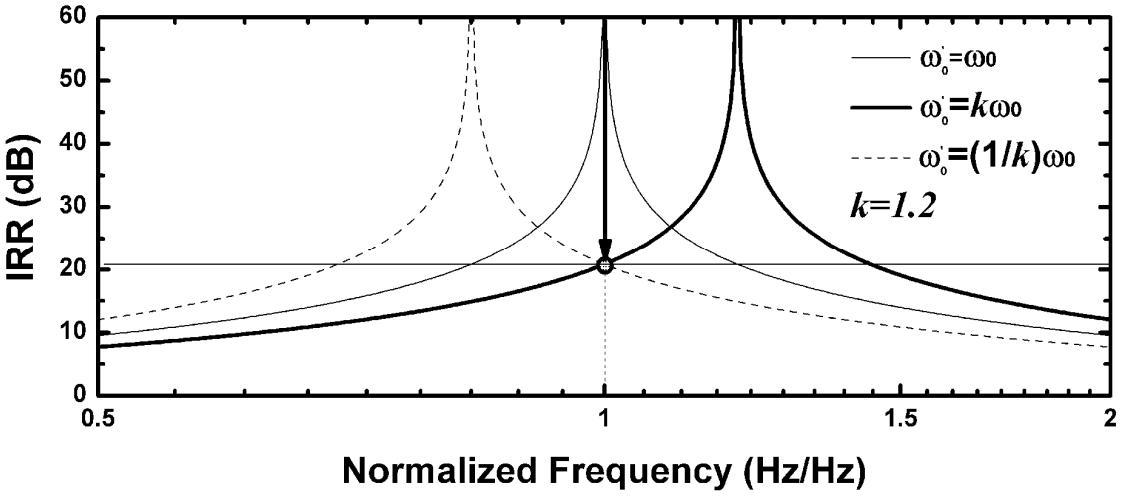


Fig. 3-4 IRR with a pole frequency deviation due to a process variation.

Moreover, Fig. 3-4 shows the correspondent IRR ($=-20\log|\varepsilon_o|$) of the lumped quadrature generator (*e.g.*, PPF) with a center frequency variation due to process variation. If a center frequency varies 20%, the IRR is drastically degraded to only 20.8 dB. Therefore, the process variation should be taken into account when deciding a sufficient IRR bandwidth.

However, multiple PPFs can be cascaded and thus extend the bandwidth but the LR-CR topology can not. The followings are the discussion of multi-band and wide-band extensions by using a multi-stage PPF.

The transfer function of a single-stage PPF [Fig. 3-3(f)] with a balanced quadrature phasor sequence ($\vec{R}$ or $\vec{L}$) is expressed as

$$A_{Vo\pm}(\omega) = \frac{1 \pm \omega/\omega_0}{1 + j(\omega/\omega_0)} \tag{3.18}$$

where $\omega_0=1/RC$ is the transmission zero of A_{Vo-} and also the pole frequency of both A_{Vo+} and A_{Vo-} .

Thus, the equivalent error function is defined as

$$\varepsilon_0(\omega) \equiv \left|\frac{A_{Vo-}}{A_{Vo+}}\right| = \left|\frac{\omega - \omega_0}{\omega + \omega_0}\right|. \tag{3.19}$$

For a quadrature signal generation, the input differential signal can be decomposed into $\vec{R}$ and $\vec{L}$ with the same amplitudes; thus, the output error function has the same meaning as the ratio of negative and positive signal gain, defined in Eqn. (3.19). For a multi-stage PPF with a balanced quadrature phasor sequence ($\vec{R}$ or $\vec{L}$), the transfer function can be expressed as

$$A_{V\pm}(\omega) = \prod_{i=1}^{N} A_{Voi\pm}(\omega)\frac{Z_{Li}}{Z_{Si} + Z_{Li}} \quad , \tag{3.20}$$

and its correspondent error function can thus be expressed as

$$\varepsilon = \frac{\prod_{i=1}^{N}\left|A_{Voi-}(\omega)\right|}{\prod_{i=1}^{N}\left|A_{Voi+}(\omega)\right|} = \prod_{i=1}^{N}\left|\frac{\omega - \omega_i}{\omega + \omega_i}\right| \tag{3.21}$$

where $A_{Voi\pm}(\omega)$ is the open-circuited voltage gain of the i_{th}-stage PPF, defined by Eqn. (3.18); $Z_{\text{Si}}/Z_{\text{Li}}$ is the equivalent source/load impedance of the i_{th} stage.

The A_{Vo+} of each stage is larger than 1 and reaches the maximum value of $\sqrt{2}$ at the center frequency. Thus, the impedance ratio between each stage and the input/output impedance dominate the overall voltage gain/loss. On the other hand, the voltage gain of the A_{Vo} has a transmission zero and results in a narrow-band rejection

response.

With different locations of transmission zeros of a multi-stage PPF, there are three typical circumstances:

1) narrow-band ($\omega_{max}/\omega_{min}\rightarrow 1$),

2) wide-band ($\omega_{max}/\omega_{min}>>1$), and

3) multi-band applications.

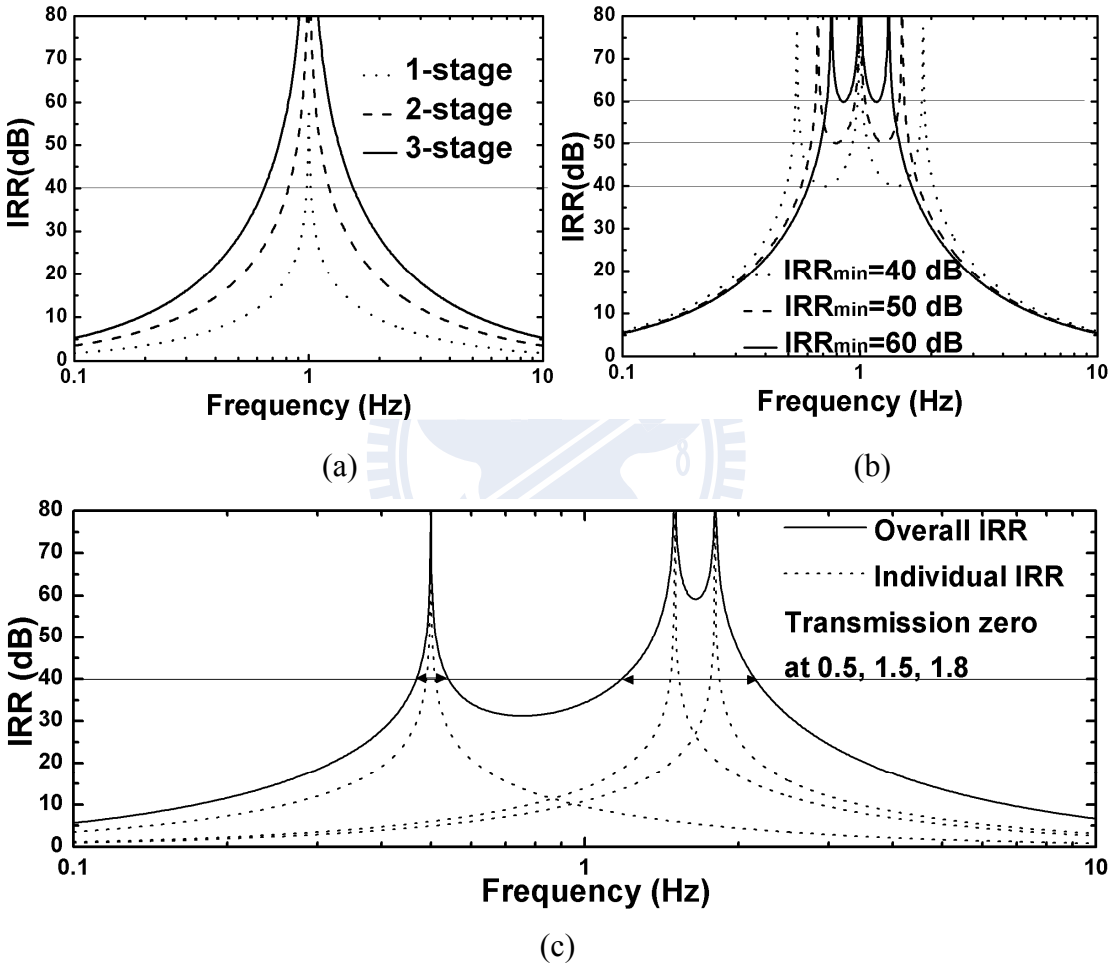


Fig. 3-5 Three-stage PPF on different pole locations (a) equal RC pole (b) unequal RC poles with an equiripple frequency response and (c) unequal RC poles for multi-band applications.

1) For a narrow-band application, all the transmission zeros are identical, ω_0; thus, an *N*-stage PPF provides a total error of $\varepsilon = \varepsilon_0^N$, thus the error is reduced with increasing cascading stages as shown in Fig. 3-5(a). In other words, for a given tolerable IRR

(−20log|ε|), the ratio bandwidth becomes

$$\frac{\omega_{\max}}{\omega_{\min}} = \left(\frac{1+\varepsilon^{1/N}}{1-\varepsilon^{1/N}}\right)^2 = \left(\frac{1+\varepsilon_0}{1-\varepsilon_0}\right)^2 \tag{3.22}$$

where ε is the target error function after the PPF, ε_o is the error function of one-stage PPF, and N is the number of stages.

Thus, for a target 40-dB IRR (ε=0.01) of a quadrature generator, the ratio bandwidth becomes 1.041, 1.494 and 2.4 for single-stage, two-stage and three-stage PPFs, respectively.

In addition, the voltage gain (or loss) of a multi-stage PPF with the same center frequency can be calculated. By Eqn. (3.20), the voltage gain of an *N*-stage PPF at the center frequency can be expressed as

$$\begin{aligned} \left|A_{Vo+}(\omega_0)\right| &= \left|\prod_1^n \frac{1+\omega/\omega_0}{1+j\,\omega/\omega_0} \prod_1^n \frac{Z_{(i+1)}}{Z_{(i+1)}+Z_{(i)}}\right| \\ &= 2^{n/2} \prod_{i=1}^n \frac{1}{1+R_{(i)}/R_{(i+1)}} \end{aligned} \tag{3.23}$$

where $Z_{(i)}(\omega_0) = R_i/(1+j) = 1/\left[\omega_0 C_i (1+j)\right]$, $\omega_0 = 1/R_i C_i$, $\forall i \in \{1,2,...,N\}$ and $Z_{N+1} = Z_L = \infty$.

Eqn. (3.23) shows that the increase of resistance lessens the voltage loss when the last stage is open-circuited [26]. However, in reality, the loading of the PPF is the gate (base) of the active mixer core with capacitive impedance of $1/sC_L$. Thus, the input impedance is typically open-circuited at low frequencies but degrades at high frequencies. The voltage gain should be modified as

$$\left|A_{V+}(\omega_0)\right| = \left|A_{Vo+}(\omega_0)\frac{Z_L}{Z_N+Z_L}\right| = \left|A_{Vo+}(\omega_0)\right| \sqrt{\frac{2}{1+(1+C_L/C_N)^2}} \,. \tag{3.24}$$

Although the increase of resistance can increase A_{Vo+}, the small capacitance at the N_{th} stage (C_N), resulting from a high resistance (R_N), may degrade the overall voltage gain, especially at high frequencies. Thus, an optimum voltage gain always exists if the source impedance (Z_S) and the output loading capacitance (C_L) are given.

2) For a wide-band application, a multi-stage PPF with logarithmic increase of pole locations results in an equiripple image rejection frequency response as shown in Fig. 3-5(b). The derivation of optimum pole locations for a minimum IRR of an *N*-stage PPF had been proposed for a given ratio bandwidth $\omega_{max}/\omega_{min}$ [26]. Thus, for a target IRR, the number of stages and the pole locations can be defined [26].

3) Finally, for a multi-band quadrature generation, each stage of a PPF is set at different desired frequencies as shown in Fig. 3-5(c). The image-rejection bandwidth becomes wider when compared to the individual response because the distant away transmission zeros still provide certain effect on a given band. Certainly, detailed information on gain and IRR bandwidth can be obtained by simulation tools.

The wideband and multi-band extensions are applied in Section 5.2 for further improvement of image rejection in a low-IF downconverter.

3.2 APPLICATIONS ON BJT GILBERT MIXERS

A Gilbert mixer, especially with a bipolar mixing core [31], has a region of flat gain as a function of the LO input power because around four times the thermal voltage ($4V_T \approx 0.1V$) is needed to make current commutate in emitter-coupled differential pairs. Typically, there is a flat-gain region of around 5 to 10 dB. Fig. 3-6 illustrates the conversion gain versus LO input power for two identical Gilbert mixers with different LO path loss. The curve B in Fig. 3-6 is the right-shifted version of the curve A because the LO path loss of the curve B is larger than that of the curve A. It shows that the Gilbert mixer is tolerant of different LO path loss if the LO input

power is in the common overlapped range shown in Fig. 3-6.

This advantage of a Gilbert mixer is more significant in BJT switching core than CMOS switching core because a CMOS differential pair requires $\sqrt{2}V_{OV}$ to make the current fully switch. Thus, a wider flat-gain regain is obtained using BJT core and thus much amplitude imbalance is tolerable.

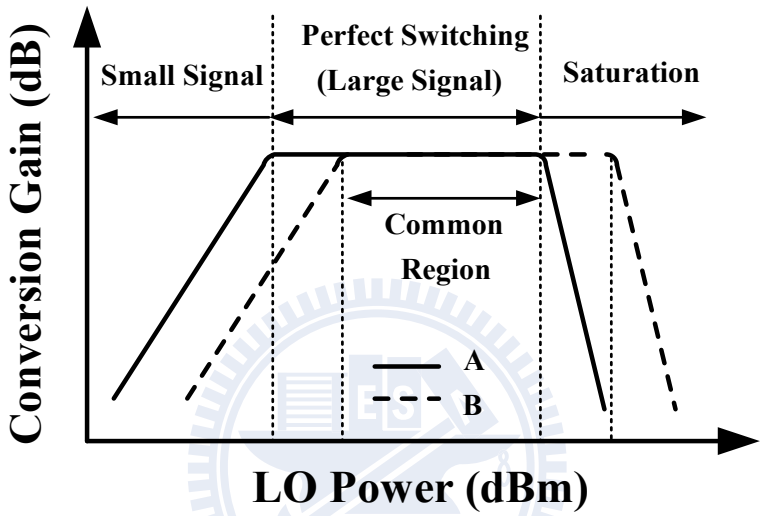


Fig. 3-6 Conversion gain versus LO power of two identical Gilbert mixers (A and B) with different LO path loss.

The followings are two interesting applications using this concept of a flat-gain region in a BJT-based Gilbert mixer. Section 3.2.1 introduces a 5.7 GHz I/Q downconversion mixer is demonstrated using 0.35-μm SiGe BiCMOS technology. A quarter-wavelength coupled line and two center-tapped transformers are utilized to generate differential quadrature LO signals. The wide flat-gain region of the BJT Gilbert mixer tolerates the LO amplitude imbalance due to the substrate loss of the quadrature coupler. On the other hand, an ultra-wideband (UWB) I/Q downconverter with an LR-CR quadrature generator is demonstrated using the same technology and is described in Section 3.2.2. The I/Q outputs of this generator are always in quadrature phase at any frequency while the BJT-type active mixer inherently

tolerates much LO power difference for a flat gain response. Consequently, the amplitude imbalance and phase error of the I/Q outputs are less than 1 dB and 2° when the RF frequency covering 3-11 GHz.

3.2.1 5.7-GHz I/Q Downconversion Mixers With an LO Quadrature Coupler

In the past, quadrature signals generated with reactive passive components were implemented on the GaAs semi-insulating substrate and high-resistive silicon substrate [32]. There is a need to integrate the quadrature coupler in the standard silicon process for the silicon RFIC era. Thus, the quadrature coupler has been demonstrated by using interconnect metals with ground shielding plane to avoid the substrate loss in the standard silicon process [33]. However, the low dielectric constant of the interconnect dielectrics results in a large size quadrature coupler. It is benign to take advantage of the high silicon dielectric constant. However, the high substrate loss in a standard silicon process leads to amplitude imbalance between the coupling port and through port in a quadrature coupler. It is difficult to employ a quadrature coupler with large amplitude imbalance. Recently, a Marchand balun consisting of two quadrature couplers has been demonstrated directly on lossy silicon substrate [31]. The demonstrated Marchand balun has balanced output signals even though each constituent quadrature coupler has unbalanced outputs.

Here, the use of a quadrature coupler directly on the lossy silicon substrate is employed in the LO ports of a Gilbert I/Q downconverter. The impact of quadrature generator amplitude imbalance is minimized by proper choice of the LO input power.

Applying the advantage of BJT mixer with a wide flat-gain region to the I/Q mixer design, we can achieve perfect current switching in both I/Q paths by properly choosing LO input power while a quadrature signal generator is employed in the LO stage with perfect phase relations at the desired frequency but unequal amplitude

caused by different LO path loss. Here, the quadrature generator is composed of a quarter-wavelength coupled line and two transformers as shown in Fig. 3-7.

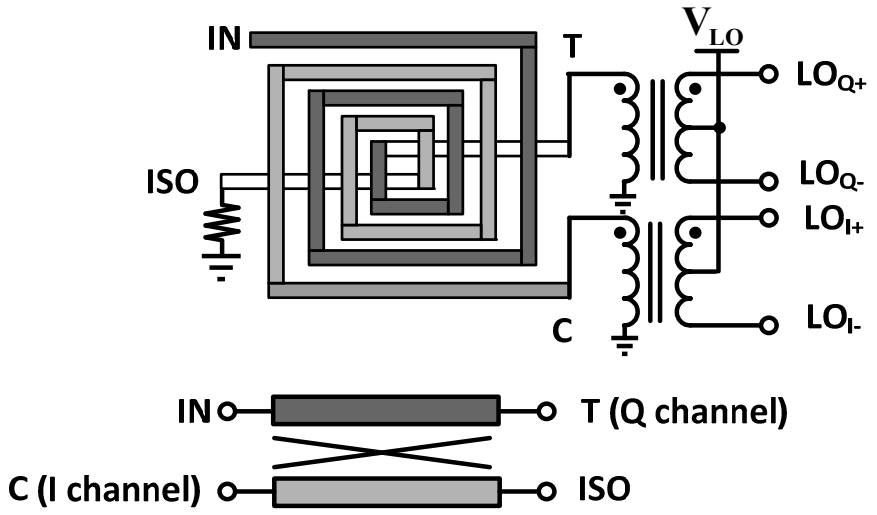


Fig. 3-7 LO quadrature signal generator using a quarter-wavelength coupled line and two center-tapped transformers.

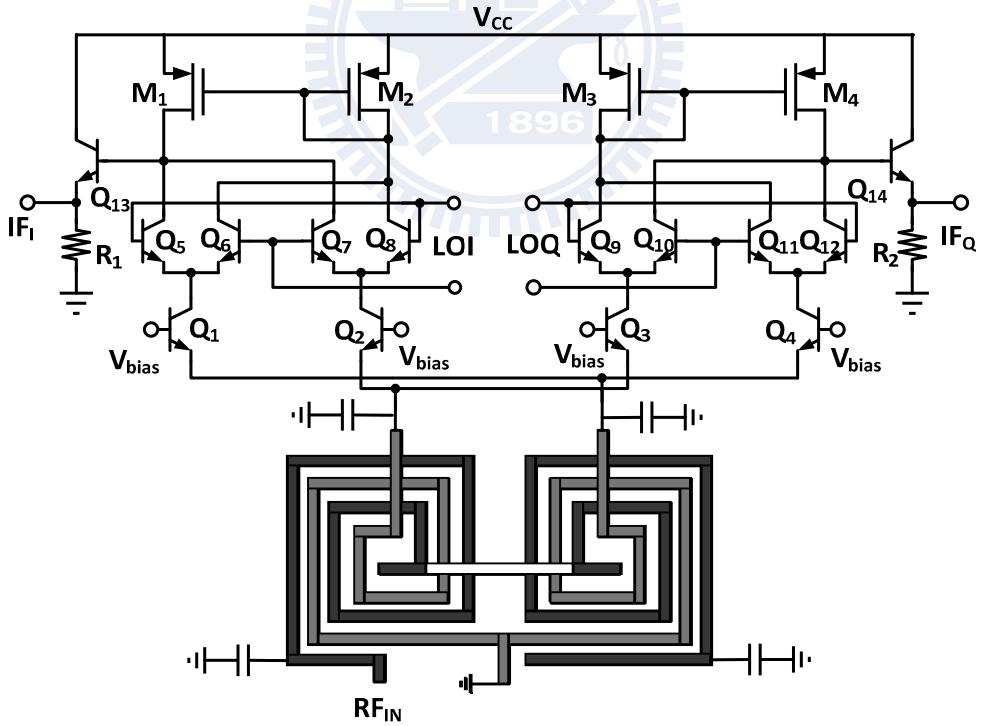


Fig. 3-8 Schematic of the SiGe BiCMOS I/Q downconverter with a reactive passive LO quadrature signal generator and an RF Marchand balun. The LO quadrature generator is shown in Fig. 3-7.

The LO signal is injected at the incident port of the quarter-wavelength coupled line. The LO ports of the I mixer are connected to the coupling port through the subsequent transformer while the through port is connected to the LO ports of the Q mixer through the other transformer. This type of quadrature generator has been implemented in the RF stage, but the intrinsic loss imbalance caused by the lossy silicon substrate in the differential quadrature generator makes IF I/Q outputs obviously unequal.

The schematic of the I/Q downconverter utilizing an LO differential quadrature signal generator and an RF Marchand balun is shown in Fig. 3-8. The Marchand balun is employed in the RF stage to convert an unbalanced signal into two balanced signals in spite of the lossy silicon substrate [31], [34]. A planar Marchand balun, consisting of two back-to-back quarter-wavelength coupled lines, has both coupling ports connected with short ends, the incident port in the opposite quarter-wavelength coupled line left open while the signal is incident in the input incident port and two balanced signals appear at the two isolated ports as shown in Fig. 3-8. The Marchand balun is followed by the common-base-configured transistors, Q_1-Q_4, for I/Q channels because of their excellent frequency response and convenience for broadband impedance matching. The short ends in the coupling ports of the Marchand balun are also utilized as the DC return ground of the common-base-configured transistors, Q_1-Q_4. Each quarter-wavelength coupled line in the Marchand balun is replaced by its shunt C- series L- shunt C lumped versions [35] as shown in Fig. 3-8 to further reduce the Marchand balun size at the cost of narrower bandwidth. The center frequency of each lumped quarter-wavelength coupled line used in the Marchand balun of the RF stage is designed around 5.7 GHz. This lumped-type quadrature coupler can also be employed in the LO port to further reduce the chip size at the cost of bandwidth.

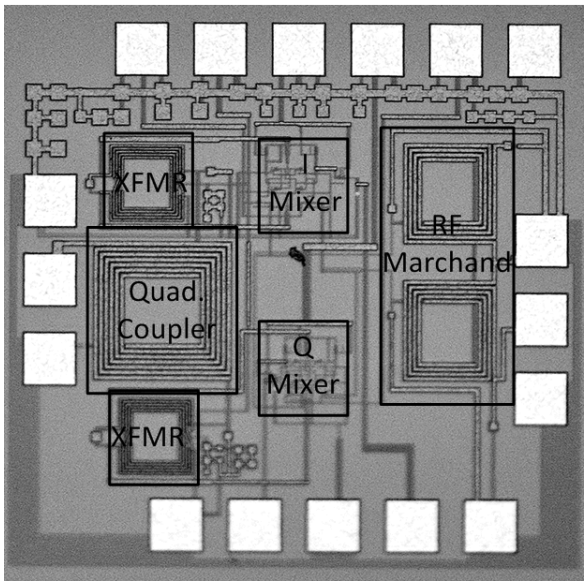


Fig. 3-9 Die photo.

The die photo of the proposed I/Q downconversion mixer is shown in Fig. 3-9. The die size is 1×1 mm^2 and is dominated by the passive elements consisting of a Marchand balun, a quarter-wavelength coupled line and two transformers. The emitter size of all the SiGe HBTs in common-base-configured transistors (Q_1-Q_4) and Gilbert mixer core (Q_5-Q_{12}) are 0.3 μm in width and 1.9 μm in length, respectively. A PMOS current combiner load is employed in each I/Q downconversion mixer to combine two differential signals into a single-ended output. A common-collector output buffer in each IF port is designed to facilitate the on-wafer measurement.

In order to shrink the size of the quarter-wavelength coupled line employed in the LO differential quadrature generator, the interleave transformer type quarter-wavelength coupled lines are employed as shown in Fig. 3-7. The LO quadrature coupler has a 7-μm line width, a 3-μm line spacing and an outer diameter of 266 μm to generate the quadrature phase in coupling and through ports at around 5.7 GHz. There are two 2:3 transformers following the quadrature coupler. Each transformer consists of two constituent inductors with line width, line spacing, and

outer diameter of 2.6 μm, 1.8 μm, and 140 μm, respectively. The dc bias voltage for the LO port is fed from the center-tapped point in the secondary coil of the transformer. On the other hand, the size of 3-stage 5-6 GHz PPF is about 180×180 μm^2 with 9.3 dB loss by calculating the RC values in [36].

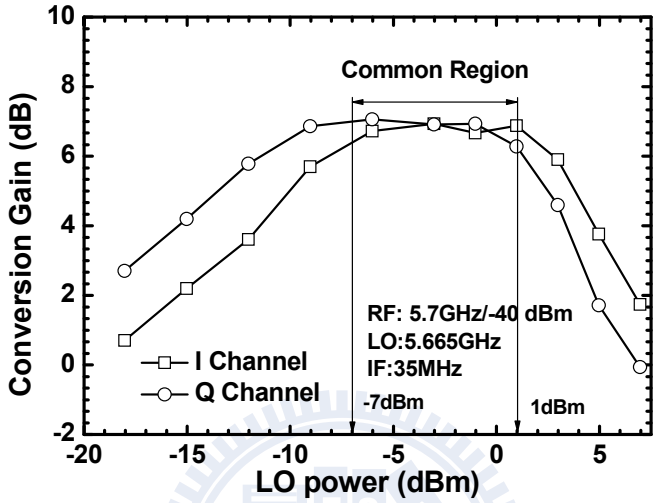


Fig. 3-10 I/Q-channel conversion gain versus LO power.

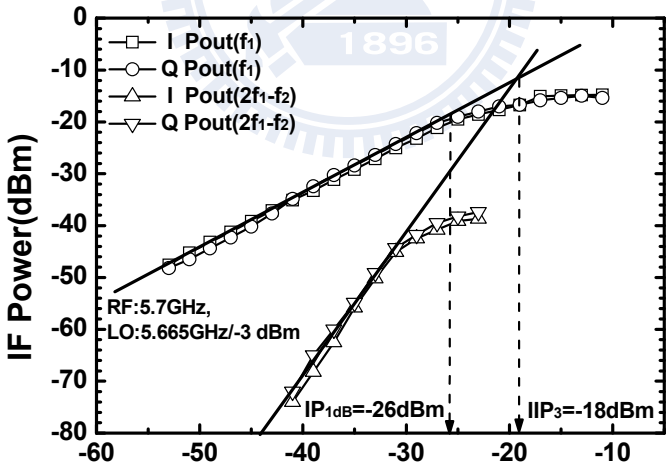


Fig. 3-11 Power performance.

The fabricated SiGe BiCMOS quadrature downconverter with the single-ended LO, RF and IF ports is convenient for on-wafer measurements. The supply voltage is 2.5 V and the total power consumption is 3.875 mW. The measured IF I/Q outputs have flat gain regions for LO power ranging from −10 dBm to 1 dBm, and −7 dBm to

3 dBm, respectively when RF=5.7 GHz, LO=5.665 GHz and IF=35 MHz. In other words, the coupling port has about 3 dB more loss than the through port has in the quadrature coupler. The conversion gain difference between I and Q channels varies within 1 dB for LO power from −7 dBm to 1 dBm as shown in Fig. 3-10.

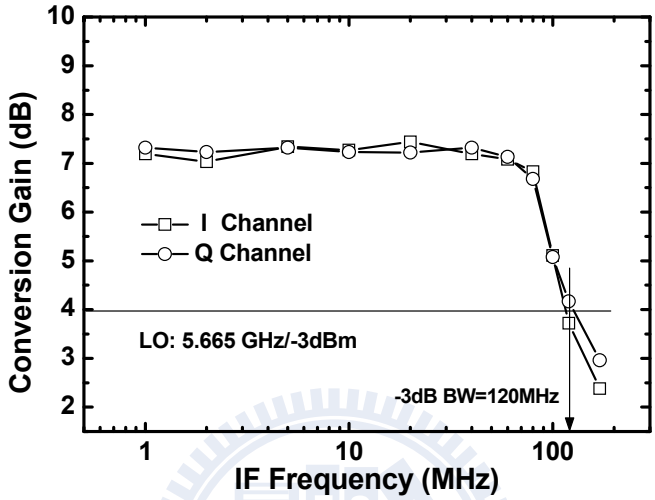


Fig. 3-12 IF bandwidth.

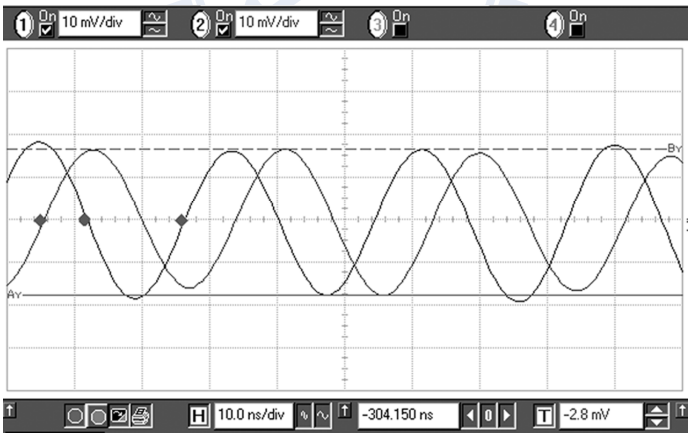


Fig. 3-13 I/Q output waveforms.

Fig. 3-11 shows the power performance of the downconverter for each I/Q channel. 7 dB conversion gain, −26 dBm IP_{1dB}, and −18 dBm IIP_3 are achieved for both I/Q outputs. The IF bandwidth of the SiGe BiCMOS I/Q downconverter is 120 MHz as shown in Fig. 3-12. The measured I/Q downconverter output waveforms are shown in Fig. 3-13. The average phase error is below 2° and amplitude error is below

0.3 dB. The RF input return loss is better than 10 dB from 4 GHz to 7 GHz. The measured double sideband noise figure is 20 dB. The I/Q channel performance of the demonstrated downconverter is well balanced in spite of the unbalanced LO path loss caused by the substrate loss. The overall performance is summarized in TABLE. 3.1.

TABLE. 3.1 PERFORMANCE SUMMARY OF THE 5.7-GHZ I/Q DOWNCONVERTER

RF Frequency (GHz)	5.7
Conversion Gain (dB)	7
I/Q Amplitude Imbalance (dB)	0.3
I/Q Phase Error (°)	<2
LO Power (dBm)	−4
DSB Noise Figure (dB)`	20
IP_{1dB} (dBm)	−26
IIP_3 (dBm)	−18
Supply Voltage (V)	2.5
Power Consumption (mW)	3.875
Technology	0.35-μm SiGe BiCMOS

On the other hand, the use of a quadrature generator in the RF path results in a 2 dB amplitude imbalance for I/Q channel output as shown in [37]-[38]. The insertion loss of 7 dB, magnitude imbalance of 4 dB and phase error of 2° from 5-6 GHz were measured for the quadrature coupler in [38].

3.2.2 UWB I/Q Downconversion Mixers With an LR-CR Quadrature Generator

The block diagram of the UWB *I*/*Q* downconverter is shown in Fig. 3-14. The ratio of V_Q (*CR*-path) and V_I (*LR*-path) can be described as Eqn. (3.14), as described in Section 3.1.3. Besides, the input impedance of the *LR*-*CR* quadrature generator is always equals to the load impedance (*R*) under the balanced condition by Eqn. (3.15).

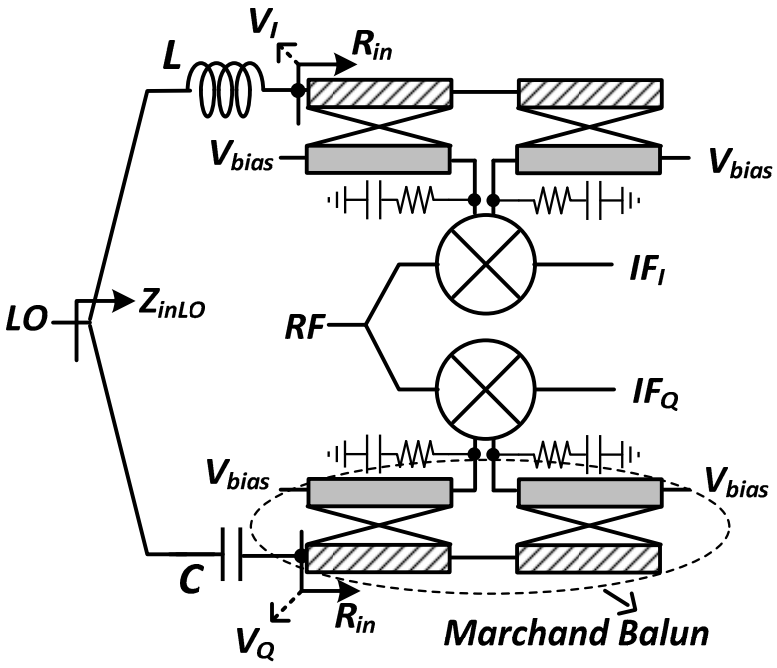


Fig. 3-14 Block diagram of the UWB I/Q downconverter and schematic of the micromixer employed in this downconverter.

Eqn. (3.14) indicates that the outputs are always 90° out of phase under the balanced condition ($L/C=R^2$) as long as the load impedance (R=50Ω) and the center frequency $[f_0 = 1/(2\pi\sqrt{LC})]$ are specified. However, the amplitude imbalance is proportional to the operating frequency with 6 dB/octave. For a UWB application, the center frequency (f_0) is designed at 5.5 GHz with L=1.447 nH and C=0.58 pF. As a result, the I/Q signals have the maximum amplitude imbalance of 6 dB within the 4:1 bandwidth, i.e., from $f_0/2$ (2.75 GHz) to $2f_0$ (11 GHz).

Such amplitude imbalance seems impossible for wideband applications at first sight; however, a BJT-type active mixer only needs a small LO voltage swing for a full current commutation and there is an *LO* input power range of around 10 dB for a flat gain response [31].

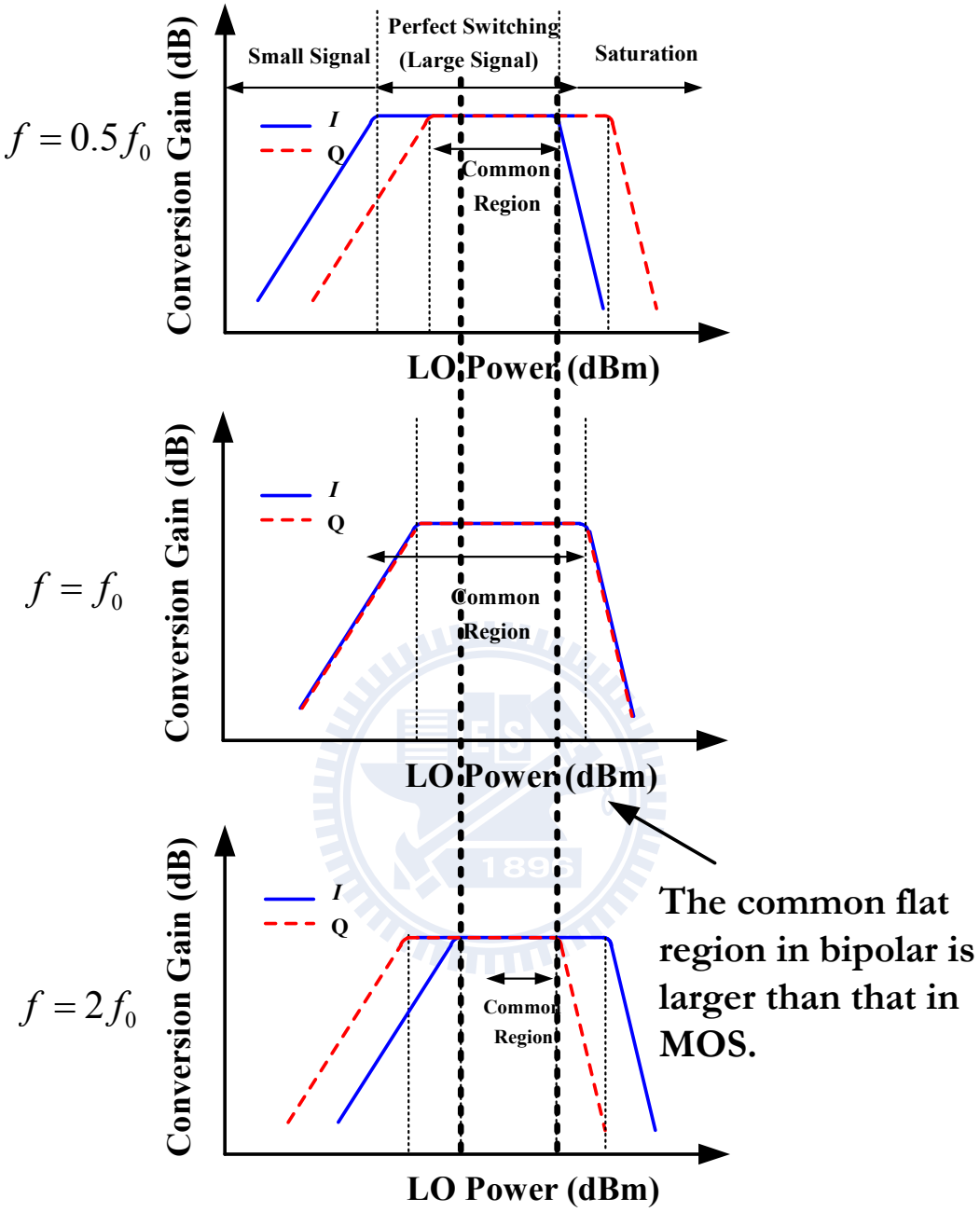


Fig. 3-15 Conversion gain as a function of LO power while an LO LR-CR quadrature generator is used.

When the operating frequency is lower than f_0, the LO voltage swing of at Q channel (V_Q) is smaller than the LO voltage swing at I channel (V_I) by Eqn. (3.14). Thus, the Q-mixer needs larger LO input power to reach the flat gain region than the I-mixer as shown in Fig. 3-15. When the operating frequency is at f_0, the conversion gain curve of both channels are overlapped because V_I=V_Q. On the contrary, the

Q-mixer needs less LO input power than the I-mixer when the LO frequency is higher than f_0. Consequently, the suitable LO power can be selected so that the IF I/Q output amplitude imbalance can be minimized with an excellent quadrature accuracy.

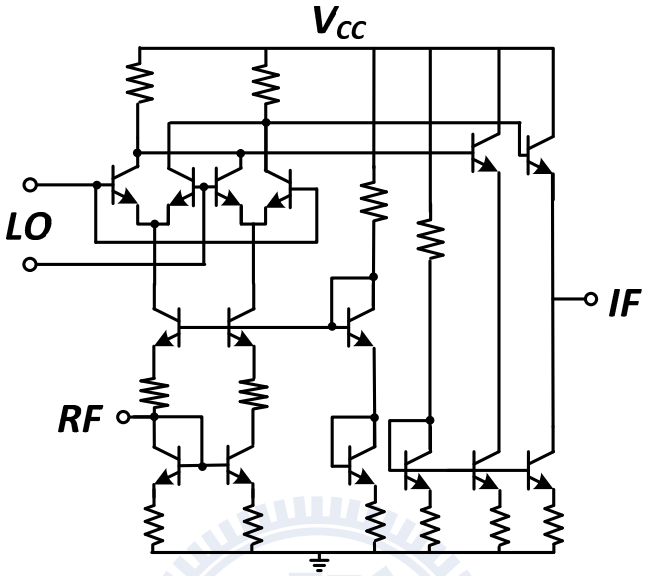


Fig. 3-16 Schematic of the micromixer employed in this downconverter.

The micromixer topology [6] is chosen in this work because it achieves an RF wideband matching and provides balanced RF currents by the input transconductance balun stage as shown in Fig. 3-16. A broadband Marchand balun [34] consisting of two coupled-line couplers is employed to generate differential signals at the *LO* port of each *I/Q* mixer. The dc bias (V_{bias}) of the mixer core is fed from the ac-ground node of the Marchand balun as shown in Fig. 3-14. A 50-Ω resistor in series with a dc-blocking capacitor is utilized at each output node to achieve a wideband 50-Ω input impedance of each balun. It is worth mentioning that an active balun can also be applied with a compact die size [39] but the linearity of an active balun should be designed carefully since the limited voltage swing degrades the operating bandwidth.

The die photo of the UWB I/Q downconverter is shown in Fig. 3-17 and the die size is 1.05×0.95 mm^2. The supply voltage is 3.3 V with the current consumption of 4.7 mA for each mixer.

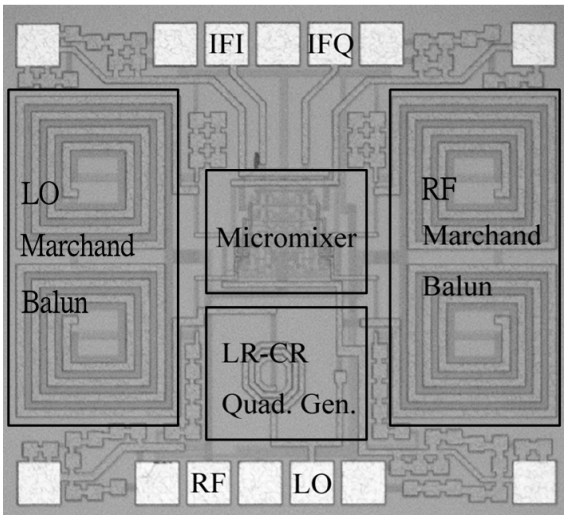
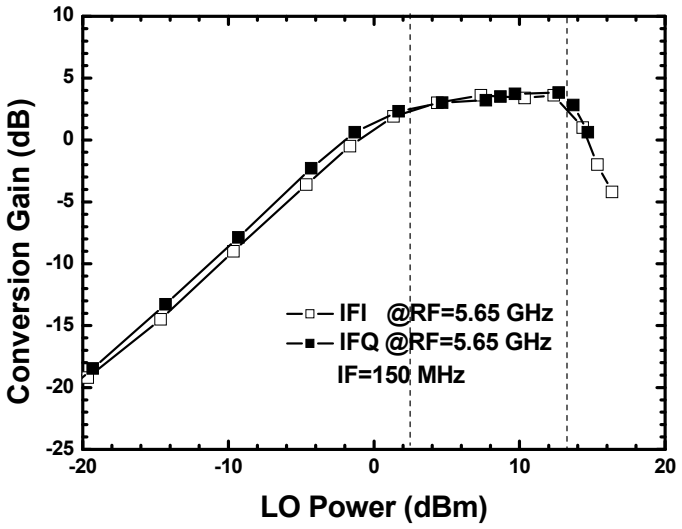


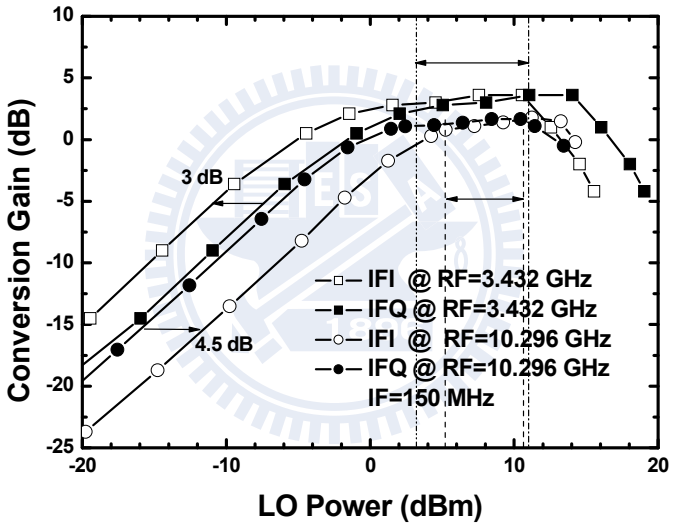
Fig. 3-17 Die photo.

Fig. 3-18(a) shows the conversion gain of the I/Q downconverter with respect to the LO power when f=5.5 GHz=f_0 and Fig. 3-18(b) shows the results when f=3.282 GHz<f_0 and f=10.146 GHz>f_0. The I/Q mixers need the same LO power for a full current commutation when the LO frequency is at the center frequency. On the other hand, the I-mixer needs less (more) LO input power to reach the flat gain region than the Q-mixer when the LO frequency is lower (higher) than the center frequency due to the amplitude imbalance of the LR-CR topology as described in Eqn. (3.14). However, the I/Q mixers still have a wide common region of the LO power for balanced quadrature outputs. Thus, an 8 dBm LO power is chosen for all the following measurements.

As shown in Fig. 3-19, the RF 3-dB bandwidth ranges from 2 GHz to 11 GHz while the IP_{1dB} and IIP_3 are better than −9 dBm and 6 dBm, respectively. Fig. 3-20 shows the amplitude imbalance <1 dB and the quadrature phase error <2° with respect to the input RF frequency when IF frequency is 150 MHz. The input return loss for RF and LO ports are better than 10 dB when frequency ranging from dc to 20 GHz and from 1.6 GHz to 13 GHz, respectively, as shown in Fig. 3-21.



(a)



(b)

Fig. 3-18 (a)Conversion gain with respect to the LO power when LO frequency is 5.5 GHz (b)LO frequency is 3.282 and 10.146 GHz, respectively.

The LO matching is achieved due to the 50-Ω impedance of the LR-CR topology as described in Eqn. (3.15) while the micromixer topology facilitates the RF impedance matching. Fig. 3-22 shows the IF 1-dB bandwidth of 500 MHz with the noise figure below 16.5 dB as IF frequency ranging from 200 kHz to 100 MHz thanks to the inherently low flicker noise corner of the SiGe HBT devices.

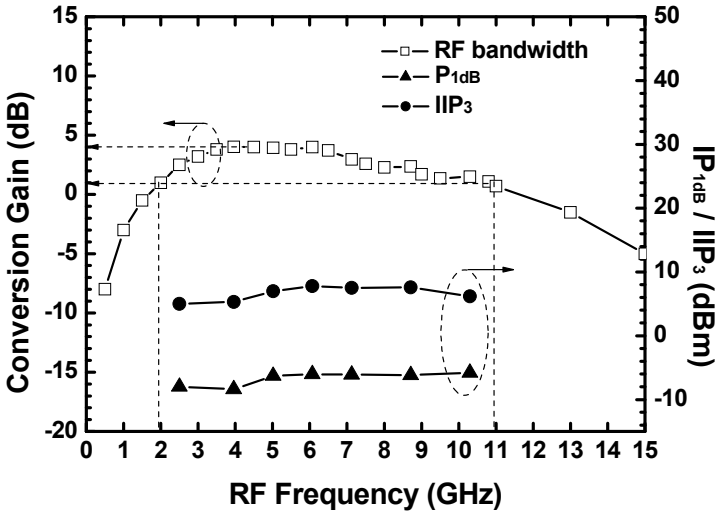


Fig. 3-19 Conversion gain and power performance (including IP_{1dB} and IIP_3).

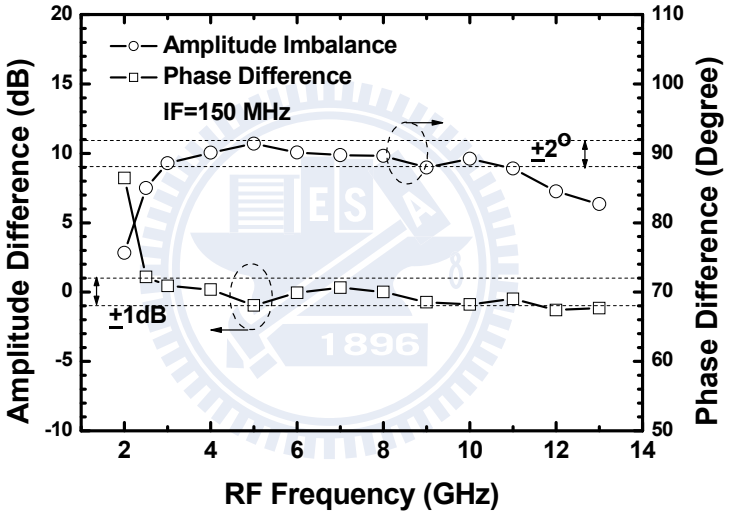


Fig. 3-20 Amplitude imbalance and phase difference of I/Q outputs.

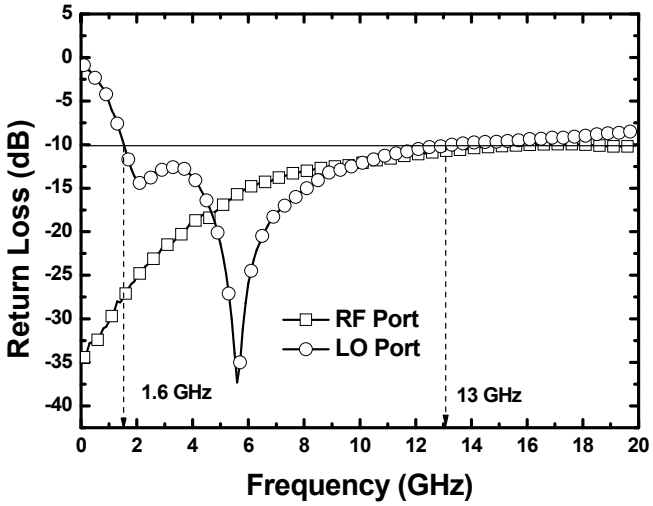


Fig. 3-21 LO and RF input return loss.

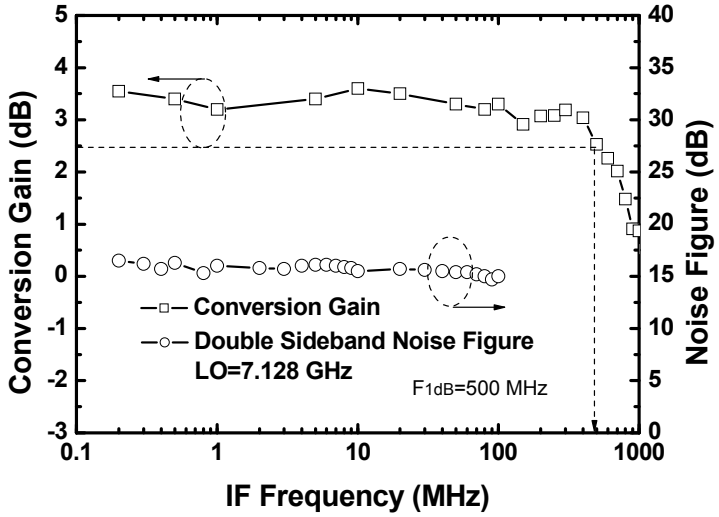


Fig. 3-22 Conversion gain and double-sideband noise figure.

The overall performance is summarized in TABLE. 3.2.

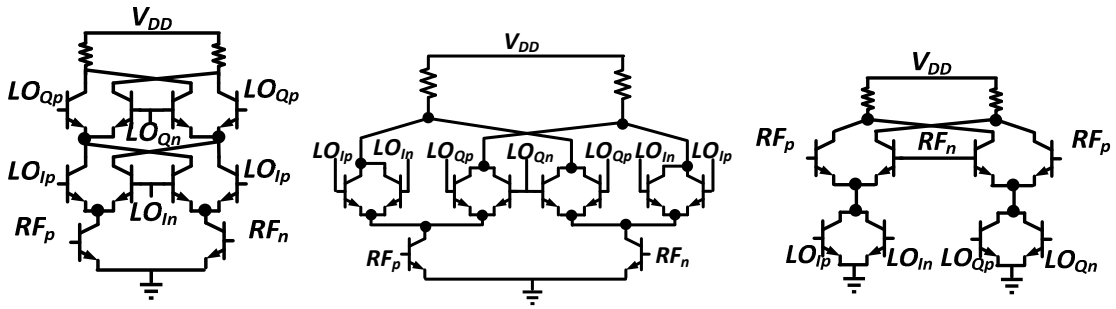
TABLE. 3.2 PERFORMANCE SUMMARY OF THE UWB DOWNCONVERTER USING LR-CR QUADRATURE GENERATOR

RF Frequency (GHz)	2-11
IF 1-dB Bandwidth (MHz)	500
Conversion Gain (dB)	7
I/Q Amplitude Imbalance (dB)	0.3
I/Q Phase Error (°)	<2
LO Power (dBm)	−4
DSB Noise Figure (dB)`	20
IP_{1dB} (dBm)	−9
IIP_3 (dBm)	6
Supply Voltage (V)	3.3
RF Return Loss (dB)	<-10 (~20 GHz)
LO Return Loss (dB)	<-10 (1.6-13 GHz)
Power Consumption (mW)	31
Technology	0.35-μm SiGe BiCMOS

Chapter 4 High-Isolation Compensated Sub-Harmonic Mixer

4.1 INTRODUCTION

Sub-harmonic mixers (SHMs), including stacked-LO [in Fig. 4-1(a)] and leveled-LO (top-LO [in Fig. 4-1(b)] or bottom-LO [in Fig. 4-1(c)]) topologies [40], [41]-[42], are commonly employed in a direct-conversion receiver (DCR) for their high LO rejection [41] and lessened self-mixing/dc-offset problems. The bottom-LO SHM has the simplest structure with the fewest numbers of transistors. Because the second-order harmonic of the parallel differential pair is used to provide the 2LO mixing signal, the operation is not similar to the current switching function of the other two topologies. The conversion gain is the most bias sensitive and typically constrained by the bias condition, not the ideal current switching maximum gain. Besides, as the LO input signal increases, the dc current also increases. As a result, the conversion gain of the bottom-LO SHM is the worst in the three topologies and the bottom-LO SHM is rarely implemented in real applications.



(a) (b) (c)

Fig. 4-1 Schematic of a (a) stacked-LO (b) top-LO (c) bottom-LO SHM.

Thus, this chapter introduces the current switching operation of a BJT-based differential pair [3] and then extends to conventional Gilbert mixers, including a

fundamental Gilbert mixer, the stacked-LO SHM and the top-LO SHM. After a fully comparison, a stacked-LO SHM with delay compensation technique will be introduced in next section.

(I) Differential Pair

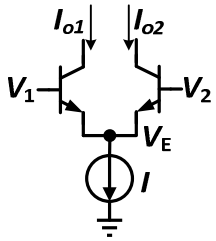


Fig. 4-2 Schematic of a BJT differential amplifier.

A differential pair with a constant current source I (or input current) is shown in Fig. 4-2. $V_1 = V_{CM} + \frac{1}{2}V_D$ and $V_2 = V_{CM} - \frac{1}{2}V_D$ are applied to the differential inputs where $V_D = V\cos\omega t$. The output current can be expressed as

$$\begin{cases} I_{o1} = I_S e^{(V_1 - V_E)/V_T} = I_S e^{(V_{CM} + V_D/2 - V_E)/V_T} = I_S e^{(V_{CM} - V_E)/V_T} \cdot e^{A} \\ I_{o2} = I_S e^{(V_2 - V_E)/V_T} = I_S e^{(V_{CM} - V_D/2 - V_E)/V_T} = I_S e^{(V_{CM} - V_E)/V_T} \cdot e^{-A} \end{cases}, \tag{4.1}$$

where $A = V_D/(2V_T)$.

Therefore, the total current is

$$I = I_{o1} + I_{o2} = I_S e^{(V_{CM} - V_E)/V_T}(e^{A} + e^{-A}) = 2I_S e^{(V_{CM} - V_E)/V_T}\cosh(A). \tag{4.2}$$

The individual current is $I_{o1} = I\,e^{A}/(e^{A} + e^{-A})$ and $I_{o2} = I\,e^{-A}/(e^{A} + e^{-A})$. The differential output can be expressed as

$$\Delta I = I_{o1} - I_{o2} = I\tanh(A). \tag{4.3}$$

The function tanh(A) can be approximately as

$$\tanh(A) = \begin{cases} A, \text{ when } |A| << 1 \\ \text{sgn}(A), \text{when } |A| >> 1 \end{cases}. \tag{4.4}$$

That is, when a small signal is applied, the small-signal transconductance gain

$$G_m = \frac{\delta \Delta I}{\delta V_D} \approx \frac{I \times A}{V_D} = \frac{I \cdot V_D / (2V_T)}{V_D} = \frac{I}{2V_T}, \quad (4.5)$$

which is the same as the g_m of the single transistor in the differential pair. On the other hand, when a large signal is applied, a square-like switching function is obtained. Thus, the differential pair acts as a single-balanced switching core and the gain tends to a constant.

If I is a constant current source, the circuit is a simple differential amplifier. However, if the I consists of an input RF small-signals ($I=I_{DC}\pm I_{RF}/2$), the frequency downconversion is achieved and vice versa.

Further, according to Eqn. (4.2), $V_E = V_{CM} - V_T \ln(I/2I_S) + V_T \ln[\cosh(A)]$, where the term $V_T \ln[\cosh(A)]$ has a significant second-order harmonic of the switching function.

(II) Double-Balanced Switching Core

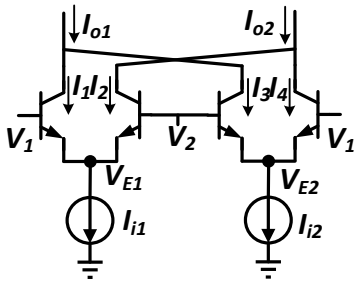


Fig. 4-3 Schematic of a double-balanced Gilbert switching core.

Since a single-balanced mixer is a simple differential amplifier, the LO signal applied at the switching core is amplified and then appears at the output. To avoid this tragedy, a well-known double-balanced switching core shown in Fig. 4-3, is widely used. The current relations are listed below.

$$\begin{cases} I_{i1} = I_1 + I_2, I_{i2} = I_3 + I_4 \\ I_{o1} = I_1 + I_3, I_{o2} = I_2 + I_4 \end{cases} \tag{4.6}$$

where

$$\begin{cases} I_1 = I_S e^{(V_1 - V_{E1})/V_T} = I_S e^{(V_{CM} - V_{E1})/V_T + A} \\ I_2 = I_S e^{(V_{CM} - V_{E1})/V_T - A} \\ I_3 = I_S e^{(V_{CM} - V_{E2})/V_T - A} \\ I_4 = I_S e^{(V_{CM} - V_{E2})/V_T + A} \end{cases}.$$

Thus, the switching function $s(t)$ is defined as the differential-in-differential-out current gain and can be derived as follows.

$$\begin{aligned} s(t) &= \frac{I_{o1} - I_{o2}}{I_{i1} - I_{i2}} = \frac{I_1 + I_3 - (I_2 + I_4)}{I_1 + I_2 - (I_3 + I_4)} \\ &= \frac{e^{(V_{CM} - V_{E1})/V_T + A} + e^{(V_{CM} - V_{E2})/V_T - A} - e^{(V_{CM} - V_{E1})/V_T - A} - e^{(V_{CM} - V_{E2})/V_T + A}}{e^{(V_{CM} - V_{E1})/V_T + A} + e^{(V_{CM} - V_{E1})/V_T + A} - e^{(V_{CM} - V_{E2})/V_T - A} - e^{(V_{CM} - V_{E2})/V_T + A}} \\ &= \frac{\left[e^{(V_{CM} - V_{E1})/V_T} - e^{(V_{CM} - V_{E2})/V_T} \right](e^A - e^{-A})}{\left[e^{(V_{CM} - V_{E1})/V_T} - e^{(V_{CM} - V_{E2})/V_T} \right](e^A + e^{-A})} \\ &= \frac{e^A - e^{-A}}{e^A + e^{-A}} = \tanh(A) \\ &= \tanh\left[V \cos \omega t / (2V_T) \right] \end{aligned} \tag{4.7}$$

As a result, the current switching function of the mixing core, defined as the ratio of the output differential current (I_{o1}-I_{o2}) and the input differential current (I_{i1}-I_{i2}), is tanh(A), which is the same as a single-balanced mixer.

Further, the emitter voltage of the two inputs nodes can be expressed as

$$\begin{cases} V_{E1} = V_{CM} - V_T \ln(I_{DC}/2I_S) + V_T \ln\left[\cosh(V \cos \omega t / 2V_T)\right] - V_T \ln(I_{id}/4I_S) \\ V_{E2} = V_{CM} - V_T \ln(I_{DC}/2I_S) + V_T \ln\left[\cosh(V \cos \omega t / 2V_T)\right] + V_T \ln(I_{id}/4I_S) \end{cases} \tag{4.8}$$

because $I_{i1} = I_{DC} + I_{id}/2$ and $I_{i2} = I_{DC} - I_{id}/2$, where I_{id}=$g_m V_{id}$ and g_m is the transconductance of the input transistor (*i.e.*, current source).

Thus, $V_{E1} \approx V_{E2}$ because, typically, the input signals is much smaller than the switching signal (*i.e.*, LO). The common 2LO signals still appear at the input signals and can be cancelled by the differential-to-single combiner, *e.g.*, a transformer.

(III) Stacked-LO Sub-Harmonic Mixing Core

Fig. 4-4 shows the schematic of a stacked-LO sub-harmonic switching core consisting of two double-balanced switching cores in cascode while the LO signals applied at top and bottom cells are in quadrature with $V_{1,2} = V_{CM1} \pm \frac{1}{2} V \cos \omega t$, and $V_{3,4} = V_{CM2} \pm \frac{1}{2} V \sin \omega t$.

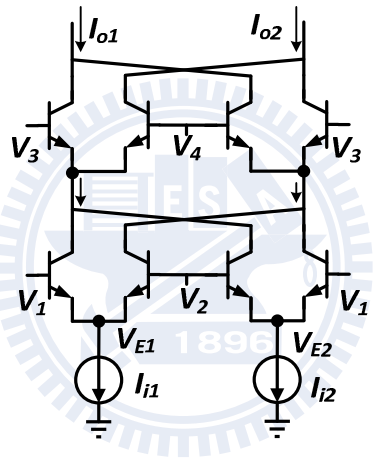


Fig. 4-4 Schematics of a stacked-LO sub-harmonic switching core.

Therefore, the switching function can be directly extended from a double-balanced Gilbert cell, *i.e.*,

$$s(t) = \tanh(A) \cdot \tanh(B) \tag{4.9}$$

where $A = \frac{V}{2V_T} \cos \omega t$ and $B = \frac{V}{2V_T} \sin \omega t$.

Besides, the input emitter node voltages are still the same as Eqn. (4.8) because only the bottom level affects the node voltage.

However, when considering both the input LO quadrature signal phase error (θ) and the finite phase delay (ϕ) of the switching function between top and bottom

levels. That is, if the in-phase signal applied at the bottom level is $V\cos\omega t$ but the quadrature-phase signal is $V\sin(\omega t+\theta)$. Further, in practice, the input current passes through the bottom stage and then enters to the top level after a certain time delay τ or phase delay $\phi = \omega\tau$. That is,

$$\begin{aligned} s(t) &= \left[\tanh(\frac{V}{2V_T}\cos\omega t) \otimes \delta(t-\tau) \right] \times \tanh[\frac{V}{2V_T}\sin(\omega t+\theta)] \\ &= \tanh[\frac{V}{2V_T}\cos\omega(t-\tau)] \times \tanh[\frac{V}{2V_T}\sin(\omega t+\theta)] \\ &= \tanh[\frac{V}{2V_T}\cos(\omega t-\phi)] \times \tanh[\frac{V}{2V_T}\sin(\omega t+\theta)] \end{aligned} \quad . \quad (4.10)$$

Thus, a significant dc term appears and results in the RF-to-IF direct leakage although the conversion gain degrades insignificantly. The dc term can be obtained by

$$s_{DC} = \int_{t=0}^{T=1/\omega} s(t)dt \, . \quad (4.11)$$

It is noteworthy that this phenomenon occurs even though perfectly quadrature signals are applied because the phase delay is unavoidable, which is inverse proportional to the transistor cut-off frequency (f_T) [40]-[43].

(IV) Top-LO Sub-Harmonic Mixer

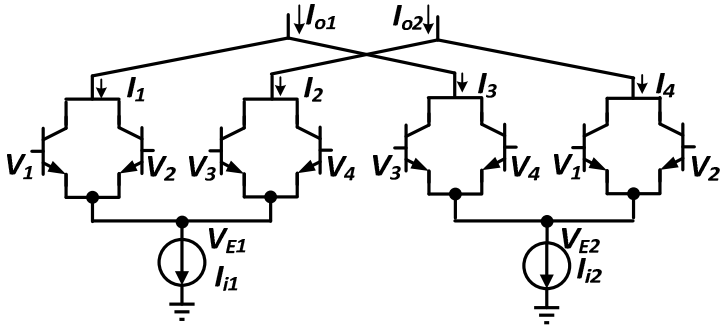


Fig. 4-5 Schematics of a top-LO sub-harmonic switching core.

The schematic of a top-LO SHM core is shown in Fig. 4-5. Unlike the cascode switching function of the stacked-LO SHM, the 2LO frequency is generated by using two transistors in parallel while the differential signals are applied. Thus, the current

relations of the top-LO SHM are listed as below.

$$\begin{cases} I_{i1} = I_1 + I_2, I_{i2} = I_3 + I_4 \\ I_{o1} = I_1 + I_3, I_{o2} = I_2 + I_4 \end{cases} \tag{4.12}$$

where

$$\begin{cases} I_1 = I_S e^{(V_1 - V_{E1})/V_T} + I_S e^{(V_2 - V_{E1})/V_T} = I_S e^{(V_{CM} - V_{E1})/V_T + A} + I_S e^{(V_{CM} - V_{E1})/V_T - A} \\ \quad = I_S e^{(V_{CM} - V_{E1})/V_T} \cdot (e^A + e^{-A}) \\ I_2 = I_S e^{(V_{CM} - V_{E1})/V_T} \cdot (e^B + e^{-B}) \\ I_3 = I_S e^{(V_{CM} - V_{E2})/V_T} \cdot (e^B + e^{-B}) \\ I_4 = I_S e^{(V_{CM} - V_{E2})/V_T} \cdot (e^A + e^{-A}) \end{cases} . \tag{4.13}$$

Thus,

$$\begin{aligned} s(t) &= \frac{I_{o1} - I_{o2}}{I_{i1} - I_{i2}} = \frac{I_1 + I_3 - I_2 - I_4}{I_1 + I_2 - I_3 - I_4} \\ &= \frac{\cosh(A) - \cosh(B)}{\cosh(A) + \cosh(B)} = \frac{2\sinh(\frac{A+B}{2})\sinh(\frac{A-B}{2})}{2\cosh(\frac{A+B}{2})\cosh(\frac{A-B}{2})} . \\ &= \tanh(\frac{A+B}{2}) \cdot \tanh(\frac{A-B}{2}) \end{aligned} \tag{4.14}$$

When compared to the switching function of a stacked-LO SHM, an additional 3-dB LO power is required for a top-LO SHM to reach the same gain level, because

$$\begin{cases} (A+B)/2 = (1/\sqrt{2}) \cdot V \cos(\omega t - \pi/4) \\ (A-B)/2 = (1/\sqrt{2}) \cdot V \sin(\omega t - \pi/4) \end{cases}, \tag{4.15}$$

and the common phase delay π/4 has no influence on the conversion gain.

The simulation results of the current switching gain of stacked-LO [Fig. 4-4] and top-LO [Fig. 4-5] topologies are drawn in Fig. 4-6 and compared to a fundamental mixer [Fig. 4-3].

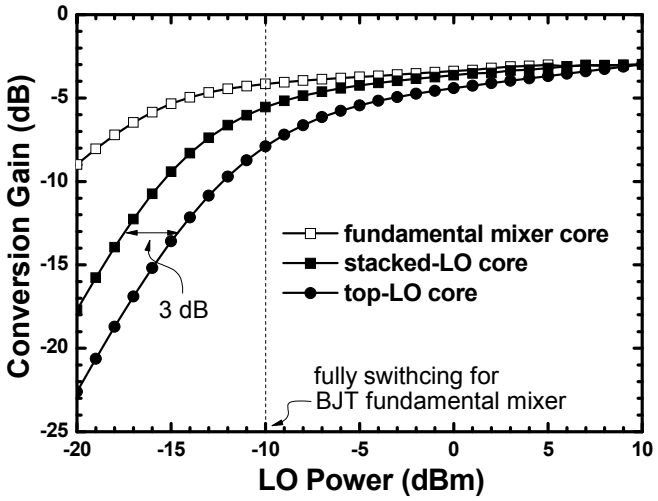


Fig. 4-6 Simulated current conversion gain of the switching core for a fundamental mixer, a stacked-LO mixer and a top-LO mixer core.

As mentioned in (III), twice the switching frequency (2LO) signals appear at the input node(s) inherently. For an SHM, the 2LO leakage to input will be mixed by the switching function again and thus, a dc offset due to self-mixing occurs. However, in the top-LO topology, the emitter nodes of the four transistors with applied base differential-quadrature signals are connected together, i.e., V_{E1} or V_{E2} in Fig. 4-5. Thus,

$$\begin{cases} I_{i1} = I_1 + I_2 = I_S e^{(V_{CM}-V_{E1})/V_T} \cdot (e^{A} + e^{-A}) + I_S e^{(V_{CM}-V_{E1})/V_T} \cdot (e^{B} + e^{-B}) \\ \quad = 2I_S e^{(V_{CM}-V_{E1})/V_T} \cdot \left[\cosh(A) + \cosh(B)\right] \\ I_{i2} = I_3 + I_4 \\ \quad = 2I_S e^{(V_{CM}-V_{E2})/V_T} \cdot \left[\cosh(A) + \cosh(B)\right] \end{cases} . \quad (4.16)$$

As a result,

$$\begin{cases} V_{E1} = V_{CM} - V_T \ln(\frac{I_{DC}}{2I_S}) + V_T \cdot \ln\left[\cosh(A) + \cosh(B)\right] - V_T \ln(\frac{I_D}{4I_S}) \\ V_{E2} = V_{CM} - V_T \ln(\frac{I_{DC}}{2I_S}) + V_T \cdot \ln\left[\cosh(A) + \cosh(B)\right] + V_T \ln(\frac{I_D}{4I_S}) \end{cases} . \quad (4.17)$$

because $I_{i1,2} = I_{DC} \pm \frac{1}{2} I_{id}$.

Similar to previous situation, the input signal is much smaller than the switching LO signals. Thus, $V_{E1} \approx V_{E2} \approx V_{CM} - V_T \ln(\frac{I_{DC}}{2I_S}) + V_T \cdot \ln\left[\cosh(A) + \cosh(B)\right]$. Thus, the 2LO frequency is totally cancelled if the differential-quadrature signals are perfect.

Despite of the gain performance and the biasing requirement, the isolation property should also be considered. In practice, the LO/2LO/RF leakage to the IF output can be filtered out by cascading a low-pass channel filter; however, the LO/2LO leakage to the RF port may mix with itself to generate an output dc offset. Moreover, the leakage may even couple to the antenna and radiate. The received LO signal after radiation and random reflection may then self-mix to generate a time-varying dc offset which cannot be calibrated out using dc-offset cancellation techniques [44]. The top-LO SHM has better 2LO-to-RF isolation than the others because the four transistors with quadrature phases are in parallel at the emitter node and the 2LO frequency component is inherently cancelled, as shown in Fig. 4-1(c) [45].

A top-LO SHM requires larger LO power than a leveled-LO SHM does. It is important to minimize the LO power requirement because a high LO power requirement results in significant dc power consumption for LO output buffers, especially at high frequencies. On the other hand, a stacked-LO requires a higher dc supply voltage because of the additional cascode Gilbert switching cell although a lower LO power is required. Further, a current phase delay occurs between the top and bottom mixing cells of a stacked-LO SHM due to the finite time delay of the transistors. As a result, the isolation and dc offset performance are degraded even if the LO signals are perfectly differential-quadrature as mentioned in Eqns. (4.10) and (4.11).

4.2 COMPENSATED STACKED-LO SUB-HARMONIC MIXER

As shown in Fig. 4-7(a), the stacked-LO core (Q_1-Q_8) consists of two pairs of Gilbert mixing cells in cascode version with quadrature LO input, say, LOI at the top cell and LOQ at the bottom one. On the other hand, the compensation circuit (Q_{1a}-Q_{8a}) is a replica of the stacked-LO core but LOQ/LOI are fed at the top/bottom cells, respectively, as shown in Fig. 4-7(b).

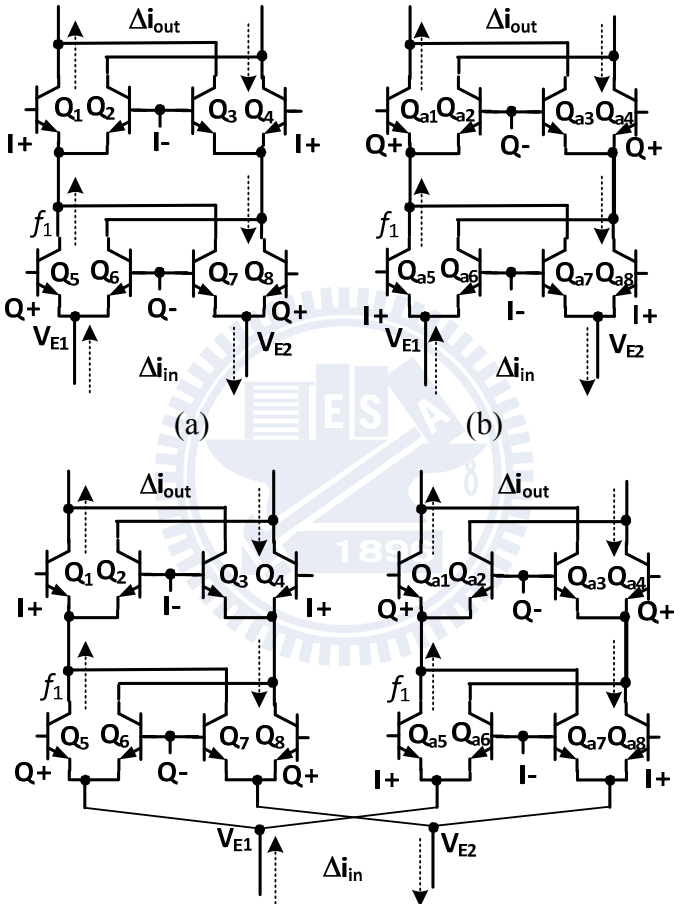


Fig. 4-7 (a) Schematic of the stacked-LO core with LOI at the top cell and LOQ at the bottom cell (b) schematic of the stacked-LO core with LOQ/LOI at top/bottom cells (c) schematic of two stacked-LO cores in parallel.

The switching mechanism of the stacked-LO core is illustrated in Fig. 4-8. $F_1(t)/F_2(t)$ represent the switching function with 0°(I)/90°(Q) LO input phase difference. Further, $F_1'(t)$ and $F_2'(t)$ represent the switching function after a certain

phase delay (ϕ). Therefore, the switching function of the stacked-LO core shown in Fig. 4-7(a) can be represented as $s_1(t) = F_2 \oplus F_1'$.

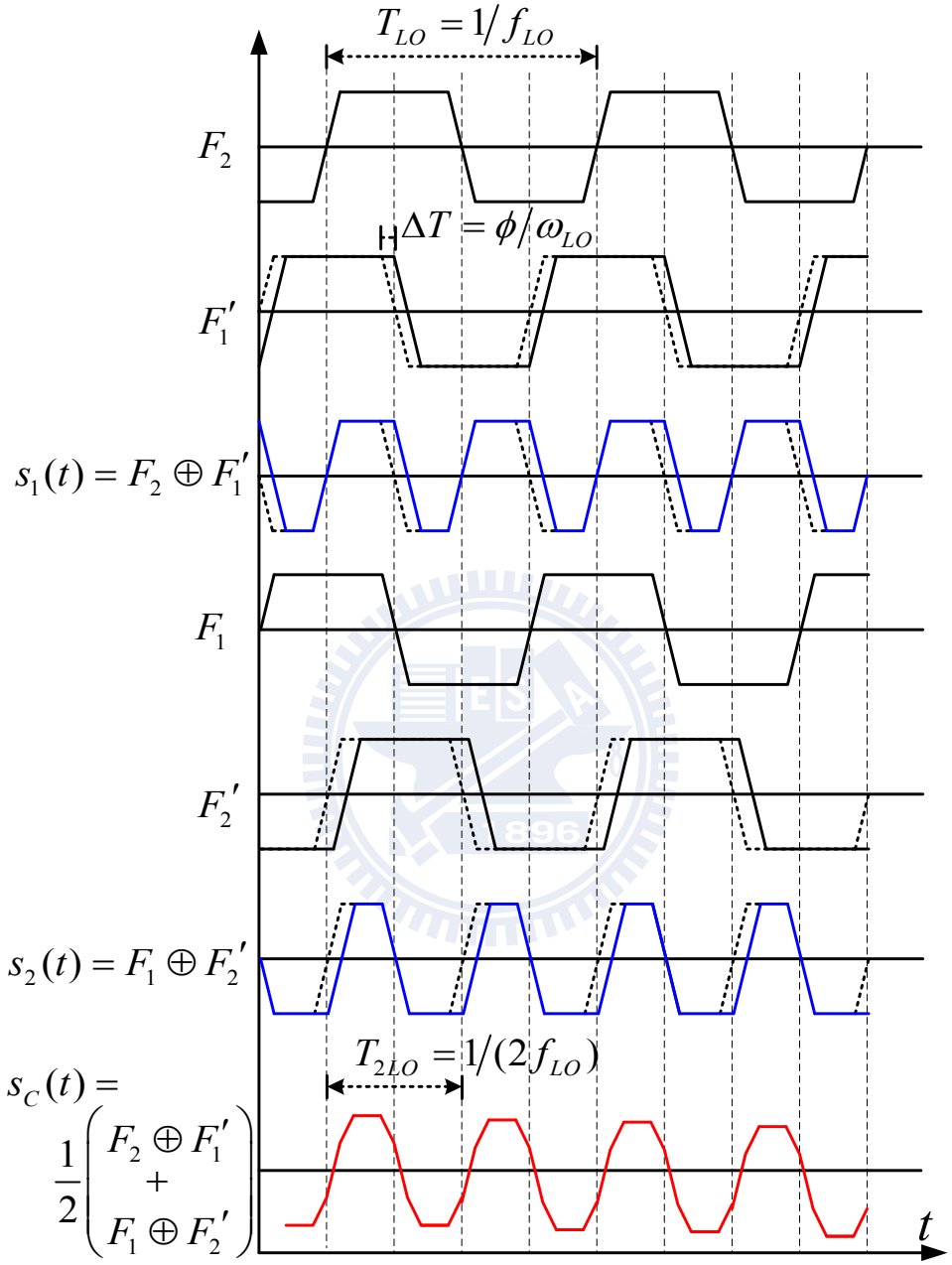


Fig. 4-8 Timing diagram of the switching function. Dotted lines represent the switching function without a phase delay, i.e., $F_1(t)$ or $F_2(t)$.

On the other hand, $s_2(t) = F_1 \oplus F_2'$ represents the switching function of the circuit shown in Fig. 4-7(b). The switching function s_1 or s_2 does not have a 50% duty cycle. If two stacked-LO cells with the same transistor sizes are in parallel as shown

in Fig. 4-7(c), the equivalent switching function becomes

$$s_C(t) = \frac{1}{2}\left[s_1(t) + s_2(t)\right] = \frac{1}{2}\left[F_2 \oplus F_1' + F_1 \oplus F_2'\right]. \quad (4.18)$$

As shown in Fig. 4-8, a 50 % duty cycle is restored again for the compensated switching function (s_C). Thus, the uncompensated switching function s_1(or s_2) has an equivalent dc term which results in an RF-to-IF leakage path while the compensated switching function (s_C) does not.

More strictly, if the switching devices are BJT (either HBT or vertical-NPN in CMOS process), the sub-harmonic switching function *s*(t), defined as the ratio of the output IF current and input RF current, can be formulated as

$$s(t) \equiv \Delta I_{IFout(w/o)} / \Delta I_{RFin} = \tanh(X\cos\omega t) \times \tanh\left[X\sin(\omega t + \phi)\right] \quad (4.19)$$

and

$$\begin{aligned} s_C(t) &\equiv \Delta I_{IFout(w/\ )} / \Delta I_{RFin} \\ &= \frac{1}{2}\left[\begin{array}{l} \tanh(X\cos\omega t) \times \tanh[X\sin(\omega t + \phi)] \\ \quad + \tanh(X\sin\omega t) \times \tanh[X\cos(\omega t + \phi)] \end{array}\right] \end{aligned} \quad (4.20)$$

for the SHMs w/ and w/o compensation, respectively, where $X = V_{LO}/2V_T$ and ϕ represents the phase delay between the top and bottom cells, respectively. That is, the differential RF input current passes through *s*(t) and generates IF output. On the other hand, a dc imbalance (dc component of ΔI_{in}) results in a leakage of s(t) containing a 2LO frequency component to outputs..

Further following Eqn. (4.8), the emitter voltage (V_E) of a stacked-LO SHM, indicated in Fig. 4-7(a), can be simplified as

$$V_E = V_{DC} + V_T \ln\left[\cosh(X\cos\omega_{LO}t)\right], \quad (4.21)$$

whose fundamental frequency is $2f_{LO}$. For the SHM with delay compensation, V_E becomes

$$V_{E(C)} = V_{DC} + V_T \ln\left[\cosh(X\cos\omega_{LO}t) + \cosh(X\sin\omega_{LO}t)\right], \tag{4.22}$$

which is the same as a top-LO SHM because both LOI and LOQ signals affect this node, as indicated in Fig. 4-7(c). To clearly validate the improvement in isolation performance, the fast Fourier transform (FFT) of V_E in both SHMs at $2f_{LO}$ with respect to LO voltage swing (V_{LO}) is plotted in Fig. 4-9(a).

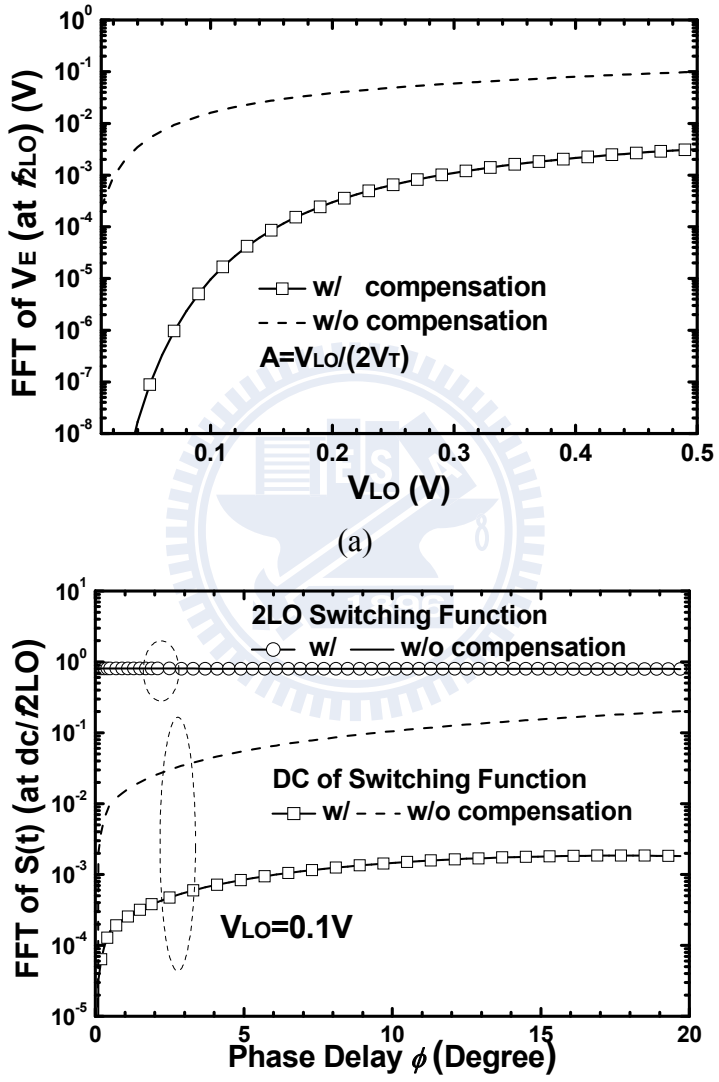


Fig. 4-9 (a) Fast Fourier transform (FFT) of the V_E at $2f_{LO}$ with respect to LO voltage (b) FFT of the S(t) at dc and $2f_{LO}$ with respect to a phase delay for both SHMs.

Ideally, the 2LO frequency component can be strongly suppressed by the proposed compensation circuit. This cancellation phenomenon has been discussed

using a graphic explanation of transient waveforms for MOS mixers but with different circuit implementations, a 4x SHM [44] and a merged LNA and I/Q mixer [45].

The FFT of the switching function $s(t)$ for both SHMs at dc and $2f_{LO}$ with respect to a phase delay (ϕ) is shown in Fig. 4-9(b). The dc of $s(t)$ results in an RF leaky path to output without a frequency translation. Using the compensation circuit, the dc term of $s(t)$ can be highly suppressed while the 2LO switching performance still maintains as shown in Fig. 4-9(b). The mathematic analyses Eqns. (4.19)-(4.22) are based on the exponential transfer curve which is still preserved at different temperatures for a SiGe HBT device. Thus, the isolation improvement by the compensation core is still significant over temperature.

In addition, the phase delay between the top and bottom cells can be approximated as $(180°/\pi)\times\tan^{-1}(f/f_T)$ which is the current phase delay of a common-base configuration and f_T is the current cut-off frequency. Conventionally, if no delay compensation is applied, the phase delay (usually >> 10° at high frequencies) greatly degrades the RF-to-IF isolation, even if the LO signal is perfectly differential-quadrature.

4.3 15-GHz SiGe HBT Sub-Harmonic Mixer With Delay Compensation

Fig. 4-10 shows the schematic of 15-GHz SHMs w/ and w/o delay compensation. Each stacked-LO core (Q_1-Q_8/Q_{a1}-Q_{a8}) consists of two Gilbert cells in cascode configuration with a 90° LO input phase offset. The LOI is applied to the top cell of the main SHM and LOQ to the bottom one while the opposite connections are applied to the top/bottom cells of the compensation core. The double-balanced topology ideally achieves infinite LO-to-RF/IF isolation; however, any signal/device mismatch and substrate coupling degrade both the isolation and even-order distortion

performance. The current bleeding technique is used to boost the conversion gain by drawing out the dc current from the mixer core to allow larger loading resistances, thus resulting in a lower transistor f_T. In this work, the current density of transistors in the SHM without compensation is 0.4 mA/μm^2 with a 40-GHz f_T. The transistor in the SHM with compensation has a current density of 0.2 mA/μm^2 with a 30-GHz f_T because the two stacked-LO cells are in parallel. Note that, a wideband common-collector voltage buffer is employed at each I/Q output to validate the pure isolation performance without additional suppression of LO leakage [40], [46]-[47].

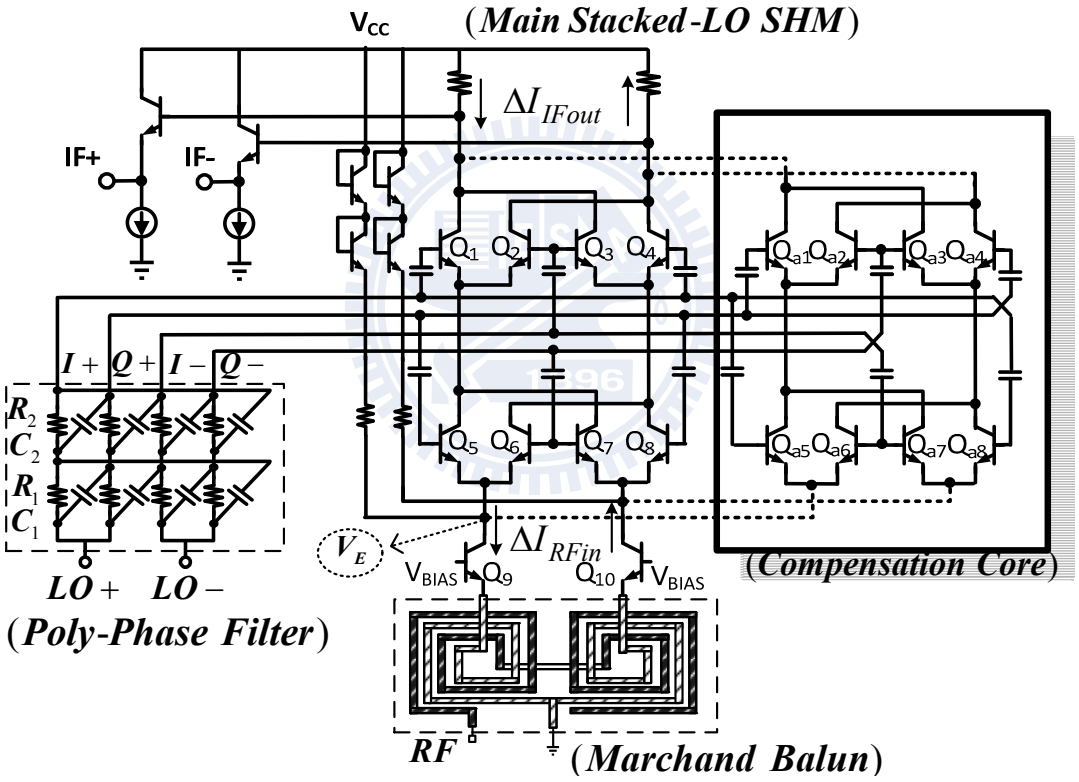


Fig. 4-10 Schematic of the SiGe HBT SHMs w/ and w/o delay compensation. (LO bias circuit is not shown for simplicity)

Differential-quadrature LO signals are generated by a two-stage poly-phase filter (PPF) from differential LO signals. For the designed center frequency of 7.5 GHz, the resistances and capacitances are 50 Ω and 0.424 pF in the first stage and are 100 Ω and 0.212 pF (two 0.424-pF capacitors in series) in the second stage. The progressive

increase of the resistances somewhat relaxes the voltage loss. Additionally, all the dc biases of the following mixer cores are fed from 5-kΩ resistors. An RF Marchand balun [31], [34], [47] consisting of two quarter-wavelength spiral edge-coupled coupled lines is used to generate differential signals as shown in Fig. 4-10. Each coupled line has a line width, line spacing and outer diameter of 8 μm, 2 μm and 270 μm, respectively.

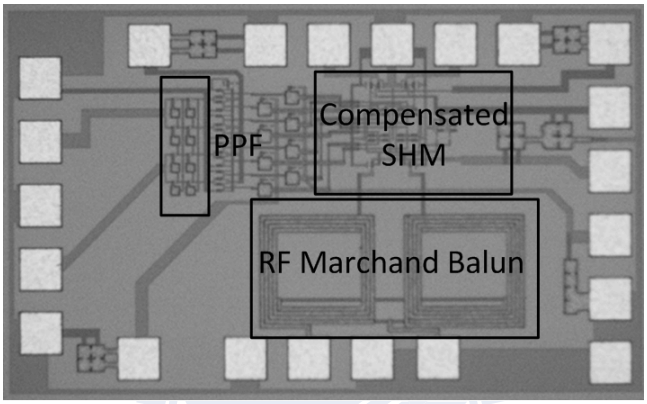


Fig. 4-11 Die photo of the SiGe HBT SHM w/ compensation.

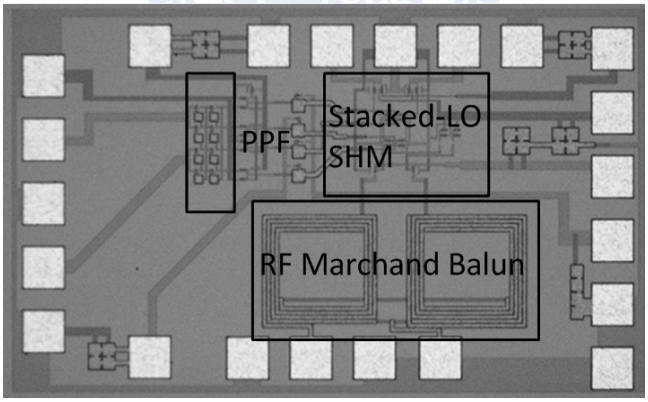


Fig. 4-12 Die photo of the SiGe HBT SHM w/o compensation.

Die photos of the SHMs w/ and w/o delay compensation are shown in Fig. 4-11 and Fig. 4-12, respectively. The supply voltage is 3.3 V with the total current consumption of 8 mA (5mA in mixer core; 1.5 mA in each IF I/Q buffer) for both circuits. The conversion gain with respect to RF frequency is shown in Fig. 4-13. With an LO power of −2 dBm, the SHMs w/ and w/o compensation have a peak

conversion gain of 10/11 dB at RF=8 GHz with an RF bandwidth of 5-17 GHz which is dominated by the RF Marchand balun. The EM simulated frequency response of the Marchand balun is also shown in Fig. 4-13.

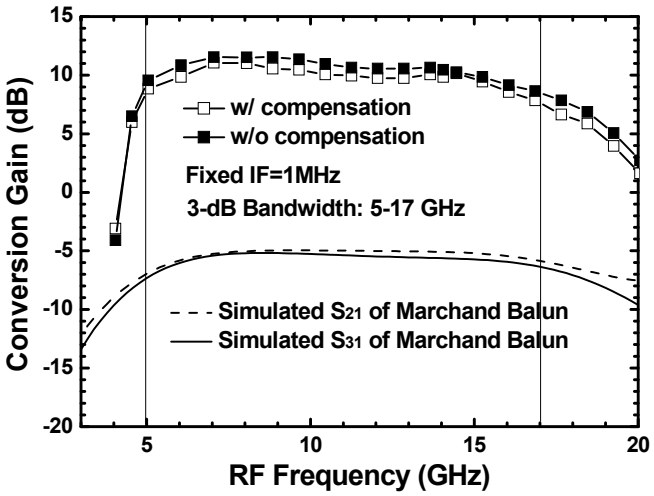


Fig. 4-13 Conversion gain as a function of RF frequency.

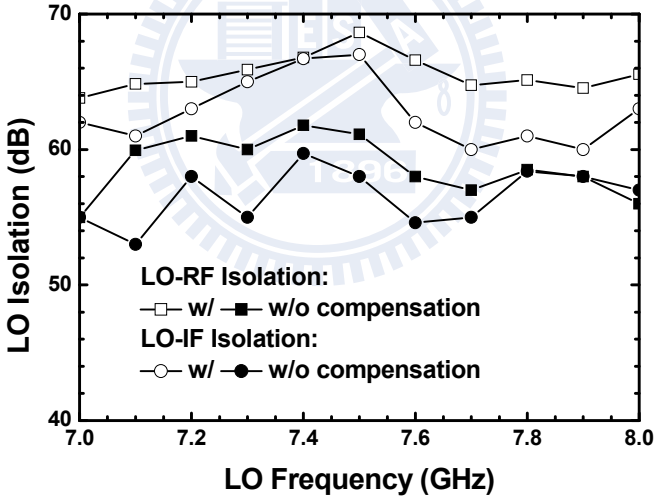


Fig. 4-14 LO-to-RF/IF isolation.

The LO-to-RF/IF isolation is shown in Fig. 4-14 and the 2LO-to-RF/IF and RF-to-IF isolation is shown in Fig. 4-15 at f_{LO}=7.5 GHz (center frequency of the PPF) and f_{RF}=15.001 GHz. By the compensation technique, large improvement covering a wide bandwidth is obtained. The 2LO-to-RF/IF isolation is improved by 34/35 dB, LO-to-RF/IF isolation by 8/9 dB and RF-to-IF isolation by 22 dB at 15 GHz. To verify the effect of process variation, five random samples are measured. Thus, the

2LO-to-RF/IF isolation performance of the SHM w/ compensation still shows at least 30 dB improvement than that of the SHM w/o compensation.

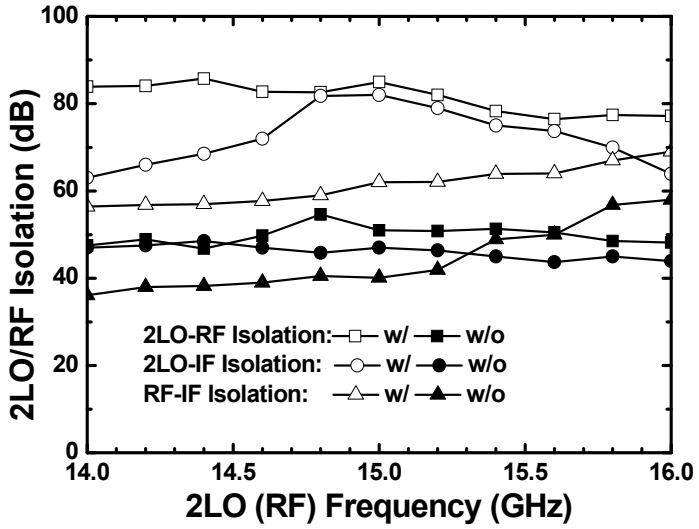


Fig. 4-15 2LO-to-RF/IF and RF-to-IF isolation.

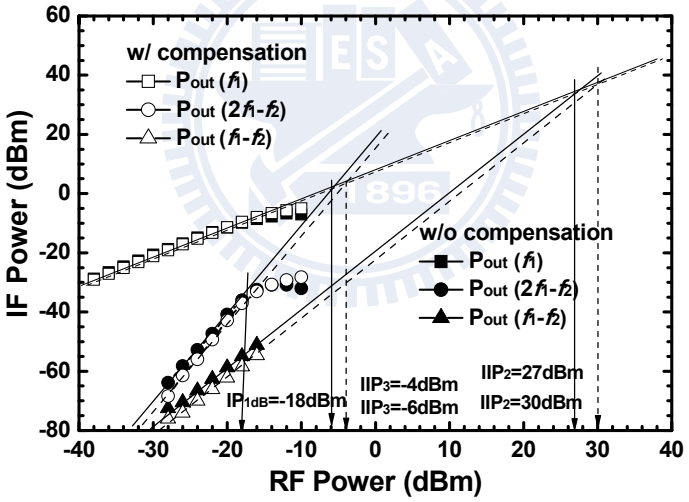


Fig. 4-16 Power performance.

Fig. 4-16 shows the power performance of the SHMs w/ and w/o compensation at f_{LO}=7.5 GHz, f_{RF1}=15.001 GHz and f_{RF2}=15.0012 GHz; thus, the IP_{1dB}, IIP_3 and IIP_2 are −18/−18 dBm, −4/−6 dBm, and 30/27 dBm, respectively. The input return loss of both SHMs is better than 11 dB from 5 to 30 GHz. The SHMs w/ and w/o compensation achieve conversion gain of 9/10 dB with 200-MHz IF bandwidth and double-sideband noise figure of 14/13.5 dB when f_{LO}=7.5 GHz as shown in Fig. 4-17.

The thermal noise of an active mixer is dominated by the RF Marchand balun and the input transconductance stage; thus, the overall noise figure is similar for both SHMs because of the identical transistor sizes and bias conditions.

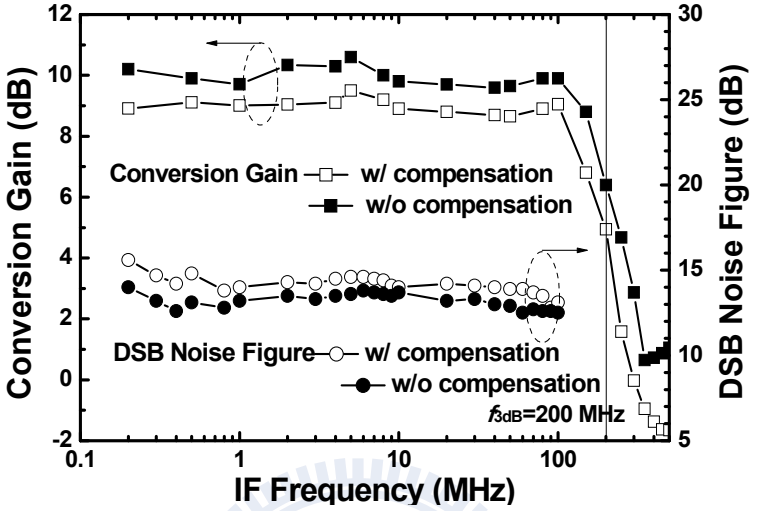


Fig. 4-17 Conversion gain and double sideband noise figure.

An SHM using a fully symmetrical LO doubler core [43] was demonstrated in our previous work [46]; however, eight extra transistors and unbalanced current density of mixer transistors in that topology limit the performance, including the maximum operating frequency and isolation performance with the same dc power consumption.

We also implemented the compensated SHM using 0.15-μm pseudomorphic high electron mobility transistor (pHEMT) technology (with peak f_T of 85 GHz) [47] and the comparisons of SHMs w/ and w/o compensation are also done by using 0.15-μm metamorphic high electron mobility transistor (mHEMT) technology (with peak f_T of 110 GHz). TABLE. 4.1 summarizes the circuit performance of the SHMs using 0.35-μm SiGe HBT, 0.15-μm pHEMT, and 0.15-μm mHEMT technologies.

However, the large difference in mobility between the two-dimensional electron gas (2-DEG) channel and electrons in AlGaAs donor layer cause the pHEMT device

sensitive to process variation. A small difference in gate recess etching results in a strong drain current variation. Thus, isolation performance was limited by a large device mismatch. On the other hand, the I-V curve in SiGe HBT technology depends on the material bandgap. The advance in modern epitaxial techniques improves SiGe HBT device match greatly by controlling the bandgap precisely. Due to the better device match in the SiGe HBT technology, 2LO-RF/2LO-IF/LO-RF/LO-IF/RF-IF isolation in this work is 35/37/29/37/32 dB better than that reported in [47] for the compensated pHEMT SHM. Further, as indicated in TABLE. 4.1, the isolation improvement in mHEMT technology is also valid. However, the device mismatch is much more significant than the effect of the current phase delay. Thus, the overall isolation performance is not good and the improvement is also limited .

TABLE. 4.1 PERFORMANCE COMPARISON OF SHMS WITH DELAY COMPENSATION USING DIFFERENT TECHNOLOGIES

Technology	0.35-μm SiGe HBT (peak f_T=67 GHz)		0.15-μm pHEMT (peak f_T=85 GHz)	0.15-μm mHEMT (peak f_T=110 GHz)	
Delay Compensation	Yes	Yes	Yes	Yes	No
RF Frequency (GHz)	15	15	40	39	42
Conversion Gain (dB)	10	11	3.1	1	0.5
Noise Figure (dB)	14	13.5	18	23	20
IP_{1dB} (dBm)	−18	−18	−5	−11	−10
IIP_3 (dBm)	−4	−6	10	−3	0
LO Power (dBm)	−2	−2	10	7	5
2LO-to-RF Isolation (dB)	85	51	50	37	32
2LO-to-IF Isolation (dB)	82	47	45	41	39
LO-to-RF Isolation (dB)	69	61	40	--	--
LO-to-IF Isolation (dB)	67	58	30	--	--
RF-to-IF Isolation (dB)	62	40	30	32	27
IF Bandwidth (MHz)	200	200	550	800	800
Supply Voltage (V)	3.3	3.3	8	7	7
Current Consumption (mA)	8	8	11	12	12

Chapter 5 Dual-Conversion Low-IF Receiver With Large Image Rejection

5.1 INTRODUCTION

A low IF downconversion architecture is widely used [48]-[50] since this architecture can directly avoid dc offset and flicker noise problems. A static or random dc offset may cause a demodulation error while preposterous flicker noise may cover up desired signals and results in a fatal detection error, especially in a CMOS process [51]-[53]. On the other hand, series capacitors can be added at the output to block the dc component in a low-IF receiver because the downconverted signal is not located at dc. The flicker noise can be avoided by choosing a proper IF band beyond the flicker noise corner. However, a higher IF band results in higher power consumption for the subsequent analog-to-digital converter (ADC). Besides, a dual-conversion downconverter alleviates the burden of a high-frequency LO signal generation, but two conversions have two image bands to be suppressed.

A single-conversion zero-IF (direct-conversion) dual-band system needs two separate systems including two LO generators [54]. On the other hand, with a suitable frequency planning, hardware reuse [including low-noise amplifier (LNA), mixer, and LO generator] is achievable in a dual-conversion system. For example, the second-stage mixer is reused [14] but two sets of LNAs, first-stage mixers and LO_1 generators are still required, as shown in Fig. 5-1(a). In [55], the dual-band concurrent LNA and the first-stage mixer are reused. The two signal bands after the first downconversion should be downconverted to baseband by two different LO_2 signals, as shown in Fig. 5-1(b). That is, at least three LO generators should be utilized. Further, as shown in Fig. 5-1(c), the first- and second-stage mixers are reused with an

RF input switchable transconductance stage while the LO_1 signal is set approximately but not exactly halfway between the two operation bands [13]. Therefore, the first-downconverted signals are near and can be selected by choosing proper LO_2, like a wideband IF architecture. However, the LO_1 and LO_2 frequencies can not be correlated for this frequency planning. Finally, fully reused first/second-stage mixers are demonstrated while the LO_1 is set exactly halfway between the two bands, as shown in Fig. 5-1(d) [56]. After the first downconversion, the two bands are located at either positive or negative frequency spectrum. Thus, the output signal can be selected in the second-stage mixer.

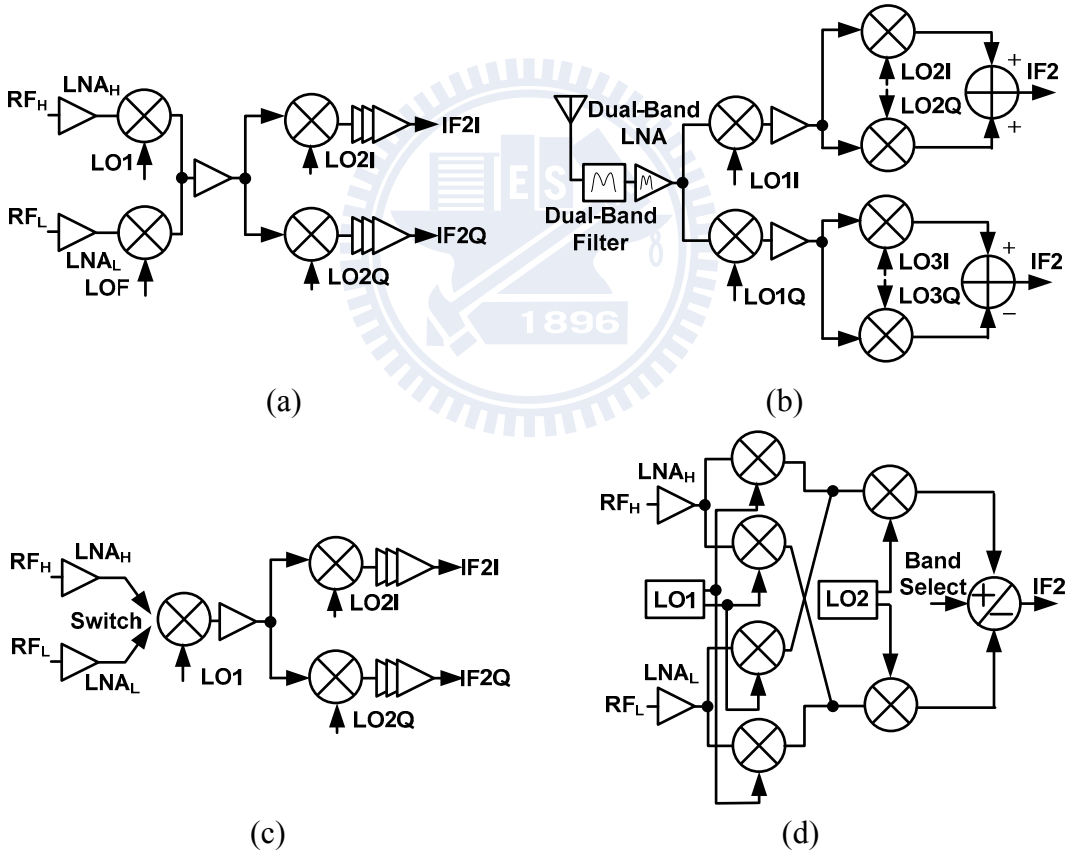


Fig. 5-1 Block diagrams of dual-conversion receivers (a) with reused second-stage mixer (b) with reused LNA and first-stage mixer (c) with reused first- and second-stage mixers and a switchable mixer RF input stage (d) with reused first- and second-stage mixers.

Unlike the zero-IF architecture discussed above, the LO_1 and LO_2 signals are easier to be generated from only one signal source (*i.e.*, VCO) in a low-IF architecture.

Besides, to avoid the flicker noise, dc offset and IIP_2 problems of a direct-conversion receiver (DCR)[57]-[58], a low-IF receiver is also widely chosen and implemented [26], [48], [59]-[60]. Instead of solving those problems in a direct-conversion system, filtering or suppressing the image signals or interference becomes the most important issue of a low-IF receiver since the final IF frequency is not zero.

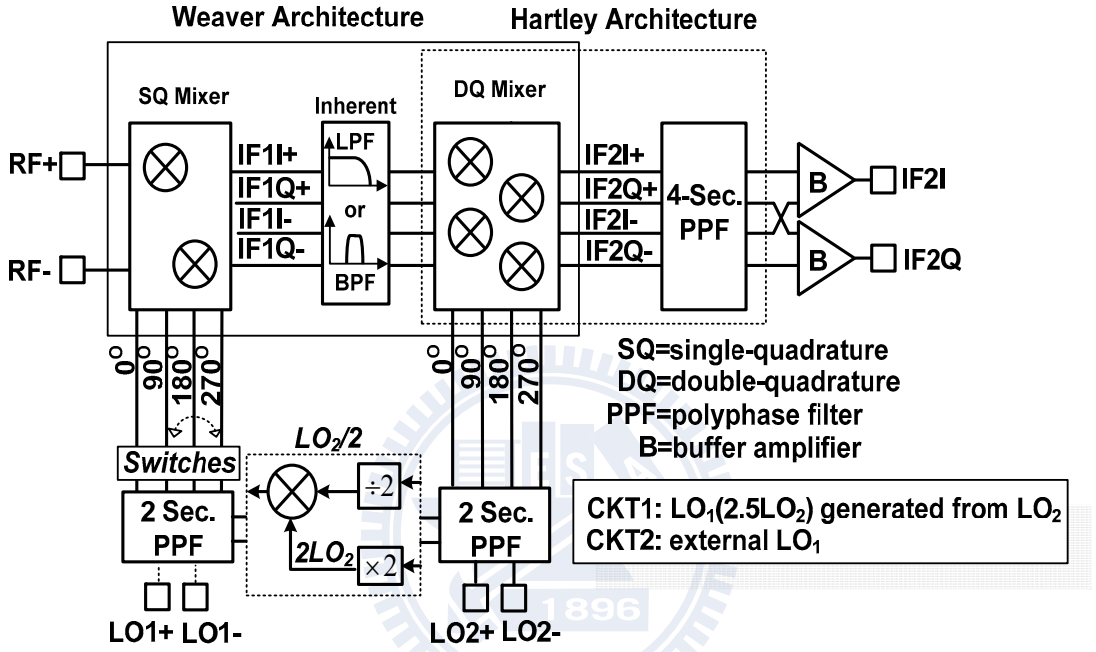
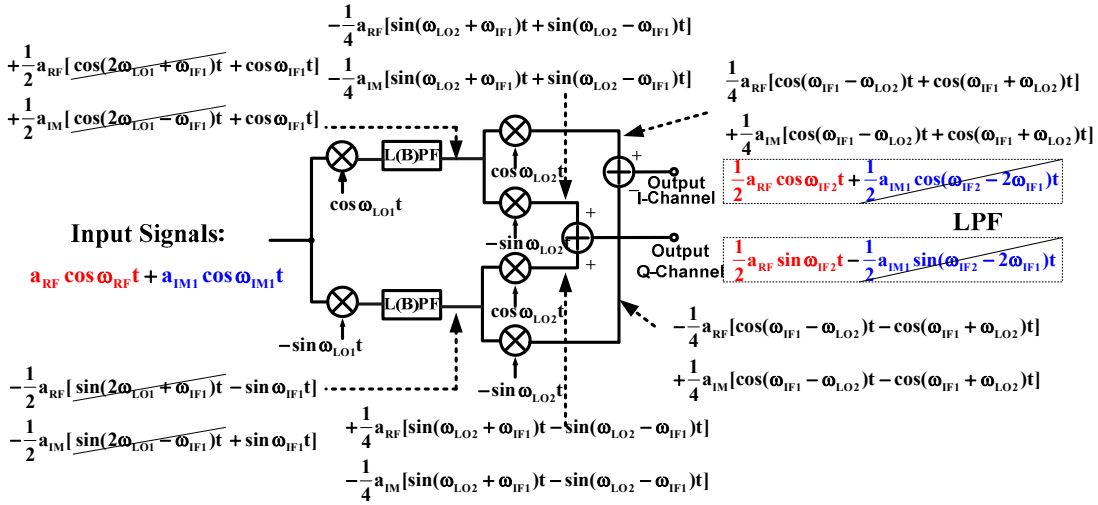


Fig. 5-2 Block diagram of a single/dual-band dual-conversion Weaver-Hartley low-IF system.

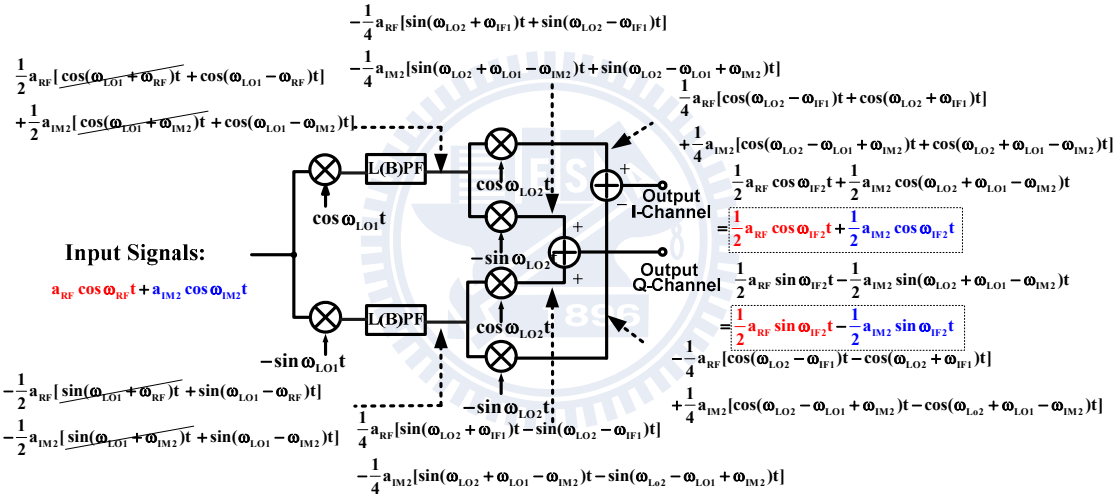
In this chapter, the dual-conversion low-IF system combines the Weaver architecture [28], [61]-[62] and Hartley architecture [63]. A Weaver architecture is a complex dual-conversion system, consisting of a single-quadrature first-stage complex mixer and a double-quadrature second-stage complex mixer as shown in Fig. 5-2. On the other hand, a Hartley architecture consists of a complex mixer and a complex filter, such as a passive microwave coupler [64], a poly-phase filter (PPF) [26], [65] or an active complex band-pass filter [50], [60], [66].

A single-quadrature complex mixer includes two real mixers with either a quadrature RF or LO input while the other is kept differential. A double-quadrature complex mixer includes four real mixers with both LO and RF signals being

quadrature.



(a)



(b)

Fig. 5-3 Block diagram of the Weaver architecture (a) when input signals are desired RF signal and first image signal (b) when input signals are desired RF signal and second image signal.

In a Weaver system, received signals are twice downconverted to a low-IF band by the LO_1/LO_2 signals. The angular frequencies of the desired RF, first image (IM_1), and second image (IM_2), LO_1, and LO_2 signals are denoted as ω_{RF}, ω_{IM1}, ω_{IM2}, ω_{LO1} and ω_{LO2}, respectively. The angular frequencies of the IF signal after the first and second downconversions are defined as ω_{IF1} and ω_{IF2}, respectively. The relations of the signals defined above can be expressed as:

$$\begin{cases} \omega_{RF} - \omega_{LO1} = \omega_{LO1} - \omega_{IM1} = \omega_{IF1} \\ \omega_{RF} - (\omega_{LO1} + \omega_{LO2}) = (\omega_{LO1} + \omega_{LO2}) - \omega_{IM2} = \omega_{IF2} \\ \omega_{IF1} = \omega_{LO2} + \omega_{IF2} \end{cases} . \quad (5.1)$$

The wire connection of the Weaver system with detailed mathematical analyses is shown in Fig. 5-3. Fig. 5-3(a) indicates the results at each node of the Weaver system when the input signals are RF and IM_1. Both signals are converted to the same IF_1 frequency (ω_{IF1}) but with opposite signs of the quadrature signals after the first downconversion. The high-frequency term ($2\omega_{LO1}+\omega_{IF1}$) can be eliminated by the low-pass/band-pass nature of the first-stage mixer. The other two signals entering the second-stage mixers are downconverted to ω_{IF2} and ($2\omega_{IF1}-\omega_{IF2}$) bands, respectively. Therefore, the shifted-out image signal can be easily filtered-out by the low-pass filter at IF_2 stage [28].

On the other hand, the RF and IM_2 signals are downconverted to ω_{IF1} and ($\omega_{IF1}-2\omega_{IF2}$), respectively, after the first downconversion, as shown in Fig. 5-3(b). The two signals are still very close and hard to be separated by a narrow-band filter. After the second conversion, the two signals locate at the same frequency (ω_{IF2}) but with opposite signs of quadrature signals. That is, the Weaver system can reject the IM_1 but it has no ability to reject the IM_2. To solve this problem, a PPF is cascaded after the Weaver system because the PPFs can reject the negative-frequency signal but pass the positive-frequency signal [26]. As a result, the image signals at the negative spectrum can be highly rejected. The second-stage complex mixers with the subsequent PPF can be called the Harley system.

For a dual-band application, the polarity of the LO_1 signal is set to be switchable (*i.e.*, the input signal can be chosen to be either left-shifted or right-shifted for a

complex mixing) [67]. In order to reuse the second-stage mixers, the LO_1 frequency is set at the halfway point between two application bands. That is, the desired signal of the high-frequency band is the image signal of the low-frequency band and vice versa. The frequency relations are given below:

$$\begin{cases} \omega_{RFH}(\omega_{IM1L}) - \omega_{LO1} = \omega_{LO1} - \omega_{IM1H}(\omega_{RFL}) = \omega_{IF1} \\ \omega_{RFH} - (\omega_{LO1} + \omega_{LO2}) = (\omega_{LO1} + \omega_{LO2}) - \omega_{IM2H} = \omega_{IF2} \\ \omega_{IM2L} - (\omega_{LO1} - \omega_{LO2}) = (\omega_{LO1} - \omega_{LO2}) - \omega_{RFL} = \omega_{IF2} \\ \omega_{IF1} = \omega_{LO2} + \omega_{IF2} \end{cases} \tag{5.2}$$

where the suffix H and L represent high-frequency and low-frequency operation modes, respectively.

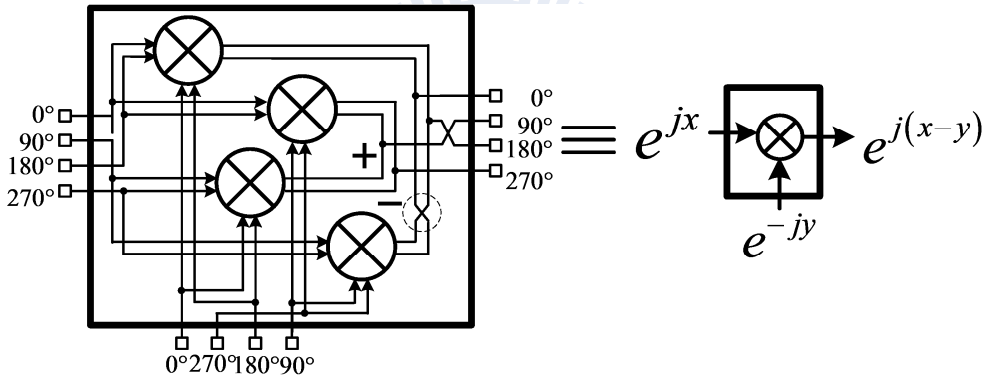
For the first conversion, the positive spectrum of the desired signal (ω_{RFH}) is left-shifted to ω_{IF1} at high-frequency mode while the negative spectrum of the desired signal ($-\omega_{RFL}$) is right-shifted to the same band (ω_{IF1}) at low-frequency mode as described in Eqn. (5.2). Similar to the single-band case, the first image signal is shifted away from the output pass-band while the second image signal is filtered out by the following multi-stage PPF, in the Weaver-Hartley hybrid system.

However, in previous literatures of dual-conversion low-IF downconverters [56], [62], [65], [67], including our previous work, the IRR_1 was limited to about 40-45 dB without an LNA; while the IRR_2 was unable to reach the theoretical limit due to device/signal mismatch, layout path imbalance, and process variations. Section 5.2 analyzes in detail image rejection performance of the dual-conversion receiver, and then introduces two Weaver-Hartley dual-conversion low-IF downconverters with large improvement in image rejection.

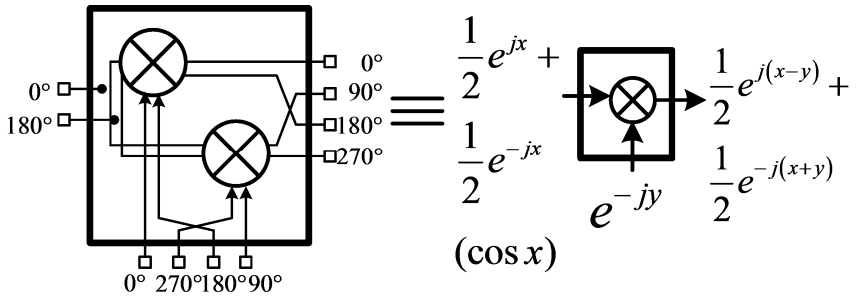
5.2 LARGE IMPROVEMENT IN IMAGE REJECTION IN WEAVER-HARTLEY RECEIVERS

5.2.1 Introduction

To deeply and clearly analyze the image rejection performance, complex signal notations are introduced. Thus the mixing operations of complex double-quadrature and single-quadrature topologies can be expressed by the complex signal multiplication as shown in Fig. 5-4 (a) and (b), respectively. A double-quadrature mixer topology includes four real mixers with two quadrature inputs while a single-quadrature complex mixer has two real mixers with only one of the two inputs being quadrature.



(a)

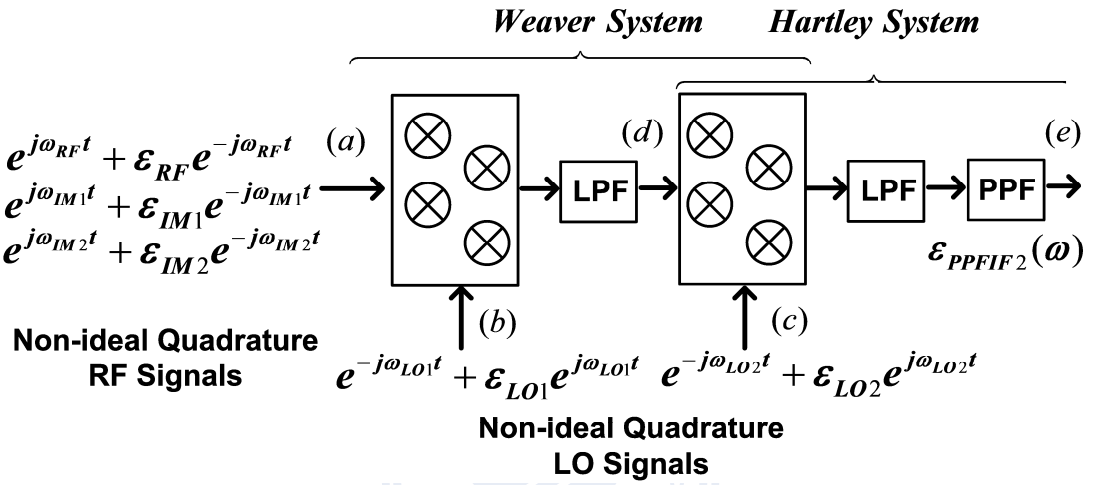


(b)

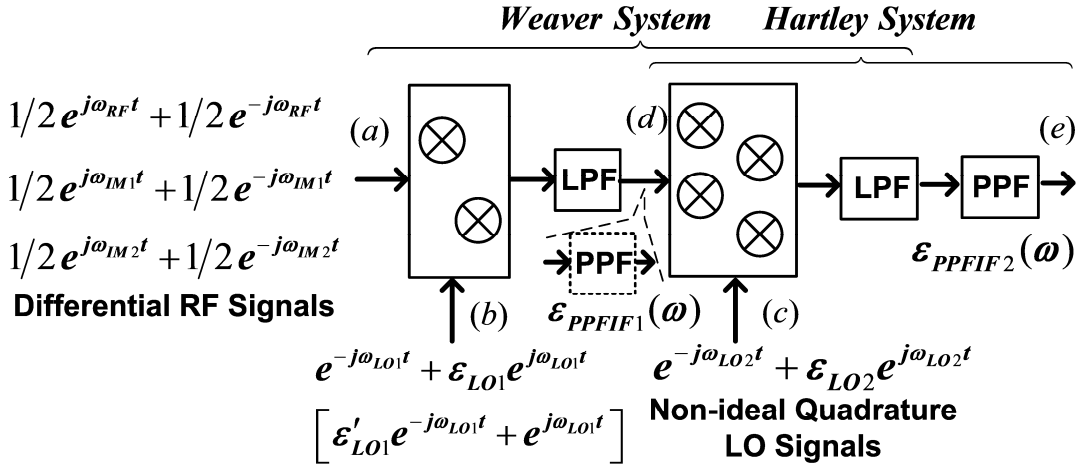
Fig. 5-4 (a)Schematic of a double-quadrature complex mixer topology and its complex representation (b) schematic of a single-quadrature topology and its complex representation.

Double-quadrature-double-quadrature/ single-quadrature-double-quadrature Weaver-Hartley architectures and their complex notations are illustrated in Fig. 5-5(a)

and (b), respectively. The desired RF signal and image signals are downconverted to a low-IF band by the first local oscillator (LO_1) and second local oscillator (LO_2). The angular frequencies of the desired, first image, second image, first LO, and second LO signals are denoted as ω_{RF}, ω_{IM1}, ω_{IM2}, ω_{LO1} and ω_{LO2}, respectively. Additionally, the angular frequencies of the IF signal after the first and second downconversions are defined as ω_{IF1} and ω_{IF2}, respectively.



(a)



(b)

Fig. 5-5 Block diagrams of (a) a double-quadrature-double-quadrature dual-conversion system and (b) a single-quadrature-double-quadrature dual-conversion system with non-ideal input signals.

The relations of the signals defined above can be expressed as Eqn. (5.1). The operations of double-quadrature-double-quadrature/ single-quadrature-double-

quadrature is described in Section 5.1. On the other hand, the dual-band operations of the Weaver-Hartley downconverter are given as Eqn. (5.2) in Section 5.1.

Input I/Q signal mismatch and device mismatch of the mixers are unavoidable for a practical circuit fabrication and lead to a degradation of IRR. The device mismatch can be referred to an input I/Q signal gain/phase mismatch. When a quadrature phase error or an amplitude mismatch exists, opposite phasor sequence (or opposite complex-frequency signal) is induced. Imperfect input signals can be represented as a positive spectrum with an error negative spectrum

$$e^{j\omega_1 t} + \varepsilon_1 e^{-j\omega_1 t} \tag{5.3}$$

where $(\omega_1, \varepsilon_1) \in \{(\omega_{RF}, \varepsilon_{RF}), (\omega_{IM1}, \varepsilon_{IM1}), (\omega_{IM2}, \varepsilon_{IM2})\}$; ε_{RF}, ε_{IM1}, and ε_{IM2} are the input error functions at ω_{RF}, ω_{IM1}, and ω_{IM2}, respectively.

Similarly, imperfect quadrature LO_1 and LO_2 signals can also be decomposed into

$$e^{-j\omega_{LO1}t} + \varepsilon_{LO1} e^{j\omega_{LO1}t} \tag{5.4}$$

$$e^{-j\omega_{LO2}t} + \varepsilon_{LO2} e^{j\omega_{LO2}t} . \tag{5.5}$$

All of the error functions are much smaller than unity. Note that, for the low-band operation of the dual-band architecture, the LO_1 signal should be switched to $e^{j\omega_{LO1}t} + \varepsilon'_{LO1} e^{-j\omega_{LO1}t}$ as shown in Fig. 6(b).

After the complex mixing operation at the first stage as shown in Fig. 5-5(a), we can obtain

$$e^{j(\omega_1 - \omega_{LO1})t} + \varepsilon_1 \varepsilon_{LO1} e^{-j(\omega_1 - \omega_{LO1})t} . \tag{5.6}$$

Here, the high-frequency terms are negligible thanks to the inherent low-pass characteristics of active mixers.

By the same token, the outputs after the second conversion can be expressed as

$$\begin{cases} e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}\varepsilon_{RF}\varepsilon_{LO1}\varepsilon_{LO2}e^{-j\omega_{IF2}t} & (RF \text{ input}) \\ \varepsilon_{IM1}\varepsilon_{LO1}e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}\varepsilon_{LO2}e^{-j\omega_{IF2}t} & (IM_1 \text{ input}) \\ \varepsilon_{IM2}\varepsilon_{LO1}\varepsilon_{LO2}e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}e^{-j\omega_{IF2}t} & (IM_2 \text{ input}) \end{cases} \quad (5.7)$$

where $\varepsilon_{PPF(IF2)}$ is the error function of the PPF at the output of the second-stage mixers.

Similar to a double-quadrature-double-quadrature downconverter, a single-quadrature-double-quadrature downconverter with differential input signals can be treated as a complex mixing with the input error function ε_1, defined in Eqn. (5.5), equaling one. The IF outputs of a single-quadrature-double-quadrature down-converter are directly rewritten as

$$\begin{cases} e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}\varepsilon_{LO1}\varepsilon_{LO2}e^{-j\omega_{IF2}t} & (RF \text{ input}) \\ \varepsilon_{LO1}e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}\varepsilon_{LO2}e^{-j\omega_{IF2}t} & (IM_1 \text{ input}) \\ \varepsilon_{LO1}\varepsilon_{LO2}e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}e^{-j\omega_{IF2}t} & (IM_2 \text{ input}) \end{cases} \quad (5.8)$$

Eqns. (5.7) and (5.8) provide detailed information for IRR degradation. Compared with Eqns. (5.7) and (5.8), the IRR_1 of a double quadrature system is ε_{IM1}^{-1} times larger than that of a single-quadrature system; thus, a fully double-quadrature system typically provides a higher IRR. However, if the quadrature LO signals are not accurate enough, the IRR_2 still degrades. But a double-quadrature-double-quadrature system suppresses the effect of the LO quadrature accuracy by a factor of ε_{IM2}^{-1} and thus guarantees that the IRR_2 can be almost determined by the IF_2 PPF. To solve the drawback of a single-quadrature-double-quadrature topology, an inter-stage PPF centered at ω_{IF1} with a frequency response of $\varepsilon_{PPF(IF1)}$ is inserted between the first- and

second-stage mixers as shown in Fig. 5-5(b). The outputs of the modified dual-conversion system are described as

$$\begin{cases} e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}\varepsilon_{LO2}\varepsilon_{PPF(IF1)}\varepsilon_{LO1}e^{-j\omega_{IF2}t} & (RF \text{ input}) \\ \varepsilon_{LO1}e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}\varepsilon_{LO2}\varepsilon_{PPF(IF1)}e^{-j\omega_{IF2}t} & (IM_1 \text{ input}) \\ \varepsilon_{PPF(IF1)}\varepsilon_{LO1}\varepsilon_{LO2}e^{j\omega_{IF2}t} + \varepsilon_{PPF(IF2)}e^{-j\omega_{IF2}t} & (IM_2 \text{ input}) \end{cases}. \quad (5.9)$$

The inserted inter-stage PPF guarantees a higher system dynamic range by reducing the large first image signal before entering the second-stage mixers even though the IRR_1 can not be improved [65]. However, when compared with Egns. (5.8) and (5.9), the quadrature accuracy of the IF signal is further improved and the IRR_2 can be further pushed to the theoretical limit of the IF_2 PPF.

PPFs are inserted at proper positions to minimize the effects of device/signal mismatches, and thus improve the image rejection without calibration. A 0.35-μm SiGe heterojunction bipolar transistor (HBT) 5.2-GHz double-quadrature-double-quadrature downconverter with an RF PPF is introduced in Section 5.2.2 while Section 5.2.3 describes a 0.18-μm CMOS 2.2/4.8-GHz single-quadrature-double-quadrature downconverter with a switched-band LNA and a narrow-band inter-stage PPF. Compared with our previous work [67], the 5.2-GHz downconverter achieves a 15 dB improvement in image-rejection ratio of the first image signal (IRR_1) even without a pre-selection filter or LNA. Additionally, the dual-band downconverter has a 25 dB improvement in image-rejection ratio of the second image signal (IRR_2), which nearly reaches the theoretical limit of a four-stage PPF covering 20-40 MHz.

5.2.2 Single-Quadrature-Double-Quadrature Architecture With an Inter-Stage Poly-Phase Filter

Fig. 5-6 shows the block diagram of a 0.35-μm SiGe HBT double-quadrature-

double-quadrature dual-conversion low-IF downconverter and corresponds to the architecture in Fig. 5-5(a). In a double-quadrature-double- quadrature downconverter, both the first- and second-stage complex mixers contain four Gilbert mixers.

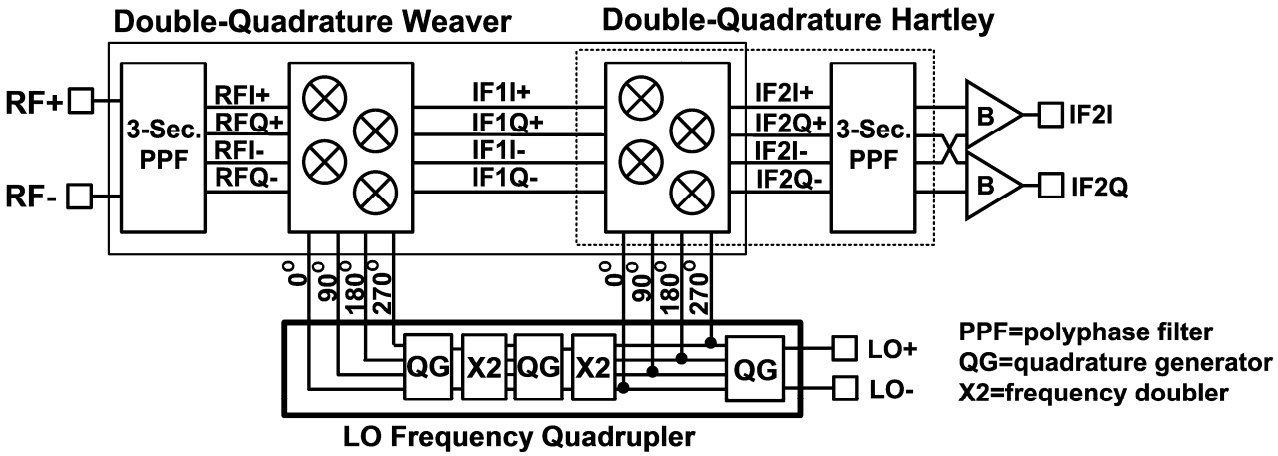
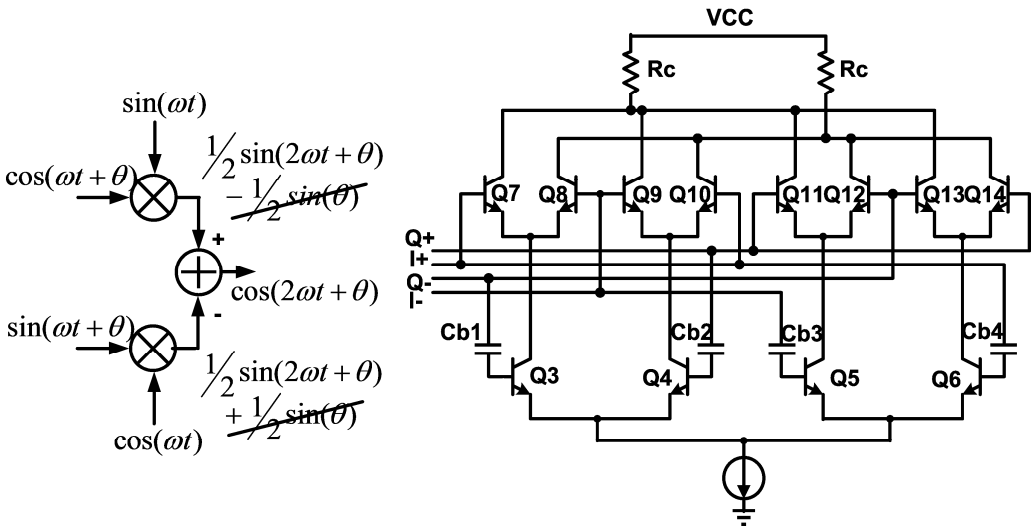


Fig. 5-6 Block diagram of a 0.35-μm SiGe HBT double-quadrature-double-quadrature Weaver-Hartley low-IF downconverter.

Correlated LO signals (LO_1 and LO_2) with the same phase error maintain a maximum IRR [28]. Fig. 5-7 (a) and (b) show the mathematic expression and the schematic of the compensated frequency doubler [43]; thus, the self-mixing dc offset, generated by the current phase delay (θ), can be eliminated. The LO frequency quadrupler in Fig. 5-6 consists of two compensated frequency doublers to generate coherent signals with less phase error.

A three-stage PPF is employed at the RF port for a quadrature signal generation at three bands, f_{RF}, f_{IM1} and f_{IM2}. The multi-band PPF design has been introduced in Section 3.1.3. Because f_{RF} (5.2 GHz) > f_{IM2} (5.14 GHz)> f_{IM1} (3.072 GHz), the transmission zeros of the three stages are set according to this order to minimize the loss of PPF. Therefore, the desired signal and image signals are perfectly quadrature in nature.



(a) (b)

Fig. 5-7 (a) Block diagram of a high-precision compensated frequency doubler (b) schematic of the compensated frequency doubler employed in the LO quadrupler. (Bias circuit is not shown for simplicity)

In the LO quadruplers, two-stage PPFs are employed in the LO_1/LO_2 output quadrature generators and the quadrature generator required by the compensated frequency doublers. The center frequencies of the two-stage PPFs are set the same and the resistance in the second stage is twice as large as that in the first stage while the capacitance is only half. Since the U-NII-1 and U-NII-2 bands covering 5.15-5.35 GHz with 200 MHz bandwidth, it means a ratio bandwidth of 1.04 (=5.35/5.15) for the RF band is needed. However, the implemented signal bandwidth needs to be designed wider than the required one to tolerate the silicon process variation. As described in Section 3.1.3, the IRR at the original center frequency becomes 20.8 dB for a single-stage PPF and 41.6 dB for a two-stage PPF if a 20% frequency deviation is applied. Therefore, a two-stage cascade PPF is sufficient for the LO generator when considering both the required signal bandwidth and process variation if a 40-dB IRR is set as the criterion. Besides, in order to obtain about 50-dB IRR within the bandwidth of 15-35 MHz, a three-stage PPF is incorporated at the end of the

downconverter.

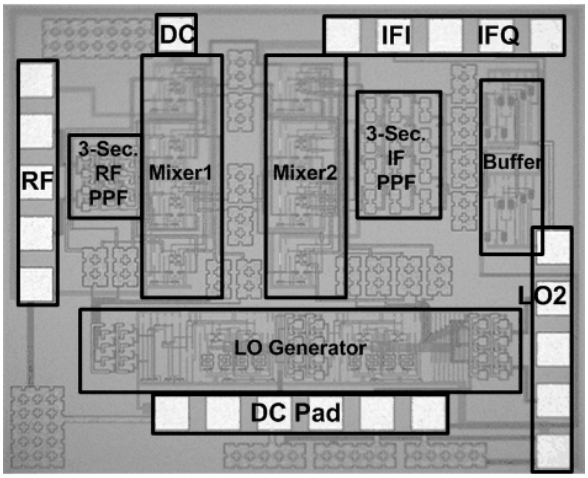


Fig. 5-8 Die photo .

A die photo of the 5.2-GHz downconverter is shown in Fig. 5-8 and the die size is 1.6×1.35 mm^2. The total current of eight mixers is 32 mA at a 3.3-V supply while the LO generator and the IF output buffers consume 35 mA. A conversion gain reaches 10 dB when the LO power is larger than –4 dBm. The measured single-sideband noise figure is lower than 20 dB for f_{IF2} ranging from 15-35 MHz as shown in Fig. 5-9. The flicker noise corner in Fig. 5-9 is absent (less than 1 MHz) thanks to the low flicker noise of SiGe HBT devices. The downconverter has an IP_{1dB} of –8 dBm and an IIP_3 of 9 dBm when f_{RF}=5.2 GHz, f_{LO2}=1.034 GHz, f_{LO1}=4×f_{LO2}, and f_{IF}=30 MHz, as shown in Fig. 5-10 . Fig. 5-11 shows the IRR from three samples to be on average about 55/50 dB for the first/second image signals, respectively. The IRR of the second image signal has a band-pass shape because the PPF is a complex notch filter for the negative spectrum covering 15-35 MHz while the frequency response of the positive spectrum is relatively flat [67]. Fig. 5-12 shows the I/Q output waveforms with 0.022 dB amplitude imbalance and 0.55° phase error. The LO-to-RF isolation is 52 dB. The measured performance is summarized and compared with state-of-the-art architectures in TABLE. 5.1 in Section 5.2.4.

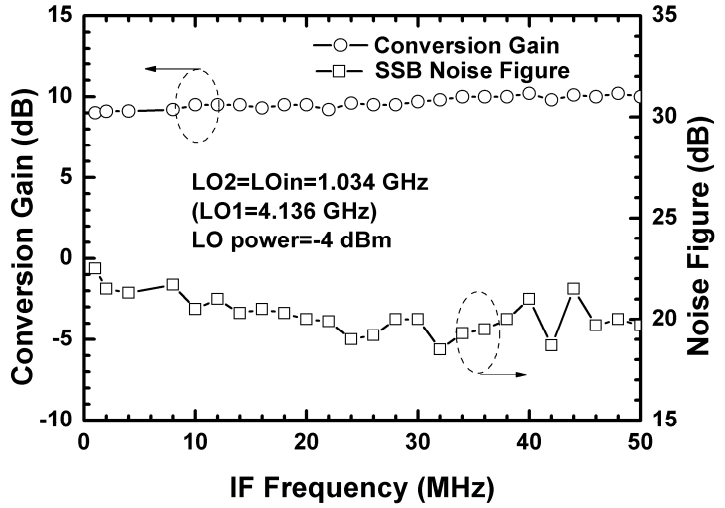


Fig. 5-9 Conversion gain and single-sideband noise figure.

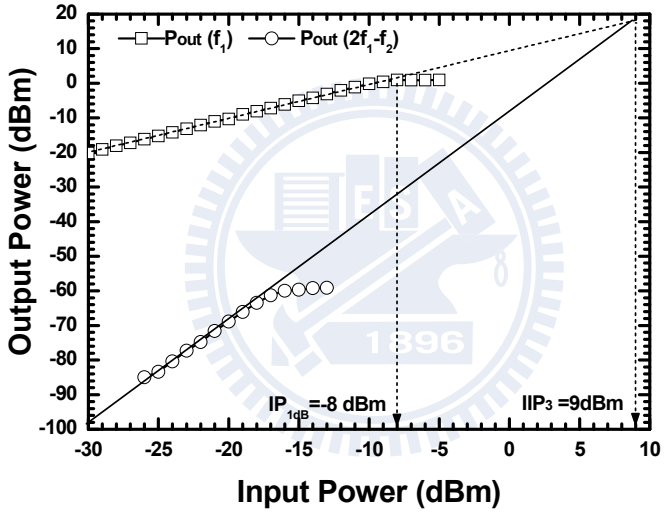


Fig. 5-10 Power performance.

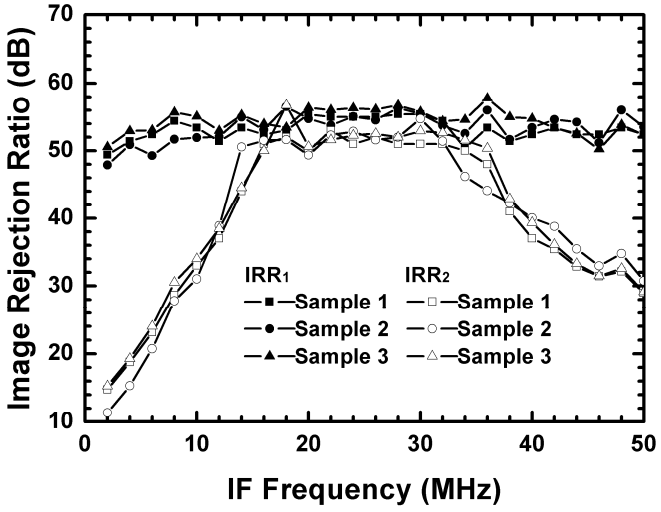


Fig. 5-11 IRR of the first/second image signals.

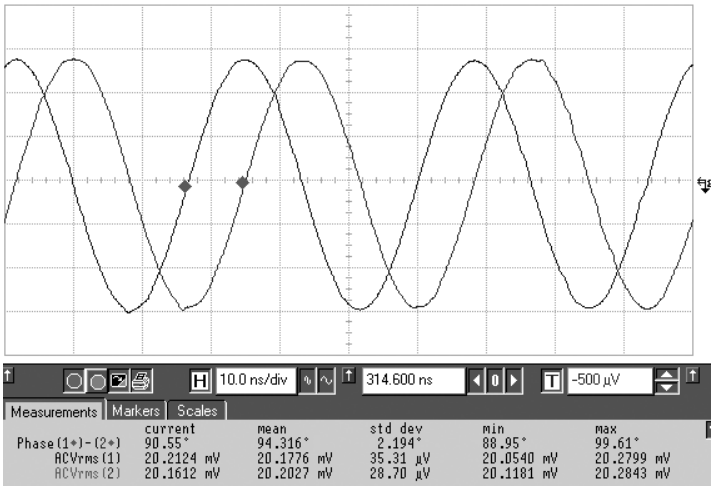


Fig. 5-12 Output I/Q waveforms.

5.2.3 Double-Quadrature-Double-Quadrature Architecture With an RF Poly-Phase Filter

Fig. 5-13 shows the block diagram of a 0.18-µm CMOS single-quadrature-double-quadrature dual-band low-IF receiver consisting of a dual-band LNA, a single-quadrature Hartley system and a double-quadrature Hartley system. Moreover, the cascaded complex mixer topology corresponding to the architecture in Fig. 5-5(b) can be treated as a Weaver architecture.

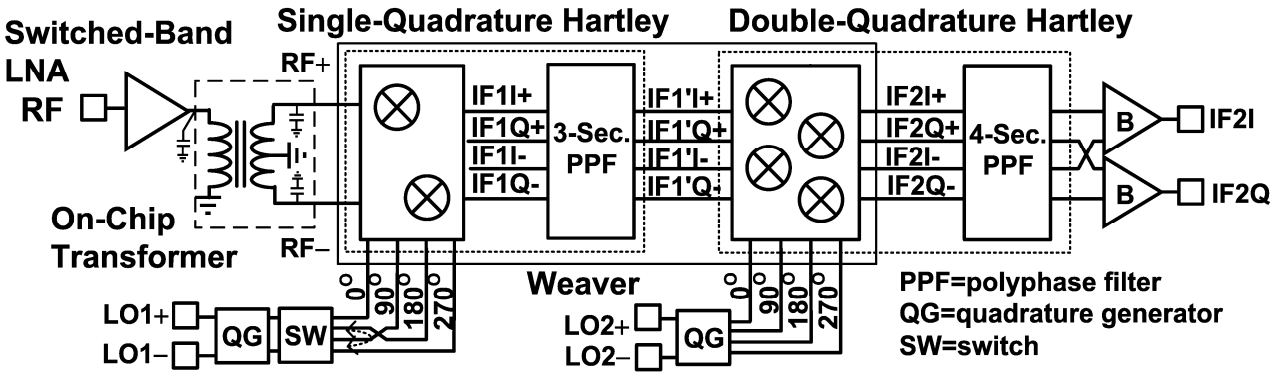
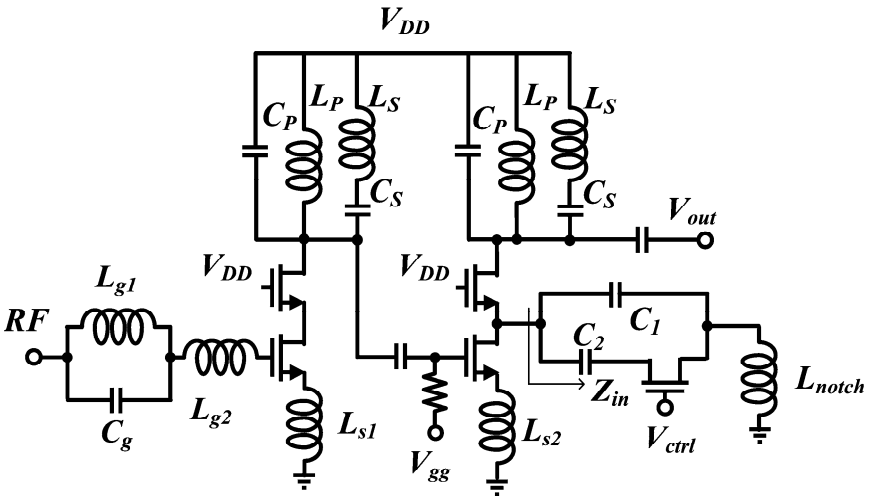
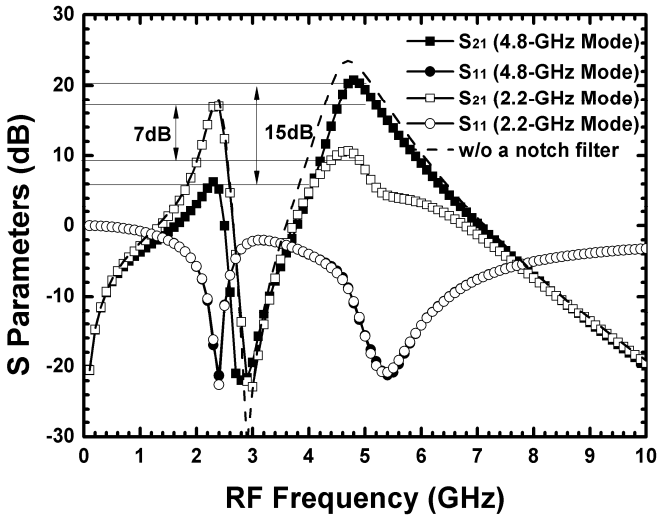


Fig. 5-13 Block diagram of a dual-band 0.18-µm CMOS single-quadrature-double-quadrature Weaver-Hartley low-IF downconverter.



(a)



(b)

Fig. 5-14 (a) Schematic of the LNA with a switchable notch filter and (b) the simulated frequency response.

Fig. 5-14(a) shows that the switched-band LNA consists of a switchable notch filter in the second stage. Previously, a notch filter consisting of a series LC resonator was inserted in the LNA to provide an additional IRR and suppress interference [69]-[69]. In this work, a switchable notch filter is employed. The resonance frequency is $1/\sqrt{L(C_1+C_2)}$ or $1/\sqrt{LC_1}$ when the control transistor is on or off, respectively. The simulated frequency response of the switched-band LNA with and without a switchable notch filter is shown in Fig. 5-14(b). The IRR_1 of a

single-quadrature-double-quadrature downconverter can be improved by a preceding narrow-band LNA to achieve over 50-dB IRR.

An on-chip miniature single-to-differential 3:2 transformer is utilized at the output of the LNA to generate differential RF signals compatible to the following double-balanced Gilbert mixers with a common-gate input stage.

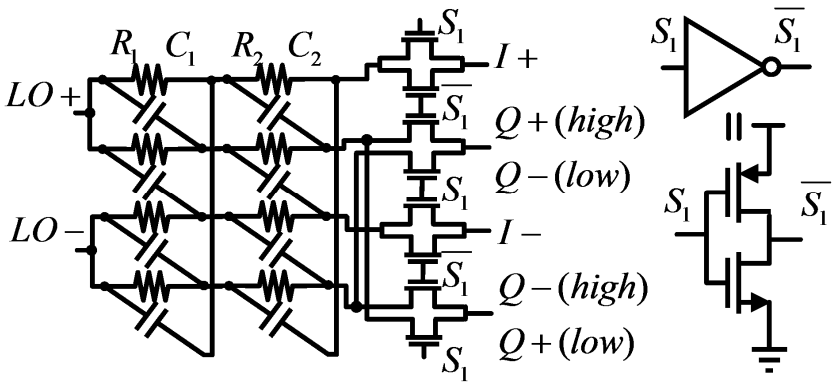


Fig. 5-15 LO1 quadrature signal generator with a two-stage PPF and NMOS switch pairs.

As shown in Fig. 5-15, two-stage PPFs generate differential- quadrature LO signals, including first- and second-stage LO signals, from differential inputs. Moreover, four NMOS switch pairs are employed at the outputs of the LO_1 generator [67]. If the control bit is high or low, 2.2-GHz or 4.8-GHz band is thus selected, respectively. LO_1 is set at the halfway point between two application bands (2.2 GHz and 4.8 GHz) to reuse the first-stage mixers (*i.e.*, LO_1 is around 3.5 GHz and thus LO_2 is around 1.27 GHz with IF_2 covering from 20 to 40 MHz). The frequency relations were introduced in Eqn. (5.2).

The single-quadrature Hartley system, after the transformer, consists of two Gilbert mixers and a three-stage PPF, while the following double-quadrature Hartley system has four mixers and a four-stage PPF. A three-stage inter-stage PPF has the ratio bandwidth of 1.4938 for a 60-dB IRR. A higher quality in quadrature input signals guarantees the maximum achievable IRR. On the other hand, the four-stage

IF_2 PPF is designed for an 80-dB IRR covering 20-40 MHz (ratio bandwidth=2).

The die photo of the dual-band low-IF downconverter is shown in Fig. 5-16, and the die size is 1.83×1.94 mm^2. The total power consumption is 95 mW at a 1.8-V supply. The conversion gain and single-sideband noise figure are shown in Fig. 5-17. The conversion gain is 14.2/12.7 dB with the in-band (20-40 MHz) noise figure of 6.2/7.2 dB at 2.2/4.8-GHz modes, respectively. Besides, flicker noise corner of the demonstrated CMOS receiver for both modes are around 5 MHz, which is away from our IF band.

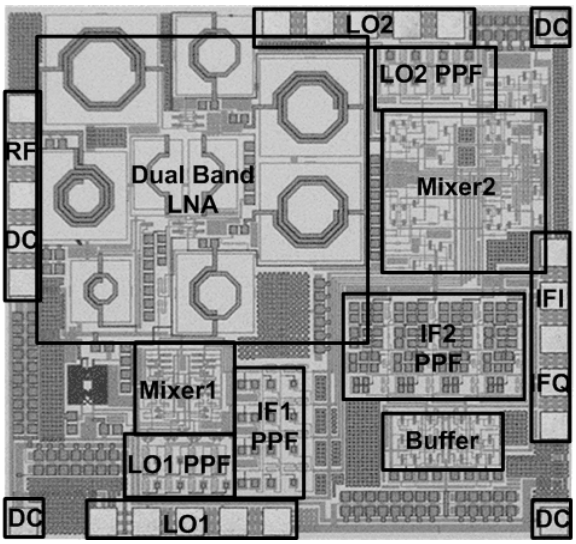


Fig. 5-16 Die photo.

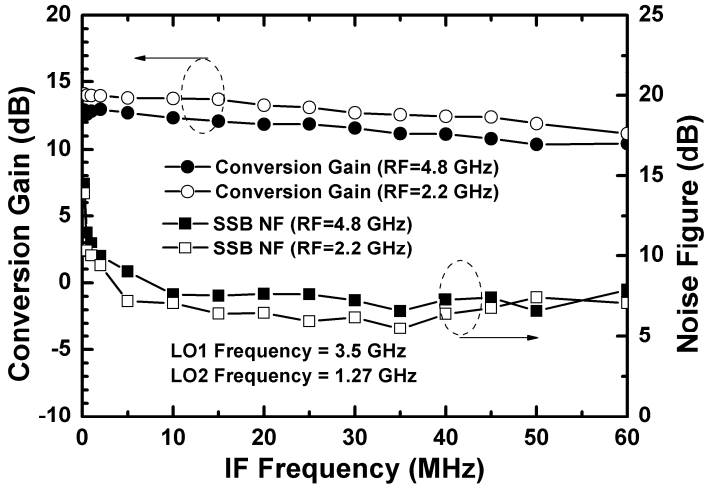


Fig. 5-17 Conversion gain and single-sideband noise figure.

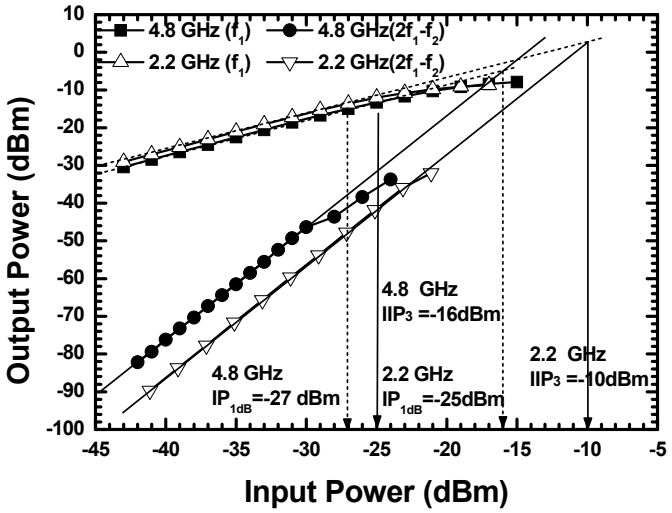


Fig. 5-18 Power performance.

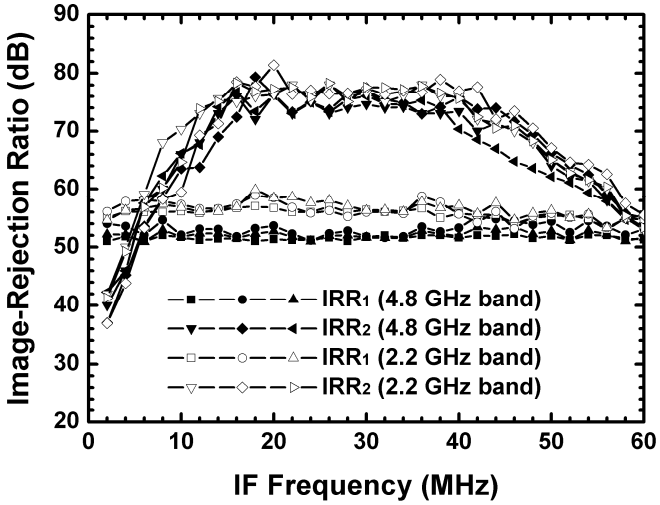


Fig. 5-19 IRR of the first/second image signals.

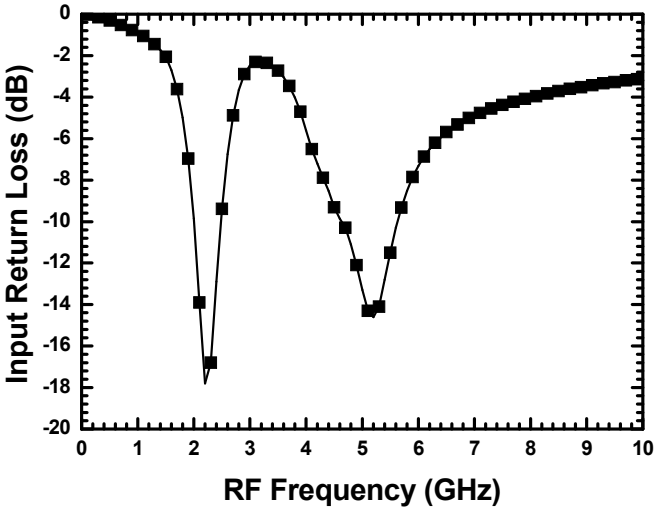


Fig. 5-20 Input return loss.

The IP_{1dB}/IIP_3 are −25/−10 dBm at 2.2-GHz mode while IP_{1dB}/IIP_3 become −27/−16 dBm at the 4.8-GHz mode when LO_1=3.5 GHz, LO_2=1.27 GHz, and IF_2=30 MHz, respectively, as shown in Fig. 5-18. Fig. 5-19 shows the IRR_1 and IRR_2 at 2.2/4.8-GHz modes from three samples. As shown in Fig. 5-19, the IRR_1 is on average about 56/52 dB at 2.2/4.8-GHz mode while the IRR_2 is about 77/74 dB. The LO_1/LO_2-to-RF isolation reaches 77/71 dB. The input return loss is better than 10 dB within 2-2.5 GHz and 4.6-5.7 GHz for both modes, as shown in Fig. 5-20. The overall measured performance is also summarized in TABLE. 5.1.

5.2.4 Comparisons and Conclusions

A double-quadrature system with the preceding PPF has much immunity of quadrature amplitude/phase mismatch and thus is preferred at both the first- and second-stage mixers to achieve excellent IRR at the cost of power consumption. Thus, a dual-conversion double- quadrature-double-quadrature low-IF downconverter with an input RF PPF and a dual-band dual-conversion single-quadrature-double-quadrature low-IF downconverter with an inter-stage PPF are demonstrated in this paper for a significant improvement in image rejection. A double-quadrature-double-quadrature downconverter with an RF PPF in our work achieves a 55-dB IRR_1. On the other hand, the IRR_1 of a single-quadrature-double-quadrature downconverter without an LNA is less than 45 dB as summarized in TABLE. 5.1. The dual-band single-quadrature- double-quadrature downconverter with an inserted inter-stage PPF in our work achieves 77/74 dB IRR_2 at 2.2/4.8-GHz and demonstrates the state-of-the-art IRR_2 in the literature as summarized in TABLE. 5.1. The proposed two architectures can almost reach the theoretical limit of the IF_2 PPF.

TABLE. 5.1 PERFORMANCE COMPARISONS OF DUAL-CONVERSION LOW-IF RECEIVERS

Reference		[56]		[62]	[65]	[67]		This Work A	This Work B	
Topology (SQ=single-quadrature DQ=double-quadrature)		Dual-band SQDQ Weaver		SQDQ Weaver	SQDQ Weaver-Hartley	Dual-band SQDQ Weaver-Hartley		DQDQ Weaver-Hartley	Dual-band SQDQ Weaver-Hartley	
Supply Voltage (V)		3		3.3	3.3	1.8		3.3	1.8	
Power Consumption (mW)		75		198 [a]	115.5	126 (mixer:25)		210 (mixer:105)	95	
Frequency (GHz)		0.9	1.8	1.9	2.4	2.4	5.7	5.2	2.2	4.8
Conversion Gain (dB)		23 (A_V)	23 (A_V)	26~78	20.3 (max)	9	8	10	14.2	12.7
Noise Figure (dB)		4.7	4.9	14(min)	7.2 (min)	23	25	18	6.2	7.2
IRR_1 (dB)	Rx	40	36	55	35	N.A.	N.A.	N.A.	56	52
	Rx w/o LNA	N.A.	N.A.	45	N.A.	40	40	55	49.5	37
IRR_2 (dB)		N.A. [b]	N.A. [b]	N.A. [b]	60 [c]	44	46	50	77	74
Technology		0.6-μm CMOS		0.6-μm CMOS	0.6-μm CMOS	0.18-μm CMOS		0.35-μm SiGe HBT	0.18-μm CMOS	

[a]Including ADC and baseband filter.

[b]IF_2=0.

[c]5-stage PPF and passive IF mixers.

Chapter 6 Low-Power Low-Noise Direct-Conversion Receiver

6.1 INTRODUCTION

Recently, direct-conversion receivers (DCRs) have been widely researched and implemented because their simpler structure results in a lower noise figure (NF) and lower power consumption than heterodyne and low-IF receivers [49]-[50], [71]. CMOS technology is commonly used for a fully integrated single-chip solution. A CMOS DCR has inherently serious flicker noise, whose noise spectral density is inverse proportional to frequency, and dc offset problems because the MOS device itself has very large flicker noise and mismatch [72]. An active Gilbert mixer suffers from a severe flicker noise problem because the flicker noise of the LO switching core directly leaks to the output at the zero-crossing, while the flicker noise of the RF stage is upconverted to the odd harmonics of the LO frequency [51]. The noise at IF output is proportional to the dc current through the switching core [51]. That is, $i_{o,n} = 4I/(S \times T) \cdot V_n$ where V_n is the gate-referred noise voltage of the switching pair, I is the tail dc current, S is the slope of voltage waveform at the zero-crossing, T is the period of LO, and $S \times T = 4\pi A_{LO}$ for a sine-wave LO of $A_{LO}\cos(\omega_{LO}t)$. As a result, there are several straightforward methods for flicker noise reduction:

1) Reduction of dc current I. A static/dynamic current injection methods were proposed [73]. On the other hand, a current-mode passive mixer has no dc current flowing through the switching core, and thus ideally no device flicker noise component will appear at the output [74]. However, unlike an active mixer, a passive mixer has no ability to reduce the noise figure of the following IF transimpedance amplifier (TIA) and variable-gain amplifier (VGA) and thus a

high-gain low-noise low-noise amplifier (LNA) is urgently required. With an advanced CMOS technology, for example, 90, 65 nm or even 45 nm CMOS process, ultra-low device NF_{min} and high cut-off frequency (f_T) results in a high-performance LNA and thus lessens the burden of the passive mixer. However, the R&D cost is incredibly high.

2) Increase of switching slope *S*. The use of cascaded inverters generates square-wave LO waveform to increase the slope at zero crossing.

3) Reduction of device flicker noise component V_n. Thus, an increase of the switching pair transistor size is a sufficient way because the gate-referred noise voltage can be expressed as $V_n^2 = K/(C_{ox} \cdot W \cdot L \cdot f)$. On the other hand, bipolar junction transistors (BJTs) have ultralow flicker noise, better device-to-device matching, and also larger transconductance (g_m) than MOS devices. Therefore, many RF transceiver chips have been fabricated using BiCMOS processes where the high performance SiGe HBT is used for the RF circuit and CMOS for the logic circuits [75]-[76]. However, the cost is high and access to the foundry process is quite limited. Continuous advances in CMOS technology provide both good RF circuits and digital VLSI at very low cost. A vertical-NPN (V-NPN) bipolar junction transistor (BJT), available in a standard low-cost deep-n-well 0.18-μm CMOS process with its low flicker noise and good device matching, is specially suitable for a DCR [77]-[78].

In this chapter, DCRs are implemented in a 0.18-μm CMOS process. Thus, every component should be carefully designed to achieve very low noise at a low power consumption. Section 6.2 describes the design concepts of the building blocks of a low-power receiver, including LNA, transformer, device characteristics of V-NPN BJTs and the IF VGA using V-NPN BJT g_m core. Then, 2.4 GHz narrow-band DCRs

are demonstrated using passive mixer (as performance reference) in Section 6.3. However, the low f_T of the V-NPN BJT actually brings up a big challenge to RF designers when applied to a mixer core. Thus, two main methods for low-f_T solutions are described in Section 6.4:

1) The BJT mixers operate at near or higher than the f_T but an inductive peaking is applied to alleviate the performance degradation. A 2.4-GHz DCR using V-NPN BJT switching core is implemented and discussed in Section 6.4.1.
2) Sub-harmonic mixing operation can directly avoid the low-f_T problem because the mixing operating frequency is only half of the RF frequency but the octet-phase LO signal generation needs to be more addressed. In Section 6.4.2, a 2.4-GHz sub-harmonic direct-conversion receiver (SH-DCR) is demonstrated and a low-loss well- balanced passive LO octet-phase poly-phase filter (PPF) is fully analyzed and employed.

Section 6.4.3 compares the performance of the three implementations in Sections 6.3 and 6.4. Further, a low-power low-noise SH-DCR covering the whole U-NII bands (5.15-5.825 GHz) is demonstrated with a tunable-band RF LNA and wideband LO octet-phase signal generator in Section 6.5.

6.2 LOW-POWER DESIGN OPTIMIZATION

The LNA plays an important role in a low-power, low-noise receiver design since the LNA must provide sufficient gain to suppress the noise figure (NF) of the whole receiver chain but itself add as little noise as possible. However, under power constraints, the design challenge is dramatically increased. Section 6.2.1 described a noise-impedance-matched LNA with the effect on lossy inductors at a power constraint. A transformer is used to generate differential RF voltage to mixer from the

single-ended current of the LNA. The optimal turn ratio of the inter-stage transformer is determined in Section 6.2.2 to provide a higher gain and also a lower noise. Besides, a V-NPN BJT in low-cost 0.18-μm CMOS technology can be used as a flicker-noise-free switching core of the mixer and a g_m cell of an IF amplifier due to its high g_m under a fixed current. Thus, the device characteristics of V-NPN BJTs are reported in Section 6.2.3. Section 6.2.4 describes an IF VGA using R-r attenuation method in both emitter and collector nodes.

6.2.1 Low-Noise Amplifier Design Optimization With On-Chip Inductors at a Fixed Power Consumption

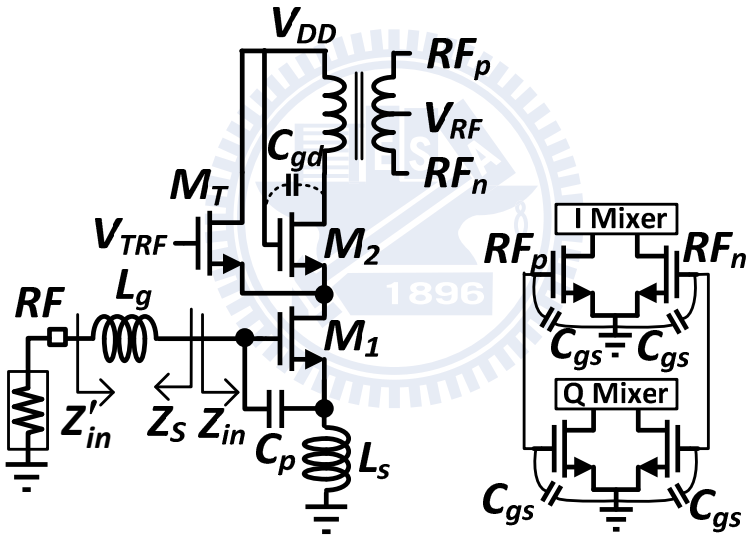


Fig. 6-1 Schematic of a cascode LNA with a single-to-differential transformer connecting to the transconductance stage of the following I/Q Gilbert mixers.

The schematic of a widely used cascode LNA with a source degeneration inductor (L_s) is shown in Fig. 6-1. The L_s is used to make the optimal noise impedance and input impedance almost equal. The cascode structure provide better reverse isolation than a common-source structure, avoiding the LO leakage leaking back to the RF input and even to the antenna.

At a high operating frequency, the intrinsic device NF_{min} and f_T are not good

enough due to the technology limitation. Besides, the matching inductor L_g (and its accompanying series resistance R_{Lg}) is relatively small as will be shown in Egn. (6.5). In this case, the intrinsic device NF_{min} dominates the overall LNA NF, not the extrinsic thermal noise of the series resistance R_{Lg}. A higher current density results in a better performance at the cost of high dc power consumption. However, over 200 μA/μm J_D, the mobility degradation occurs and results in lower g_m and thus lower f_T and also the increase of NF_{min}. As a result, for a well-known high-frequency CMOS LNA design, a device with approximately 150-μA/μm current density (J_D) is generally used for a minimum NF and high f_T, and thus, a maximum gain [79]. Note that using an advanced technology can lead to better NF_{min}, f_T, and also less power consumption at a higher cost.

At a low operating frequency, the intrinsic device NF_{min}, f_T and the resulting gain are sufficiently good, and thus, a power-constrained noise optimization design (PCNO), proposed by Shaeffer and Lee [80], is more practical for a low-power design. However, a small device size with a high J_D results in an incredibly large L_g. The extrinsic thermal noise of R_{Lg} instead of the intrinsic device NF_{min} dominates the overall NF and there exists an optimal device size for the best noise performance [81]. Recently, Nguyen *et al.* proposed a power-constrained simultaneous noise and input matching (PCSNIM) by adding a parallel capacitance C_p in Fig. 6-1 for LNA design. The NF of the resulting LNA approaches the intrinsic device NF_{min} and impedance matching is achieved at the same time for every transistor size at a fixed I_D when wire-bonding is employed for L_g and thus the R_{Lg} is negligible [82]. There is no discussion on the effect of lossy matched inductor for PCSNIM in this literature yet. Here, the effect of R_{Lg} is discussed and the benefit of the parallel C_p for a significant reduction of extrinsic thermal noise of R_{Lg} is highlighted by clear and detailed graphic

analysis. There also exists an optimal device size for the best NF and the resulting NF is better than the NF obtained by PCNO method [81].

A. SNIM Method

The simultaneous noise and input matching (SNIM) is achieved by adopting a reactive degeneration inductor L_s. The input impedance and noise matching are discussed as follows.

1) Input Matching with the Effect of Low-Q Inductors

The input impedance of a cascode LNA, shown in Fig. 6-1, can be expressed as

$$Z'_{in} = (sL_g + R_{Lg}) + (sL_s + R_{Ls}) + 1/sC_t + g_m (sL_s + R_{Ls})/(sC_t) \qquad (6.1)$$

where R_{Lg}/R_{Ls} represent the series resistance of the inductance L_g/L_s. Typically, R_{Ls} is much smaller than R_{Lg} and can be neglected. $C_t = C_{gs} + C_p$ when a parallel capacitance C_p is applied.

Since an on-chip planar inductor can be modeled as an inductor L in series with a resistor R when the operating frequency is lower than $f_{Qmax.}$ Here, Q_L of an inductor is defined as $\omega_0 L/R$. Generally speaking, the series resistance is proportional to the geometric length and thus proportional to the series inductance. That is, $R = (\omega_0/Q)L \equiv \alpha_0 L$, where α_0 is close to a constant, only relating to the geometrical shape (including metal width, spacing and metal thickness). Thus, the Z'_{in} in (1) can be modified as

$$Z'_{in} = \left[\alpha_0 (L_g + L_s) + g_m L_s / C_t\right] + \left[s(L_g + L_s) + (1 + g_m \alpha_0 L_s)/sC_t\right]. \qquad (6.2)$$

To achieve impedance matching at a target resonance frequency (ω_0) and the target matching impedance R_S=50Ω when the device size (C_{gs}) (or C_t) and bias (g_m) are decided,

$$\begin{cases} R'_{in} = \alpha_0 (L_g + L_s) + g_m L_s / C_t = R_S \\ \dfrac{1 + g_m \alpha_0 L_s}{(L_g + L_s) C_t} = \omega_0^2 \end{cases} . \tag{6.3}$$

Thus,

$$L_s = \frac{R_S C_t}{g_m} \left(1 - \frac{\alpha_0}{\omega_0^2 C_t R_S}\right) \Bigg/ \left[1 + \left(\frac{\alpha_0}{\omega_0}\right)^2\right] \tag{6.4}$$

and

$$L_g = \frac{1 + g_m \alpha_0 L_s}{\omega_0^2 C_t} - L_s . \tag{6.5}$$

Note that, if no series resistance R_{Lg} is considered (*i.e.*, α_0=0), the well-known results for impedance matching are $L_s = R_S C_t / g_m$ and $L_g = 1/(\omega_0^2 C_t) - L_s$.

Besides, the transconductance gain of the input transistor M_1 at resonance can be expressed as

$$\left|G_m(\omega_0)\right| = \frac{1}{R_S} \frac{g_m}{\omega_0 C_t} = \frac{g_m \cdot Q_S}{1 + g_m R_{Ls}} \approx g_m \cdot Q_S . \tag{6.6}$$

where $Q_S = \omega_0 (L_g + L_s) / R_S = (1 + g_m R_{Ls}) / (\omega_0 C_t R_S)$ is the quality factor of the input impedance. Note that, $|G_m(\omega_0)|$ can be expressed as $1/(\omega_0 L_s)$ when α_0=0 [83]. In other words, a smaller L_s results in a higher gain.

2) Noise Matching

In this part, we consider the equations for the lossless matching condition (without R_{Lg}) because the mathematical expressions will be complicated and the insight is lost when considering the effect of lossy inductors. Later in the following sections, a graphical analysis is adopted for a clear view of the noise optimization.

The general formula of the optimal noise impedance (Z_{opt}) of the common-source configuration with L_s and a parallel capacitance C_p can be expressed as

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} + j(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}})}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \quad , \tag{6.7}$$

where $\alpha=g_m/g_{d0}$, γ is a constant for the channel thermal noise current, δ is a constant for the gate induced noise current, and c is a correlation coefficient of the gate-induced noise current and the channel noise current [82], [84]. If no C_p is applied, an optimal device size (or C_{gs}) can be determined by fulfilling $\mathrm{Re}\{Z_{opt}\}=\mathrm{Re}\{Z_S\}$ by setting $C_t=C_{gs}$ in Eqn. (6.7). Then, the size of L_s is determined by $\mathrm{Im}\{Z_{opt}\}=-\mathrm{Im}\{Z_S\}$. For the given values C_{gs} and L_s, the value of V_{gs} (or the dc current consumption I_D) can then be determined from $\mathrm{Re}\{Z_{in}\}=\mathrm{Re}\{Z_S\}$. Thus, under lossless matching condition, the minimum noise factor (F_{min}) can be expressed as

$$F_{\min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{r\delta(1-|c|^2)} \, . \tag{6.8}$$

B. PCNO Method with the Effect of Low-Q Inductors

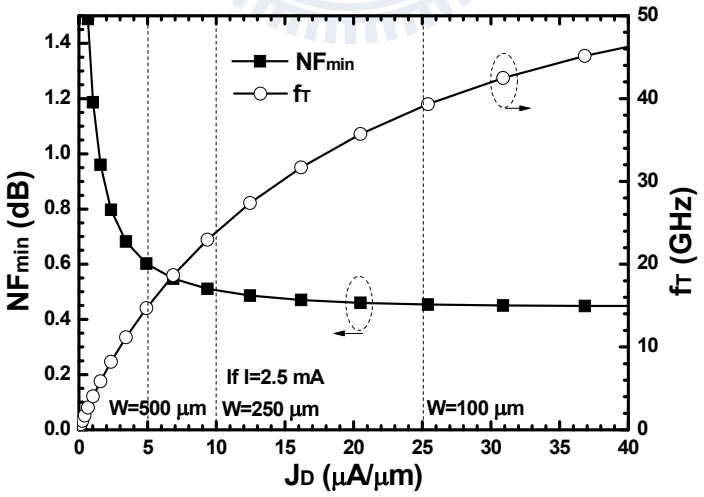


Fig. 6-2 Simulated device minimum noise figure (NF_{min}) at 2.4 GHz and cut-off frequency (f_T) of a 0.18-μm RF NMOS as a function of current density ($J_D=I_D/W$).

When the operating frequency is low (such as 2.4 GHz in this paper), the optimal transistor size is very large because $\mathrm{Re}\{Z_{opt}\}$ is inverse proportional to ωC_{gs} by Eqn.

(6.7). Thus, the F_{min} can only be reached at a high I_D. Fig. 6-2 shows the simulated NF_{min} at 2.4 GHz and f_T of a single RF NMOS device (W/L=240μm/0.18μm). Thus, if the I_D is fixed, a larger transistor size (*i.e.*, a lower J_D) results in a lower f_T and a higher NF_{min}. It reveals that even though a perfect noise matching is achieved using a large device, the NF may be even higher than the NF using a small device because of the limited f_T and the higher device NF_{min} at a fixed I_D.

As a result, the PCNO method [80] is preferred to achieve a sub-optimal $NF_{min,P}$ at a fixed dc current criterion I_D. The I_D is set by the requirements on gain, NF and linearity of the LNA. However, $NF_{min,P} \geq NF_{min}$ because of the mismatch between Z_S and Z_{opt}. Eventually, $NF_{min,P}$ tends to approach NF_{min} as the I_D increases.

Here, a cascode LNA with a parallel *RLC* resonance load (=400 Ω at resonance) as shown in Fig. 6-1 is simulated for different transistor size (W_1) of M_1, series inductance L_g/L_s and C_p, while the gate width (W_2) of M_2 is 240 μm and the *RLC* tank is resonated at 2.4 GHz. All of the device gate lengths are kept at 0.18 μm. The device model is BSIM3v3.24 provided by the foundry. Here, α_0=0, 1, and 2 Ω/nH are simulated for both L_g and L_s and the corresponding $Q_L=\omega_0/\alpha_0=\infty$, 15, and 7.5 at 2.4 GHz. α_0=2 Ω/nH is especially addressed because it is the typical value of an on-chip spiral inductor using ultra-thick metal (UTM) and metal width is 6 μm while the f_{Qmax} is still higher than the operating frequency.

Following the PCNO concept, Fig. 6-3(a) shows the required L_g and L_s of the LNA while the I_D is fixed at 2.5 mA. The corresponding NF and A_V of the LNA are indicated in Fig. 6-3(b) and (c), respectively. The L_s should be smaller when a larger α_0 is applied, as shown in Fig. 6-3(a) and can also predicted in Eqn. (6.4). Note that, the difference in L_s due to different α_0 is less than 0.4 nH. L_g is typically the same for different α_0, because C_{gs} remains the same and L_g is much larger than L_s. As

mentioned above, the NF (α_0=0) of a large device is higher than that the NF of a small device at a fixed I_D, The $NF_{min,P}$ of a cascode LNA has the same trend of a pure device.

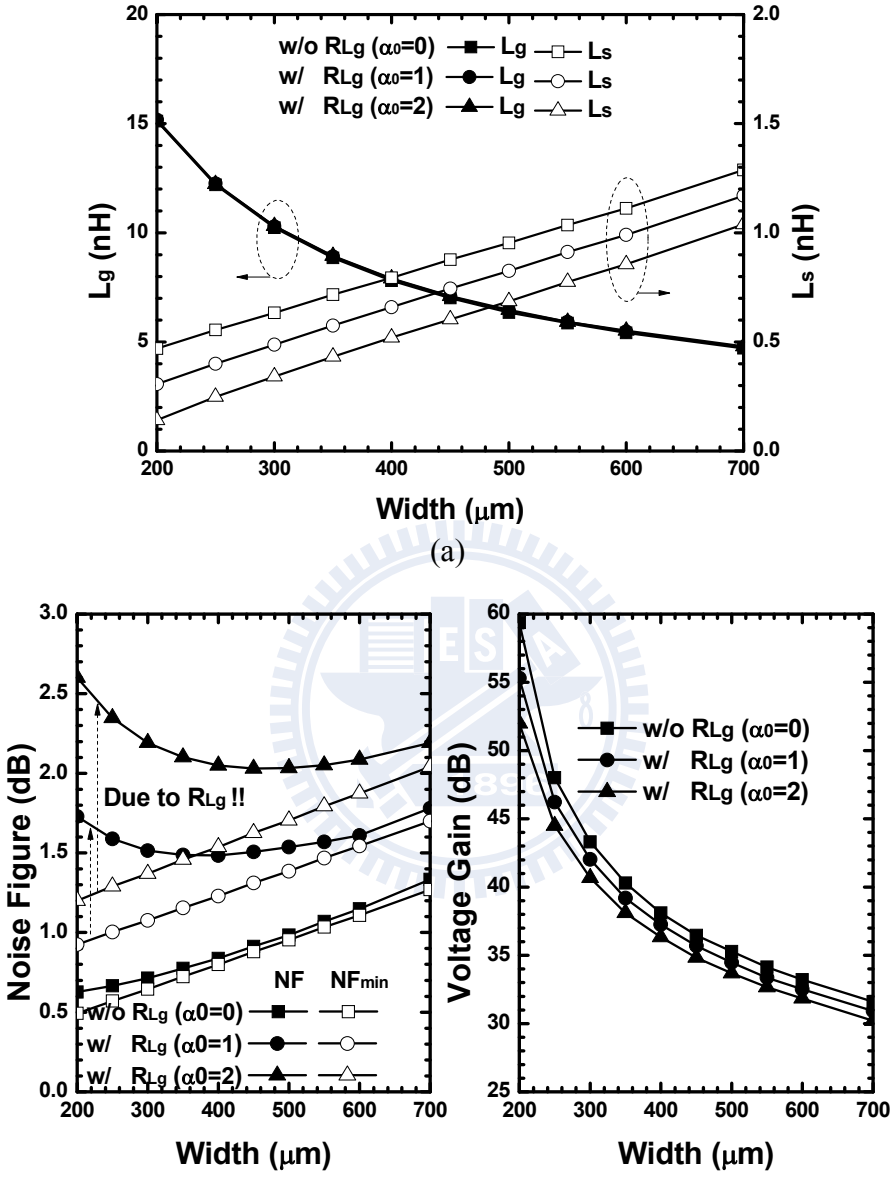


Fig. 6-3 (a) L_g and L_s for power-constrained noise optimization at 2.4 GHz and the corresponding. The required L_g for different α0 is very similar due to the same C_{gs} and a small L_s (b) noise figure and (c) voltage gain of the cascode LNA without C_p while the supply current is 2.5 mA. The unit for α_0 is Ω/nH.

In this case, a smaller device with lower device NF_{min} and higher f_T is preferable except for the input matching bandwidth because the input impedance matching

bandwidth $\Delta f_{10\ \mathrm{dB}}$ (for $|S_{11}|<-10$ dB) is $\omega_0/(6\pi Q_{in})$, where $Q_{in}=\omega_0(L_g+L_s)/(R'_{in}+R_S)$ $=Q_S/2$ in this paper because $R'_{in}=R_S$ is designed [85]. However, when considering the extrinsic R_{Lg} (i.e., $\alpha_0\neq 0$), the noise factor (F) has one additional term of $(R_{Lg}+R_{Ls})/R_S$ when compared to the F ($\alpha_0=0$) [81], *i.e.*,

$$F \approx 1+\frac{R_{Lg}+R_{Ls}}{R_S}+\left[\begin{array}{l}\gamma g_{d0}R_S\left(\frac{\omega_0}{\omega_T}\right)^2\left(1+\frac{\delta\alpha^2}{5\gamma}\right)\\ \quad +2|c|\left(\frac{\omega_0}{\omega_T}\right)\sqrt{\frac{\delta\gamma}{5}}+\frac{\delta}{5g_{d0}R_S}\end{array}\right]. \tag{6.9}$$

Therefore, the series resistances of on-chip low-Q inductors make the NF increase dramatically and even dominate the overall NF. As shown in Fig. 6-3(b), the phenomenon is serious especially when a small device is chosen or at a low operating frequency because the required large L_g accompanies enormously large R_{Lg}. That is, the NF optimization suffers from severe trade-offs between the thermal noise of extrinsic R_{Lg} and the intrinsic device NF_{min}. For an extreme case, a series on-chip low-Q inductor may directly used for lossy impedance matching without the need of L_s. However, the NF is always larger than 3 dB, theoretically, because of the 50-Ω input series resistor [86]. For the case of $\alpha_0=2$ Ω/nH, the minimum achievable NF is around 2.03 dB with 450-μm W_1 (*i.e.*, $J_D=5.6$ μA/μm) although the NF is still higher than the NF_{min}.

Note that, a smaller α_0 always leads to a lower NF. Thus, external wire-bonding and off-chip matching network are sometimes employed for input matching [80], [82] because of the very low series resistance in an inductor (*i.e.*, $\alpha\rightarrow 0$). However, these have significant percentage error and are time-consuming and difficult to mass produce. On the other hand, for an on-chip low-Q inductor, a wider line width results in a smaller series resistance (*i.e.*, a smaller α_0) but a lower f_{Qmax}. If the f_{Qmax} is near or

even lower than the operating frequency, the simple inductor model (R=$\alpha_0 L$) fails and the overall NF of the LNA increases, too. Thus, the passive component layout optimization is required for a sufficiently low α_0.

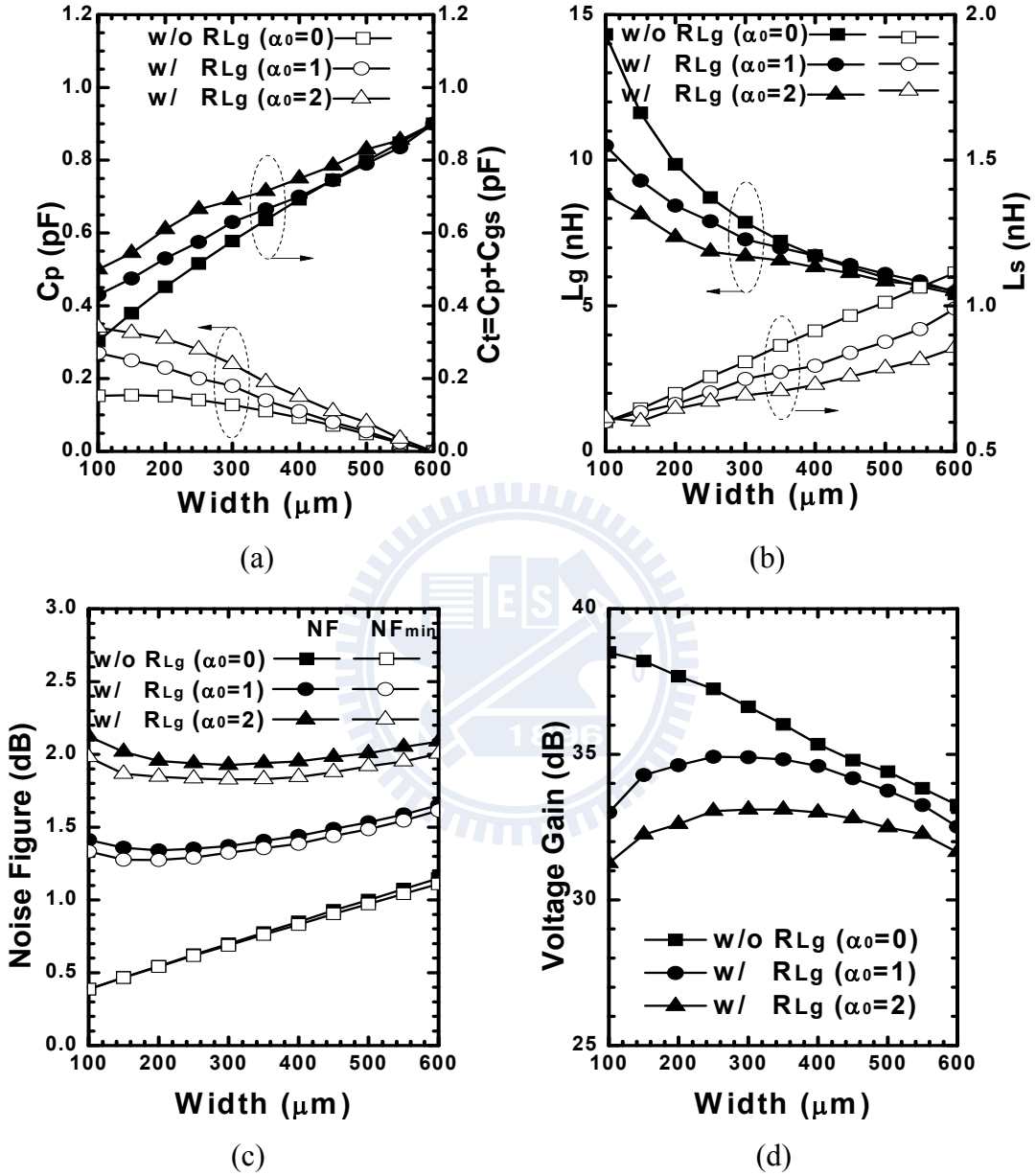


Fig. 6-4 (a) C_p (b) L_g and L_s for power-constrained simultaneous noise and impedance matching at 2.4 GHz and the corresponding (c) noise figure and (d) voltage gain of the cascode LNA with C_p while the supply current is 2.5 mA. The unit for α_0 is Ω/nH.

C. PCSNIM Method with the Effect of Low-Q Inductors

For the PCSNIM method in reference [82], a C_p is applied to modify the Re$\{Z_{opt}\}$ without changing the NF_{min} described by Eqn. (6.8) and makes the noise and

impedance matching achieved at the same time for every transistor size at a fixed I_D when R_{Lg} is negligible. A graphical method is employed here for the PCSNIM method with the effect of low-Q inductors.

Fig. 6-4 shows the simulation results of the cascode LNA w/ C_p following a PCSNIM method while I_D=2.5 mA. The C_p chosen for optimal noise performance and the C_t=C_{gs}+C_p are drawn in Fig. 6-4(a). However, no C_p is required to achieve noise matching when W_1 is larger than 600 μm. The corresponding L_s and L_g are drawn in Fig. 6-4(b). Fig. 6-4(c) and (d) show the corresponding achievable NF and A_V (voltage gain), respectively. The line with square symbols in Fig. 6-4(c) clearly shows the results using PCSNIM but without R_{Lg}. When considering low-Q (high-α_0) inductors, a higher α_0 of an inductor requires a larger C_p to reduce the required L_g and the corresponding R_{Lg} for an optimal overall NF, as shown in Fig. 6-4(a) and Fig. 6-4(b). This advantage is much more significant than the reduction of the device noise. As a result, when considering the R_{Lg}, the minimum achievable NF w/ C_p [in Fig. 6-4(b)] is lower than the NF w/o C_p [in Fig. 6-3(b)] for a given α_0. Note that, when $\alpha_0 \neq 0$, the A_V using PCNO decreases progressively when W_1 increases as shown in Fig. 6-3(c). However, when using PCSNIM with low-Q inductors, the applied C_p degrades the overall G_m of the LNA as shown in Eqn. (6.6) while the device NF_{min} remains the same especially for a small transistor size. Thus, not only the NF but also A_V has an optimal device size when R_{Lg} is considered. Besides, the optimal width increases if a larger α_0 is applied as shown in Fig. 6-4(c) and Fig. 6-4(d). As a result, the C_p for minimum achievable NF is around 0.2~0.3 pF when α_0=2 Ω/nH. The corresponding L_g is around 6~7 nH, which is implementable and occupies a small die area. The minimum NF is below 2 dB and A_V is above 33 dB when W_1 ranges from 200 to 400 μm (J_D=6.5~12.5 μA/μm).

Further, if the matching condition is not limited to a perfect 50 Ω, a smaller chosen of matching impedance R_S is selected, the A_V also increases, as predicted in Eqn. (6.6) and NF slightly decreases due to the smaller R_{Lg} at the cost of the matching bandwidth. Thus, changing the matched impedance to around 35~40 Ω by decreasing the L_s results in a higher A_V, a lower NF and allowable matching bandwidth. Finally, the W_1=240 μm (4-μm unit width×60 fingers) is chosen to achieve both optimal NF and A_V.

6.2.2 Inter-Stage Transformer Design Optimization

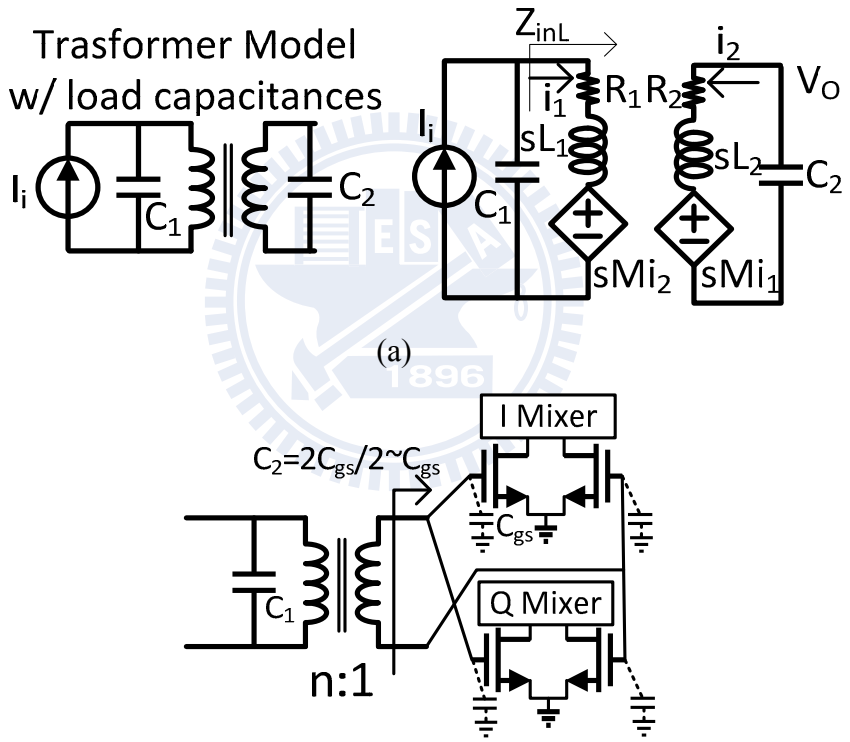
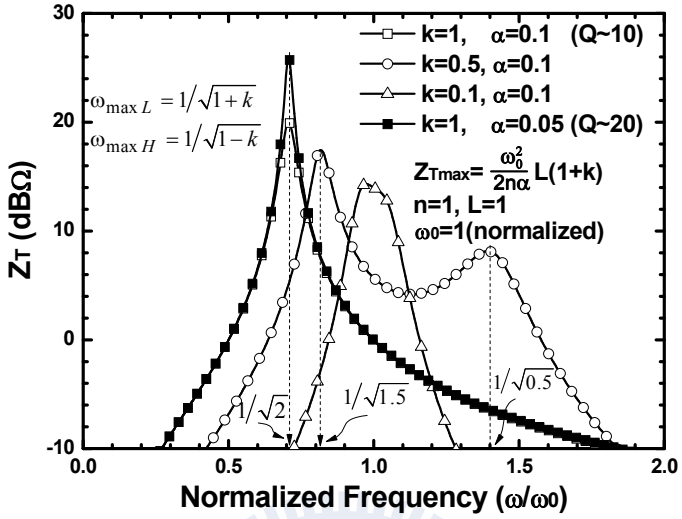


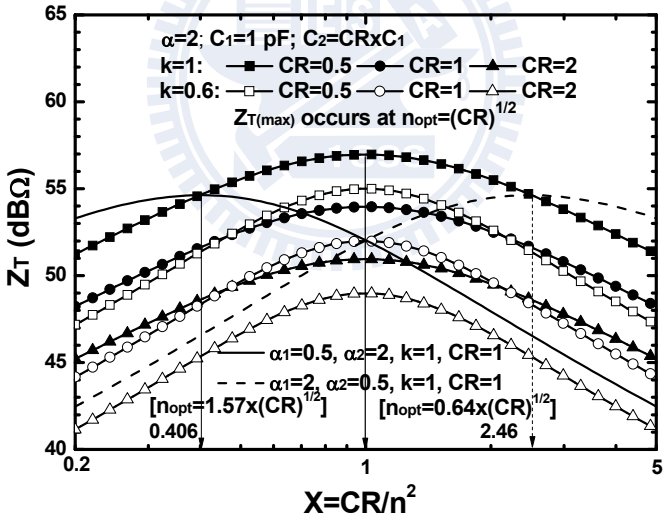
Fig. 6-5 (a) Transformer model with a capacitance load C_1/C_2 at the primary/secondary coil, respectively (b) schematic of the LNA transformer with an input varactor and output pure capacitance load.

The load of an LNA is a transformer to generate differential output signals. An n:1 transformer model is illustrated in Fig. 6-5(a) with the turn ratio $n = \sqrt{L_1/L_2}$,

coupling coefficient $k = M/\sqrt{L_1 L_2}$ and mutual inductance M. Similar to an inductor, the series resistance of each coil is assumed to be proportional to the series inductance. That is, $R_i = (\omega/Q_i)L_i \equiv \alpha_i L_i$, i=1, 2. where α_i is close to a constant.



(a)



(b)

Fig. 6-6 (a) Transimpedance gain (Z_T) of a transformer as a function of frequency (b) Z_T at a target frequency with respect to $X=n^2/CR$ for different input/output loading capacitance.

Here, we focus on the situation of pure capacitive load, which is especially suitable for an active mixer load. C_1/C_2 consists of the loading capacitance C_{in}/C_{out} and the intrinsic parasitic capacitance C_{p1}/C_{p2} of the transformer at each input/output node. The transimpedance gain (Z_T) is specifically considered because the output

current of the cascode LNA is fed to the transformer and then the differential output voltage is directly transferred to the transconductance (g_m) stage of the following active mixer, as indicated in Fig. 6-5(b).

Following the lumped model in Fig. 4(a), the Z_T can be expressed as

$$Z_T(s) = \frac{sM}{(1+sR_1C_1+s^2L_1C_1)(1+sR_2C_2+s^2L_2C_2)-s^4M^2C_1C_2}, \qquad (6.10)$$

which is derived in Appendix A.

Fig. 6-6(a) shows the frequency response of Z_T in a normalized frequency condition. As shown in Fig. 6-6(a), the Z_T usually has two peak frequencies $\omega_{maxL}=\omega_0/\sqrt{1+k}$ and $\omega_{maxH}=\omega_0/\sqrt{1-k}$, where $\omega_0 = 1/\sqrt{L_1C_1}$ when the Q of the transformer is high. The mathematical derivation is also summarized in Appendix A. However, because the ω_{maxH} tends to infinity for high coupling conditions and is not suitable for real applications. Thus, ω_{maxL} is typically chosen. In addition, the optimal turn ratio $n_{opt}=\sqrt{CR}=\sqrt{C_2/C_1}$ is obtained after a thorough derivation in Appendix A, if $\alpha_1=\alpha_2=\alpha_0$ (which is true for the two coils on the same layer with the same line with). Fig. 6-6(b) shows the Z_T at a target frequency with respect to $X=CR/n^2$ for different input/output loading capacitance. The peak gain occurs at X=1, as predicted. When $n=\sqrt{CR}$, *i.e.*, $L_1C_1=L_2C_2=1/\omega_0^2$, the peak gain $|Z_T(\omega_{maxL})|$ may be simplified as

$$|Z_T| = \frac{\omega^2 L_1}{2n\alpha_0}(1+k)^2 = Q\frac{\omega L_1}{2n}(1+k)^2 = \frac{\omega_0^2 L_1}{2n\alpha_0}(1+k). \qquad (6.11)$$

The reason is also indicated in Appendix A. It is noteworthy that if $\alpha_1\neq\alpha_2$, which is true especially for a stacked transformer using two layers, n_{opt} shifts. Fig. 6-6(b) also shows that n_{opt} increases if $\alpha_1<\alpha_2$, and vice versa. However, the case of $\alpha_1=\alpha_2$ is suitable in this chapter.

6.2.3 Device Characteristics of Vertical-NPN BJTs

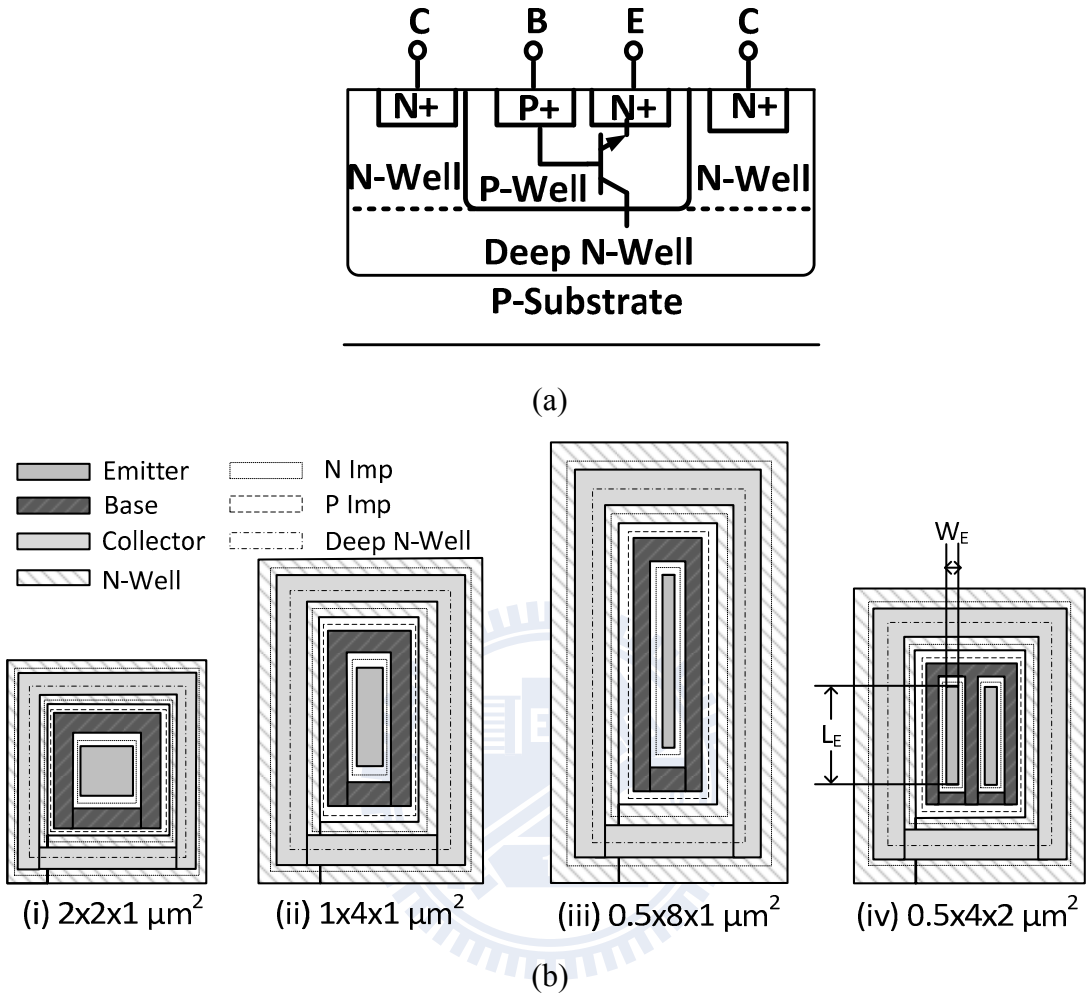


Fig. 6-7 (a) Cross-section view of the vertical-NPN (V-NPN) BJT in deep n-well 0.18-μm COMS process (b) layout of the V-NPN BJTs with four shapes but the same emitter area of 4 μm^2.

Nowadays, most of the state-of-the-art CMOS foundries provide a deep n-well technology, which can provide excellent isolation against the substrate coupling noise among and between digital baseband logic circuits and RF circuits. Besides, the V-NPN BJT can be obtained without extra cost from this deep n-well CMOS technology [77]-[78]. The V-NPN BJT is composed of the source-drain diffusion as the emitter, the p-well diffusion as the base, and the deep n-well as the collector as shown in Fig. 6-7(a).

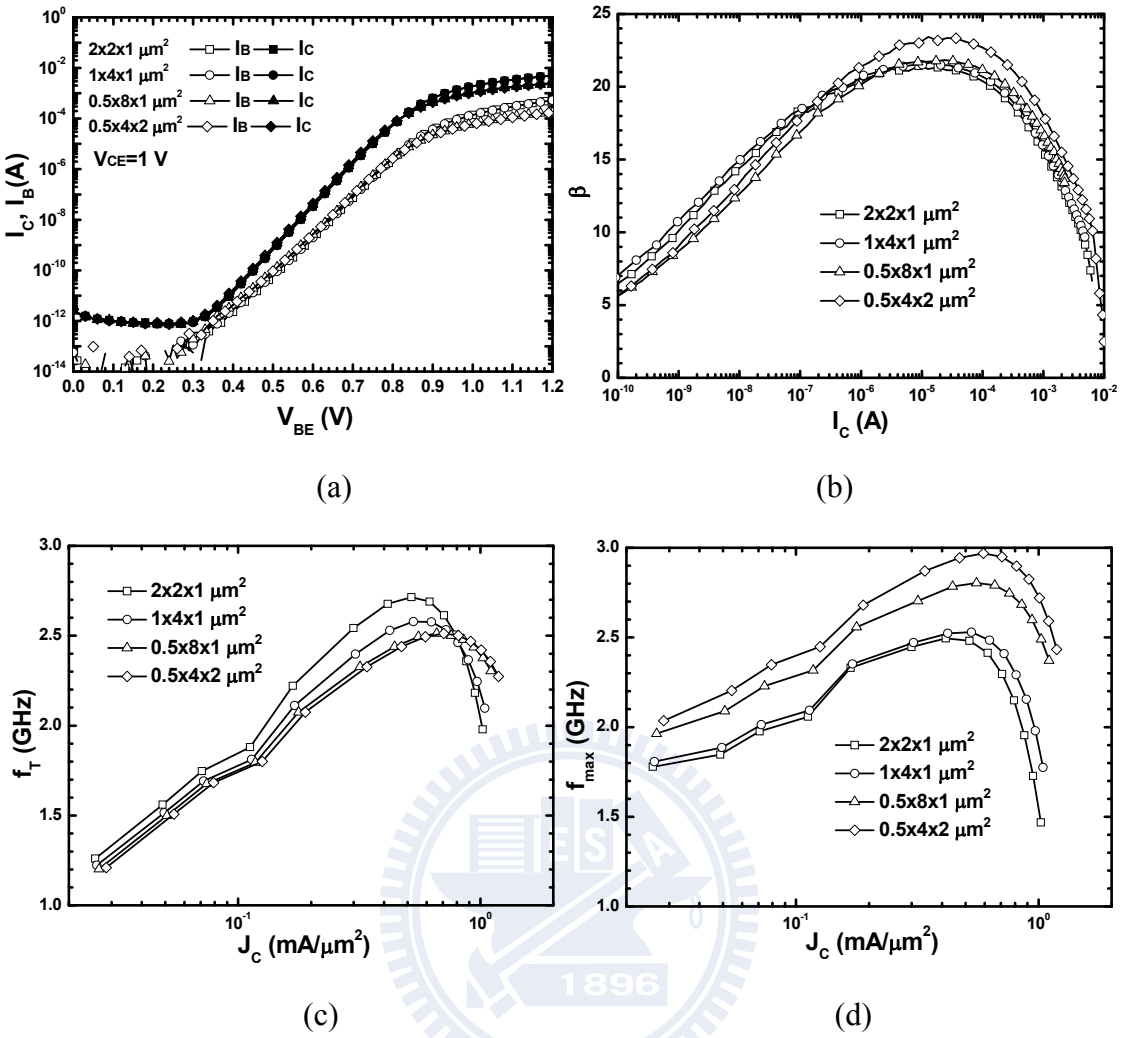


Fig. 6-8 (a) Gummel plot (b) current gain (c) current cut-off frequency (d) maximum oscillation frequency of the V-NPN BJT with four shapes but the same emitter area of 4 μm^2.

A deep-n-well V-NPN BJT provides not only lower collector resistance but also thinner p-base thickness, both of which can lead to good BJT performance. Moreover, a V-NPN BJT has much better uniformity, reproducibility, device matching, driving capability, and more ideal BJT characteristics than the lateral form [78]. Fig. 6-7(b) shows the layout of four devices with identical emitter areas of 4 μm^2: (i) $W_E \times L_E \times n = 2 \times 2 \times 1$ μm^2 (ii) $W_E \times L_E \times n = 1 \times 4 \times 1$ μm^2 (iii) $W_E \times L_E \times n = 0.5 \times 8 \times 1$ μm^2 and (iv) $W_E \times L_E \times n = 0.5 \times 4 \times 2$ μm^2, where W_E, L_E, and n represent the emitter stripe width, emitter length, and number of emitter fingers, respectively. The measurement results are compared in Fig. 6-8.

The Gummel plot is shown in Fig. 6-8(a) while the current gain (β) is displayed in Fig. 6-8(b). β reaches 20 for a wide range of I_C from 1 to 100 μA. The f_T and maximum oscillation frequency (f_{max}) of the four devices obtained from S parameter measurements are drawn in Fig. 6-8(c) and (d), respectively. Fig. 6-8(c) indicates that the four devices with different layout shapes have similar f_T because of the same base thickness. On the other hand, $f_{\max} \approx \sqrt{f_T/(8\pi R_B C_C)}$ where $R_B=r_0$W/L, $C_C=C_0$WL, r_0 and C_0 are the intrinsic base resistance and collector capacitance per unit area. Thus, $f_{\max}$ can be re-written as

$$f_{\max} \approx \frac{1}{2W}\sqrt{\frac{f_T}{2\pi r_0 C_0}}, \tag{6.12}$$

which indicates the importance of emitter stripe width on $f_{\max}$ [87]. Thus, a V-NPN BJT with a rectangular emitter shape has a higher f_{max} than a V-NPN BJT with a square emitter as shown in Fig. 6-8(d). Here, R_B (or f_{max}) is noted in this paper because it affects the LO power loss, which will be described later.

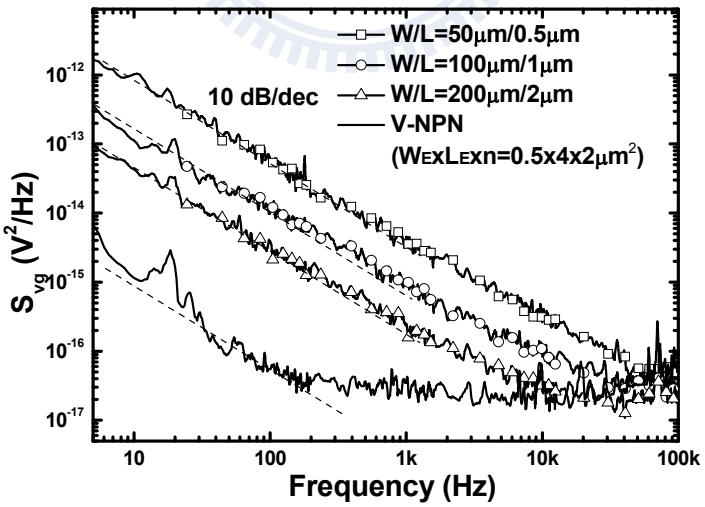


Fig. 6-9 Output noise current spectral density of V-NPN BJT and MOS devices. The dc current is 250 μA for the devices.

Fig. 6-9 shows the device input-referred noise voltage spectral density, measured by an Agilent 35670A dynamic signal analyzer, for PMOS devices [(i) W/L=

50μm/0.5μm (ii) 100μm/1μm (iii) 200μm/2μm] and V-NPN BJT with $W_E \times L_E \times n = 0.5 \times 4 \times 2\ \mu m^2$. The flicker noise corner ranges from 10 kHz to 100 kHz for (i)/(ii)/(iii) devices and a wider gate width leads to a lower flicker noise corner. By contrast, the V-NPN BJT has only around 200-Hz flicker noise corner, while the advanced 0.18-μm NMOS device has around several-MHz corner frequency under the same dc current of 250 μA.

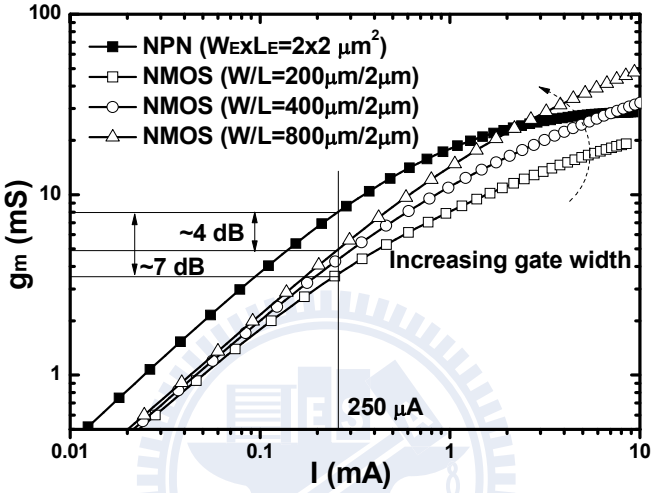


Fig. 6-10 Simulated g_m as a function of drain/collector current of both V-NPN BJT/NMOS transistors.

Besides, Fig. 6-10 shows the simulated g_m with respect to the drain/collector current of the NMOS/BJT transistors. A wider gate width results in a larger g_m at a fixed drain current since $g_m = \sqrt{2I\mu_n C_{ox}\frac{W}{L}}$. Besides, as illustrated in Fig. 6-10, the BJT-based g_m ($=I/V_T$) is larger than the g_m of the NMOS transistor ($2I/V_{OV}$), where V_{OV} is the gate overdrive voltage. Due to the parasitic emitter resistance R_E, the equivalent transconductance should be modified as $g_m/(1+g_m \times R_E)$. As a result, at the low-current operation, the transconductance is still near $I/V_T \propto I$, but at the high-current operation, g_m saturates to the limit of $1/R_E$. Thus, the g_m of the parasitic V-NPN may be even less than that of the NMOS transistor. However, the V-NPN is very suitable for the low-current operation.

6.2.4 *Variable-Gain Amplifier With Linear-in-dB Tuning Scheme*

V-NPN BJTs are also used at the input g_m stage of the IF amplifier to eliminate the flicker noise problem. Besides, the g_m of a BJT transistor is much larger than that of a MOS transistor for the same bias current. Thus, the voltage gain of the VGA is improved using V-NPN BJTs. Conventionally, the quasi-exponential function was realized by an *R-r* attenuation load with a combination of the constant resistance *R* of the rigid resistance and the variable resistance *r* implemented by a MOS transistor in the triode region as shown in Fig. 6-11 [88]-[89]. The impedance of the *R-r* attenuator can be expressed as $R/(1+R\times g_{ds})$, and has an approximate exponential characteristic in a certain region [88]. It is well known that g_{ds} is proportional to V_{OV} ($=V_{gs}-V_T$) in the triode region. Thus, we can control the impedance of the attenuation load with the *R-r* exponential function. The *R-r* attenuation load is typically implemented at the load of the VGA. However, the output 1-dB compression point (OP_{1dB}) degrades in low-gain mode due to the limited input linear range, especially for a BJT input g_m cell. Therefore, both loading and emitter *R-r* attenuators are applied to maintain the OP_{1dB} of the VGA, especially in low-gain mode. The equivalent two-section *R-r* attenuation results in a wider linear-in-dB tuning range (~20 dB) while typically a one-section *R-r* attenuator has a linear-in-dB tuning region of 10 dB approximately.

The schematic of the VGA with both loading/emitter *R-r* attenuators is shown in Fig. 6-11. A PMOS is employed at the drain node and an NMOS is chosen for the emitter degeneration. The drain-source resistance ($R_{ds}=1/g_{ds}$) of the NMOS/PMOS transistor in the triode region decreases/increases as the IF tuning voltage, V_{TIF}, increases. Thus, the voltage gain has a positive gain slope with respect to the V_{TIF}.

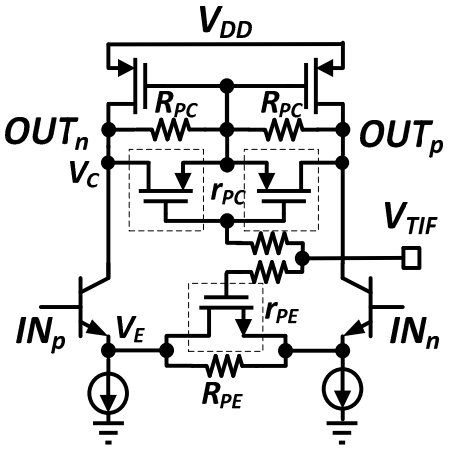
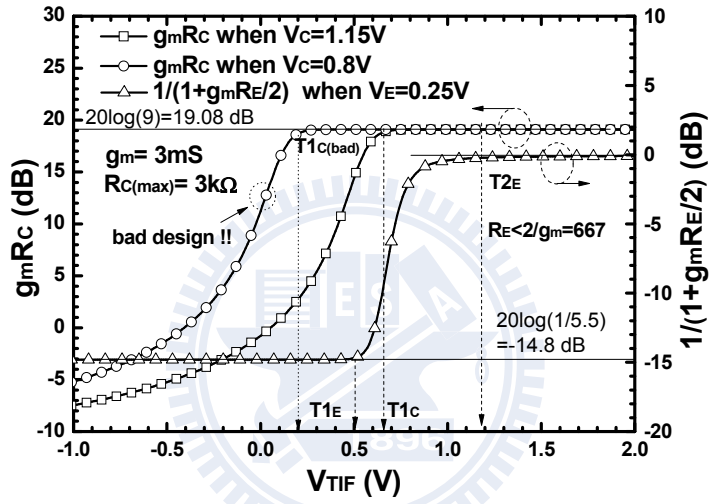
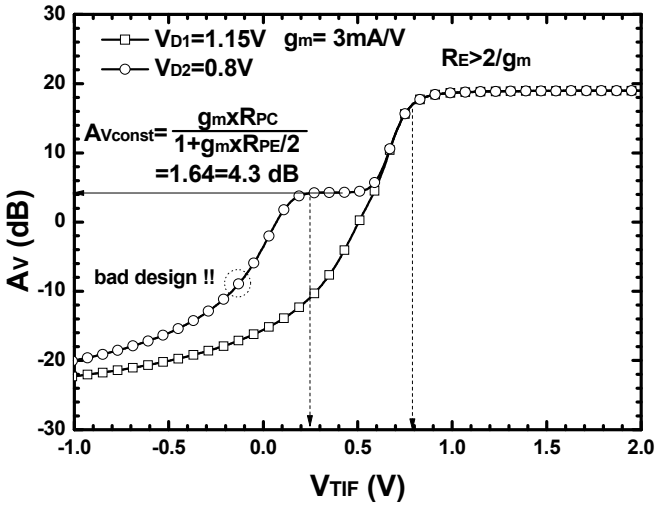


Fig. 6-11 VGA with a modified *R−r* attenuation method.



(a)



(b)

Fig. 6-12 (a) numerator (g_mR_C) and inverse of the denominator [$1/(1+g_mR_E/2)$] of the voltage gain (A_V) with different locations of transitions (c) the corresponding A_V as a function of V_{TIF}.

The differential voltage gain of the VGA can be easily formulated as

$$A_V = \frac{g_m R_C}{1 + g_m R_E / 2} \tag{6.13}$$

where $R_E = R_{PE} \parallel r_{PE}$ and $R_C = R_{PC} \parallel r_{op} \parallel r_{on} \parallel r_{PC} \approx R_{PC} \parallel r_{PC}$ while assuming r_{op}, $r_{on} >> R_{PC}$. $R_{PE,C}$ is the rigid resistor and $r_{PE,C}$ is the NMOS/PMOS drain-source resistance in the triode region.

Fig. 6-12(a) shows the calculated numerator $g_m \times R_C$ and the inverse of the denominator, $1/(1+g_m \times R_E/2)$, as a function of the IF tuning voltage (V_{TIF}). On the curve of $g_m \times R_C$, the transition ($T1_C$) occurs when r_{PC} becomes larger than R_{PC}. The curve of $1/(1+g_m R_E/2)$ has two transitions, $T1_E$ and $T2_E$. $T1_E$ transition occurs as r_{PE} becomes smaller than R_{PE} while $T2_E$ occurs as $g_m R_E/2$ becomes less than 1 (*i.e.*, $R_E < 2/g_m$). Typically, two tuning voltages should be used to control the two tuning operations. However, after proper design of bias points by transistor sizes, one tuning voltage can be adopted by properly overlapping the two constituent tuning curves. Because A_V is the multiplication of both curves, different sequences of transitions result in different composite tuning curves. Fig. 6-12(b) shows the calculated A_V for two sequences (1) $T1_C < T1_E < T2_E$ and (2) $T1_E < T1_C < T2_E$, respectively. For the former sequence, there is a certain region with a constant voltage gain which is not permissible for real applications as shown in Fig. 6-12(b). On the contrary, a smooth tuning curve can be obtained by the latter sequence of $T1_E < T1_C < T2_E$.

6.3 2.4 GHz Receiver With Passive Mixer Realization

A 2.4-GHz 0.18-μm CMOS DCR is demonstrated using passive mixers to avoid the flicker noise problem in this section. The block diagram of the proposed 2.4-GHz DCR is shown in Fig. 6-13, including an LNA with a single-to-differential transformer load, I/Q passive mixers and IF TIAs and VGAs. Besides, the quadrature

LO signal is generated by a two-stage PPF with the center frequency of 2.4 GHz.

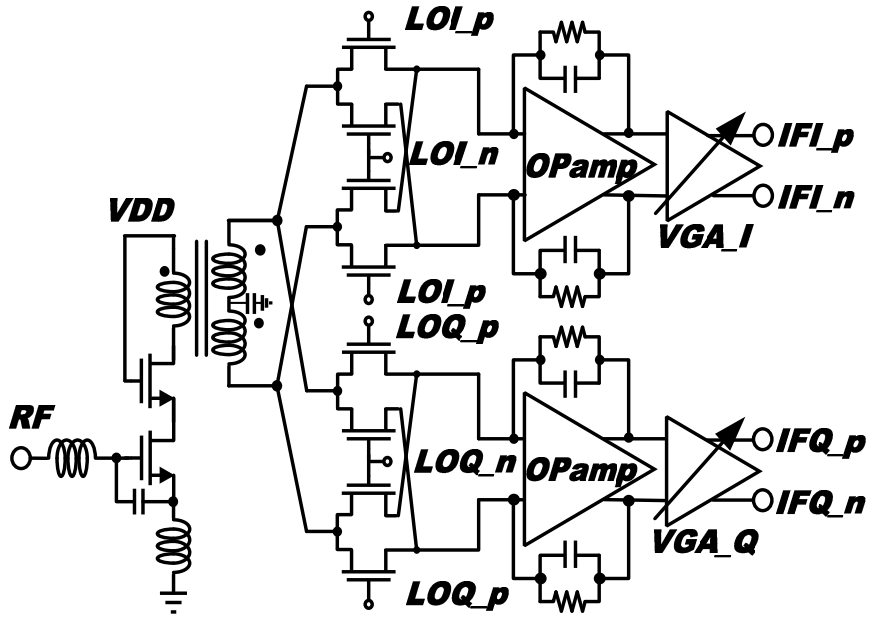


Fig. 6-13 Block diagram of the 0.18-μm CMOS 2.4-GHz DCR using passive mixers.

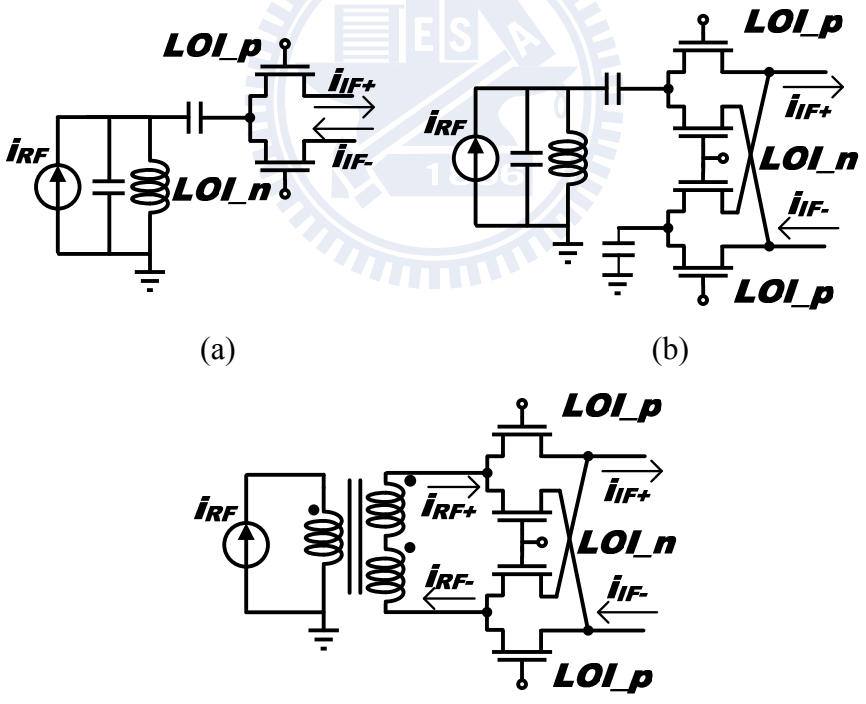


Fig. 6-14 Schematic of (a) single-balanced passive mixer (b) double-balanced passive mixer with single-ended RF input (c) double-balanced mixer with differential RF input.

A cascode LNA with a parallel capacitance C_p is shown in Fig. 6-1. The parallel C_p can be used to reduce the noise impedance under a low power dissipation,

especially at such a low operating frequency of 2.4 GHz, as fully discussed in Section 6.2.1.

Fig. 6-14(a) shows a single-balanced mixer structure which can downconvert the RF sign al but has large amount of LO-to-IF leakage, which can only be suppressed by the following low-pass circuits. Besides, the RF-to-IF leakage is typically a common-mode leakage, which can be cancelled if the following circuits are fully differential. On the other hand, for the double-balanced structure, shown in Fig. 6-14(b) and (c), the large LO signal is cancelled at the IF port. However, the latter structure with fully differential RF inputs performs better RF-to-IF isolation even if the IF output is taken at each signal end. Hence, a single-to-differential transformer is used between the LNA and the passive mixer.

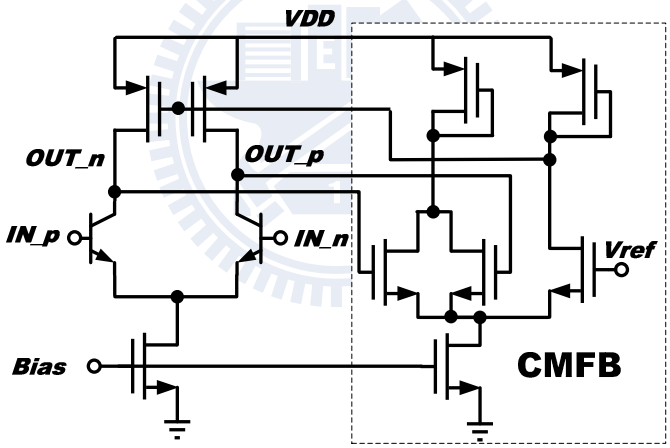


Fig. 6-15 Schematic of a single-stage OP-amp with V-NPN transconductance stage.

The TIA cascaded after the passive mixer consists of a single-stage operational amplifier (OP-amp) with parallel R/C feedback paths. When compared with a common-gate amplifier, which is another widely used structure, the lower input impedance results in better mixer current gain and also better noise performance [74]. Besides, the V-NPN BJT is employed as the g_m stage of the OP-amp, as shown in Fig. 6-15 because of the free of flicker noise and a high gain at a low current, as emphasized in Section 6.2.3. On the other hand, the *R-r* attenuation method is applied

at the IF VGA to achieve a linear-in-dB tuning scheme while the V-NPNs are also used at the g_m stage as shown in Fig. 6-11 described in Section 6.2.4.

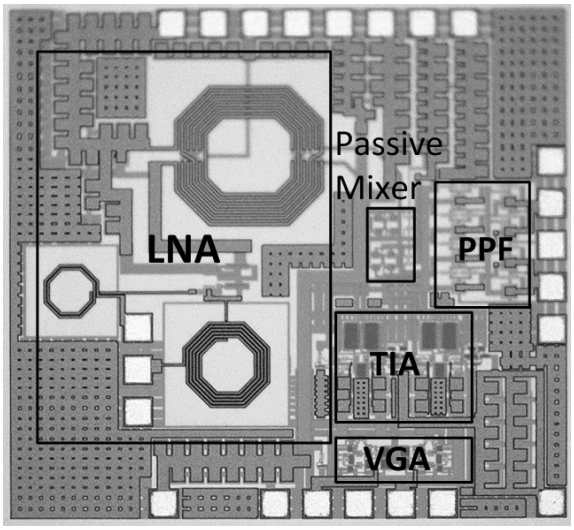


Fig. 6-16 Die photo.

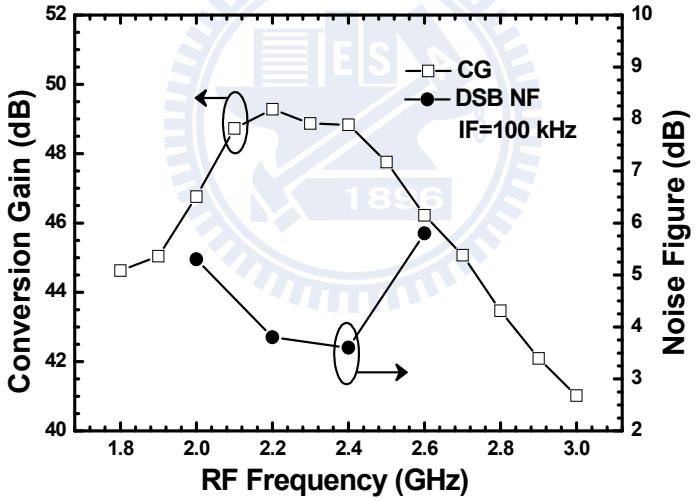


Fig. 6-17 Conversion gain and double-sideband noise figure.

The die photo of the 2.4-GHz DCR is shown in Fig. 6-16 and the die size is 1.3×1.25 mm^2. On-wafer measurement facilitates the RF performance. Fig. 6-17 shows the conversion gain and double-sideband noise figure as a function of the RF frequency. The conversion gain is around 49 dB from 2.1 to 2.4 GHz when LO power is 10 dBm. The minimum noise figure is 3.7 dB and less than 4 dB within 2.2-2.4 GHz. The flicker corner is around 100 kHz when LO frequency is 2.4 GHz, as shown

in Fig. 6-18. Fig. 6-19 indicates the conversion gain with respect to VGA tuning voltage (V_{tune}). An over 20 dB tuning range is achieved.

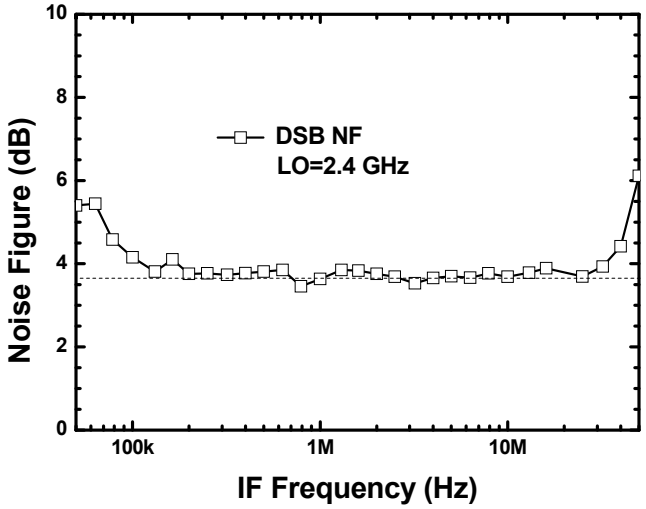


Fig. 6-18 Noise figure with respect to IF frequency.

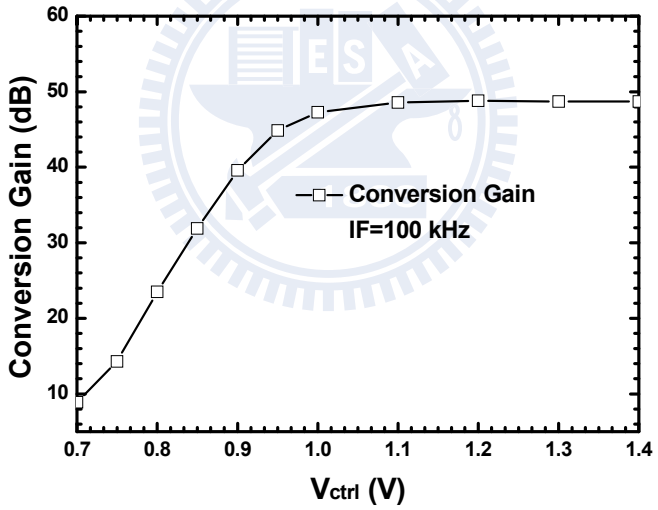


Fig. 6-19 Conversion gain with respect to IF VGA tuning voltage.

The I/Q output waveforms are shown in Fig. 6-20 with 0.13 dB gain difference and 1.03º phase error when RF =2.4001 GHz and LO=2.4 GHz. Fig. 6-21 shows the gain difference < 0.3 dB and I/Q phase error < 2° when LO frequency ranges from 2 to 3 GHz. The input return loss is lower than 10 dB covering 2.1-2.8 GHz as shown in Fig. 6-22.

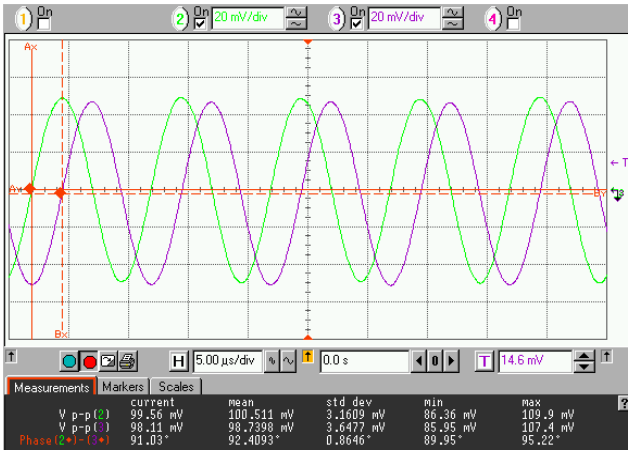


Fig. 6-20 Output I/Q waveforms.

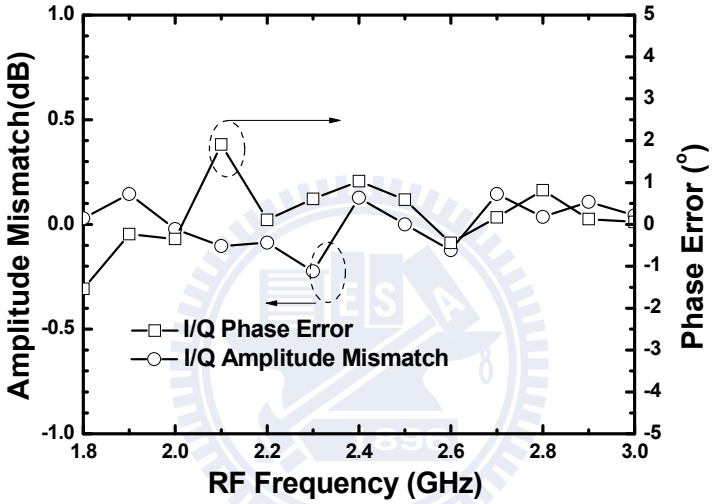


Fig. 6-21 I/Q amplitude mismatch and phase error.

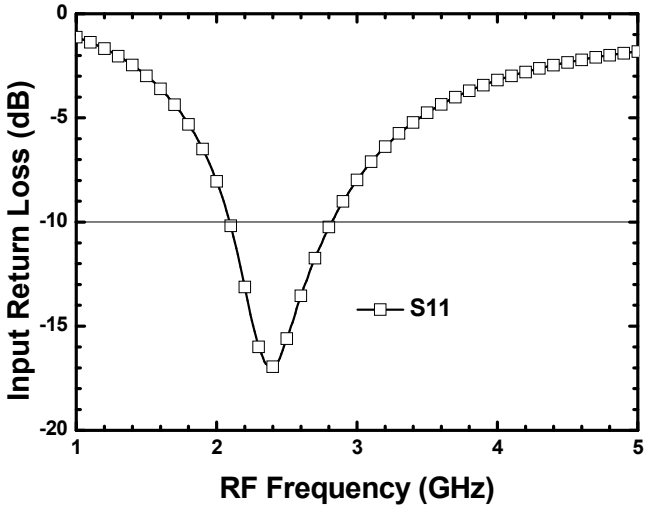


Fig. 6-22 Input return loss.

Moreover, the LO-to-RF/LO-to-IF/RF-to-IF isolation are around 90/50/50 dB,

respectively, when LO frequency is near 2.4 GHz, as shown in Fig. 6-23. The circuit performance is summarized and compared with state-of-the-art DCRs in TABLE. 6.1.

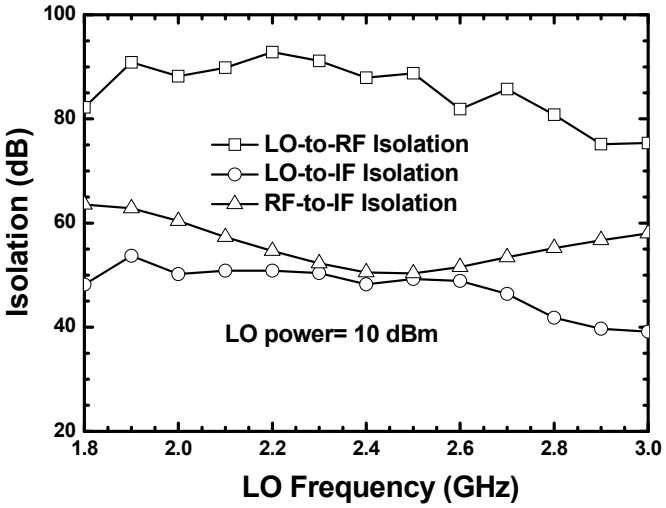


Fig. 6-23 LO-to-RF/IF isolation.

TABLE. 6.1 PERFORMANCE COMPARISON OF DCRS USING PASSIVE MIXERS

Reference	[74]		[90]	[91]	[92]	[93]	This Work
RF Frequency (GHz)	2		2	2	2.4	1.55-2.3	2.4
Conversion Gain (dB)	36	42	30	29	30	22.5-25	49
Noise Figure (dB)	3[a]	2[a]	3.1[a]	3.9	7.3	7.7-9.5[c]	3.7
Flicker Noise Corner (kHz)	N.R.	N.R.	40	70	70	~50	100
IIP_3 (dBm)	−10.4	−9.9	−12	−1	−8	>7	−35 (at max gain) −15 (w/o VGA)
Supply Voltage (V)	1.2		1.5	1.8	1.8	2	1.8
Power Dissipation (mW)	LNA:9.84 CG TIA:1.92	LNA:9.84 OP-amp-based TIA:1.92	12[b]	15	6.3	10 (TIA)	8.5
Technology	65 nm digital CMOS		0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS

[a] off-chip input matching

[b] excluding off-chip baseband circuits

[c] w/o LNA

6.4 2.4 GHz Low-Noise Receiver With Vertical-NPN BJT

6.4.1 2.4 GHz Receiver With Vertical-NPN BJT Operating at Near Cut-Off Frequency

A 2.4-GHz low-power low-noise DCR is demonstrated using parasitic V-NPN BJTs in a standard 0.18-μm CMOS process. The current switching operation of a Gilbert mixer with finite transistor f_T is thoroughly analyzed and discussed in this section. When the mixer operates near or higher than the transistor f_T, the loss of the PPF due to the capacitive loading of the mixer is a main issue. Thus, BJT devices with smaller base resistance and an inductive peaking technique with symmetric 3D realization are employed in this paper to reduce LO power by 4.5 dB.

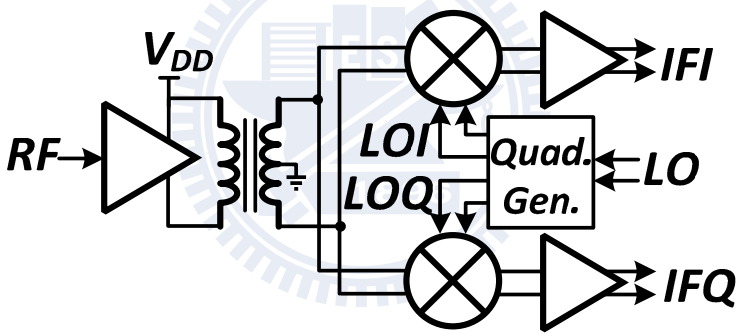
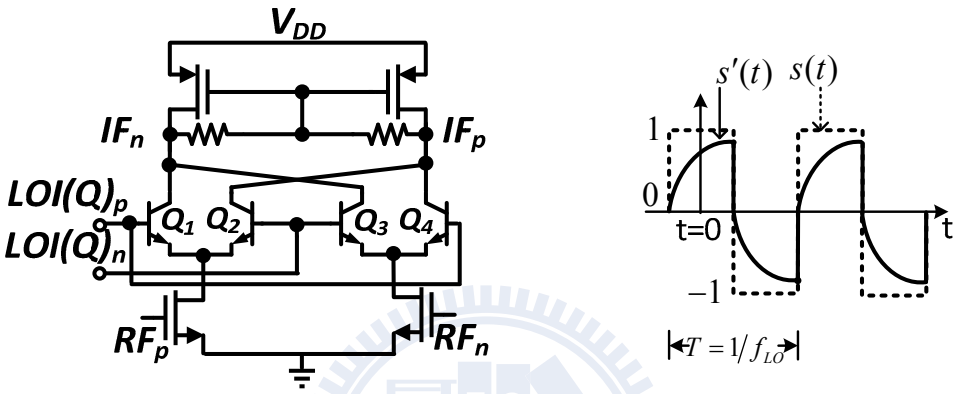


Fig. 6-24 Block diagram of the DCR including LNA, I/Q mixers, I/Q VGAs and an LO quadrature generator.

Fig. 6-24 shows the block diagram of the DCR consisting of a single-in-differential-out LNA, I/Q Gilbert mixers with the V-NPN BJT switching core, I/Q VGAs and an LO quadrature generator. The schematic of the LNA is shown in Fig. 6-1. The noise-impedance-matched LNA under power constraint with the effect on lossy inductors is fully discussed in Section 6.2.1. A tuning transistor (M_T) is used to achieve gain reduction and avoid signal compression when a large RF signal is applied. The transistor M_T acts as a current switch that reduces the output signal by

shunting the RF current away from the inductive load, as shown in Fig. 6-1. In addition, a 5:4 transformer is employed at the load of the cascode LNA to transform the single-ended input current to differential output voltage. The gate dc voltage of the g_m stage in I/Q mixers is fed from the center-tap of the secondary coil in the transformer. On the other hand, an IF VGA with 20-dB linear-in-dB tuning range is implemented using an *R-r* attenuation method, as shown in Fig. 6-11 in Section 6.2.4.



(a) (b)

Fig. 6-25 (a) Schematic of the Gilbert mixer with V-NPN BJT in LO switching core (b) LO switching function with infinite/finite f_T in large LO region.

The V-NPN BJT has only around 200-Hz flicker noise corner, while the advanced 0.18-μm NMOS device has around several-MHz corner frequency under the same dc current of 250 μA, as shown in Fig. 6-9 in Section 6.2.3. Thus, V-NPN BJTs are used in the LO switching core to guarantee a low flicker corner as shown in Fig. 6-25(a). Instead of a pure resistive load (without flicker noise contribution), PMOS devices with a 2-μm gate length are applied for a more constant dc bias against process variation and still have allowable flicker noise performance. On the contrary, the high-performance but high flicker corner NMOS device can be used in the RF LNA and the RF g_m stage of the mixers because the low-frequency noise at the RF stage will be upconverted to the odd harmonics of the LO signals, not baseband, after the switching operation.

Although the V-NPN BJT in the mixer core has a 200-Hz flicker noise corner, it has a relatively low f_T. Here, we stress the effect of the transistor f_T on the switching function. The BJT-based Gilbert cell has an exact mathematical expression of current switching function [3]

$$s(t) = \frac{i_{out}}{i_{RF}} = \tanh(u) \tag{6.14}$$

where $u = \frac{V_{LO}}{2V_T}\cos\omega_{LO}t$.

The small-signal conversion gain of the current switching function can be computed as the mean dc output current when the input signal is $i_{RF} = \hat{i}_{RF} \cdot \cos(\omega_{LO}t)$:

$$CG = \frac{\overline{i_{out}}}{\hat{i}_{RF}} = \frac{1}{T}\int_0^T s(t)\cos(\omega_{LO}t)dt \,. \tag{6.15}$$

The current switching function can be simplified for two extreme cases:

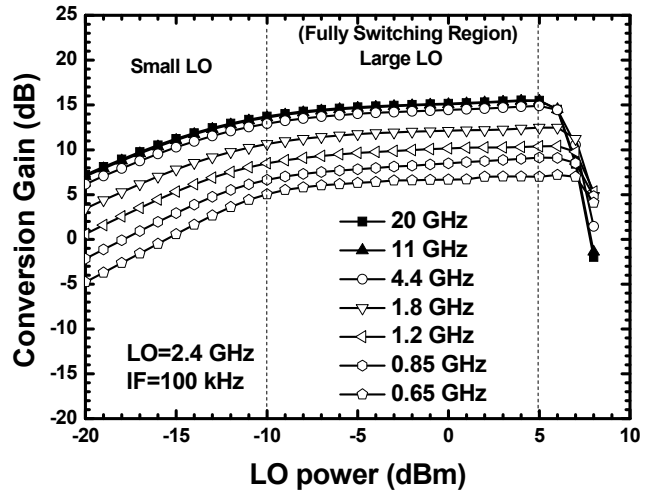
$$s(t) = \begin{cases} \text{sgn}(u), & |u| >> 1 \text{ (large LO)} \\ u, & |u| << 1 \text{ (small LO)} \end{cases} . \tag{6.16}$$

That is, the switching function of the mixing core in the large-LO (fully-switching) region can be approximated as a square-wave, drawn by the dotted line in Fig. 6-25(b).

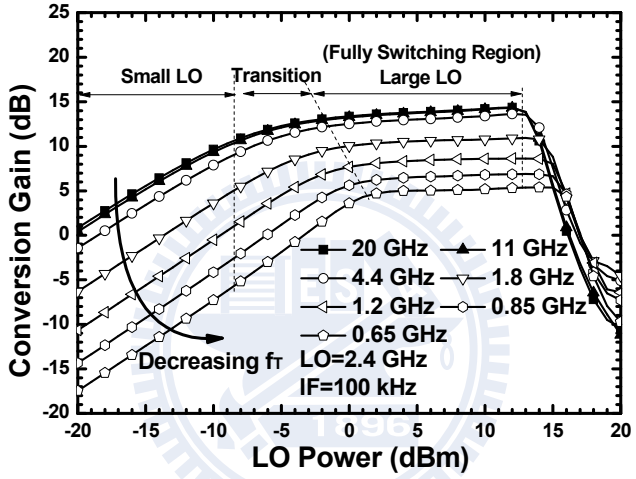
Therefore, the *CG* of the switching function $s(t)$ in the large-LO region is $2/\pi$ [94]. On the other hand, when the LO power is small, the *CG* can be calculated as

$$CG = \frac{1}{T}\int_0^T \left(\frac{V_{LO}\cos(\omega_{LO}t)}{2V_T}\right)\cdot\cos(\omega_{LO}t)\cdot dt = \frac{V_{LO}}{4V_T} \,. \tag{6.17}$$

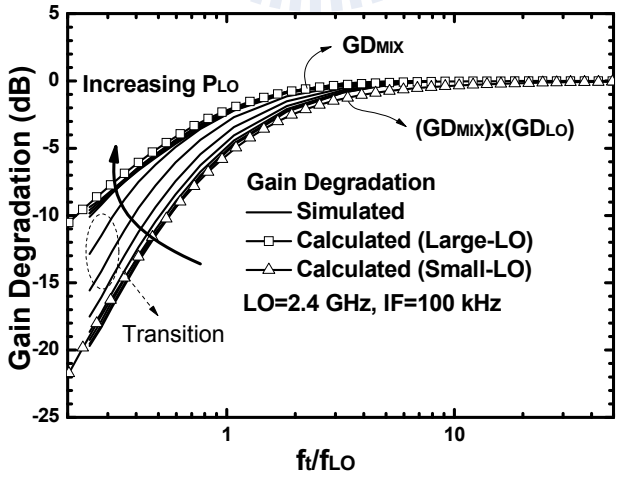
That is, the *CG* is proportional to the LO voltage swing (V_{LO}).



(a)



(b)



(c)

Fig. 6-26 Conversion gain with respect to LO power at different for different f_T when (a) LO voltage signals are directly fed to the base nodes of the switching core (b) LO signals are generated from a two-stage PPF (c) conversion gain degradation as a function of relative cut-off frequency ($f_T' = f_T / f_{LO}$).

The simulated *CG* of a Gilbert mixer [Fig. 6-25 (a)] is shown in Fig. 6-26(a) with different f_T of the BJT switching core, while the differential LO voltage signals are fed from the base nodes of the switching core. Fig. 6-26(a) clearly shows that the *CG* increases as the LO power increases when the LO power is small. Gradually, the *CG* reaches a wide flat gain response (*i.e.*, in the large-LO region). The wide LO power range with a flat-gain response covers typically more than 10 dB. However, when the LO signals are generated by a two-stage PPF, the conversion gain with respect to the LO power can be re-drawn as Fig. 6-26(b). Comparing Fig. 6-26(a) and (b), the required LO power increases when adopting a PPF. Further, at a higher frequency, the required LO power is also larger and thus the flat-gain region becomes narrower.

On the other hand, the conversion gain at the flat-gain region is the same in two figures at a given frequency. In the large-LO region, the switching function $s'(t)$ replaces $s(t)$ as indicated by a solid line in Fig. 6-25(b) when a finite f_T is considered and can be expressed as

$$s'(t)=\begin{cases}1-e^{-\omega_T(t-nT+T/4)}, & nT-T/4<t<nT+T/4\\ -\left[1-e^{-\omega_T(t-nT-T/4)}\right], & nT+T/4<t<nT+3T/4\end{cases}. \tag{6.18}$$

That is, the whole current charges the capacitance (C_π) of Q_1/Q_4 in the positive LO period while $C_{\pi 2}$ and $C_{\pi 3}$ are charged in the negative LO period. Thus, after the detailed derivations summarized in Appendix B, the CG of $s'(t)$ is

$$CG=\frac{2}{\pi}\left[1-\frac{1}{2}\frac{1+e^{-\pi f_T'}}{1+(f_T')^2}\right] \tag{6.19}$$

where $f_T'=f_T/f_{LO}$ represents the relative cut-off frequency. It is evident that a lower f_T results in a lower *CG* as shown in Fig. 6-26(a).

As a result, the gain degradation of the mixer (GD_{MIX}) due to the finite transistor

f_T can be represented as

$$GD_{MIX}=\frac{CG}{CG_{\max}}=1-\frac{1}{2}\frac{1+e^{-\pi f_T'}}{1+(f_T')^2}. \tag{6.20}$$

where $CG_{\max}$ is defined as the CG when the f_T is infinite.

In fact, the low f_T of the switching transistors also results in an LO voltage loss because of the loading effect of the LO PPF [95]. The flat gain region corresponding to the fully switching function becomes smaller for a lower f_T as shown in Fig. 6-26(a). Thus, the LO voltage loss is tolerable in the large-LO region.

On the other hand, the CG degrades much more seriously in the small-LO region than in the large-LO region as shown in Fig. 6-26(b). Because the CG is proportional to V_{LO} when the Gilbert mixer operates in the small-LO region, the degradation of the LO voltage directly leads to CG degradation. As a result, the GD due to LO loss (GD_{LO}) should be included and the overall GD can be approximated as

$$GD_{total}= GD_{MIX}\times GD_{LO}. \tag{6.21}$$

The GD_{LO} can be expressed as follows

$$GD_{LO}=\sqrt{\frac{2}{1+\left[1+2g_mR_n/f_T'\right]^2}} \tag{6.22}$$

where g_m is the transconductance of the switching device and R_n is the resistance at the n_{th} stage (last stage) of the PPF. The complete derivation is also summarized in Appendix B.

For a more clear observation of the GD, Fig. 6(c) shows the GD with respect to the relative cut-off frequency (f_T') at different LO power levels and the data is directly taken from Fig. 6-26(b). The line with the square symbol represents the calculated GD in the large-LO switching function (*i.e.*, GD_{MIX}) while the GD with small LO input is indicated by triangular symbols (*i.e.*, $GD_{MIX}\times GD_{LO}$). Two lines

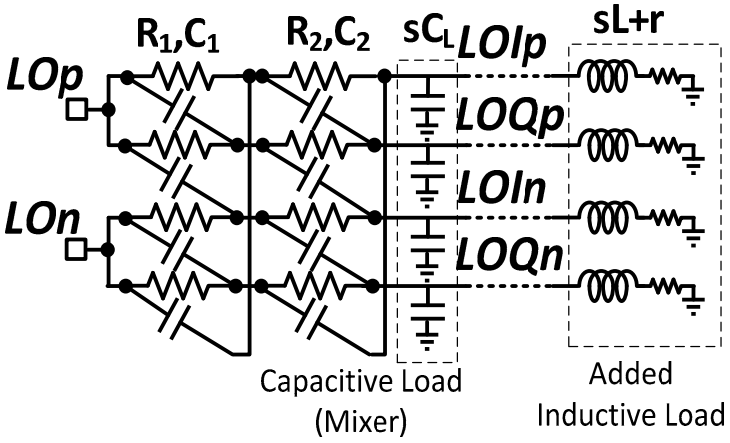
successfully represent the upper and lower bounds of the *GD* at different LO power levels while the solid lines represent the simulated *GD* at different LO power and are thoroughly located within the two calculated boundaries.

It is noteworthy that, this phenomenon is also suitable for an MOS switching core. However, a larger LO power is required to commute the tail current from one side to the other because a MOS differential pair requires a $\sqrt{2}V_{ov}$ LO voltage swing while only around $4V_T$ (~0.1 V) is required for a BJT core. As a result, the fully-switching region of the LO power range is relatively narrow and even disappears if a low-supply voltage is applied.

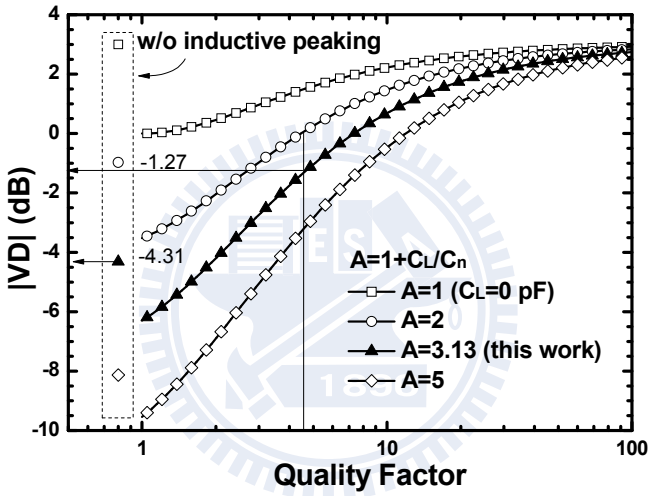
A multi-stage PPF is widely used as a quadrature generator in single-sideband upconverters, image-rejection downconverters and I/Q downconverters [26], [95]. Since the quadrature phase error of the *n*-stage PPF can be expressed as $\phi = 2\tan^{-1}[(\omega-\omega_0)/(\omega+\omega_0)]^n$ where ω_0 is the designed center frequency. In other words, for a given tolerable phase error ϕ_0, the ratio bandwidth becomes $[(1+\varepsilon_n)/(1-\varepsilon_n)]^2$ where $\varepsilon_n = \tan^{1/n}(\phi_0/2)$. That is, more stages of the PPF results in a less phase error within the target bandwidth or a wider tolerable bandwidth for a given phase error. In addition, the phase accuracy is independent of loading, but the loadings affect the overall voltage loss, as mentioned in [95]. The PPF has a certain voltage loss due to both the inter-stages and the loading stages. In this work, we are especially concerned with the loss due to the output loading (*i.e.*, the mixers) because it is the sole term related to the mixer transistor f_T. As proposed in [95], the voltage division (*VD*) at the output node can be expressed as

$$VD(\omega_0) = \frac{Z_L}{Z_L + R_n \,||\, (1/j\omega_0 C_n)} \tag{6.23}$$

where $\omega_0 = 1/(R_n C_n)$.



(a)



(b)

Fig. 6-27 (a) Schematic of the two-stage PPF with original capacitive load and additional inductive load (b) calculated optimal voltage division (*VD*) as a function of inductor quality factor (Q) for different capacitive loadings.

Conventionally, Z_L is typically a capacitive load (C_L) due to an active/passive mixer. Thus,

$$\left|VD(\omega_0)\right| = \frac{2}{\sqrt{1+(1+C_L/C_n)^2}}. \tag{6.24}$$

A large loading capacitance results in an incredible loss. In this work, parallel inductors are employed to optimize the LO voltage loss, as shown in Fig. 6-27(a). A

simple model of a real inductor consists of a series resistor (R_S) and an inductor (L_S) with a quality factor (Q) defined as $\omega_0 L_S / R_S$. Generally, the R_S is proportional to the geometric length and thus also proportional to the L_S. In fact, the parasitic capacitance C_{par} should be included for each inductor, which can be merged to C_L for simplicity.

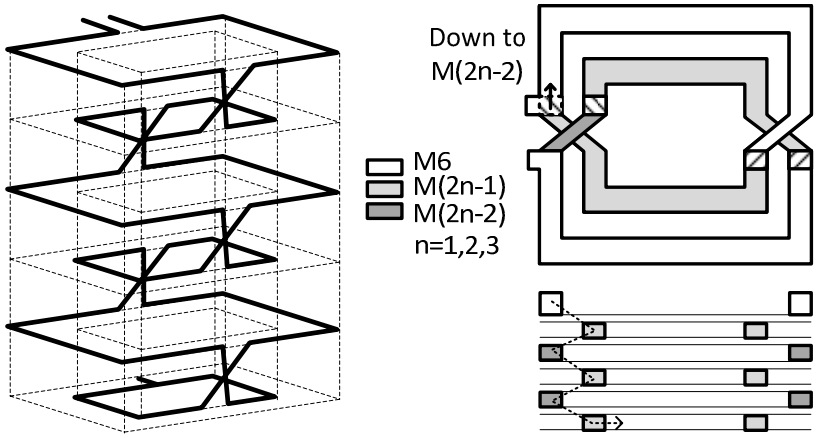
After detailed derivations summarized in Appendix C, the maximum $|VD(\omega_0)|$ and its corresponding L_{opt} are

$$\begin{cases} \left|VD(\omega_0)\right|_{opt} = \dfrac{\sqrt{2(1+Q^2)}}{A+Q} \\ L_{opt} = \dfrac{1}{\omega_0^2 C_n (A-1/Q)} = \dfrac{1}{\omega_0^2 \left[C_n (1-1/Q) + C_L\right]} \end{cases} \tag{6.25}$$

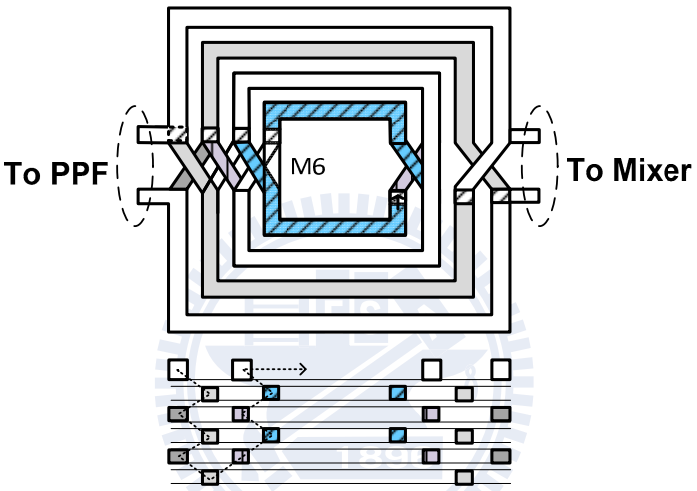
where $A=1+C_L/C_n$.

Fig. 6-27(b) shows the $|VD|$ as a function of Q with different $A(=1+C_L/C_n)$. The $|VD|$ without peaking inductors is also indicated in the same figure. It reveals that when the loading capacitance is small, an inductive peaking technique has no improvement. Further, when Q reaches infinity, the $|VD|_{opt}$=+3 dB, which is the same as the result in an open-load situation. However, in practice $|VD|_{opt}$ degrades due to a finite Q. For the double-balanced structure of a Gilbert mixer, the peaking inductor parallel between the PPF and mixer core should be also symmetric to maintain a fully differential performance. Besides, the differential inductor can provide size reduction and a better Q than separate inductors [96].

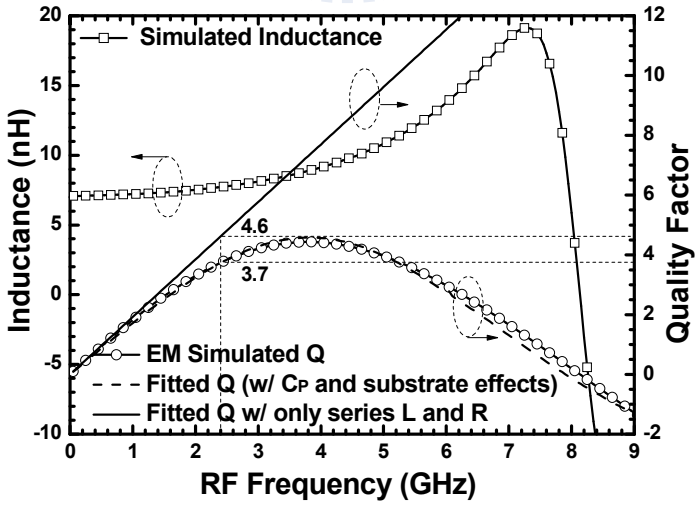
In this work, a 3D symmetric inductor realization is employed for further area saving. Fig. 6-28(a) shows the multi-layer structure of a pseudo-two-turn symmetric 3D inductor proposed in [97]. The top view and cross-section view of this 3D inductor are shown in Fig. 6-28(b).



(a) (b)



(c)



(d)

Fig. 6-28 (a) 3D view and (b) top view of the pseudo-two-turn layout of the fully symmetric stacked inductor (c) top view and (d) simulated inductance and quality factor of the proposed pseudo-four-turn (equivalent eleven turns) fully symmetric stacked inductor.

A pseudo-two-turn layout can provide at most six turns of an inductor in a 1P6M 0.18-μm CMOS process. However, the inductance is not enough. Using the basic idea of interleaving the inner and outer turns, this structure can be extended to a pseudo-four-turn formation as illustrated in Fig. 6-28(c). As a result, a 3D inductor with eleven turns is achieved with 8-μm line width, 2-μm line spacing and an outer diameter of only 100 μm. The EM simulated differential inductance and quality factor are 7.2 nH and Q_{max}=4.5 with f_{Qmax}/f_{res} of 3.6/8.2 GHz as shown in Fig. 6-28(d). Here, we emphasize that the Q of the inductor degrades by the parasitic capacitance but this is not included in the Q used in (13). In fact, after extraction, the 3D inductor has a differential inductance of 7.2 nH and a series resistance of 23.6 Ω. That is $Q=\omega_0 L/R$=4.6, not 3.7, as indicated in Fig. 6-28(d). Moreover, additional parasitic capacitance should be added to C_L when calculating Eqn. (6.25).

In this work, C_n=0.444 pF (R_n=150 Ω), C_L=0.945 pF, and Q_{ind}=4.6. As a result, the loss due to the pure capacitive load C_L (i.e., without inductive peaking) is around 4.31 dB. Around 3-dB improvement is obtained when using the inductive peaking technique, as shown in Fig. 6-27(b).

Further, all the above discussions are concerned about the pure capacitive mixer load. However, it is noteworthy that the series R_B of the V-NPN BJT is important for the LO power loss, especially for the parasitic devices even though the current switching mechanism is dominated by the transistor f_T. As indicated in Fig. 6-29, the R_B not only decreases the load impedance (at resonance) of the PPF (*i.e.*, increases the voltage loss due to the PPF loading) but also reduces the voltage delivered to V_π by a factor of $1/(1+sR_BC_\pi)$. The simulated CG with respect to LO power for different R_B is shown in Fig. 6-30. Thus, a small R_B results in a lower LO power requirement but the maximum CG are almost the same with different R_B. As discussed in Section 6.2.3,

f_{max} is a criterion for the parasitic resistance R_B; thus the device of $W_E \times L_E \times n = 0.5 \times 4 \times 2\mu m^2$ is chosen for its lowest required LO power to reach the peak CG of the Gilbert mixer.

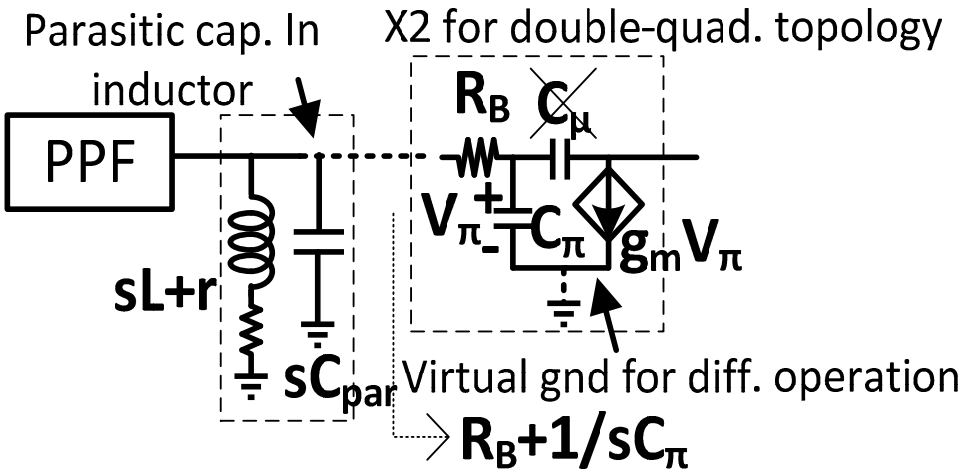


Fig. 6-29 Schematic polyphase loadings including 3D inductor and mixer with parasitic R_B.

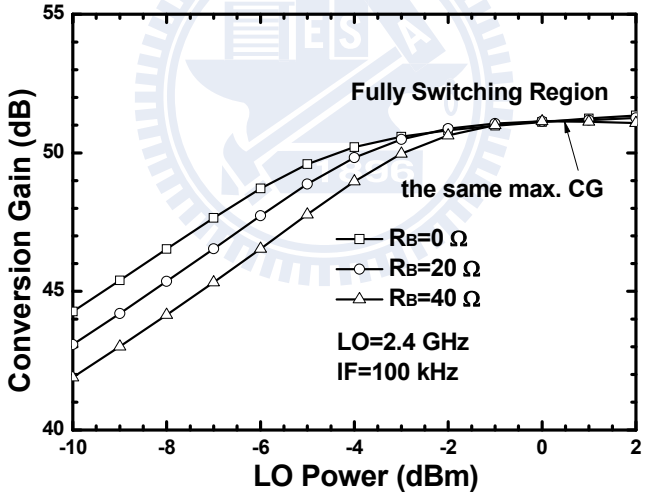


Fig. 6-30 Simulated conversion gain as a function of LO power with different transistor R_B.

The die photo of the 2.4-GHz low-power low-noise DCR is shown in Fig. 6-31 and the die size is 1.15×1.05 mm^2. On-wafer measurement facilitates the RF performance. Fig. 6-32 shows the CG and noise figure as a function of the RF frequency. The peak CG is 52 dB at 2.45 GHz with a 1-dB gain-flatness bandwidth ranging from 2.4 to 2.55 GHz. The minimum noise figure is 3.2 dB at 2.4 GHz and less than 4 dB within 2.3-2.6 GHz.

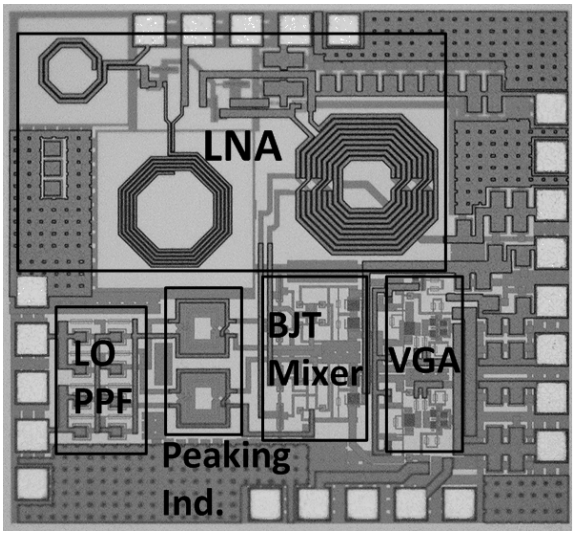


Fig. 6-31 Die photo.

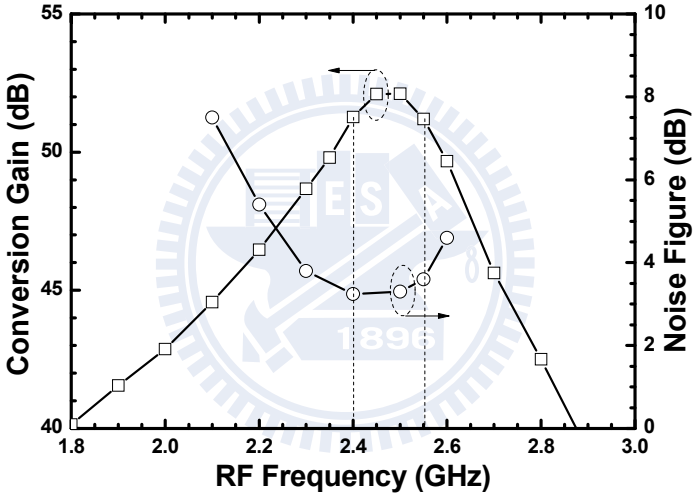


Fig. 6-32 Conversion gain and noise figure with respect to RF frequency.

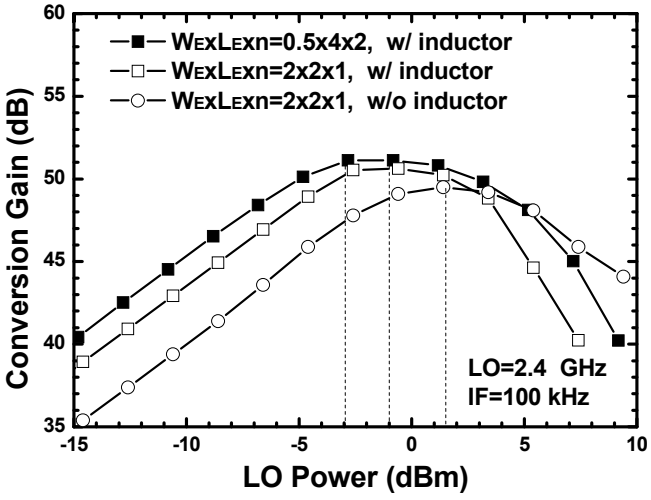
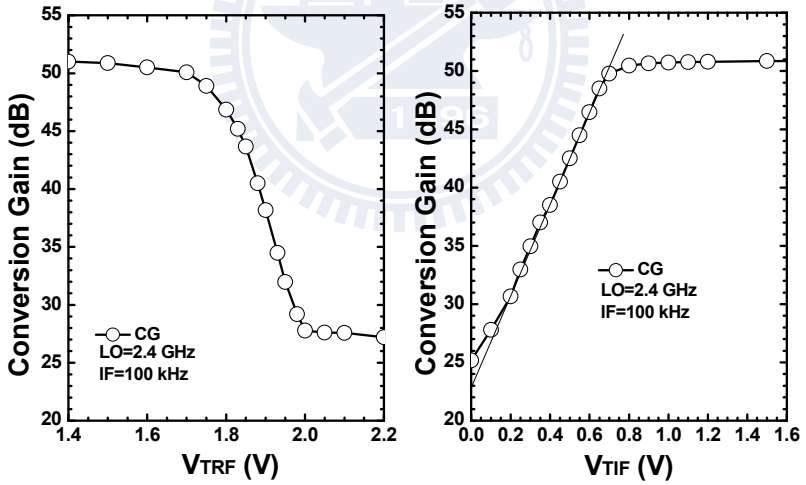


Fig. 6-33 Conversion gain as a function of LO power.

Fig. 6-33 shows the CG with respect to the LO power at LO=2.4 GHz of three designs. The first design (the main design) uses two parallel inductors and the BJT size is $W_E \times L_E \times n = 0.5 \times 4 \times 2$ μm^2. Compared to the first design, the second and third designs have the BJT size of $W_E \times L_E \times n = 2 \times 2 \times 1$ μm^2 (with lower f_{max}) and the former has parallel inductors but the latter does not. As a result, only -3-dBm LO power is used to reach the maximum CG of 51 dB at 2.4 GHz for the main design. As shown in Fig. 6-33, using a higher f_{max} transistor results in around 2-dB less LO power requirement while the peak gain is similar, as predicted. On the other hand, the mixer without resonance inductors (the third design) requires around 2.5-dB larger LO power to reach the peak gain than that with inductors (*i.e.*, the second design). That is, using both a better device selection and an inductive peaking technique, the overall LO power is reduced by around 4.5 dB.



(a) (b)

Fig. 6-34 Conversion gain with respect to (a) RF tuning voltage (b) IF tuning voltage.

Fig. 6-34(a) shows the CG as a function of the LNA RF tuning voltage (V_{TRF}) while Fig. 6-34(b) indicates the CG with respect to the VGA IF tuning voltage (V_{TIF}). An over 20 dB tuning range is achieved by both RF and IF tuning schemes. Fig. 6-35 shows the noise figure when LO=2.4 GHz at different LNA gain. The noise figure is

around 3.2/6/10 dB when CG=51/46/41 dB, respectively, while the flicker corner is around 70 kHz. Besides, the noise figure is kept below 4 dB when the IF VGA gain is reduced by over 20 dB while the LNA is on the maximum gain condition.

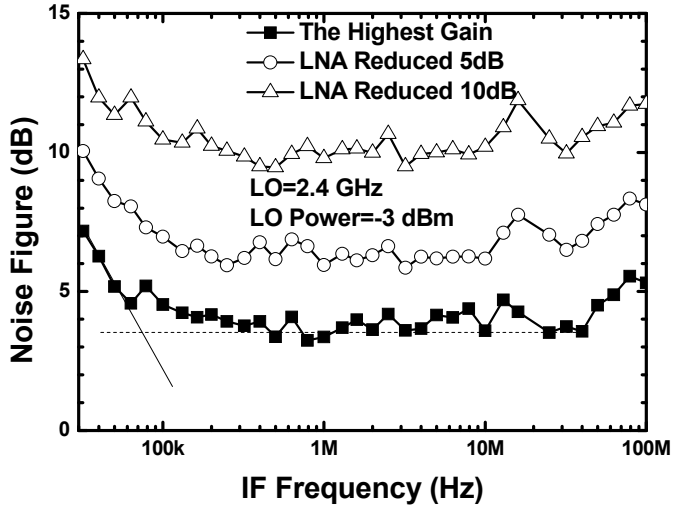


Fig. 6-35 Noise figure with respect to IF frequency.

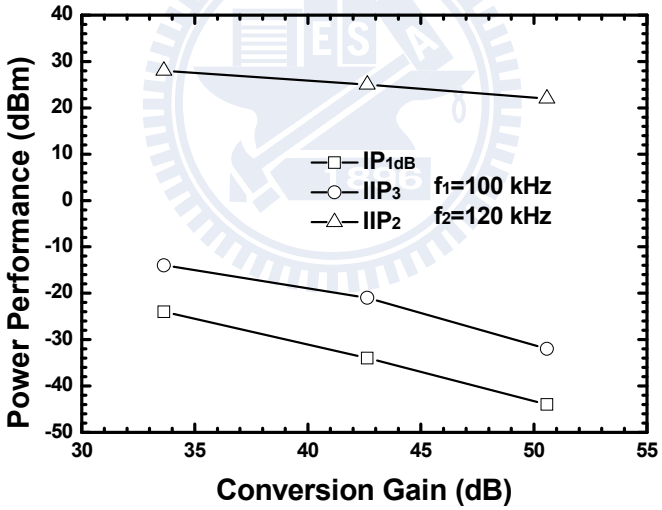
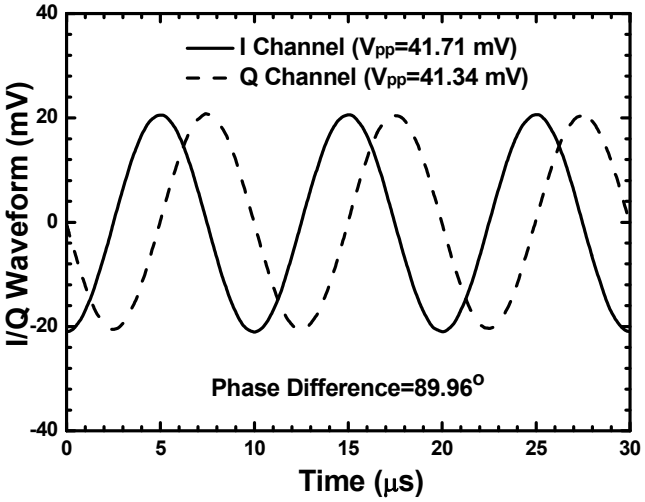
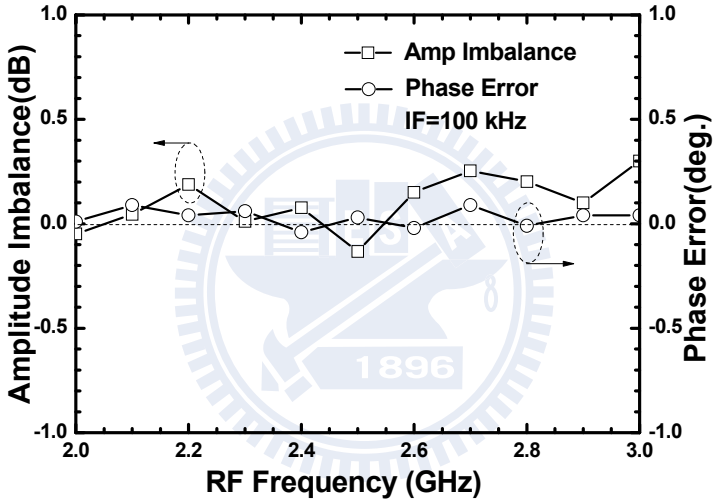


Fig. 6-36 Power performance, including IP_{1dB}, IIP_3, IIP_2.

Fig. 6-36 shows the power performance, including IP_{1dB}, IIP_3, IIP_2, at different gain conditions. The I/Q output waveforms are shown in Fig. 6-37(a) with 0.077 dB gain difference and 0.04º phase error when RF =2.4001 GHz and LO=2.4 GHz. Fig. 6-37(b) shows the gain difference <±0.3 dB and I/Q phase error <±0.1° when LO frequency ranges from 2 to 3 GHz. The input return loss is less than 10 dB covering 2.2-2.6 GHz.



(a)



(b)

Fig. 6-37 (a) I/Q waveforms at RF=2.4 GHz (b) I/Q amplitude imbalance and phase error.

The circuit performance is summarized and compared with state-of-the-art DCRs in TABLE. 6.2. The passive mixer realizations [91]-[92] typically have worse noise performance, but the off-chip input matching inductors and off-chip baseband circuits results in a very low noise figure and also a very low flicker noise corner [90]. On the other hand, active mixer realizations [98]-[99], [102] suffer from a serious flicker noise problem (i.e., flicker noise corner is typically higher than 1 MHz) while the current bleeding technique reduces the flicker noise corner down to 350 kHz [101], which is still higher than this work. In [100], a low-noise high-gain receiver was

proposed using BiCMOS technology to directly avoid the flicker noise problem at a higher cost. As a result, the proposed receiver has excellent RF performance using low-cost 0.18-μm CMOS process.

TABLE. 6.2 PERFORMANCE COMPARISON OF DCRS AT AROUND 2 GHZ

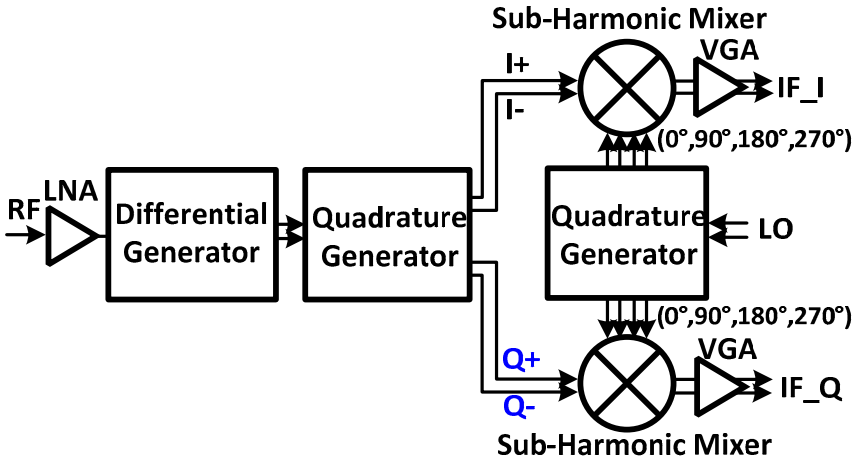
Reference	[90]	[91]	[92]	[98]	[99]	[102]	[101]	[100]	This Work
Mixer Topology (**A**: Active; **P**: Passive)	**P**	**P**	**P**	**A**	**A**	**A**	**A** w/ current bleeding	**A** w/ BJT core	**A** w/ BJT core
RF Frequency (GHz)	2	2	2.4	2.4	1.6	2.5	1.9	2	2.4
Single-Ended Input	Yes	No	Yes	No	Yes	No	No	Yes	Yes
Conversion Gain (dB)	30	29	30	52	36	43	47	33	51
Noise Figure (dB)	3.1[a]	3.9	7.3	24.5	4.8	5	5.6	4.3	3.2
Flicker Noise Corner (kHz)	40	70	70	N/R	~1000	N/R	350	10	70
IIP_3 (dBm)	−12	−1	−8	−21	−19	−37	−2	−14.5	−32
IIP_2 (dBm)	39	35	40	18	N/R	N/R	44.8	34	22
Supply Voltage (V)	1.5	1.8	1.8	1.2	1.2	1.2	1.8	1.8	1.8
Power Dissipation (mW)	12[b]	15	6.3	3.3	5.4[c]	1.4	37.8	22.5	8.1
Technology	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.35μm BiCMOS	0.18μm CMOS

[a] Off-chip input matching
[b] Excluding off-chip baseband circuits
[c] VCO power is included

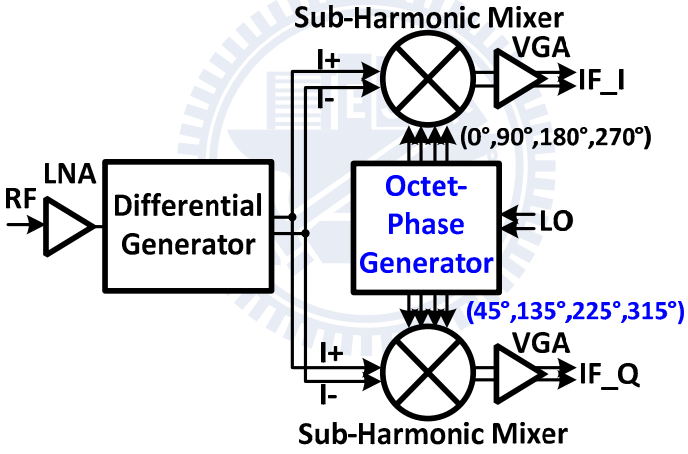
6.4.2 2.4 GHz Sub-Harmonic Receiver With Multi-Stage Octet-Phase Poly-Phase Filter

An SHM topology is chosen in this section to avoid the low-f_T switching operation because the transistor f_T (~2GHz) is larger than the LO frequency (1.2 GHz),

which is only half the RF frequency. Besides, the SHM also achieves a low dc offset because of its additional LO rejection (LOR) [41].



(a)



(b)

Fig. 6-38 Block diagram of an I/Q SH-DCR with (a) both quadrature RF and LO signals (b) differential RF and octet-phase LO signals.

For a single-quadrature I/Q DCR, either RF or LO should be in quadrature. As a result, there are two main types of I/Q SHM topologies to achieve an I/Q SH-DCR. For the corresponding SHMs, an equivalent differential switching operation at 2LO frequency requires that the LO signal should be in quadrature as shown in Fig. 6-38(a) while a quadrature 2LO operation straightforwardly requires octet-phase LO signals as shown in Fig. 6-38(b). Thus, Fig. 6-38(a) consists of both quadrature RF and LO

signals [38] while Fig. 6-38(b) consists of differential RF but octet-phase LO signals [41], [103]-[104]. The IF quadrature phase accuracy is determined by the RF quadrature generator while the quadrature LO signals are only used to perform a 2LO differential switching operation in the former topology. Thus, the former topology has lower loss in the LO signal generation. However, the loss of the RF quadrature generator is especially undesirable in a high-gain low-noise receiver.

On the other hand, an octet-phase LO topology can be employed to avoid the additional RF loss through the gain path as long as the LO power is sufficient and balanced octet-phase LO signals can be generated. A BJT switching core requires a smaller LO power than an MOS switching core and the use of V-NPN BJT with its low f_T of 2 GHz does not cause performance degradation because the LO frequency (~1.2 GHz) is only half the RF frequency for a sub-harmonic mixing operation. Thus, in this work, the latter topology incorporating a multi-stage octet-phase PPF [105] is chosen to generate well balanced octet-phase LO signals. A thorough analysis of the octet-phase PPF is also described in this section.

The block diagram of the proposed SH-DCR is shown in Fig. 6-38(b), including a single-ended-input LNA, I/Q SHMs with BJT switching core, I/Q VGAs and an LO octet-phase PPF.

1) Sub-Harmonic Mixer

The detailed comparisons of the BJT stacked-LO [41], bottom-LO [106] and top-LO [38], [103], [107] SHMs are done in Section 4.1. The top-LO SHM as shown in Fig. 6-39 is chosen here to simultaneously fulfill both the supply-voltage (1.8-V) requirement and the gain/noise performance. The RF NMOS is still applied to the RF gm cell due to the higher f_T and lower noise.

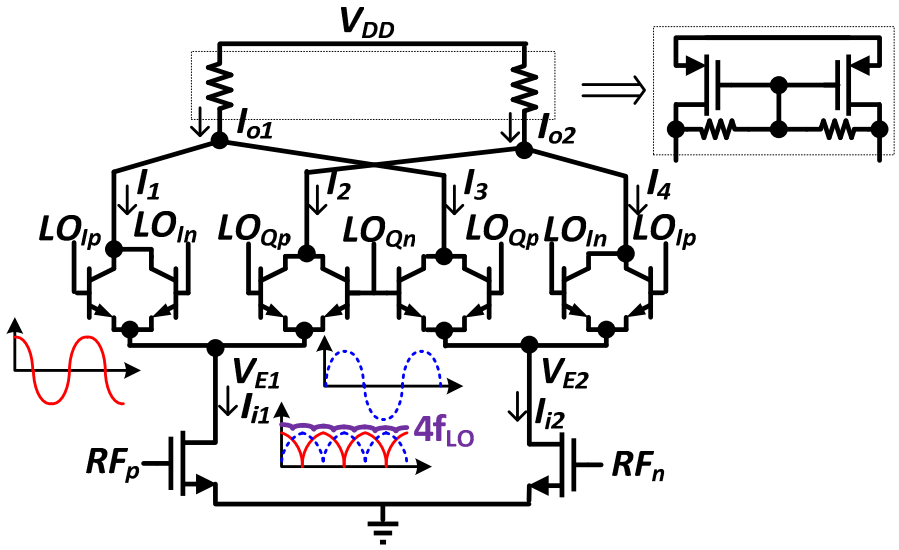


Fig. 6-39 Top-LO SHM with V-NPN BJTs in LO core.

Active PMOS loads with a 2 μm gate length to guarantee the flicker noise less than 10 kHz are applied in this work. The top-LO SHM requires a 3-dB larger LO power than a stacked-LO one, as mentioned in Section 4.1. Thus, the LO octet-phase generator should be carefully chosen and designed to reduce the unwanted LO loss. Although an SHM requires larger LO power than a fundamental mixer, there is still a flat-gain region to a certain extent and can tolerate the amplitude imbalance of the LO signals.

2) Multi-Stage Octet-Phase Poly-Phase Filter

A well-known multi-stage PPF is widely employed as a differential-quadrature generator [95]. However, an octet-phase PPF should be applied to generate the eight vectors required by the top-LO I/Q SHMs. As shown in Fig. 6-40, a single stage PPF is applied at the first stage to generate differential-quadrature outputs (*i.e.*, $[x_1(1), x_1(2), x_1(3), x_1(4)]=[1, j, -1, -j]$) at the center frequency (ω_0) in spite of loadings [95]. The four vectors are further split into eight vectors $x_2(i)$, $i \in \{1,2,\ldots,8\}$ by the following equations

$$\begin{cases} x_2(1) = \dfrac{-jR + 2/sC + R}{2(R + 1/sC)} = \dfrac{(2 + \omega/\omega_0) + j(\omega/\omega_0)}{2(1 + j\,\omega/\omega_0)} \overset{(\omega=\omega_0)}{=} \dfrac{3 + j}{2(1 + j)} \\ x_2(2) = \dfrac{2R + 1/sC + j/sC}{2(R + 1/sC)} = \dfrac{1 + j(1 + 2\,\omega/\omega_0)}{2(1 + j\,\omega/\omega_0)} \overset{(\omega=\omega_0)}{=} \dfrac{1 + 3j}{2(1 + j)} \end{cases} \tag{6.26}$$

and $x_2(k+2) = j \cdot x_2(k), k \in \{1, 2, \ldots, 6\}$.

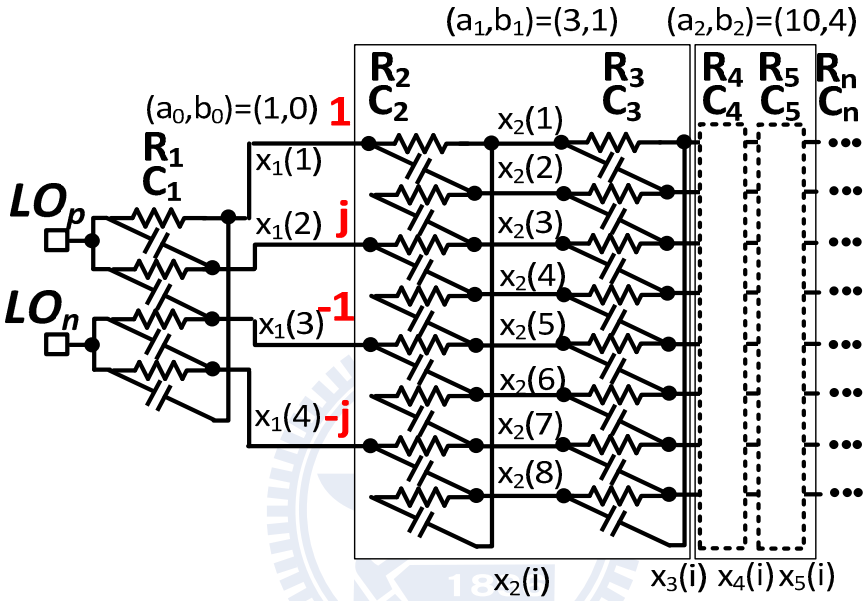


Fig. 6-40 Schematic of a multi-stage octet-phase PPF.

Fig. 6-41(a) shows the vector diagram at the second-stage output. Here, the common denominator is neglected because it only affects the absolute (not relative) gain and phase. Here, we define two variables to quantify the octet-phase signal accuracy

$$AD(\text{amplitude difference}) = \frac{|V(k)|}{|V(l)|} \tag{6.27}$$

and

$$PE(\text{phase error}) = \left|\phi(k) - \phi(l) - 45°\right| \tag{6.28}$$

where $|k - l| = 1,$ and $k, l \in \{1, 2, \ldots, 8\}$.

As a result, all $|x_2(k)|$ are the same (*i.e.*, *AD*=1) but the *PE* is $|\tan^{-1}3-\tan^{-1}(1/3)-45^\circ)|=\tan^{-1}(1/7)=8.13^\circ$, which is not acceptable in a real application.

From the third stage, the gain of each stage follows

$$\begin{aligned} x_n(k) &= \frac{j\omega/\omega_0\, x_{n-1}(k-1)+x_{n-1}(k)}{1+j\,\omega/\omega_0} \\ &= \frac{jx_{n-1}(k-1)+x_{n-1}(k)}{1+j} \\ &= \frac{x_{n-1}(k+1)+x_{n-1}(k)}{1+j} \end{aligned} \tag{6.29}$$

where $k \in \{1,2,...,8\}$ and define $x_{n-1}(0)=x_{n-1}(8)$.

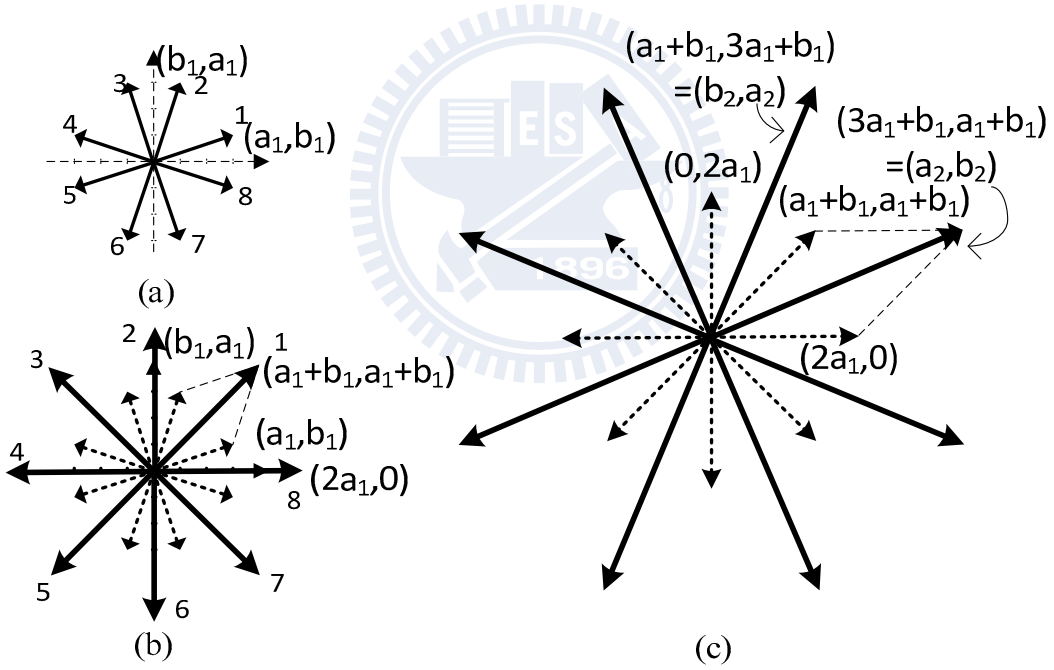


Fig. 6-41 Phasor diagram at (a) second (b) third stage and (c) fourth stage.

Here, $x_{n-1}(k+1)=jx_{n-1}(k-1)$ holds if the quadrature signal at the first stage is perfect. The output vectors at the third stage are shown in Fig. 6-41(b). Thus, perfect 45º phase difference is obtained (*i.e.*, *PE*=0º) but $AD=3/(2\sqrt{2})$=0.51 dB.

If we extend the analysis to more stages, the results are summarized as follows

(1) At the even ($2n_{th}$) stage, the eight vectors are ($\pm a_n$,$\pm b_n$) and ($\pm b_n$, $\pm a_n$)

where $a_n \geq b_n$ is assumed. As a result,

$$\begin{cases} AD = 1 \\ PE = \left| \tan^{-1}(\frac{a_n}{b_n}) - \tan^{-1}(\frac{b_n}{a_n}) - 45° \right| = \tan^{-1} \left| \frac{a_n^2 - b_n^2 - 2a_n b_n}{a_n^2 - b_n^2 + 2a_n b_n} \right| \end{cases}. \quad (6.30)$$

(2) At the odd [$(2n+1)_{th}$] stage, the eight vectors are ($\pm 2a_n$,0), (0,$\pm 2a_n$), and ($\pm(a_n+b_n)$, $\pm(a_n+b_n)$). Thus,

$$\begin{cases} AD = \dfrac{\sqrt{2}a_n}{(a_n + b_n)} \\ PE = 0° \end{cases}. \quad (6.31)$$

Note that, following Fig. 6-41(a) to Fig. 6-41(c), the recursive formula can be directly obtained

$$\begin{bmatrix} a_{n+1} \\ b_{n+1} \end{bmatrix} = X \begin{bmatrix} a_n \\ b_n \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} a_n \\ b_n \end{bmatrix} \quad (6.32)$$

and $(a_1,b_1)=(3,1)$.

It is interesting that, after more stages are cascaded, perfect octet outputs with balanced amplitude/phase are achieved eventually at either the even or odd stage. The detailed derivations are summarized in Appendix D. However, the voltage loss when cascading many stages is unacceptably large. As a result, a three-stage octet-phase PPF is employed in consideration of both voltage loss and signal accuracy. A 0.51-dB LO amplitude imbalance is tolerable because when the LO signal is large enough for an active mixer, the mixer output amplitude imbalance is even smaller, as shown in Fig. 4-6. Finally, an IF VGA with around 20-dB linear-in-dB tuning range is implemented using an *R-r* attenuation method, described in Section 6.2.4. In addition, the V-NPN BJTs are used at the input g_m stage because of the ultra-low flicker noise and the larger g_m under the same dc current consumption than NMOS transistors.

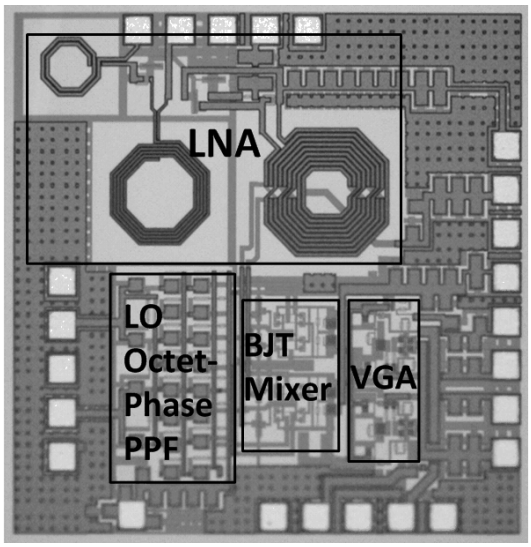


Fig. 6-42 Die photo.

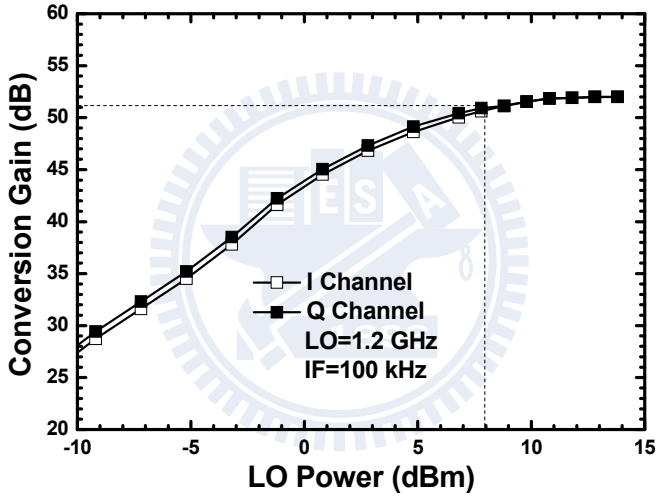


Fig. 6-43 Conversion gain with respect to LO power.

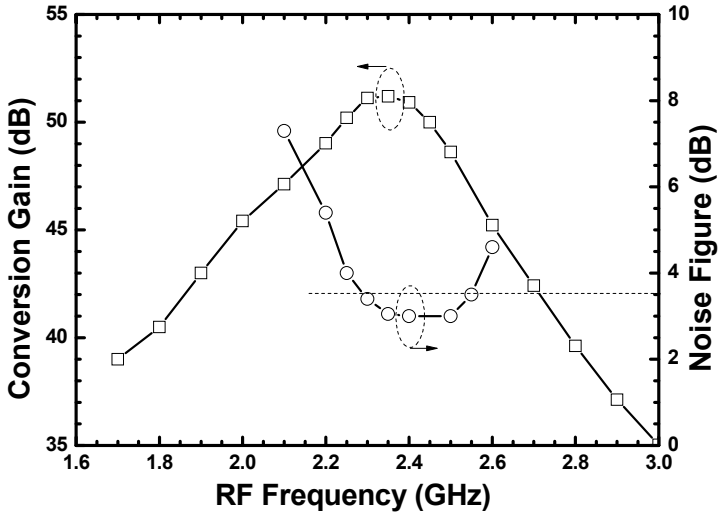


Fig. 6-44 Conversion gain with respect to RF frequency.

The die photo of the 2.4-GHz SH-DCR is shown in Fig. 6-42, and the die size is 1.15×1.05 mm^2. On-wafer measurement facilitates the RF performance. Fig. 6-43 shows the CG of each I/Q channel with respect to the LO power when RF=2.4001 GHz and LO=1.2 GHz. The CG of I/Q channel has around 0.7-dB gain difference at low LO power. When the LO power exceeds 8 dBm, the CG of both channels is almost the same. A maximum CG is 52 dB when LO power exceeds 10 dBm. However, an 8-dBm LO power is applied for all the following measurements. Fig. 6-44 shows the CG and NF as a function of RF frequency. The peak CG is 51.2 dB at 2.35 GHz with a 1-dB bandwidth ranging from 2.25 to 2.45 GHz while the minimum NF is 3 dB and less than 3.5 dB within 2.3-2.55 GHz.

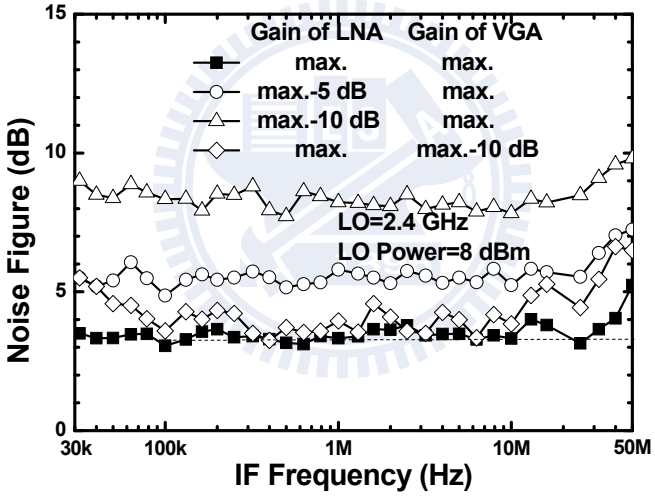
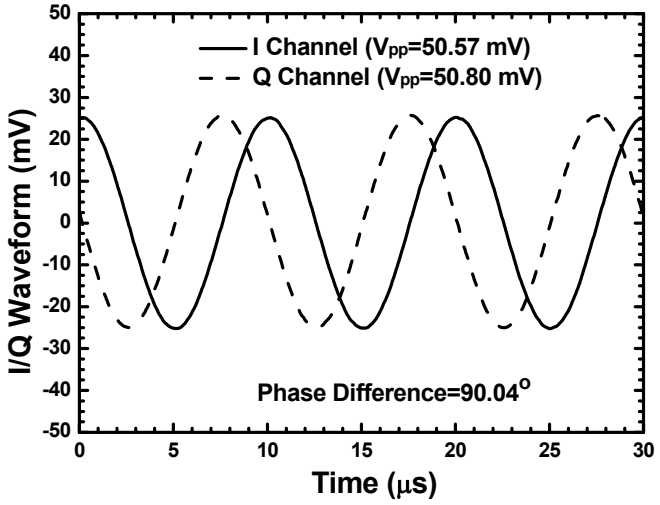


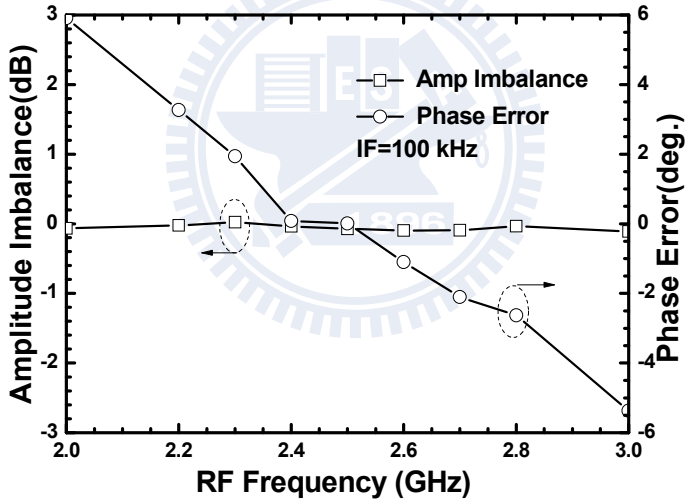
Fig. 6-45 Noise figure with respect to IF frequency.

Fig. 6-45 shows the NF with respect to IF frequency when LO=1.2 GHz. The NF is 3 dB at the highest gain while NF is 5 or 8 dB when the LNA gain is reduced by 5 or 10 dB, respectively. Further, the NF remains around 3 dB when the IF VGA is reduced by 10 dB. The flicker corner is much less than 30 kHz, which is limited by the noise source and dc block in NF measurement. The I/Q output waveforms are shown in Fig. 6-46(a) with 0.04 dB gain difference and 0.04º phase error when RF =2.4001 GHz and LO=1.2 GHz. Fig. 6-46(b) shows the gain difference <0.2 dB and

I/Q phase error <1° when LO frequency ranges from 2.35 to 2.6 GHz. However, the phase error increases when LO frequency is away from center frequency (1.2 GHz).



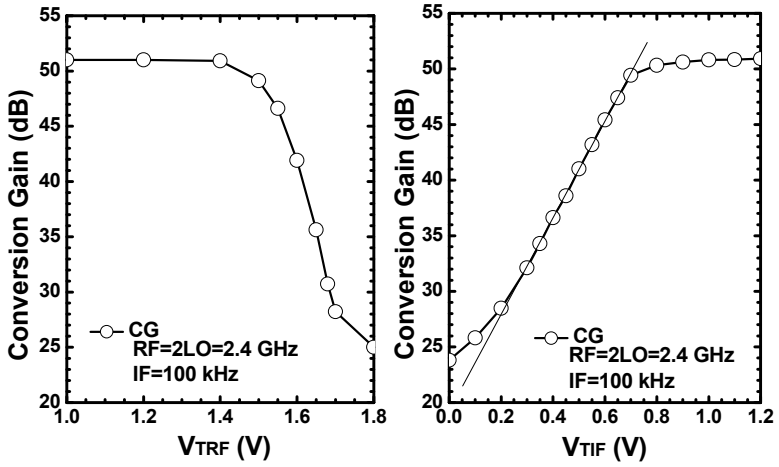
(a)



(b)

Fig. 6-46 (a)I/Q waveform at RF=2.4001 GHz, LO=1.2 GHz (b) amplitude imbalance and phase error.

Fig. 6-47(a) shows the CG as a function of the LNA RF tuning voltage (V_{TRF}) while Fig. 6-47(b) indicates the CG with respect to the VGA IF tuning voltage (V_{TIF}). A tuning range of around 20 dB is achieved by each RF/IF tuning scheme. Fig. 6-48 shows the power performance, including IP_{1dB}, IIP_3, IIP_2, at different gain conditions by RF gain tuning.



(a) (b)

Fig. 6-47 Conversion gain with respect to (a) RF tuning voltage (V_{TRF}) (b) IF tuning voltage (V_{TIF}).

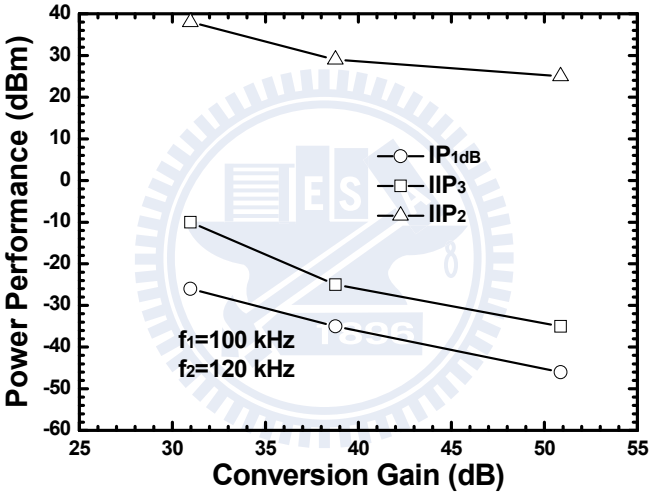


Fig. 6-48 Power performance (including IP_{1dB}, IIP_3 and IIP_2).

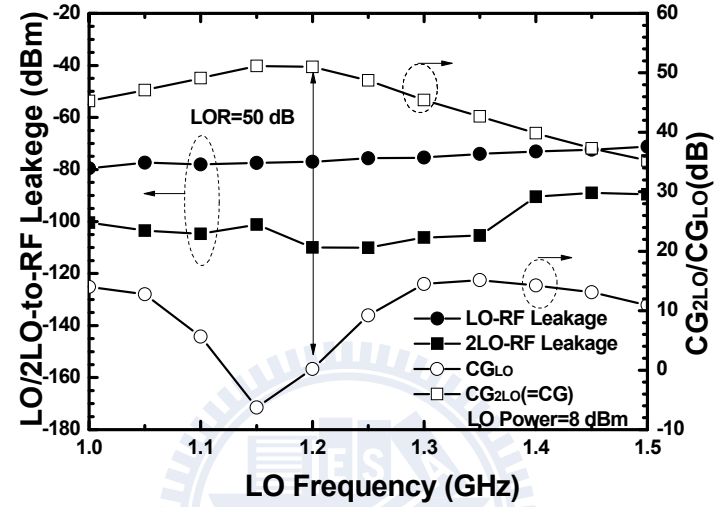
As shown in Fig. 6-49(a), the LO/2LO-to-RF leakage is less than −77/−105 dBm when the LO frequency ranges from 2.5 to 3.2 GHz. The worst-case dc offset due to LO/2LO self-mixing is calculated following [104]

$$\begin{cases} V_{DC-offset(due\ to\ LO)} = V_{LO-LEA} \cdot CG_{\mathrm{LO}} \\ V_{DC-offset(due\ to\ 2LO)} = V_{2LO-LEA} \cdot CG_{2\mathrm{LO}} \end{cases}. \tag{6.33}$$

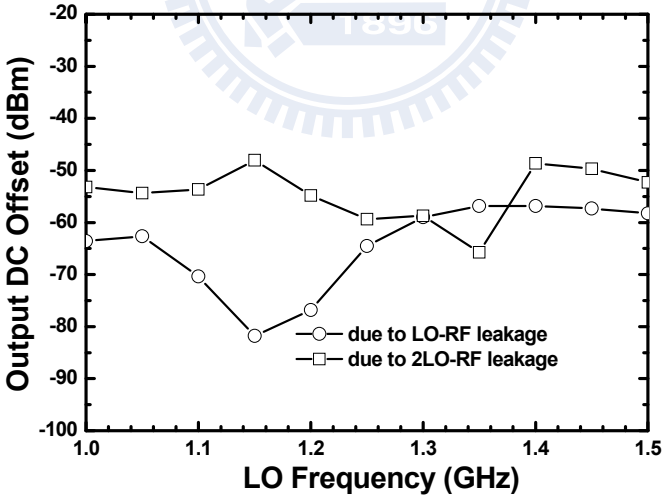
where $V_{LO\text{-}LEA}/V_{2LO\text{-}LEA}$ represents the observed LO/2LO leakage at the RF port and CG_{LO}/CG_{2LO} stands for the conversion gain of a mixer when input signal at LO/2LO

frequency is applied. Here, CG_{2LO}=CG for an SH-DCR.

Thus, the dc offset due to self-mixing is strongly reduced for an SHM and 50 dB LOR at LO=1.2 GHz is obtained, as shown in Fig. 6-49(a). The dc offset due to LO/2LO is drawn in Fig. 6-49(b). That is, an overall worst-case dc offset of 0.44 mV appears at the output. The input return loss is better than 10 dB from 2.1 to 2.6 GHz.



(a)



(b)

Fig. 6-49 (a) LO/2LO-to-RF leakage (b) equivalent output dc offset while the LO power is 8 dBm.

The circuit performance is summarized and compared with state-of-the-art SH-DCRs in TABLE. 6.3 [38], [41]-[42], [103].

TABLE. 6.3 PERFORMANCE COMPARISONS OF SH-DCRS

Reference	[41]	[103]	[42]	[38]	This Work
Topology (I) quadrature RF and LO (II) differential RF and octet-phase LO	Active Stacked-LO (II)	Active Top-LO (II)	Passive Parallel Stacked-LO (No Q-path output)	Active Top-LO (I)	Active Top-LO (w/ BJT core) (II)
RF Frequency (GHz)	2	2	2.2	5-6	2.4
Conversion Gain (dB)	19.2	20 (1 MΩ load)	4.5	26.2	51(1 MΩ load) 31 @ low-gain mode
LO Power (dBm)	>12[a]	3[a]	−18[a]	15.5	8
Noise Figure (dB)	7.8	8.5	11	7.2/5.2[b]	3
Flicker Noise Corner (kHz)	N/R	100	100	3000	<30
IIP_3 (dBm)	−3	4 (50 Ω load)	0	−12.5	−30 (1 MΩ load) −10 @ low-gain mode
IIP_2 (dBm)	35	41 (50 Ω load)	35	N/R	25 (1 MΩ load) 38 @ low-gain mode
DC Offset (mV)	N/R	9	0.7	0.002	0.44
Supply Voltage (V)	3.3	1.8	1.2	1	1.8
Power Dissipation (mW) (excluding LO generator)	18.5	13.32 (LO generator: 10.8)	7.2 (LO generator:5.5)	45.5	9
Technology	0.5μm SiGe HBT	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS

[a] LO buffer is employed

[b] After inductively coupled plasma (ICP) post process

A MOS active mixer has typically over 1-MHz flicker noise corner [38]. Besides, even though only quadrature LO signals are required, the LO power is still high because of the MOS switching core. A separate bias of the mixer core and the RF g_m

stage is applied in [103]. PMOS devices with lower flicker noise property and a lower dc current flowing into the mixer core result in a lower flicker noise leaking to IF output [103]. On the contrary, a g_m stage biased at a higher current can maintain sufficient linearity and noise figure of the active mixer. Passive mixer realization is an alternative for low flicker noise performance [42] but the conversion loss of the passive mixer raises the NF floor if the preceding LNA does not have sufficient gain. The flicker noise problem can be avoided using SiGe HBT technology [41] or using V-NPN BJTs in low-cost CMOS process because of the device nature. However, the LO power requirement of this work is 4-dB lower than that in reference [41], even though the top-LO SHM in this work inherently requires 3-dB more LO power than the stacked-LO SHM in reference [41]. That is, the passive loss of the proposed octet-phase generator is very low.

6.4.3 Comparison of the Demonstrated 2.4-GHz Direct-Conversion Receivers

TABLE. 6.4 shows the performance comparison of 0.18-μm CMOS 2.4-GHz DCRs using passive mixer (in Section 6.3) and V-NPN BJT Gilbert mixer with inductive peaking technique (in Section 6.4.1) and a V-NPN BJT sub-harmonic Gilbert mixer (in Section 6.4.2).

Similar conversion gain of around 50 dB, NF of around 3dB, and flicker noise corner of below 100 kHz are achieved by the three implementations at similar dc power dissipation of below 9 mW. The fundamental V-NPN BJT Gilbert mixer with inductive peaking technique requires only −3 dBm LO power even though the $f_{LO}>f_T$. Besides, the passive mixer with off-overlap biasing has lower flicker noise contribution at the cost of higher LO power. However, the design of the input impedance of the TIA can improve the conversion gain and also the flicker noise

performance. On the other hand, even though the LO power of the BJT SHM requires 8 dBm, which is the same as that of the passive mixer.

The passive mixer has lower toleration of LO amplitude imbalance. Thus, any amplitude/phase imbalance degrades the isolation property, output I/Q accuracy and also the dc offset due to LO self-mixing. Thus, the passive mixer has relative higher dc offset due to self-mixing (if no additional offset cancellation circuit is applied). The DCR with SHMs has the lowest noise figure and the flicker noise corner of the three implementations at the cost of a large LO power and a narrower I/Q tolerable RF bandwidth.

TABLE. 6.4 PERFORMANCE COMPARISON OF DEMONSTRATED 2.4-GHZ DCRS

Topology	Fundamental Passive Mixer	Fundamental V-NPN BJT Mixer	Sub-Harmonic V-NPN BJT Mixer
RF Frequency (GHz)	2.4	2.4	2.4
Conversion Gain (dB)	49	51	51
LO Power (dBm)	8	-3	8
Noise Figure (dB)	3.7	3.2	3
Flicker Noise Corner (kHz)	~70	70	<30
IIP_3 (dBm)	-35	-32	-30
IIP_2(dBm)	20	22	25
DC Offset (mV)	26	10	0.44
Amp./Phase I/Q Imbalance @ RF=2.4 GHz	0.13 dB/1.03^o	0.077dB/0.04^o	0.04dB/0.07^o
I/Q (±0.5dB/±1°) Tolerable RF Bandwidth	>1200 MHz (1.8-3GHz)	>1200 MHz (1.8-3GHz)	250 MHz (2.35-2.6GHz)
Supply Voltage (V)	1.8	1.8	1.8
Power Dissipation (mW)	8.5	8.1	9
Technology	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS

6.5 SUB-HARMONIC RECEIVER WITH TUNABLE-BAND RF LNA AND WIDEBAND LO GENERATOR AT U-NII BANDS

In this section, a low-power tunable-band SH-DCR is demonstrated using 0.18-μm CMOS technology. Our application is focused on the U-NII radio band, consisting of three frequency bands of 100 MHz each in the 5 GHz band: 5.15-5.25 GHz (for indoor use only), 5.25-5.35 GHz and 5.725-5.825 GHz. Although the LNA has a low transconductance gain (g_m) due to its low dc current, its high load resistance (high quality factor Q) provides sufficient voltage gain for a better NF of the whole receiver at the cost of the RF bandwidth. In addition, a narrower RF bandwidth results in little received noise and interference from other channels or other communication systems. Thus, a tunable/switchable narrow-band LNA has better gain/noise performance than an LNA with a wideband design at a given power consumption. As a result, a two-stage LNA with tunable loads, including the first-stage LC tank and the second-stage transformer load, is employed.

A DCR is still chosen in this work. The dc offset, 1/f noise and IIP2 problems are the primary issues for such systems instead of the image and spurious problems of non-zero-IF architectures. An SHM is chosen for a low output dc offset due to LO self-mixing because of the additional LO rejection [41]. In addition, MOS switching cores are directly replaced by V-NPN BJTs, available in a standard 0.18-μm CMOS process and have the 1/*f* noise corner of below 1 kHz [49]-[50]. Further, an LC filter is applied at the common emitter node to greatly improve the IIP_2 performance [108]. Moreover, to overcome the low f_T of V-NPN BJTs, using both resonance inductors (at mixer LO port and the LC filter) and sub-harmonic mixing structure, the proposed SHM successfully operates at over three times the transistor f_T. On the other hand, a wideband LO octet-phase signal generator is chosen to avoid tuning both RF and LO

bands simultaneously in practical use.

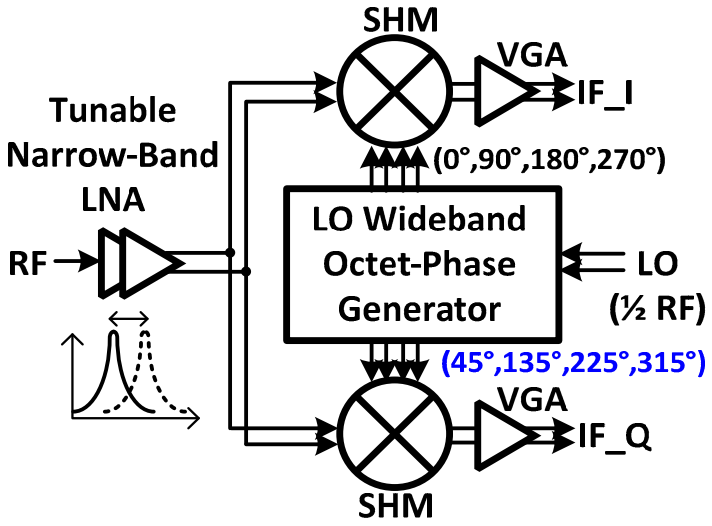


Fig. 6-50 Block diagram of the I/Q SH-DCR with a tunable narrow-band LNA and a wideband LO generator using 0.18-μm CMOS technology.

Since the RF LNA is a tunable-band structure while the mixer and the LO generator are wideband topologies, a tunable narrow-band SH-DCR is proposed to cover whole U-NII bands when the 1-dB RF bandwidth is around 200 MHz. Fig. 6-50 shows the block diagram of the proposed SH-DCR, including a two-stage tunable-band LNA, I/Q SHMs with V-NPN BJT switching core, I/Q VGAs and a wideband LO octet-phase generator.

1) Tunable Band LNA

The impedance of a parallel LC tank with lossy inductor ($sL+R_s$) is

$$Z(s)=\frac{R_s+sL}{1+sCR_s+s^2LC}. \tag{6.34}$$

Typically, the series resistance R_s can be assumed as $R=(\omega/Q)L\equiv\alpha L$, where α is close to a constant, only relating to the geometrical shape (including width, spacing and thickness).

Thus,

$$|Z|_{\max} = \left[1 + (\frac{\omega_0}{\alpha})^2\right] \cdot \alpha L = (1 + Q^2) R_s = R_p \,, \tag{6.35}$$

when $(\omega_0^2 + \alpha^2)LC = 1$ as proved in Appendix E. That is why an LC tank with a lossy inductor is widely approximated as an RLC parallel tank, as shown in Fig. 6-51.

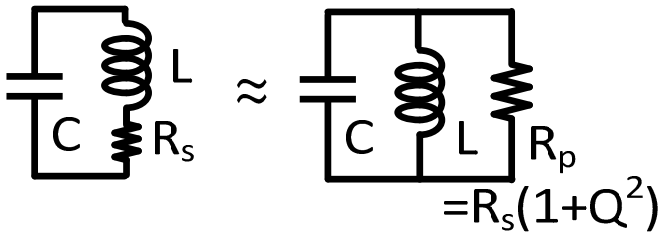


Fig. 6-51 Schematic of an LC tank with a lossy inductor.

Further, in Appendix E, a more general case, *n* stages of RLC tanks in cascade with the same *Q*, is considered for bandwidth. Thus, an *m*-dB bandwidth can be calculated as $k\omega_0/Q$, where $k = \sqrt{10^{m/10n} - 1}$, which is defined in Appendix E. If the target bandwidth boundaries are ω_L and ω_H, the required *Q* can be obtained by

$$Q = \frac{k\omega_0}{\Delta\omega} = k\frac{\sqrt{\omega_H \omega_L}}{\omega_H - \omega_L}, \tag{6.36}$$

where the center frequency is $\sqrt{\omega_H \omega_L}$, as also shown in Appendix E.

By Eqn. (6.36), to achieve a 3-dB bandwidth covering the whole U-NII band (5.15-5.825 GHz), the *Q* should be lower than 8.11. More strictly, if the gain flatness is required to be within 1 dB covering the whole band, the *Q* should be reduced to below 4.13. On the other hand, if multiple tanks are in cascade and located at the same frequency, the greater number of stages in cascade results in a smaller *k* and thus a narrower bandwidth as also described in Fig. 6-52(a). Either a *Q* value reduction or a separation of resonance frequencies can fulfill the original bandwidth requirement as illustrated in Fig. 6-52(b) and Fig. 6-52(c), respectively. However, the gain

degrades when using either method.

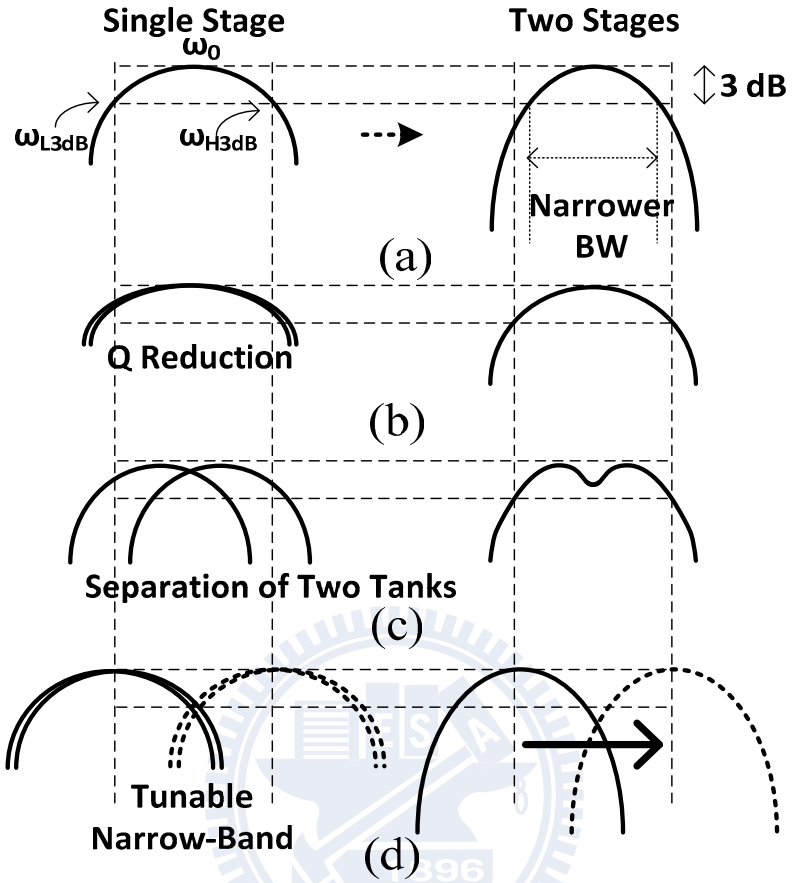


Fig. 6-52 (a)Frequency response of the single/two stage(s) of LC resonator(s) (b) Q reduction for each tank (c) wideband response with separation of tanks (d) tunable narrow-band response.

For the requirements of low power, high gain, low noise and RF bandwidth of 5.15-5.825 GHz in this work, a two-stage cascode LNA with a tunable RF band is chosen. A two-stage LNA is required for a sufficient gain to suppress the NF of the following SHMs at a low dc current consumption. The center frequencies of the two stages are set the same and vary together as described in Fig. 6-52(d). Thus, a higher gain is obtained when compared with the wideband solutions, especially in a low-power condition. Since the IF bandwidth is much lower than the RF bandwidth, the frequency response of the narrow RF tank is still nearly constant within the IF bandwidth (<50 MHz).

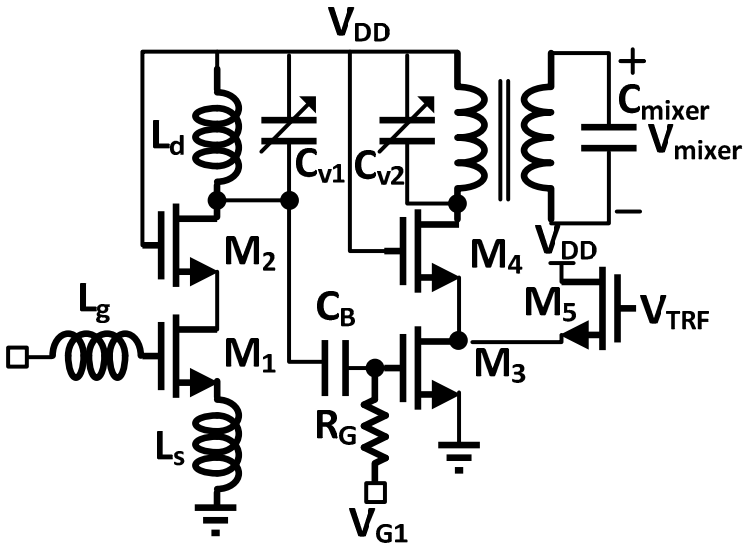


Fig. 6-53 Two-stage LNA with a tunable first-stage LC tank and a tunable second-stage transformer

The schematic of a two-stage cascode LNA is shown in Fig. 6-53. An LC tank is used at the load of the first stage and a transformer at the second stage. A series inductor L_g is sufficient for an input matching covering 5-6 GHz. Further, a gain tuning transistor (M_T) is in parallel with the cascode transistor in the second stage to reduce the gain when a large RF signal is applied.

The frequency tuning capability of both an LC tank and a transformer load with a varactor are fully discussed as follows.

Assume the higher/lower RF bandwidth boundaries (ω_H/ω_L) are 5.825/5.15 GHz, respectively. Thus, the first-stage LC tank follows

$$\begin{cases} L_d C_{\min} = 1/\omega_H^2 = 1/(2\pi \times 5.825 \times 10^9)^2 \\ L_d C_{\max} = 1/\omega_L^2 = 1/(2\pi \times 5.15 \times 10^9)^2 \end{cases}. \tag{6.37}$$

As a result,

$$\frac{C_{\max}}{C_{\min}} = (\frac{\omega_H}{\omega_L})^2 = (\frac{5.815}{5.15})^2 = 1.28 . \tag{6.38}$$

However, $C(V) = C_{const} + C_V(V)$ where C_{const} is a constant capacitance including device and substrate capacitances, and $C_V(V)$ is a capacitance of a varactor

ranging from $C_{V,\min}$ to $C_{V,\max}$. Typically, in CMOS process, a MOS varactor $C_V(V)$ operating in an accumulation mode has a tuning ratio ($C_{V,\max}/C_{V,\min}$) of around 2.5. Moreover, if the varactor capacitance ratio C_r is defined as $C_{V,\min}/C_{const}$,

$$\frac{C_{\max}}{C_{\min}} = \frac{C_{const} + C_{V,\max}}{C_{const} + C_{V,\min}} = \frac{1 + 2.5 \times C_r}{1 + C_r} > 1.28 . \tag{6.39}$$

That is, C_r should be set above 0.23 to cover the whole U-NII band. The C_{const} can be changed by modifying the size of the cascode transistor, the following common-source transistor, and the dc blocking capacitance. Thus, in this work, C_{const} is tuned to 0.4 pF and C_r=0.3 and C_{max}/C_{min} are around 0.7/0.52 pF, respectively. Further,

$$L_d = 1/(\omega_H^2 C_{\min}) = 1/[\omega_H^2 (1 + C_r) C_{const}] . \tag{6.40}$$

Thus, the calculated L_d is around 1.44 nH. Finally, the used inductor in the first-stage LNA has an inductance of 1.42 nH, Q of 11, and f_{Qmax}/f_{res} of 13.5/30 GHz, respectively.

On the other hand, when considering a transformer, if varactors are employed at both nodes, and $L_1C_{1(V)}$=$L_2C_{2(V)}$ is still fulfilled, *i.e.*,

$$\frac{\omega_H^2}{\omega_L^2} = \frac{C_{1,\max}}{C_{1,\min}} = \frac{C_{2,\max}}{C_{2,\min}} , \tag{6.41}$$

which is the same as the result of a parallel LC tank because the peak frequency ω_{pk} is proportional to tank resonance frequency ω_0 ($\omega_{pk} = \omega_0 / \sqrt{1+k}$).

If only C_1 can be tuned, assuming $L_2C_2 = 1/\omega_0^2$ yields,

$$\frac{\omega_H^2}{\omega_L^2} = \left(\frac{C_{1,\max}}{C_{1,\min}}\right)^{1/2} , \tag{6.42}$$

which is derived in Appendix F.

That is, the tuning capability of a transformer with only one varactor on either side is half of a parallel LC tank or a transformer with varactor loads at both sides. Thus, a higher C_r should be applied to cover the desired frequency range.

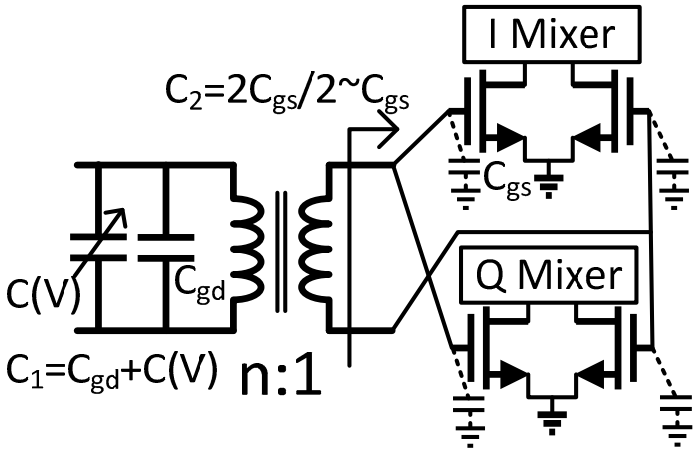


Fig. 6-54 Schematic of the LNA transformer with an input varactor and output pure capacitance load.

As shown in Fig. 6-54, C_1 mainly consists of the varactor and the C_{gd} of the cascode device in the second-stage LNA. On the other hand, at the output stage, the differential capacitances of the transconductance stage of the mixers are in series but I and Q mixers are in parallel. Therefore, the differential load capacitance C_2 is approximately equal to C_{gs} of a single transistor.

Similar to an LC tank, the decision of the varactor value can also be applied. Thus,

$$\frac{C_{1,\max}}{C_{1,\min}} = \frac{C_{1,const} + C_{V1,\max}}{C_{1,const} + C_{V1,\min}} = \frac{1 + 2.5 \times C_r}{1 + C_r} = 1.637 \,. \qquad (6.43)$$

Thus, C_r should be larger than 0.417 and is set to 0.5 in this work. If $C_{1,\text{const}}$ is set to 0.3 pF, the $C_{1,\max}$/ $C_{1,\min}$=1.05/0.45 pF, respectively. $C_{1,\text{center}}=(C_{1,\max}\times C_{1,\min})^{1/2}$= 0.687 pF while $C_2=C_{gs}$ =0.3 pF. The best transformer turn ratio n is $(0.3/0.687)^{1/2}$ $= 0.66 \approx 2/3$. Thus, a 2:3 planar single-to- differential transformer is chosen. The applied 2:3 transformer load has a line width of 9 μm, a line spacing of 2 μm and an outer diameter of 190 μm.

2) Sub-Harmonic Mixer

An SHM has better dc-offset output than a fundamental mixer because of the additional LO rejection, inherently [41]. A top-LO SHM is applied because of a lower voltage headroom requirement and a better isolation when compared with a stacked-LO SHM at the cost of a larger LO power requirement. Additionally, parasitic V-NPN BJTs, obtained in deep-n-well CMOS process without extra mask [50], is applied at the mixer switching core to directly eliminate the 1/*f* noise problem, as shown in Fig. 6. Since the V-NPN BJT has a low f_T of around 2 GHz, a receiver covering U-NII bands is rarely achievable originally. However, using both resonance inductors (at LO differential base nodes and common emitter nodes) and the sub-harmonic operation, an SHM operated at three times the transistor f_T is achieved in this work. Four differential inductors are in parallel with the base nodes of the switching core of the I/Q mixers and the output nodes of the LO generator to reduce both the conversion loss of the switching operation and the LO loss of the LO generator simultaneously. The details about the LO loss reduction will be discussed later.

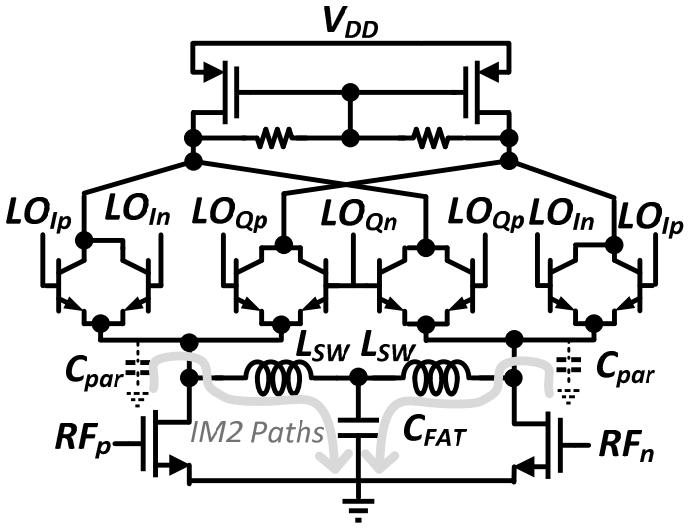


Fig. 6-55 Top-LO sub-harmonic Gilbert mixer with vertical-NPN BJT in the switching core while an LC network is applied for an IM2 improvement.

On the other hand, self-mixing, transconductor nonlinearity, switching pair nonlinearity, and mismatch in load resistors are the main reasons for the IIP_2 degradation in downconversion mixers [109]. Self-mixing of RF signals due to coupling into the LO port can be significantly reduced by means of layout concerns, *e.g.*, metal lines carrying RF and LO signals should never cross each other, or at a minimum, should be kept orthogonal. Further, employing highly linear polysilicon resistors makes the effect of load resistors negligible. Device nonlinearity of RF transconductor generates the second-order inter-modulation distortion (IM_2) components. A perfectly matched switching stage upconverts the input differential baseband spectrum at mixer output. However, the RF IM_2 components leak into the IF output by the low-frequency gain of the switching pairs if mismatches in the switching stage devices are considered. In principle, low-frequency RF IM_2 components can be filtered out by AC coupling the switching stage. However, the additional power consumption of separately biasing the input stage and mixer core is not desirable in our low-power application.

In this work, an LC filter (L_{SW}-C_{FAT}-L_{SW}) is applied to filter out the IM_2 current in RF transconductor [108], as shown in Fig. 6-55, since the shunt inductor L_{SW} has a relatively low impedance at low frequencies and the IM_2 current can be directly shorted to ground by the by-pass capacitor (C_{FAT}) applied at the center-tapped node of the symmetric inductor. It is noteworthy that C_{FAT} should be large enough for an IIP_2 improvement. In this work, C_{FAT} is 15 pF. When compared to the tens of MHz RF applications, the IIP_2 value drops dramatically due to the parasitic capacitance C_{par} at high frequencies [108]. The L_{SW} in the LC filter can also resonate out the parasitic C_{par}. Thus, both the high-frequency gain and the IIP_2 performance of the Gilbert mixer can be improved.

For a chip area concern, a 3D symmetric inductor realization is used, as described in Section 6.4.1. The symmetrical 3D inductors (effectively 6 turns from metal 6 to metal 1) with 8-μm line width, 2-μm line spacing and 70-μm outer diameter are applied at the LC filters in I/Q mixers and have the differential inductance of 2.4 nH and Q=3.6 at around 5-6 GHz.

3) Wideband LO Octet-Phase Generator

The proposed wideband octet-phase signal generator used at the LO port of the SHM, shown in Fig. 6-56, consists of a differential-type wideband 45° phase shifter [41], [110], two differential buffer amplifiers and two PPFs with symmetrical inductor loads.

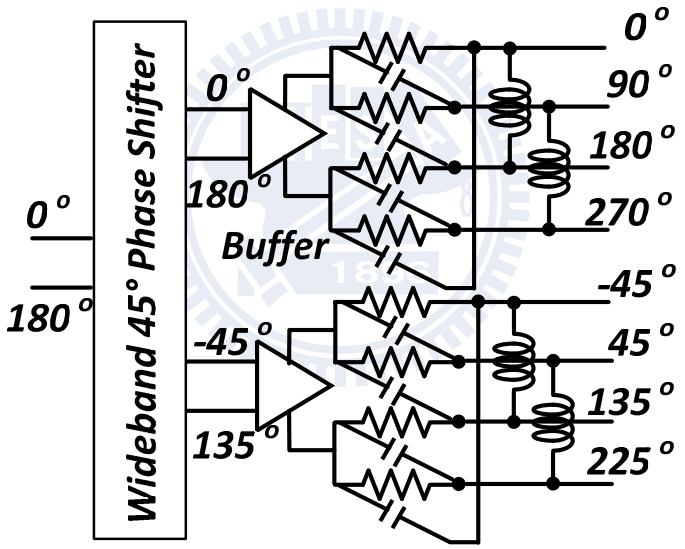
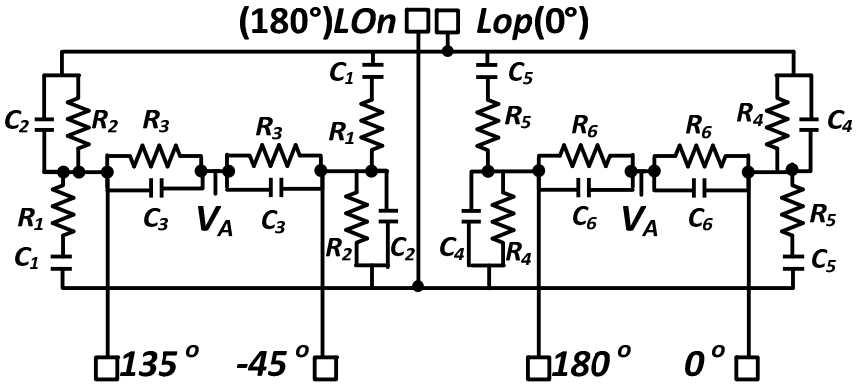


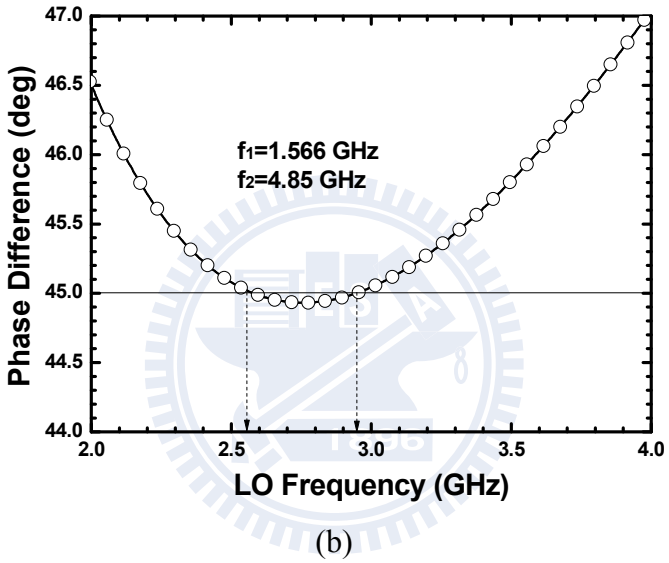
Fig. 6-56 Block diagram of an LC octet-phase generator including a wideband 45° phase shifter, cross-coupled buffer amplifiers and single-stage PPF with resonance inductors.

The LO amplitude/phase should be very accurate covering around 2.5-3 GHz (half of U-NII band frequency). A first-order RC phase shifter has the perfect 45° phase shift only at a single frequency. Further, a tunable version of the phase shifter using varactors is applicable but tunable narrow-band structures of both RF and LO parts lead to much inconvenience in controlling both ends under precise conditions in practical use. Thus, a second-order RC phase shifter is employed to cover a given

bandwidth without tuning.



(a)



(b)

Fig. 6-57 (a) Schematic of a differential-type wideband 45° phase shifter (b) phase difference shifter with respect to frequency.

The schematic of the phase shifter is shown in Fig. 6-57(a) and the RC relations are summarized as follows.

$$\begin{cases} R_1C_1 = R_2C_2 = R_3C_3 = 1/(2\pi f_1) \\ R_4C_4 = R_5C_5 = R_6C_6 = 1/(2\pi f_2) \\ R_2 = abR_1, R_3 = bR_1 \\ R_4 = abR_5, R_6 = bR_5 \end{cases} . \tag{6.44}$$

The output voltage of the phase shifter can be expressed as

$$V_{oi} = (-1)^i \frac{V}{a+1} \frac{1-F_i^2 + jF_i(2-ab)}{1-F_i^2 + jF_i(2+\frac{ab}{a+1})}, \tag{6.45}$$

where $F_i = f/f_i$, i=1 or 2.

To obtain balanced amplitudes of all nodes at all frequencies, b=4(a+1)/a^2 should be chosen and the voltage loss can be re-expressed as

$$V_{oi} = (-1)^i \frac{V}{a+1} \frac{1-F_i^2 - jkF_i}{1-F_i^2 + jkF_i} \tag{6.46}$$

where k=2+4/a, i=1 or 2.

As a result,

$$\begin{cases} |V_{o1}| = |V_{o2}| = \dfrac{V}{a+1} \\ \Delta\phi = \phi_2 - \phi_1 = \pi - 2\tan^{-1}(\dfrac{kF_2}{1-F_2^2}) + 2\tan^{-1}(\dfrac{kF_1}{1-F_1^2}) \end{cases}. \tag{6.47}$$

According to Eqn. (6.47), the voltage loss only depends on the coefficient a, and is independent of frequency. A smaller a results in lower loss; thus, a=1 (b=8) is chosen in this work to achieve a voltage loss of 6 dB. Besides, the phase error varies as the two center frequencies f_1 and f_2. Thus, f_1/f_2 are set at 1.566/4.85 GHz, respectively, for the perfect 45° LO phase difference achieved at around 2.55 and 2.95 GHz, as shown in Fig. 6-57(b). Thus, ideally phase error of below ±0.1° is achieved covering the LO frequency from 2.5 to 3 GHz (*i.e.*, 2LO frequency of 5-6 GHz).

The amplitude/phase relationships derived above hold only when the load impedance is infinity. Thus, when a PPF is cascaded after the phase shifter for quadrature signal generation, the low input impedance of the PPF results in a significant phase error. Conversely, if the resistance is set high (e.g., over kΩ), *i.e.*, the capacitance of the PPF should be small because ω_{LO}=1/RC, meaning that the voltage loss due the output capacitance loadings will be unacceptable [95]. As a result, an

inter-stage buffer amplifier is required to provide a high load impedance of the phase shifter and a low source impedance of the following PPF. Parallel inductors resonate the capacitance including the loading mixer capacitances and PPF capacitance at ω_{LO}, resulting in a higher output impedance and reducing the PPF loss.

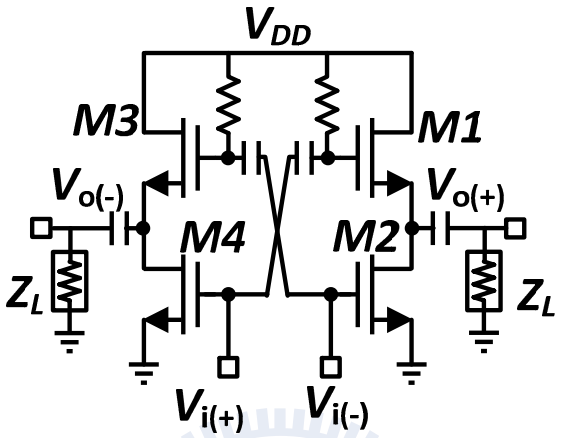


Fig. 6-58 Cross-coupled differential voltage buffer applied in the LO generator.

Fig. 6-58 shows the schematic of the cross-coupled differential buffer amplifier [102]. The voltage gain is described as

$$\begin{cases} v_{o(+)} = v_{i(+)} \dfrac{g_{m1} Z_L}{1+g_{m1} Z_L} + v_{i(-)} \left[-g_{m2} \left(\dfrac{1}{g_{m1}} \| Z_L \right) \right] \\ \qquad = \dfrac{Z_L}{1+g_{m1} Z_L} \left[g_{m1} v_{i(+)} - g_{m2} v_{i(-)} \right] \\ v_{o(-)} = -\dfrac{Z_L}{1+g_{m1} Z_L} \left[g_{m2} v_{i(+)} - g_{m1} v_{i(-)} \right] \end{cases} \tag{6.48}$$

where g_{m1} is the transconductance of the M_1/M_3, g_{m2} is the transconductance of M_2/M_4, and Z_L is the load impedance of the following stage.

Ideally, the voltage gain $(\Delta V_o / \Delta V_i)$ is $2g_m Z_L / (1+g_m Z_L)$ if $g_m = g_{m1} = g_{m2}$. When compared with a single common-source amplifier with a diode-connected load or a common-drain amplifier, the cross-coupled amplifier has twice the voltage gain and can also reduce the amplitude/phase error of the input signals. If input differential

signals have amplitude imbalance and phase error, *i.e.*, $v_{-}(i) = -E_r v_{+}(i)$, where E_r is a complex value near to unity. The ratio of the differential outputs may thus be expressed as

$$\frac{v_{-(o)}}{v_{+(o)}} = \frac{g_{m1}v_{-(i)} - g_{m2}v_{+(i)}}{g_{m1}v_{+(i)} - g_{m2}v_{-(i)}} = -\frac{g_{m1}E_r + g_{m2}}{g_{m1} + g_{m2}E_r} \quad . \qquad (6.49)$$
$$= -1 \ \ (\text{if } g_{m1} = g_{m2})$$

That is, the output voltages are perfectly differential if g_{m1}=g_{m2} even though the input signals have certain amplitude/phase mismatches.

As mentioned, the capacitance loadings (mixers) of the PPF result in incredible loss. The peaking inductors are in parallel with the SHM cores. The LO base 3D inductor with 11 turns is used with 8-μm line width, 2-μm line spacing and an outer diameter of only 100 μm. The differential inductance is 12 nH and quality factor is 3.5 at around 2.5~3GHz. By simulation, the placement of the 3D inductor reduces around 3-dB LO power loss when compared with a pure capacitive mixer loads, although the inductor Q is not high.

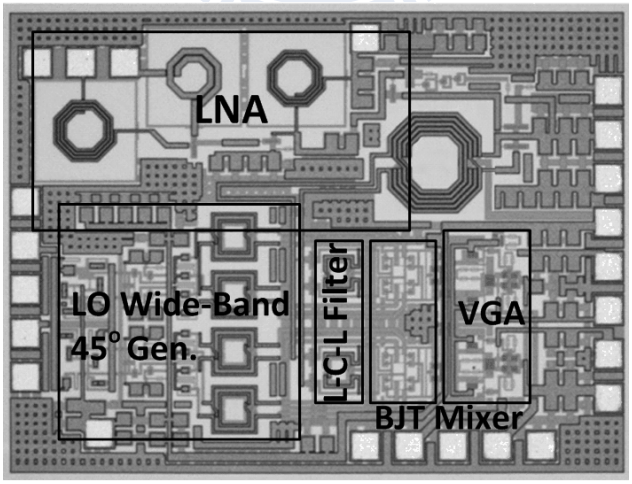


Fig. 6-59 Die photo.

The die photo of the low-power low-noise tunable-band SH-DCR for U-NII bands is shown in Fig. 6-59, and the die size is 1.4×1.05 mm^2. On-wafer measurement facilitates the RF performance. Fig. 6-60 shows the conversion gain (CG) and the NF

as a function of RF frequency while IF=200 kHz. Because of the tunable RF band, two situations with maximum CG at 5.2/5.8 GHz are reported. The 5.2-GHz mode is tested for U-NII-1 band and U-NII-2 band while 5.8-GHz mode is tested for U-NII-3 band. The peak CG at 5.2/5.8 GHz is 48/50 at its corresponding maximum condition, while the minimum NF is 4.5/4.8 dB.

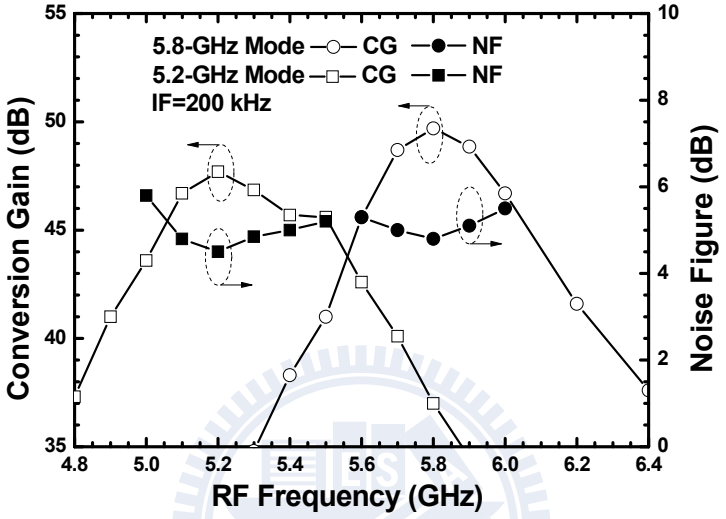


Fig. 6-60 Conversion gain and noise figure with respect to RF frequency.

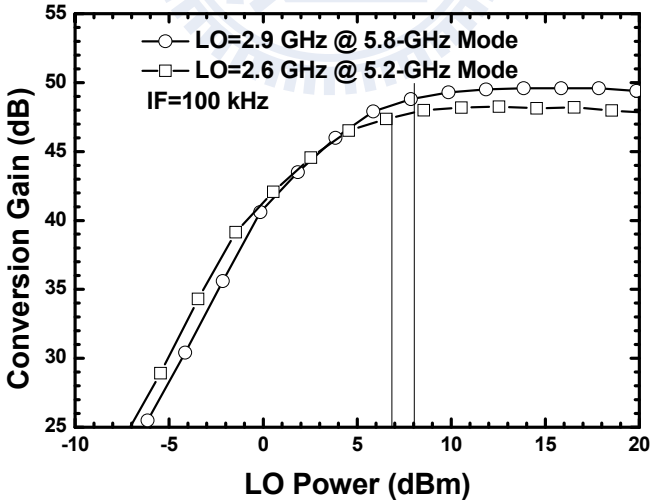


Fig. 6-61 Conversion gain with respect to LO power.

Fig. 6-61 shows the CG with respect to the LO power when RF=5.2002/5.8002 GHz and LO=2.6/2.9 GHz, respectively. 7/8-dBm LO power is applied for all the following measurements.

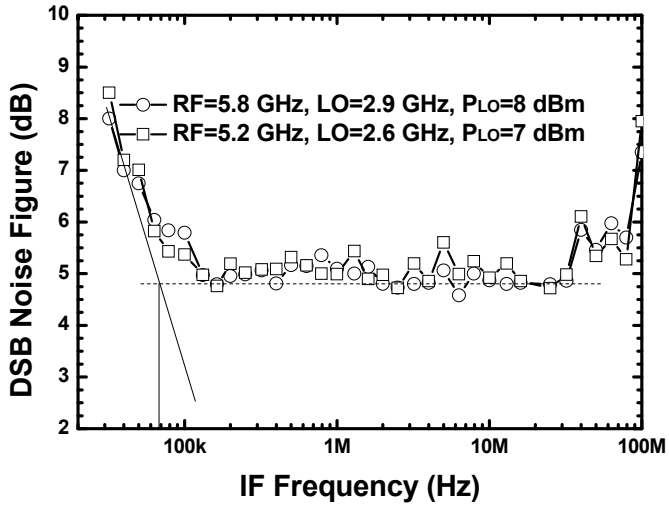


Fig. 6-62 Noise figure with respect to IF frequency.

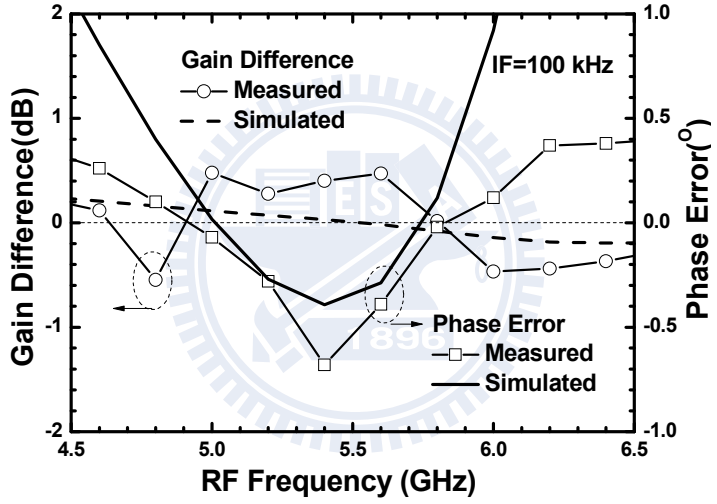
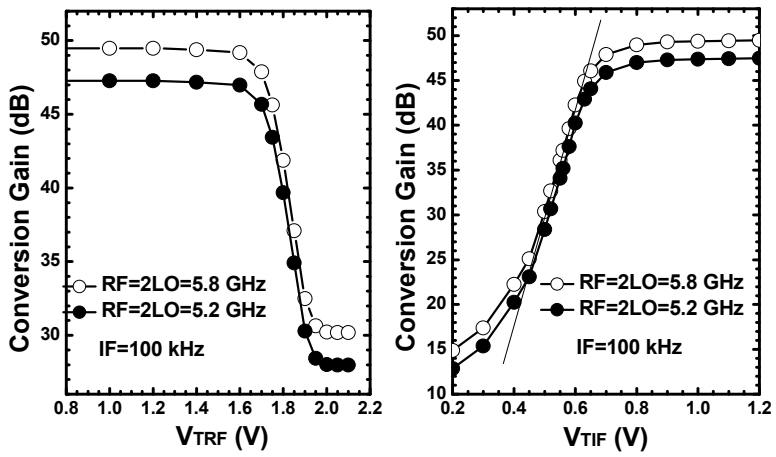


Fig. 6-63 Gain difference and phase error of the IF I/Q outputs.



(a) (b)

Fig. 6-64 Conversion gain with respect to (a) RF tuning voltage (V_{TRF}) (b) IF tuning voltage (V_{TIF}).

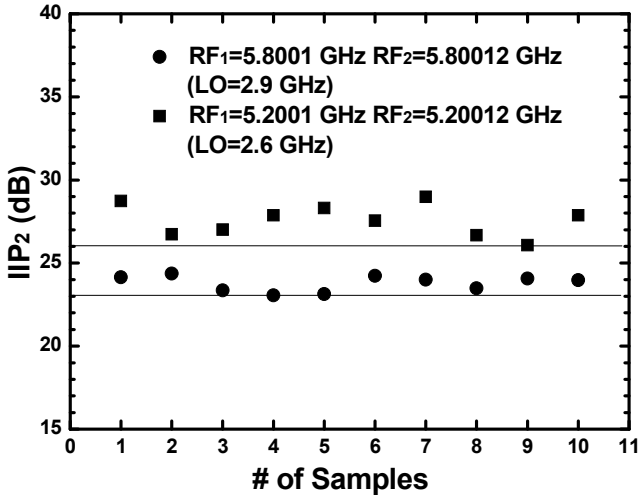
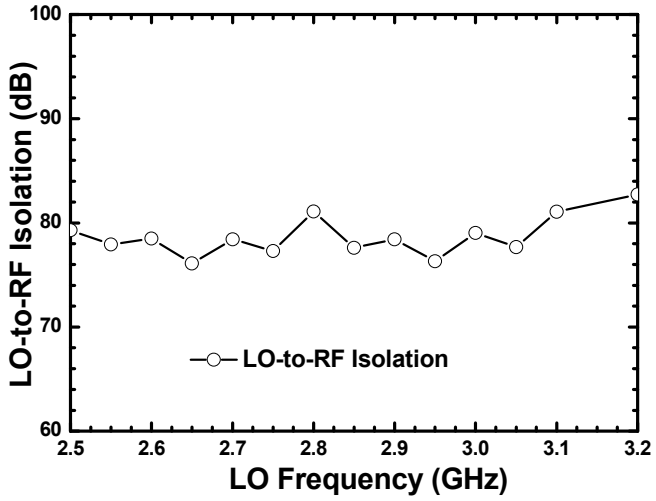


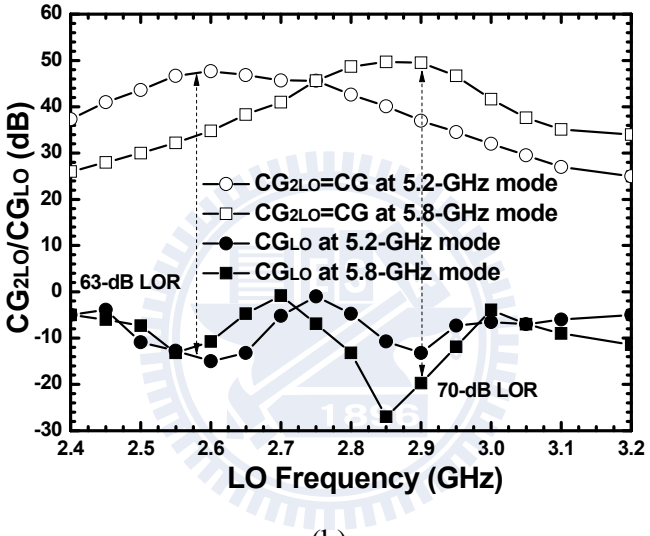
Fig. 6-65 IIP_2 measured by 10 samples.

Fig. 6-62 shows the NF with respect to IF frequency when LO=2.6/2.9 GHz, respectively and the 1/*f* corner is around 70 kHz while the measured IF gain bandwidth is 50 MHz. Fig. 6-63 shows the gain difference and I/Q phase error with respect to RF frequency. The phase/amplitude imbalance are extracted from the IF output waveforms measured by the oscilloscope. The phase error has a bowl shape and is less than±1º within 4.5-6.4 GHz while the amplitude imbalance is less than ±0.6 dB. Fig. 6-64(a) shows the CG as a function of the LNA RF tuning voltage (V_{TRF}) at RF=5.2/5.8 GHz, respectively, while Fig. 6-64(b) indicates the CG with respect to the VGA IF tuning voltage (V_{TIF}). A tuning range exceeding 20 dB is achieved by each RF/IF tuning scheme. Fig. 6-65 shows the IIP_2 of the SH-DCR of 10 samples. The minimum IIP_2 is 18/15 dBm at 5.2/5.8 GHz band, respectively.

The LO-to-RF isolation is over 75 dB while the LO frequency ranging 2.5 to 3.2 GHz as shown in Fig. 6-66(a). As shown in Fig. 6-66(b), the dc offset due to self-mixing is strongly reduced because around 63/70 dB LO rejection is obtained at LO=1/2×RF=2.6/2.9 GHz, respectively. The worst-case dc offset due to LO self-mixing can be calculated using Eqn. (6.33) is around −93 dBm (*i.e.*, 5 μV) at LO near both 2.6/2.9 GHz bands.



(a)



(b)

Fig. 6-66 (a) LO/2LO-to-RF isolation (b) Conversion gain when RF=LO+IF and RF=2LO+IF.

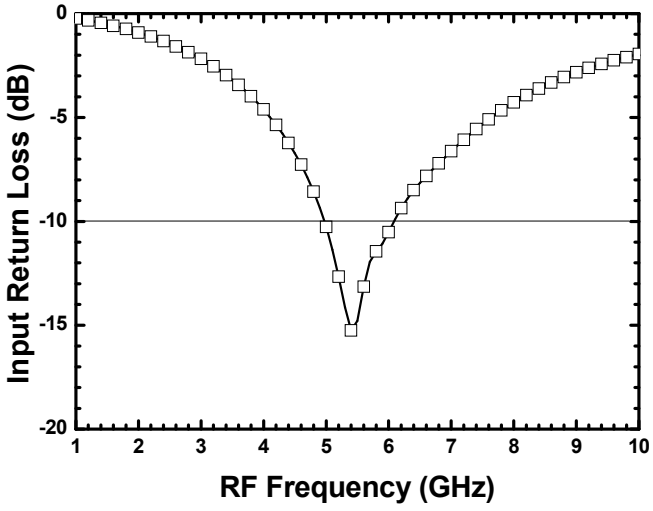


Fig. 6-67 Input return loss.

In addition, the input return loss is less than −10 dB covering 5-6 GHz as shown in Fig. 6-67. Finally, the circuit performance is summarized and compared with the state-of-the-art DCRs in TABLE. 6.5.

TABLE. 6.5 PERFORMANCE COMPARISONS OF SH-DCRS

Reference	[53]	[111]	[112]	[113]	[20]	[38]	This Work
Topology (**F**: fundamental; **SH**: sub-harmonic **P**: Passive, **A**:Active)	**F, P**	**F, P**	**F, A**	**SH, A**	**SH, A**	**SH, A**	**SH, A** (Top-LO, w/ BJT core)
RF Frequency (GHz)	5.15-5.35	5	5.8	5.8	5	5-6	5.2/5.8 (Tunable)
Conversion Gain (dB)	29	26	20.23	13.6	18-20	26.2	48/50 28/30 (low gain)
LO Power (dBm)	0	N/R	-10[a]	0	−5	15.5	7/8
Noise Figure (dB)	5.3	3.5	9.89	9.7	6.8	7.2/5.2[b]	4.5/4.8
Flicker Noise Corner (kHz)	45	200	--	--	--	3000	70
IIP_3 (dBm)	−21	−2	-6.76	N/R	N/R	−12.5	−34/−36 −14/−15(low gain)
IIP_2 (dBm)	13	18-24	21	N/R	29[c]	45.9[c]	26/23
DC Offset (mV)	N/R	0.4[d]	<1	N/R	N/R	0.001[d]	0.005[d]
Supply Voltage (V)	--	1.8	2.8-3.75	2.7	3.3	1	1.8
Power Dissipation (mW)	I_d=17.5 mA	72	64[e]	16.74[c]	52.8	45.5	15.3
Technology	0.18μm CMOS	0.13μm CMOS	SiGe HBT (f_T=47 GHz)	SiGe HBT (f_T=50 GHz)	SiGe HBT (f_T=50 GHz)	0.18μm CMOS	0.18μm CMOS

[a] 2LO input for LO divider

[b] After inductively coupled plasma (ICP) post process

[c] Only mixers

[d] Calculated using $V_{LO\text{-}LEA} \times CG_{LO}$

[e] Only LNA+I/Q mixers (excluding LO divider)

A DCR with fundamental mixers [53], [111]-[112] has simpler downconversion circuit structures than that with SHMs [20], [38], [113] but has a poorer output dc offset due to LO self-mixing. Both passive mixers [53], [111] and BJT active mixers (including using SiGe HBT technology [20], [112]-[113] or V-NPN BJT in standard CMOS process in this work) have excellent 1/*f* noise corner when compared with the pure CMOS active mixers [38]. The proposed tunable-band SH-DCR has less power consumption than the references for similar topologies listed in TABLE. 6.5 but maintains excellent gain/noise performance.

Chapter 7 Conclusion and Future Work

In this dissertation, various methods for different performance improvement are discussed and provided. The high-linearity cross-coupled differential pair employed as the transconductance amplifier in the active Gilbert upconversion mixer in Chapter 2 can also be used as the input transconductance of a baseband amplifier if the linearity performance is a concern.

The phasor expression introduced in Chapter 3 for quadrature signal accuracy analysis is also used for the analysis of the image rejection of the whole receiver in Chapter 5. In addition, the amplitude imbalance toleration of the BJT Gilbert mixer is especially addressed and is very helpful for the constant-quadrature-phase type quadrature generator because the amplitude imbalance can be absorbed by the BJT Gilbert mixers. Thus, the frequency bandwidth with balanced output I/Q signals can be further extended without addtional power loss using other wideband techniques. Besides, the V-NPN BJT available in standard 0.18-μm CMOS process has the same advantage and is used in Chapter 6.

The delay-compensated stacked-LO SHM introduced in Chapter 4 cancels the phase delay between the two cascode Gilbert mixer cores and improves the RF-to-IF isolation and even the dc offset due to self-mixing. Besides, the 2LO isolation is further improved by the four differential-quadrature-phase LO signals are simultaneously fed into the input or output node and can be highly cancelled at either node. This topology can also be implemented for CMOS active or passive mixer. However, this topology cannot cancel the device mismatch. Thus, the pHEMT or mHEMT SHM with delay compensation can still improve the isolation but is limited due to its inherent large device mismatches.

In Chapter 5, single-quadrature-double-quadrature and double-quadrature-

double-quadrature topologies of the dual-conversion low-IF receiver are fully discussed. Thus, the IRR can nearly reach the theoretical limit of the IF poly-phase filter (PPF) even if the LO quadrature imbalance and device mismatches still exist. The dual-band single-quadrature-double-quadrature architecture is also introduced in Chapter 5. However, as mentioned in Section 5.2.1, if a dual-band double-quadrature-double-quadrature architecture needs to be implemented for further improvement on image rejection (both IRR_1 and IRR_2), opposite quadrature RF polarities are required at the two operating frequencies. Thus, a conventional double-quadrature-double-quadrature topology can not be realized as a dual-band variant straightforwardly.

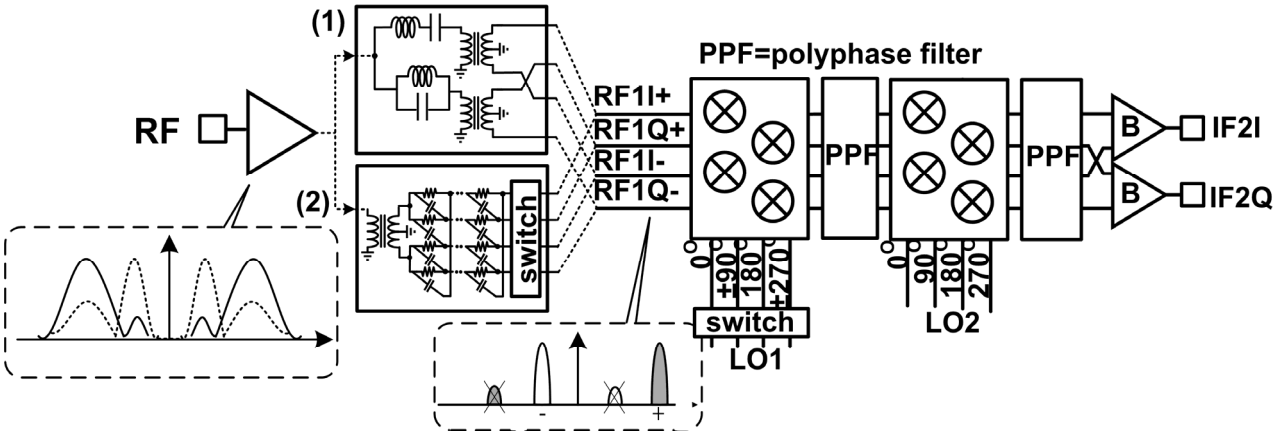


Fig. 7-1 Block diagram of a dual-band double-quadrature-double-quadrature dual-conversion low-IF downconverter.

As shown in Fig. 7-1, a dual-band quadrature RF signal generation with opposite polarities can be achieved by two possible ways:

1) A dual-band LR-CR topology [43] or
2) A multi-stage PPF with different transmission zeros and followed by switch pairs, similar to the LO_1 switch pairs.

When operating at high-frequency band, the polarity is positive but the polarity

is switched to be negative at low-frequency operation mode. Moreover, a switched-band LNA is preferred since any interference (including the image signals) can be pre-filtered out by the LNA. Therefore, the proposed dual-band architecture maintains excellent image-rejection performance by the double-quadrature-double-quadrature topology and the inter-stage PPF.

Chapter 6 provides many design concept in a low-power condition. The power-constraint LNA design with on-chip low-Q inductor is very useful not only in low-cost 0.18-μm CMOS technology but also in advanced 90 nm or even 65 nm technology. The device capacitance (C_{gs}) becomes much smaller due to the size scaling. At the same operating frequency, the required inductance for input matching is incredibly large. Thus, the noise due to the lossy on-chip inductor is much higher than the device noise. The additional parallel capacitance (C_p) plays an important role for noise optimization since the fully integration is the trend when considering yield and cost for mass production. On the other hand, the V-NPN BJT is utilized in Gilbert mixer core and the IF transconductance stage for the ultra low flicker noise and high transconductance gain. The inductive peaking technique applied to the Gilbert mixer for the low-f_T of V-NPN BJTs. However, this technique is also suitable for low-end CMOS process or operating at a very low current density. The inductive peaking at base/gate, described in Section 6.4.1, or the input emitter/source node, described in Section 6.5, can reduce the LO loss and increase the mixer conversion gain.

Besides, the pseudo-four-turn symmetrical 3D inductor for size reduction has good quality factor and self-resonance frequency. For a lower operating frequency, a larger inductance can be obtained by extending the pseudo-four-turn layout to a pseudo-six-turn layout for an inductor with maximum 16 turns, as shown in Fig. 7-2.

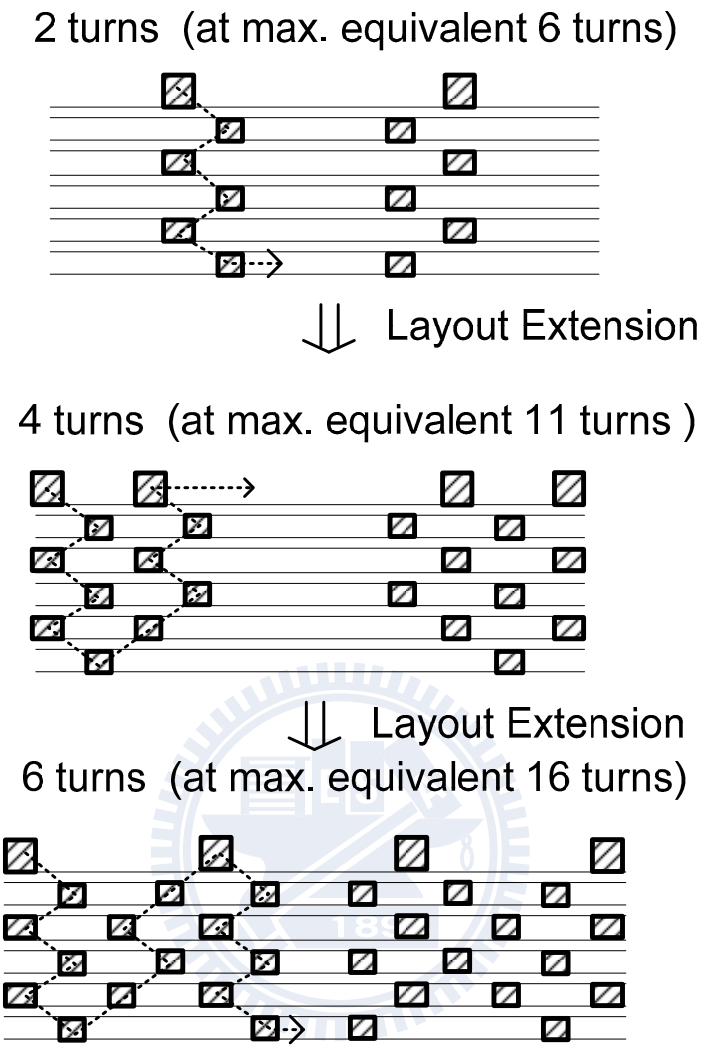


Fig. 7-2 Layout extension of the 3D symmetrical inductor.

The implementations in Chapter 6 do not focus on any specific application. Contrarily, long distance, high data rate (for high quality and accurate control) but still low cost are the main goals. All the proposed techniques and demonstrations are based on these goals. In fact, the best topology chosen and circuit performance can only be achieved when the system specifications are given. Moreover, a fully integration of multi-band and multi- standard is another goal in the future.

Appendix A Derivation of the Transimpedance Gain of a Transformer

The input impedance seen from the primary coil of the transformer (Z_{inL}), shown in Fig.4(a), can be expressed as

$$Z_{inL} = R_1 + sL_1 + sM\, i_2/i_1 = R_1 + sL_1 - \frac{s^2M^2}{R_2 + sL_2 + 1/sC_2}. \tag{A.1}$$

The Z_T of the transformer may thus be calculated as follows.

$$\begin{aligned} Z_T(s) &= \frac{V_o}{I_i} = \frac{i_1}{I_i} \times \frac{i_2}{i_1} \times \frac{V_o}{i_2} \\ &= \frac{1}{1 + sC_1 Z_{inL}} \times \frac{-sM}{R_2 + sL_2 + 1/sC_2} \times \frac{-1}{sC_2} \\ &= \frac{}{(1 + sR_1C_1 + s^2L_1C_1)(1 + sR_2C_2 + s^2L_2C_2) - s^4M^2C_1C_2} \\ &= \frac{sM}{(1 + s\alpha_0L_1C_1 + s^2L_1C_1)(1 + s\alpha_0L_2C_2 + s^2L_2C_2) - s^4k^2L_1C_1L_2C_2} \\ &= \frac{sM}{(1 + \frac{s\alpha_0}{\omega_0^2} + \frac{s^2}{\omega_0^2})(1 + \frac{s\alpha_0}{\omega_0^2}X + \frac{s^2}{\omega_0^2}X) - \frac{s^4k^2}{\omega_0^4}X} \end{aligned} \tag{A.2}$$

where $X = (L_2C_2)/(L_1C_1) = CR/n^2$, $\omega_0 = 1/\sqrt{L_1C_1}$, $R_1 = \alpha_0 L_1$, $R_2 = \alpha_0 L_2$ and $M = k\sqrt{L_1L_2}$.

That is,

$$\begin{aligned} Z_T(\omega) &= \frac{j\omega M}{\left[1 - (\frac{\omega}{\omega_0})^2 + j\frac{\alpha_0}{\omega}(\frac{\omega}{\omega_0})^2\right]\left[1 - (\frac{\omega}{\omega_0})^2 X + j\frac{\alpha_0}{\omega}(\frac{\omega}{\omega_0})^2 X\right] - (\frac{\omega}{\omega_0})^4 k^2 X} \\ &= \frac{j\omega\frac{k}{n}L_1}{\left[1 - W^2 + j\frac{1}{Q}W^2\right]\left[1 - W^2X + j\frac{1}{Q}W^2X\right] - W^4k^2X} \end{aligned}$$

$$= j\omega\frac{k}{n}L_1 \Bigg/ \begin{Bmatrix} \left[(1-W^2)(1-W^2X)-(1/Q^2)W^4X-W^4k^2X\right] \\ +j(W^2/Q)\left[(1-W^2X)+X(1-W^2)\right] \end{Bmatrix}$$

$$= \frac{\omega\frac{k}{n}L_1}{(W^2/Q^2)\left[1+(1-2W^2)X\right]-j\left[1-W^2(X+1)+W^4X(1-k^2-1/Q^2)\right]} \quad \text{(A.3)}$$

$$= \frac{\omega\frac{k}{n}L_1}{\mathrm{Re}(W,X)-j\,\mathrm{Im}(W,X)}$$

where

$$\begin{cases} W=\omega/\omega_0\,, Q=\omega/\alpha_0 \\ \mathrm{Re}(W,X)=(W^2/Q)\left[1+(1-2W^2)X\right] \\ \mathrm{Im}(W,X)=1-W^2(X+1)+W^4X(1-k^2-1/Q^2) \end{cases}.$$

Here, the W and X should be determined to find the $|Z_T(W,X)|_{max}$ at a certain operation frequency ω. In the above equation, $Q=\omega/\alpha_0$ is a constant at target frequency ω. $|Z_T(W,X)|_{max}$ occurs when $\mathrm{Im}(W,X)=0$, *i.e.*,

$$W_{opt}^2=\frac{X+1\pm\sqrt{(X+1)^2-4XP}}{2XP}, \quad \text{(A.4)}$$

where $P=(1-k^2-1/Q^2)$.

Thus, Z_T can be re-written as

$$Z_T=\frac{\omega\frac{k}{n}L_1}{(W^2/Q)\left[1+(1-2W^2)X\right]}. \quad \text{(A.5)}$$
$$=Q\omega\frac{k}{n}L_1/Z(X)$$

where

$$Z(X) = W^2\left[1+(1-2W^2)X\right] = (X+1)W^2 - 2XW^4$$

$$= \frac{X+1\pm\sqrt{(X+1)^2-4XP}}{2XP}(X+1)$$

$$-2X\frac{(X+1)^2+(X+1)^2-4XP\pm 2(X+1)\sqrt{(X+1)^2-4XP}}{(2XP)^2}$$

$$= \frac{1}{2XP}\left\{\begin{array}{l}(X+1)^2\pm(X+1)\sqrt{(X+1)^2-4XP} \\ -\frac{2}{P}\left[(X+1)^2\pm(X+1)\sqrt{(X+1)^2-4XP}-2XP\right]\end{array}\right\}$$

$$= \frac{P-2}{2P^2}\frac{X+1}{X}\left[X+1\pm\sqrt{(X+1)^2-4XP}\right]+\frac{2}{P}$$

$$= \frac{P-2}{2P^2}U(X)+\frac{2}{P}$$

and

$$U(X) = \frac{X+1}{X}\left[X+1\pm\sqrt{(X+1)^2-4XP}\right]$$

$$= \frac{X+1}{X}\left[X+1\pm Y\right] = \frac{(X+1)^2}{X}\pm\frac{X+1}{X}Y$$

with $Y=\sqrt{(X+1)^2-4XP}$.

To determine the optimal X for $Z_T(X)_{max}$, the $Z(X)_{min}$ (or $U(X)_{min}$) should be also achieved. After complete calculation of $U'=0$, where

$$U' = \frac{2(X+1)X-(X+1)^2}{X^2}\pm\left[\frac{X-(X+1)}{X^2}Y+\frac{X+1}{X}Y'\right]$$

$$= \frac{X^2-1}{X^2}\pm\left[\frac{-1}{X^2}Y+\frac{X+1}{X}\frac{X+1-2P}{Y}\right]$$

$$= \frac{X^2-1}{X^2}\pm\frac{1}{X^2Y}\left[-Y^2+X(X+1)(X+1-2P)\right]$$

$$= \frac{X^2-1}{X^2}\pm\frac{1}{X^2Y}\left[-(X+1)^2+4XP+X(X+1)^2-2X(X+1)P\right]$$

$$= \frac{X^2-1}{X^2} \pm \frac{1}{X^2 Y}\left[X(X+1)^2(X-1) - 2XP(X-1) \right] .$$

$$= \frac{X-1}{X^2}\left[X+1 \pm \frac{X}{\sqrt{(X+1)^2-4XP}}\left[(X+1)^2 - 2P \right] \right]$$

The three solutions for $U'=0$ are $1, -(1+P) \pm \sqrt{(1+P)^2-1} (<0)$. Thus, the only one "positive" solution is X=1. Thus, the optimal turn ratio of a transformer $n_{opt}=\sqrt{CR}=\sqrt{C_2/C_1}$ by the definition of $X=(L_2C_2)/(L_1C_1)=CR/n^2$.

Further, substituting X=1 into Eqns (A.4) and (A.5),

$$\begin{cases} W^2_{(X=1)} = \dfrac{1 \pm \sqrt{1-P}}{P} \\ Z_{T(X=1)} = Q\omega \dfrac{k}{n} L_1 \Big/ \left\{ \dfrac{2}{P}\left[(1-\dfrac{2}{P})(1 \pm \sqrt{1-P}) + 1 \right] \right\} \end{cases} . \tag{A.6}$$

However, for a high-coupling condition (P=1–k^2–1/Q^2→0), $\lim_{P\to 0} W^2_{\max H} = (1+\sqrt{1-P})/P \to \infty$ and $\lim_{P\to 0} Z_{T\max H} \to 0$. As a result, W_{maxH} is not an applicable solution and thus W_{maxL}= $(1-\sqrt{1-P})/P$ is typically chosen.

If Q is large enough, *i.e.*, $P=1-k^2$,

$$W^2_{\max L} = \frac{1-\sqrt{1-P}}{P} = \frac{1-\sqrt{1-(1-k^2)}}{1-k^2} = 1/(1+k) \tag{A.7}$$

and

$$\begin{aligned} Z_{\min L} &= 2\frac{(P-2)(1-\sqrt{1-P})+P}{P^2} \\ &= 2\frac{(1-k^2-2)(1-k)+1-k^2}{(1-k^2)^2} \\ &= 2\frac{k(1-k)^2}{(1-k^2)^2} = \frac{2k}{(1+k)^2} \end{aligned} . \tag{A.8}$$

Thus, the maximum Z_T can be re-written as

$$Z_T = \frac{Q}{2n}\omega L_1(1+k)^2 . \tag{A.9}$$

Appendix B Derivation of Conversion Gain with Finite Cut-Off Frequency and Gain Degradation due to LO Loss

The Fourier series coefficient at ω of the switching function $s'(t)$ can be calculated by

$$\begin{aligned} CG &= \frac{1}{T}\int_0^T s'(t)\cos\omega t dt \\ &= \frac{2}{T}\int_{-T/4}^{T/4}(1-e^{-\omega_T(t+T/4)})\cos\omega t dt \\ &= \frac{2}{T}\int_0^{T/2}(1-e^{-\omega_T t})\sin\omega t dt \\ &= \frac{2}{\pi}\left[1-\frac{1}{2}\frac{1+e^{-\omega_T T/2}}{1+(\frac{\omega_T}{\omega_{LO}})^2}\right] = \frac{2}{\pi}\left[1-\frac{1}{2}\frac{1+e^{-\pi f_T'}}{1+(f_T')^2}\right] \end{aligned} \tag{B.1}$$

where $T=2\pi/\omega$ and $f_T' = f_T / f_{LO}$.

On the other hand, the voltage division (VD) due to capacitive loading ($C_L \approx 2C_\pi$) can be expressed as

$$VD_{LO} = \frac{2}{\sqrt{1+(1+2C_\pi/C_n)^2}} \approx \frac{2}{\sqrt{1+\left[1+2g_m R_n / f_T'\right]^2}} \tag{B.2}$$

where $\omega_T \approx g_m / C_\pi$ and $\omega_{LO} = 1/(R_n C_n)$.

As a result, the maximum VD_{LO} is $\sqrt{2}$ (i.e., +3 dB gain) when f_T reaches infinity. Thus, the gain degradation due to LO loss (GD_{LO}) is defined as

$$GD_{LO} = \frac{VD}{VD_{\max}} = \sqrt{\frac{2}{1+\left[1+2g_m R_n/(f_t/f_{LO})\right]^2}}\,. \tag{B.3}$$

Appendix C Derivation of Optimal Inductance for an Inductive Peaking Between LO Poly-Phase Filter and Mixer Core

The load impedance of series *L*-*R* with parallel C_L can be expressed as

$$Z_L = \frac{1}{sC_L + \frac{1}{(s+\omega_0/Q)L}} = \frac{(j\omega+\omega_0/Q)L}{1-\omega^2 C_L L + j\frac{\omega_0}{Q}\omega L C_L} . \quad \text{(C.1)}$$

where $R=\omega_0 L/Q$.

As a result, the *VD* at the output node of the LO poly-phase filter (PPF) is

$$\begin{aligned} VD(\omega_0) &\equiv \frac{Z_L}{Z_L + R_n \,\|\, (1/j\omega_0 C_n)} \\ &= \frac{\omega_0 L(1+j)(1+jQ)}{\omega_0 L(1+j)(1+jQ) + R_n\left[Q + j\omega_0^2 C_L L(1+jQ)\right]} \\ &= \frac{(1+j)(1+jQ)}{(1-AQ) + R_n\frac{Q}{\omega_0 L} + j(A+Q)} \end{aligned} \quad \text{(C.2)}$$

where $\omega_0 = 1/(R_n C_n)$ and $A=1+C_L/C_n$.

Taking the absolute value,

$$\left|VD(\omega_0)\right| = \frac{\sqrt{2(1+Q^2)}}{\sqrt{K - 2\frac{M}{L} + \frac{N}{L^2}}} \quad \text{(C.3)}$$

where

$$\begin{cases} M = \dfrac{QR_n}{\omega_0}\left[QA-1\right] \\ N = \dfrac{Q^2R^2}{\omega_0^2} \\ K = (1+A^2)(1+Q^2) \end{cases} .$$

By setting the first-order differential equation to zero, L_{opt} is obtained

$$L_{opt} = \frac{N}{M} = \frac{R_n}{\omega_0 (A - 1/Q)} = \frac{1}{\omega_0^2 C_n (A - 1/Q)} . \tag{C.4}$$

Substituting Eqn. (C.4) back into Eqn. (C.3),

$$\left| VD_O(\omega_0) \right|_{opt} = \frac{\sqrt{2(1+Q^2)}}{\sqrt{(1+A^2)(1+Q^2) - (QA-1)^2}} = \frac{\sqrt{2(1+Q^2)}}{A+Q} . \tag{C.5}$$

If L reaches infinity (i.e., without inductor), the VD becomes

$$\left| VD(\omega_0) \right| = \frac{2}{\sqrt{1+A^2}} = \frac{2}{\sqrt{1+(1+C_L/C_n)^2}} , \tag{C.6}$$

which is the same as the case of pure capacitive loads in Eqn. (3.24).

Appendix D Derivation of Amplitude/Phase Relations of a Multi-Stage Octet-Phase Poly-Phase Filter

For additional stages, the vector $[a_n, b_n]$ should be obtained first because both *AD* and *PE* can be formulated using it by Eqns. (6.27) and (6.28). As mentioned in Section 6.4.2-2,

$$\begin{bmatrix} a_{n+1} \\ b_{n+1} \end{bmatrix} = X \begin{bmatrix} a_n \\ b_n \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} a_n \\ b_n \end{bmatrix} \tag{D.1}$$

where $n \geq 1$.

The matrix X can be eigendecomposed to $X = VEV^{-1}$

where

$$V = \begin{bmatrix} v_1 & v_2 \\ -v_2 & v_1 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} & \frac{1}{\sqrt{4-2\sqrt{2}}} \\ \frac{-1}{\sqrt{4-2\sqrt{2}}} & \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} \end{bmatrix}, \quad V^{-1} = \begin{bmatrix} v_1 & -v_2 \\ v_2 & v_1 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} & \frac{-1}{\sqrt{4-2\sqrt{2}}} \\ \frac{1}{\sqrt{4-2\sqrt{2}}} & \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} \end{bmatrix},$$

and

$$E = \begin{bmatrix} E_1 & 0 \\ 0 & E_2 \end{bmatrix} = \begin{bmatrix} 2-\sqrt{2} & 0 \\ 0 & 2+\sqrt{2} \end{bmatrix}.$$

Thus,

$$\begin{aligned} \begin{bmatrix} a_{n+1} \\ b_{n+1} \end{bmatrix} = X^n \begin{bmatrix} a_1 \\ b_1 \end{bmatrix} &= \begin{bmatrix} v_1 & v_2 \\ -v_2 & v_1 \end{bmatrix} \begin{bmatrix} E_1^n & 0 \\ 0 & E_2^n \end{bmatrix} \begin{bmatrix} v_1 & -v_2 \\ v_2 & v_1 \end{bmatrix} \begin{bmatrix} a_1 \\ b_1 \end{bmatrix} \\ &= E_2^n \begin{bmatrix} (K^n v_1^2 + v_2^2) & (1-K^n) v_1 v_2 \\ (1-K^n) v_1 v_2 & (K^n v_2^2 + v_1^2) \end{bmatrix} \begin{bmatrix} a_1 \\ b_1 \end{bmatrix} \end{aligned} \tag{D.2}$$

where $K = \frac{2-\sqrt{2}}{2+\sqrt{2}} = 3-2\sqrt{2} < 1$.

When n reaches infinity,

$$\frac{b_\infty}{a_\infty} = \lim_{n\to\infty}\left[\frac{b_{n+1}}{a_{n+1}}\right] = \frac{v_1 v_2 a_1 + v_1^2 b_1}{v_2^2 a_1 + v_1 v_2 b_1} = \frac{v_1}{v_2} = \sqrt{2} - 1 . \tag{D.3}$$

Consequently, at the $2n_{th}$ stage, AD=1 remains but

$$\begin{aligned} PE_\infty &= \tan^{-1}\left|\frac{a_\infty^2 - b_\infty^2 - 2a_\infty b_\infty}{a_\infty^2 - b_\infty^2 + 2a_\infty b_\infty}\right| \\ &= \tan^{-1}\left|\frac{a_\infty^2 - (3-2\sqrt{2})a_\infty^2 - 2(\sqrt{2}-1)a_\infty^2}{a_\infty^2 - (3-2\sqrt{2})a_\infty^2 + 2(\sqrt{2}-1)a_\infty^2}\right| = 0 \end{aligned} . \tag{D.4}$$

Further, at the $(2n+1)_{th}$ stage, PE=0º remains but

$$AD = \frac{\sqrt{2}a_n}{(a_n + b_n)} = \frac{\sqrt{2}a_n}{a_n + (\sqrt{2}-1)a_n} = 1 . \tag{D.5}$$

Therefore, perfect octet-phase accuracy can be obtained under any arbitrary initial condition of a_1 and b_1. However, choosing closer a_1 and b_1 results in less necessary stages for a tolerable criterion.

Appendix E Derivation of the Peak Gain and the Corresponding Criterion of the LC Tank with Lossy Inductor

As mentioned in Section 6.5-1, the impedance of the LC tank with $R_s = \alpha L$ can be expressed as

$$Z(s) = \frac{R_s + sL}{1 + sCR_s + s^2 LC} = \frac{\alpha L + sL}{1 + s\alpha LC + s^2 LC}. \tag{E.1}$$

Thus,

$$|Z| = \frac{\sqrt{\omega^2 + \alpha^2}\, L}{\sqrt{(1 - \omega^2 LC)^2 + (\alpha\omega LC)^2}}. \tag{E.2}$$

Take the differentiation by C, $|Z|_{\max}$ occurs at $(\omega^2 + \alpha^2)LC = 1$.

As a result,

$$\begin{aligned} |Z|_{\max} &= |Z|_{(\omega = \omega_0 = \sqrt{1/(LC) - \alpha^2})} \\ &= \frac{(\omega_0^2 + \alpha^2)L}{a} = \left[1 + (\frac{\omega_0}{\alpha})^2\right] \cdot (\alpha L) \\ &= (1 + Q^2) \cdot R_s \equiv R_p \end{aligned}. \tag{E.3}$$

Dividing Eqn. (A.2) by Eqn. (A.3), $|Z|/|Z|_{\max}$ can be obtained as

$$\begin{aligned} \frac{|Z|}{|Z|_{\max}} &= \frac{\sqrt{\omega^2 + \alpha^2}\, L}{\sqrt{(1 - \omega^2 LC)^2 + (\alpha\omega LC)^2}} \Bigg/ \left[\frac{(\omega_0^2 + \alpha^2)L}{a}\right] \\ &= \frac{\alpha\sqrt{\omega^2 + \alpha^2}}{\sqrt{\left[\omega^2 - (\omega_0^2 + \alpha^2)\right]^2 + (\alpha\omega)^2}} \quad \because (\omega_0^2 + \alpha^2)LC = 1 \\ &= \frac{1}{Q}\sqrt{(\frac{\omega}{\omega_0})^2 + \frac{1}{Q^2}} \Bigg/ \sqrt{\left[\frac{\omega^2}{\omega_0^2} - (1 + \frac{1}{Q^2})\right]^2 + (\frac{1}{Q}\frac{\omega}{\omega_0})^2} \end{aligned}. \tag{E.4}$$

Further, substitute $W=(\omega/\omega_0)$ for simplicity and assume $Q=\omega_0/\alpha >> 1$ for a high-Q condition, $|Z|/|Z|_{max}$ can be re-written as

$$\frac{|Z|}{|Z|_{\max}} = \frac{W/Q}{\sqrt{(W^2-1)^2+(W/Q)^2}}. \tag{E.5}$$

More generally, the The $|Z|/|Z|_{max}$ for the n stages of LC tanks in cascade can be expressed as

$$\frac{|Z|}{|Z|_{\max}} = \left(\frac{W/Q}{\sqrt{(1-W^2)^2+W^2/Q^2}}\right)^n . \tag{E.6}$$

The m-dB bandwidth is calculated by letting $|Z|/|Z|_{max}=1/10^{-m/20}$. As a result,

$$W^2 \pm kW/Q - 1 = 0 \tag{E.7}$$

where $k=\sqrt{10^{m/10n}-1}$.

Thus,

$$W = \frac{\sqrt{(k/Q)^2+4} \pm k/Q}{2}. \tag{E.8}$$

$\Delta W=W_H-W_L=k/Q$ where W_H and W_L are the two solutions of Eqn. (E.8).

Besides, if ω_H and ω_L are the target bandwidth boundaries, the center frequency will be $\sqrt{\omega_H\omega_L}$ because $W_H \times W_L=1$, where W_H and W_L are obtained from Eqn. (E.8). The Q value for a target bandwidth from ω_L to ω_H may thus be obtained by

$$Q = \frac{k\omega_0}{\Delta\omega} = k\frac{\sqrt{\omega_H\omega_L}}{\omega_H-\omega_L} . \tag{E.9}$$

Appendix F Derivation of the Tuning Capability of A Transformer With Only One Varactor in Either Side

A transformer with input/output capacitor loadings (C_1/C_2) is shown in Fig. 6-5(a). If only C_1 can be tuned, assume $L_2C_2 = 1/\omega_2^2$ and design $L_1C_{1,\max} = 1/\omega_{1,\min}^2 = X_a/\omega_2^2$, $L_1C_{1,\min} = 1/\omega_{1,\max}^2 = 1/(X_a\omega_2^2)$ where X_a>1.

Since $X = \omega_1^2/\omega_2^2$, $\omega_1 = \omega_0$, Eqn. (A.4) can be re-written as

$$\omega_{opt}^2 = \frac{\omega_1^2 + \omega_2^2 - \sqrt{(\omega_1^2 + \omega_2^2)^2 - 4\omega_1^2\omega_2^2 P}}{2P}, \tag{F.1}$$

where $P = (1 - k^2 - 1/Q^2) \approx 1 - k^2$ is nearly a constant because Q is large.

As a result,

$$\omega_H^2 = \frac{\omega_2^2}{2P}\left[X_a + 1 - \sqrt{(X_a + 1)^2 - 4X_a P}\right] \tag{F.2}$$

and

$$\omega_L^2 = \frac{\omega_2^2}{2P}\left[\frac{1}{X_a} + 1 - \sqrt{(\frac{1}{X_a} + 1)^2 - 4\frac{1}{X_a}P}\right] = \frac{\omega_H^2}{X_a} \tag{F.3}$$

That is,

$$\frac{\omega_H^2}{\omega_L^2} = X_a = (\frac{C_{1,\max}}{C_{1,\min}})^{1/2}. \tag{F.4}$$

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Curriculum Vitae

姓　名： 徐金詳
性　別： 男
出生年月日： 民國　73 年　8 月　22 日
籍　貫： 臺灣省桃園縣
學　歷： 國立交通大學 電信工程學系 學士 2002~2006
國立交通大學 電信工程學系 碩士 2006~逕讀博士班
國立交通大學 電信工程學系 博士 2007~2011

獲　獎：

2009~2011	聯發科技國內博士班獎學金 (MediaTek Fellowship)
2007~2008	教育部獎學金
2007	國家晶片設計中心（CIC）年度晶片設計優良獎
2007	直升博士班(春季入學)
2006	系上第一名畢業於國立交通大學電信系
	榮獲斐陶斐榮譽學會會員
2002~2006	電信工程學系 書卷獎(八學期第一名)
2005	大三榮獲朱順一合勤獎學金
2004	送珍敦品勵學獎學金
2003	送珍敦品勵學獎學金
2002	微積分獎(上、下學期各一次)

經　歷：

2008	台灣積體電路製造股份有限公司暑期實習
2008	專題:射頻積體電路實驗(研究所課程)助教: 講授 Spectre RF
2007~2008	交通大學通訊與電腦整合應用人材培訓計畫(實作)助教:
	講授 Spectre RF
2007	類比積體電路(研究所課程)助教
2007	電子學(二)助教
2006~2007	國家奈米元件實驗室高頻量測員

論文題目：

(中文) 應用於解決 CMOS 閃爍雜訊之低中頻接收機架構和深 N 型井雙極性接面電晶體直接降頻接收機

(英文) CMOS Flicker Noise Solutions by Low-IF Receiver Architecture and Deep-N-Well BJT Direct-Conversion Receiver

Publication List

（A）Significant Journal

[1] **J.-S. Syu**, C. C. Meng, Y.-H.Teng, and H.-Y. Liao, “Large improvement in image rejection of double-quadrature dual-conversion low-IF architectures,” ***IEEE Trans. Microw. Theory Tech.*,** vol. 58, no. 7, pp. 1703−1712, Jul. 2010.

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（B）International Journal

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