

使用金氧半導體基板正偏壓設計的 射頻高輸出功率放大器

研究生：張秦豪 指導教授：吳重雨 教授

國立交通大學

電子工程學系 電子研究所碩士班

摘要

本篇論文主旨在設計一個可供長距離傳輸的高輸出功率的射頻放大器，其規格設定在 FCC 15.247。此設計是強調用基板正偏壓來減少所須金氣半導體的 size，使 output stage 的輸入端的閘極的寄生電容下降，進而使 driving stage 能傳遞更大的輸出信號進入 output stage。另外為了兼顧線性度與效率，此電路設計第一級操作在 class-A, 第二級操作在 class-AB。而加上 differential+cascode 架構來增加輸出功率及避免閘極-汲極 breakdown 問題，另外以穩定加強電路來加強高低頻的穩定，使電路能達到操作時無條件穩定。

此設計的晶片是使用標準點 25 微米 1P5M 互補式金氧半導體製程。此晶片在量測過程中完全沒有振盪現象發生。實際量測此晶片在操作溫度 26.2°C、1.9GHz 的頻率時，輸入信號功率為 0dBm 情況下，能提供 25.3 dBm 的輸出功率，同時有 17.51% 的效率，而 1dB compression gain (P1dB) 是 -9dBm, Adjacent channel power ratio(ACPR)在 GSM(1.8GHz) 標準信號輸入下，在 400kHz 的頻寬下的 ACPR 是 -43.07dBc。

THE DESIGN OF HIGH-OUTPUT-POWER RF POWER AMPLIFIER USING MOS DEVICES WITH POSITIVE SUBSTRATE BIAS

Student: Chin-Hao Chang Advisor: Prof. Chung-Yu Wu

Degree Program of Electrical Engineering Computer Science

National Chiao Tung University

ABSTRACT

This thesis is proposed for designing a high-output-power RF CMOS power amplifier using MOS devices with positive substrate bias. This design is targeted on the standard of FCC 15.247. The MOS device with positive substrate bias was used to reduce the devices size and relative parasitic capacitance. Furthermore, it's helped that the driver stage can deliver large enough signal to output stage and improve the efficiency. To consider the linearity and efficiency, the input stage operates in class-A and output stage operates in class-AB. The differential with cascade topology is used to alleviate the gate-drain breakdown phenomenon. Besides, stability enhanced circuits are used to ensure that the design can operate in unconditional stable.

This chip is fabricated in a standard 0.25 μ m single-poly-five-metal CMOS process. There are no oscillated phenomenon during experiment. Experimental results showed this chip can provide 25.3 dBm output power with 17.51% PAE at input power equal 0dBm at 26.2°C. The 1dB compression gain is -9 dBm and the ACPR is -43.07dBc at 400kHz frequency when used GSM(1.8GHz) modulated signal as input.

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