CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The expansion of the market for portable wireless communication devices has given tremendous push to the development of a new generation of low power radio frequency integrated circuit(RFIC) products. Cellular and cordless phones, pagers, wireless modems, and RF ID tags, require more compact and power saving solutions to accommodate the ever-growing demand for lighter and cheaper products [1].

The optimum integrated circuit technology choices for RF transceivers in terms of optimum devices and levels of integration are still evolving. Engineers planning to implement wireless transceivers are confronted with various possibilities: silicon CMOS, BiCMOS, and bipolar technologies, GaAs MESFET, hetero-junction bipolar transistor(HBT), and PHEMT, as well as discrete filters. Traditional commercial implementation of high performance wireless transceivers typically utilizes a mixture of these technologies in order to implement a complete system [2]. The VLSI capabilities of CMOS make this technology particularly suitable for very high levels of mixed signal radio integration while increasing the functionality of a single chip radio to cover multiple RF standards [3].

The research in the area of power amplifiers is divided into two main categories; the design and monolithic implementation of power amplifiers, and the integration of Linearization techniques. While the implementation of a complete transceiver was the focus of many publications [4]-[6], the power amplifier was included in only two of the reported CMOS wireless transceivers [4].

Many publications advocated that CMOS would be limited only to low-power low-performance applications. In [7] a 1W-2.5V supply monolithic power amplifier was reported. The PA targeted NADC standards (824MHz-849MHz). A gain of 25dB is achieved through 3 gain stages (operating in class A, AB, and C), with the output stage operating in class D(the transistor is used as a switch). This power amplifier has a measured drain efficiency of 62% and a PAE of 42%. It does not achieve a high degree of integration sine the output-matching network is implemented of chip. Bond wires are also used as a part of the inter-stage matching network.

A sample of the publications listed in Table 1.4 shows that even though the inductors and capacitors that may be realized in CMOS technology are not suitable for high performance RF circuits, CMOS transistors have still adequate gain till 2GHz to allow the design of low cost hybrid 1W amplifiers. The real merits of CMOS PAs lie in the potential for integration. While the feasibility of a stand alone CMOS PA does not imply its compatibility in a larger system, the integration issues will rely on system, circuit and layout solutions rather than the design of the individual block.

The design of high-output-power RF CMOS power amplifiers in CMOS technology is mainly affected by the following factors:

(1). Low breakdown voltage of deep sub-micron technologies.

This limits the maximum gate-drain voltage since the output voltage at the transistor's drain normally reaches 2 times the supply for classes B, and F, and around 3 times the supply for class E operation. Thus, transistors have to operate at a lower supply voltage, delivering lower power.

(2). Low current drive capability

It's the series problem to design a high-output-power RF power amplifier. Since the

large current we need, the large MOSFET devices sizes have to be designed. The parasitic caps are direct proportional to devices sizes. Hence the parasitic cap results in the lower gain of driving stage.

(3). Output matching network

The output device impedance in the high-output-power PA is very low, requiring higher impedance transformation ratios. Usually the output matching network is implemented off chip with lower loss lumped elements. It's difficult to get the well value and high performance lumped elements.

(4). Oscillation issue

The mere mention of high-output-power RF power amplifier usually generates an instantaneous and fearful reaction over the near certainty of uncontrollable and destructive oscillations. Generally, RF power amplifier oscillation problem can be broadly categorized into two kinds: Bias oscillations and RF oscillations. Bias oscillations occur at very low frequency. On the other hand, RF oscillation typically occur either in band or out of band but still quite close to the design bandwidth. One of the most common causes of instability is the attempt to duplicate the functions of RF grounding and supply decoupling with on large-value capacitor. Nevertheless, Stability is still an issue to design a power amplifier. Owing to the large voltage and large current change that output stage experienced. The accuracy of large signal CMOS RF models and bond wire modeling are critical to the successful design and stable operation of integrated CMOS radio frequency power amplifier.

1.2 REVIEW OF CLASS-AB HIGH-OUTPUT-POWER CMOS POWER AMPLIFIER

Because the low current driving ability, to design a high-output-power CMOS power amplifier is difficult. In the linearization area, few papers were published that dealt with monolithic implementation, while most of the published work focused on system simulations and discrete implementation. Besides, most of high-output-power RF CMOS power amplifiers which publication recent years were bias at class-AB.

There are a number of reasons to choose this mode of operation.

1. Class AB close to Class B is relatively linear. This is not the case for class C and E amplifiers. The linearity is, however, not as good as class A.
2. The efficiency is relatively good, the ideal maximum efficiency is 78.5%, compared with 50% for the class A amplifier and class-C, E amplifiers have theoretical efficiencies of up to 100%.
3. The maximum drain voltage is twice the supply voltage, this is important due to the possible breakdown of the gate-oxide. Class-C and E amplifiers easily exceed three times the supply voltage.
4. The power utilization factor (PUF), which is a measure of the gain compared to the output power, is reasonable compared with class A, and better than class C and E.
5. The required output load impedance is not too low to implement efficiently, which is often the case for class C.

The publications of high-output-power CMOS power amplifier which bias at class-AB were list in Table

In [9] a 900 MHz fully-integrated CMOS RF amplifier is reported as Fig.1-1.

Parasitic associated with transistors and on-chip passive components, such as inductors and capacitors, as well as the package, limit the performance of RF integrated circuits. To design a fully-monolithic RFIC requires extensive use of a sophisticated CAD tools to mitigate the impact of the aforementioned parasitic effects. Use of a CAD technique optimizes design of a distributed amplifier and a balanced power amplifier. This design uses only on-chip spire inductor with Q-values in the range of 2-4, and the active devices used BSIM2 models with added gate resistance terms. The output stage operates in Class-AB and gets overall PAE is 23% and output power is 17.4 dBm. At 1 dB compression, the PA supplies 55mW at 49% efficiency.

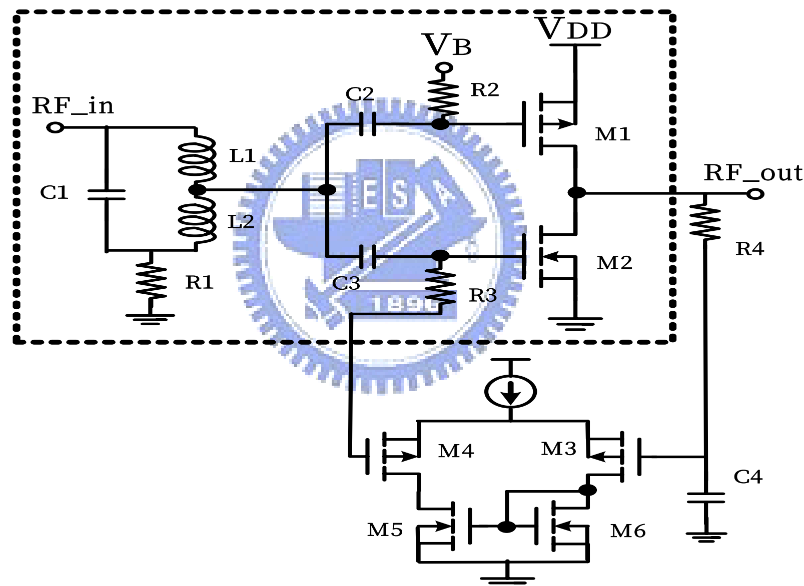


Fig. 1-1 Simplified schematic of [9].

In [10] a 1W 0.35 μm CMOS power amplifier for GSM-1800 with 45% PAE is reported. It is designed for a 0.35 μm bulk CMOS process with a substrate receptivity of 10~20 ohm. The input-matching network is made with a fully-integrated highpass LC matching section. The output-matching network is placed primarily off-chip due to efficiency. To improve harmonic termination, a capacitor is placed on-chip, directly at the drain of the transistor. Input and output stages are operate in class-AB. This design gets

overall PAE is 45% and output power is 30.4 dBm.

In [11] a 1W CMOS power amplifier for GSM-1800 with 55% PAE is reported. The design of this power amplifier followed the design and simulation methodologies described in [10]. This design shows higher integration and much better efficiency than previously presented. The RF chokes for the output stage as well as the input stage are relatively short microstrips, which can be implemented without increasing the overall PCB size. This design get overall PAE is 55% PAE and output power is 30.4 dBm.

Fig. 1-2 Simplified schematic of [10]、[11]

Table I   The publications of high-output-power CMOS power amplifier which bias at class-AB

	B. Ballweber [9]	Fallesen et. Al. [10]	Fallesen et. Al. [11]
Target standard	ISM band	GSM-1800	GSM-1800
Frequency (MHz)	900	1750	1750
1st / 2nd stage operating Class	AB / AB	AB / AB	AB / AB
Ropt (ohm)	Load pull	4	4
Driver stage size : W/L (μm/μm)	—	1000 /0.35	1000 /0.35
Output stage size : W/L (μm/μm)	3000 /1.2	8000 /0.35	8000 /0.35
Circuit structure	Differential	Single	Single
Die size : W*L (mm^2)	0.79 × 0.79	1.9 × 1.9	1.15 × 1.1
Voltage (V)	3	3.3	3.3
P_DC (W)	0.084	2.4	1.8
Pout (dBm)	17.4	30.4	30.4
PAE (%)	23	45	55
P1dB (dBm)	12	—	—
input / output matching network	on / on chip	on / off chip	on / off chip

1.3 MOTIVATION

For applications requiring moderate to high-output-power, the power amplifier contributes significantly to the total transceiver power consumption, making the output power critical to the overall system performance. In order to realize a complete transceiver on chip, issues related to system specifications, individual block performance, and the layout of the whole chip have to be dealt with. Without regarding the integration issue, a stand-alone power amplifier, implemented in CMOS, and capable of covering multi-frequency bands can provide low-cost solution to less demanding wireless standards, e.g. Bluetooth, WLAN.

FCC 15.247 standard defines the maximum power for different modulation system、minimum spread spectrum 、peak power spectral density in ISM band(902 ~928 MHz, 2400MHz~2483.5MHz, and 5725~5850 MHz). The modulation scheme is Complementary Code Keying (CCK). This is specifies a 2.4GHz Frequency-Hopped Spread-Spectrum system that enables the users to easily connect to a wide range of computing and telecommunication devices, e.g. Asses Point(AP). The maximum power of an assess point (AP) for wireless LAN is 30dBm.

The research of this thesis focuses on a high-output-power (29dBm) class-AB power amplifier with small MOS devices size. The MOS devices size should be reduced by using the positive substrate bias. This design is targeted on the standard of FCC 15.247 specification.

1.4 MAIN RESULTS

The high-output-power amplifier RF CMOS power amplifier using MOS devices

with positive substrate bias has been designed and fabricated. Measured output power of the designed PA is 25.3dBm with 17.51% PAE @0dBm input power, and output power spectrum mask is -43.07dBc at 400kHz bandwidth.

1.5 THESIS ORGANIZATION

This thesis is divided into five chapters. The chapter 1 introduces the background, motivation and high-output-power RF CMOS PA design challenge. Chapter 2 will discuss common architectures of the power amplifier and review the recent progress of Class-AB high-output-power CMOS Pas.

The proposed power amplifier will be presented at Chapter 3. Design consideration of the power amplifier is discussed in Section 3.1. The PA design procedure is presented in section 3.2. Section 3.2.1 shows the design procedure of output stage of the High-output-power PA. Section 3.2.2 shows the design procedure of pre-amplifier stage. The stability enhanced circuits of PA is proposed in Section 3.2.3. The current capability calculation and design is proposed in Section 3.2.4. The post-simulation results are shown in Section 3.3.

The experimental results will be shown in Chapter 4. Finally, the conclusions and future works will be presented Chapter 5

CHAPTER 2

RF POWER AMPLIFIER REVIEW

2.1 RF POWER AMPLIFIER CLASSES

RF Power amplifiers can be divided into linear amplifier and nonlinear amplifier. Linear amplifiers have been categorized as bias point dependent, such as class A, B, C, AB. Nonlinear amplifiers have been categorized as passive element in the output matching network dependent, such as class D, E, F. In the next subsections, the details of each operating class are discussed.

2.1.1 Class A, B, AB, and C Power Amplifiers

The primary distinction between these power amplifier classes is the fraction of the RF cycle for which the transistor conducts. Figure 2.1 illustrates the general model for these four types of PA.

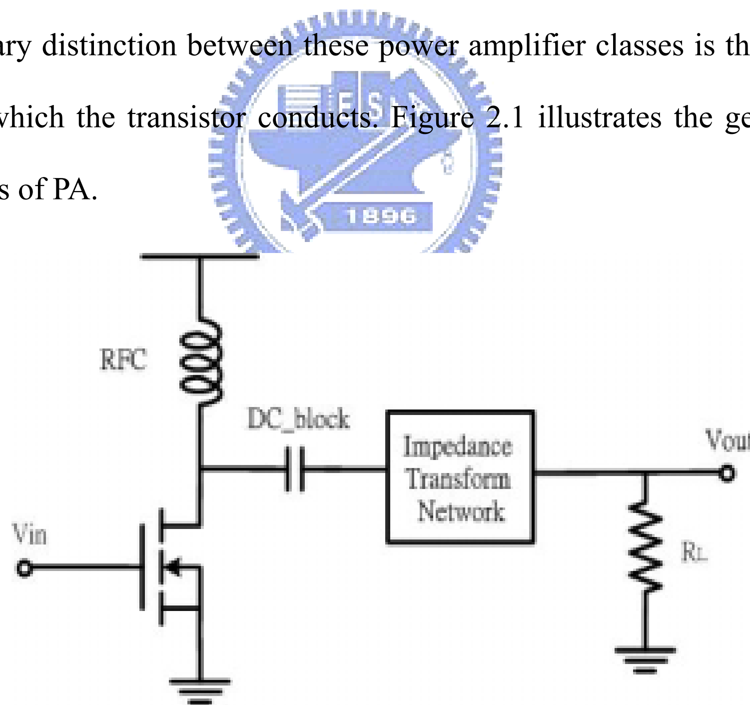


Fig. 2-1 RF power amplifier general model

In this model, the resistor RL represents the output load to which the PA delivers the output power. RFC is a big inductor which means RF choke. The λ/4 transmission lines usually instead of RF choke at radio frequency. The impedance transform network is used

to transform output load RL to smaller impedance.

2.1.1.1 Class- A Amplifier

A class-A amplifier is one in which the operating point and input signal level are chosen such that the output drain current flows at all times. It therefore operates in the linear portion of its characteristic and hence the signal suffers minimum distortion. The drain voltage and current waveform is shown in figure 2-2 In fact, class-A amplifiers are often by no means linear, and highly linear amplifiers are not necessarily, or even frequently, of the class-A type.

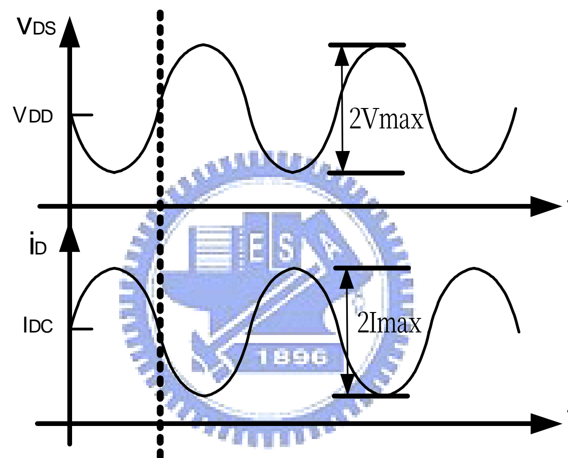


Fig. 2-2 Drain voltage and current for ideal class-A

2.1.1.2 Class-B Amplifier

Class-B operation is significantly more efficient than class-A for use in linear power amplifiers, whilst still providing useful levels of linearity. Usually, a class-B amplifier conducts for 50 % of the input cycle (sinusoidal wave will be assumed) and hence produces significant distortion. The drain voltage and current waveform is shown in figure 2-3

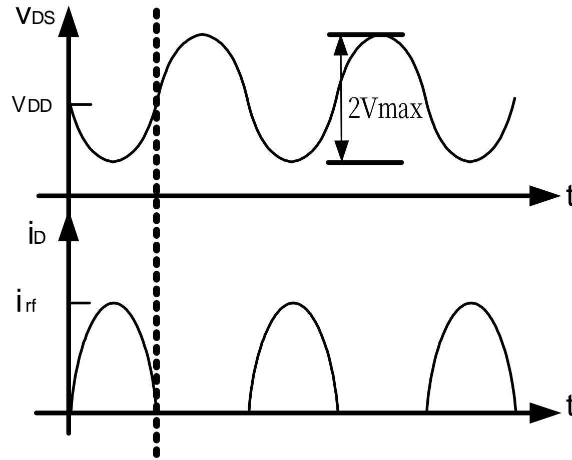


Fig. 2-3 Drain voltage and current for the ideal Class-B amplifier

2.1.1.3 Class-AB Amplifier

A class-AB amplifier is a compromise between the two extremes of class-A and class-B operation. The output signal of this type of amplifier is zero for part, but less than one-half of the input sinusoidal signal. The Drain current of class-AB amplifier conducts between 50% and 100% cycle, which depends on bias levels it choose. The device is biased to a quiescent point which is somewhere in the region between the cutoff point and the class-A bias point. Consequently, its efficiency and linearity are intermediate between those of a class-A and class-B amplifier.

2.1.1.4 Class-C Amplifier

In a class-c amplifier, the transistor is on for less than half cycle so as to improve the efficiency. This class of amplifier will thus result in significant distortion of the input signal wave shape during the amplification process, thus making it unsuitable of 'linear' amplification applications. The drain voltage and current waveform of classical class-C amplifier is showed in Fig. 2-4.

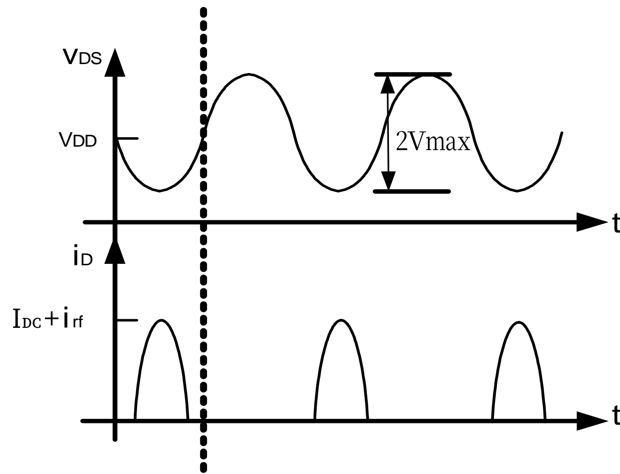


Fig. 2-4 Drain voltage and current for classical Class-C amplifier

The I-V curve, conduction angle and summary of Class A, B, AB, C are shown in figure 2-5 and the summary of Class A, AB, B, C characteristic are as Table II

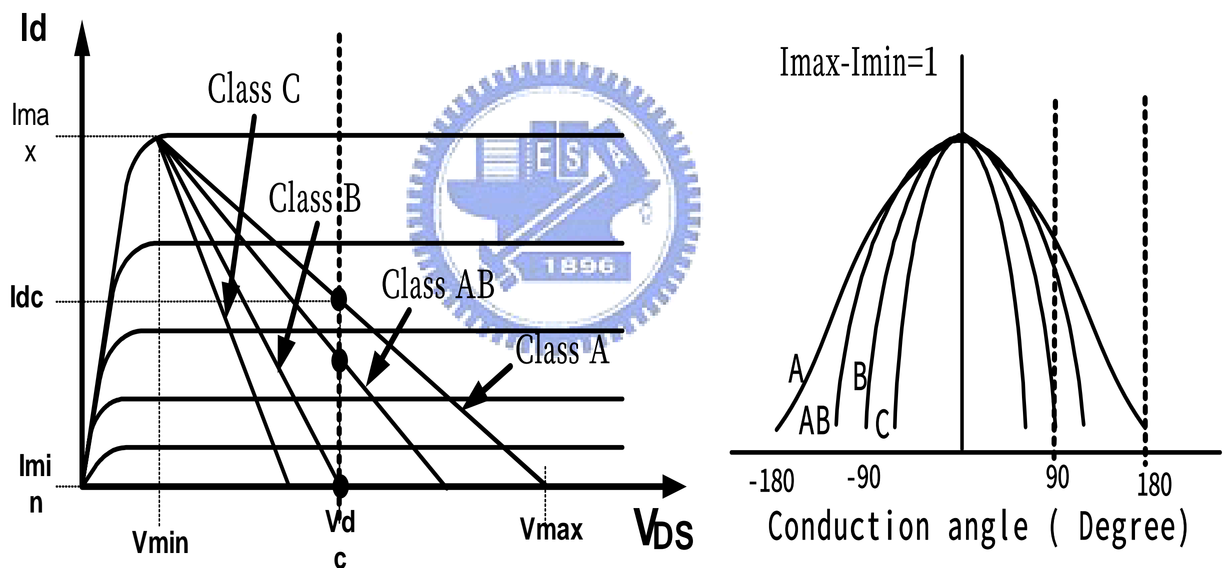


Fig. 2-5 Class A, AB, B, C I-V curve and conduction angle

Table II Summary of Class A, AB, B, C power amplifier

Class	Conduction Angle	Efficiency	Gain	Linearity
A	360°	50%	High	Good
AB	180 ~ 360°	50~78 %	-3 ~ -6 dB	Harmonics
B	180°	78.50%	-6 dB	Harmonics
C	0 ~ 180°	>78.5 %	Low	Harmonics

2.1.2 Class D, E, and F Power amplifiers

Class-D, E amplifiers utilize the active device as a switch and hence the theoretical maximum efficiency is 100%, assuming that the device has zero switching time, zero on-resistance and infinite off-resistance. Class-F attempt to improve upon the basic efficiency of class-B or –C amplifiers by adopting modified forms of the standard circuit topologies.

2.1.2.1 Class-D Amplifier

The transformer-coupled class-D configuration is similar in structure to the transformer-coupled class-B design. As in the complementary class-D amplifier, the input transformer results in the transistors turning on and off alternately. A series RLC output filter allows only the fundamental component to flow into the load. The supply voltage V_{DD}, is thus placed across alternate halves of the primary winding, resulting in positive and negative transformed versions of V_{DD} across the secondary.

The efficiency may again be shown to be 100%, with the output filter performing the same function. Practically, there is no such a perfect switch. Nonzero saturation voltage results in static power dissipation in the switches and finite switches and finite switching speeds cause that the switch V-I product is nonzero during the transitions. Besides, the parasitic capacitances of drain may be charged and discharged once per RF cycle, resulting in power loss that is proportional to V_{DD}. There are three main configurations for the class-D stage (the complementary switch and voltage or current transformer coupled designs as figure 2-6) and these are based on the class-B designs described earlier. The complementary voltage switching configuration is the most straightforward of these and will be described first. The drain voltage and current was as Fig. 2-7.

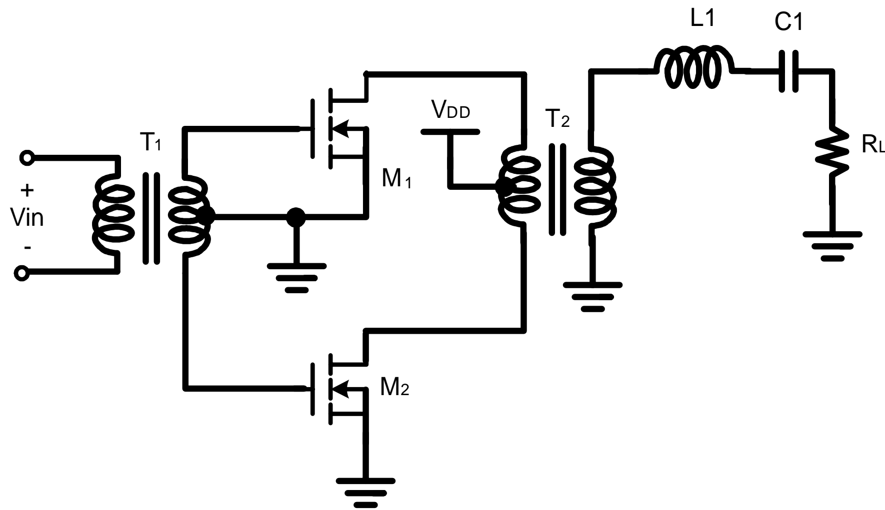


Fig. 2-6 The transformer-coupled class-D amplifier configuration

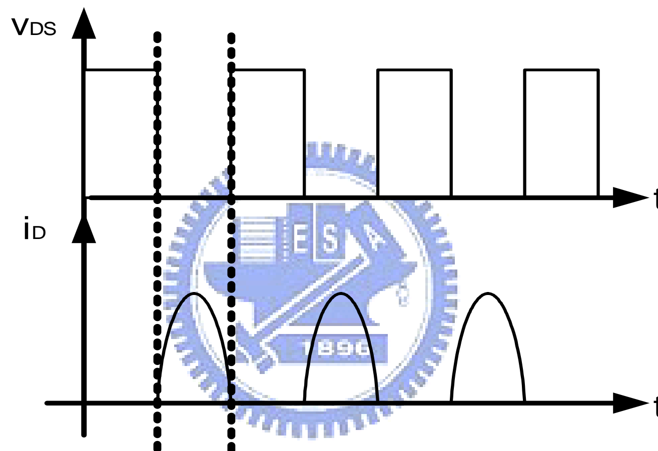


Fig. 2-7 The M1 drain voltage and current for ideal class D amplifier

2.1.2.2 Class-E Amplifier

The class-E amplifier is a single-ended configuration with a passive load network as shown in Figure 2-8. In the operation of the class-E stage, the MOS device is assumed to operate as an ideal switch with zero 'on'-resistance and infinite 'off'-resistance. The result is an ideal efficiency of 100%.

In practice, the drain current of the MOS is near maximum when the switch turns off. Unfortunately, if the switch was not infinitely fast, it would induce a significant switch

turn off losses. Hence, it reduces the efficiency. Besides, another drawback is the large peak voltage that the switch sustains in the off state, approximately 3.56VDD which is shown in Figure 2-9. Hence the circuit Q, saturation voltage and switching time will reduce the efficiency in practice.

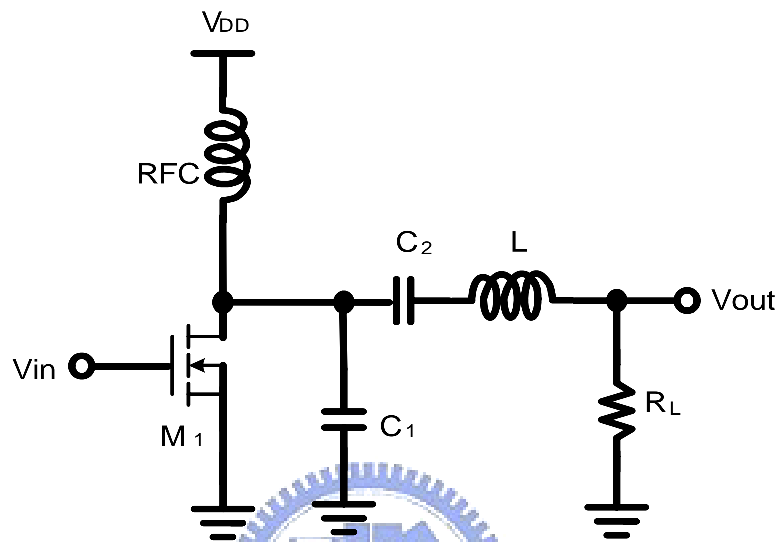


Fig. 2-8 Single-ended class-E amplifier

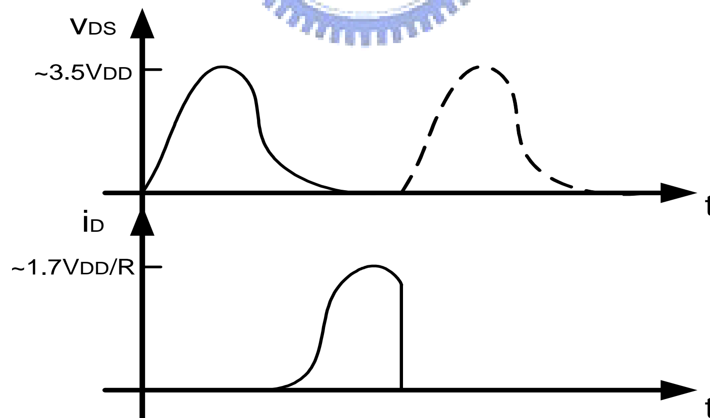


Fig. 2-9 Voltage and current waveforms for class-E amplifier

2.1.2.3 Class-F Amplifier

A class-F amplifier has a resonator network at one or more harmonic frequencies in

addition to its resonance at the fundamental frequency. A class-F amplifier with a resonant network was as Fig. 2-10. The voltage waveform includes one or more odd harmonics and approximates a rectangular waveform. Sometimes, we replace the harmonic resonant circuit with a quarter-wave transmission-line which simulates the equivalent of an infinite number of resonators. The efficiency of an ideal class-F amplifier increases from 50% toward unity. The class-F PA requires more complex filter network than other PAs.

Fig. 2-10 A Class-F amplifier with a resonant network

2.2 Conjugate match and load-line match

The concept of conjugate match is widely known as setting the value of the load impedance equals to the real part of the generator's impedance such that maximum output power is delivered to the load. However, this delivered power is limited by the maximum rating of the transistor acting as a current generator, together with the available supply voltage. As Figure 2-11 it is evident that the device in this case would show limiting action at a current considerably lower than its full capacity. To utilize the maximum

current and voltage swing of the transistor, a load resistance of lower value than the real part of the generator's impedance value needs to be selected; this value is commonly referred to as the load-line match, Ropt and in its simplest form is the ratio Ropt=Vmax/Imax, assuming the generator/s resistance is much higher than the optimum load resistance.

Thus the load-line match represents a real compromise that is necessary to extract the maximum power from RF transistor, and at the same time keep the RF voltage swing within the specified limits of the transistor and the available dc supply.

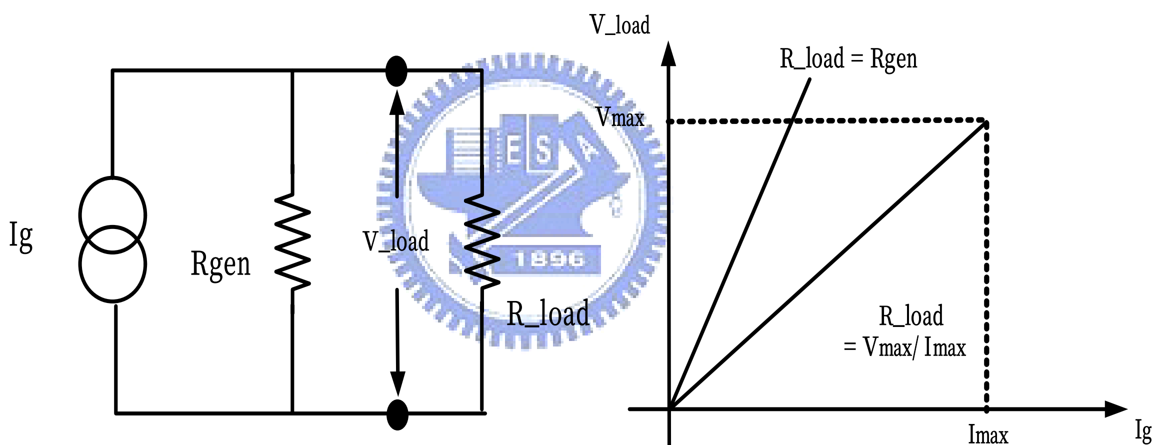


Fig. 2-11 Conjugate match and load-line match

Figure 2-12 illustrates the effect of the difference of gain match versus power (load-line) match on the output of a linear amplifier.

The solid line shows the response of an amplifier that has been conjugately matched at much lower drive levels. The two points A and B, refer to the maximum linear power and the 1dB compression power. In a typical situation, the conjugate match yields a 1dB compression power about 2dB lower than that which can be obtained by the correct power tuning, shown by the dotted line in Figure 2-12. This means the device would

deliver 2dB lower power than the device manufacturers specify. Since in power amplifier design, it is always required to extract the maximum possible power from the transistor, power-matched condition has to be taken more seriously, despite the fact that the gain at lower signal levels may be 1 dB or less than the conjugate-matched condition. Across a wide range of devices and technologies, the actual difference in output power, gained by power-matched condition, may vary over a range of 0.5dB to 3dB [12].

However, a load-line (power) matched rather than a conjugate(gain) match, might cause reflections and voltage standing wave ratio (VSWR) in a system to which it is connected. The reflected power is entirely a function of the degree of match between the antenna and the 50-ohm system. The PA does present a mismatched reverse termination, which could be a problem in some situations. An Isolator or a balanced amplifier [13] is a simple and effective way of dealing with the problem.

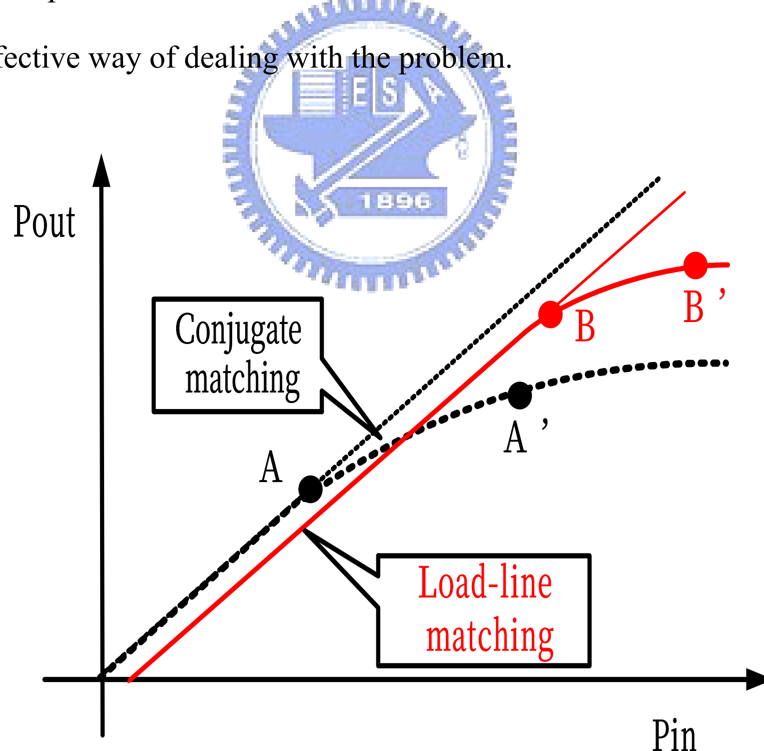
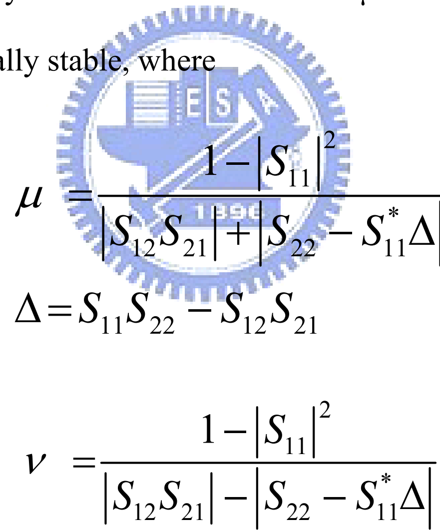


Fig. 2-12 Compression characteristics for conjugate match (s22) (dotted curve) and load-line match (solid curve). 1dB gain compression points (B,B') and maximum power points (A, A') show similar improvements under power-matched conditions.

2.3 STABILITY FACTOR μ

Two new stability parameters "μ"and "ν"are defined for linear two port circuits using a geometrically approach. The magnitudes of both μ and ν parameters determine the geometrical relation between SC(stability circle) and USC(Unit Smith Chart) in Γ_L plane.If $|\nu| > |\mu| > 1$, SC is outside the USC. If $|\nu| > 1 > |\mu|$, SC interests the USC. If $1 > |\nu| > |\mu|$, SC is inside the USC. The signs of ν parameter determine that the region inside SC (disk) is stable if ν>0or the region outside the SC is stable if ν<0. The stable region includes the USC origin if μ parameter is negative.

Edwards et al [15] used a single geometrically derived parameter "μ" to establish the criterion for unconditionally stable. It was shown that μ>1 is necessary and sufficient for a circuit to be unconditionally stable, where



$$\mu = \frac{1-|S_{11}|^2}{|S_{12}S_{21}| + |S_{22} - S_{11}^* \Delta|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$\nu = \frac{1-|S_{11}|^2}{|S_{12}S_{21}| - |S_{22} - S_{11}^* \Delta|}$$

If $|\nu| > |\mu| > 1$, SC is outside the USC as illustrated in figure 2-13 , Fig. 2-13(a) and Fig. 2-13(c) correspond to unconditionally stable cases. The Rollet factor K is large than one for the cases of figure Fig. 2-13(a) and Fig. 2-13(c). It is evident that stable region is a disk when ν>0 and stable region is a disk complement when ν<0. Both Fig. 2-13 (a) and Fig. 2-13 (c) have the USC origins in the stable regions because μ>0. It can be easily observed that all the passive terminations inside the USC in Fig. 2-13(b) and Fig. 2-13(d)

result in absolutely unstable conditions. The Rollet factor K is less than -1 for the cases of Fig. 2-13(b)and Fig. 2-13(d)

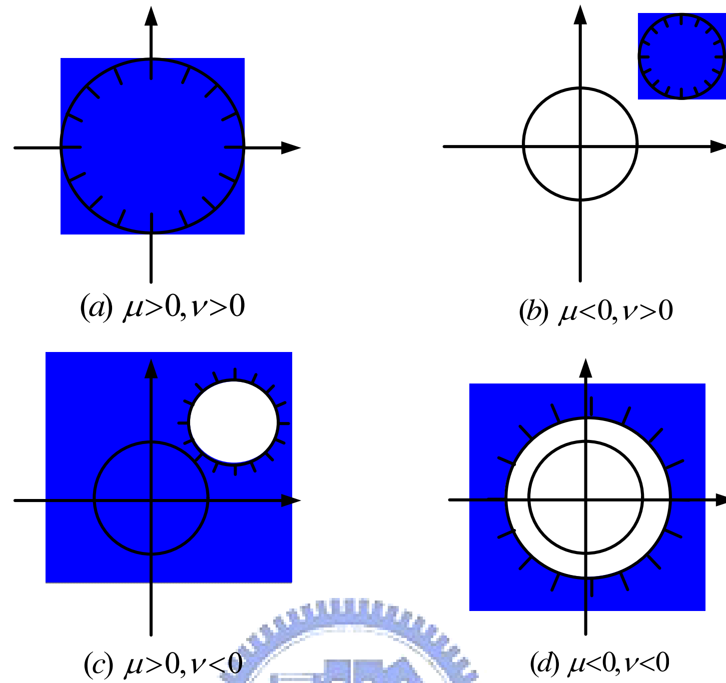


Fig. 2-13 SC and USC in Γ_L plane when $|\nu| > |\mu| > 1$

If $|\nu| > 1 > |\mu|$, SC intersects the USC in two points as shown in Fig. 2-14. The situations in Fig. 2-14 corresponds to $|K| < 1$. Most semiconductor devices such as MESFET, HBT and PHEMT have $|K| < 1$ at wireless communication frequencies (several GHz). Thus, the geometrical relation between SC and USC provides useful insights and information for the design of conditionally stable devices with $|K| < 1$.

If $1 > |\nu| > |\mu|$, SC is inside the USC as illustrated in Fig. 2-15 . All the situations in Fig. 2-15 correspond to conditionally stable cases with $|K| > 1$. The K factor is large than one for the cases of Fig. 2-15 (a) and Fig. 2-15 (b); while the K factor is less than -1 for the cases of Fig. 2-15(c) and Fig. 2-15(d)

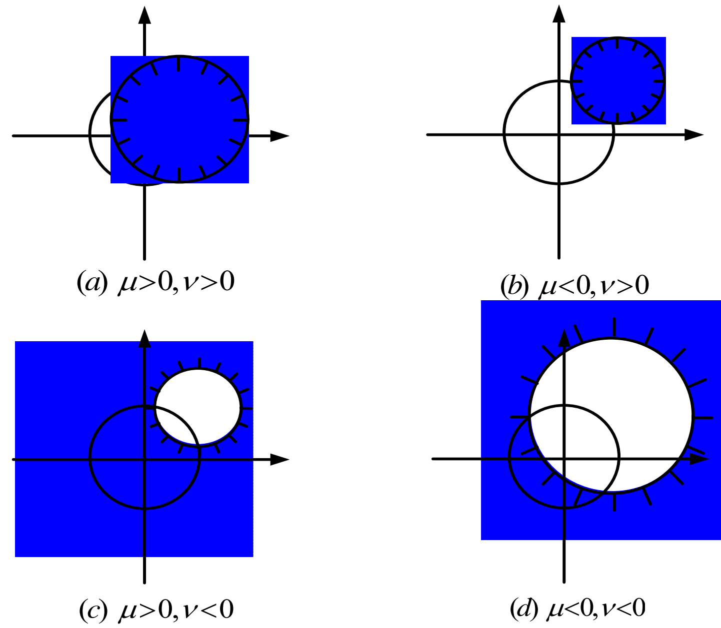


Fig. 2-14 SC and USC in Γ_L plane when $|\nu| > 1 > |\mu|$

For all case in Fig. 2-13~Fig. 2-15, the signs of ν parameter determine that the region inside SC is stable or the region outside the SC is stable. The signs of μ parameter determine whether the stable region includes the USC origin or not.

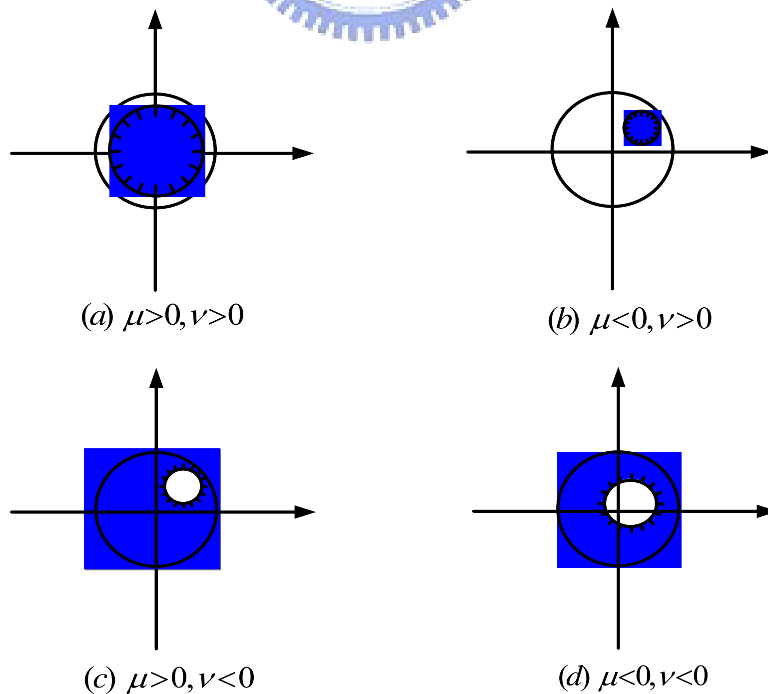


Fig. 2-15 SC and USC in Γ_L plane when $1 > |\nu| > |\mu|$

CHAPTER 3

CIRCUIT STRUCTURE AND POST-SIMULATION RESULTS

3.1 DESIGN CONSIDERATION

Traditionally, hetero-junction bipolar transistor (HBT), GaAs MESFET, PHEMT, BiCMOS are used to design the power amplifier. Recently, CMOS power amplifier is reported due to integrating the whole RF transceiver into a single chip. The challenges in the design of high-output-power RF CMOS power amplifier were discussed in section 1.3

In this research, two stages with fully differential cascade topology are adopted as Fig. 3-1. The cascade topology was used to solve the low breakdown voltage of CMOS, the MOS devices with positive substrate bias are used to reduce the parasitic effects for driving large currents 、stability enhanced circuits are used to make sure the design circuits are unconditional stable.

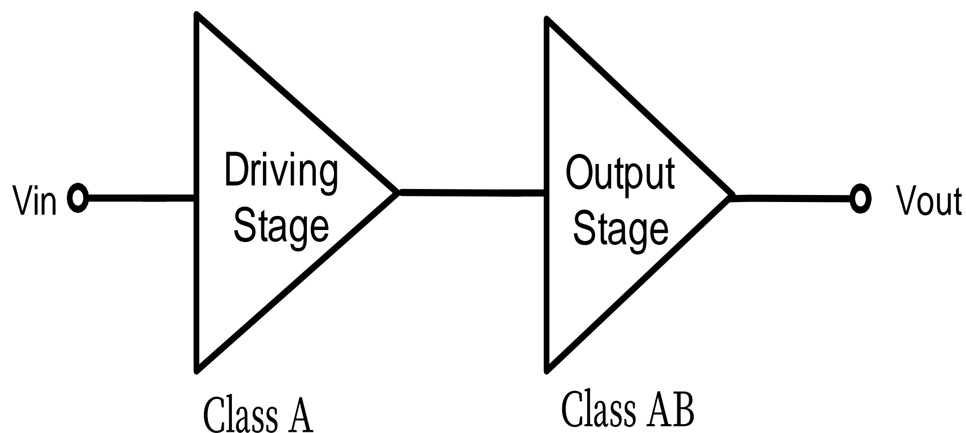


Fig. 3-1 Architecture of the designed power amplifier

3.2 CIRCUIT DESIGN

3.2.1 Output Stage

Output stage was used to deliver the maximum output power to the load. The output stage design starts by determining the MOS Drain current, power supply, one can get the optimum resistance (Ropt). Then adjusting the bias point and input signal amplitude to achieve the class you want. In this research, we want to design an output power 29dbm (800mw) Power amplifier. The power supply is 3.3 Volt , assume threshold voltage is 0.8 volt. Although it's helpful to use the load-pull test equipment to find the constant power contours and realize the optimum matching resistance., we can calculate the optimum resistance from Cripps rule as the following :

$$Pout = \frac{V_{swing}^{2}}{8R_{opt}} = \frac{V_{swing} \cdot I_{swing}}{8}$$

$$800mw = \frac{(2(V_{dd} - V_{th}))^2}{8 * R_{opt}} = \frac{(2(3.3 - 0.8))^2}{8 * R_{opt}}$$

$$R_{opt} \approx 4 \ ohm$$

$$I_{swing} \approx 1.28 \ A$$

$$I_{peak} = 0.64A \ , \ I_{differential} = 0.32 \ A$$

We get the optimum matching resistance is 4 ohm and the current I_{peak} *is* $0.64A$.

Actually, the current would be 0.32A in differential topology. The optimum output matching resistance on smith chart is as Fig. 3-1

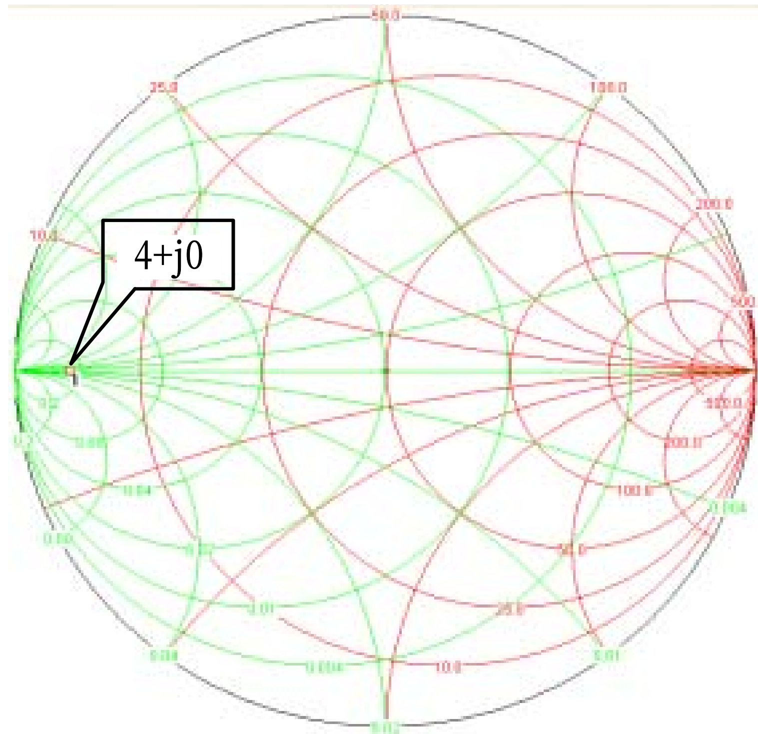


Fig. 3-1 The optimum output matching impedance on smith chart

The TSMC 0.25 μm process was used in this research. We can determine the output stage sizes with length=0.35 μm and width =4800 μm which the I-V curve was show as Fig. 3-2

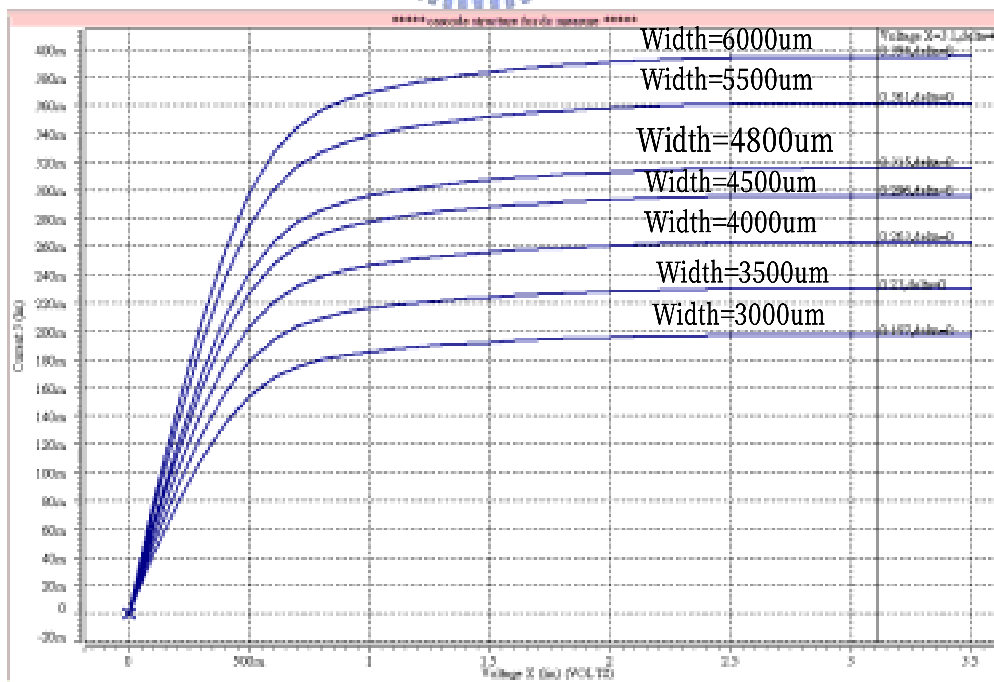


Fig. 3-2 The I-V curve of conventional NMOS device

The parasitic capacitance of gate was 8.2p under this MOS device size. It's hard to tune out the capacitance of the gate of the desired frequency by the inductor of driver stage. A good method to reduce the parasitic capacitance but current driving capability is positive substrate bias which was show as Fig. 3-3.

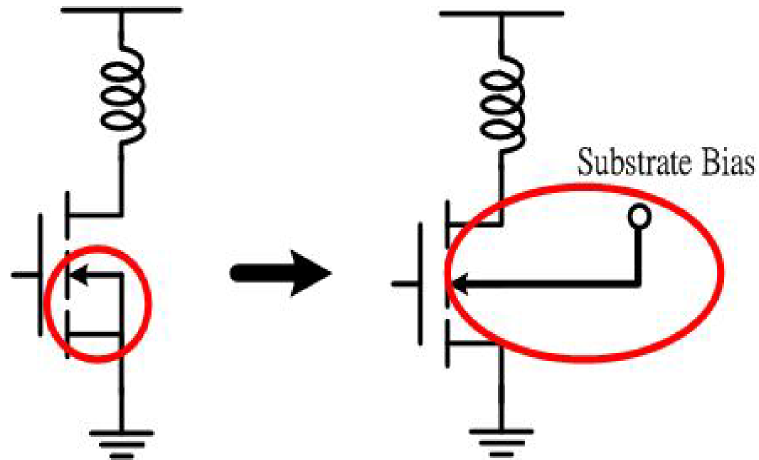


Fig. 3-3 Modified MOS devices with substrate bias topology

The I-V curve of the MOS device with substrate bias was show as Fig. 3-4. The MOS width was decrease from 5000 μm to 3500 μm and the parasitic capacitance was reduce form 8.2 pf to 5.9 pf .

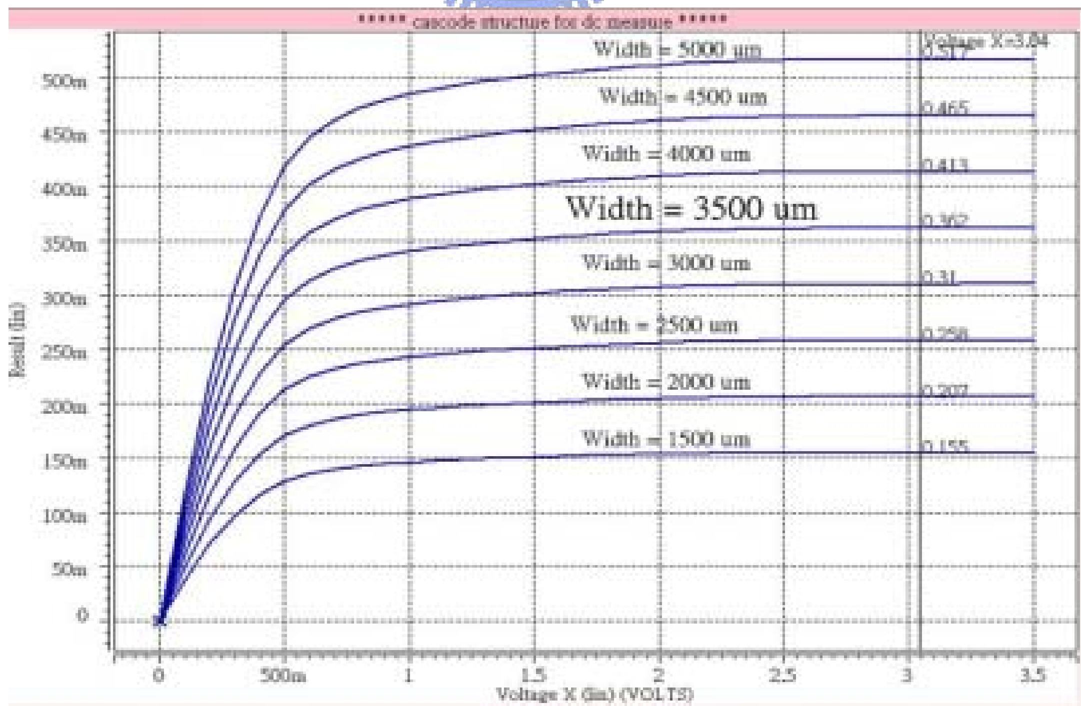


Fig. 3-4 The I-V curve of NMOS device with substrate bias

The L matching network which shows as Fig. 3-5 was used to output matching topology. The inductor L1 was implemented by bondwire.

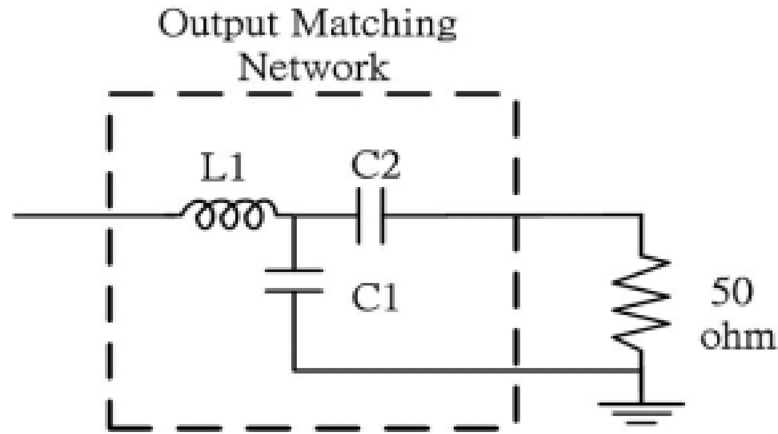


Fig. 3-5 Output matching network topology

For example, the parasitic capacitance of drain (C_{out}) was 4.6pf. We can design the value of each component as following procedures:

$$C_{out} \approx 4.6pf$$

$$\therefore \quad X_{out} = \frac{1}{2*\pi*2.44G*4.6p} \approx 14.18$$

$$R_s = \frac{3.9}{1+\left(\frac{3.9}{14.18}\right)^2} \approx 3.63$$

$$X_s = 3.63*\frac{3.9}{14.18} \approx 1$$

$$Q \quad \frac{R_L}{1+Q^2} < R < R_L$$

$$\therefore \quad X_{L1} = Q*R = 5*3.63 = 18.2$$

$$X_{L1}' = X_{L1} + |X_s| = 18.2+1 = 19.2 \qquad \therefore \quad L_1 = \frac{19.2}{2*\pi*2.44G} = 1.25nH$$

$$X_{c1} = \frac{R_s(1+Q)^2}{Q-\sqrt{\frac{R_s}{R_L}(1+Q)^2-1}} = 23.26 \qquad \therefore \quad C_1 = \frac{1}{2*\pi*2.44G*23.26} = 2.8pf$$

$$X_{c2} = R_L*\sqrt{\frac{R_s}{R_L}(1+Q)^2-1} = 47.1 \qquad \therefore C_2 = \frac{1}{2*\pi*2.44G*47.1} = 1.38pf$$

Then we get the C1=2.8pf, C2=1.38pf, L1=1.25nH where C1,C2 were implemented

by lumped elements and L1 was made by two bond wires.

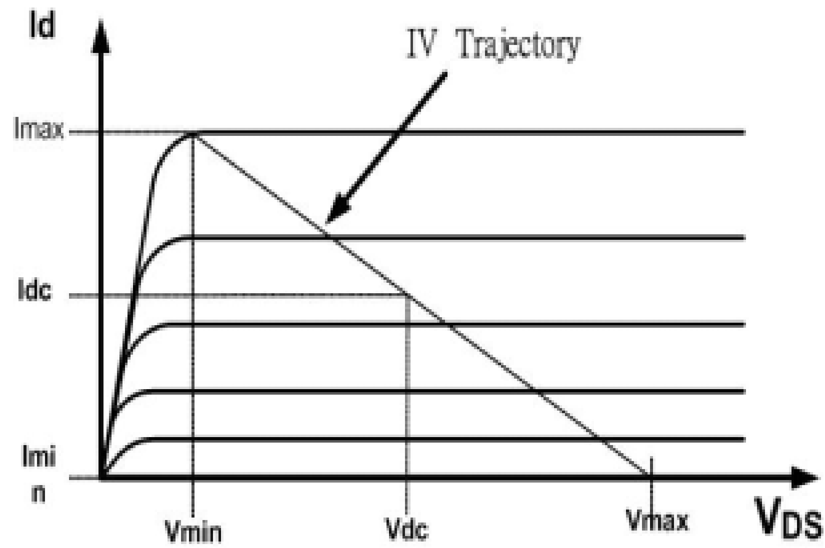


Fig. 3-6 Basic I-V curve for NMOS

Although we can reduce the parasitic capacitance by using substrate bias, the large current and voltage swing still result in oxide breakdown phenomenon. The Fig. 3-6 shows the basic I-V curve for NMOS. Imax means the maximum current of the transistor, and Imin means the minimum current of the transistor. Vmin means the minimum voltage difference between the drain and source of the transistor. Vmax means the maximum voltage difference between the drain and source of the transistor.

Therefore, the transistor voltage and current swing is shown as:

$$V_{swing} = V_{\max} - V_{\min} \tag{3.1}$$

$$I_{swing} = I_{\max} - I_{\min} \tag{3.2}$$

So the adjust resistor value for full ac swing can be obtained:

$$R_{opt} = \frac{V_{swing}}{I_{swing}} = \frac{V_{\max} - V_{\min}}{I_{\max} - I_{\min}} \tag{3.3}$$

From (3.1) (3.2), the root mean square of voltage and current can be shown as:

$$V_{rms} = \frac{V_{swing}}{2\sqrt{2}} \quad and \quad I_{rms} = \frac{I_{swing}}{2\sqrt{2}} \tag{3.4}$$

Then, the output power can be expressed:

$$P_{rf} = V_{rms} I_{rms} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \tag{3.5}$$

And, the dc voltage, current, and power can be shown as:

$$V_{dc} = \frac{(V_{max} + V_{min})}{2} \tag{3.6}$$

$$I_{dc} = \frac{(I_{max} + I_{min})}{2} \tag{3.7}$$

$$P_{dc} = \frac{(V_{max} + V_{min})(I_{max} + I_{min})}{4} \tag{3.8}$$

From above formulas, we can determine the transistor size of the single-transistor single-ended output stage.

Because the voltage swing is very large in the power amplifier and usually results in oxide breakdown phenomenon. In order to alleviate this problem, cascode topology is chosen. If the bias of the cascode device (M2) is set appropriately, the maximum stress on the gate-drain oxide of M2 is

$$V_{OX(MAX)} = V_{OUT(MAX)} - V_{BIAS}, \tag{3.9}$$

where V_{BIAS} is the bias voltage on the gate of the cascode device. In the case of the single transistor stage, the maximum oxide stress is

$$V_{OX(MAX)} = V_{OUT(MAX)} - V_{IN(MIN)}, \tag{3.10}$$

which places a limit on the available output voltage swing.

.

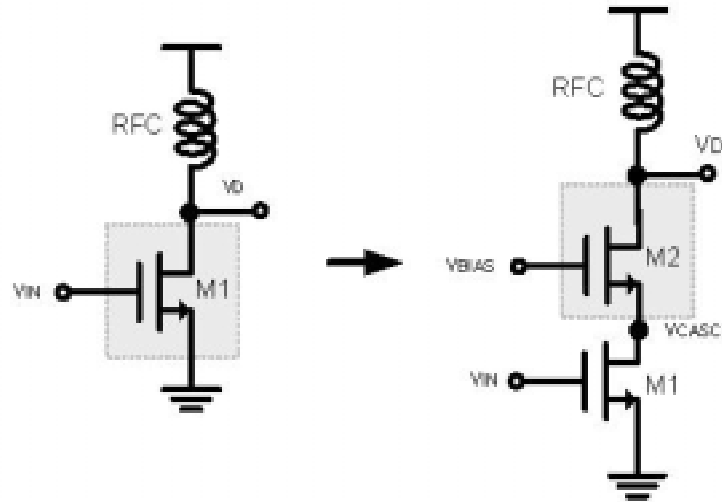


Fig. 3-7 Single transistor modify to cascade topology

In cascode structure, the oxide stress on the lower device (M1) is now limited to

$$V_{OX} = V_{CASC} - V_{IN} \tag{3.11}$$

which may or may not be a problem, depending on the voltage of the cascode node. To first order, the maximum voltage on the cascode node will be limited to

$$V_{CASC(MAX)} = V_{BIAS} - V_T \ . \tag{3.12}$$

The maximum voltage stress across the oxide of M1 is thus set by

$$V_{OX(MAX)} = V_{BIAS} - V_T - V_{IN(MIN)} \ , \tag{3.13}$$

It's a more reasonable value than in the single-ended case. As the result, the maximum output voltage is now increased to

$$V_{OUT(MAX)} = V_{BIAS} + V_{OX(MAX)} \ , \tag{3.14}$$

It is apparent that the maximizing the bias voltage of the gate node of the cascode device will allow for the largest possible output swing, reducing the amount of the current that needs to be drawn from the supply to deliver required output power. Another benefit of the cascode structure is that it insulates the output node from the input node. Furthermore, the cascode structure can reduce the impact of the Miller capacitor, by reducing the gain across the feedback capacitor of the MOS device. Based on this reason,

the size of the upper common gate cascode MOS is chosen as the same with the lower common source MOS to get the same transconductance, g_m, and reducing the Mill effect.

Equation (3.15) shows the voltage gain of the cascode structure. R_L is the load resistance seen by drain of the common gate cascode MOS, M2 and $g_{m1,\ 2}$ are the transconductance of the M1, 2 respectively. Also, $r_{o1,\ 2}$ are the output resistance of the M1, 2 respectively.

$$A_v \approx g_{m1}\left[\left(g_{m2} r_{o2} r_{o1}\right) \| \left(R_L\right)\right] \tag{3.15}$$

Since the R_L is very small compared with $g_{m2}r_{o2}r_{o1}$, the voltage gain of the cascode stage can be simplified as

$$A_v \approx g_{m1} R_L \quad , \tag{3.16}$$

which is the same as the single common source amplifier. Though, we can merge cascode structure as the single MOS structure to find its I-V curve.

To get the large power output , the output stage have to driving large current and voltage swing, but the MOS device have poor current driving capability. It's a good method to use the differential pair to provide twice the available voltage and the amount of current required of each side can be half of the single-ended one to achieve the same output power. This reduction in current allows that the devices used in the output stage of the PA to be more reasonably sized while the efficiency doesn't increase.

The fully differential and cascade output stage with substrate bias topology was shown in Fig. 3-8.

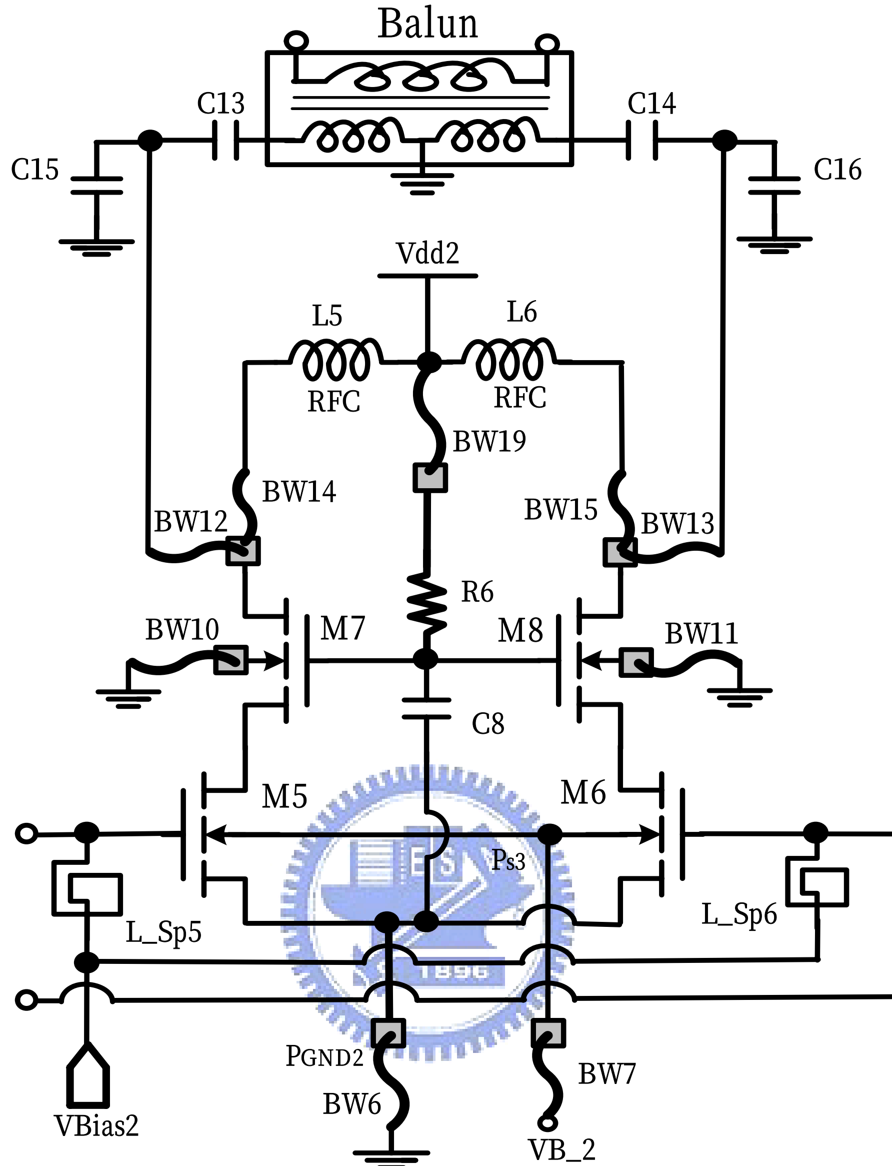


Fig. 3-8 Fully differential and cascade of output stage using MOS devices with positive substrate bias

3.2.2 Driving Stage

Driving stage also names pre-amplifier. It's used to drive the output stage of PA A band pass gain stage based on inductive load is employed as the input stage (Fig. 3-9). Inductive loads suit low voltage operation design since they don't consume dc headroom. Thus the inductor tunes out the capacitance of the gate of the output stage transistor. Sometimes, we placed a capacitor on drain which can resonant with the inductor in the band we design. Besides, the cascade transistor is used to reduce the miller capacitance

and to alleviate the gate-drain breakdown phenomenon. The main design issues are to decide the operation class and to adjust LC resonates at the desired frequency.

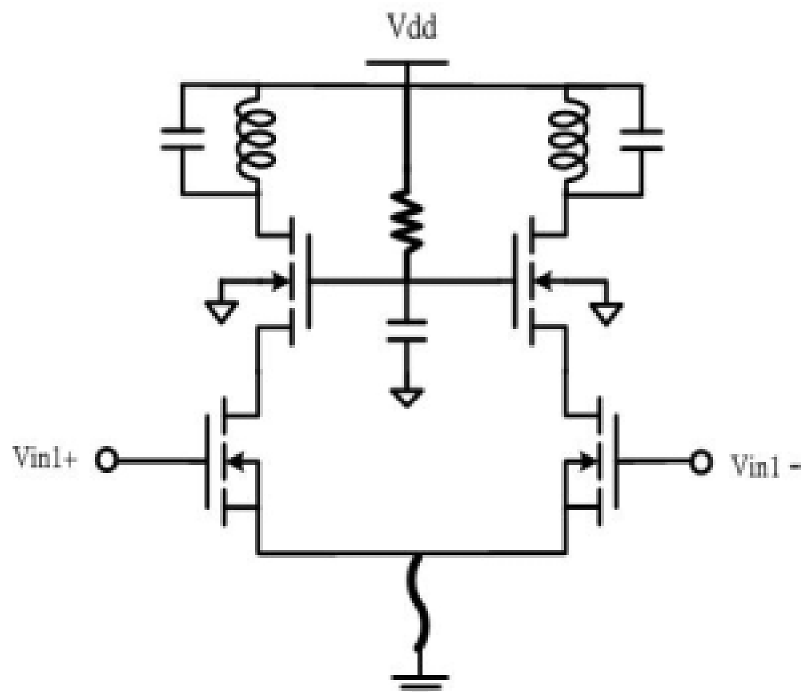


Fig. 3-9 Basic driving stage (pre-amplifier)

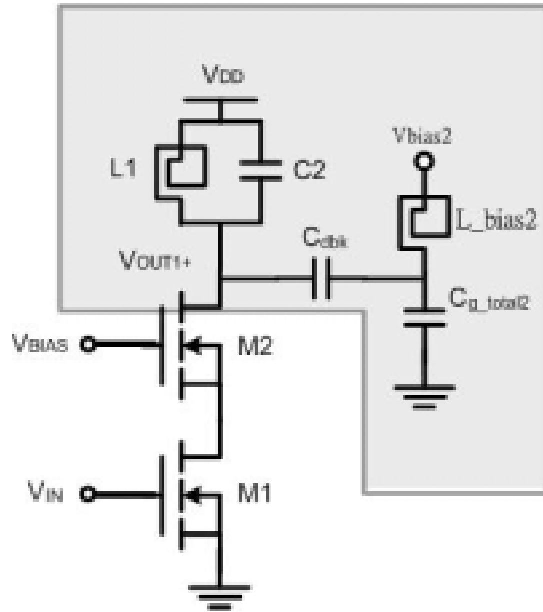
If gm1 equal 0.6 (A/V), we can get the voltage gain from equation 3.5

$$A_v(output\ stage) = -g_{m1}R_{opt} = -0.6*4 = -2.4$$

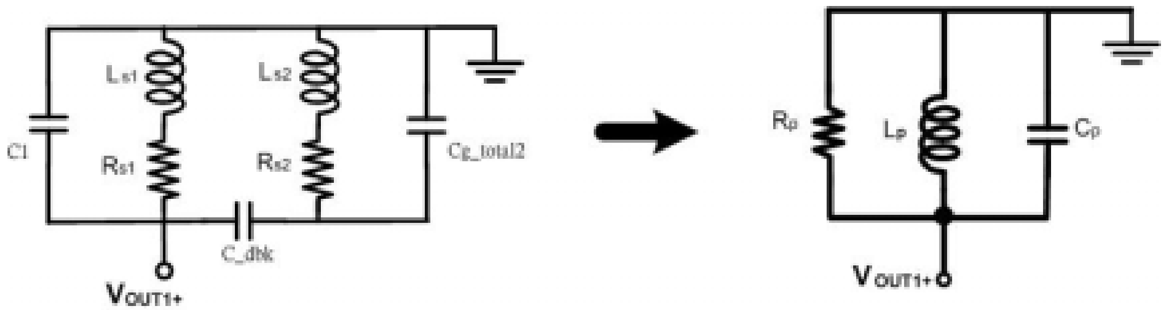
From equation 3.5 we can know our single-ended input voltage swing of output stage is about 2.1 V. Then, form the typical input power level is 0dBm (0.636 voltage swing), we can get

$$A_v(driver\ stage) = \frac{V_{out}}{V_{in}} = 3.3 = -g_{m1}R_L$$

Then we can get the R_L=33 at least when gm1= 0.1. The loading of single-ended pre-amplifier stage can be simplified as Fig. 3-10.



(a)



(b)

Fig. 3-10 (a) Pre-amplifier stage (b) Derivate RL of Pre-amplifier

The series resistance (R_s) of the spiral inductor L1, 2.12nH, is about 4Ω. The series resistance (R_s) of the spiral inductor L2, 0.5nH, is about 1Ω. Utilizing equation (3.17) and equation (3.18), the series R_s-L_s circuit can be replaced by an equivalent

$$R_p = R_s\left(1+Q^2\right) \tag{3.17}$$

$$L_p = L_s\left(\frac{Q^2+1}{Q^2}\right) \tag{3.18}$$

parallel circuit consisting of R_p-L_p, as shown in Fig. 3-10(b). R_p is just the loading resistance of the Pre-amplifier stage. The quality factor of this spiral inductor is around 7.

Substituting this value into equation (3.17), we can get the R_L approximately 160Ω. Consequently, the transconductance of the Pre-amplifier transistor can be found. The device size can be determined too.

3.2.3 Stability Enhanced Circuits and Grounded Substrate

As stated earlier, the stability is a very critical issue for high-output-power PA. The new stability factor μ was defined for linear two port circuits using a geometrically approach. [14]

$$\mu = \frac{1-|S_{11}|^2}{|S_{12}S_{21}|+|S_{22}-S_{11}^*\Delta|}$$

$$\Delta = S_{11}S_{22}-S_{12}S_{21}$$

$$\nu = \frac{1-|S_{11}|^2}{|S_{12}S_{21}|-|S_{22}-S_{11}^*\Delta|}$$

$$\Delta = S_{11}S_{22}-S_{12}S_{21}$$

To increase stability, the substrate of the cascade device have to short to ground which shown as Fig. 3-11.

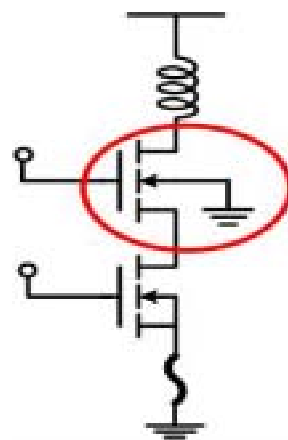


Fig. 3-11 Grounded substrate of cascade MOS devices

It needs to add the stability enhanced circuits to reach to unconditional stable.

The input port need to add a stability enhanced circuits which shown as Fig. 3-12. Rin (10 ohm) adds loss and stabilizes at higher frequencies. Lin(3.9nH), Cin(1.1pF) resonate at 2.4GHz, shorting Rin(10 ohm) that negating loss of gain at 2.4GHz due to stabilization.

Fig. 3-13 shows the stability factor μ in the designed circuit without the stability enhanced circuits. The circuit operates in unstable state at freq. 2GHz ~ 2.5GHz. Fig. 3-14 shows the stability factor μ in the designed circuit without grounded substrate. The circuit operates in unstable state except low freq. and about 2.4 GHz. Fig. 3-15 shows the stability factor μ in the designed circuit without stability enhanced circuits and grounded substrate. One can find the designed circuit gets more unstable.

Fig. 3-16 shows the stability factor μ in the designed circuit with stability enhanced circuits and grounded substrate is greater than 1 from 10MHz to 10GHz. Observably, the designed circuit will operate in unconditional stable state.

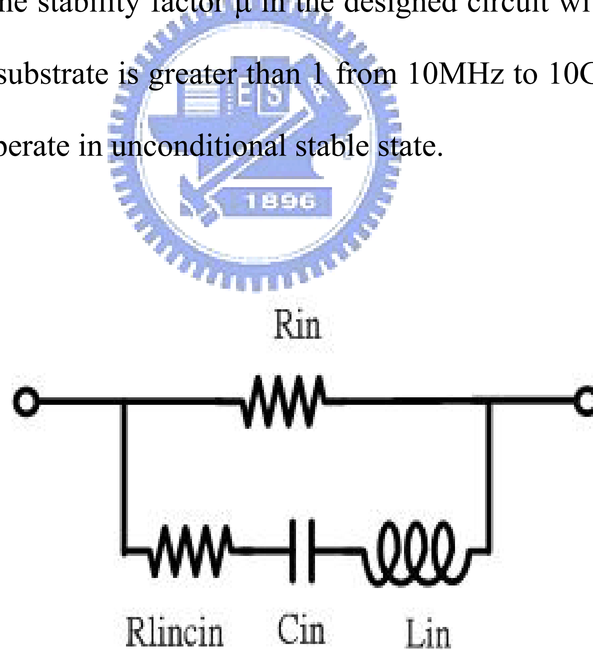


Fig. 3-12 Stability enhanced circuit

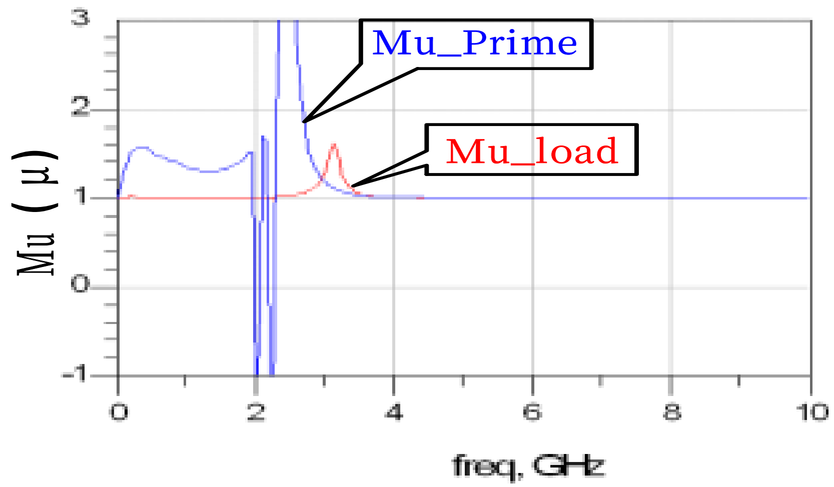


Fig .3-13 μ in the PA without stability enhanced circuits

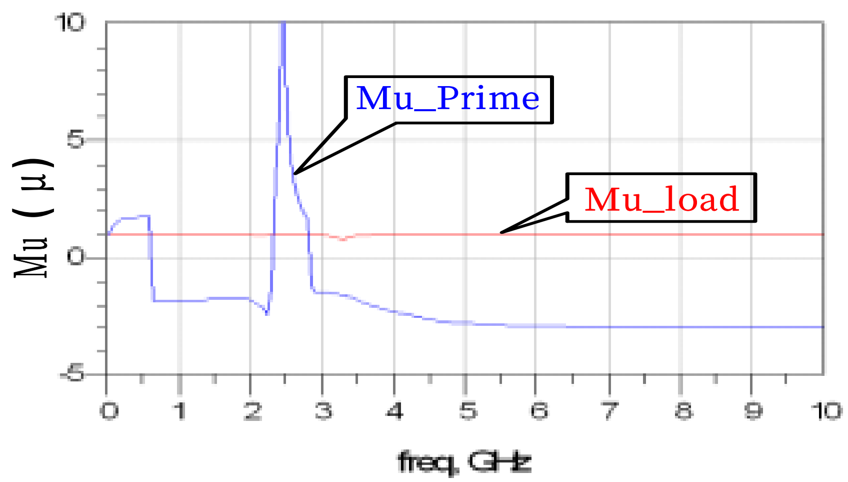


Fig .3-14 μ in the PA without grounded substrate

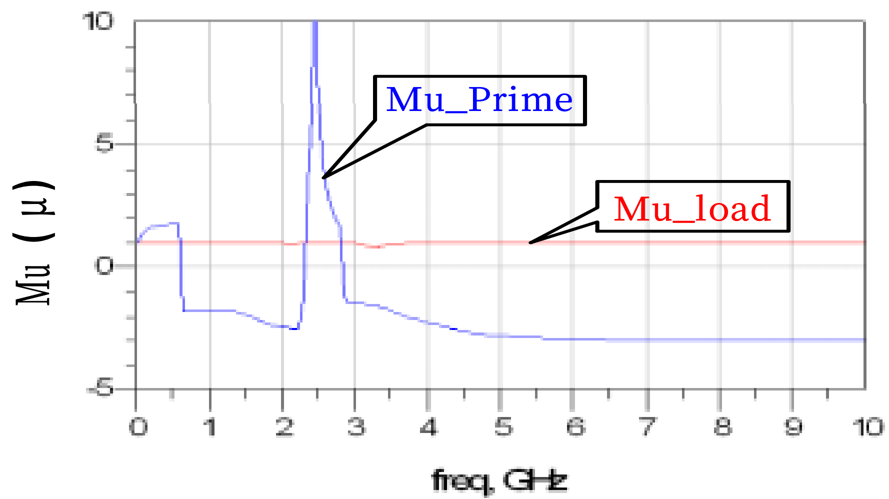


Fig .3-15 μ in the PA without stability enhanced circuit and grounded substrate

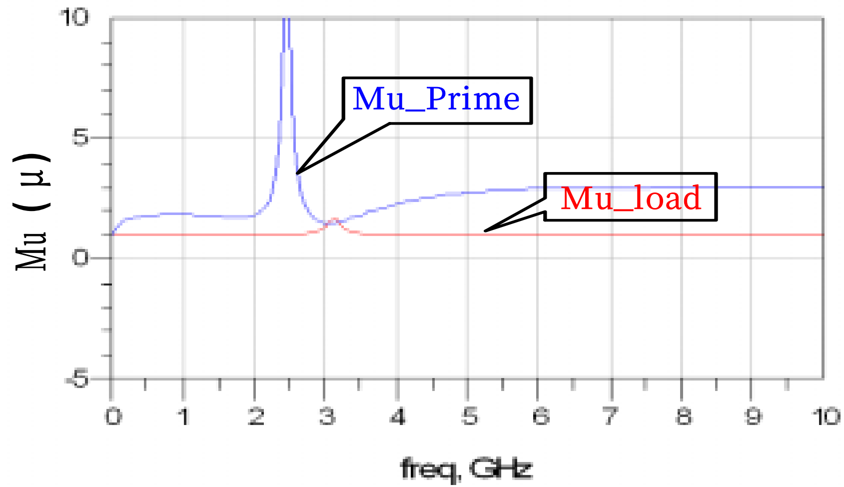


Fig .3-16 μ in the PA with stability enhanced circuit and grounded substrate

3.2.4 Current Capability Calculation and Layout Design

Because the large current of high-output-power PA will result in the reliability issue, it's important to calculate the current density capability. All vias and metals max. current density allowed spec was show as Table III

Table III Vias and metals current capability of TSMC 0.25µm CMOS process

	Current density capability (mA / μm)
Via 1	0.403
via 2	0.403
via 3	0.403
via 4	0.706
Metal 1	1
Metal 2	1
Metal 3	1
Metal 4	1
Metal 5	1.6

Four metals (metal 1~ metal 4) through by vias are used to alleviate the current density of MOS devices. The lateral structure was show as Fig. 3-17. Table V shows the compare the current capability of each MOS device. The current density of drain was less than the maximum current capability after using Table structure. Besides, the current capability of bonding wires is considered, too. The boning wire spec is as Table IV

Table IV The bonding wire spec

Aluminum Bonding wire (P/N)	AFW Al/Si 29s
Diameter (mil)	1
Fusing Current (amp)	0.45
Electrical Resistance (ohm/mm)	0.1
MELT Power (VA)	1
Elongation (%)	1~4
Breaking load (g)	18~21

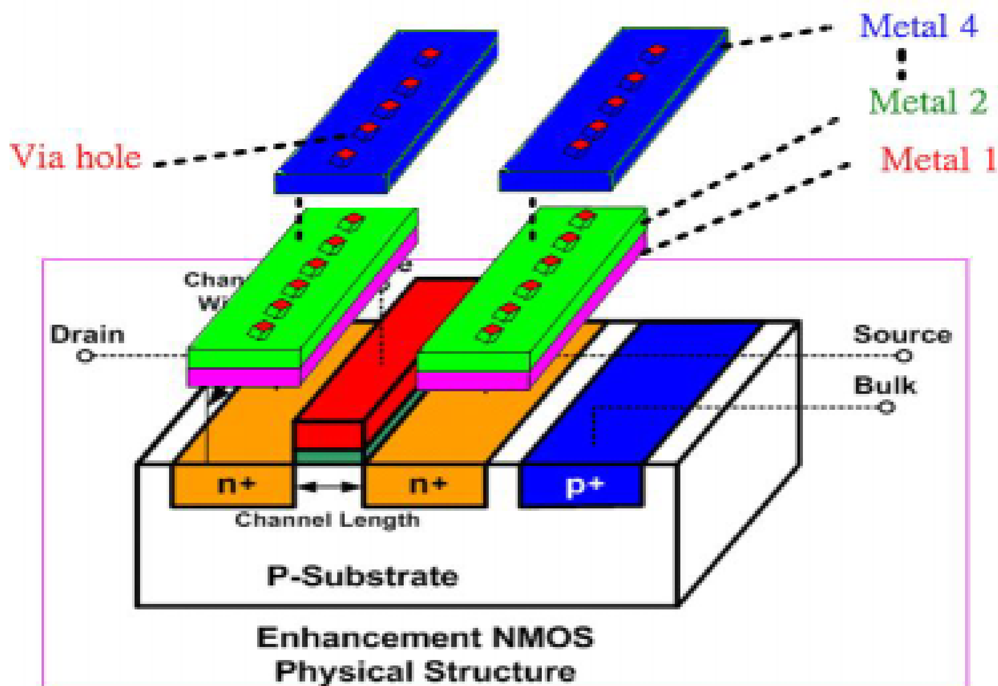


Fig. 3-17 Layout design for large current capability

Table V. Current capability design of MOS devices

	Driving stage	Current Source	Output Stage
MOS device	M1~M4	M9	M5~M8
Width / Length (μm/ μm)	10 / 0.35	10 / 0.4	10 / 0.35
M (parallel branches)	70	140	350
Total drain Current (mA)	40	80	390
Current / Drain (mA)	1.15	1.15	2.2
Metal 1 , W x L (um^2)	0.7x10	0.7x11	0.7x12
Metal 2 , W x L (um^2)	0.5x10	0.5x11	0.5x12
Metal 3 , W x L (um^2)	0.5x10	0.5x11	0.5x12
Metal 4 , W x L (um^2)	0.6x10	0.6x11	0.6x12
Max. Current Capability	2.3 mA	2.3 mA	2.3 mA

1896

3.3 Post-Simulation Results

We would present the post-simulation results of the high-output-power PA using MOS devices with positive substrate bias. All power amplifier were simulated by HSPICE、Advanced Design System, and were designed by TSMC 0.25 μm 1P5M CMOS technology with a 3.3V supply voltage.

The on chip bias circuit and the schematic of power amplifier using MOS device with positive substrate bias were shown as Fig. 3-18 and Fig.3-19. The components values of this PA are shown in Table VI. The expected bond-wires values and off-chip bias resistances' values of the PA is as the Table VII. The input and output match are off-chip in this design. The input and output matching were made with LC matching section. Fig. 3-20 shows the input matched to 48.8 ohm. Fig. 3-21 shows the output

matched to 4.51 ohm. The stability factor μ was greater than one form 10MHz to 10 GHz in this design. (Fig. 3-22). In order to avoid substrate forward bias, 0.4V was selected to be substrate bias voltage. The voltage swing of M5/M6 device's substrate and source were as Fig. 3-23. Vbs (0.495V) is smaller than Vth (0.518V) and the current (Ibs) is 90uA. It means that the designed substrate bias has no forward bias problem. The output power and power added efficiency (PAE) are presented in Fig. 3-24 and Fig. 3-25, respectively. The output power is 26.3dBm with 22.76% PAE at 0dBm input power. The drain efficiency is 22.8 %. The power gain is shown in Fig. 3-25.

Driving stage biases at class-A in order to trade off MOS devices size、linearity and efficiency. MOS devices size (W/L) of driving stage should be 700μm/0.35μm in class-A and 1500μm/0.35μm in class-AB if 800mw output-power is designed. Fig. 3-27 shows the P-1dB is -7dBm in class-A and -9dBm in class-AB. Table VIII compared the parameters of class-A and class-AB of driving stage. Linearity is the only one parameter that gets better (increasing 3.2%). It's the reason that class-A was chosen for driving stage. The four corners of the designed power amplifier were shown in Fig. 3-28.Table IX summarizes the simulation results of the PA.

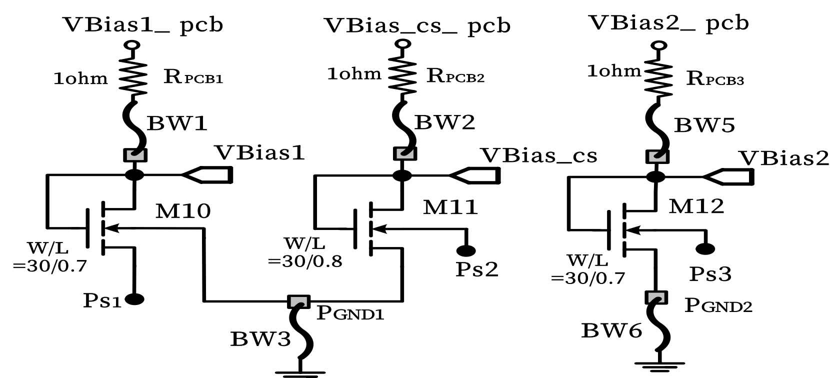


Fig. 3-18 On chip bias circuits of the designed power amplifier

Fig. 3-19 The high-output-power RF power amplifier using MOS devices with positive substrate bias

Table VI Components values and devices dimensions of the designed PA

Parameters	Value
M1 ~ M4 : W/L	700µm / 0.35µm
M5 ~ M8: W/L	3500µm / 0.35µm
M9: W/L	1400µm / 0.4µm
R1 ~ R2	100 Ω
R3 ~ R4	5 Ω
R5	10 kΩ
R6 ~ R7	100 Ω
R8 ~ R9	20 Ω
L1 ~ L2	3.9 nH
L3 ~ L4	70 nH
L5 ~ L6	1µH
L7 ~ L8	1 nH
L_Sp1 ~ L_Sp2	TSMC Spir 2
L_Sp3 ~ L_Sp4	Spir 1 (0.5 nH)
C1 ~ C2	1.1 pF
C3 ~ C4	2.8 pF
C5 ~ C6	10 pF
C7 ~ C8	1 pF
C9 ~ C10	2.2 pF
C11 ~ C12	10 pF
C13 ~ C14	1.6 pF
C15 ~ C16	3.5 pF
C17 ~ C18	70 pF

Table VII Bond wires expect inductance and resistance

	Parameters	
Bonding wire	**Inductance**	**Resistance**
BW1,BW2,BW7,BW12,BW13	1nH	0.1 ohm
BW3,BW18	0.5nH	0.05 ohm
BW4,BW5,BW14,BW15	2nH	0.2 ohm
BW10,BW11, BW16,BW17	1.5nH	0.15 ohm
BW6	0.3nH	0.03 ohm
BW8,BW9	3.3nH	0.33 ohm

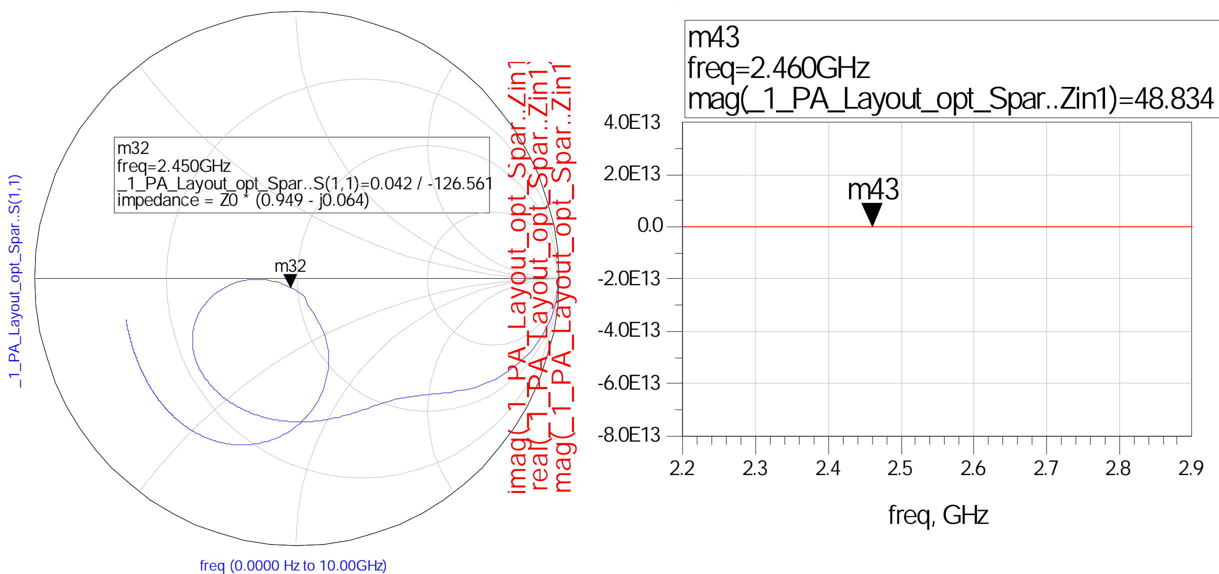


Fig. 3-20 Input matching impedance of simulation results

Mag (R_opt) = 4.51 ohm

Real (R_opt) = 4.49 ohm

Imag (R_opt) = 0.27 ohm

Fig. 3-21 Output matching impedance of simulation results

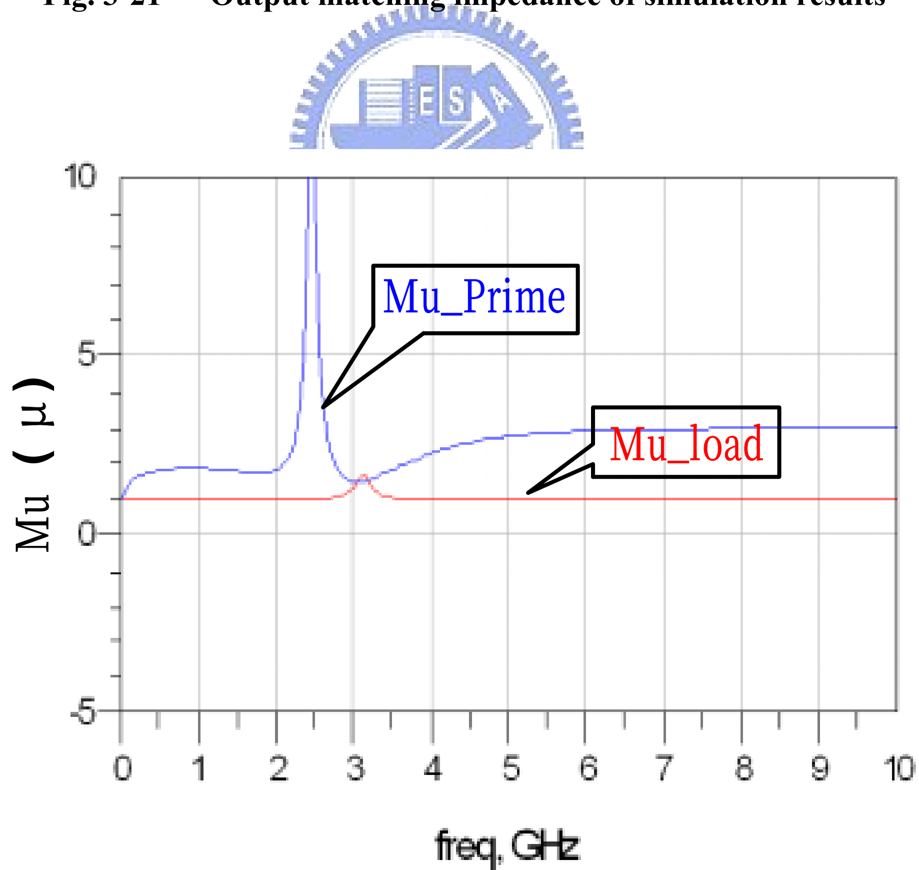


Fig. 3-22 Stability factor μ of input/ output stage

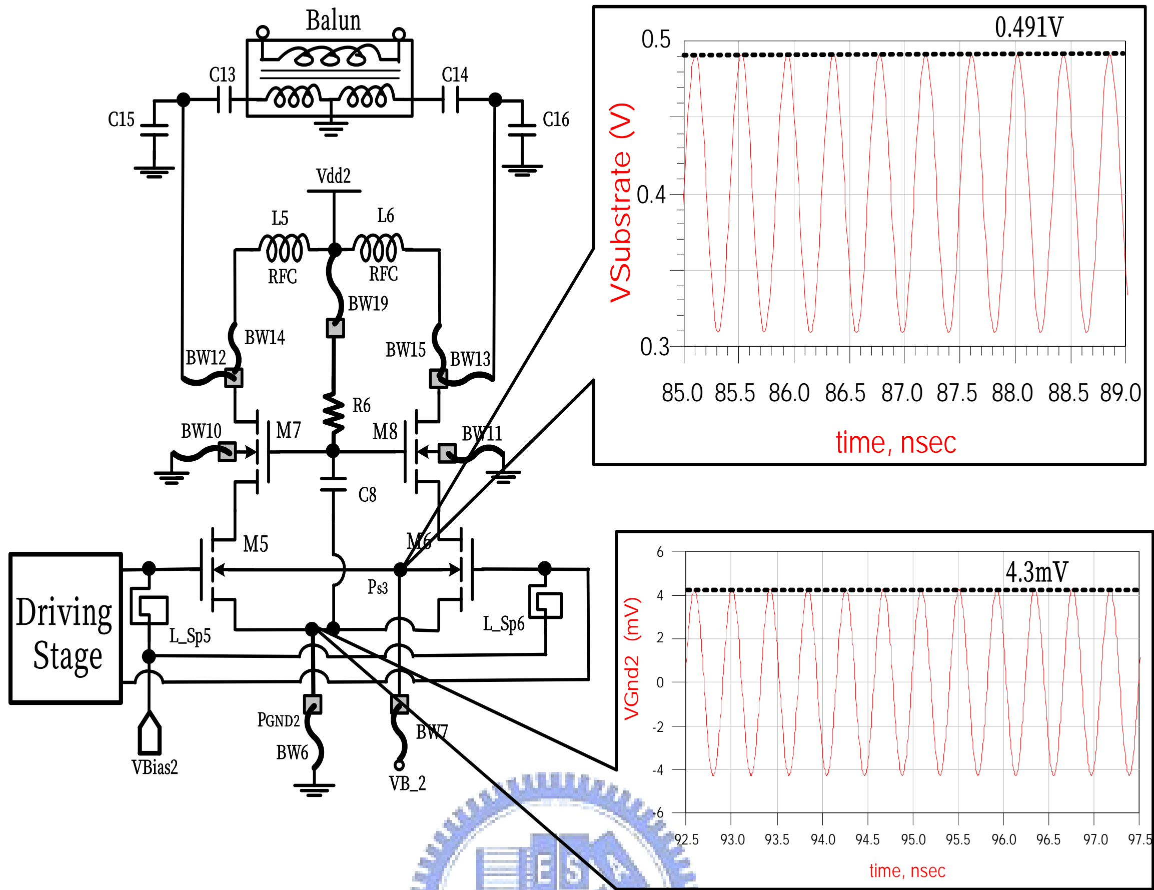


Fig. 3-23 Voltage swing of M5/M6 device's substrate and source

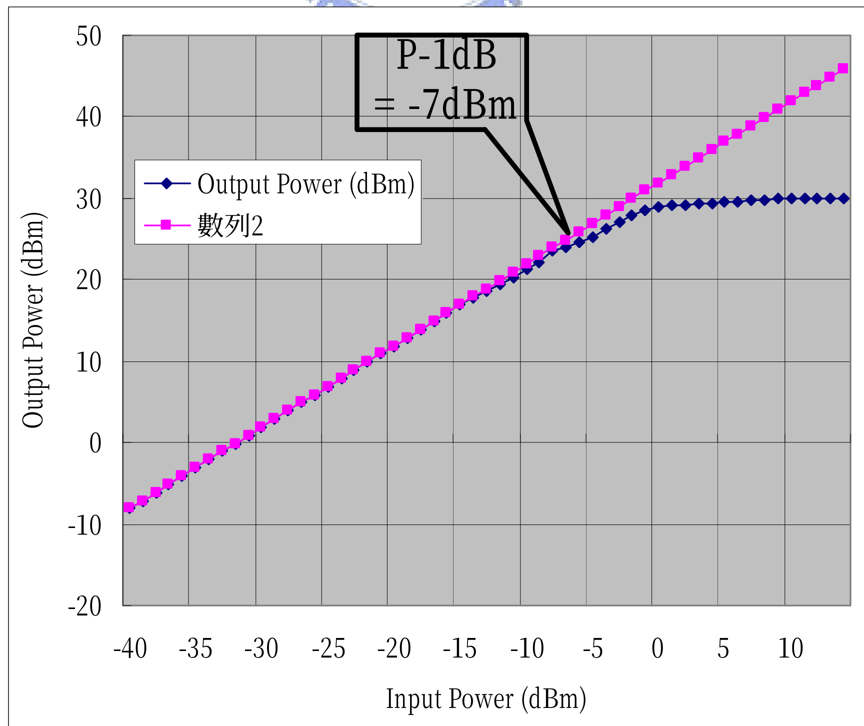


Fig. 3-24 Simulated output power vs. Input power

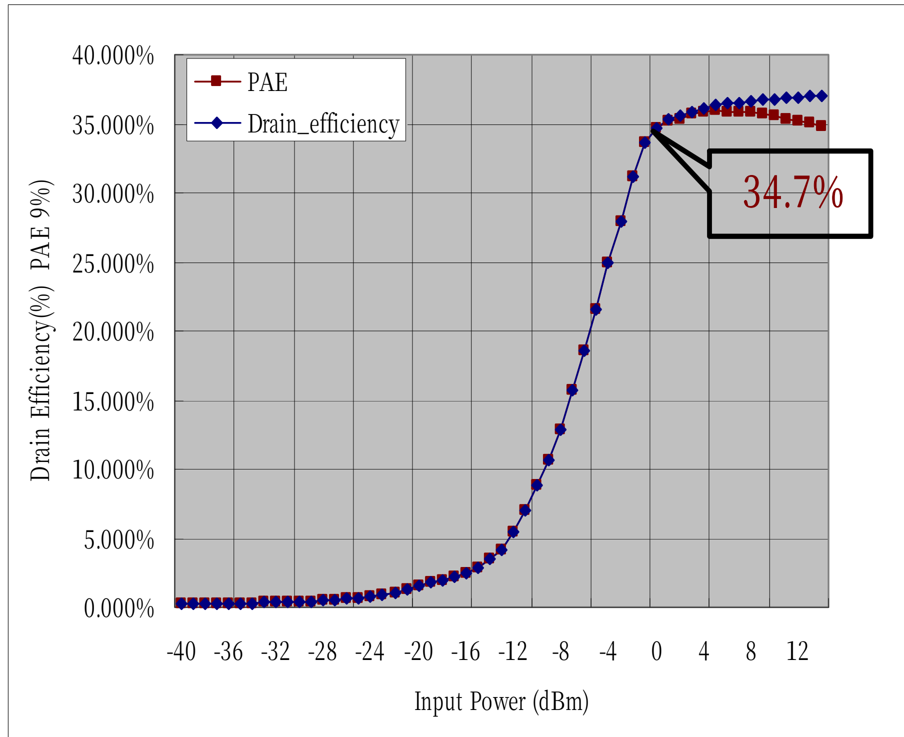


Fig. 3-25 Simulated power added efficiency (PAE) vs. Input power

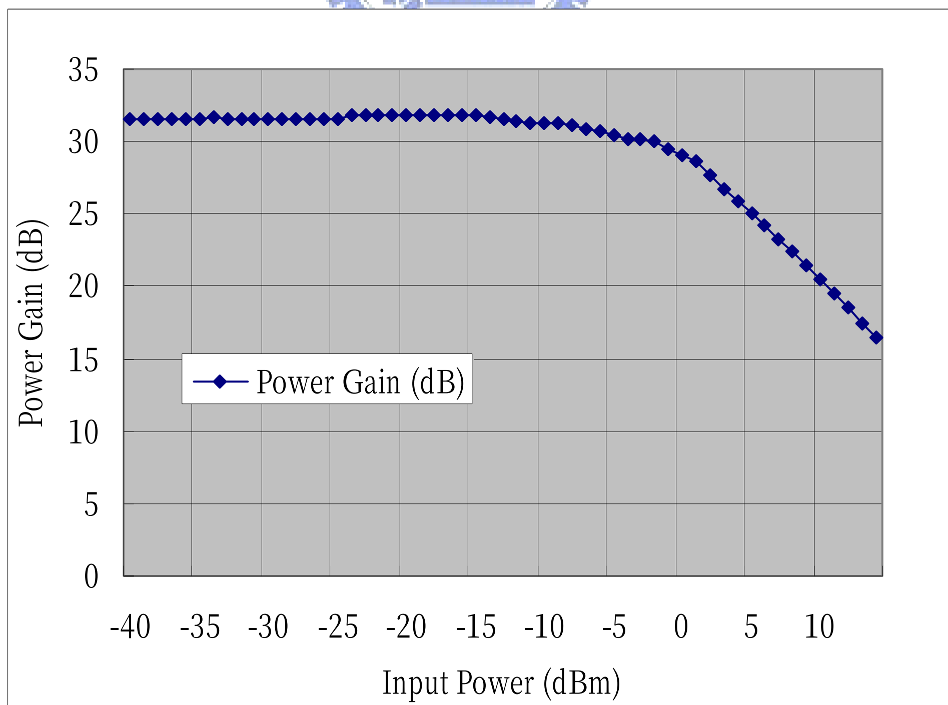


Fig. 3-26 Simulated power gain vs. input power

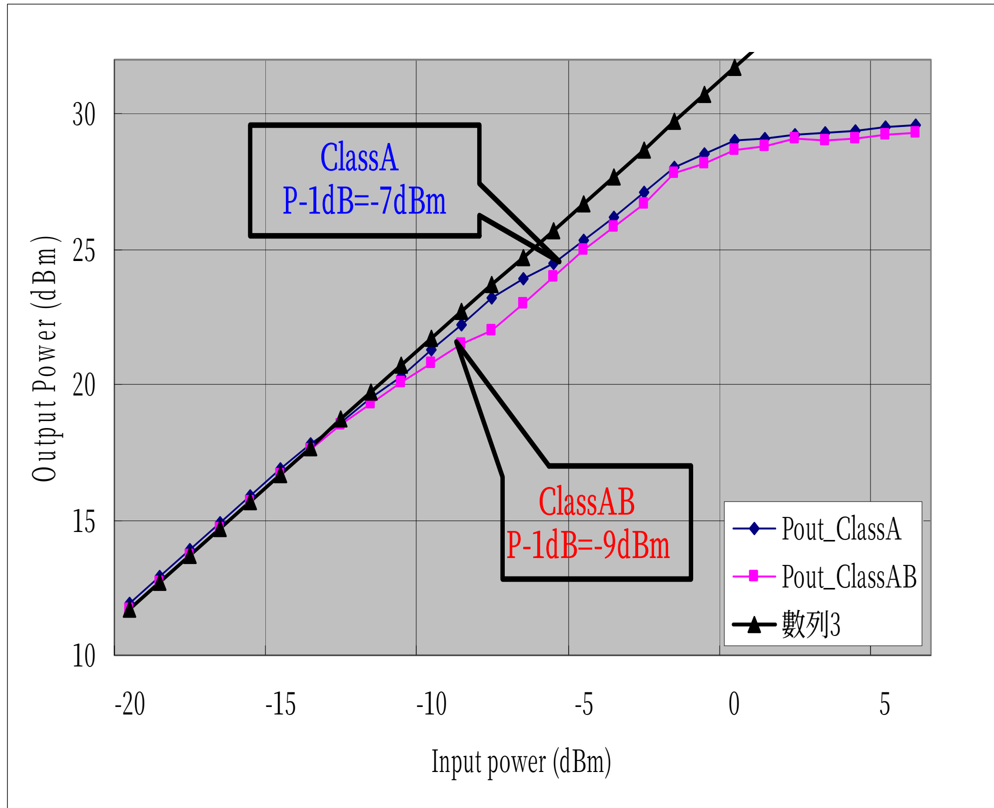


Fig. 3-27 P-1dB of class-A and class-AB of driving stage

Table VIII Compared the parameters of class-A and class-AB of driving stage

	Class A	Class AB
VBias1	1.7	0.9
MOS device size : W/L(μ m/ μ m)	700 / 0.35	1500 / 0.35
P-1dB (dBm)	-7	-9
PAE (%)	34.7	37.9

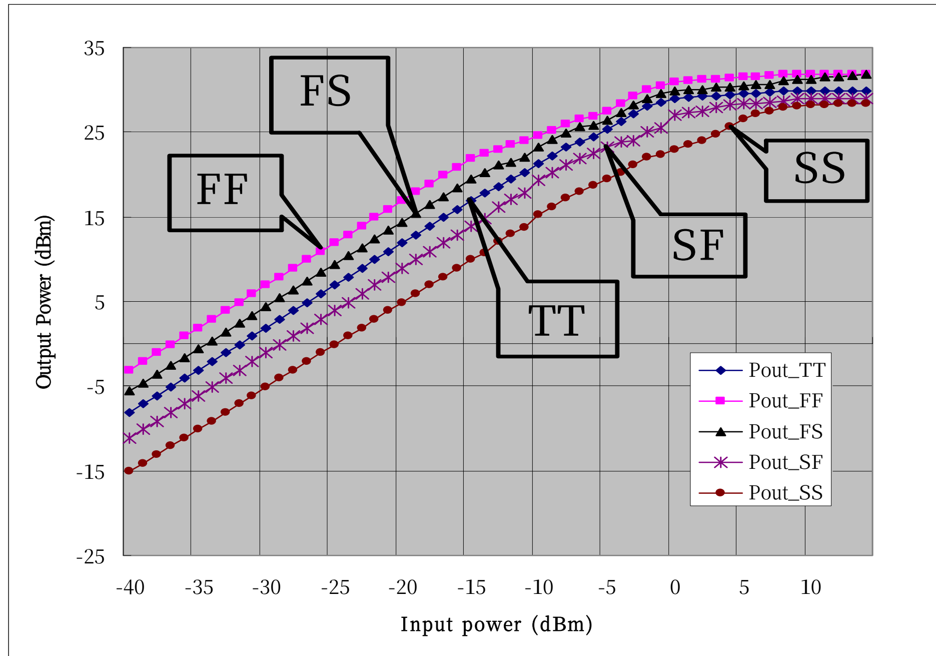


Fig. 3-28 Four corners of the designed power amplifier

Table IX Summary of post-simulated results

Technology	**TSMC 0.25 μ m 1P5M CMOS**
Supply Voltage	**3.3 V**
Frequency	**2.4 GHz**
Substrate Bias	**VB_1=0.2V, VB_2=0.4V**
Output Power	**29.2 dBm**
Power Gain	**29.2 dB**
Drain Efficiency	**34.73%**
Power Add Efficiency	**34.70%**
P-1dB	**-7 dBm**
Power Consumption	**2352 mW**

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 EXPERIMENTAL EQUIPMENTS SETUP

The experimental equipment setup for power amplifiers measurement and measured environment are shown in Fig. 4-1 and Fig. 4-2. The input signal is a 2.4GHz from signal generator. The input balun converts the single-ended signal to differential signal, and then applies this differential signal into device under test. The output balun converts differential signal to single again and sends it into the spectrum analyzer.

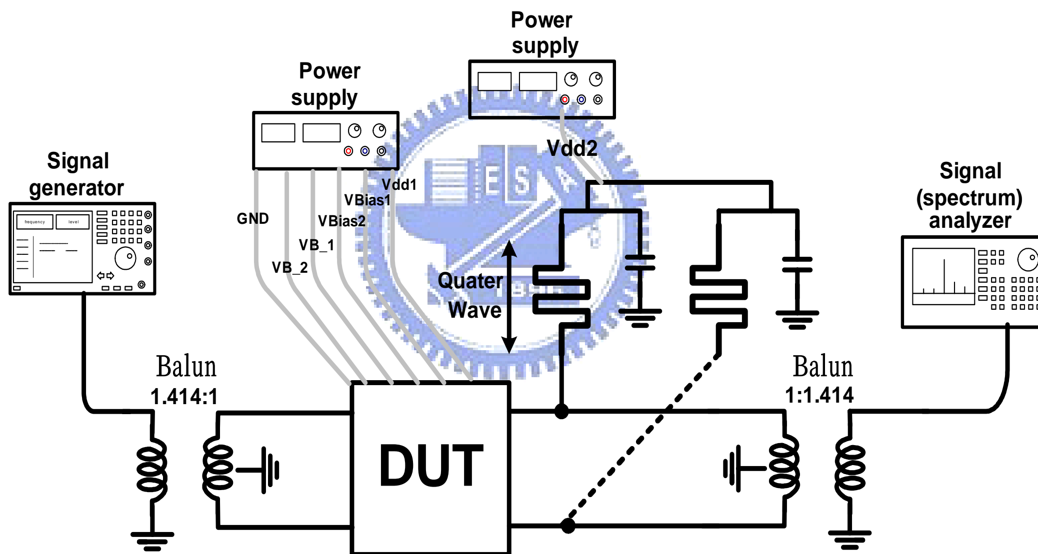


Fig. 4-1 Experimental equipments setup

Fig. 4-2 The photo of the measured environment

4.2 TESTING FIXTURE FOR THE DESIGNED POWER AMPLIFIER

. The overall layout and bonding pads description of this design was shown was Fig. 4-3. The chip area is 1.696 mm x 1.980 mm including pads. The testing fixture for the designed power amplifier was as Fig. 4-4 (a). The die was placed in the signal board by bonding wire. (Fig. 4-4(b))

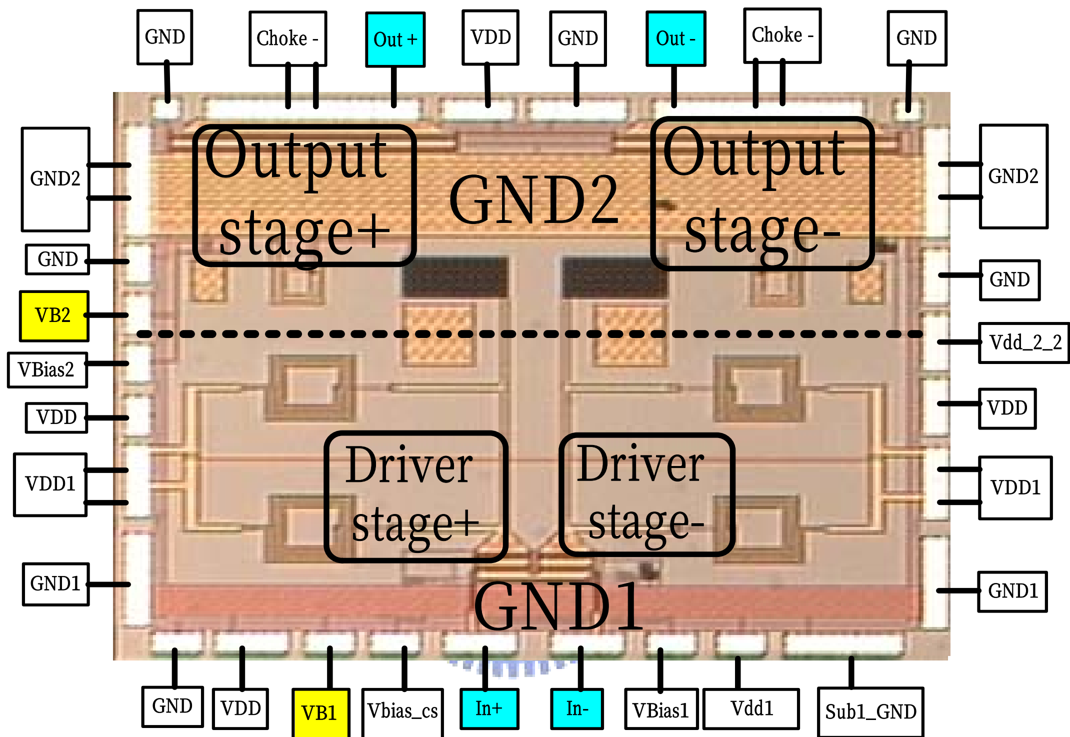
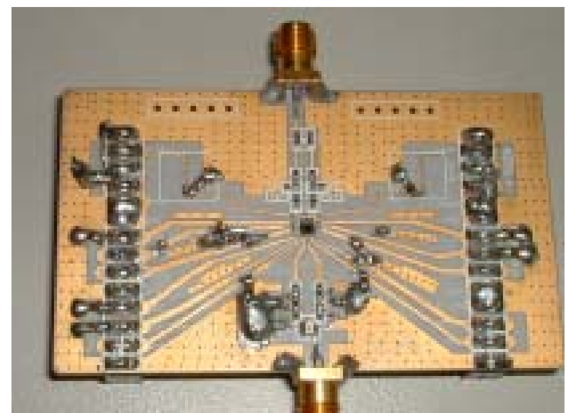


Fig. 4-3 Layout and bonding pads description of the PA



(a) **(b)**

Fig. 4-4 (a) Testing fixture (b) Signal board

4.3 MEASUREMENT

4.3.1 Input and Output Matching

The input matching should be matched to 50 ohm. After implementing the lump elements, input was matching to 62+j0.01 ohm as Fig. 4-5.

The output matching should be matched to about 4 ohm as we stated earlier (section 3.2.1).Fig. 4-6 shows the impedance of Rout is 3.8+j8.

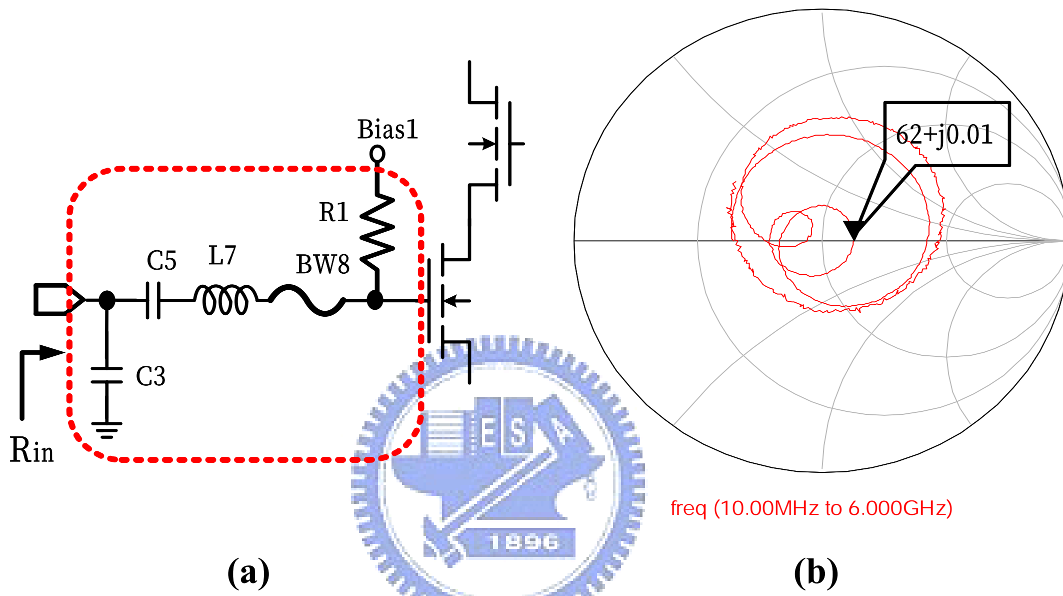


Fig. 4-5 (a) Input matching network (b) Matching Rin on the smith chart

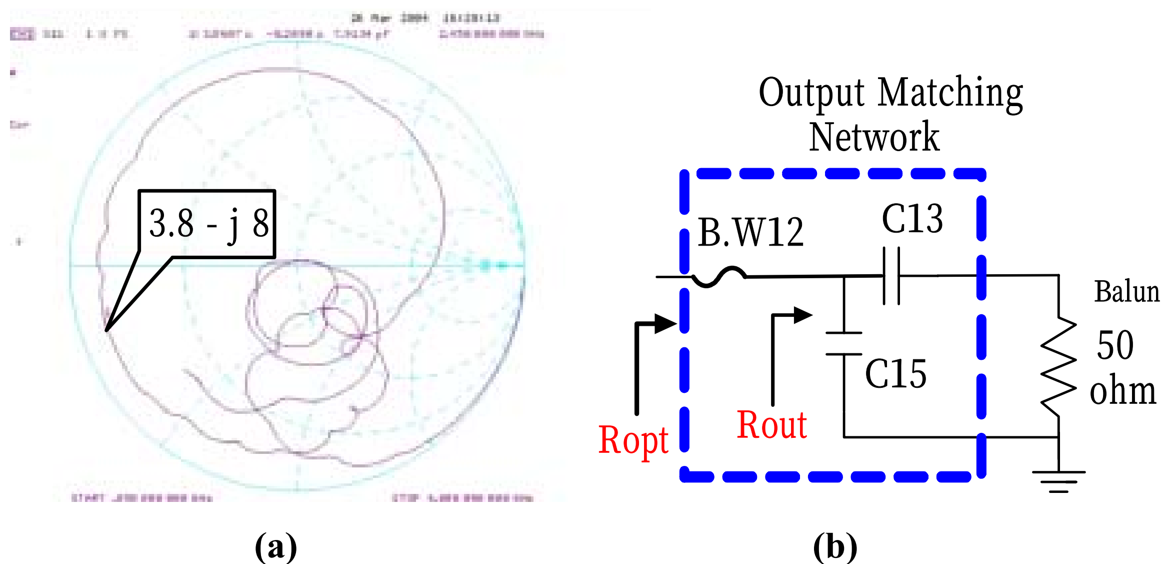


Fig. 4-6 (a) Matching Rout on the smith chart (b) Output matching network

4.3.2 Output Power Measurement

The frequency versus output power of this design is shown in Fig. 4-7. In this figure, we can find that the center frequency now is moved to 1.9GHz. We redesign the external components values of mating network to 1.9GHz as Table. X. Under 3.3V supply voltage, the output power(1.9GHz) is 20.06 dBm when the input power is 0 dBm as shown in Fig. 4-8. In the signal board, we add two baluns to transform the differential signals to single-ended output signal. The coaxial cable, SMA, and PCB have loss, too. Table XI shows the loss list. As the results, the output power of this design should be added 4.65 dBm for compensating all the losses. So the output power of this design is 24.7dBm at 1.9GHz and 19.8 dBm at 2.4GHz.

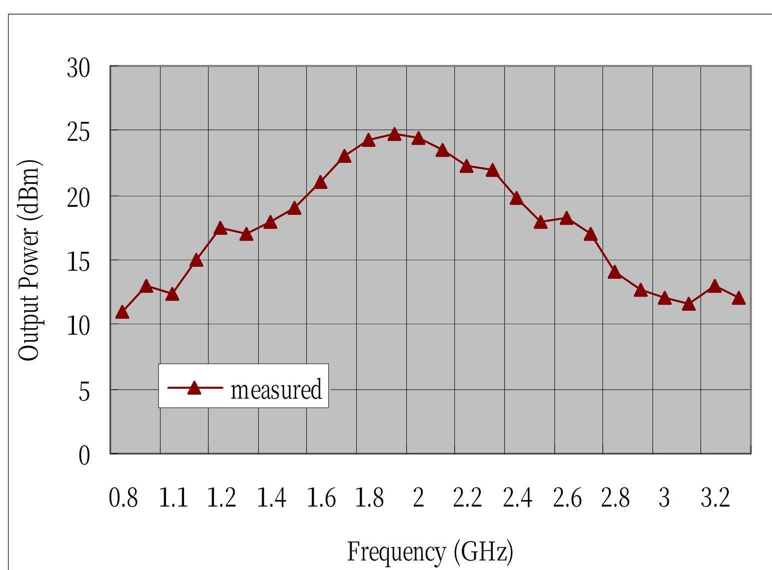


Fig. 4-7 Measured output power vs. frequency

Table X Redesign of external components values of matching circuits

Frequency	2.4GHz	1.9 GHz
L1~L2	3.9 nH	4.9 nH
C3~C4	1.5 pF	2.8 pF
C13 ~ C14	1.7 pF	1.2 pF

C15 ~ C16	3.6 pF	3.2 pF

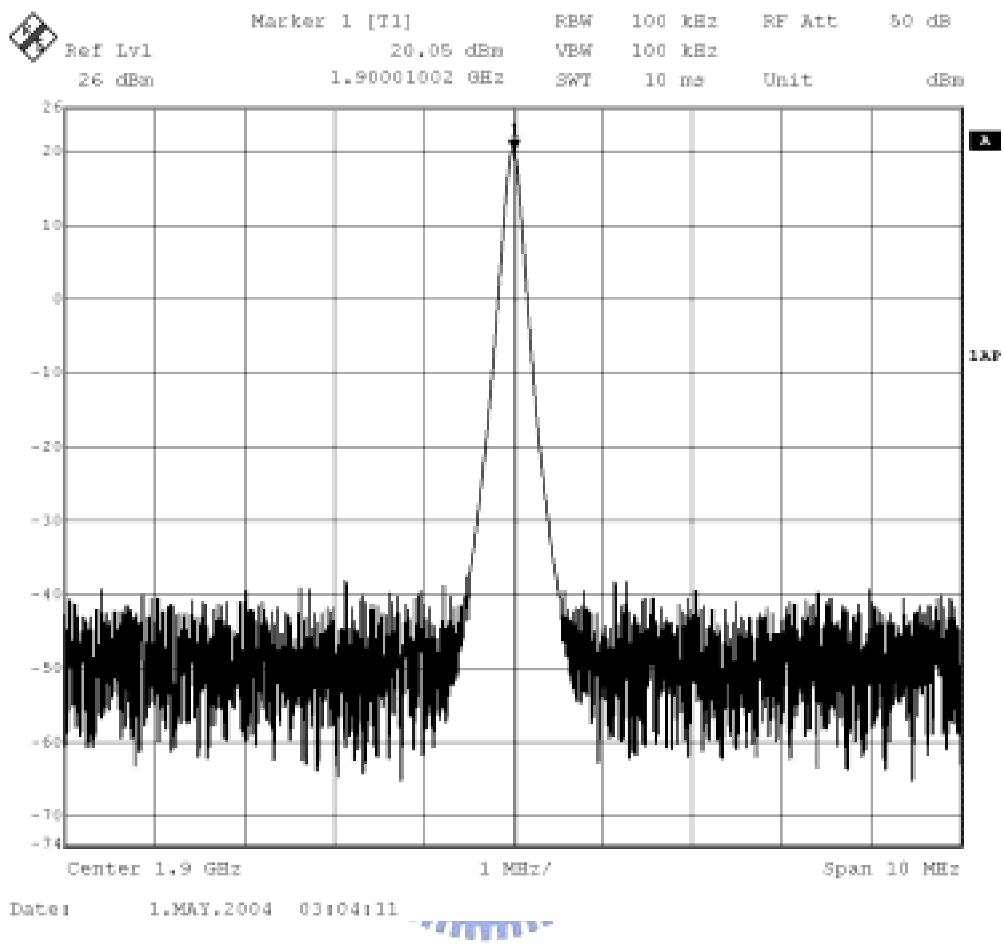


Fig. 4-8 Measured output power spectrum at 1.9GHz

Table XI The losses of measurement

	Loss (dBm)
Rg316 RF cable	2.3
PCB	0.65
SMA x 2	0.3
Balun x 2	1.4

4.3.3 Parameters and Chip's temperature measurement

To examine the temperature of chip which results from the large drain current is impartment. A LASER diode detected thermometer was used to measure the die's temperature.(Fig. 4-9) in this experiment.

Fig. 4-10 shows the temperature is 24.2˚C when power off.

Fig. 4-11 shows the temperature is 42.8˚C after turning on the power with fan 5 minutes

Fig. 4-12 shows the temperature is 64.8˚C after turning on the power without fan 5 minutes

Fig. 4-13 shows the P-1dB of simulation is -7dBm and measurement is -9dBm at 42.8 ˚C. Fig. 4-14 shows the drain efficiency of simulation is 20.3% and measurement is 15.14%. Fig. 4-15 shows the PAE of simulation is 20.23% and measurement is 15.1%.Fig. 4-16 shows the power gain of simulation is 26.3dBm and measurement is 24.7dBm Fig. 4-17 shows the ACPR of the PA is -43.07dBc at 400kHz and -55.82dBc at 600KHz when used GSM standard modulation as input. All parameters in this design were measured under the condition as Fig. 4-11. To redo the post simulation in 42.8˚C and compare to the measurement results is needed.

Fig. 4-9 The LASER diode detected thermometer

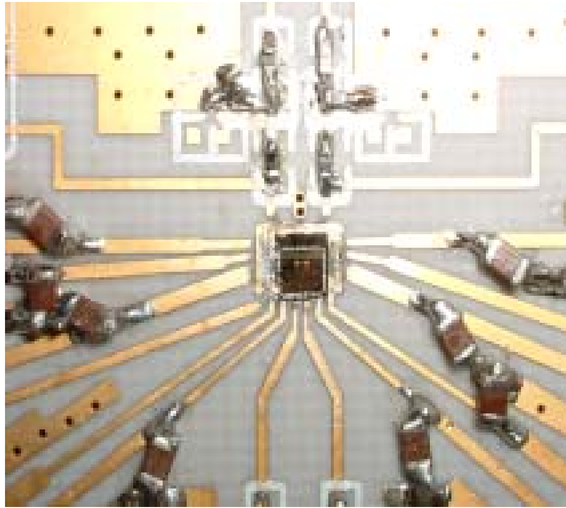


Fig. 4-10　Chip's temperature when power off

Fig. 4-11　Chip's temperature when power on with fan

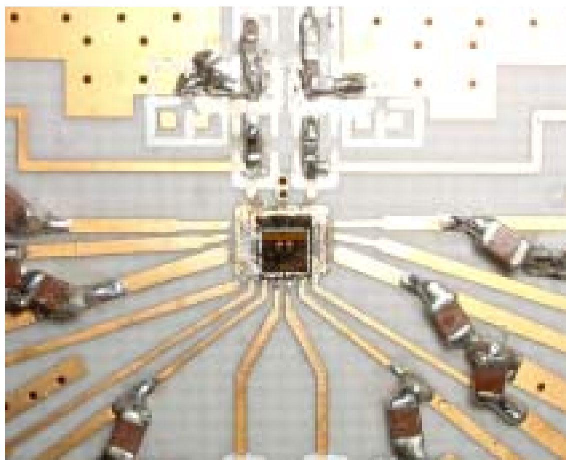


Fig. 4-12　Chip's temperature when power on without fan

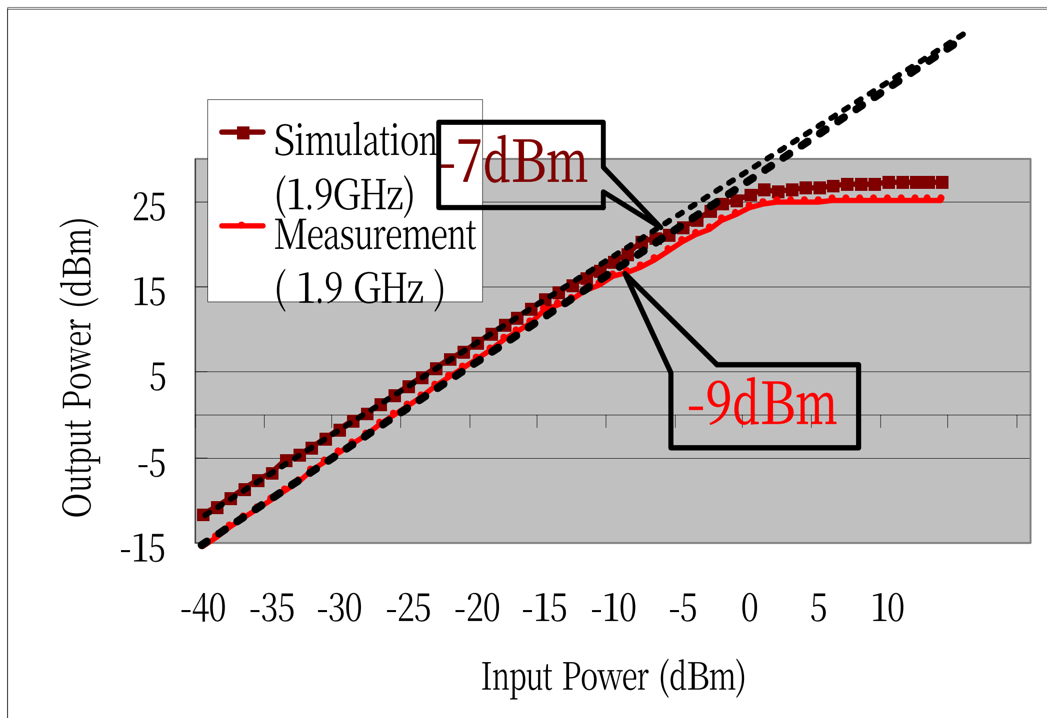


Fig. 4-13 Measured P-1dB at 42.8 ˚C

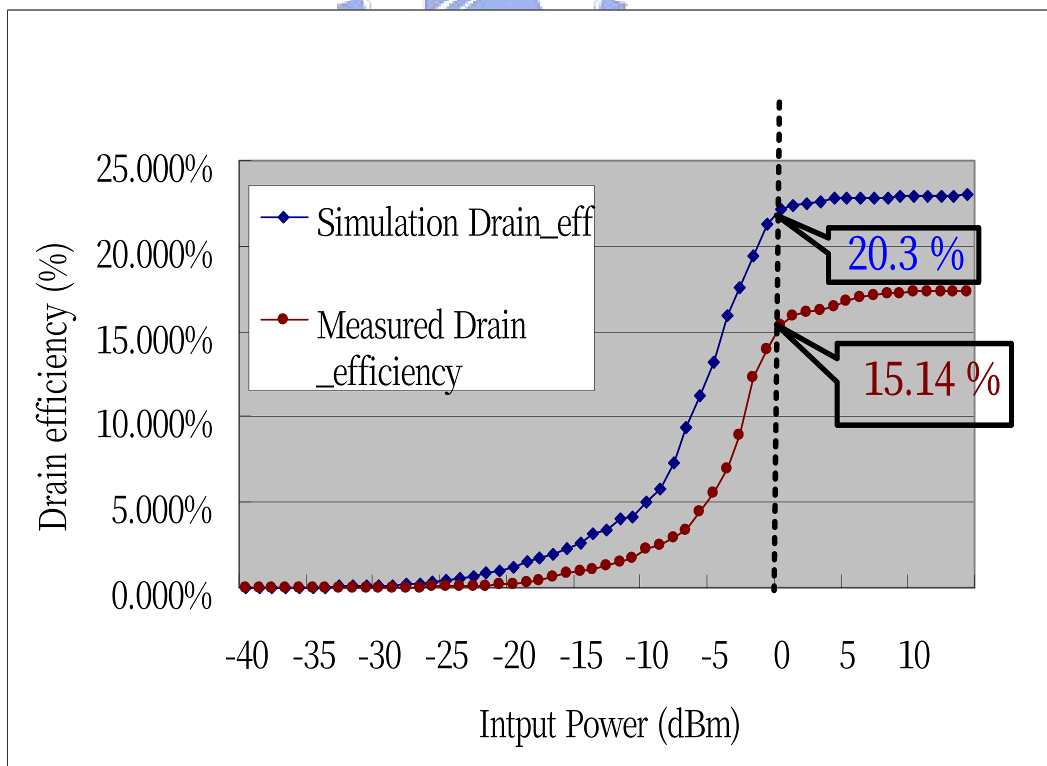


Fig. 4-14 Measured drain efficiency versus input power at 42.8˚C

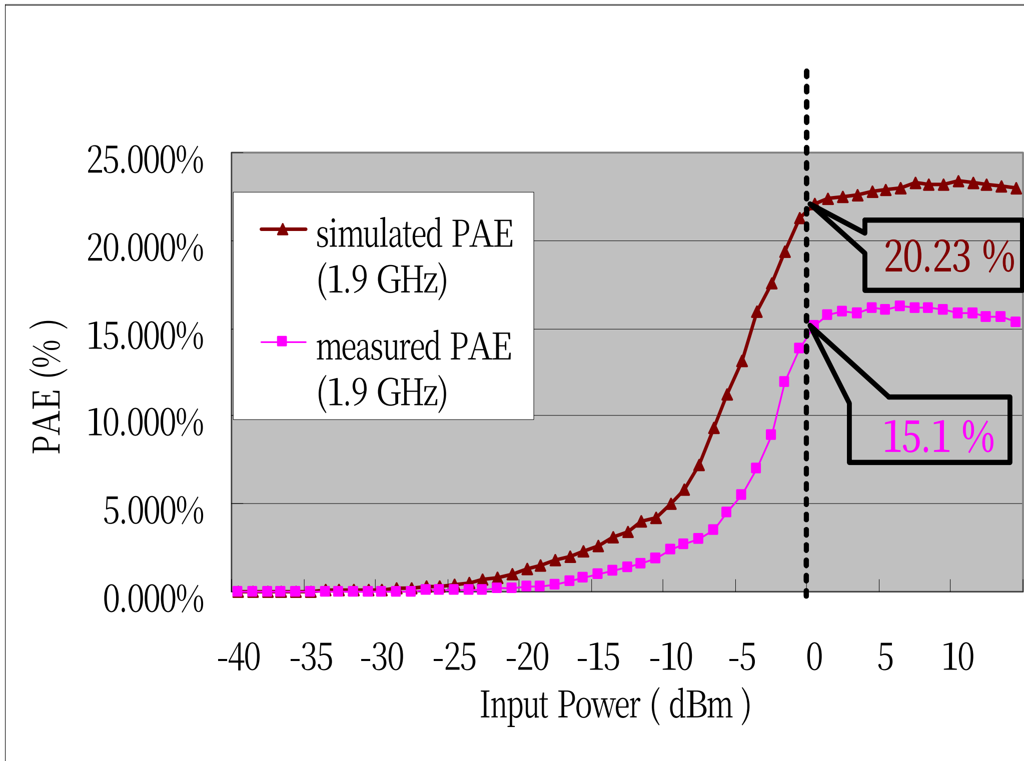


Fig. 4-15 Measured PAE versus input power at 42.8˚C

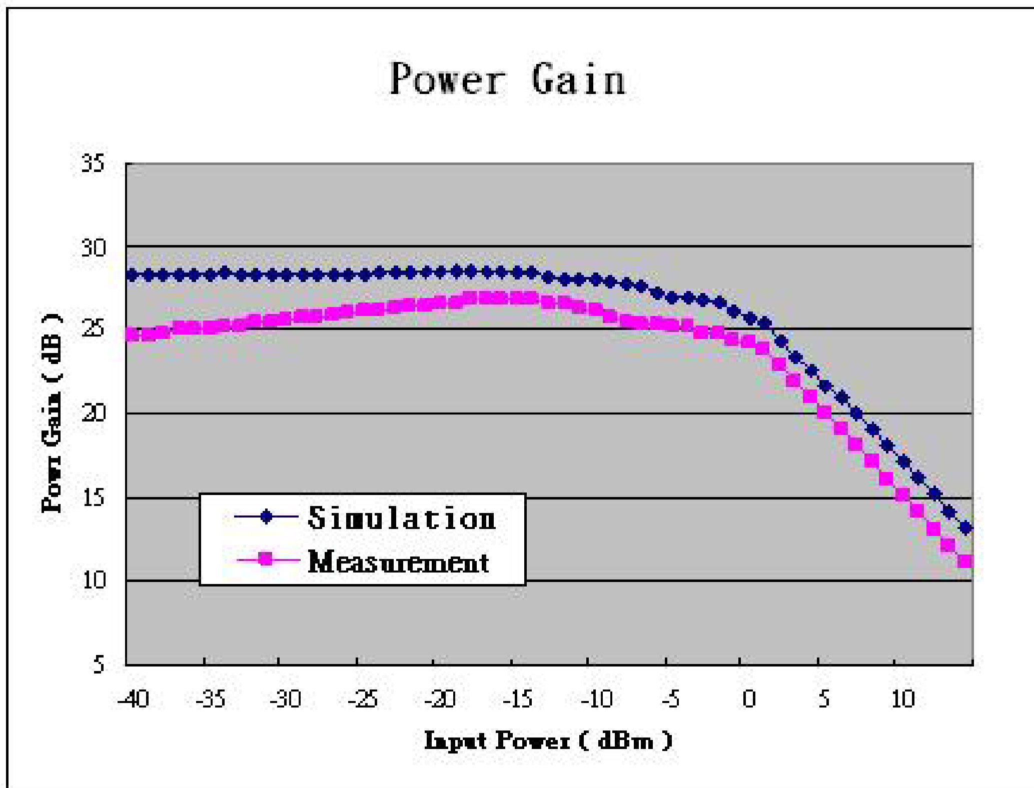
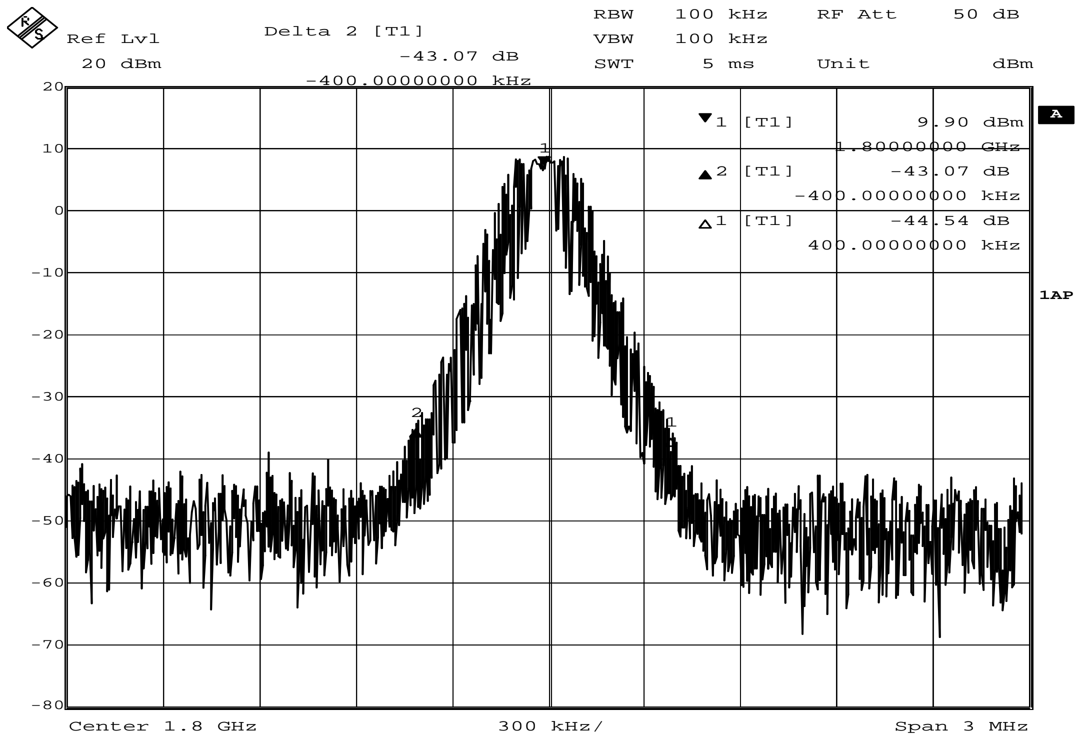
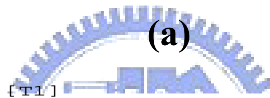
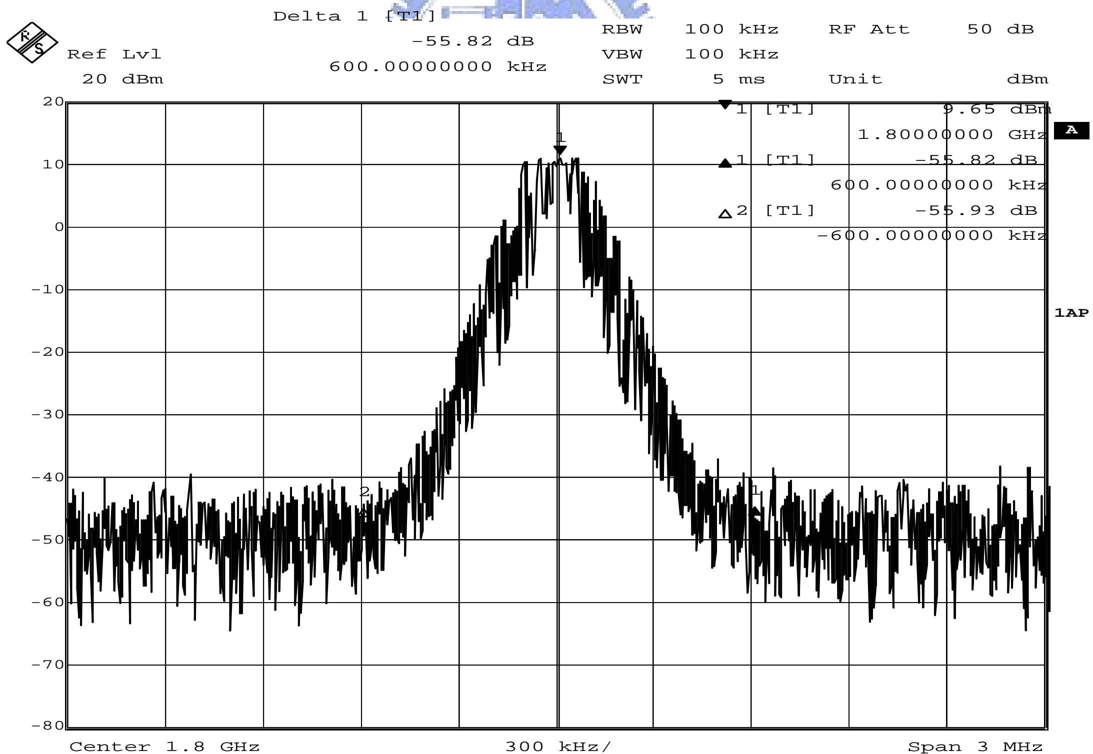


Fig. 4-16 Measured power gain versus input power at 42.8˚C



(a)





(b)

Fig. 4-17 Measured ACPR of PA at (a) 400 kHz (b) 600 kHz of PA when used GSM standard modulation as input

4.3.4 Cooling Down the Chip

After redoing the post simulation, we find the output power increase 0.5dBm and reach to 26.8dBm. We planed to cool the chip with a freezer spray until room temperature and measured the output power. Fig. 4-18 shows the testing fixture and cooling tools. Fig. 4-19 shows that we standby to cool down the chip which is operate in 0dBm input power. Fig. 4-20 shows the instantaneous photo when cooling the chip. After cooling down the chip about five seconds, the chip's temperature is about 26.2˚C as Fig. 4-21.Fig. 4-22 shows the measured output power increase 0.3~0.6dBm (temp. =42.8˚C ~ 26.2˚C.)

Fig. 4-18 Testing fixture and cooling tools

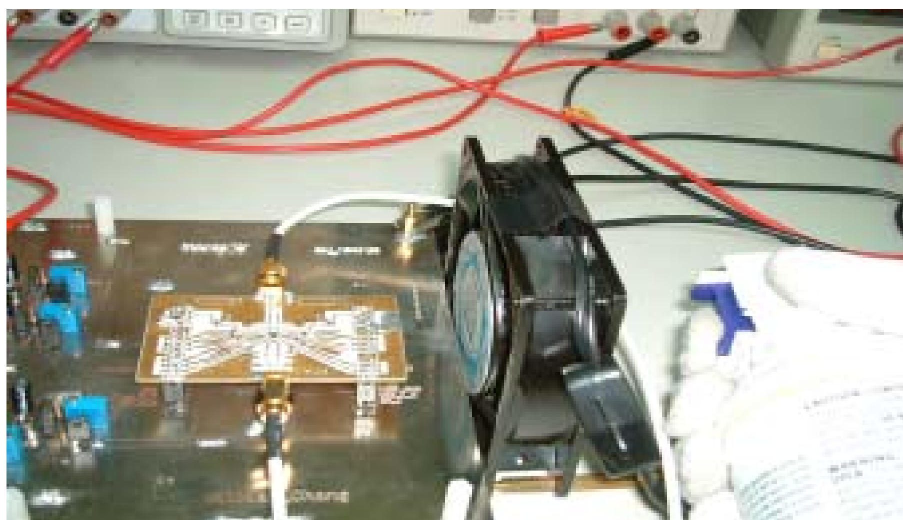


Fig. 4-19 Standby before cooling down the chip

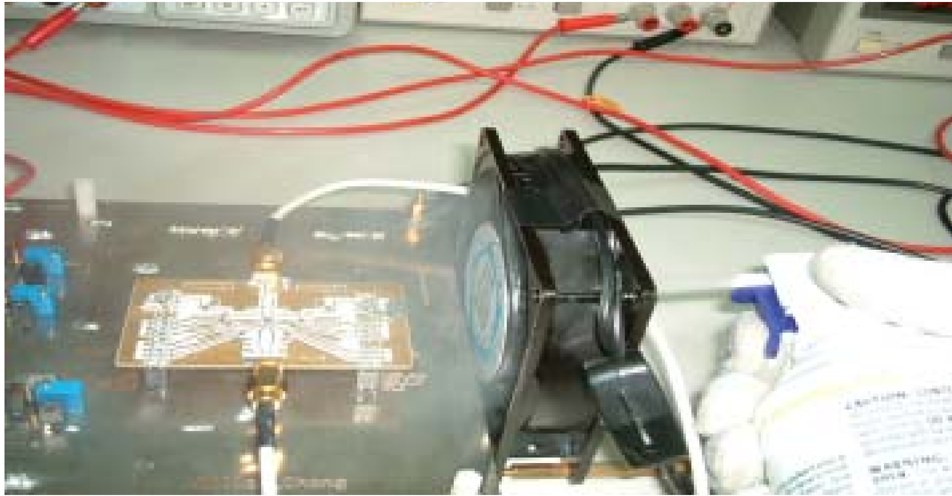


Fig. 4-20 Cooling down the chip

Fig. 4-21 Measured chip's temperature after cooling down the chip 5 seconds

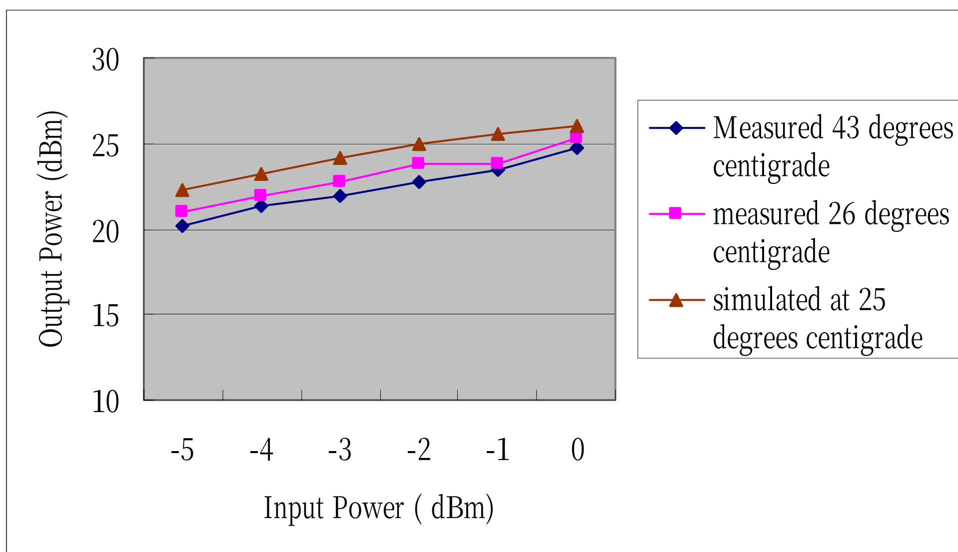


Fig. 4-22 Measured output power vs. input power at different temperature

4.3.5 Summary of Measured Results

We've cooled the chip to room temperature (26.2˚C) by freeze spray in section 4.3.4. The summary of measurement results for 42.8˚C and 26.2˚C was as Table X. We can find the output power increase about 0.5dBm and equal to 25.3dBm and PAE increase 2.3% and equal to 17.51%.

Table XII Measured summary

	Measurement	Measurement
Temperature (centigrade)	26.2	42.8
Technology	TSMC 0.25 μm 1P5M CMOS	
Supply Voltage	3.3 V/ 3.3V	3.3 V/ 3.3V
Die Size	2.11 mm × 2.2 mm	
Frequency	1.9 GHz	1.9 GHz
Output Power	25.3 dBm	24.7 dBm
Drain Efficiency	17.56%	15.26%
PAE	17.51%	15.23%
Power Gain	25.3 dB	24.7 dB
P1dB	-9 dBm	-9 dBm
ACPR at 400kHz	-43.07 dBc	-43.07 dBc
DC_Bias	Vbias1 = 1.7V Vbias2 = 1.01 V	Vbias1 = 1.7V Vbias2 = 1.01 V
Substrate Bias	V_stg1 = 0.2V V_stg2 = 0.4V	V_stg1 = 0.2V V_stg2 = 0.4V
DC Power Consumption (Stand by)	1811 mW	1811 mW
DC Power Consumption At Pin = 0dBm	1935 mW	1930 mW

4.4 DISCUSSIONS

4.4.1 Frequency Shift

Fig. 4-23 (a) shows the original circuit design of the driver stage. The layout of the original design should be as Fig. 4-23(b). The AC frequency response is as the Fig. 4-24. Because we forgot to add the decouple caps of Vdd1 in the layout. The practical layout for aping out is as Fig. 4-25(a) and the equivalent circuit was as Fig. 4-25(b). Fig. 4-26 shows the AC frequency response will drift to 1.9GHz when bondwire was up to 1.1nH.

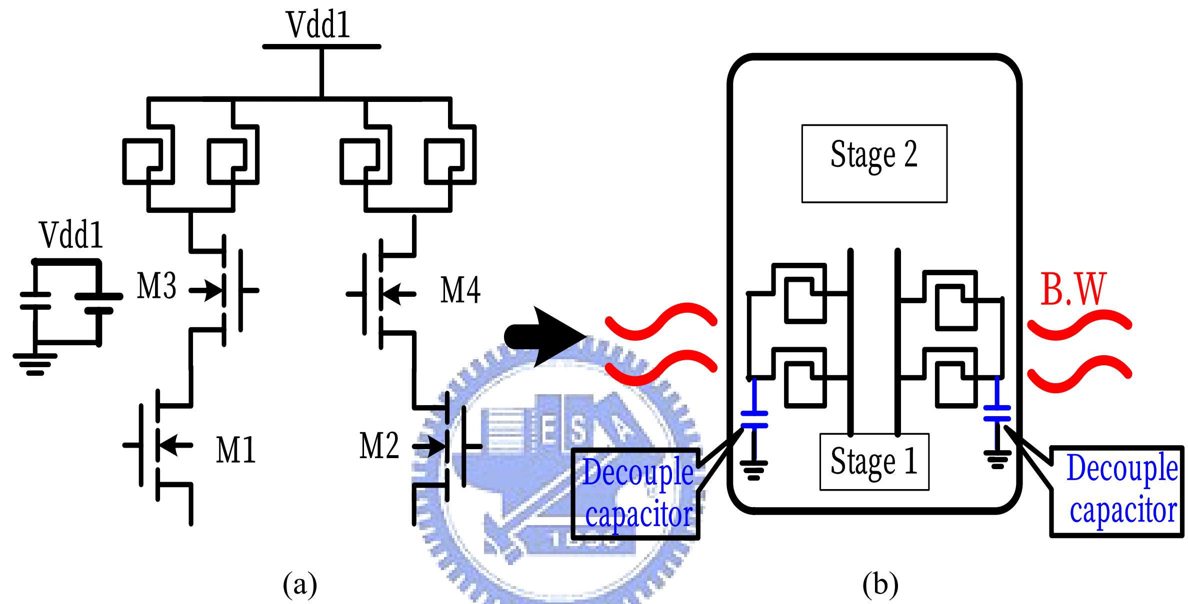


Fig. 4-23 Original circuit design of the driver stage (a) Brief schematic

(b) Equivalent layout

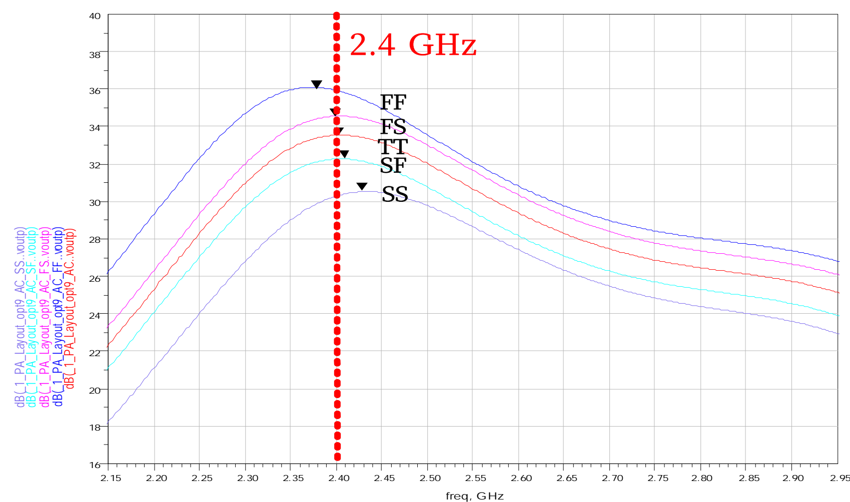
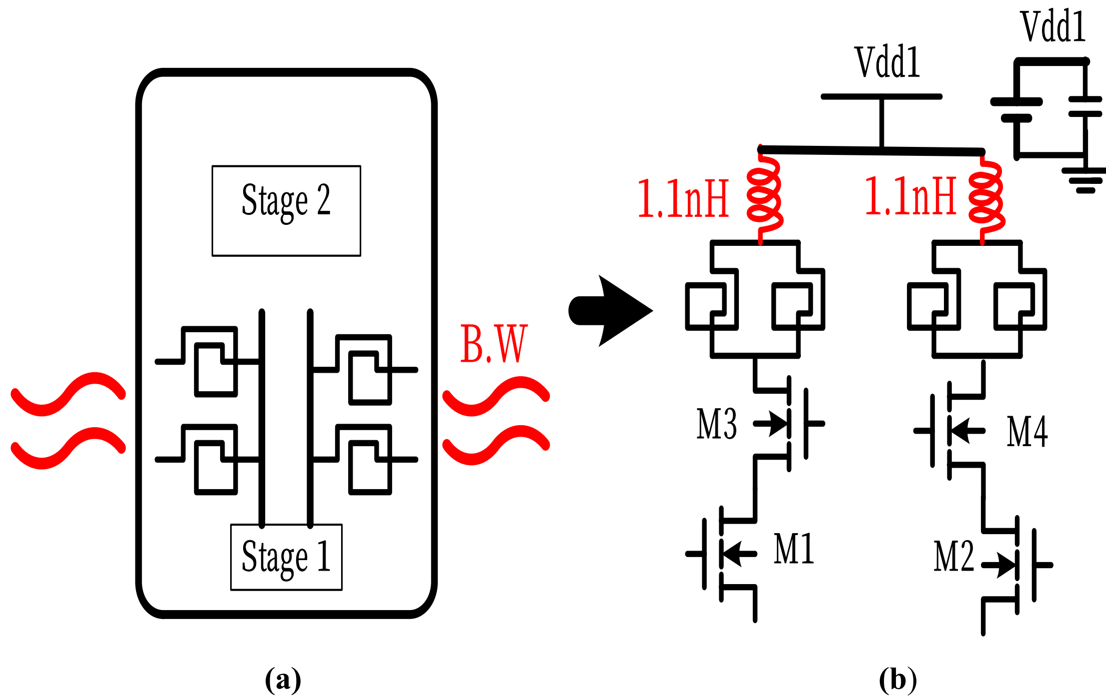


Fig. 4-24 Frequency response for four corners of the original designed chip



(a) (b)

Fig. 4-25 The taping out chip (a) Brief layout of driver state

(b) Equivalent circuit

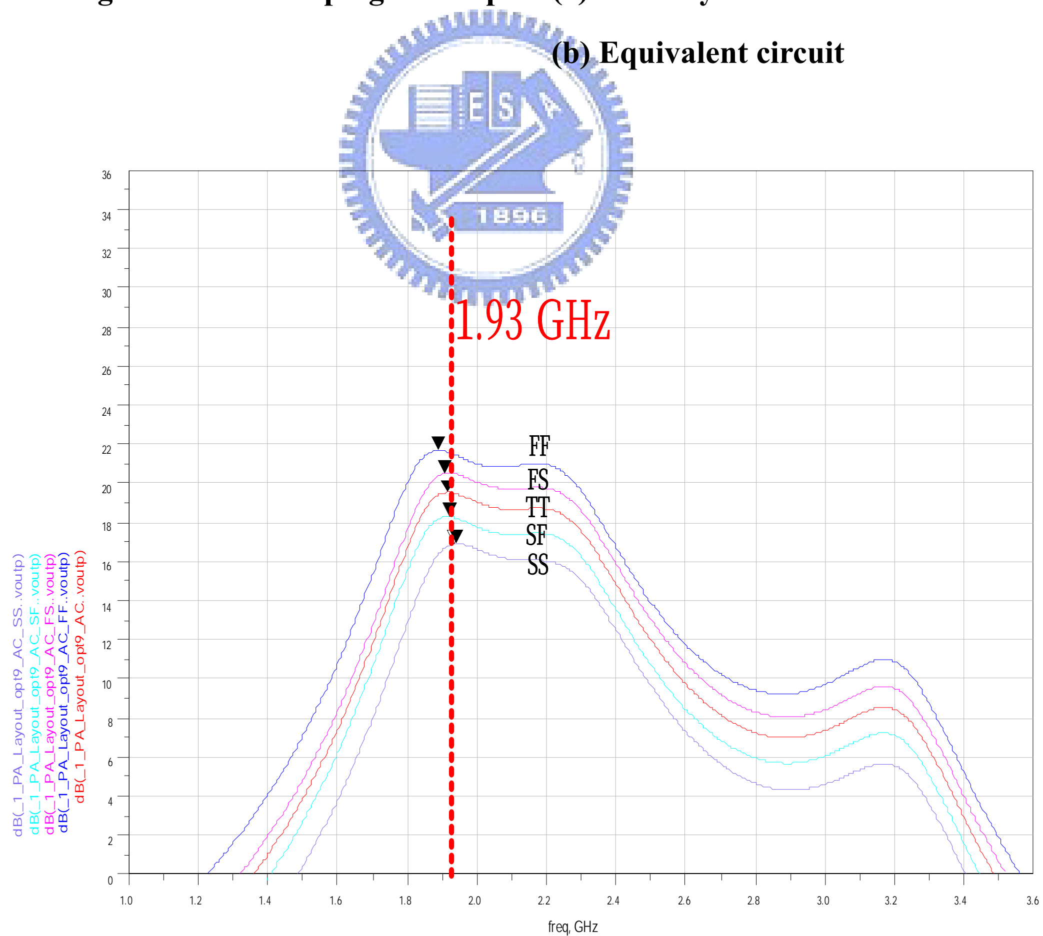
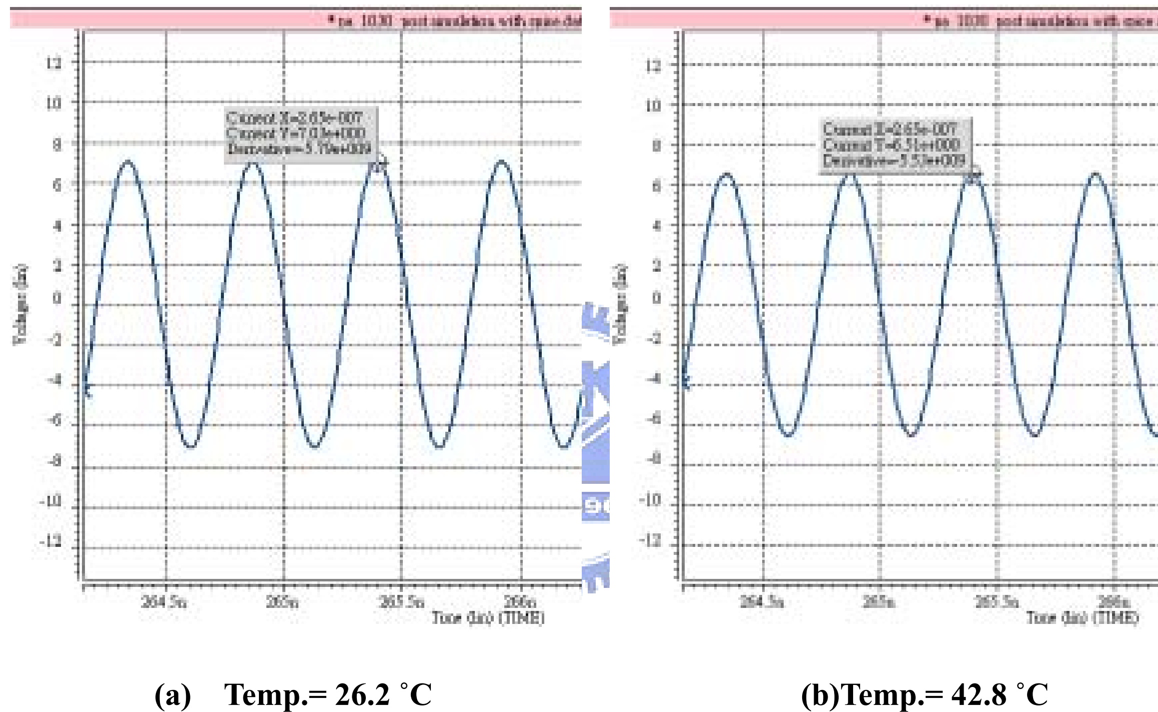


Fig. 4-26 Frequency response for four corners of the taping out chip

4.4.2 Temperature Effect

After measuring the chip's temperature when power on with fan, we get chip temperature is about 42.8˚C (chapter 4). We redo the simulation at 42.8˚C. Fig. 4-27 and Fig. 4-28 shows the output power and 1dB compression gain . Table XI shows the summary of the simulation and measurement results at at 26.2˚C and 42.8˚C.

We can find the output power increases about 0.5dBm from 42.8˚C to 26.2˚C.



(a) Temp.= 26.2 ˚C (b)Temp.= 42.8 ˚C

Fig. 4-27 The output waveform at different temperature

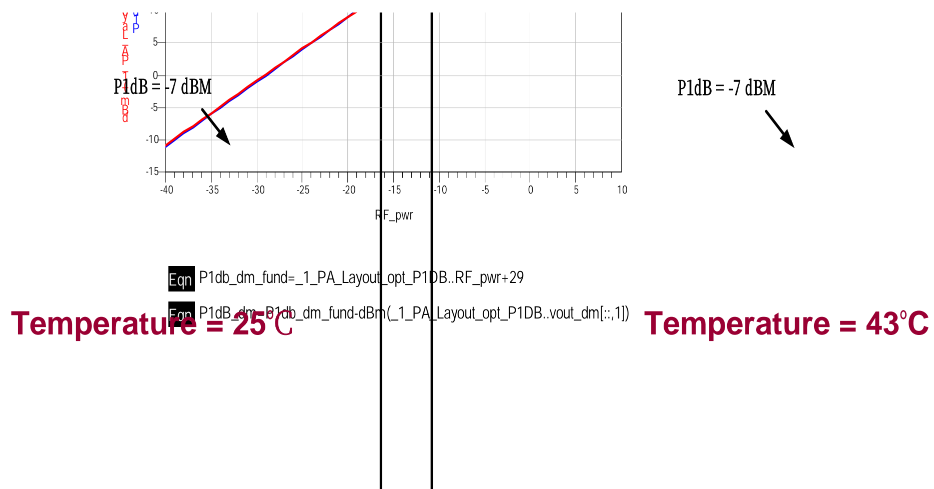


Fig. 4-28 1dB compression gain at 26.2˚C and 42.8˚C

Table XIII Summary of post-simulated and measured results at 26.2˚C and 42.8˚C.

	Post-Simulation	Measurement	Post-Simulation	Measurement
Temperature (centigrade)	26.2	26.2	42.8	42.8
Technology	TSMC 0.25 μm 1P5M CMOS			
Supply Voltage	3.3 V/ 3.3V	3.3 V/ 3.3V	3.3 V/ 3.3V	3.3 V/ 3.3V
Die Size	2.11 mm × 2.2 mm			
Frequency	1.9 GHz	1.9 GHz	1.9 GHz	1.9 GHz
Output Power	26.8 dBm	25.3 dBm	26.3 dBm	24.7 dBm
Drain Efficiency	22.80%	17.56%	20.30%	15.26%
PAE	22.76%	17.51%	20.23%	15.23%
Power Gain	26.8 dB	25.3 dB	26.3 dB	24.7 dB
P1dB	-7 dBm	-9 dBm	-7 dBm	-9 dBm
ACPR at 400kHz	-	-43.07 dBc	-	-43.07 dBc
DC_Bias	Vbias1 = 1.7V Vbias2 = 1.1 V	Vbias1 = 1.7V Vbias2 = 1.01 V	Vbias1 = 1.7V Vbias2 = 1.1 V	Vbias1 = 1.7V Vbias2 = 1.01 V
Substrate Bias	V_stg1 = 0.2V V_stg2 = 0.4V	V_stg1 = 0.2V V_stg2 = 0.4V	V_stg1 = 0.2V V_stg2 = 0.4V	V_stg1 = 0.2V V_stg2 = 0.4V
DC Power Consumption (Stand by)	1931 mW	1811 mW	1931 mW	1811 mW
DC Power Consumption At Pin = 0dBm	2110 mW	1935 mW	2100 mW	1930 mW

4.4.3 Substrate Bias versus Output Power

The MOS devices with substrate bias of output stage are used to reduce the parasitic capacitance and make sure the current could be large enough for the load-line match. The substrate bias of output stage versus the output power was as the Fig.4-29. We can find the output power increase about 1.3dBm in simulation and 1.1dBm in measurement when substrate bias is applied from 0v to 0.6v. Table XII shows the simulated parameters of MOS devices with substrate bias. Although we can get the largest current when substrate bias equal to 0.6V, it still designed to operate at 0.4V lest the P-N junction be barely on condition.

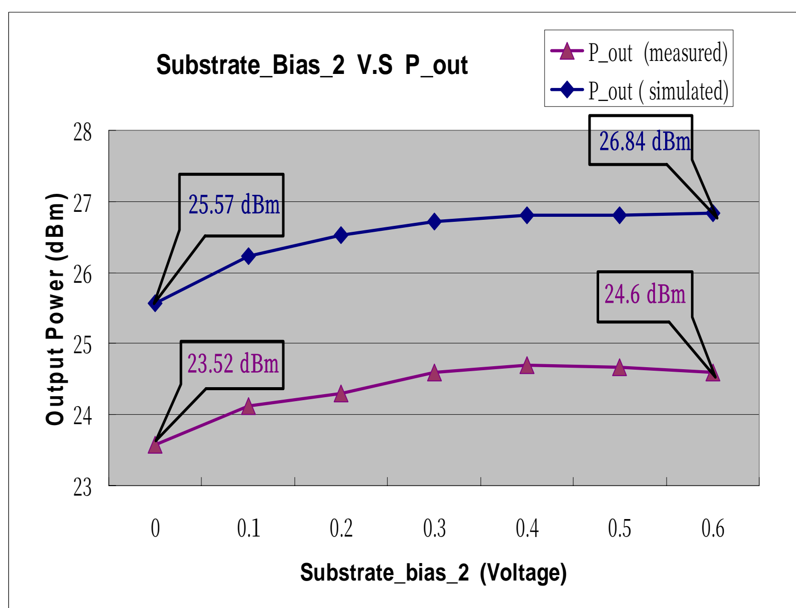


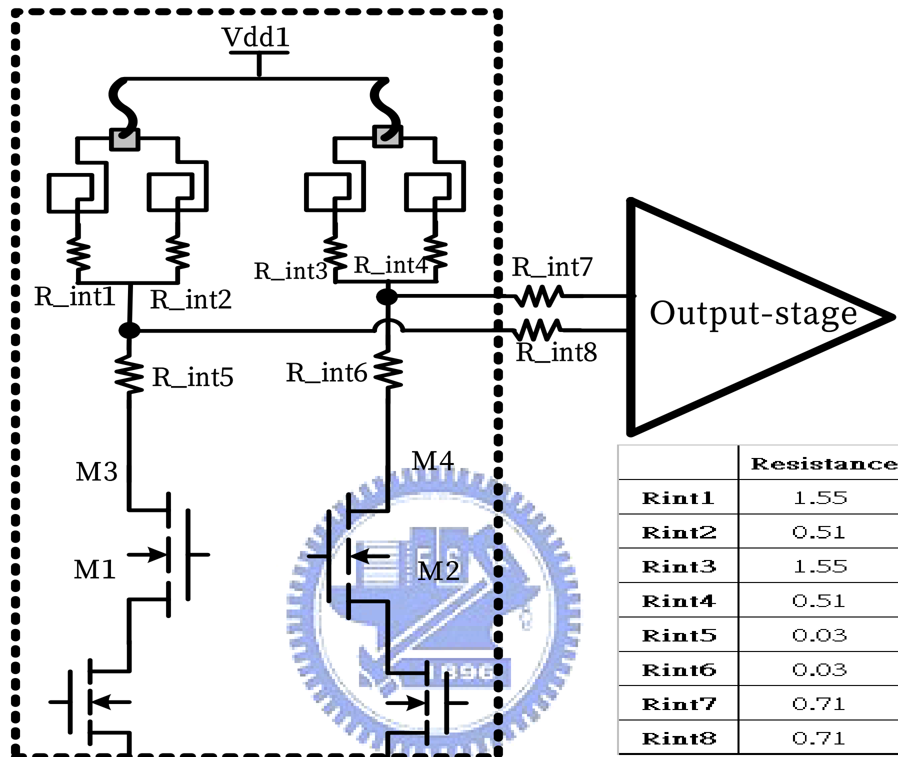
Fig. 4-29 Output power versus substrate bias

Table XIV Simulated parameters of MOS devices with substrate bias

Vdd	3.3V				
Width / Length	3500 / 0.35				
Vg	1.1				
V_substrate	0	0.2	0.4	0.5	0.6
Id (mA)	243	272	295	308	320
gm	0.645	0.667	0.679	0.684	0.688
cg_total (pf)	5.94	5.95	5.97	5.98	5.99

4.4.4 Output Power Degradation

We calculate and place the interconnection resistance (R_int1~R_int8) as Fig. 4-30 The voltage gain of the PA was as Fig. 4-31. The output-power is less about 2.4 dBm from post-simulation.



	Resistance
Rint1	1.55
Rint2	0.51
Rint3	1.55
Rint4	0.51
Rint5	0.03
Rint6	0.03
Rint7	0.71
Rint8	0.71

Fig. 4-30 Simplified driving-stage with interconnection resistance

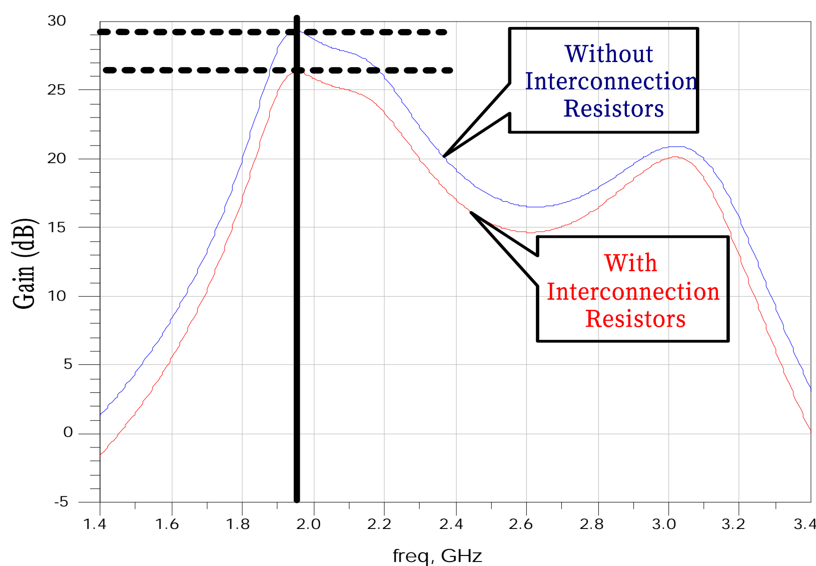


Fig. 4-31 Voltage gain of designed power amplifier

4.4.5 Comparison of Post-Simulation, Measurement and Spec

From the Table XV, simulation results show that this design chip can deliver 26.8dBm output power at 0dBm input power with 22.76% PAE at 1.9GHz at 26.2˚C . The measurement results show that the chip can provide 25.3dBm output power with 17.51% PAE at 1.9GHz. After redesign the circuit to 2.4GHz, this chip could provide 29.2dBm output power at 0dBm input power with 34.7% PAE. It could meet the FCC.15.247 spec.

Table XV Comparison of post-simulation, measurement and spec

	Post-Simulation	Post-Simulation	Measurement	FCC 15.247
Frequency	2.4 GHz	1.9 GHz	1.9 GHz	ISM Band
Temperature (centigrade)	26.2	26.2	26.2	—
Technology	TSMC 0.25 μm 1P5M CMOS			
Supply Voltage	3.3 V/ 3.3V	3.3 V/ 3.3V	3.3 V/ 3.3V	—
Die Size	2.11 mm × 2.2 mm			
Output Power @ 0 dbm Pin	29.2 dBm	26.8 dBm	25.3 dBm	30 dBm (max.)
Drain Efficiency	34.73%	22.80%	17.56%	—
PAE	34.70%	22.76%	17.51%	—
Power Gain	29.2 dB	26.8 dB	25.3 dB	—
P1dB	-7 dBm	-7 dBm	-9 dBm	—
ACPR at 400kHz	-	-	-43.07 dBc	-20 dBc
DC_Bias	Vbias1 = 1.7V Vbias2 = 1.1 V	Vbias1 = 1.7V Vbias2 = 1.1 V	Vbias1 = 1.7V Vbias2 = 1.01 V	—
Substrate Bias	V_stg1 = 0.2V V_stg2 = 0.4V	V_stg1 = 0.2V V_stg2 = 0.4V	V_stg1 = 0.2V V_stg2 = 0.4V	—
DC Power Consumption (Stand by)	1931 mW	1931 mW	1811 mW	—
DC Power Consumption At Pin = 0dBm	2352 mW	2110 mW	1935 mW	—

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 CONCLUSIONS

A new 2.4GHz high-output-power RF CMOS power amplifier using MOS devices with positive substrate bias was designed and fabricated. Two-stage methodology was chosen in this design. To consider the linearity and efficiency, the input stage operates in class-A and output stage operates in class-AB. The differential with Cascode topology was used to increase output power and alleviate breakdown problem. MOS devices with positive substrate bias are used to reduce MOS size and ensure that the driver stage can deliver large enough signal to output stage. The stability enhanced circuits are used to ensure that the circuit operates in unconditional stable. The simulation results showed this chip can provide 29.2dBm output power with 34.7% PAE at input power equal 0dBm (2.4GHz) at 26.2 ˚C

We redesign the external components values of matching networks to 1.9GHz due to the frequency shift. After adding the interconnection resistance and redoing the post -simulation, this chip can provide 26.8dBm output power with 22.76% PAE at input power equal 0dBm (1.9GHz) at 26.2 ˚C. The 1dB compression gain is -7dBm. The positive substrate bias is 0.4V in output stage and 0.2v in driver stage. The total dc power consumption is 640 mA from 3.3V supply voltage.

This chip was fabricated in a standard TSMC 0.25μm 1P5M CMOS process without any additional process tweaking. The chip area is 2.11mmX2.2mm. The experimental results show the temperature of this chip was about 42.8˚C when power on with fan. Hence We redo the post simulation at 42.8˚C. The simulation results showed the chip can provide 26.3 dBm with 20.23% PAE, and 1dB compression gain is still -7 dBm at input

power equal 0dBm(1.9GHz) at 42.8˚C. The total dc power consumption is 640mA form 3.3V supply voltage.

The measurement results showed the power amplifier can provide 24.7 dBm output power with 15.23% PAE at input power equal 0dBm when chip's temperature is about 42.8˚C. ACPR is -43.07dBc at 400kHz frequency bandwidth when GSM standard modulation was chosen The positive substrate bias is 0.4v in the output stage and 0.2v in the driver stage. The total dc power consumption is 585mA form 3.3V supply voltage.

After cooling down the chip till 26.2˚C, measurement results showed this chip can provide 25.3 dBm output power with 17.51% PAE at input power equal 0dBm. The 1dB compression gain is -9 dBm and the ACPR is -43.1dBc at 400kHz frequency bandwidth when GSM standard modulation was chosen. The positive substrate bias is 0.4v in the output stage and 0.2v in the driver stage. The total dc power consumption is 586mA form 3.3V supply voltage.

The design of high-output-power RF power amplifier using MOS devices with positive substrate bias is presented. The post-simulation and measurement results can meet the FCC 15.247 spec. Compare to the publications of class-AB RF high-output-power CMOS PA [10]-[11], this chip size is relatively small. In other words, we can design the PA using smaller MOS devices size with substrate bias to achieve high-output-power.

5.2 FUTURE WORKS

The designed power amplifier is focus on high-output-power and stability. Form experimental results we can find the PA operates in unconditional stable. The operated frequency was drift to 1.9GHz due to bonding wire effect of driving stage. It's important to add a large enough decouple capacitor in the Vdd1 bonding pads of the driver stage in the future. The interconnection resistance results in lower output power. So we have to redesign the PA and fabricate the chip with correct functions.

Besides, the input and output matching networks of this design are implemented on PCB board. To integrate matching networks and stability enhanced circuits into chip is needed in the future . The power added efficiency (PAE) of this power amplifier is 34.7% form post–simulation results at 2.4GHz. Although we figured out the reason of efficiency degradation is high temperature and interconnection resistance, finding a structure that can improve the efficiency is needed for this power amplifier. Furthermore, to design a linearization structure for the designed RF CMOS PA without decreasing output power is another issue.

References

[1] P. Miliozzi, K. Kundert, K. Lampaert, P. Good, and M. Chian, “A design system for RFIC: Challenges and solutions,”Proceedings of the IEEE, vol. 88, pp.1613-1632, Oct. 2000.

[2] L.E.Larson, “Integrated circuit technology options for RFIC present status and future directions,” IEEE J.Solid-State Circuits, vol. 33, pp.387-399, March 1998

[3] J.C. Rudell, J.J.ou, R.S. Narayanaswami, et al. “Recent developments in high integration multi-standard CMOS transceivers for personal communication systems,” Invited paper at the 1998 International Symposium on Low Power Electronics, 1998.

[4] A.Rofougraran, G. Chang, J.Rael, et al.”A single-chip 900MHz spread spectrum wireless transceiver in 1mm CMOS-part I:architecture and transmitter design,”IEEE J. Solid-State Circuits, vol. 33, pp. 513-534, April 1998.

[5] J.Rudell, et al.”A 1.9GHz wide band IF double conversion CMOS receiver for cordless telephone applications”, IEEE J. Solid-State Circuits, vol. 32, pp. 2071-2088, Dec. 1997

[6] M. Steyaert, M. Borremans, J. Janssens, et al. “A 900MHz/1.8GHz CMOS receiver for dual-band applications” in In Int. Solid-State Circuits Conf. Dig. Tech. Papers, (San Francisco), pp. 48-49, Feb. 1998.

[7] D. Su and W. McFarland, “A 2.5V, 1Watt monolithic CMOS RF power amplifier,” in Proc. Custom Integrated Circuits Conf.,pp. 179-182, May 1997

[8] Seoung-Jae Yoo, Hong Jo Ahn, Mona M Hella, and Mohammed Ismail, “The design of 433 MHz Class- AB CMOS Power Amplifier” 2000 IEEE International

Solid-State Circuits Conference.

[9] Brain Hallweber, Ravi Gupta, David J. Allstot, “Fully-Integrated CMOS RF Amplifiers” 1999 IEEE International Solid-State Circuits Conference.

[10] C Fallesen and P.Asbeck, “A 1W 0.35 μm CMOS power amplifier for GSM-1800 with 45% PAE” in 2001 IEEE International Solid-State Circuits Conference, (San Francisco, USA), February 2001

[11] C Fallesen and P.Asbeck, “A 1W CMOS power amplifier for GSM-1800 with 55% PAE” in 2001 IEEE MTT-S Digest, (San Francisco, USA), February 2001

[12] S.C.Cripps, “RF Power Amplifiers for Wireless Communication”. Artech House, first ed., 1999.

[13] G.Gonzalez, “Microwave Transistor Amplifiers: Analysis and Design.” Prentice-Hall,second ed., 1996

[14] C. C. Meng, H. Y. NI, “Determining stability circle using two geometrically derived parameters” IEEE transactions on microwave theory and techniques, 2000

[15] Marion Lee Edwards and Jeffrey H.Sinsky, “New Criterion for Linear 2-port Stability Using a Single Geometrically Derived Parameter”, IEEE transactions on microwave theory and techniques, Vol. 40 No. 12, December 1992.