國立交通大學

電機資訊學院 電子與光電學程

碩 士 論 文

應用於超寬頻系統之低雜訊放大器與混波器設計

Design of Low Noise Amplifier and Mixer for Ultra-Wideband Application

研 究 生：林志修

指導教授：郭建男 教授

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A Thesis

Submitted to Degree Program of Electrical Engineering and Computer Science

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Master of Science

In

Electronics and Electro-Optical Engineering

May 2005

Hsinchu, Taiwan, Republic of China

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摘要

本篇論文主要是利用標準 0.18μm CMOS 製程設計應用於超寬頻系統前端接收器之低雜訊放大器和混波器積體電路。在第一顆晶片裡，適用於接收端超寬頻系統之寬頻放大器被設計與分析。我們利用負回授電阻達到寬頻之輸入輸出組抗匹配以及自偏壓。實際量測結果顯示此一放大器在 0.1GHz 到 6.6GHz 頻率下有著最高功率增益(S21) 6.2dB，輸入返回損耗(S11)及輸出返回損耗(S22)小於-10 dB，以及平均雜訊指數 8.1dB，此電路消耗之功率為 16.2mW。

第二顆晶片中，我們利用柴比席夫濾波器來達到寬頻匹配，設計超寬頻系統接收器第二級之混波器，並在轉導級和混波級中間加入電感來使高頻的增益增加。實際量測結果顯示此寬頻混波器在 3~8GHz 有最高的轉換增益(Conversion Gain) 7.4dB，輸入返回損耗(S11)小於-4dB，平均 IIP3 為+3.4dBm，最小雜訊指數 7.1dB。此電路消耗功率為 11.8mW。

Design of Low Noise Amplifier and Mixer for Ultra-Wideband Application

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ABSTRACT

This thesis aim is to design an ultra wideband low noise amplifier and mixer in the UWB receiver system using standard 0.18um CMOS process. In first chip, an ultra wideband low noise amplifier is analyzed and designed in UWB system. We employ the negative feedback resistor to achieve input, output broadband matching. In the measured data, we show the maximum power gain is 6.2dB and input matching (S11) and output matching (S22) are less than -10dB from 0.1GHz to 6.6GHz. The average noise figure is 8.1dB. The total power consumption is 16.2mW.

In second chip, we design a mixer which is the second stage of the UWB system. In this design, we use the chebyshev filter to achieve 3~8GHz broadband matching. And an inductor adds to between transconductance stage and switching stage which improve the high frequency gain. The measured result shows the highest conversion gain is 7.4dB at 3~8GHz band. Input return loss is less than -4dB. The average iip3 is +3.4dBm. The minimum noise figure is 7.1dB. The total power consumption is 11.8mW.

誌謝

首先，我要感謝我的指導教授郭建男博士在這二年多來耐心的給與指導和鼓勵，使我學到許多射頻積體電路方面的知識及設計電路需克服的困難，填補了以前在工作上似懂非懂的感覺，並感謝一起建立實驗室並共患難的同學們，傅昶綜是個熱心助人的學長、卓宏達是個電磁學高手、劉上逸、傅敬銘、洪英瑞-常幫我解決工作站及量測的問題、及個性認真的小馬和喜歡鬥嘴的王柏之與陳仰鵑，有了大家的努力才有這麼乾淨的讀書環境。還要感謝低功率計畫的指導教授郭治群教授和成員蔡坤宏-大家都叫他 Dr. 岡田，及詹維嘉-書卷獎的常客，從你們身上獲得其他專業領域的知識。並在課業閒餘，大家一起烤肉，出外踏青，減輕課業上的壓力。有了以上大家的幫助才能讓我很快的進入狀況並完成論文。

還有大學的專題夥伴兼室友維修，在同一家公司上班，並一起離職到交大唸書的一段孽緣。並特別感謝球友兼同窗小肥趙在多次寒冷的冬天請吃火鍋的辛勞及小柯與射手小賊昌的友情贊助。

最後，還要感謝我父母及弟弟志倫在精神上的支持，及遠在澳洲求學和我常 MSN 的表弟挺毓，讓我能夠安心的在交大完成碩士學位。

林志修

九十四年 五 月

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS


E
S
A
1896

Chapter 1

Introduction

1.1 Motivation

Ultra-wideband (UWB) technology has been around since the 1980s[1], but it has been mainly used for radar-based applications until now, because of the wideband nature of the signal that results in very accurate timing information. However, due to recent developments in high speed switching technology, UWB is becoming more attractive for low cost consumer communications applications. UWB system allows to overlay existing narrowband systems, and result in a much more efficient use of the available spectrum. Therefore, the Federal Communications Commission (FCC) has allocated 7500MHz of spectrum for unlicensed use of ultra-wideband devices (UWB) in the 3.1 to 10.6GHz frequency band. UWB is emerging as a solution for the IEEE 802.15.3a (TG3a) standard. This standard is to provide a specification for a low complexity, low cost, low power consumption, and high data rate wireless connectivity among devices within or entering the personal operating space. The data rate must be high enough (greater than 110Mb/s) to satisfy a set of consumer multimedia industry needs for wireless personal area networks (WPAN) communications. The standard also addresses the quality of service (QoS) capabilities required to support multimedia data types.

In order to achieve low power dissipation, low cost and easy to integrate with other device, CMOS (metal oxide semiconductors) offers a good solution for these purposes, although bipolar transistors usually simplify analog circuit design. It offers both active and passive devices. Active devices present cut-off frequencies up to 40GHz and are suitable for RF applications in the wireless communications. However,

the passive devices such as inductors are not working well in RF band because the quality factor is degraded by losses in both the metal and the substrate.

In this thesis, we use standard TSMC 0.18μm CMOS process to design an ultra-wideband low noise amplifier and a 3~8 GHz direct convention broadband mixer. Low noise amplifier (LNA) and mixer are the first and second stage in all wireless receiver system. LNA is the first stage in the wireless system that noise requirement is very serious. However the mixer needs high linearity characteristic in the wireless system.

1.2 Introduction to Ultra Wideband System

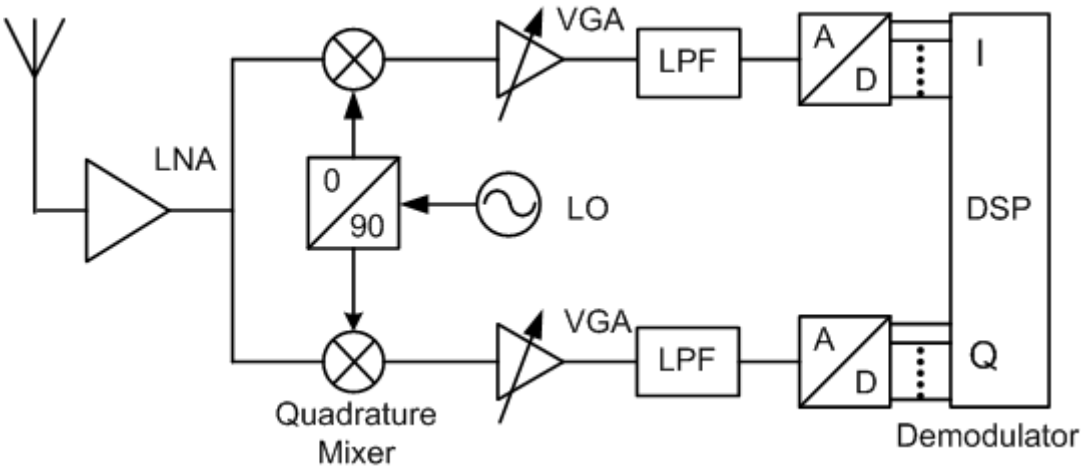


Fig. 1.1 Ultra wideband system block diagram

Fig. 1.1 is an ultra wideband receiver front end system block diagram. FCC issued in February 2002, allocated 7500MHz of spectrum for unlicensed use of ultra-wideband devices (UWB) in the 3.1 to 10.6 GHz frequency band. It has two possible solutions for the future standard IEEE 802.15.3a (TG3a). The first one is that UWB systems can be designed to use the 7500MHz available UWB spectrum. It means that the signal can be shaped so that its envelope occupies the full spectrum. The other one is that it can be shaped so that it occupies only 500MHz bandwidth,

allowing 15 such signals to cover the entire band. There are, of course, intermediate cases, e.g., five signals of 2.5GHz bandwidth each. We will explain briefly these two methods below.

Impulse Radio:

This is single band solution. Information can be encoded in an UWB signal in a variety of methods. The most popular modulation schemes developed to date for UWB are pulse-position modulation (PPM), pulse-amplitude modulation (PAM), and binary phase-shift keying (BPSK). In PPM encoding method which is based on the principle of encoding information with two or more positions in time, referred to the nominal pulse position. A pulse transmitted at the nominal position represents a 0, and a pulse transmitted after the nominal position represents a 1. In PAM encoding method which is based on the principle of encoding information with the amplitude of the impulses. In bi-phase modulation, information is encoded with the polarity of the impulses. The polarity of the impulses is switched to encode a 0 or a 1.

Multi-Band:

The multi band system is based on the principle of transmitting different symbols in different bands in a periodic sequence, very similarly to frequency hopping. Each band occupies 500MHz bandwidth, and the hopping rate varies between 16 and 32MHz. The sequences can be used to reduce collisions with other users by using different sequences for different networks. The link margin with respect to 30 and 12ft. The Fig. 1.2 illustrates the division of the UWB spectrum into sub-bands.

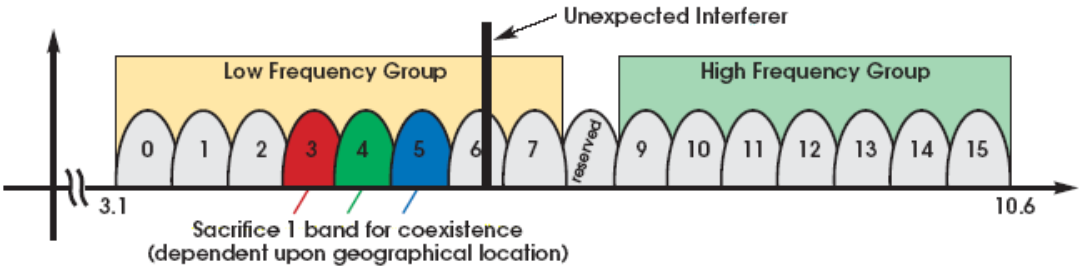


Fig. 1.2 Multi-band spectrum allocation

1.3 Thesis Organization

This thesis discuss about the receiver front-end circuits (low noise amplifier and mixer) design and implementation for the UWB frequency bands. The contents consist of two major topics: “A 0.18μm CMOS ultra-wideband low noise amplifier circuit” and “A 0.18μm CMOS 3~8GHz direct conversion broadband mixer circuit”.

In Chapter 2, we will introduce the fundamentals of conventional low noise amplifiers and mixer. And some theoretical MOSFET noise model and noise theory are presented. LNA noise analysis also introduce in this chapter. Furthermore, many important design parameters and direct conversion receiver front end would be presented in this chapter.

In Chapter 3, we start to design an ultra-wideband low noise amplifier. The matching method of ultra-wideband amplifiers design is negative resistor feedback plus the inductive degeneration method to enhance bandwidth. And the feedback resistors are the main components to achieve the ultra-wideband matching.

In Chapter 4, we design a 3~8 GHz direct convention broadband mixer based on gilbert cell structure. In this work, we will use chebyshev bandpass filter method to satisfy input return loss less than -10dB in our interest band.

In Chapter 5, conclusions and future work. Some issues that should be noted for future works on this topic are also summarize.

Chapter 2

The Fundamentals of Low Noise Amplifier and Mixer

In this chapter, we will introduce the principles of the low noise amplifier and mixer. Furthermore, this chapter also shows what kinds of parameters and consideration are important in LNA and mixer design. In section 2.1 illustrates the noise sources type and MOSFET noise model [2,3,4]. In section 2.2 shows principle of low noise amplifier and its noise analysis [3,4]. In section 2.3 shows the principle of mixer and some of its important characteristic [5,6]. In section 2.4, we will introduce the advantage and disadvantage of the direct conversion receivers [6].

2.1 Noise Analysis

The LNA is the first stage of the receiver front end. The noise performance is first consideration in design low noise amplifiers. Therefore, the study of noise is very important because it represents a lower limit to the size of electrical signal that can be amplified by a circuit without significant deterioration in signal quality. In this section, the various sources of electronic noise are considered separately. And MOSFET's noise model will be described here.

2.1.1 Source of Noise Type

In the integrated circuit, there are many kinds of noise sources, such as shot noise, thermal noise and flicker noise (1/f noise).

Shot noise is always associated with a direct current flow and is present in diodes, MOS and bipolar transistors. The origin of shot noise can be seen by considering the diode and the carrier concentrations in the device in the forward-bias region. The

passage of each carrier across the junction, which can be modeled as a random event, is dependent on the carrier having sufficient energy and a velocity directed toward the junction. The shot noise current can be represented as $\overline{i^2} = 2qI_D\Delta f$, q is the electronic charge ($1.6\times10^{-19}C$), Δf is the bandwidth in hertz.

Thermal noise is generated from the conventional resistors. It is due to the random thermal motion of the electrons and is unaffected by the presence or absence of direct current, since typical electron drift velocities in a conductor are much less than electron thermal velocities. Since this source of noise is due to the thermal motion of electrons, we expect that it is related to absolute temperature T. The thermal noise can be represented by a series voltage generator $\overline{v^2}$ or shunt current generator $\overline{i^2}$. These representations are $\overline{v^2} = 4kTR\Delta f$, $\overline{i^2} = 4kT(1/R)\Delta f$ where k is Boltzmann's constant. At room temperature: $4kT = 1.66\times10^{-20}V - C$.

Flicker noise is a type of noise found in all active devices, as well as in some discrete passive elements such as carbon resistor. The origins of flicker noise are varied, but it is caused mainly by traps associated with contamination and crystal defects. These traps capture and release carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies. Flicker noise, which is always associated with a flow of direct current, displays a spectral density of the form $\overline{i^2} = K_1(I^a / f^b)\Delta f$, where Δf is small bandwidth at frequency f , I is direct current, K1 is constant for a particular device, a is constant in the range 0.5 to 2, b is constant of about unity. It is apparent that flicker noise is most significant at low frequencies, although in devices exhibiting high flicker noise levels, this noise source may dominate the device noise at frequencies well into the megahertz range.

2.1.2 Noise Model of MOSFET

MOSFET's noise source mainly comes from gate current noise, drain current noise (channel thermal noise) and flicker noise.

Drain current noise $\overline{i_d^2}$ (channel thermal noise) is the dominant noise source of MOS devices. Since MOSFETs are essentially voltage-controlled resistors, they exhibit thermal noise. In the triode region of operation particularly, one would expect noise commensurate with the resistance value. Indeed, detailed theoretical considerations lead to the following expression for the drain current noise of FETs.

$$\overline{i_d^2}=4kT\gamma g_{d0}\Delta f \qquad (2\text{-}1)$$

where g_{d0} is the drain-source conductance at zero V_{DS}. The parameter g has a value of unity at zero V_{DS} and, in long devices, decreases toward a value of 2/3 in saturation. Note that the drain current noise at zero V_{DS} is precisely that of an ordinary conductance of value g_{d0}.

Another kind of thermal noise is gate current noise $\overline{i_g^2}$. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current. Although this noise is negligible at low frequencies, it can dominate at radio frequencies. The gate current noise may be expressed as

$$\overline{i_g^2}=4kT\delta g_g\Delta f \qquad (2\text{-}2)$$

$$g_g=\frac{\omega^2 C_{gs}^2}{5g_{d0}}$$

where δ is the coefficient of gate noise, classically equal to 4/3 for long-channel devices. Equation (2-2) is valid when the device is operated in saturation.

The gate noise is partially correlated with the drain noise, with a correlation coefficient given by

$$c \equiv \frac{\overline{i_g \times i_d^*}}{\sqrt{\overline{i_g^2} \times \overline{i_d^2}}} \approx 0.395j \tag{2-3}$$

where the value of 0.395j is exact for long-channel devices. The correlation can be treated by expressing the gate noise as the sum of two components, the first of which is fully correlated with the drain noise, and the second of which is uncorrelated with the drain noise. Hence, the gate noise is re-expressed as

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g(1-|c|^2) + 4kT\delta g_g|c|^2 \tag{2-4}$$

Because of the correlation, special attention must be paid to the reference polarity of the correlated component. The value of c is positive for the polarity.

In electronic devices, 1/f noise (flicker noise) arises from a number of different mechanisms, and is most prominent in devices that are sensitive to surface phenomena. Charge trapping phenomena are usually invoked to explain 1/f noise in transistors. Some types of defects and certain impurities can randomly trap and release charge. The trapping times are distributed in a way that can lead to a 1/f noise spectrum in both MOS and bipolar transistors. Larger MOSFETs exhibit less 1/f noise because their larger gate capacitance smooths the fluctuation in the channel charge. Here, if good 1/f noise performance is to be obtained from MOSFETs, the largest practical device sizes must be used (for a given gm). The mean-square 1/f drain noise current is given by

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \approx \frac{K}{f} \omega_T^2 \cdot A \cdot \Delta f \tag{2-5}$$

where A (=WL) is the area of the gate and K is a device-specific constant. Thus, for a fixed transconductance, a larger gate area and a thinner dielectric reduce this noise term.

2.2 Principle of Low Noise Amplifiers

In the design of low noise amplifiers, there are several common goals. These include minimizing the noise figure of the amplifier, providing gain with sufficient linearity – typically measured in terms of the third order intercept point, IP3 and providing a stable 50Ω input impedance to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier. A good input matching is even more critical when a preselect filter precedes the LNA because such filters are often sensitive to the quality of their terminating impedances. The additional constraint of low power consumption which is imposed in portable systems further complicates the design process.

2.2.1 Basic Topologies of Low Noise Amplifier

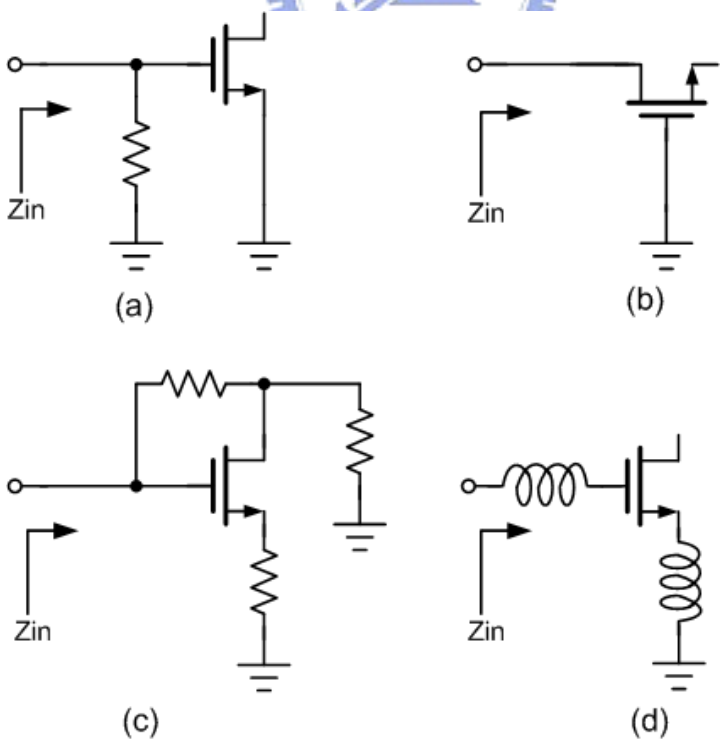


Fig 2.1 Common LNA architectures (a) Resistive termination (b) 1/g_m termination (c) Shunt - series feedback (d) Inductive degeneration [3]

Here, there are four basic topologies of low noise amplifiers as shown in Fig. 2.1. These techniques provide good stable input impedance matching. The first technique of low noise amplifiers is shown in Fig. 2.1(a). It uses resistive termination of the input port to provide 50Ω impedance. Unfortunately, the use of real resistors in this fashion has a deleterious effect on the amplifier's noise figure.

The second architecture, shown in Fig. 2.1(b), uses the source or emitter of a common gate or common base stage as the input termination. It's also called $1/g_m$ termination architecture. Assuming matched conditions, yields the following lower bounds on noise factor for the cases of bipolar and CMOS amplifiers:

$$\text{Bipolar:} \quad F=\frac{3}{2}=1.76\text{dB}$$

$$\text{CMOS:} \quad F=1+\frac{\gamma}{\alpha}\geq\frac{5}{3}=2.2\text{dB} \quad \text{where} \quad \alpha=\frac{g_m}{g_{d0}}$$

The bipolar representation neglects the effect of base resistance in bipolar devices. In CMOS expressions, γ is the coefficient of channel thermal noise, g_m is the device transconductance, and g_{d0} is the zero bias drain conductance. For long channel devices, $\gamma=2/3$, $\alpha=1$. But in short channel MOS devices, γ can be greater than one, and α can be much less than one. Accordingly, the minimum theoretically achievable noise figures tend to be around 3dB or greater in practice.

The third topology is shown in Fig. 2.1(c). This architecture uses resistive shunt and series feedback to set the input and output impedances of the LNA. Amplifiers using shunt-series feedback often have extraordinarily high power dissipation compared to others with similar noise performance. Intuitively, the higher power is partially due to the fact that shunt series amplifiers of this type are naturally broadband, and hence techniques which reduce the power consumption through LC tuning are not applicable. For GPS applications, a broadband front end is not required,

and it is desirable to make use of narrowband techniques to reduce power.

The fourth topology is shown in Fig. 2.1(d). It is desirable to have a narrowband RF signal processing, to get rid of out of band blockers. It employs inductive source or emitter degeneration to generate a real term in the input impedance. It offers the possibility of achieving the best noise performance of any architecture.

2.2.2 L-degeneration LNA Noise Analysis

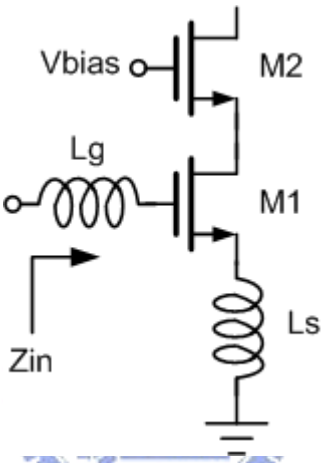


Fig. 2.2 Cascode LNA architecture

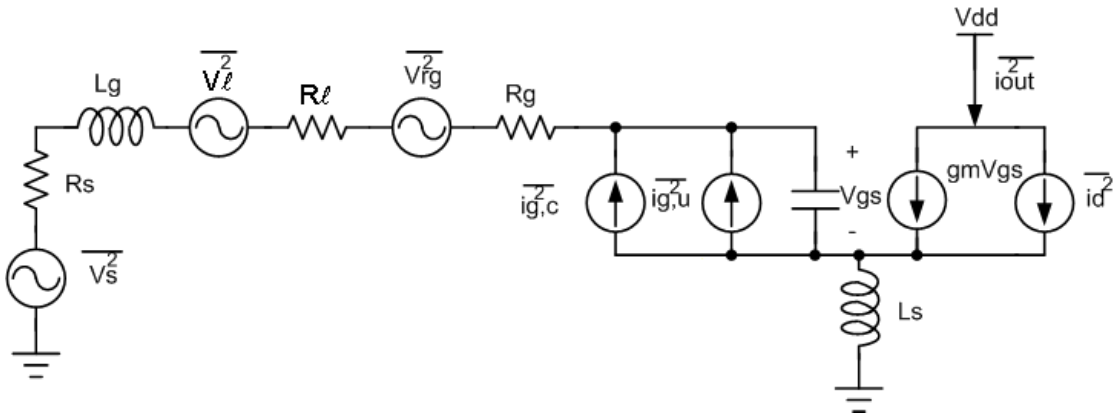


Fig. 2.3 Small-signal model for LNA noise calculations [3]

Fig. 2.2 shows the basic cascode LNA architecture. A simple analysis of the input impedance shows that

$$Z_{in}=s(L_s+L_g)+\frac{1}{sC_{gs}}+(\frac{g_{m1}}{C_{gs}})L_s=\omega_T L_s \quad \text{(at resonance)} \tag{2-6}$$

The noise figure of the cascade LNA can be computed by analyzing the circuit shown in Fig. 2.3. In this circuit, $R\ell$ represents the series resistance of the inductor Lg, Rg is the gate resistance of the NMOS device, $\overline{i_d^2}$ represents the channel thermal noise of the device. $\overline{i_{g,c}^2}$ represents the portion of the total gate noise that is correlated with the drain noise. $\overline{i_{g,u}^2}$ represents the portion that is uncorrelated with the drain noise. Analysis based on this circuit neglects the contribution of subsequent stages to the amplifier noise figure. Recall that the noise factor for an amplifier is defined as

$$F=\frac{\text{Total\_output\_noise}}{\text{Total\_output\_noise\_due\_to\_the\_source}} \tag{2-7}$$

To evaluate the output noise when the amplifier is driven by a 50Ω source, we first evaluate the transconductance of the input stage. With the output current proportional to the voltage on Cgs, and noting that the input circuit takes the form of a series-resonant network

$$G_m=g_m Q_{in}=\frac{g_m}{\omega_o C_{gs}(R_s+\omega_T L_s)}=\frac{\omega_T}{2\omega_o R_s} \tag{2-8}$$

Qin is the effective Q of the amplifier input circuit. From the equation (2-8), the output noise power density due to the 50Ω source is

$$S_{a,src}(\omega_o)=S_{src}(\omega_o)\cdot G^2_{m,eff}=\frac{4kT\omega_T^2}{\omega_o^2 R_s(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-9}$$

In a similar way, the output noise power density due to $R\ell$ and Rg can be expressed as

$$S_{a,R\ell,Rg}(\omega_o)=\frac{4kT(R\ell+R_g)\omega_T^2}{\omega_o^2 R_s^2(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-10}$$

Next, the noise power density associated with the correlated portion of the gate noise and drain noise can be expressed as

$$S_{a,id,ig,c}(\omega_o)=\kappa S_{a,id}(\omega_o)=\frac{4kT\gamma\kappa g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-11}$$

where

$$\kappa=\frac{\delta\alpha^2}{5\gamma}|c|^2+\left[1+|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 \tag{2-12}$$

$$Q_L=\frac{\omega_o(L_s+L_g)}{R_s}=\frac{1}{\omega_o R_s C_{gs}}$$

$$\alpha=\frac{g_m}{g_{d0}}$$

The last noise term is the contribution of the uncorrelated portion of the gate noise. This contributor has the following power spectral density:

$$S_{a,ig,u}(\omega_o)=\xi S_{a,id}(\omega_o)=\frac{4kT\gamma\xi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-13}$$

where $\xi=\frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q^2_L)$

We observe that all of the noise terms contributed by the first device M1 are proportional to $S_{a,id}(\omega_o)$, the contribution of the drain noise. Hence, it is convenient to define the contribution of M1 as a whole as

$$S_{a,M1}(\omega_o)=\chi S_{a,id}(\omega_o)=\frac{4kT\gamma\chi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-14}$$

where, after some slight simplification

$$\chi=\kappa+\xi=1+2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\frac{\delta\alpha^2}{5\gamma}(1+Q^2_L) \tag{2-15}$$

with (2-14) and (2-15), it is clear that the effect of induced gate noise is to modify the

noise contribution of the device in proportion to χ. It follows directly that

$$F=1+\frac{R_\ell}{R_s}+\frac{R_g}{R_s}+\gamma\chi g_{d0}R_s\left(\frac{\omega_o}{\omega_T}\right)^2 \tag{2-16}$$

where χ is defined as in (2-15). By factoring out Q_L from the expression for χ, and noting that

$$g_{d0}Q_L=\frac{g_m}{\alpha}\frac{1}{\omega_o R_s C_{gs}}=\frac{\omega_T}{\alpha\omega_o R_s} \tag{2-17}$$

We can re-express F as

$$F=1+\frac{R_\ell}{R_s}+\frac{R_g}{R_s}+\frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_o}{\omega_T}\right) \tag{2-18}$$

To understand the implications of this new expression for F, we observe that χ includes terms which are constant, proportional to Q_L, and proportional to Q^2_L. It follows that (2-18) will contain terms which are proportional to Q_L as well as inversely proportional to Q_L. Therefore, a minimum F exists for a particular Q_L.

2.3 Principle of Mixers

The mixer is an ubiquitous component of wireless systems. An ideal mixer multiplies the signal at the radio frequency (RF) port with a signal at the local-oscillator (LO) port to create the intermediate-frequency (IF) signal. If the RF and LO signals are sinusoids, it is clear that the IF signal has components at two frequencies. There is a high frequency component at the sum of the RF and LO frequencies, and a low frequency signal at the difference of the RF and LO signals. Therefore, a mixer can effect up conversion or down conversion [5]. In design of RF CMOS mixers is a very challenging task involving trade offs between gain, linearity, noise figure, voltage supply and power consumption.

2.3.1 *Conversion Gain*

One important mixer characteristic is conversion gain, which is defined as

$$\text{Conversion Gain}=\frac{\text{the desired IF output}}{\text{the value of the RF input}} \tag{2-19}$$

The gain of mixers must be carefully defined to avoid confusion. The "voltage conversion gain" of a mixer is defined as the ratio of the rms voltage of the IF signal to the rms voltage of the RF signal. Note that these two signals are centered around two different frequencies. The voltage conversion gain can be measured by applying a sinusoid at ω_{RF} and examining the amplitude of the downconverted component at ω_{IF}.

The "power conversion gain" of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source. If the input impedance and the load impedance of the mixer are both equal to the source impedance, for example, 50Ω, then the voltage conversion gain and power conversion gain of the mixer are equal when expressed in decibels.

Conjugate matching at the input of the mixers is necessary in the first downconversion stage of heterodyne receivers that employ image reject filters. The transfer function of these filters is usually characterized for only a standard termination impedance and may exhibit ripples if other impedance levels are used. The load impedance of the mixer, on the other hand, is typically not equal to 50Ω because most passive IF filters have an input impedance of 500 to 1000Ω. In architectures such as homodyne topologies, the load seen by the mixer may be even higher to maximize the voltage gain.

From the above observation, we note that the voltage and power conversion gains of a mixer may not be equal in decibels.

2.3.2 *Noise Figure : SSB and DSB*

Noise Figure is defined as

$$\text{Noise Figure}=\frac{\text{signal to noise ratio at RF port}}{\text{signal to noise ratio at IF port}} \tag{2-20}$$

In a typical mixer, there are actually two input frequencies that will generate a given intermediate frequency. One is the desired RF signal, and the other is called the image signal. The existence of an image frequency complicates noise figure computations because noise originating in both the desired and image frequencies therefore becomes IF noise, yet there is generally no desired signal at the image frequency. In the usual case where the desired signal exists at only one frequency, the noise figure that one measures is called the single-sideband noise figure (SSB NF); the rarer case, where both the "main" RF and image signals contain useful information, leads to a double-sideband (DSB) noise figure. Clearly, the SSB noise figure will be greater than for the DSB case, since both have the same IF noise but the former has signal power in only a single sideband. Hence, the SSB NF will normally be 3dB higher than the DSB NF.

2.3.3 *Isolation*

Isolation is one of another parameter in design mixer. It is generally desirable to minimize interaction among the RF, IF, and LO ports. For instance, since the LO signal power is generally quite large compared with that of the RF signal, any LO feedthrough to the IF output might cause problems at subsequent stages in the signal processing chain. This problem is exacerbated if the IF and LO frequencies are similar, so that filtering is ineffective. Even reverse isolation is important in many instances, since poor reverse isolation might permit the strong LO signal to work its way back to

the antenna, where it can radiate and cause interference to other receivers.

2.3.4 Single Balanced and Double Balanced Gilbert Mixer

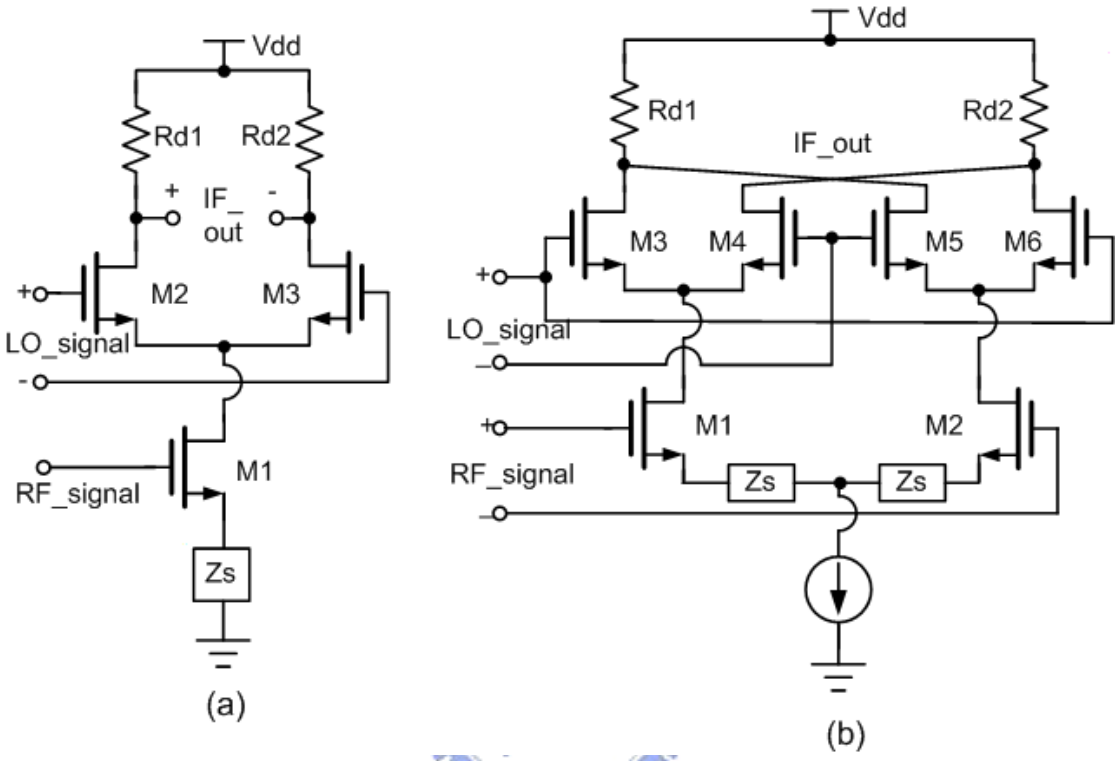


Fig. 2.4 Single Balanced and Double Balanced Gilbert Mixer

The circuit of single balanced and double balanced Gilbert mixer is shown in Fig. 2.4. The lower stage is operated as a transconductance amplifier which converts RF voltage into a current and then performs a multiplication in the current domain. V_{LO} is chosen large enough so that the transistors alternately switch all of the tail current from one side to the other at the LO frequency. In single balanced mixers, the output consists of sum and difference components, each the result of an odd harmonic of the LO mixing with the RF signal. It makes the linearity worse. So the double balanced mixers exploit symmetry to remove the undesired output LO component through cancellation. Double balanced mixers make the linearity better than single balanced mixers.

In the low voltage applications, the DC current source can be replaced by a parallel LC tank to create a zero headroom AC current source. The resonant frequency of the tank should be chosen to provide rejection of whatever common mode component is most objectionable. If several such components exist, one may use series combinations of parallel LC tanks.

2.4 Direct Conversion Receivers

Fig. 2.5 is a simple direct conversion receiver, where the LO frequency is equal to the input carrier frequency. The circuit of Fig. 2.5(a) operates properly only with double-sideband AM signals because it overlaps positive and negative parts of the input spectrum. For frequency- and phase-modulated signals, the down-conversion must provide quadrature outputs [Fig. 2.5(b)] so as to avoid loss of information. This is because the two sides of FM or QPSK spectra carry different information and must be separated into quadrature phases in translation to zero frequency.

The simplicity of the direct conversion architecture offers two important advantages. First, the problem of image is circumvented because $\omega_{IF}=0$. As a result, no image filter is required, and the LNA need not drive a 50Ω load. Second, the IF SAW filter and subsequent down-conversion stages are replaced with low pass filters and base-band amplifiers that are amenable to monolithic integration. But this architecture has a DC offset problem. We will discuss this issue in detail below.

DC Offsets problem:

Since in a direct conversion topology the downconverted band extends to zero frequency, extraneous offset voltages can corrupt the signal and, more importantly, saturate the following stages. To understand the origin and impact of offsets, consider the receiver shown in Fig. 2.6, where the LPF is followed by an amplifier and an A/D

converter. Let us make two observations. First, the isolation between the LO port and the inputs of the mixer and LNA is not infinite; that is, a finite amount of feedthrough exists from the LO port to points A and B [Fig. 2.6(a)]. Called " LO leakage," this effect arises from capacitive and substrate coupling and, if the LO signal is provided externally, bond wire coupling. The leakage signal appearing at the inputs of the LNA and the mixer is now mixed with the LO signal, thus producing a DC component at point C. This phenomenon is called "self-mixing." A similar effect occurs if a large interferer leaks from the LNA or mixer input to the LO port and is multiplied by itself [Fig. 2.6(b)]. Second, the total gain from the antenna to point X is typically around 80 to 100dB so as to amplify the microvolt input signal to a level that can be digitized by a low cost, low power ADC. Of this gain, typically 25 to 30dB is contributed by the LNA/mixer combination.

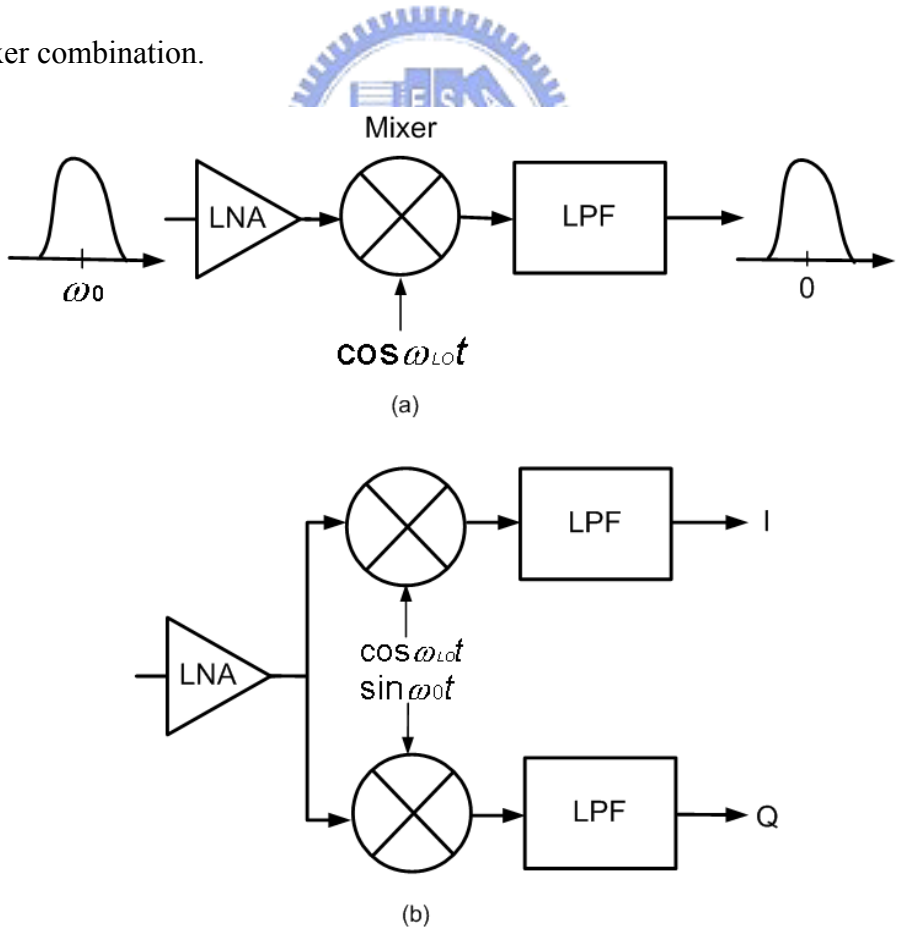
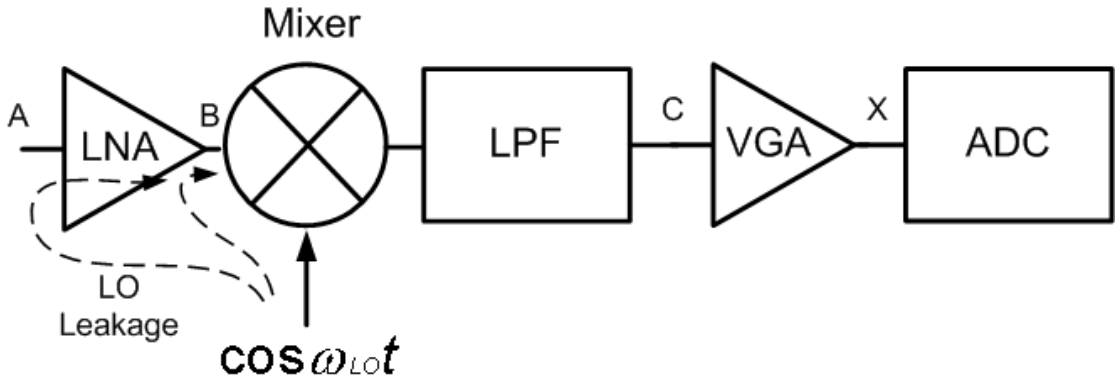
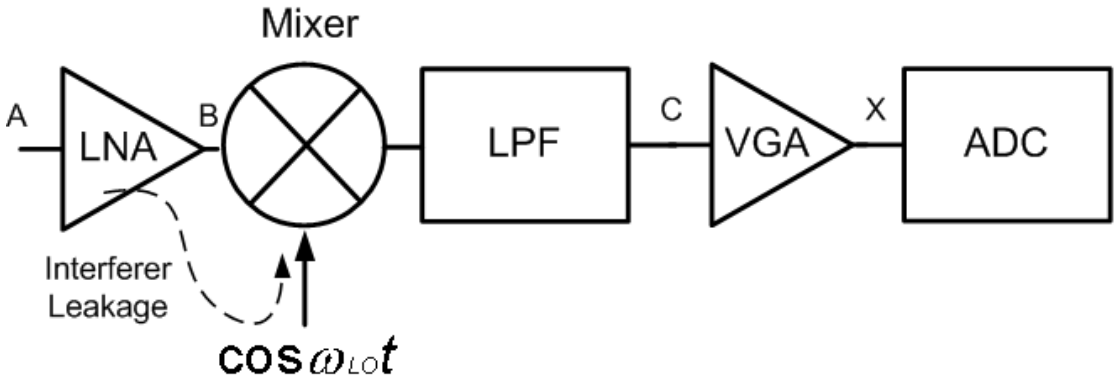


Fig. 2.5 (a) Simple direct conversion receiver

(b) Direct conversion receiver with Quadrature downconversion



(a)



(b)

Fig. 2.6 Self-mixing of (a) LO Signal (b) A strong interferer

Chapter 3

Ultra-wideband Low Noise Amplifier

This chapter describes principle of Ultra Wideband Low Noise Amplifier and this chip fabricated by TSMC 0.18 μm RF CMOS technology.

3.1 Introduction

Due to data communication capacity increase progressively and portable, the wide bandwidth and low power are the urgent requirements. Therefore, FCC allocated 7500MHz of spectrum for unlicensed use of UWB devices in 3.1 to 10.6GHz frequency band and defined power consumption must less than 250mW. The first stage of the UWB receiver front end is LNA. There are many critical parameters in design ultra wideband amplifier, such as broadband flat gain, good linearity, good noise performance, good group delay, and good input matching from dc to high frequency. Distributed Amplifier (DA) is a popular solution to implement ultra wideband amplifier. DA usually employs transmission line to transfer signal to next stage without loss. Its frequency range can extend to high frequency, but power consumption and die size are very large. Another method is used chebyshev band-pass filter to achieve broadband matching [6]. This method's don't consume more power consumption to achieve broadband function. In next chapter, we will use this method to implement a mixer. In this chapter, we employ resistance negative feedback to achieve broadband matching and use skill of pain peaking method to compensate the gain loss at high frequency.

3.2 Principle of the Circuit Design

In this section, the design of ultra wideband low noise amplifier is presented. Fig. 3.1 is the schematic of ultra-wideband low noise amplifier. The circuit includes two stage common source amplifiers. M1 is the input transconductance. The resistors, R_{F1} and R_{F2} provide input and output matching and self-biasing. The transistor M2 is the second stage transconductance. It provides better isolation and system LNA transconductance gain improve.

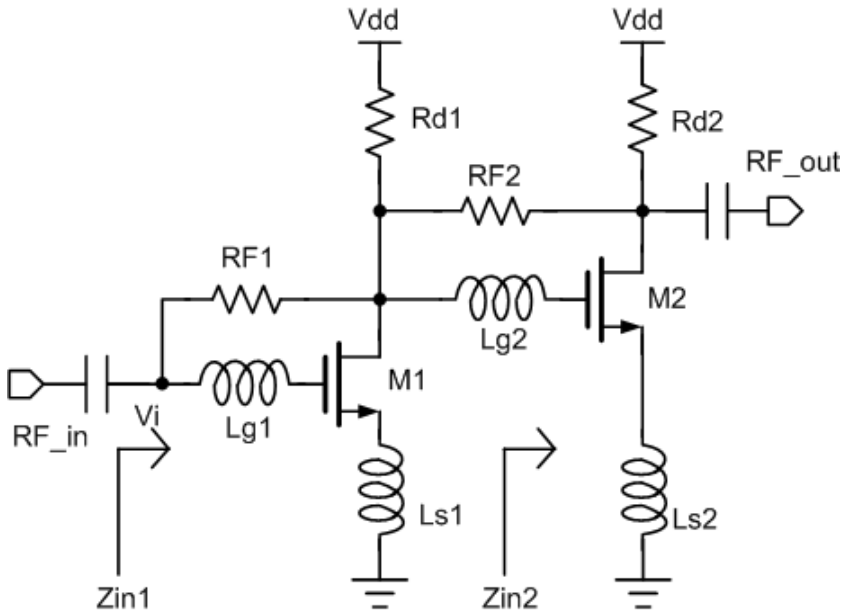


Fig. 3.1 Schematic of ultra wideband low noise amplifier

3.2.1 Input Matching principle

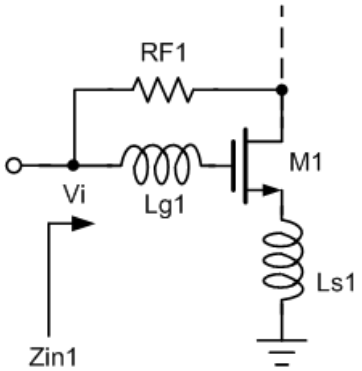


Fig. 3.2 Input matching of ultra wideband LNA

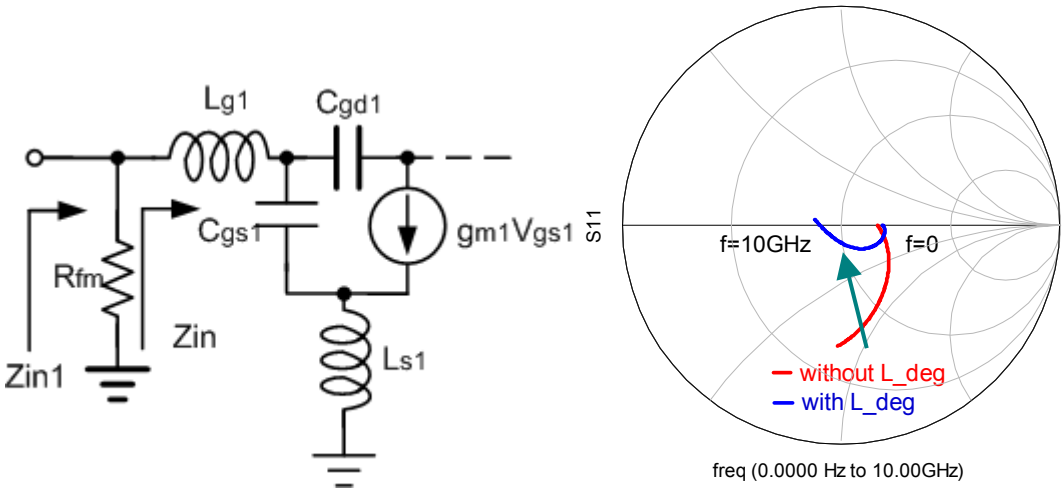


Fig. 3.3 Input small signal model and L-deg effect of ultra wideband LNA

The LNA input stage is shown as the Fig. 3.2, and Fig. 3.3 is equivalent circuit. The input matching network has combined two matching methods. One is inductive source degeneration matching, and another one is resistive negative feedback. Using this method, the input matching can rather extend to high frequency as Fig. 3.3's smith chart. If the C_{gd} is neglected, the input impedance can be expressed as the following

$$Z_{in1} \approx R_{fm} // Z_{in} = \frac{R_{F1}}{1-A_{v1}(s)} // \left[s(L_{g1}+L_{s1}) + \omega_T L_{s1} + \frac{1}{sC_{gs1}} \right] \quad (3\text{-}1)$$

where R_{fm} is Miller effect impedance of R_{F1}. $A_{v1}(s)$ is the voltage gain of the first stage.

In the low frequency, the input impedance is

$$Z_{in1}|_{\omega=0} \approx Z_{fm} = \frac{R_{F1}}{1-A_{v1}(s)} \quad (3\text{-}2)$$

Depending on equation (3-2), we can observe the resistance is determined by R_{F1} at the low frequency.

At the resonance frequency, Z_{in1} can express as the following equation.

$$Z_{in1}|_{\omega=\omega_o} \approx \frac{R_{F1}}{1-A_{v1}(s)} // \omega_T L_{s1} \approx \omega_T L_{s1} \quad (3\text{-}3)$$

Depending on equation (3-3), we can observe the $Z_{in1} \approx \omega_T L_{s1}$ at the resonance frequency. Since these two levels $Z_{in1}(\omega=0)$ and $Z_{in1}(\omega=\omega_0)$ give the impedance range as the frequency sweeps, adjusting both levels near 50Ω shall ensure good S11 over the entire frequency band.

3.2.2 Ultra wideband gain flatness analysis

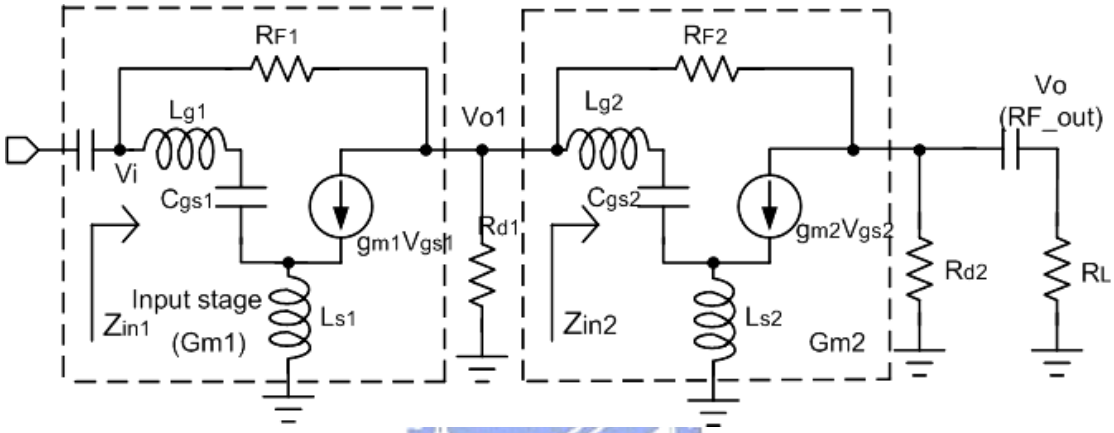


Fig. 3.4 Small signal circuit of ultra wideband low noise amplifier

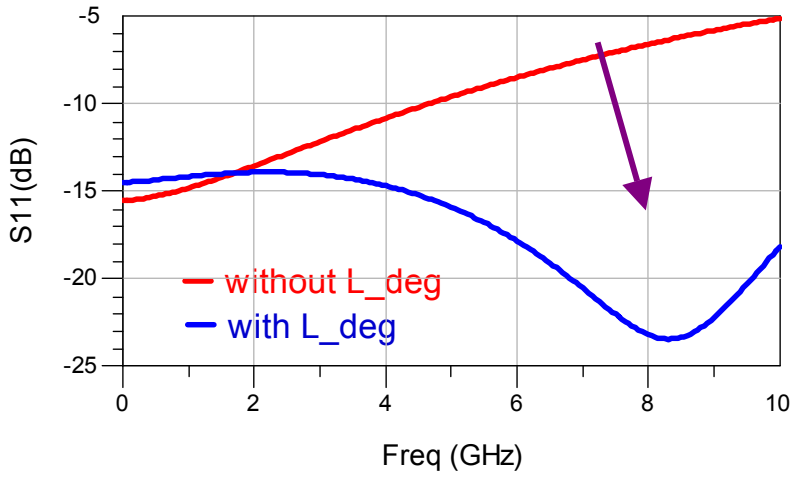


Fig. 3.5 S11 with and without L_deg input matching

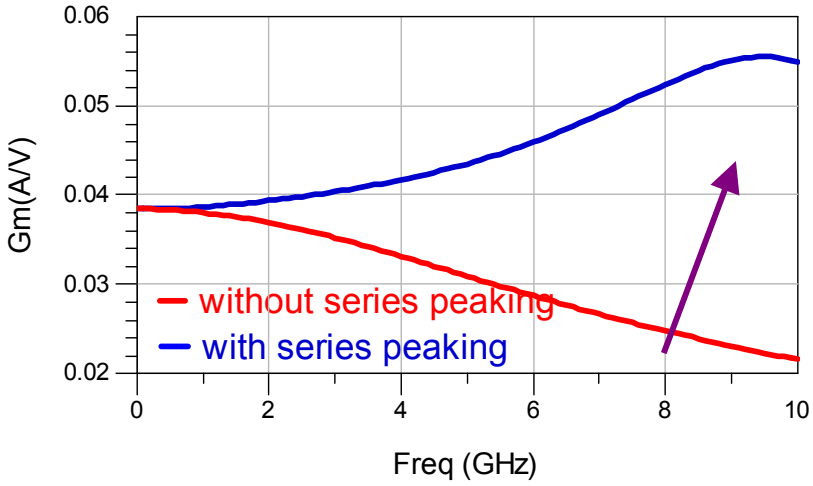


Fig. 3.6 Gm with and without series peaking of second stage

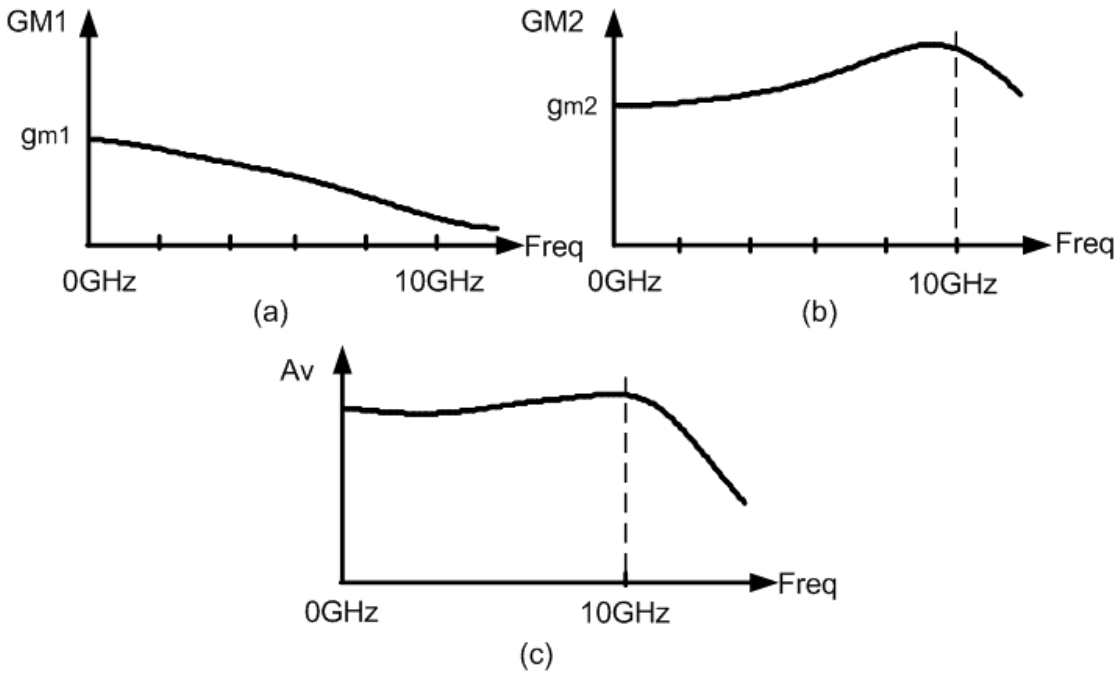


Fig. 3.7 Frequency response of ultra wideband low noise amplifier

The Fig. 3.4 is the small signal circuit of ultra wideband amplifier. All the analysis, the C_{gd} is ignored. The complete voltage gain of ultra wideband LNA can be expressed as

$$A_v=\frac{V_o}{V_{o1}}\frac{V_{o1}}{V_i}\frac{V_i}{V_s}=G_{m2}\cdot(R_{d2}//R_L)\cdot G_{m1}\cdot(R_{d1}//Z_{in2})\cdot\frac{Z_{in1}}{Z_{in1}+R_s}$$
$$\approx\frac{1}{2}\cdot G_{m1}\cdot G_{m2}\cdot(R_{d1}//Z_{in2})\cdot(R_{d2}//R_L) \quad (3\text{-}4)$$

where

$$Z_{in1} \approx R_{fm} // Z_{in} = \frac{R_{F1}}{1-A_{v1}(s)} // \left[s(L_{g1}+L_{s1}) + \omega_T L_{s1} + \frac{1}{sC_{gs1}} \right]$$

$$Z_{in2} = \frac{R_{F2}+(R_{d2}//R_L)}{1+\frac{sC_{gs2}\cdot\omega_{o2}^2\cdot\left[R_{F2}+(R_{d2}//R_L)\right]}{s^2+s\frac{\omega_{o2}}{Q_2}+\omega_{o2}^2} + \frac{g_{m2}\cdot\omega_{o2}^2\cdot(R_{d2}//R_L)}{s^2+s\frac{\omega_{o2}}{Q_2}+\omega_{o2}^2}}$$

where Rs is source impedance. G_{m1} is the first stage of M1 transconductance. G_{m2} is the second stage of M2 transconductance. Z_{in1} is the input stage impedance. Z_{in2} is the second stage input impedance. R_L is the load impedance. ω_{o1}, ω_{o2} are the resonance frequency of the first and second stage.

The purpose of the first stage of LNA let input matching S11 less than 10dB from dc to 10GHz which is described in section 3.2.1. According to the equation (3-5), $\omega_{o1}=1/\sqrt{(L_{g1}+L_{s1})\cdot C_{gs1}}$, we can decide the Lg1=0.85nH and Ls1=0.7nH resonance at 10GHz. The Fig. 3.5 shows the condition with and without L_deg and the G_{m1}'s frequency response is shown in Fig. 3.7(a). Due to Gm1 frequency response is not flatness, we add another stage to compensate high frequency transconductance gain. The G_{m2} frequency response is shown as Fig. 3.6. The Lg2=1.2nH and Ls2=0.4nH resonance at 10GHz. The transconductance Gm2 is higher than low frequency at resonance frequency. According to (3-4), the voltage gain is Gm1*Gm2*output resistive. The Fig. 3.7 (c) is the frequency response after the gain compensation. The G_{m1}, G_{m2} can be derived as

$$G_{m1} = \frac{g_{m1}}{\left[s^2 C_{gs1}(L_{g1}+L_{s1}) + sC_{gs1}\omega_T L_{s1} + 1\right]} - \frac{1}{R_{F1}} = \frac{g_{m1}}{s^2+s\frac{\omega_{o1}}{Q_1}+\omega_{o1}^2} - \frac{1}{R_{F1}} \quad (3\text{-}5)$$

where $\omega_{o1}=\frac{1}{\sqrt{(L_{g1}+L_{s1})\cdot C_{gs1}}}$ $Q_1=\frac{1}{g_{m1}\cdot L_{s1}\cdot \omega_{o1}}$

$$G_{m2}=\frac{g_{m2}}{\left[s^2C_{gs2}(L_{g2}+L_{s2})+sC_{gs2}\omega_T L_{s2}+1\right]}-\frac{1}{R_{F1}}$$

$$=\frac{g_{m2}}{s^2+s\frac{\omega_{o2}}{Q_2}+\omega_{o2}{}^2}-\frac{1}{R_{F2}}$$

where $\omega_{o2}=\frac{1}{\sqrt{(L_{g2}+L_{s2})\cdot C_{gs2}}}$ $Q_2=\frac{1}{g_{m2}\cdot L_{s2}\cdot \omega_{o2}}$

3.3 Chip Implementation and Measured Result

3.3.1 Microphotograph of Chip

A microphotograph of the UWB LNA circuit is shown in Figure3.6. The circuit is fabricated in the TSMC 0.18μm CMOS technology. The die area including bonding pads is 0.873 mm by 0.636 mm.

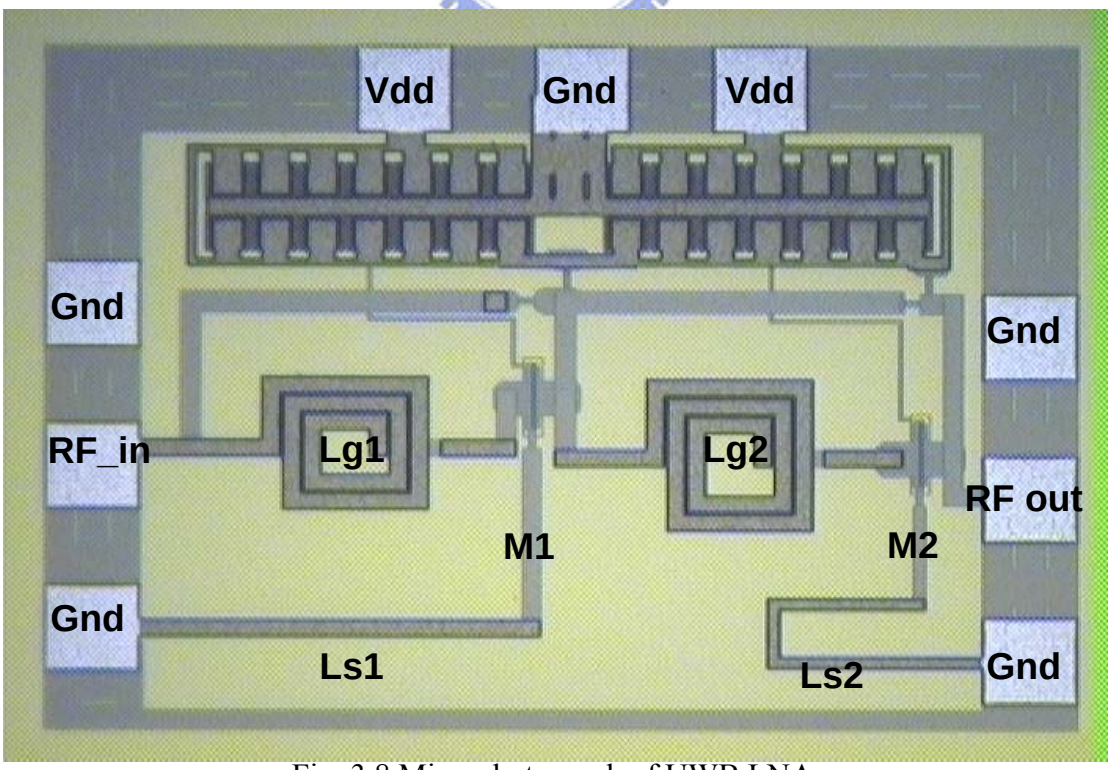


Fig. 3.8 Microphotograph of UWB LNA

3.3.2 Measurement and Simulation Result

Measurement is conducted by on-wafer RF probing. Measured S-parameters are plotted in Fig. 3.7 to Fig. 3.14, together with simulation results and troubleshooting for comparison. The solid line is the measured data. The circle plot is the simulation result. The square plot is the troubleshooting result.

The measured power gain S21 achieves the maximum value of 6.3dB at 100MHz. It is almost matched the simulation result at low frequency. Above 6GHz, the measured power gain start to decrease and deviate from the simulation result. The measured 3dB bandwidth range is from 100MHz to 6.6GHz. Because of the lower gain measured in high frequency, the higher noise figure is measured. The Fig. 3.11 is shown the condition. The difference of measured data and simulation result on the S21 may be due to the lower transconductance. From the equation $\omega_T = g_m / C_{gs}$, we can understand the transconductance and cutoff frequency is determined by transistor's input capacitor. A capacitor (Cp=150fF) is included between the gate and source of the transistor. It is in order to reduce the input transconductance of the transistor for troubleshooting. In the Fig. 3.7, the square plot is the troubleshooting result which is similar to the measured result. The other S-parameters such as S11, S22 and S12 are similar to the simulation result.

The Fig. 3.11 is the measured and simulation result of noise figure. The measured data is above the simulation result. The average value of noise figure is 8.1dB. Discrepancy at high frequency may be the degradation of S21 and inaccurate noise model. The linearity analysis is conducted by the two-tone test. The Fig. 3.12 is the linearity measured data at 5GHz. The Fig. 3.13 is the IIP3 measured data at 3~8GHz. The Fig. 3.14 is the group delay simulation and measured data. The simulation result is 67~71ps. The measured result is 40~83ps. The total power of the

UWB LNA is 16.2mW with a power supply 1.8V. The table 3.1 is the summary of measured performance and comparison to other wideband amplifier.

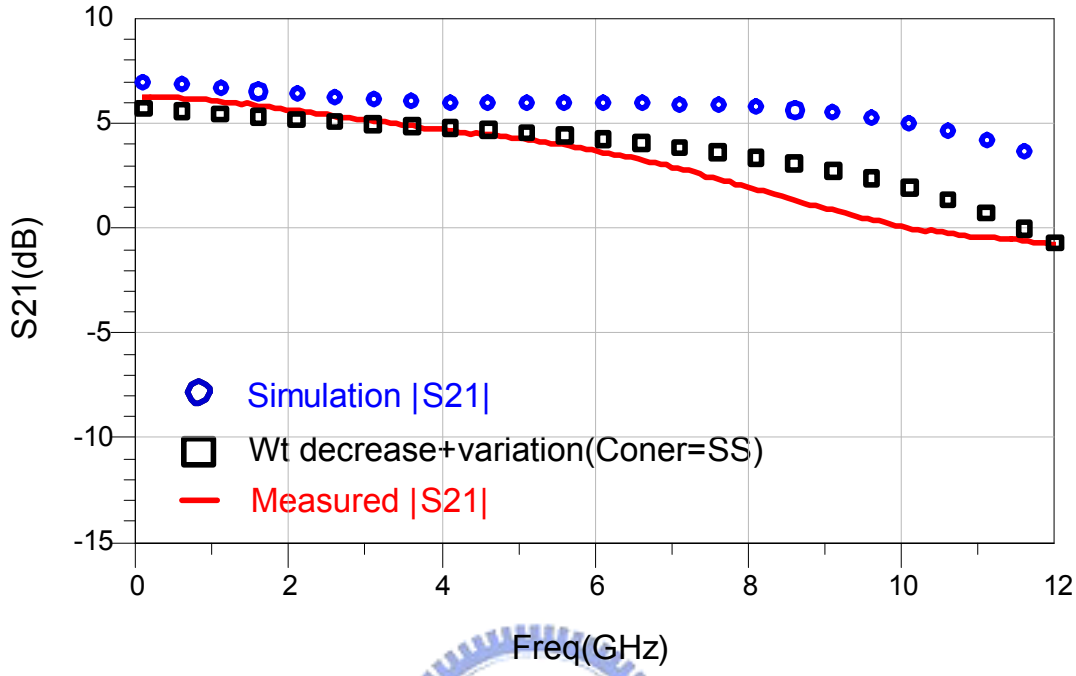


Fig. 3.9 S21 simulation and measured result of UWB LNA

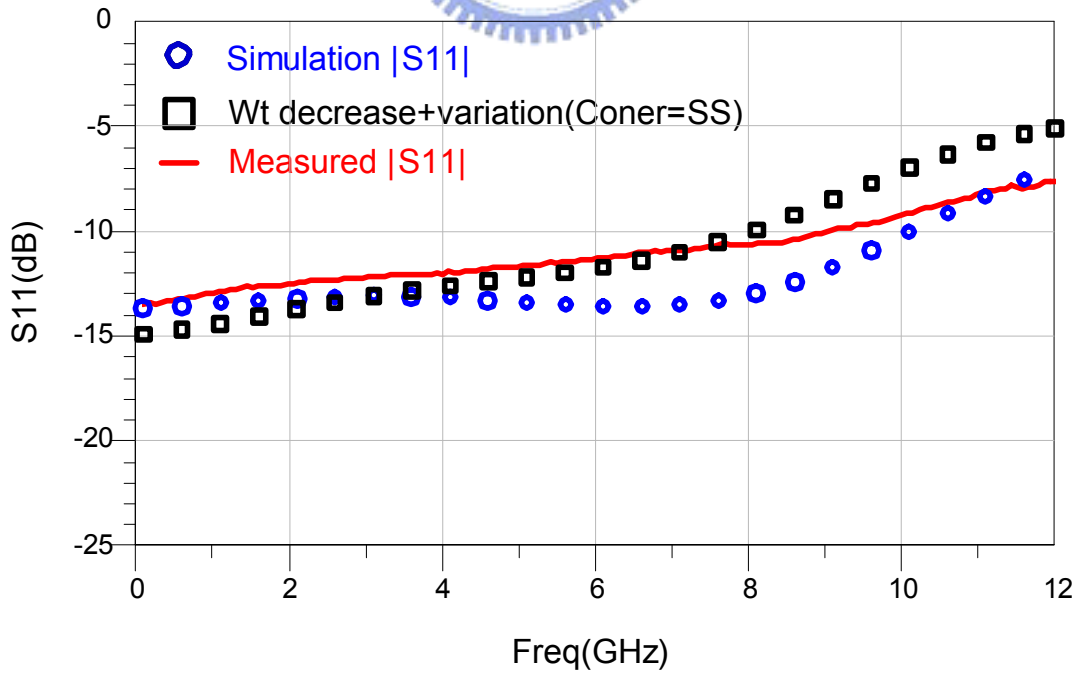


Fig. 3.10 S11 simulation and measured result of UWB LNA

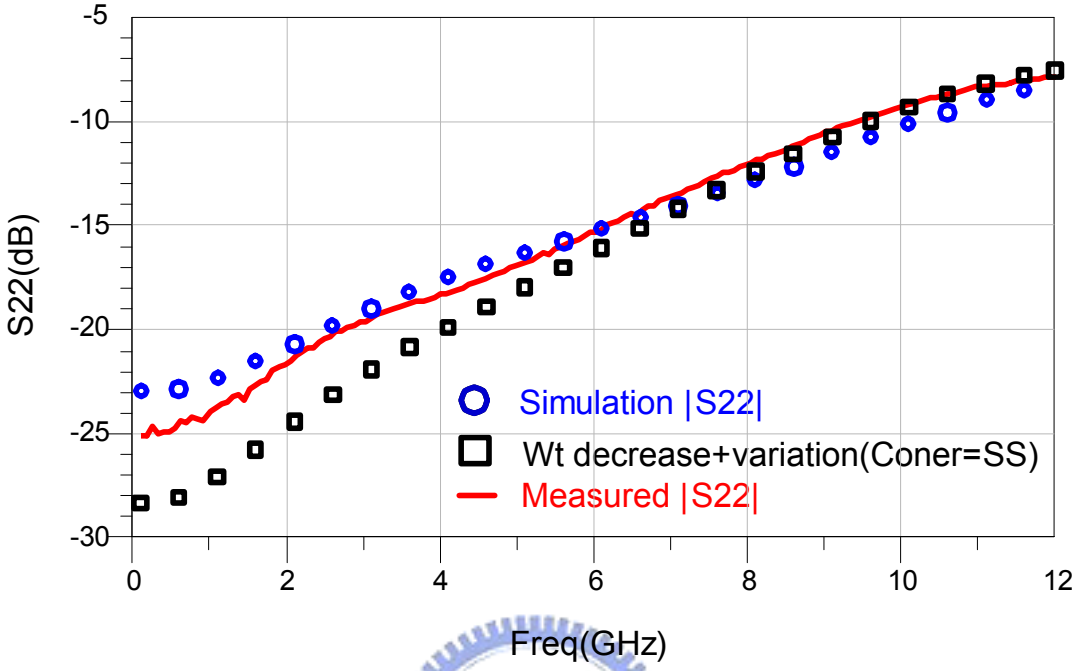


Fig. 3.11 S22 simulation and measured result of UWB LNA

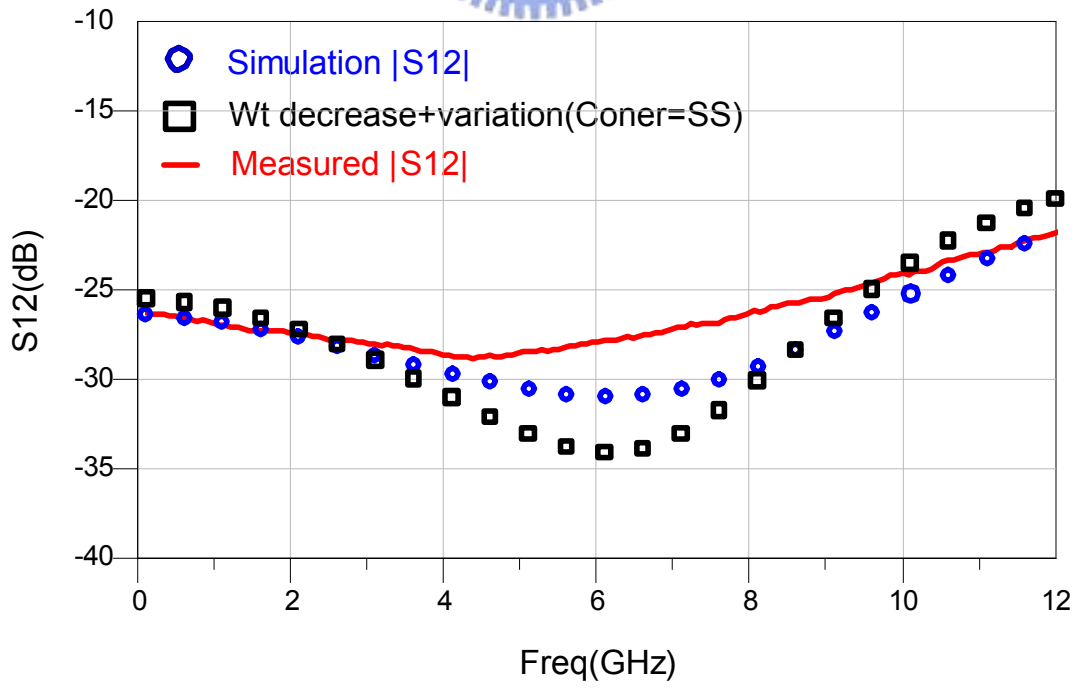


Fig. 3.12 S12 simulation and measured result of UWB LNA

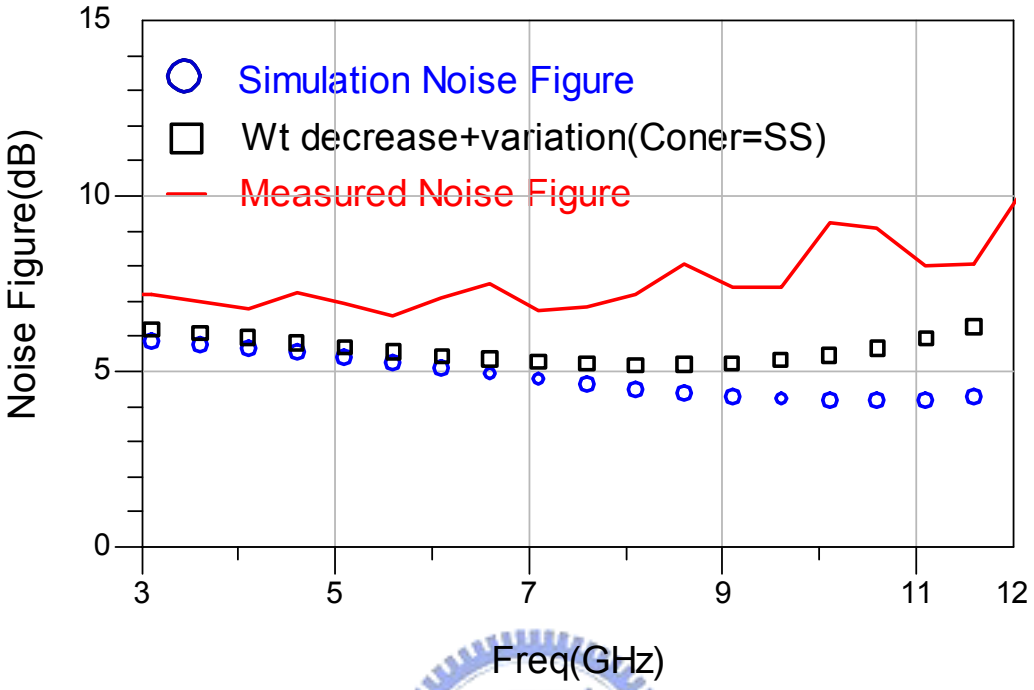


Fig. 3.13 Noise Figure simulation and measured result of UWB LNA

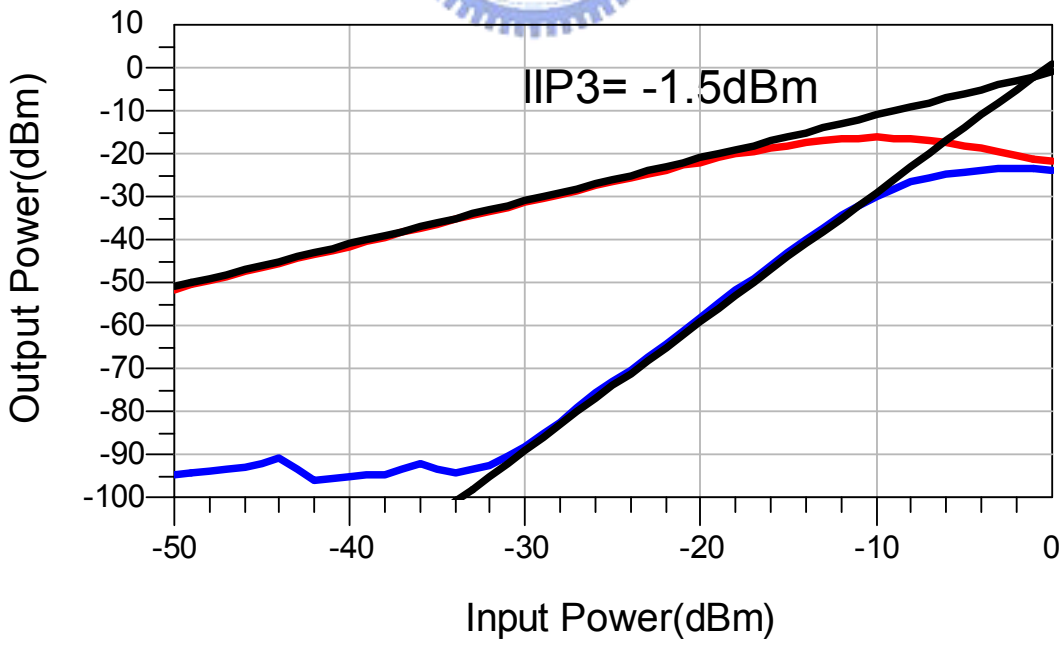


Fig. 3.14 Linearity at 5GHz of UWB LNA

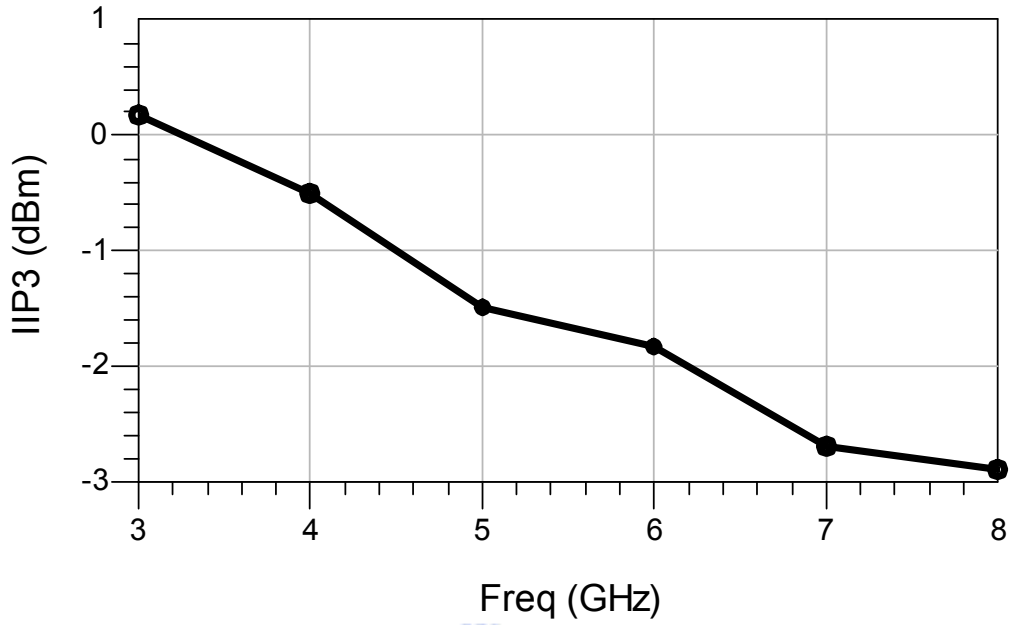


Fig. 3.15 Linearity measured result versus frequency

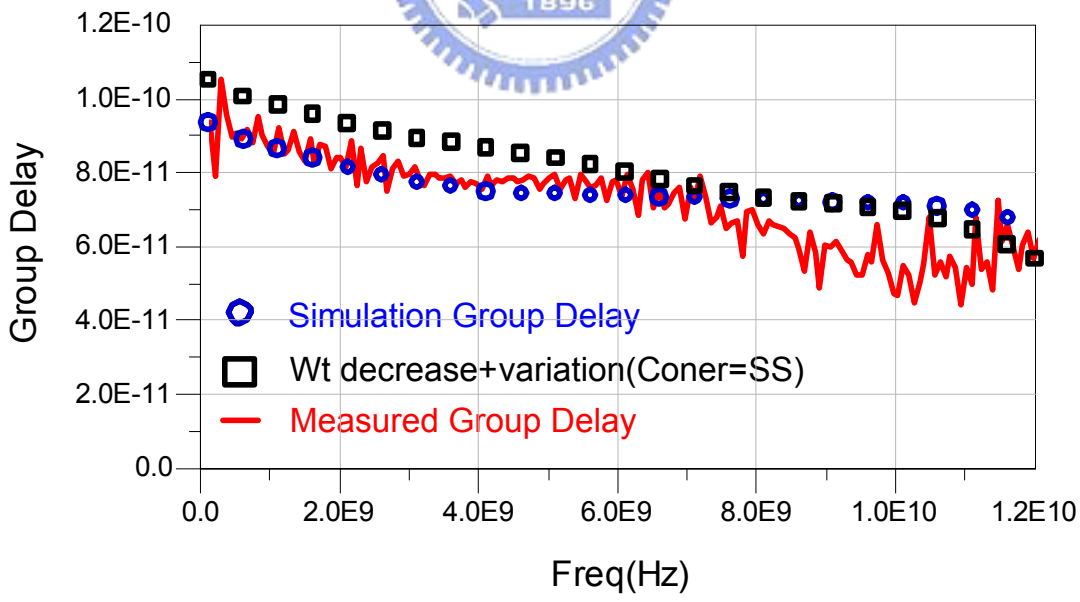


Fig. 3.16 Group Delay simulation and measured result of UWB LNA

TABLE 3.1 Summary of measured performance and comparison to other wideband amplifier

	BW[GHz]	Gmax[dB]	S11[dB]	NFmin[dB]	IIP3[dBm]	Area[mm^2]	P[mW]
Simulation	0.1-10	6.7	<-10	4.1	-3.1	0.54	16.2
Measured	0.1-6.6	6.2	<-10	6.5	-1.6	0.54	16.2
[7]	2.9-9.2	9.3	<-9.9	4.0	-6.7	1.1	9
[8]	0.6-22	7.3	<-8	4.3	N/A	1.35	52
[9]	0.5-4	6.5	<-7	5.4	N/A	0.62	83.4
[10]	1.5-7.5	5.5	<-9.5	8.5	N/A	2.86	216

3.4 Conclusion

In this work, we design an ultra wideband low noise amplifier for the receiver path of UWB system which is used the standard TSMC 0.18μm CMOS process. This circuit uses the feedback resistor and inductive degeneration to achieve the input, output broadband matching. Between two stages, we add an inductor to compensation the high frequency transconductance. The measured result shows that S11, S22 and S12 parameters are similar to simulation result. It shows the L-degeneration method is useful at this work. The measured 3dB frequency range is from 0.1 to 6.6GHz. The measured maximum power gain is 6.2dB. The average IIP3 is -1.6dB. The noise figure minimum is 6.5dB. From Table 3.1, the power consumption of our work is lower than other distributed amplifier [8,9,10] and die size is also small than others.

Chapter 4

A 3 ~ 8 GHz Direct Conversion Broadband Mixer

This chapter describes circuit design principle of a 3~8GHz direct conversion broadband mixer. And this chip fabricated by TSMC 0.18 μm RF CMOS technology.

4.1 Introduction

Due to data communication capacity increase progressively, the wide bandwidth and low power are the urgent requirements.

Direct conversion receiver (DCR) is most popular architecture in recently years. The frequency of RF signal is the same with the frequency of LO (local oscillator) signal, and down converts to around DC frequency. The homodyne receiver (DCR) offers two important advantages over a heterodyne receiver. First, there are no image problems, so image rejection filter is not required. Second, the SAW filter and subsequent down-conversion stages are replaced with low pass filter and baseband amplifiers that are amenable to monolithic integration. In general, the homodyne receiver just needs small chip area.

In this chapter, we employ chebyshev filter to design a 3~8GHz direct conversion mixer. Its advantage has easy to achieve high gain, broadband matching and doesn't consume extra power but it needs large die size and accurate inductor model. Therefore, this mixer can receive signals from 3~8GHz and down convert to baseband signal directly. The extra current source is used to decrease the current of switch MOS, and increase the lower stage's transconductance gain. An inductor adds to the inter-stage between the switch and transconductance stage whose the high frequency gain can be improved.

4.2 Principle of the Circuit Design

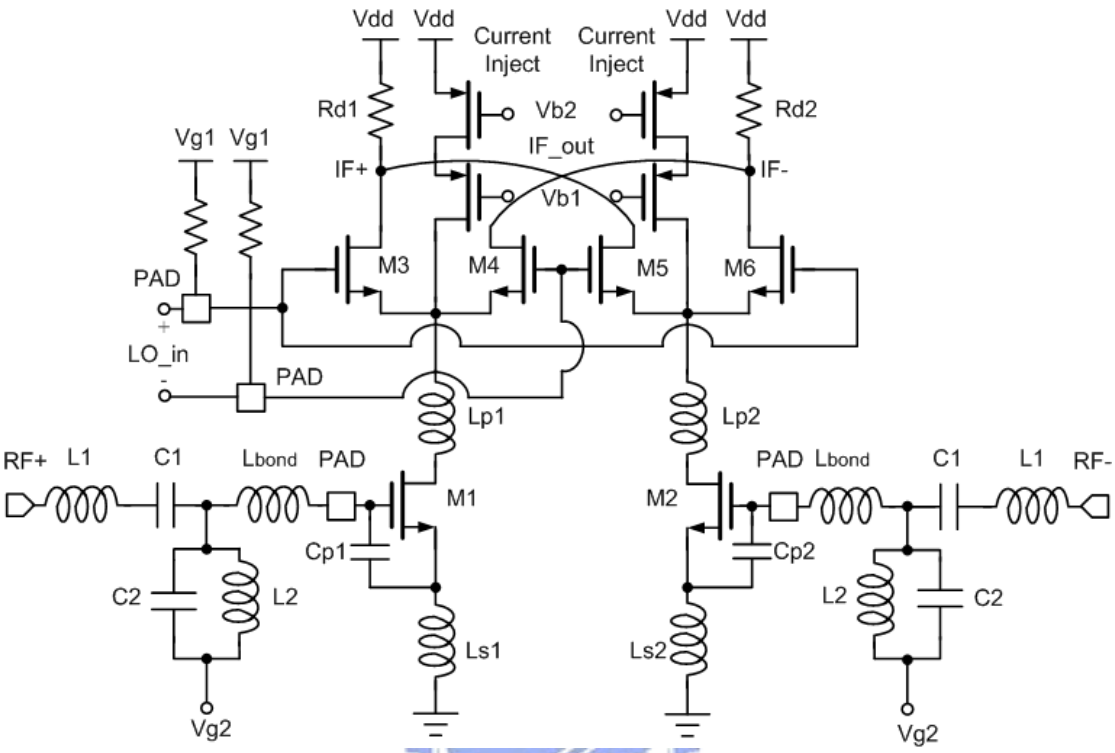


Fig. 4.1 Schematic of 3~8GHz direct conversion broadband mixer

In this section, the circuit design principle of 3~8GHz direct conversion mixer is presented. This circuit of mixer uses chebyshev filter design to achieve broadband matching. In section 4.2.1 will introduce the broadband matching. Inductor adds to the inter-stage between the switch and transconductance stage then the high frequency gain can be improved. In section 4.2.2 will introduce the inductive peaking function. In order to down covert the RF signal, the mixing stage is needed. In section 4.2.3 will introduce the mixing stage.

4.2.1 Input Broadband Matching

Fig. 4.2 shows the input impedance matching of this circuit. Input matching uses the chebyshev filter design. The filter design technique has two kinds of methods. One

is the image parameter method, and another one is insertion loss method [11]. In this work, we use insertion loss method to design filter. Insertion loss uses network synthesis techniques to design filters with a completely specified frequency response. The design is simplified by beginning with low pass filter prototypes that are normalized in terms of impedance and frequency. Transformations are then applied to convert the prototype designs to the desired frequency range and impedance level. So, the insertion loss method is the most common technique to design filter. The Fig. 4.3 shows the filter design procedure of insertion loss method.

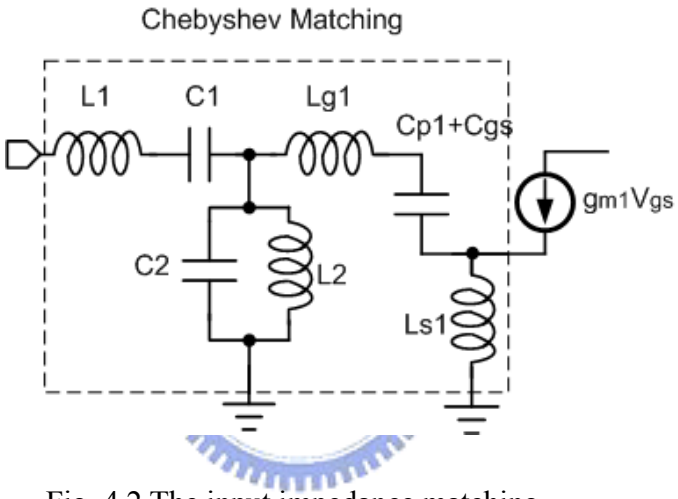


Fig. 4.2 The input impedance matching

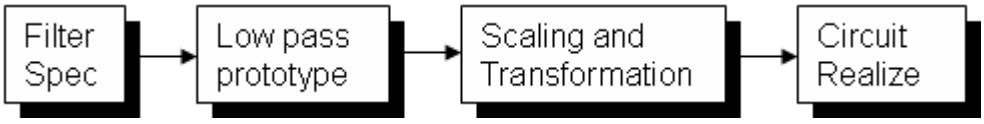


Fig. 4.3 Insertion loss method design procedure

4.2.1.1 Low Pass Filter Prototype

In the insertion loss method a filter response is defined by its insertion loss, or power loss ratio, PLR:

$$P_{LR}=\frac{\text{Power available from source}}{\text{Power delivered to load}}=\frac{1}{1-|\Gamma(\omega)|^2} \qquad (4\text{-}1)$$

where $|\Gamma(\omega)|^2 = \Gamma(\omega)\cdot\Gamma^*(\omega) = \Gamma(\omega)\cdot\Gamma(-\omega) = |\Gamma(-\omega)|^2$, so

$|\Gamma(\omega)|^2$ is an even function of ω

we can rewrite $|\Gamma(\omega)|^2$ as

$$|\Gamma(\omega)|^2 = \frac{M(\omega^2)}{M(\omega^2)+N(\omega^2)} \tag{4-2}$$

where M and N are real polynomials in ω^2

Substituting this form in equation (4-1), we get

$$P_{LR} = 1 + \frac{M(\omega^2)}{N(\omega^2)} \tag{4-3}$$

Thus, for a filter to be physically realizable its power loss ratio must be of the form in equation (4-3). Notice that specifying the power loss ratio simultaneously constrains the reflection coefficient, $\Gamma(\omega)$. We now discuss two practical filter responses below.

<1>Butterworth filter:

Butterworth response provides the flattest possible passband response for a given filter complexity, or order. For a low pass filter, it is specified by

$$P_{LR} = 1 + k^2\left(\frac{\omega}{\omega_c}\right)^{2N} \tag{4-4}$$

where N is the order of the filter, and ω_c is the cutoff frequency. The passband extends from ω=0 to $\omega=\omega_c$. The power loss ratio is $1+k^2$ at the band edge.

<2>Chebyshev filter:

A chebyshev polynomial is used to specify the insertion loss of an N-order low pass filter as

$$P_{LR} = 1 + k^2 T^2_N\left(\frac{\omega}{\omega_c}\right) \tag{4-5}$$

where $T_N(x) = \cos(N\cdot\cos^{-1}x)$, $x = \frac{\omega}{\omega_c}$

then a sharper cutoff will result, although the passband response will have ripples of amplitude $1+k^2$, as shown in Fig. 4.4, since $T_N(x)$ oscillates between ± 1 for $|x| \le 1$. Thus, k^2 determines the passband ripple level. For large x, $T_N(x) \simeq 1/2(2x)^N$

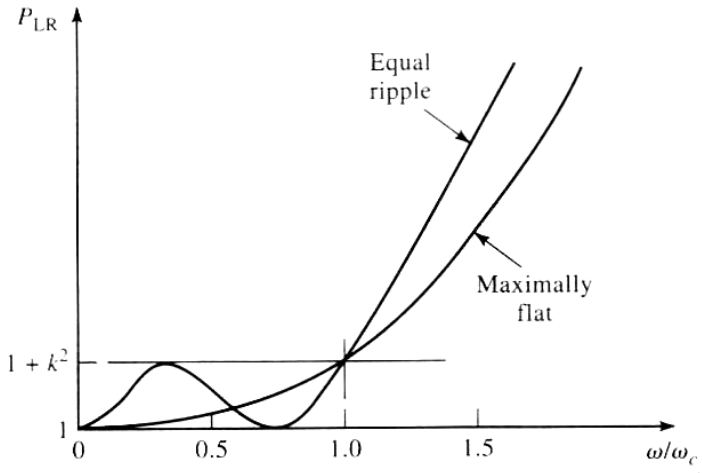


Fig. 4.4 Butterworth and Chebyshev Low pass filter responses (N=3)

From the power loss ratio equation of butterworth and chebyshev filter, then we could derive the normalized element values of L and C of low pass filter prototype. The element values for the ladder type circuits of Fig. 4.5 and the normalize values of L and C are presented in Table 4.1 and Table 4.2.

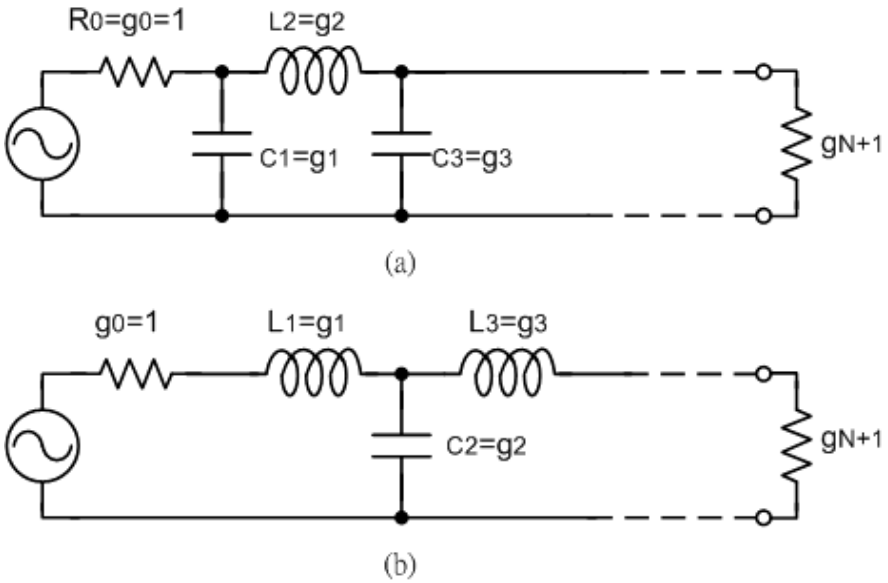


Fig. 4.5 Ladder circuits for Low pass filter prototypes and their element definitions

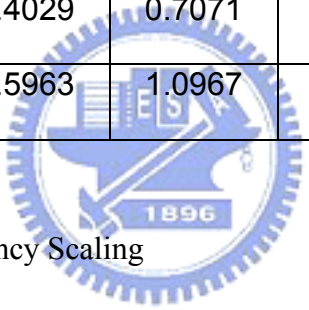
Table 4.1 Element values for Butterworth Low Pass Filter prototypes($g_0=1, \omega_c=1$)

N (order)	g1	g2	g3	g4
1	2.0	1.0		
2	1.4142	1.4142	1.0	
3	1.0	2.0	1.0	1.0

Table 4.2 Element values for Chebyshev Low Pass Filter prototypes($g_0=1, \omega_c=1$)

Ripple=0.5dB

N (order)	g1	g2	g3	g4
1	0.6986	1.0		
2	1.4029	0.7071	1.9841	
3	1.5963	1.0967	1.5963	1.0



4.2.1.2 Impedance and Frequency Scaling

Impedance scaling: In the prototype design, the source and load resistances are unity (expect for chebyshev filters with even N, which have nonunity load resistance). A source resistance of R_0 can be obtained by multiplying the impedances of the prototype design by R_0. Then, if we let primes denote impedance scaled quantities, we have the new filter component values given by

$$L'=R_0L \tag{4-6}$$

$$C'=\frac{C}{R_0} \tag{4-7}$$

$$R'_s=R_0 \tag{4-8}$$

$$R'_L=R_0R_L \tag{4-9}$$

where L, C, and R_L are the component values for the original prototype

Frequency scaling for low pass filters: To change the cutoff frequency of a low pass prototype from unity to ω_c requires that we scale the frequency dependence of the filter by the factor $1/\omega_c$, which is accomplished by replacing ω by ω/ω_c:

$$\omega \leftarrow \frac{\omega}{\omega_c} \tag{4-10}$$

then the new power loss ratio will be

$$P'_{LR}(\omega)=P_{LR}(\frac{\omega}{\omega_c}) \tag{4-11}$$

where ω_c is the new cutoff frequency; cutoff occurs when $\omega/\omega_c = 1$, or $\omega=\omega_c$.

Therefore, the new element values are determined by applying the substitution of (4-10) to the series reactances, $j\omega L_k$, and shunt susceptances, $j\omega C_k$, of the prototype filter. Thus,

$$jX_k=j\frac{\omega}{\omega_c}L_k = j\omega L'_k \Rightarrow L'_k=\frac{L_k}{\omega_c} \tag{4-12}$$

$$jB_k=j\frac{\omega}{\omega_c}C_k = j\omega C'_k \Rightarrow C'_k=\frac{C_k}{\omega_c} \tag{4-13}$$

Usually, both impedance and frequency scaling are required, thus the new value is

$$L'_k=\frac{R_0 L_k}{\omega_c} \tag{4-14}$$

$$C'_k=\frac{C_k}{R_0\omega_c} \tag{4-15}$$

4.2.1.3 Bandpass Transformation

Low pass prototype filter designs can also be transformed to have the bandpass responses illustrated in Fig. 4.6. If ω_1 and ω_2 denote the edges of the passband, then a bandpass response can be obtained using the following frequency substitution:

$$\omega \leftarrow \frac{\omega_0}{\omega_2-\omega_1}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right) \tag{4-16}$$

where $\Delta=\frac{\omega_2-\omega_1}{\omega_0}$

is the fractional bandwidth of the passband. The center frequency, ω0, could be chosen as the arithmetic mean of ω1 and ω2, but the equations are simpler if it is chosen as the geometric mean:

$\omega_0=\sqrt{\omega_1\omega_2}$

Then the transformation of (4-16) maps the bandpass characteristics of Fig. 4.5(b) to the low pass response of Fig. 4.5(a) as follows:

When $\omega=\omega_0$, $\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=0$ (4-17)

When $\omega=\omega_1$, $\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=\frac{1}{\Delta}\left(\frac{\omega_1^2-\omega_0^2}{\omega_0\cdot\omega_1}\right)=-1$ (4-18)

When $\omega=\omega_2$, $\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=\frac{1}{\Delta}\left(\frac{\omega_2^2-\omega_0^2}{\omega_0\cdot\omega_2}\right)=1$ (4-19)

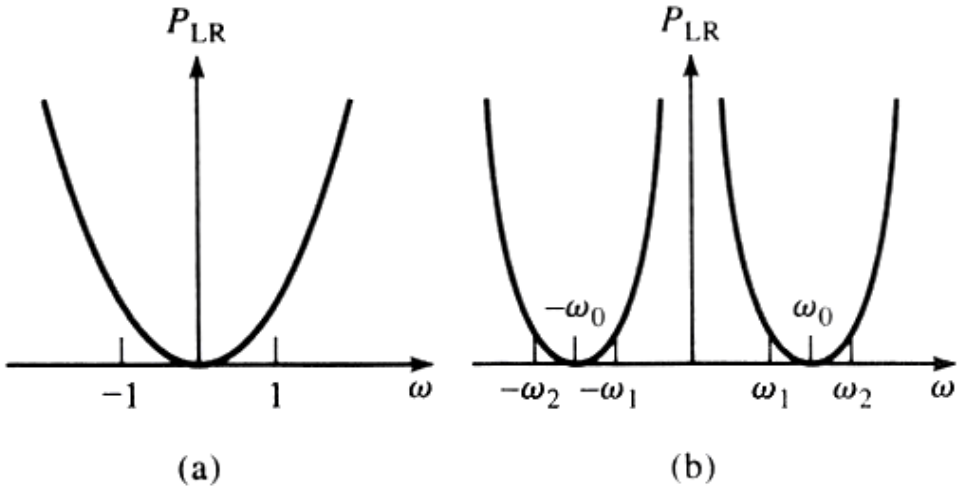


Fig. 4.6 (a) Low pass filter prototype frequency response for ωc=1

(b) Transformation to bandpass filter frequency response

The new filter elements are determined by using (4-16) in the expressions for the series reactance and shunt susceptances. Thus,

$$jX_k=\frac{j}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)L_k=j\omega L_k'-j\frac{1}{\omega C_k'} \tag{4-20}$$

which shows that a series inductor, L_k , is transformed to a series LC circuit with element values,

$$L_k'=\frac{L_k}{\Delta\omega_0} \tag{4-21}$$

$$C_k'=\frac{\Delta}{\omega_0 L_k} \tag{4-22}$$

Similarly,

$$jB_k=\frac{j}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)C_k=j\omega C_k'-j\frac{1}{\omega L_k'} \tag{4-23}$$

which shows that a shunt capacitor, C_k , is transformed to a shunt LC circuit with element values,

$$L_k'=\frac{\Delta}{\omega_0 C_k} \tag{4-24}$$

$$C_k'=\frac{C_k}{\Delta\omega_0} \tag{4-25}$$

The low pass filter elements are thus converted to series resonant circuits (low impedance at resonance) in the series arms, and to parallel resonant circuits (high impedance at resonance) in the shunt arms. Notice that both series and parallel resonator elements have a resonant frequency of ω_0. The Fig. 4.7 shows the condition. The Fig. 4.8 is the complete circuit of low pass filter transformed to bandpass filter.

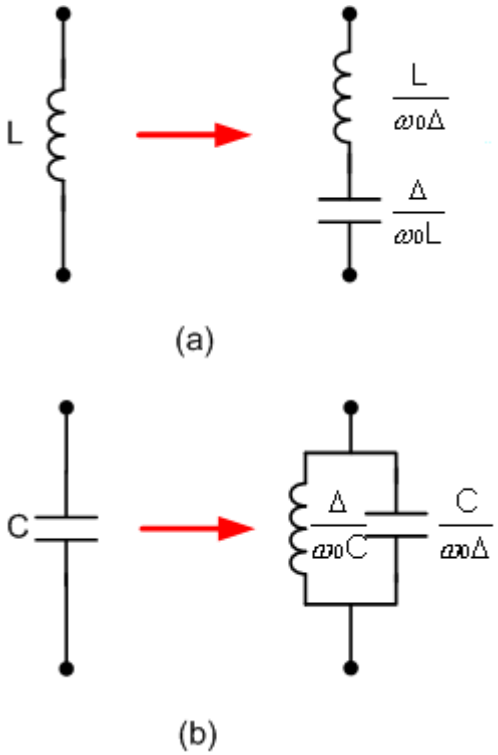


Fig. 4.7 Components transformation of low pass filter transfer to bandpass filter

(a) Series inductor transformed to series LC

(b) Parallel capacitor transformed to shunt LC

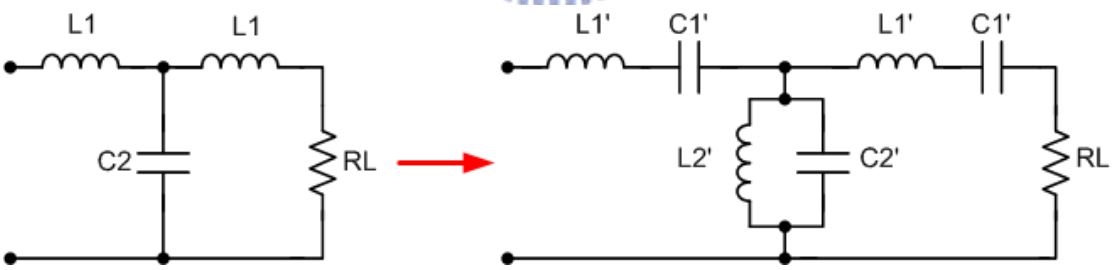


Fig. 4.8 Complete circuit of bandpass filter tansformation

4.2.2 Inductive-peaking Function

The Fig. 4.9 is the inductive peaking function of single end mixer which help us to understand this function [12,13]. The differential pair mixer is the same as the single end. In this double balanced gilbert mixer, we put an inductor (L_{p1}) between

the transconductance stage and mixing stage in order to enhance the high frequency gain. The equivalent circuit is shown in Fig. 4.10. The capacitor (Cp) and resistor (R) is the equivalent model that looking into the mixing stage. The capacitor (C_L) is the equivalent element which looking into the drain node of transconductance stage. As the Fig. 4.10(a), we can derive

$$V_{out}=I_{in}\cdot\frac{R}{sR(C_L+C_p)+1} \tag{4-26}$$

where $\omega=\frac{-1}{R\cdot(C_L+C_p)}$ (pole) (4-27)

(4-27) is shown the pole location would be decrease the signal at high frequency.

As the Fig. 4.10(b) shown, we can derive relationship of current and voltage with inductive peaking function.

$$V_{out}=I_{in}\cdot\frac{R}{s^3RC_pC_LL_{p1}+s^2C_LL_{p1}+sR(C_p+C_L)+1} \tag{4-28}$$

We can adjust L_{p1} to enhance transconductance gain (Gm) at high frequency. The Fig. 4.10 shows the result that with and without inductive peaking.

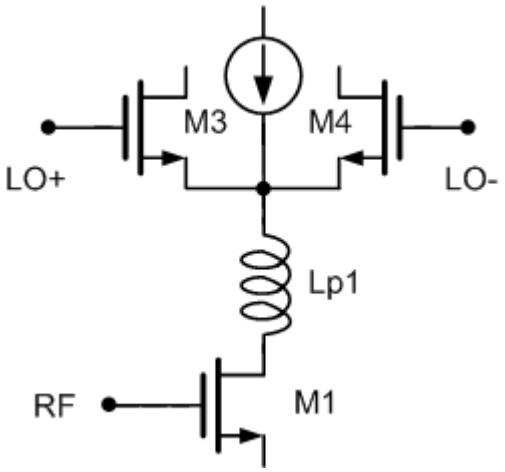


Fig. 4.9 The inductive peaking function

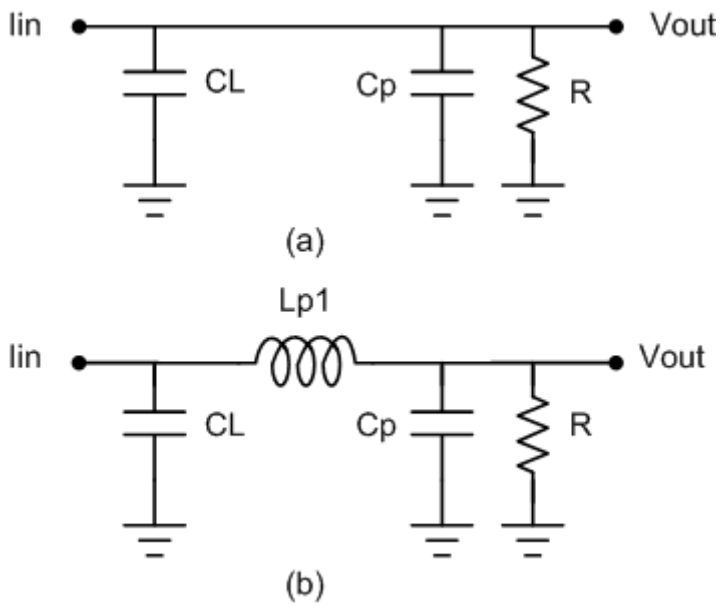


Fig. 4.10 (a) without inductive peaking (b) with inductive peaking

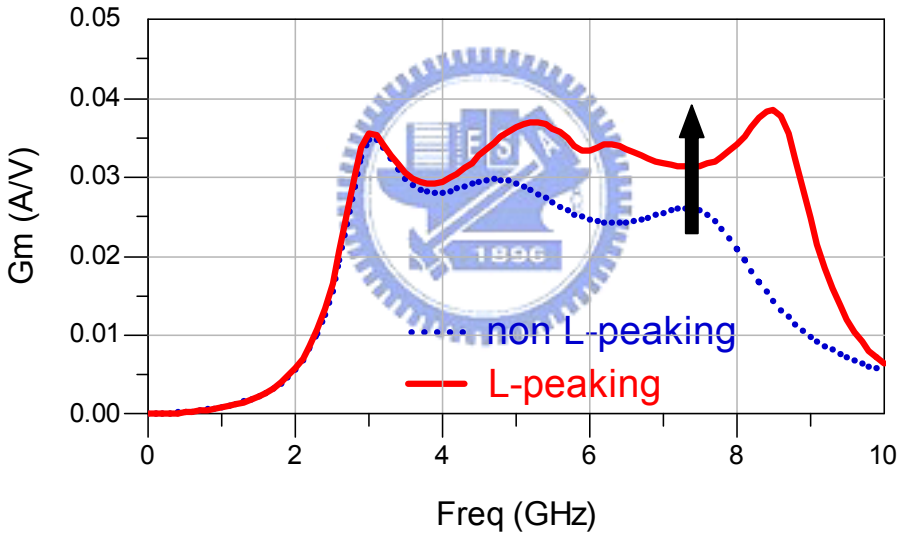


Fig. 4.11 Gm curve with and without inductive peaking

4.2.3 Switching Stage of the 3~8 GHz Direct Conversion Mixer

The Fig. 4.12 is the mixing stage of this mixer. The main noise source of the mixer comes from the flicker noise. The (4-29) is the noise current representation.

$$\overline{i^2_n} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \approx \frac{K}{f} \cdot \omega_T^2 \cdot A \cdot \Delta f \qquad (4\text{-}29)$$

From the equation (4-29), we would observe two conditions to reduce noise. One is increase the transistor area size, and another one is decrease the transistor's gm. The smaller gm means the less current flow of the transistor. The bias current of the transistor set to about 500 μA which is around the saturation region. It can improve the noise figure that bias at around the saturation region. The current source is used to enhance the voltage conversion gain and decrease the current flow of the transistor of M3-M6.

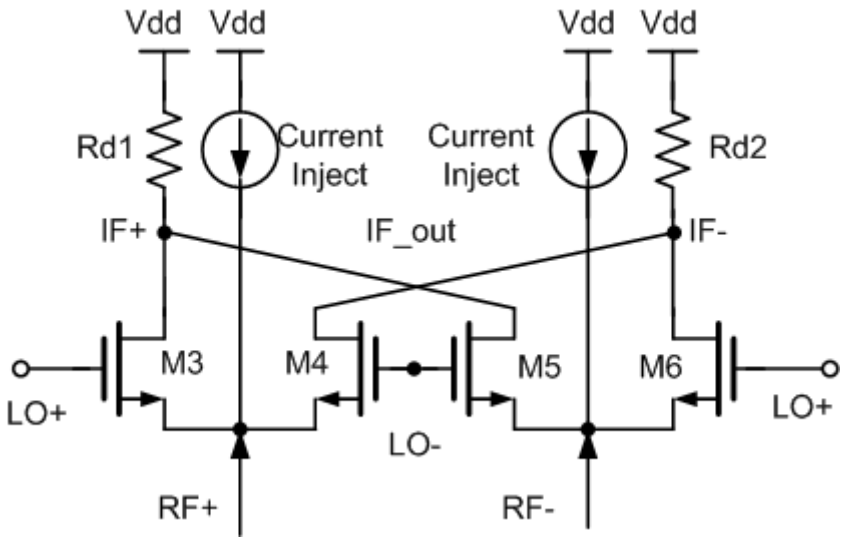


Fig. 4.12 Switching stage of the 3~8GHz direct conversion mixer

4.3 Chip Implementation and Measured Result

4.3.1 Microphotograph of Chip

A microphotograph of the 3~8GHz direct conversion broadband mixer circuit is shown in Fig. 4.13. The circuit is fabricated in the TSMC 0.18μm CMOS technology. The die area including bonding pads is 0.96 mm by 0.985 mm.

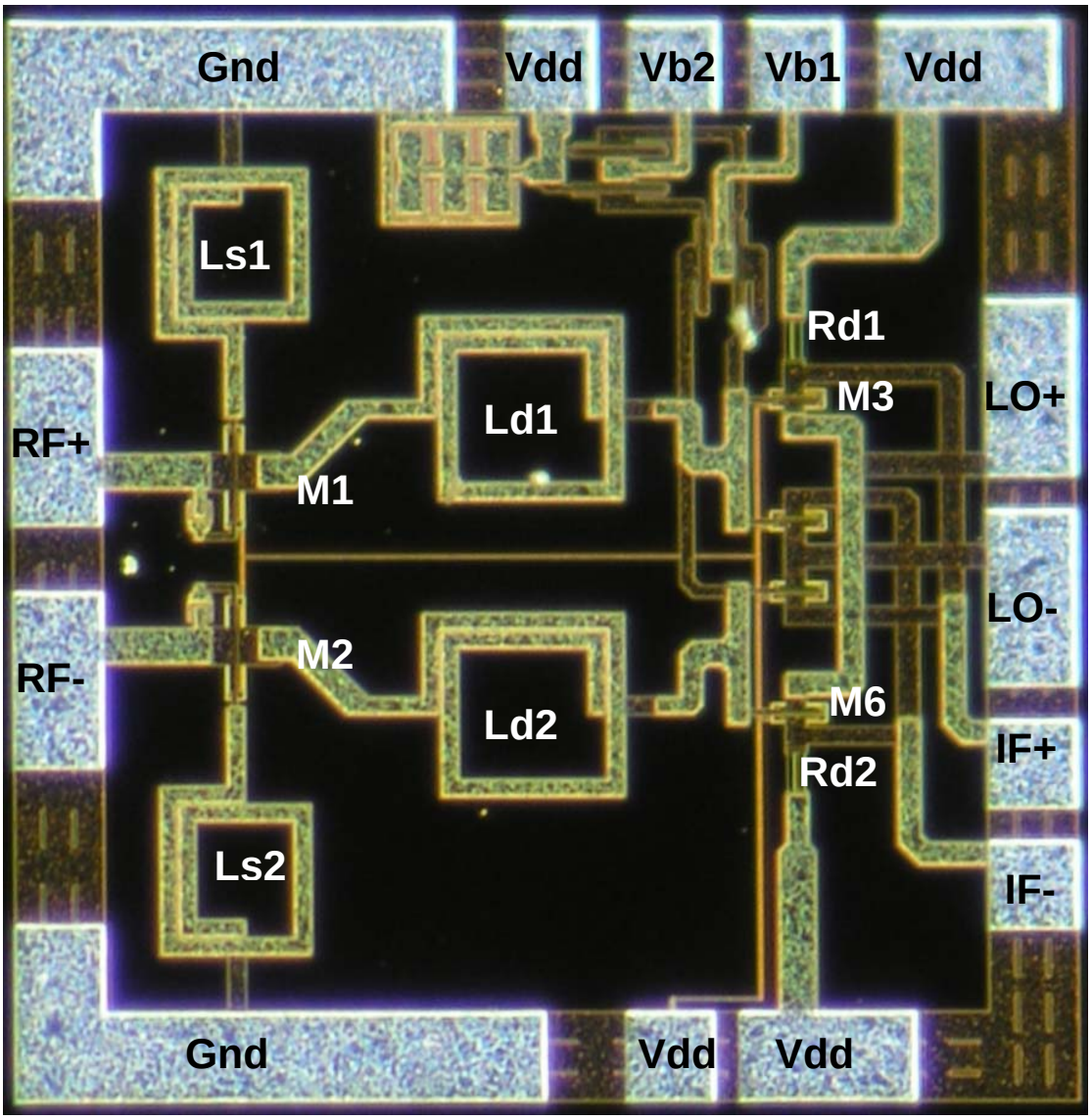


Fig. 4.13 Microphotograph of 3~8GHz Direct Conversion Broadband Mixer

4.3.2 Photograph of On Board Measurement

This 3~8Ghz broadband mixer is used by on board probing. The photograph of on board probing is shown as Fig. 4.14. The output stage uses an OP Amplifier (AD9631) as output buffer. The measurement setup is shown Fig. 4.15. The RF port and LO port that we design is differential, so we need to connect a balun to transfer signal. This balun type we choose is Anaren 30056 and 30057 as shown in Fig. 4.16. The measurement characteristic of Anaren 30056 balun is shown from Fig. 4.17 to Fig. 4.19. The Fig. 4.17 is the return loss of balun. The Fig. 4.18 is the gain difference curve. The Fig. 4.19 is the phase difference curve. The Anaren 30057's characteristic is shown from Fig. 4.20 to Fig. 4.22.

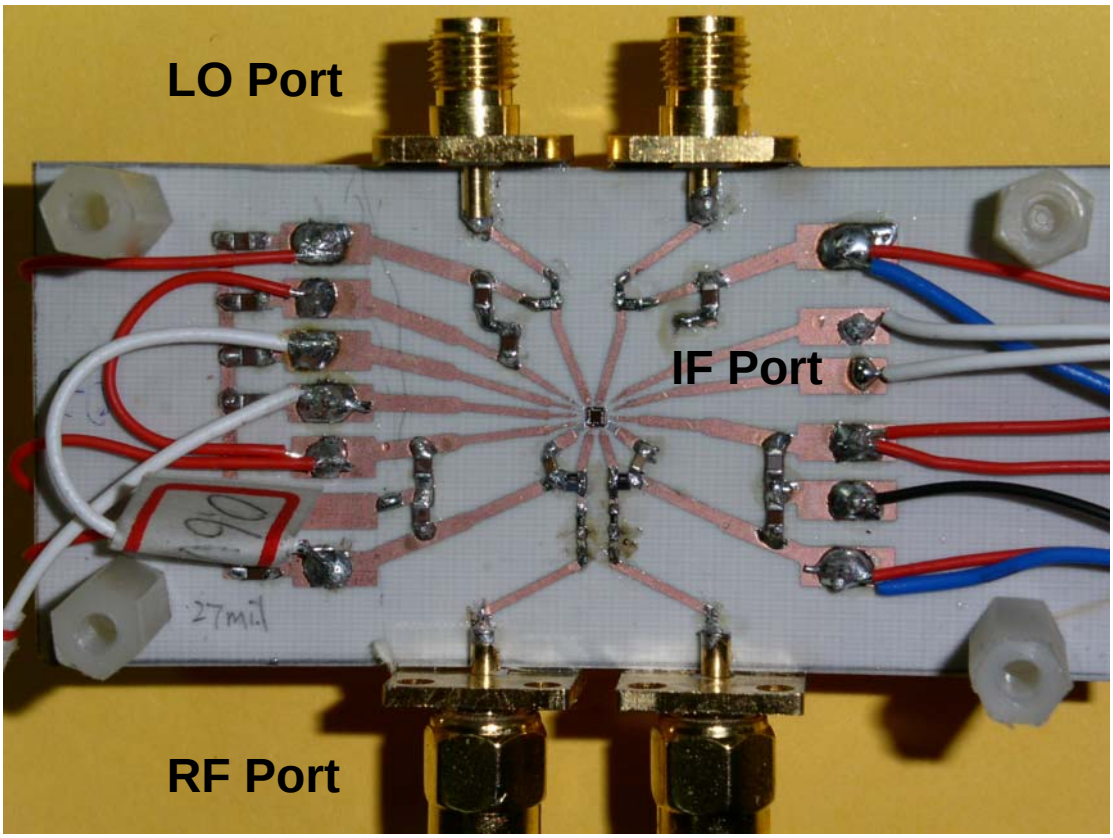


Fig. 4.14 Photograph of on board measurement of broadband mixer

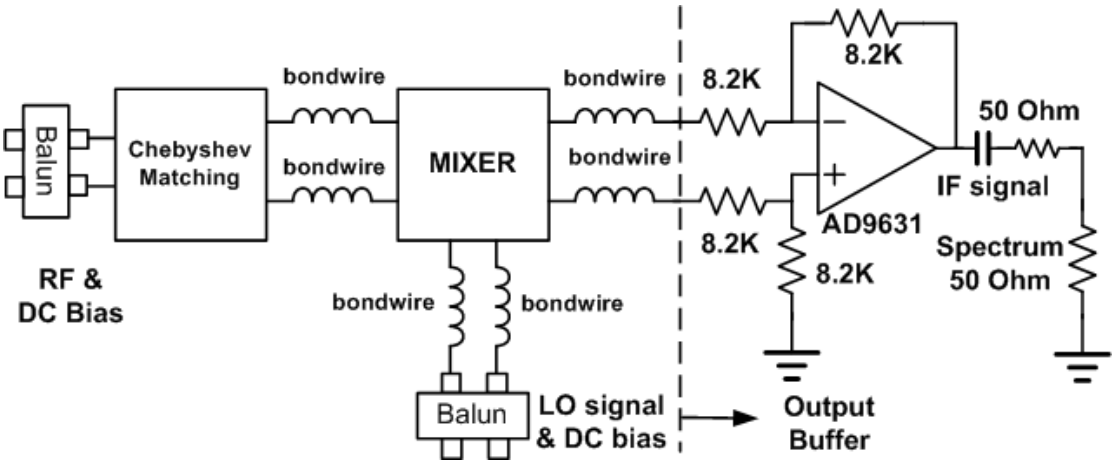


Fig. 4.15 Block diagram of measurement setup

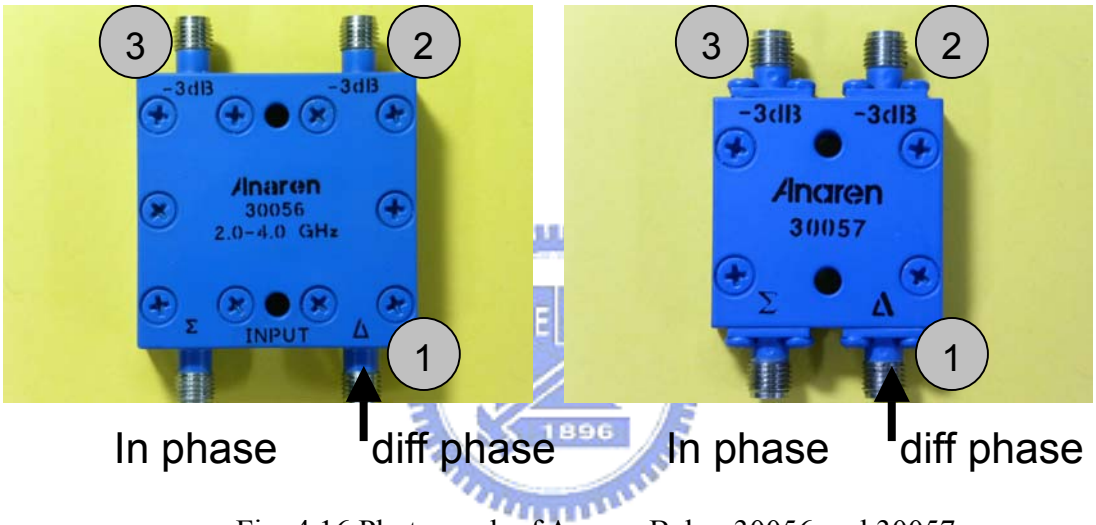


Fig. 4.16 Photograph of Anaren Balun 30056 and 30057

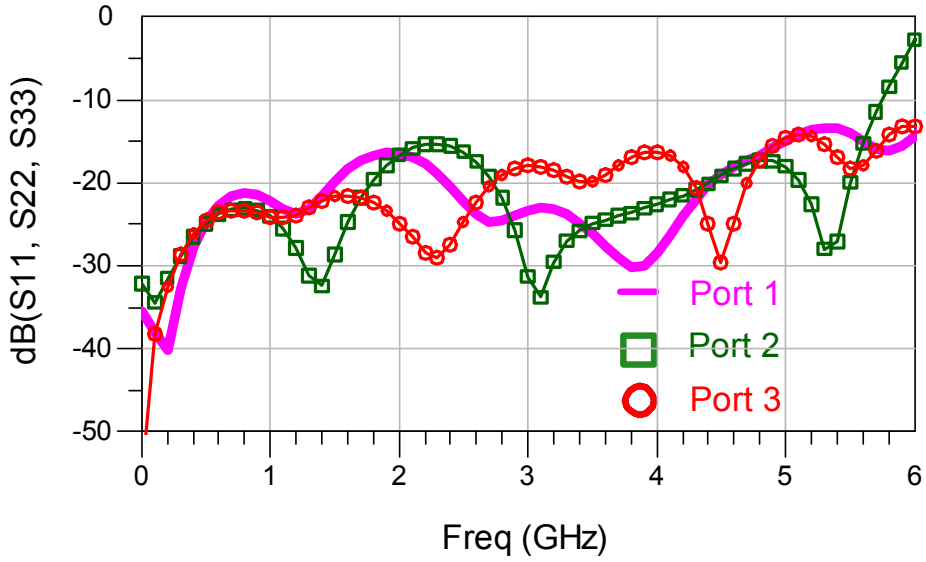


Fig. 4.17 Return loss of Anaren Balun 30056

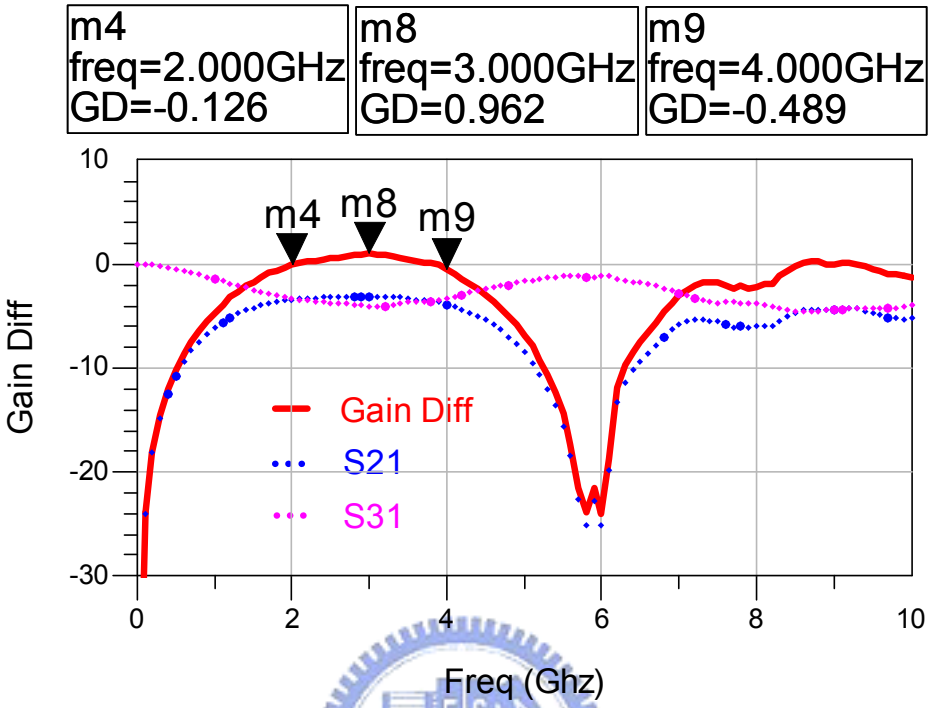


Fig. 4.18 Gain difference of Anaren Balun 30056

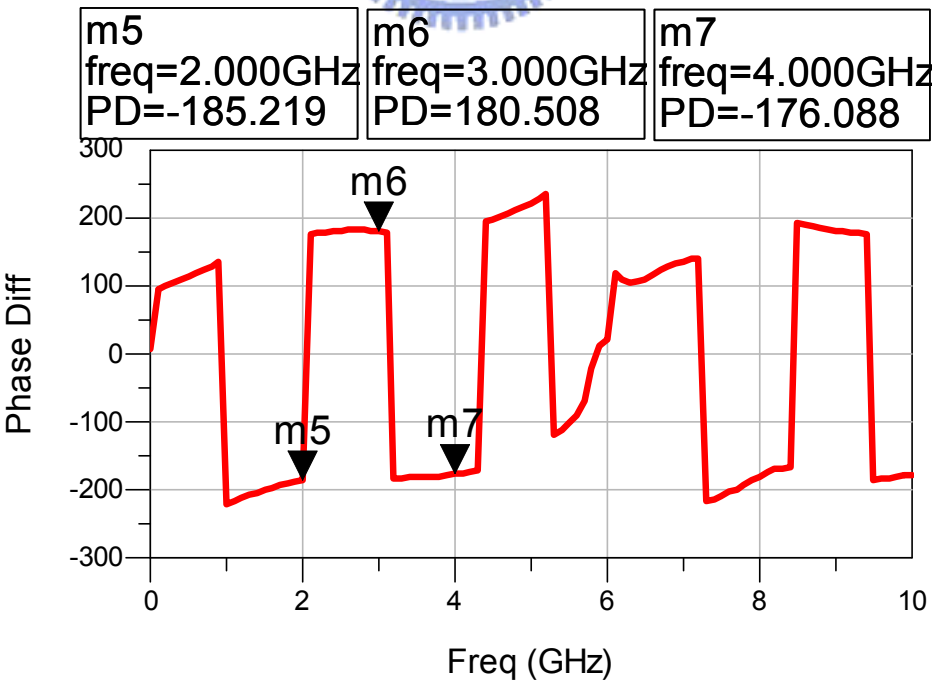


Fig. 4.19 Phase difference of Anaren Balun 30056

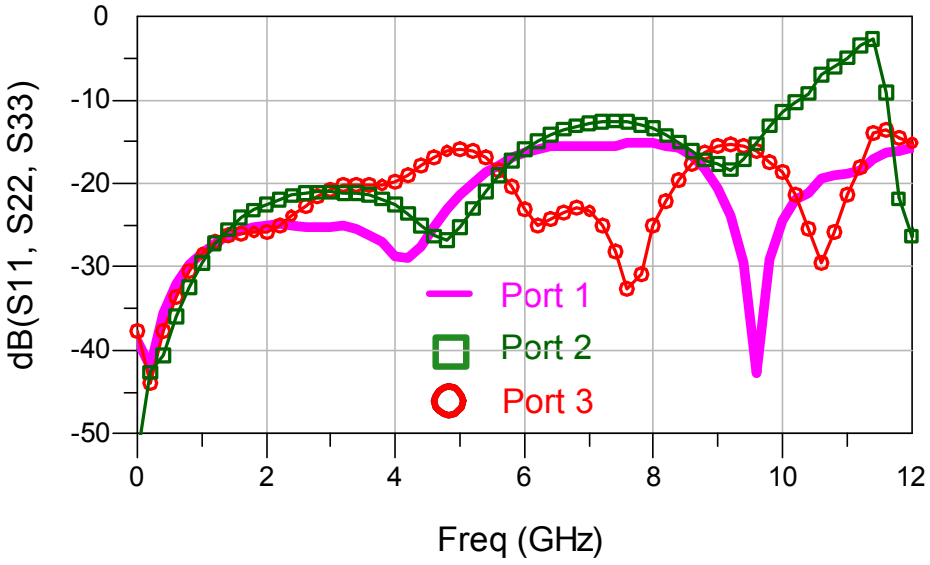


Fig. 4.20 Return loss of Anaren Balun 30057

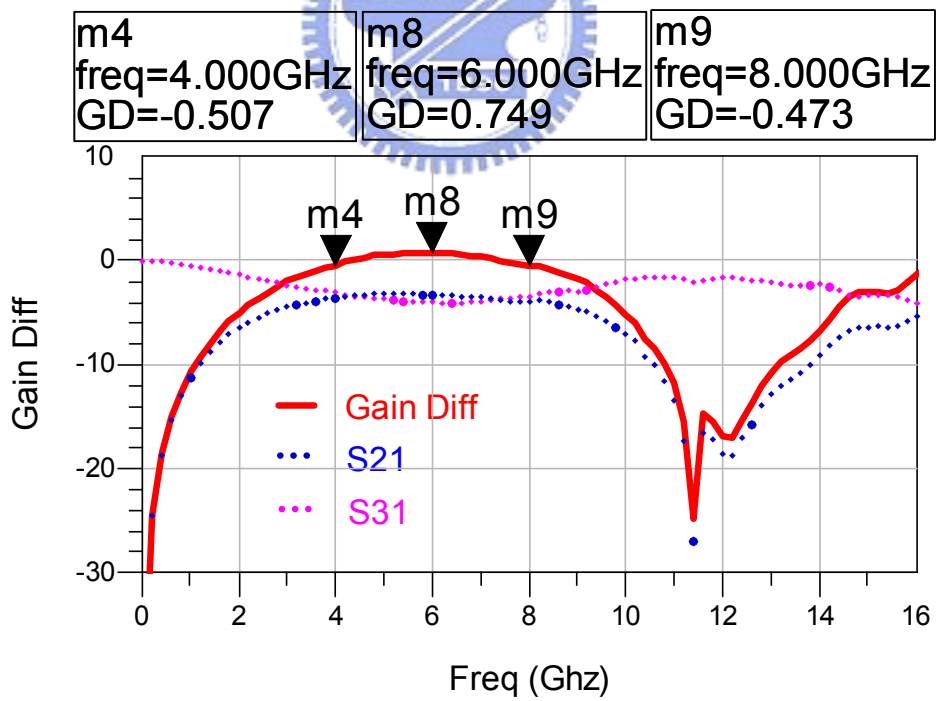


Fig. 4.21 Gain difference of Anaren Balun 30057

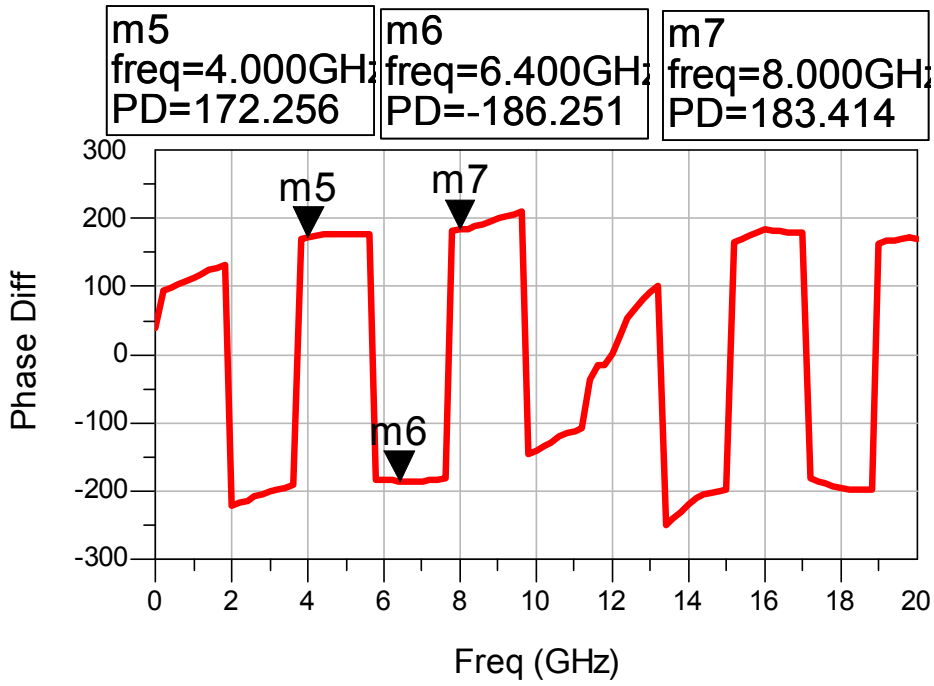


Fig. 4.22 Phase difference of Anaren Balun 30057

4.3.3 On Board PCB Layout Consideration

Because of our broadband mixer design is at high frequency range, we must carefully layout our PCB board. The PCB layout diagram is shown Fig. 4.23. First, the transmission line's distance between the series inductor and series capacitor (series resonance) can't be long. In this layout, we just reserve two components' pad. This is because long distance transmission line would influence our input broadband matching. Second, the parallel inductor and capacitor (parallel resonance) would be layout into the signal path, otherwise, it could causes the loading effect. Then, we put the bypass capacitor 0.1uF near the tank at the bias voltage Vg. It let the ac signal ground. The total length of transmission line between two series resonance can't exceed 5mm.

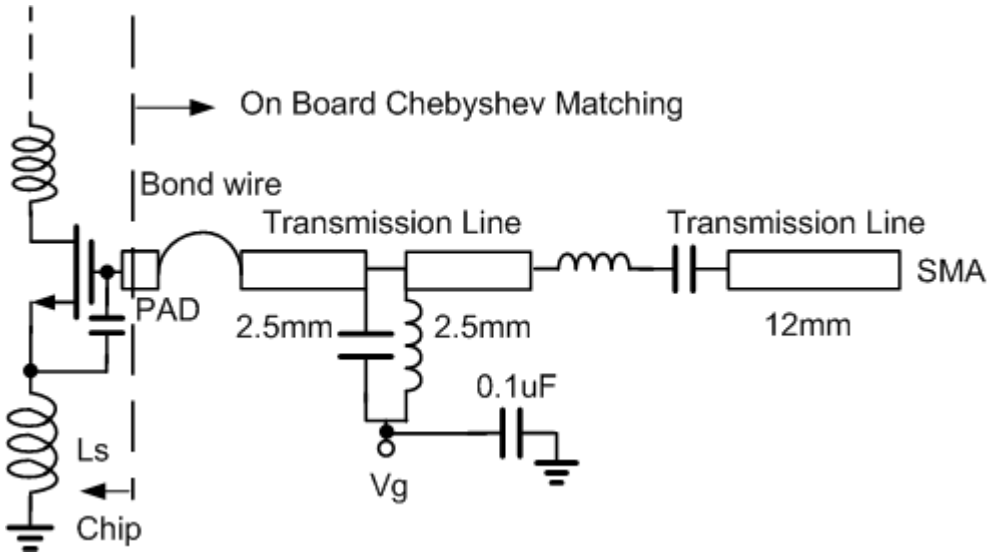


Fig. 4.23 On board PCB layout diagram

4.3.4 Measurement and Simulation Result

Measurement is used on-board probing. The measured S-parameter is plotted in Fig. 4.24, together with simulation results for comparison. The circuit plot is the measured result. The solid line is the simulation result. The triangle plot is the measured result with no balun connection. The low frequency is matched the simulation result, but high frequency is not. The cause is the transmission line performance is not good at high frequency. The board we use is RO4003C. The Fig. 4.28 is the measured result of various transmission line width of RO4003C. In these curves, we can observe the transmission line's return loss is poor in 3 ~ 6 GHz.

The measured maximum conversion gain is 7.4dB at 3-MHz IF band. The Fig. 4.25 is plotted the measured result, together with simulation result for comparison. The circle plot is the measured result. The solid plot is the simulation result. This mixer's bandwidth is about 3GHz from 2 to 5 GHz. The IIP3 measured result is shown in Fig. 4.26 and Fig. 4.27. The simulation noise figure is shown in Fig. 4.27. The minimum

noise figure is 7.1dB. The total power of this broadband mixer is 11.8mW with a power supply 1.6V. The table 4.3 is the comparison of simulation and measured result.

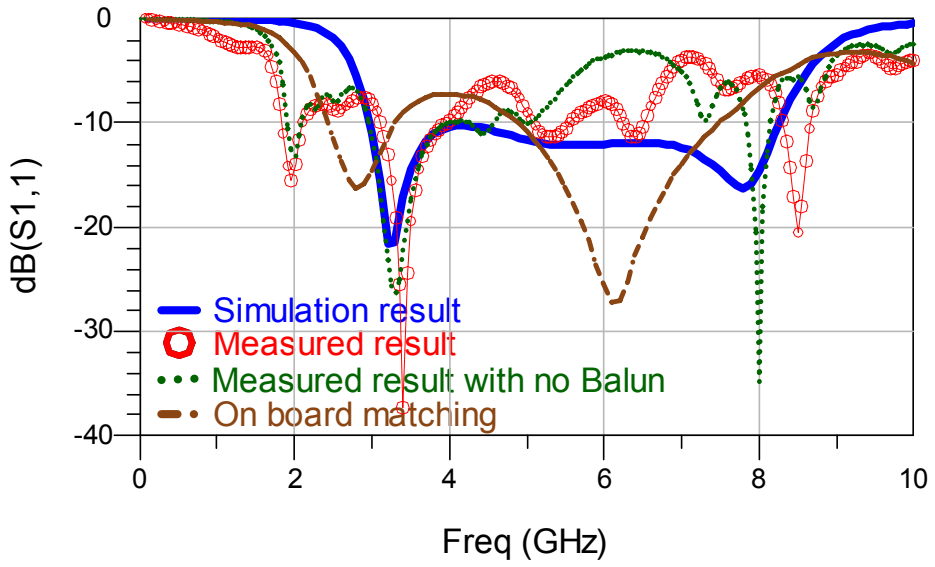


Fig. 4.24 S11 Simulation and measured result of broadband mixer

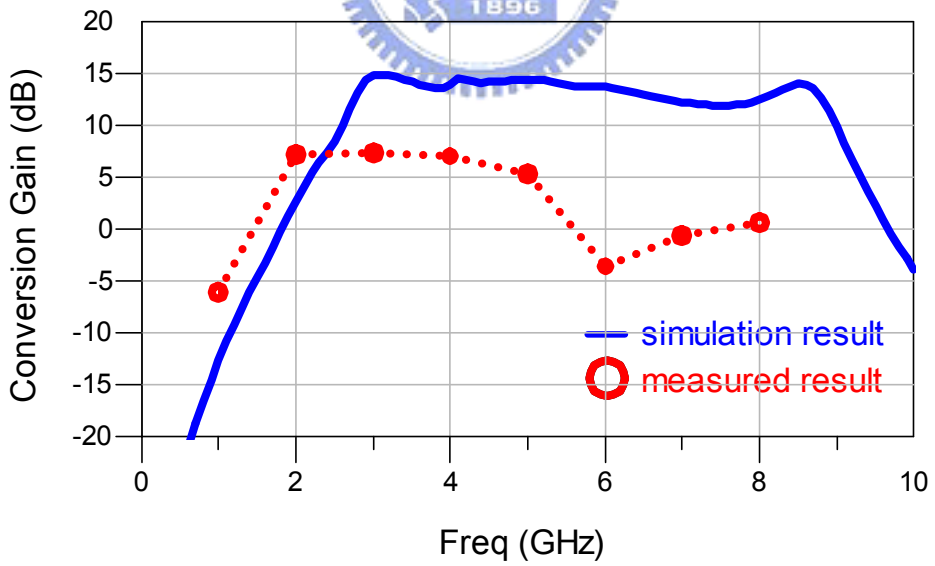


Fig. 4.25 Conversion gain simulation and measured result of broadband mixer

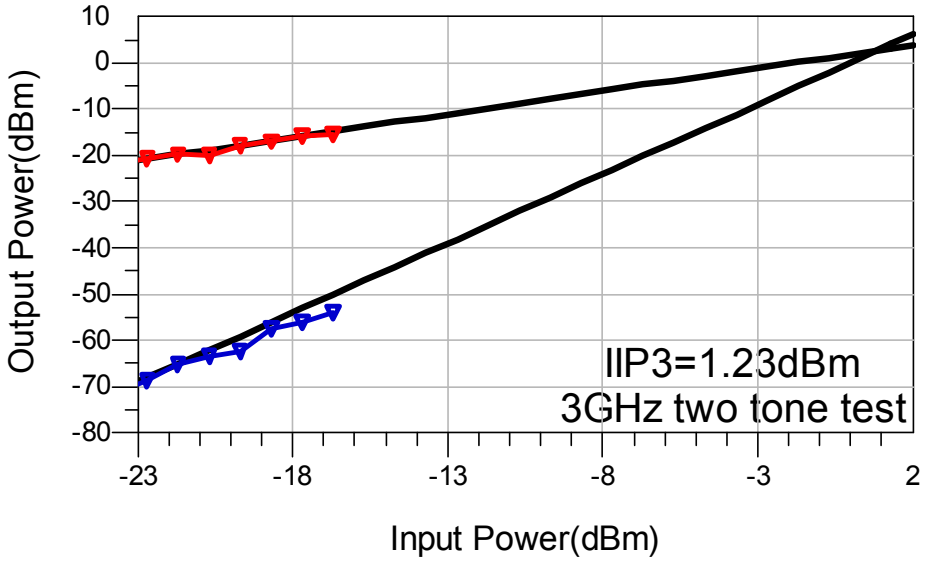


Fig. 4.26 Linearity measured result at 3GHz of 3~8GHz mixer

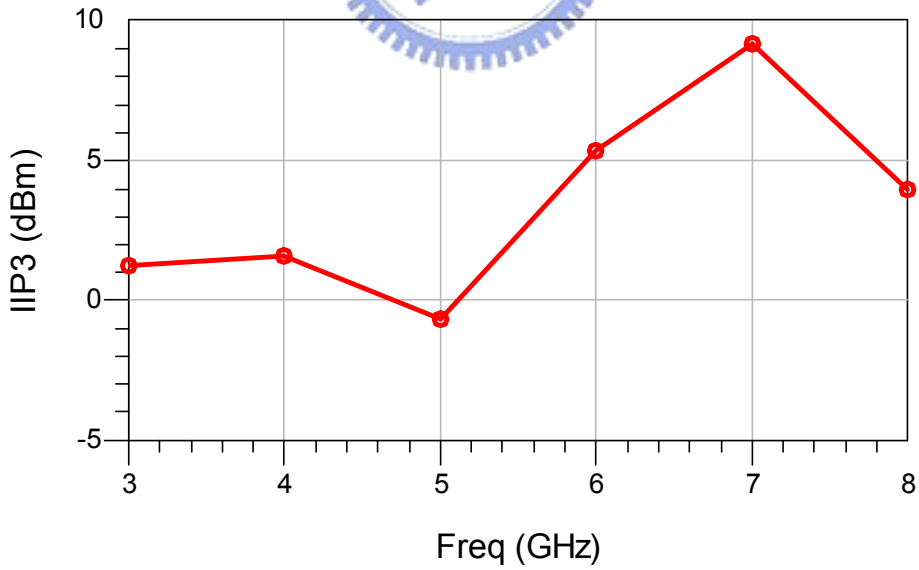


Fig. 4.27 Linearity measured result versus frequency of broadband mixer

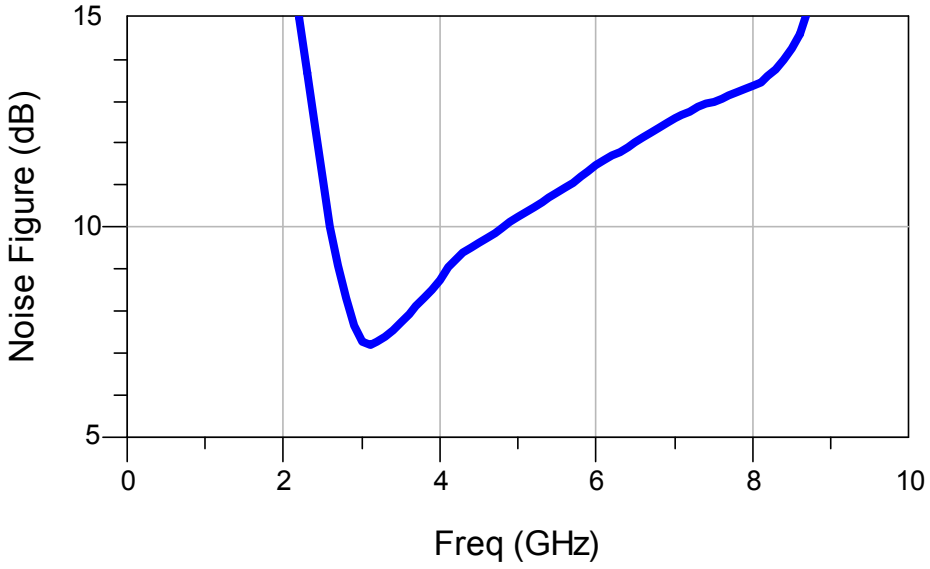


Fig. 4.28 Simulation result of Noise Figure of broadband mixer

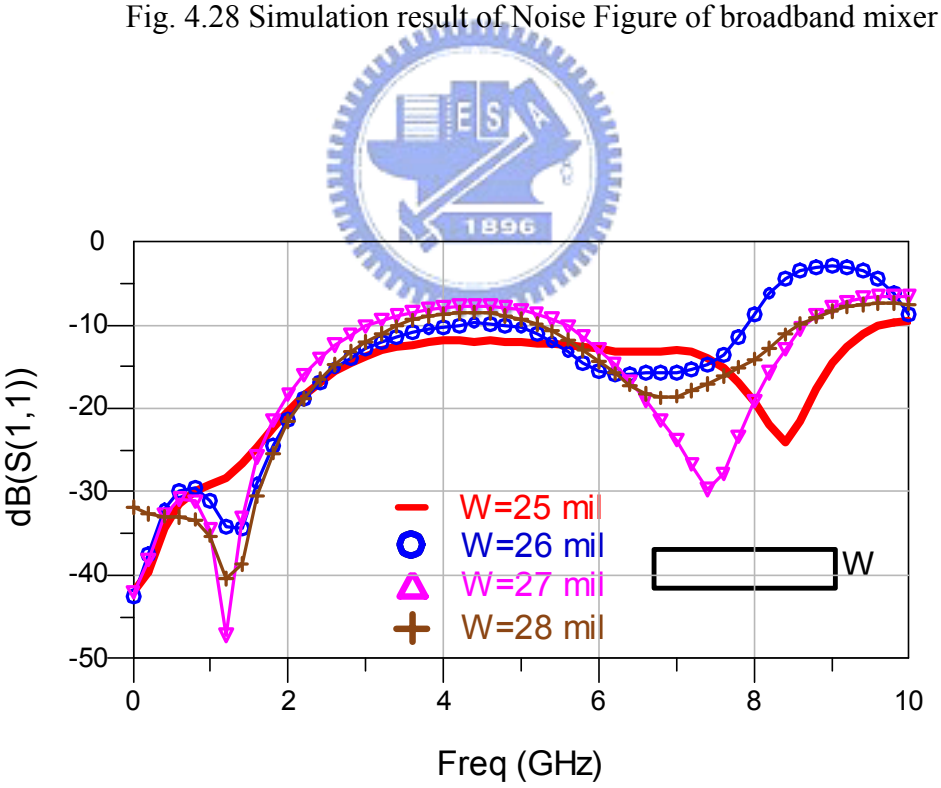


Fig. 4.29 Various width of transmission line of RO4003C

TABLE 4.3 Comparison of simulation and measured performance

	Simulation Result	Measured Result
Bandwidth	3 ~ 8 GHz	2 ~ 5 GHz
Power consumption	9.2 mW	11.8 mW
S11	< -10 dB	< -4 dB
Conversion Gain (max)	14.8 dB	7.4 dB
Noise Figure(min)	7.1 dB	N/A
IIP3 (average)	-4 dBm	+3.4 dBm

4.3.5 Discuss and Troubleshooting

According to previous section, we observe the worse return loss and conversion gain whose reason maybe the transmission line and bond-wire's variation. Then, we use ADS Momentum to simulation the transmission line of RO4003C's board effect. The Fig. 4.30 and 4.31 are the simulation results of considering the board effect and bond-wire variation. The cross plot is the bond-wire inductor which value is 1nH. The triangle plot is the bond-wire inductor which value is 0.5nH. The diamond plot is the bond-wire inductor which value is 1.5nH. In Fig. 4.30, the measured result is similar to the bond-wire inductor which value is 0.5nH. Relatively, in Fig. 4.31, the conversion gain is lower than simulation result but not similar to measured result. So, replaced the TSMC_v3 model to new TSMC_1.2A model and bond-wire inductor fix to 0.5nH, the simulation result is shown in Fig. 4.32 and Fig. 4.33. In Fig. 4.32, the S11 is alike between previous and current version of TSMC model but the conversion gain is serious degrade at high frequency. In Fig. 4.34, a capacitor (Cp=100fF and 400fF) is included between the gate and source of the transistor in TSMC_v3 model.

We find out a phenomenon in Fig. 4.33 and Fig. 4.34. The new TSMC model's conversion gain is similar to parasitic capacitor about 400fF included between the gate and source of the transistor in old model. The Fig 4.35 is shown the conversion gain with PMOS current source and ideal current source. The gain difference is around 1dB. So, we can conclude the old model is not accurate at high frequency. The noise figure with and without board simulation is shown in Fig. 4.36.

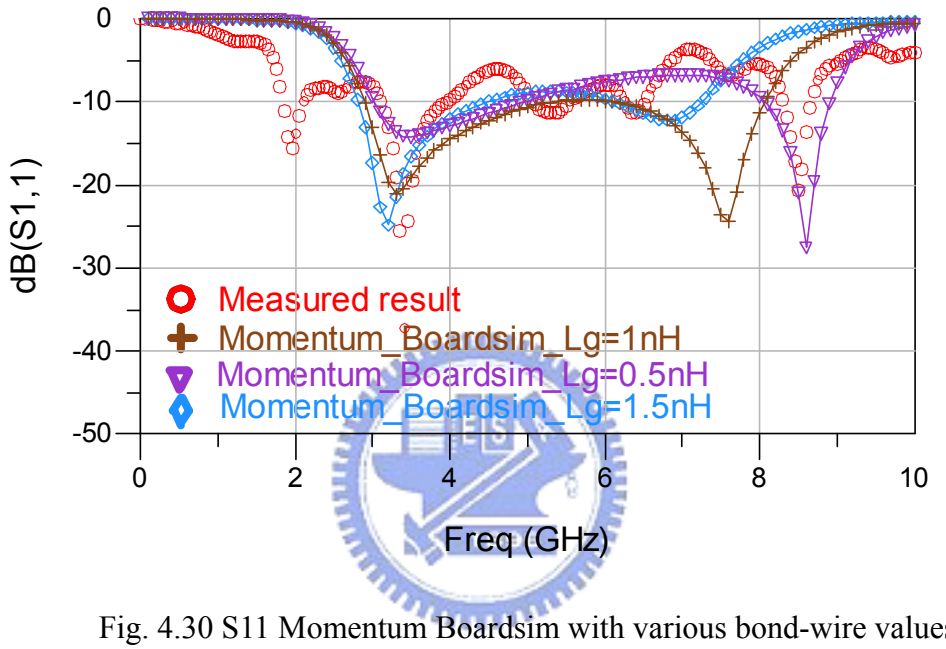


Fig. 4.30 S11 Momentum Boardsim with various bond-wire values

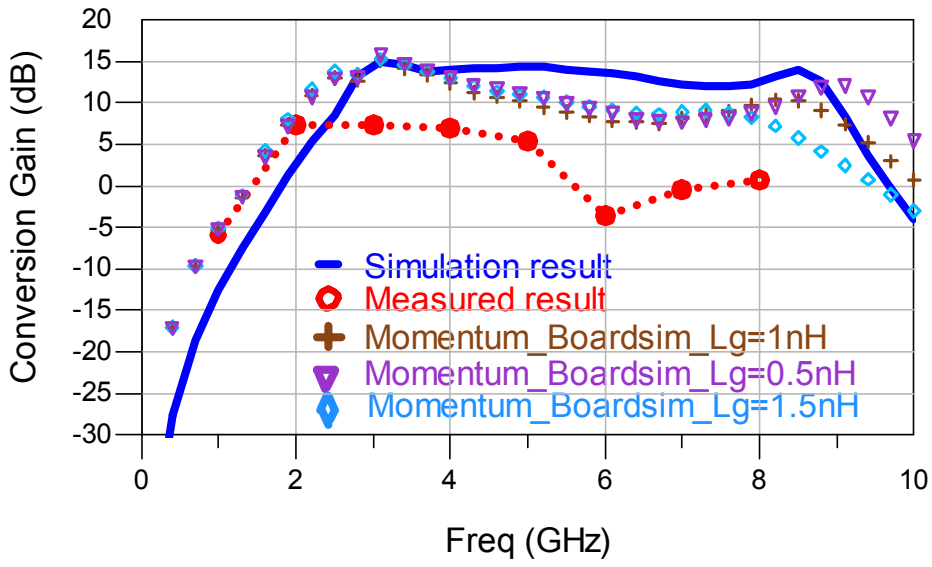


Fig. 4.31 Conversion gain Momentum Boardsim with various bond-wire values

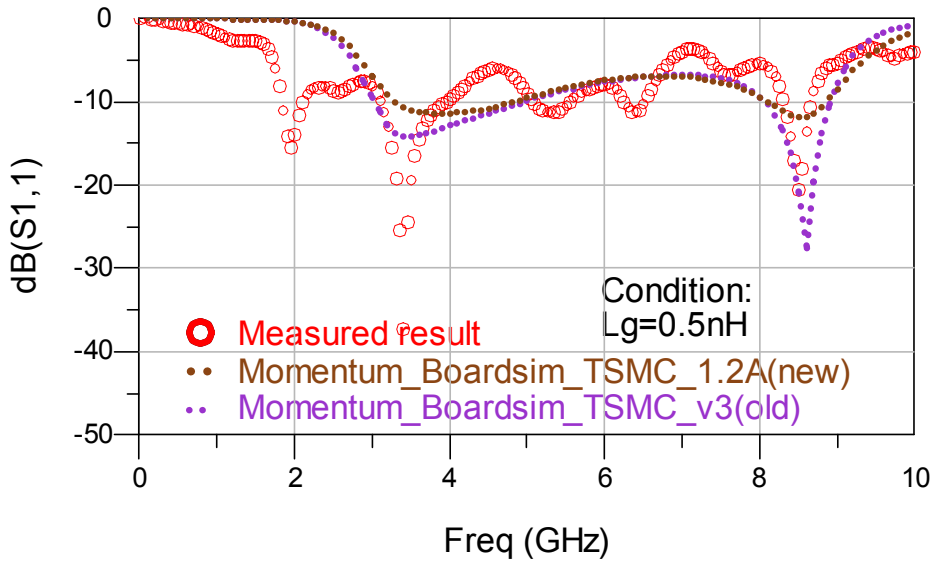


Fig. 4.32 S11 Momentum Boardsim with two TSMC models

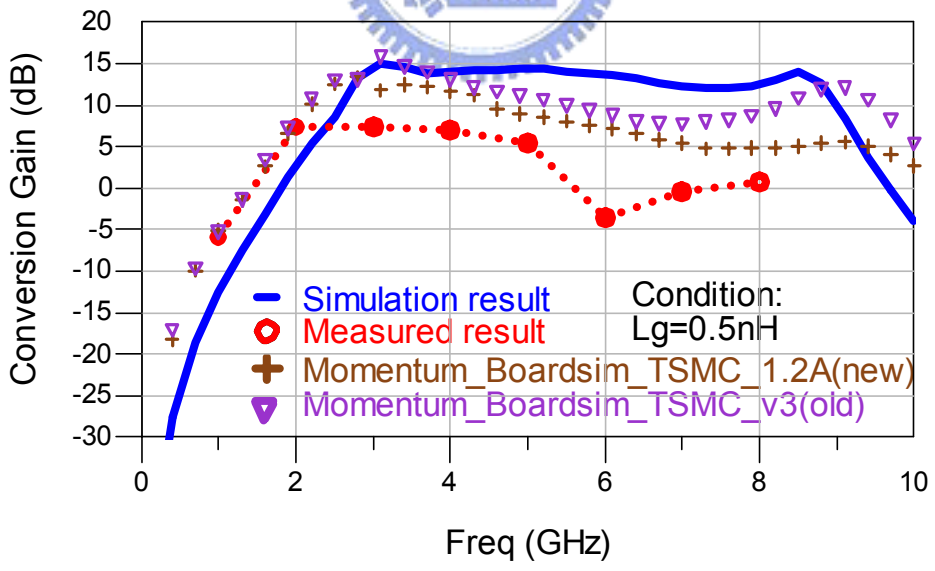


Fig. 4.33 Conversion Gain Momentum Boardsim with two TSMC models

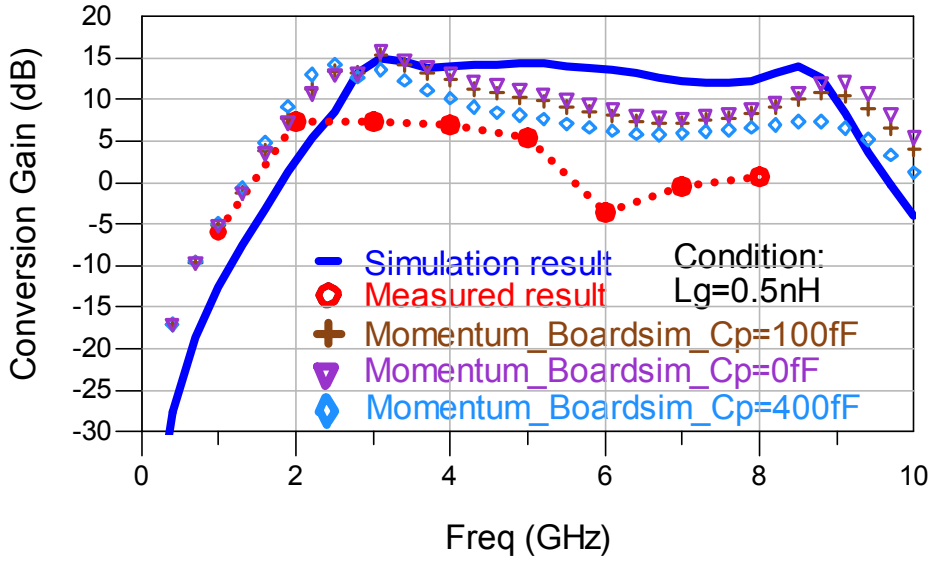


Fig. 4.34 Conversion Gain Momentum Boardsim with various parasitic capacitors

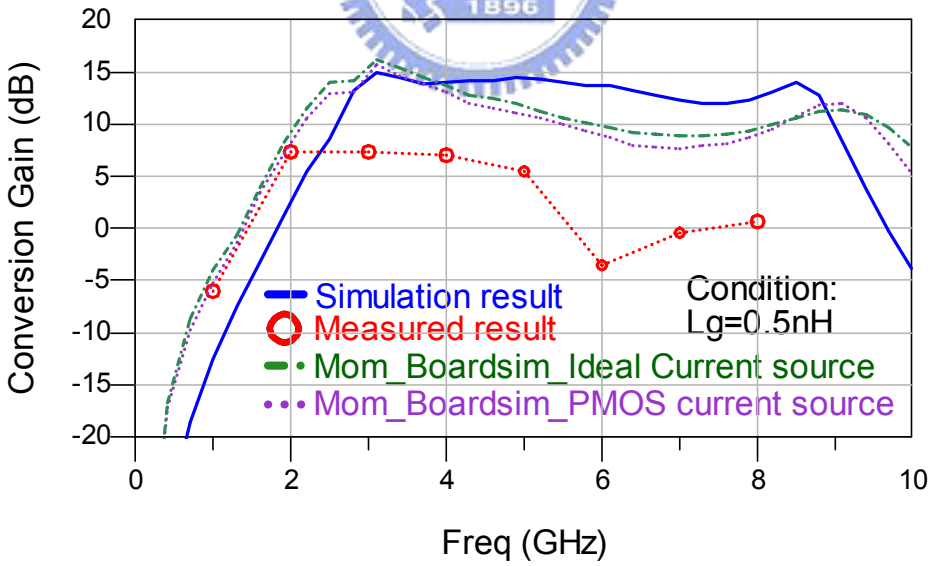


Fig. 4.35 Conversion Gain with and without PMOS current source

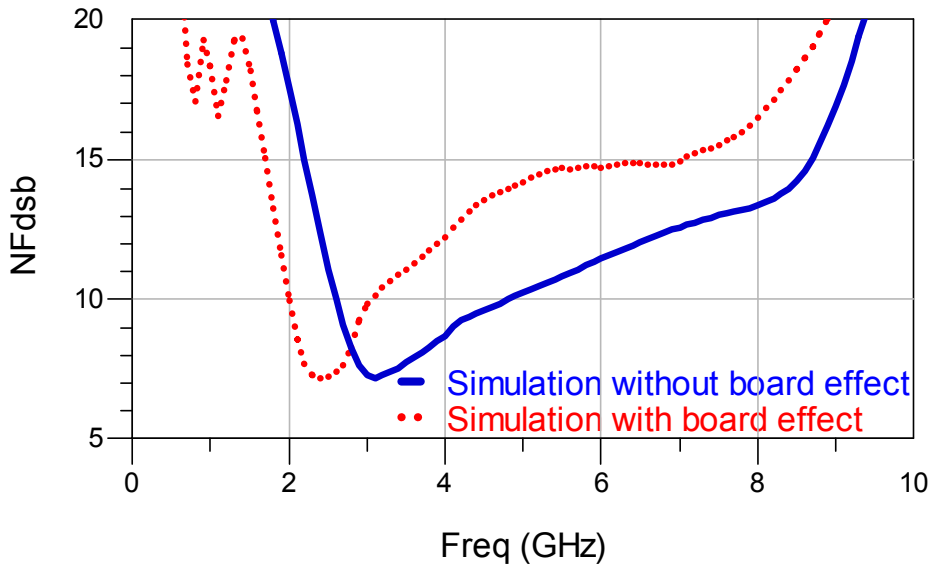


Fig. 4.36 Noise figure with and without Momentum Boardsim

4.4 Conclusion

In this work, we design a 3~8GHz direct conversion broadband mixer of the second stage of ultra wideband receiver front end. This circuit uses the chebyshev filter for input matching in order to reduce extra power consumption. The inductive peaking also uses in this circuit in order to compensation the high frequency transconductance. Due to the RO4003C board's transmission line effect and inaccuracy TSMC model, it makes the return loss poor and conversion gain will be degrade at high frequency as we discuss in section 4.3.5. The measured maximum conversion gain is 7.4dB at 3-MHz IF band. The average measured IIP3 is 3.4dB. The bandwidth is 3GHz from 2 to 5GHz. The input return loss is less than 4dB at 3 to 8GHz.

Chapter 5

Summary and Future Works

5.1 Summary

In the chapter 2, we will introduce the fundamentals of conventional low noise amplifiers and mixer. And some theoretical MOSFET noise model and noise theory are presented. LNA noise analysis also introduce in this chapter. Furthermore, many important design parameters and direct conversion receiver front end would be presented in this chapter.

In the chapter 3, we design an ultra wideband low noise amplifier for the receiver path of UWB system which is used the standard TSMC 0.18μm CMOS process. This circuit uses the feedback resistor to achieve the input, output broadband matching. But actually, the transistor's parasitic capacitor (Cgs) will serious degrade performance at high frequency. So, we add inductive degeneration matching method to enhance bandwidth. And between two stages, we add an inductor to compensation the high frequency transconductance. The measured result shows that S11, S22 and S12 parameters are similar to simulation result. The measured 3dB frequency range is from 0.1 to 6.6GHz. The measured maximum power gain is 6.2dB. The average IIP3 is -1.6dB. The noise figure minimum is 6.5dB.

In the chapter 4, we design a 3~8 GHz direct conversion broadband mixer of the second stage of ultra wideband receiver front end. This circuit uses the chebyshev filter for input broadband matching. Its advantage has easy to achieve high gain, broadband matching and doesn't consume extra power consumption but it needs large die size and accurate inductor model. The inductive peaking also uses in this circuit in

order to compensation the high frequency transconductance. Due to the board's transmission line effect, it makes the return loss poor at high frequency. The measured maximum conversion gain is 7.4dB at 3-MHz IF band. The average measured IIP3 is 3.4dB. The bandwidth is 3GHz form 2 to 5GHz. The input return loss is less than 4dB at 3 to 8GHz.

5.2 Future Works

The ultra-wideband LNA and mixer using frequency compensation can achieve flatness gain at UWB frequency band. But actually, the measured results present poor gain and noise figure in comparison to our simulation results. This could be the lower transconductance gain and inaccuracy model. It is presented in section 4.3.5. In next work, we can replace the TSMC accuracy model then the measured data will be close to the simulation result. Furthermore, we can merge LNA and Mixer with an broadband active balun.

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