國立交通大學

電機資訊學院 電子與光電學程

碩士論文

適用於 IEEE802.11a 接收機之差異積分調變

CMOS 頻率合成器設計

CMOS Delta-Sigma Frequency Synthesizer

Design for 802.11a Transceiver

研 究 生：李維傑

指導教授：溫瓌岸 教授

中 華 民 國 九 十 三 年 六 月

CMOS Delta-Sigma Frequency Synthesizer Design for 802.11a Transceiver

適用於 IEEE802.11a 接收機之差異積分調變 CMOS 頻率合成器設計

研 究 生：李維傑　　Student：Wei-Jie Lee

指導教授：溫瓌岸　　Advisor：Dr. Kuei-Ann Wen

國 立 交 通 大 學

電機資訊學院 電子與光電學程

碩 士 論 文

A Thesis

Submitted to Degree Program of Electrical Engineering Computer Science

College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronics and Electro-Optical Engineering

June 2004

Hsinchu, Taiwan, Republic of China

適用於 IEEE802.11a 接收機之差異積分調變 CMOS 頻率合成器設計

研 究 生：李維傑　　指導教授：溫瓌岸 教授

國立交通大學

電機資訊學院 電子與光電學程（研究所）碩士班

摘 要

本篇論文主旨在於設計可工作於 1.8V 直流電壓且以全積體化互補式金半導體 0.18-um 為製程，適用於 IEEE802.11a 接收機之差異積分調變分數型頻率合成器。此頻率合成器在 5.12GHz~5.376GHz 之頻率合成範圍內可以提供 16Hz 之頻率解析度，並且具有 6us 之快速鎖頻與低分數突波的特性。所設計的頻率合成器電路包含壓控震盪器(Voltage Controlled Oscillator)、相位/頻頻比較器(Phase-Frequency Detector)、多模數除頻器(multi-modulus divider)、電荷充放電濾波器(Charge-Pump filter)以及三階之差異積分調變器。

電壓控制振盪器由負電阻，螺旋型電感和 P/N 接面可變電容所組成，振盪器的輸出頻率可經由可變電容調整，經設計於控制電壓 1.8V 內，振盪器輸出頻率範圍可從 4.88GHz 到 5.436GHz。

在前置除頻器(prescaler)方面，為了能達到在高速操作並且低耗電的目標，故採用 pseudo-NMOS 搭配 TSPC 型式的除法器來完成。至於多模數除頻器，可除頻倍數從 16 到 31。整個除頻器經測量最高可工作在 5.9GHz。相位/頻率偵測器是比較外部輸入參考信號與內部除頻後信號的相位/頻率差，產生充電 UP 和放電 DN 的數位信號，此數位信號會透過電荷充放電轉成類比訊號，透過三階低通濾波器變成近似 dc 的類比連續信號以控制壓控震盪器。

除以上所述電路之外，此頻率合成器亦整合一個全數位管線化，以多級雜訊整形為架構之三階差異積分調變器，藉由此差異積分調變器的雜訊整形技術來降低由除數控制訊號所產生的相位雜訊，此差異積分調變器製作於可編程邏輯程式元件(FPGA)。經測量此差異積分調變器能達到 60dB 雜訊整形的能力，此外對調變器輸出取樣 2^{18} 筆資料平均後，其分數的產生精確度可達到 99.999%。

此頻率合成器使用是採用 UMC 0.18um CMOS 1P6M 製程並操作在 1.8V 的直流電壓。包含 pads 的晶片面積為 $2500\times2500\ um^2$，總功率消耗小於 49 毫瓦。

CMOS Delta-Sigma Frequency Synthesizer Design for 802.11a Transceiver

Student: Wei-Jie Lee **Advisor:Kuei-Ann Wen**

Degree Program of Electrical Engineering Computer Science

National Chiao-Tung University, Hsinchin, 2004

Abstract

This thesis presents the design of a fully integrated CMOS delta-sigma (ΔΣ) fractional-N frequency synthesizer with quadrature phase outputs intended for the local oscillator in WLAN 802.11a system using 0.18-um CMOS technology and 1.8-V single power supply. The proposed synthesizer can provide 16Hz frequency resolution within synthesized frequency range from 5.120GHz to 5.376GHz and meanwhile achieve fast locking time which is no more than 6us. Furthermore, its phase noise also improved by ΔΣ Fractional-N technology.

The designed ΔΣ fractional-N synthesizer is composed of a LC-tuned voltage-control oscillator (VCO), a divide-by-16 prescaler, a multi-modulus divider (MMD), a phase-frequency detector (PFD), a charge pump with third-order passive loop filter and third-order ΔΣ modulator.

The VCO is an LC-tuned negative-resistance oscillator. Its output frequency can be adjusted by P+/N-well varactor and can be varied from 4.88 to 5.436 GHz at 1.8-V power supply.

For low power and high speed consideration, the feedback high-speed divide-by-16 prescaler is composed of a pseudo-NMOS type divider and a True-Single-Phase-Clock (TSPC) based frequency divider. The multi-modulus divider has a frequency divide ratio, ranging from 16 to 31. The highest input-frequency of the frequency divider is 5.9GHz.

The charge pump receives the UP and DN signals from the PFD and output successive dc-like analog signal for the VCO through the third-order passive loop filter.

The third-order all-digital $\Delta\Sigma$ MASH modulator is implemented in FPGA which operates together with the multi-modulus divider that is be used in this frequency synthesizer. To achieve the desired operation frequency range (16 MHz or higher) while providing low-power dissipation and small area. The pipelining technique was utilized in the design. The third-order MASH modulator measurement results confirm the 60 dB per decade increase in the spectrum, validating the third-order noise shaping. Furthermore, for 2^{18} samples of modulator output the fraction was represented to an accuracy of 99.999%. The pipelining technique was utilized in the design

The $\Delta\Sigma$ fractional-N frequency synthesizer has been fabricated with UMC 0.18-um CMOS (1P6M) 1.8V technology except for the $\Delta\Sigma$ modulator. The total chip area is 2500×2500 um^2. The total power consumption is 49mW from a single 1.8V supply.

誌謝

能順利完成這篇論文，首先要感謝我的指導教授溫瓌岸博士。在求學態度及研究問題的方法上對我的教導，使我獲益良多，並且提供豐富的研究資源來幫助我的研究，那麼這篇論文便不可能會如此順利的完成。此外，感謝高曜煌教授、詹益仁教授與張志揚撥冗擔任我的口試委員，耐心聆聽與指教，並提供保貴意見，使得本論文得以更加完整。

感謝實驗室溫文燊學長、陳哲生學長、周美芬學長等人提供我在生活的幫助以及學業上指導，讓我受益良多。感謝實驗室的同學嘉富、聯興、木山、永正、敬文、佳欣，學弟建銘、兆鈞、格輝、相霖、富昌、皓名的互相砥礪，讓研究生涯充滿歡樂與回憶。

感謝的是聯華電子公司、智森科技公司、矽品精密工業所有幫助過我順利生產晶片的人。若不是有這麼多人的幫助，這篇論文不可能如期完成，在此我誠摯的對這些幫助過我的人表達我的謝意。

最後我要感謝我的家人，他們無怨無悔的付出，使我求學過程中無後顧之憂，僅以此論文與我的家人及好友分享我的收穫與喜悅，願他們永遠平安，快樂。

誌于 2004

李維傑

Table of Contents

List of Figures

List of Tables


E
S
A
1896

Chapter 1 Introduction

1.1 Motivation

With the development of wireless communication, the demand for higher data rate of transmission increasing. For all the wireless local area network (WLAN) applications, there are several communication standards produced, such as Bluetooth, GSM, 802.1x etc. Wireless LANs generally need to provide data rates in excess of 10Mb/s to compete with existing wired LANs. For the IEEE802.11b standard, it provides data rates of up to 11Mb/s in the 2.4GHz ISM band. In the US new spectrum, called the unlicensed nation information infrastructure (U-NII) band, has been allocated for high data rate wireless communications. The U-NII band consists of a 300MHz span from 5.15GHz to 5.35GHz and 5.725GHz to 5.825GHz. The IEEE 802.11a standard is one of the technology targets on developing of this band. This standard is based on orthogonal frequency division multiplexing (OFDM) and can provide the maximum data rate of 54Mb/s, minimum data rate 6Mb/s and minimum sensitivity –82dBm. Besides, the carrier frequencies are from 5180MHz to 5320MHz with spacing 20MHz [1], [2].

The rapid growth of mobile communication systems and wireless LANs (local area network) have led to an increasing demand of low-cost high-performance and compact communication integrated circuits. Integration of the analog RF part of wireless transceivers in cheap digital CMOS technology seems a viable solution. A major challenge in the design of future CMOS single-chip transceivers is the frequency synthesizer. The most popular synthesizer type is the Phase Locked Loop (PLL). The past years fractional-N, a PLL technology, allows improvement of phase

noise and switching speed. The fractional-N synthesis technique enables fine frequency resolution with a high reference frequency by employing fractional division. The fractional division of the synthesizer is mainly achieved by interpolation between two integer modulus. However, the fractional spurs that come from the sawtooth phase error of the phase detector degrade the output spectrum. The delta-sigma ($\Delta\Sigma$) modulator is used to suppress the fractional spurs and push the quantization noise to out-of-band such that it can be filtered by the intrinsic low-passed characteristic of PLL.

In this thesis, a fully integrated CMOS delta-sigma ($\Delta\Sigma$) fractional-N frequency synthesizer with quadrature phase outputs intended for the local oscillator in WLAN 802.11a system will be proposed. This system is used for the direct-conversion architecture. For the frequency synthesizer, the requirement of various center frequencies provision, high accuracy of the output of synthesizer, low noise, quadrate phases for I,Q paths and the stability issues makes the design goal of the RF frequency synthesizer. In this thesis, the 5.12~5.436GHz frequency synthesizer was realized in UMC 0.18-um CMOS one-poly six-metal (1P6M) process and runs off of a 1.8-V supply. The frequency synthesizer is designed for specifications of the WLAN 802.11a standard, generates the output frequency from 5.12 to 5.436GHz with quadrature phases.

1.2 Thesis Organization

As described, the design goals of frequency synthesizer are: accuracy of the output frequency, low noise, the prompt settling time, sufficient output power level and

lower power consumption. For solving these problems, the later chapters will have the discussion about these issues and the optimizations for the design of the frequency synthesizer.

Chapter2 introduces the specifications of frequency synthesizer for 802.11a transceiver, including the frequency tuning range and locking time, frequency accuracy, phase noise, output power, quadrate phase, sideband spurious tones, stability, and power consumption.

Chapter3 introduces the basic component of PLL, including basic concept of PLL, operation principles of PLL. The architecture of frequency synthesizer will be discussed and there will have some analysis about their advantages and disadvantages for wireless communications.

Chapter4 will have the discussions about all the circuits in the frequency synthesizer such as voltage controlled oscillator (VCO), programmable frequency divider, phase detector, charge pump and loop filter. And each circuit has the simulation results and some considerations in practice. The overall frequency synthesizer based on real MOS design will be discussed also. Finally, layout, ESD protection, package, PCB for the circuit implementation will be discussed.

Chapter5 provides the behavior simulations and circuit specifications about the overall frequency synthesizer.

Chapter6 is the measurement results, including the VCO output power, frequency tuning range, phase noise, locking time and third order MASH $\Delta\Sigma$ modulator performance.

Chapter7 will come out the conclusions and the suggestions of future works.

Chapter 2 Frequency Synthesizer For IEEE 802.11a

2.1 Role of Frequency Synthesizer for IEEE 802.11a Transceiver

IEEE 802.11a is a popular wireless standard, and it has many specifications, of course, including the RF part, the transmitter mask and the ability of rejection for adjacent channel will define linearity and the sharp of signal. The receiver SNR will be required for demodulated in baseband part and the system sensitivity for all kinds of the date rate, and sensitivity and transmitter mask will define the dynamic range. Therefore, there are some specifications for RF transmitter and RF receiver.

A generic wireless transceiver is shown in Fig. 2.1. The role of a frequency synthesizer is to provide the local oscillation frequency for transmitting and receiving channel signals in IEEE 802.11a Transceiver.

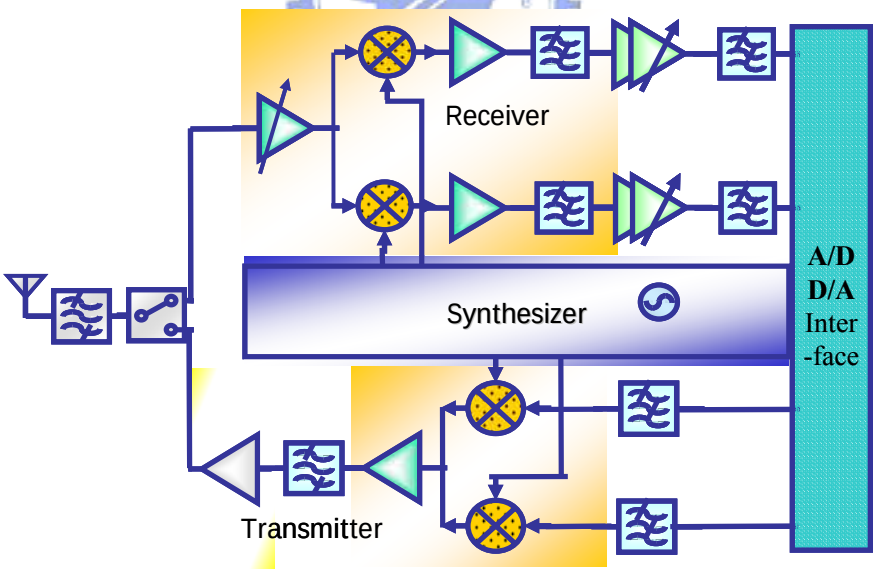


Fig. 2.1. 802.11a wireless LAN direct-conversion architecture.

For the frequency synthesizer, only the locking time, center frequencies and

frequency accuracy have the specification to design. However, for typical wireless system, lower phase noise and lower sideband spurious tones will make the design of RF transmitter and RF receiver more easily because the transmitter mask and adjacent channel rejection are hard to design if large phase noise and large sideband spurious tones. In addition, output power is important issue because of the too small power of the frequency synthesizer will have less ability to drive the switch of the RF mixer and the actions for up-conversion and down-conversion will fail. In typical wireless system, the in-phase and quadrate paths are used for good modulation and demodulation, thus four phases synthesizer at least is required. Finally, the accuracy of the frequency synthesizer is another issue, for IEEE 802.11a standard, the carrier frequency offset is ± 20 ppm. Thus, the typical specifications for the frequency synthesizer are tuning range and locking time, frequency accuracy, phase noise, output power, quadrate phase, sideband spurious tones, stability, and power consumption.

2.2 Specification of Frequency Synthesizer

Locking Time

The locking time for the IEEE 802.11a standard is 224us, this means the carrier switching time is less than 224us.

Phase Noise

The phase noise is the important performance for the frequency synthesizer. Bad phase noise will block the desire signal due to the adjacent channel, thus, the good control for the phase noise is important. Fortunately, the phase-locked loop has the

good performance on phase noise.

Considering the system specification as the Fig. 2.2, for the each date rate, the each reference has given, for the worse case, minimum sensitivity is –82 dBm when the date rate is 6MHz per second, and thus considering the adjacent channel, the calculation about the phase noise is:

$$L\{\omega_m\} = P_{dseire} - SNR_{\min} - 10\log(20MHz) - P_{adjacent}$$
$$= -99dBc/Hz@20\text{MHz offset frequency}$$

For the non-adjacent channel, the phase noise can be calculated as –118dBc/Hz at 40MHz offset frequency. However, for the typical case, the phase noise of the desire frequency falls in VCO $1/f^2$ region. Thus if the phase noise is –99dBc/Hz at offset frequency 20MHz, then the phase noise at the offset frequency 40MHz is –99-10log2^2=-105dBc/Hz. Therefore, the phase noise should be defined as –118dBc/Hz at the offset frequency 40MHz or -112dBc/Hz at the offset frequency 20MHz, thus the specification about phase noise has been set.

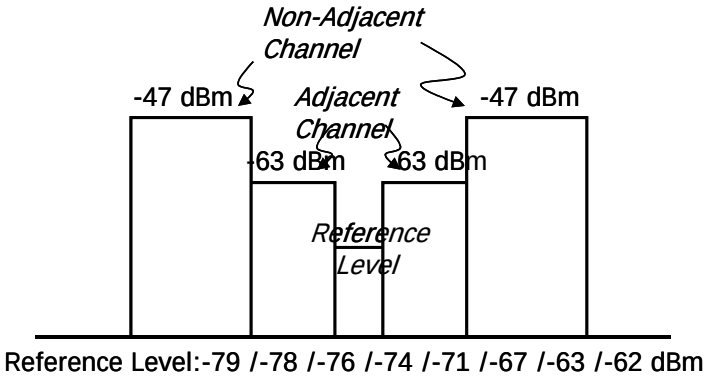


Fig. 2.2. The spectrum of the system specification.

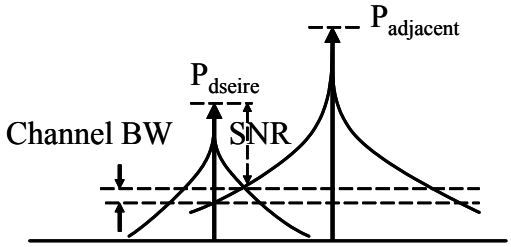


Fig. 2.3. Out-band calculation of the phase noise.

The noise discussed above is from out-band calculation, however, the in-band calculation should be taken in consideration, for non-ideal frequency synthesizer (with phase noise), the received signal will be convoluted with non-ideal LO signal and then the down converted signal will get worse SNR than ideal LO signal. Therefore, for consideration of in-band phase noise, the specification about phase noise is based on base-band modulation, for IEEE 802.11a standard, the signal modulation is OFDM and the required phase noise is about -90dBc/Hz at offset frequency 100kHz (From BB simulation). For this specification, is strict than out-band specification. Therefore, we will take in-band phase noise as specification.

Additional, I, Q phase mismatch should less than 5^0 for correct demodulation.

Chapter 3 Review of Frequency Synthesizer Architecture

3.1 Basic PLL Operation

A basic PLL consists of a reference oscillator, phase/frequency detector, charge pump, loop filter, voltage controlled oscillator(VCO) and divider. The reference oscillator is obtained often from a quartz, with a very accurate frequency. With a constant divisor of N, the loop forces the VCO frequency to be exactly N times the reference frequency. The phase/frequency detector and charge pump deliver either positive or negative charge pulses depending on whether the reference signal phase leads or lags the divided VCO signal phase. These charge pulses are integrated by the loop filter to generate a tuning voltage to move the VCO frequency up or down until the phases are synchronized.

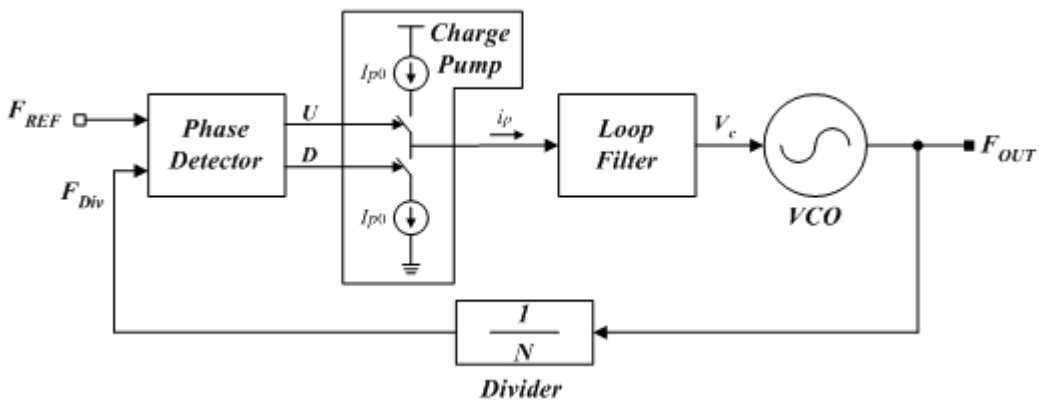


Fig. 3.1. The block diagram of the synthesizer.

PLLs are used as frequency synthesizers in many applications where it is necessary to generate a precise signal with low spurs and good phase noise. A VCO's frequency may be changed by varying either the reference frequency or the divisor.

But the reference is often a stable, fixed oscillator so it is the divisor that is varied in integer steps, such that *Fout* = *N* * *Fref*.

One limitation with this type of PLL is that the VCO frequency cannot be varied in steps any smaller than that of the reference. With a little more circuitry, though, a 1/M divider could be placed between the reference and the phase/frequency detector, in which case the VCO output would be determined by the ratio of the integer divider, such that *Fout* = (*N*/*M*)**Fref*.

Even when the loop is locked the charge pump still outputs small charge pulses, caused by mismatches in the PLL's positive and negative charge pumps and other factors such as non-ideal phase/frequency detection. These pulses create sidebands, or spurs, in the VCO output spectrum at offset frequencies equal to the reference.

Dealing with these spurs requires design tradeoffs for fine frequency resolution we want a low reference frequency, but this will cause spurs to be generated closer to Fout and a tighter loop filter bandwidth is required to filter them. PLLs with tighter loop bandwidths have longer transient settling times (from one frequency to another.) Also, the narrower the loop bandwidth the less suppression there is of the VCO's phase noise outside the loop bandwidth.

3.2 Linear Model of PLL

Although the PLL is nonlinear since the phase detector is nonlinear, it can accurately be modeled as a linear device when the loop is in lock. When the loop is locked, it is assumed that the phase detector output voltage is proportional to the difference in phase between its inputs; that is,

$$Vd = K_P(\theta_i - \theta_{div}) \tag{3-1}$$

where θ_i and θ_{div} are the phases of the input and divider output signals,

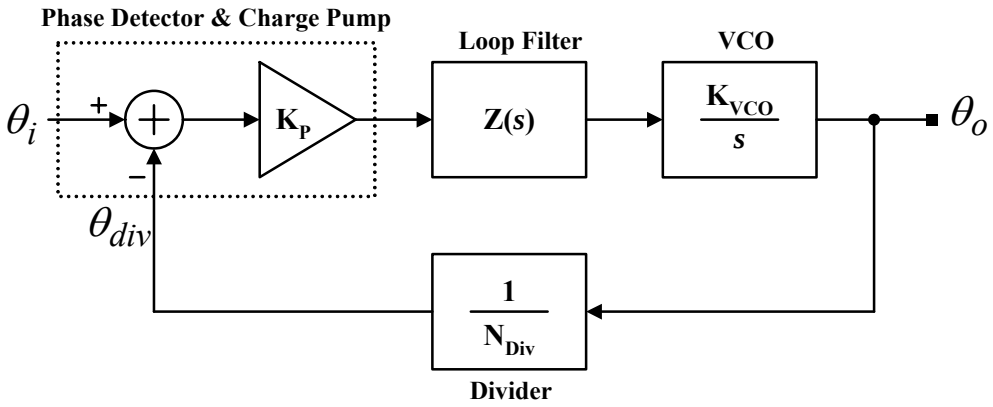


Fig. 3.2. Linear model of a PLL synthesizer.

Respectively. K_P is the phase detector gain factor and has the dimensions of voltage per radian. It will also be assured that the VCO can be modeled as a linear device whose output frequency deviates from its free-running frequency by an increment of frequency,

$$\Delta\omega = K_{VCO}V_C \tag{3-2}$$

where V_C is the voltage at the output of the low-pass filter and K_{VCO} is the VCO gain factor, with the dimensions of rad/s per volt. Since frequency is the time derivative of phase, the VCO operation can be described as

$$\Delta\omega = \frac{d\theta_o}{dt} = K_{VCO}V_C \tag{3-3}$$

With these assumptions, the PLL can be represented by the linear model shown in Fig. 3.2 [8]. $Z(s)$ is the transfer function of the low-pass filter. The linear transfer function relating $\theta_o(s)$ and θ_i is

$$H(s) = \frac{\theta_o}{\theta_i} = \frac{K_P Z(s) K_{VCO} / N}{s + K_p Z(s) K_{VCO} / N} \tag{3-4}$$

If no low-pass filter is used, the transfer function is

$$H(s) = \frac{\theta_o}{\theta_i} = \frac{K_P K_{VCO} / N}{s + K_p K_{VCO} / N} = \frac{K}{s + K}, \qquad K = \frac{K_P K_{VCO}}{N} \tag{3-5}$$

which is equivalent to the transfer function of a simple low-pass filter with unity DC gain and bandwidth equal to *K*.

3.3 PLL Noise Analysis

The job of any frequency synthesizer is to generate a spectrally pure output signal. An ideal periodic output signal in the frequency domain has only an impulse at the fundamental frequency and perhaps some other impulse energy at DC and harmonics. In the actual oscillator implementation, the zero crossings of the periodic wave vary with time as shown in Fig. 3.3. This varying of the zero crossings is known as time-domain jitter.

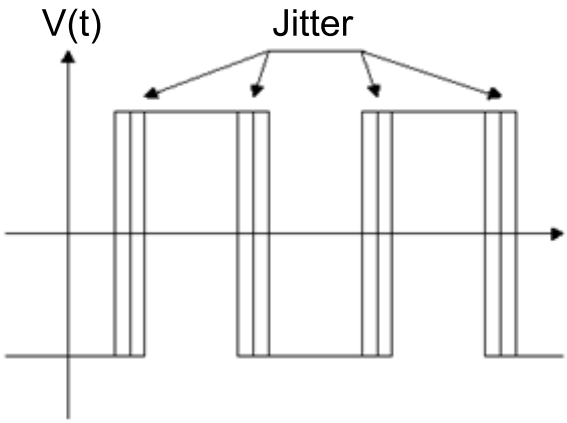


Fig. 3.3. Periodic signal with jitter.

A signal with jitter no longer has a nice impulse spectrum. Now the frequency spectrum consists of impulses with skirts of energy as shown in Fig. 3.4. These skirts are known as phase noise.

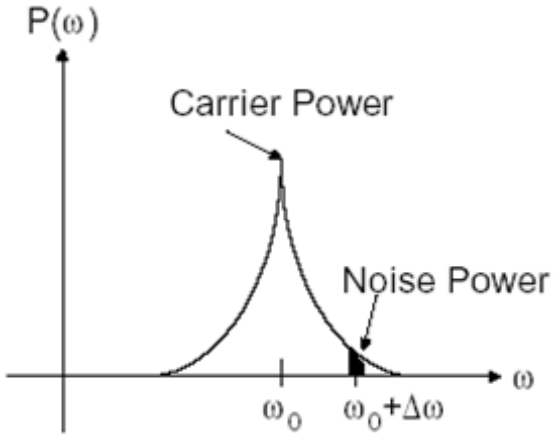


Fig. 3.4. Frequency spectrum of a signal with phase noise.

Phase noise is generally measured in units of dBc/Hz at a certain offset from the desired or carrier signal. The formal definition of phase noise is the ratio of the sideband noise power in a 1Hz bandwidth at a given frequency offset $\Delta\omega$ from the carrier over the carrier power as shown in the following.

$$L\{\Delta\omega\} = \frac{P_{sideband}\left(\omega_o + \Delta\omega,\ 1Hz\ Bandwidth\right)}{P_{carrier}} \tag{3-6}$$

The PLL can be designed in such a way as to minimize the phase noise of the output signal. Fig. 3.5 shows the simplified PLL model with noise sources. The major noise sources of the PLL include an external reference input noise (θ_{in}), VCO internal noise (θ_{vco}), phase detection noise (ΔI_p), and frequency divider noise (θ_{div}). The way the PLL is designed depends on what is the dominant source of noise in the loop.

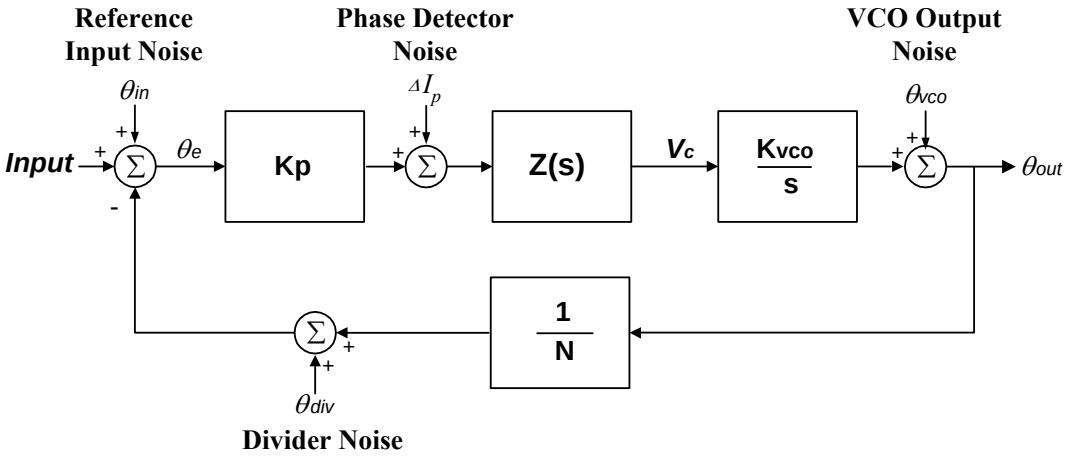


Fig. 3.5. Simplified PLL model with noise sources.

The transfer function of the output noise (θ_{out}), due to each of the noise source, can be calculated as follows.

$$\theta_{out} = \frac{1}{1+\frac{I_P K_{VCO} Z(s)}{2\pi N s}}\theta_{vco} + \frac{\frac{I_P K_{VCO} Z(s)/(2\pi s)}{1+\frac{I_P K_{VCO} Z(s)}{2\pi N s}}}{Kp}\theta_{in}$$

$$+ \frac{\frac{I_P K_{VCO} Z(s)/(2\pi s)}{1+\frac{I_P K_{VCO} Z(s)}{2\pi N s}}}{Kp}\theta_{div} + \frac{1}{1+\frac{I_P K_{VCO} Z(s)}{2\pi N s}}\Delta I_p \qquad (3\text{-}7)$$

where

N value of the output divider,
Kp $= I_p / 2\pi$, the gain of the phase detector
K_{VCO} $(d\omega / dv)$, VCO gain,
$Z(s)$ transfer function of the loop filter,
I_p charge pump current.

If the transfer function $Z(s)$ is denoted by $Z(s) = \frac{M(z)}{N(z)}$ where both $M(z)$ and $N(z)$ are polynomials, then the (3.7) can be rewrote as:

$$\theta_{out} = \frac{sN(s)}{sN(s)+\frac{I_P K_{VCO} M(s)}{2\pi N}}\theta_{vco} + \frac{I_P K_{VCO} M(s)/(2\pi)}{sN(s)+\frac{I_P K_{VCO} M(s)}{2\pi N}}\theta_{in}$$

$$+\frac{I_P K_{VCO} M(s)/(2\pi)}{sN(s)+\frac{I_P K_{VCO} M(s)}{2\pi N}}\theta_{div}+\frac{1}{Kp}\frac{I_P K_{VCO} M(s)/(2\pi)}{sN(s)+\frac{I_P K_{VCO} M(s)}{2\pi N}}\Delta I_p \qquad (3\text{-}8)$$

, when DC is under consideration, $\theta_{out}=N(\theta_{in}+\theta_{div}+(1/Kp)\Delta I_p)$, and this means that the spectrum of phase noise will be N^2 times the input noise and hence $20\log(N)$, and it is shown in Fig. 2.9. From equation (3-8), the output phase noise due to phase noise of VCO is a high pass characteristic when $N(s)$ is a function of constant, or band pass behavior when $N(s)$ and $M(s)$ are higher order polynomial than function of constant. And the output phase noise due to the other source is a low pass characteristic. Taking third order PLL for example, the output phase noise is:

$$\theta_{out,3}=\frac{s^2C_1\left(\frac{\tau s}{r+1}+1\right)}{s^2C_1\left(\frac{\tau s}{r+1}+1\right)+\frac{I_P K_{VCO}}{2\pi M}\frac{r}{r+1}(\tau s+1)}\theta_{vco}+\frac{I_P K_{VCO} C_1\frac{r}{r+1}(\tau s+1)/(2\pi)}{s^2C_1\left(\frac{\tau s}{r+1}+1\right)+\frac{I_P K_{VCO}}{2\pi M}\frac{r}{r+1}(\tau s+1)}\theta_{in}$$
$$+\frac{I_P K_{VCO} C_1\frac{r}{r+1}(\tau s+1)/(2\pi)}{s^2C_1\left(\frac{\tau s}{r+1}+1\right)+\frac{I_P K_{VCO}}{2\pi M}\frac{r}{r+1}(\tau s+1)}\theta_{div}$$
$$+\frac{1}{Kp}\frac{I_P K_{VCO} C_1\frac{r}{r+1}(\tau s+1)/(2\pi)}{s^2C_1\left(\frac{\tau s}{r+1}+1\right)+\frac{I_P K_{VCO}}{2\pi M}\frac{r}{r+1}(\tau s+1)}\Delta I_p \qquad (3\text{-}9)$$

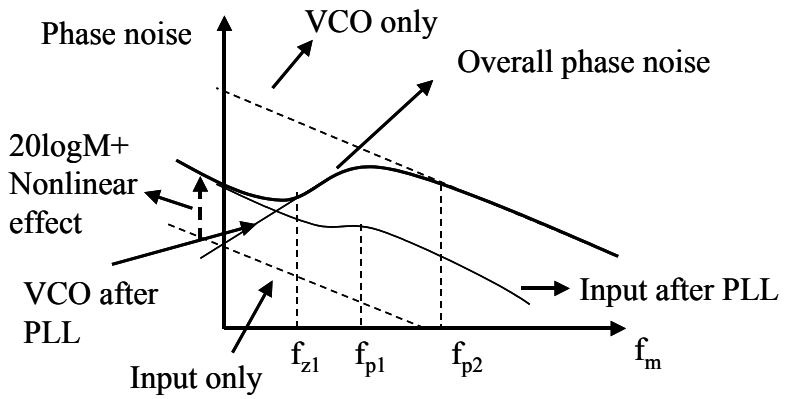


Fig. 3.6. Output phase noise of a charge pump PLL with a frequency divider.

, the transfer function of output phase noise has some points, at low frequency, $s^2 C_1\left(\frac{\tau s}{r+1}+1\right) << \frac{I_P K_{VCO}}{2\pi M}\frac{r}{r+1}(\tau s+1)$, thus $\theta_{out} \approx N(\theta_{in}+\theta_{div}+(1/Kp)\Delta I_p)$ and the input phase noise, or other noise is dominant, and at high frequency, $s^2 C_1\left(\frac{\tau s}{r+1}+1\right) >> \frac{I_P K_{VCO}}{2\pi M}\frac{r}{r+1}(\tau s+1)$, thus $\theta_{out,3} \approx \theta_{vco}$ and the noise from VCO is dominant. Although at low frequency, the output phase noise has been times N^2, the crystal oscillator for input source has an excellent phase noise, the output phase noise has not caused much high phase noise. However, the choice of the frequency divide ratio still should be taken care and should not be taken a too large divide ratio. Additional, for high frequency wireless system, the VCO has a high frequency and large tuning range, this will make gain constant of VCO, K_{VCO}, become very large. Therefore, the noise on control voltage of VCO is very important for overall output phase noise, thus there are many points to be taken care, one is layout consideration, the metal line of control voltage should be far from other circuit elements, and the noise from supply and resister of loop filter should be made sure that the thermal noise of these items do not cause too much noise peaking at low frequency while maintaining the low noise at higher frequency. The noise sources from the loop resister and supply can be expressed as follows:

$$\frac{\phi_{ni}}{v_{n1}} = \frac{sC_1}{RC_1 s+1} \Rightarrow \frac{\phi_{no,3}}{v_{n1}} = \frac{sC_1}{RC_1 s+1}\cdot\frac{\phi_{no,3}}{\phi_{ni}} \qquad (3\text{-}10)$$

, where v_{n1} is the equivalent voltage noise of R, and the noise source from supply is the same with (3-10). Thus, too large value of the resister will make large voltage

noise and have the influence on phase noise.

From above analysis, we know that there are many kinds noise source in PLL system, some of them have a low pass characteristic, such as frequency divider, phase detector, resister of the loop filter, charge pump, and the other has a high pass characteristic, such as VCO. Therefore, good choice for loop filter can make noise optimized and makes the design of the mixer more easily in the whole transceiver. There is a well-known trade-off in the design of a PLL [9] between the loop bandwidth, jitter performance and the locking speed. If the loop bandwidth is large, the PLL takes little time for locking and has large jitter reduction of the internal VCO noise, but cannot have a good suppression of the external input noise. If, on the other hand, the loop bandwidth is small, the PLL can have large input jitter reduction, but takes longer time for locking and leaves much of the internal VCO noise unreduced. Therefore, it is desirable to optimize the loop bandwidth such that the PLL has sufficient noise reduction of both the external input and the VCO.

3.4 Direct Digital Frequency Synthesizer

When extremely fast switching speed of the synthesizer is required, as is the case for frequency-hopped systems, direct-digital frequency synthesis (DDFS) is a potential solution. The basic architecture is depicted in Fig. 3.7.

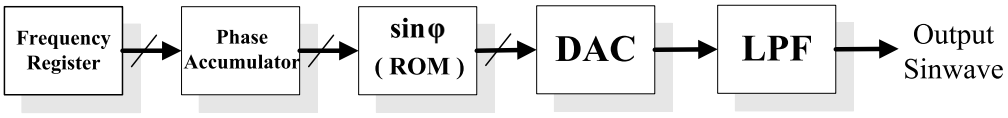


Fig. 3.7 Direct-digital frequency synthesis architecture.

The basic operation is straightforward sine it is purely a feedforward system. By

changing the value (K) of the frequency register, the phase will accumulate at a different speed and the frequency of the sine wave ROM output changes as a result. Therefore the synthesized output frequency is given by

$$f_{out} = f_{clk} \cdot \frac{K}{L_{acc}} \tag{3-11}$$

Where L_{acc} is the accumulator length and f_{clk} is the reference clock frequency. The digital sine wave is sent through a digital-to-analog converter (DAC) and lowpass filtered to remove unwanted high-frequency content. Since DDFS is a feedforward system, the switching time is essentially instantaneous. The frequency resolution is determined by the word length in the phase accumulator and can be much less than 1 Hz. The output spurious tones are caused by truncation in the phase accumulator and are approximately equal to

$$P_{spur}(dB) = 10\log\left(\frac{2^{-2(k-1)}}{3}\right) \tag{3-12}$$

Where k is the input bit length of DAC. Therefore, if spurious levels of -56dBc are specified, the accumulator and DAC would require 10 bits of dynamic range.

Several limitations to DDFS have restricted is application. First, the output frequency of the sine wave ROM is limited by the Nyquist criterion to half of the speed of the DAC. Furthermore, for low spurious levels, a very high-precision DAC is needed. The combination of high-speed and high-precision makes the power consumption too large to be useful in portable applications. To provide an RF carrier, the output of the DDFS must be mixed up using a single-sideband mixer with a fixed-frequency oscillator.

3.5 Integer-N and Fractional-N Frequency Synthesizer

Fig. 3.8 shows the basic blocks of a PLL frequency synthesizer. For integer-N phase-locked loop (PLL) frequency conventional synthesizers, the phase detector comparison frequency must be equal to the channel spacing (frequency resolution) because the main divider (N) can only increment and decrement in integer steps. In this architecture of synthesizers the loop bandwidth and the frequency resolution are closely interrelated. A high frequency resolution inherently implies a small reference frequency, and thus a slow switching time [10]. As a rule of thumb, the loop bandwidth should be less than one tenth of the reference frequency to achieve adequate reference suppression [11].

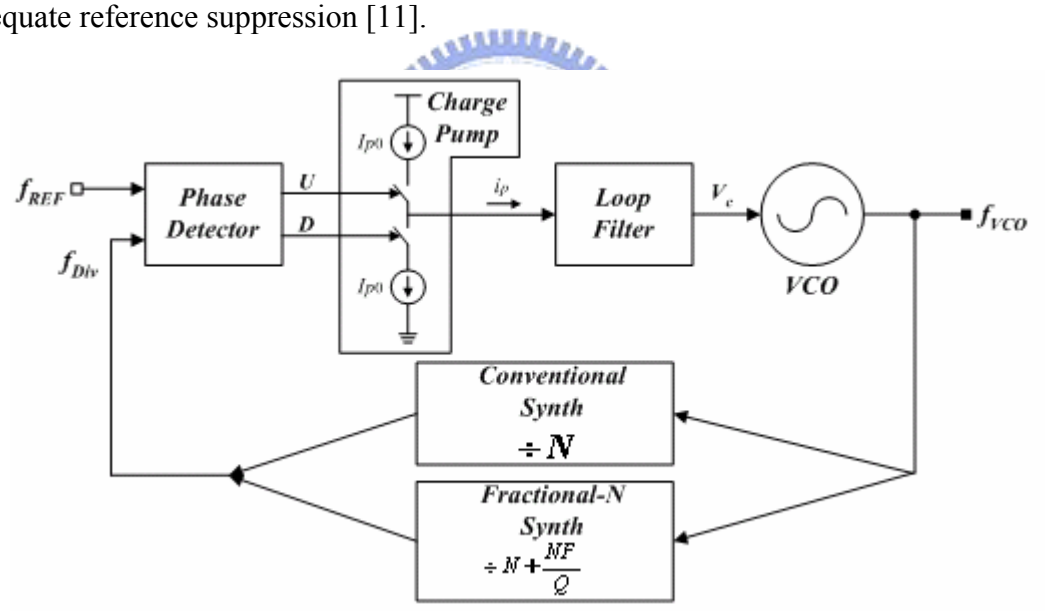


Fig. 3.8. The block diagram of the synthesizer.

The fractional-N PLL architecture allows frequency steps far smaller than the reference frequency. In other words, the main divider of the fractional-N synthesizer is capable of generating steps to be a fraction of the comparison frequency. Now the total divide ratio consists of an integer part (N) and fractional part (NF/Q). The

numerator (NF) and the denominator (Q , either 5 or 8) of a fraction are controlled through software programming.

The advantage of fractional-N synthesizers is two-fold. Since the close-in noise floor is directly related to total divided ratio (N), reducing N five or eight time theoretically implies a close-in noise floor improvement of 14dB(20log 5) or 18dB(20log8), respectively. At the same time, the comparison frequency will be 5 or 8 times great than it would be if a conventional synthesizer were used. This allows a wider loop filter to be used, that is to say, the loop bandwidth can be larger, alleviating the requirements for the voltage-controlled oscillator (VCO) phase noise and achieving a faster switching time. However, the fractional division causes spurious tones is shown in Fig. 3.9 at offset frequencies of

$$\frac{n}{F} \cdot fref, \quad n = 1,2,.....$$

where F is the denominator of the fractional divisor.

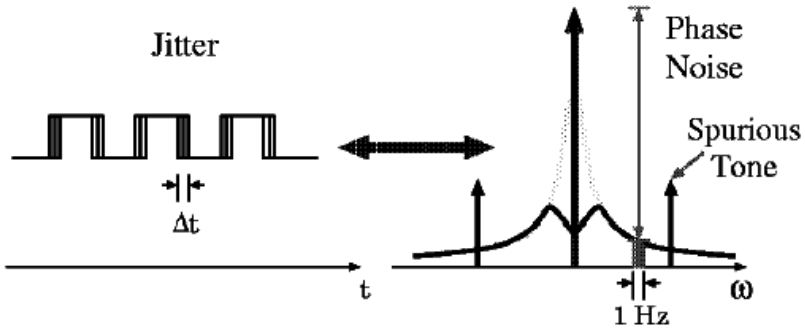


Fig. 3.9. Spurious tone.

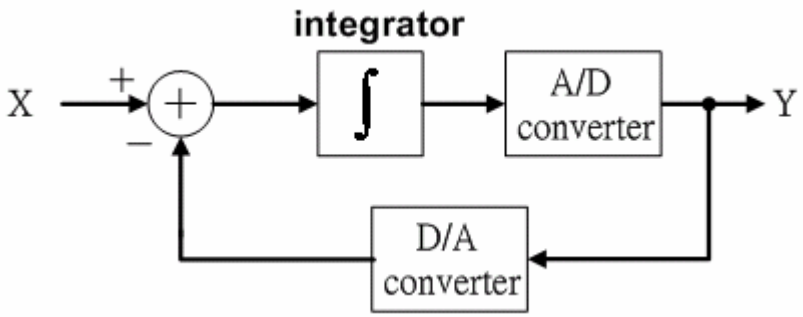
The loop filter attenuates these spurs, which restricts the loop bandwidth to reduce the spurs to an acceptable level. The result compared to integer-N is a wider loop bandwidth and an improvement in phase noise but at the cost of introducing unwanted spurs.

3.6 Delta-sigma Fractional-N Frequency Synthesizer

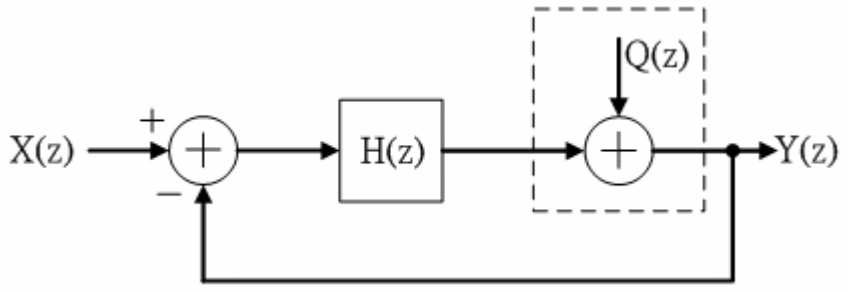
Since the spurious noise of fractional-N synthesizer comes from periodical phase error contributed by PFD, eliminating the phase error before modulating the VCO is a possible solution. Several methods to overcome the spurious problem have been proposed [12], [13], [14], out of which the method of reducing the noise by using a delta-sigma (ΔΣ) modulator has shown to be most promising and to be widely accepted as the best one.

3.6.1 ΔΣ Modulator Basics

A general delta-sigma modulator and its linear model are shown in Fig. 3.10. Fig. 3.10(a) shows a block diagram of how the system is implemented with integrator circuits. The integrator is a switch-capacitor discrete-time integrator. The A/D converter can be implemented in many ways. In order to simplify the explanation, assuming the A/D converter is a simple 1-bit quantizer or comparator. The D/A converter take the digital output and convert it back to an analog signal that is subtracted from the input signal at the input to the integrator. This system can be represented by the discrete-time equivalent linear model shown in Fig. 3.10(b). The switch-capacitor integrator is represented by its transfer function H(z), and the feedback path represents the 1-bit D/A converter.



(a)



(b)

Fig. 3.10 (a) general ΔΣ modulator and (b) linear model of the ΔΣ modulator

Treating the linear model shown in Fig. 3.10(b) as having two independent inputs, input signal X(z) and quantization noise Q(z). We can derive a signal transfer function, S_{TF} (z), by setting Q(z)=0.

$$S_{TF}(z) = \frac{H(z)}{1+H(z)} \tag{3-13}$$

We can also derive a noise transfer function, N_{TF}(z), by setting X(z)=0.

$$N_{TF}(z) = \frac{1}{1+H(z)} \tag{3-14}$$

From equation (3-14), as we have seen, the zero of the noise transfer function, N_{TF}(z), will be equal to the poles of H(z). In other words, Then H(z) goes to infinity, we see equation (3-14) that N_{TF}(z) will go to zero. We can also write the output signal as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function. In the discrete frequency domain, we have corresponding transfer function. In the discrete frequency domain, we have

$$\begin{aligned} Y(z) &= S_{TF}(z)\cdot X(z) + N_{TF}(z)\cdot Q(z) \\ &= \frac{H(z)}{1+H(z)}\cdot X(z) + \frac{1}{1+H(z)}\cdot Q(z) \end{aligned} \tag{3-15}$$

To noise-shape the quantization noise in a useful manner, H(z) are properly chosen such that its magnitude is large from DC to f_0 (i.e., over the frequency band of

interest). With such a choice, the signal transfer function, S_{TF} (z), will approximate unity over the frequency band of interest. Furthermore, the noise transfer function, $N_{TF}(z)$, will approximate zero over the same band. In other words, $N_{TF}(z)$ will have a high-pass response. Thus the quantization noise is reduced over the frequency band of interest while the signal itself is unaffected.

3.6.2 Higher-Order ΔΣ Modulator for Divider Control

Ideally the divisor would be continuously variable, set arbitrarily, which would attain continuous frequency resolution, without spurs. Of course this is not possible because the divider must be set to integer values. In the fractional-N PLL, the desired fraction is converted by the accumulator to a sequence of 1s,0s and with overflow, which could be considered a coarse, 1-bit ADC.

Fig 3.10 shows the basic modulator used in sigma-delta A-D converters x(k) is the modulator input, y(k) is the modulator output, and $e_q(k)$ is the quantization error added by the 1-bit A/D. In fractional-N synthesis application, the input to the delta-sigma modulator is the desired fractional offset, which is a digital word. Consequently, the integrator may be digitally implemented and the 1-bit D-A is not required.

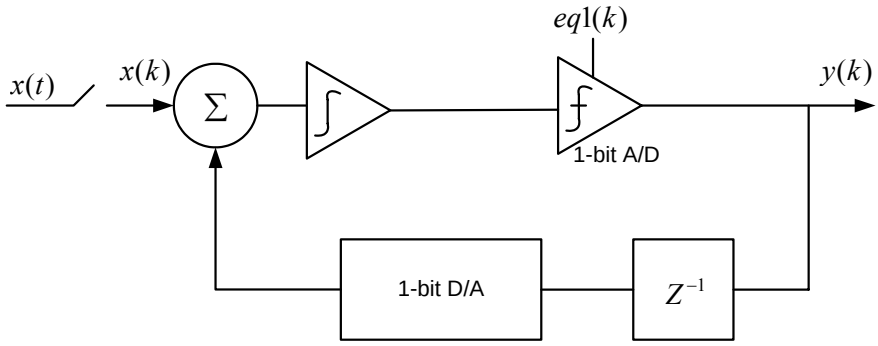


Fig. 3.11 Sigma-delta Modulator

Fig.3.11 shows a sigma-delta modulator suitable for fractional-N synthesizer.

$$Y(z) = \frac{1/(1-z^{-1})}{(1+z^{-1})/(1-z^{-1})}(X(z)) + \frac{1}{(1+z^{-1})/(1-z^{-1})}E_q(z)$$

$$= X(z) + (1-z^{-1})E_q(z) \qquad (3\text{-}16)$$

where Y(z), X(z) and $E_q(z)$ are the Z-transforms of y(k), x(k), and $e_{q1}(k)$,respectively.

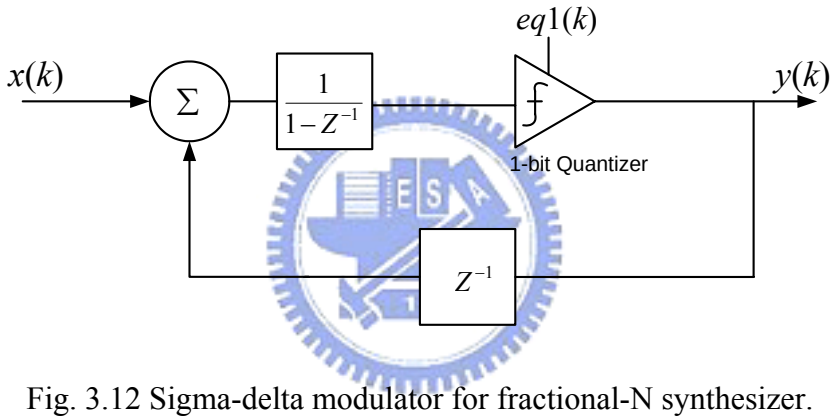


Fig. 3.12 Sigma-delta modulator for fractional-N synthesizer.

Higher-order delta-sigma modulators improve the noise-shaping characteristic at low frequencies. The analysis of higher-order modulators are much more complicated than first order ones and given in literatures [15] [16]. Because the mathematical description for higher-order stability is difficult, the design of higher-order modulator is usually based on several empirical rules rather than analytical solutions [17]. Higher order modulators with several feedback are not always stables but this problem can be solved as the MASH (Multistage noise shaping technique) structure, proposed in the article [18]. A cascade of first-order modulator is used to shape progressively to a high degree the input. If we filter out the high frequency component H_{noise}, the

component *X*(z) remains.

The total order of the modulator is fixed by the number of first-order modulators placed in cascade. Usually the third-order or fifth-order modulator is used. We will develop the equation associated with a third-order structure as shown in Fig. 3.13 and consider the practical implementation.

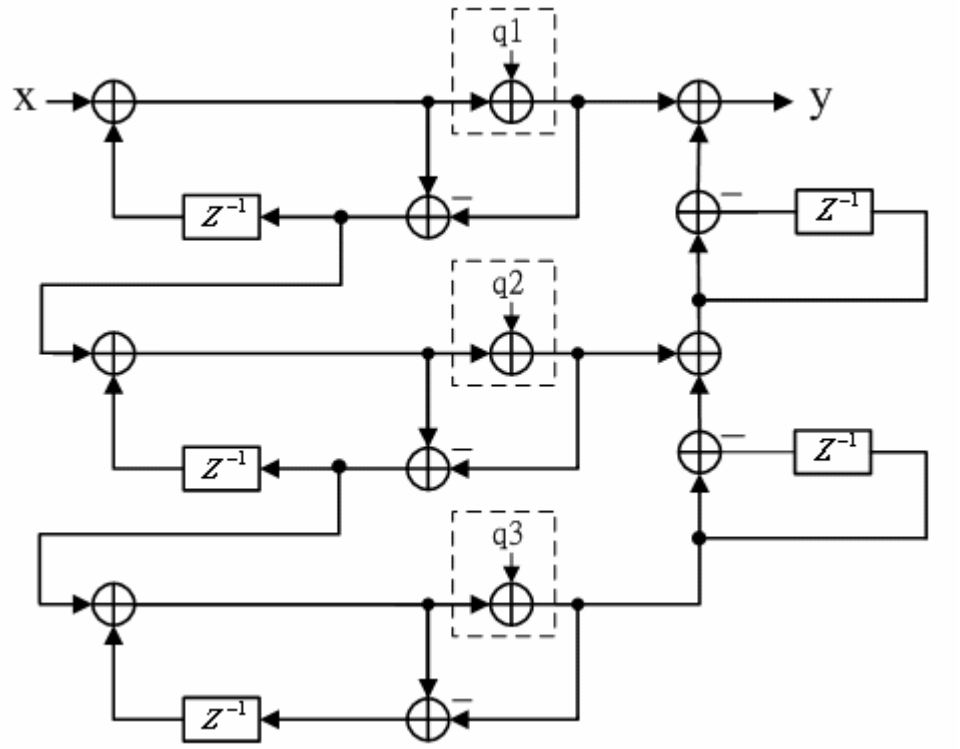


Fig. 3.13. Multistage noise shaping, in the MASH 1-1-1.

In Fig 3.12, the output y is expressed as a summation of different contributions from the input $x = \frac{K}{F}$ and several one-bit quantizers q_1, q_2 and q_3, where for all i, q_i is a quantization noise not correlated with the input and with the other noise sources. The expression of y is give by

$$Y(z) = X(z) + Q_1(1 - z^{-1})$$

$$+(-Q_1+Q_2(z)(1-z^{-1}))(1-z^{-1})$$

$$+(-Q_2+Q_3(z)(1-z^{-1}))(1-z^{-1})^2$$

$$=X(z)+(1-z^{-1})^3Q_3(z)$$

$$=X(z)+H_{noise}(z)Q_3(z) \qquad (3\text{-}17)$$

From the equation (3-17) we can deduce the frequency noise introduced by fractional division when the MASH3 controls the division ratio by $N/N+1$ with $x=\frac{K}{F}$ and N given. Indeed $\int_{vco}=(N_{\text{int}eger}+N_{fractiona}l)f_{ref}$ .From this term the constant term $Nf_{ref}+\frac{K}{F}f_{ref}$ is removed and the fluctuating term

$$f_{noise}(f)=H_{noise}(f)Q_3(f)f_{ref}=Nf_{ref}+(\frac{K}{F}+H_{noise}(f)Q_3(f))f_{ref} \qquad (3\text{-}18)$$

remains, which is the expression of the frequency fluctuation noise introduced by fractional-N frequency synthesis.

A 1-bit quantizer produces a quantization q_3 which is uncorrelated with x. Furthermore if q_3 is assumed to be a uniformly distributed white-noise sequence, the mean of q_3 is zero and the variance is $\partial_{q_3}{}^2=\frac{\Delta}{12}$, with $\Delta=1$. As the power is spread over the bandwidth f_{ref}, the power spectral density (PSD) of the quantization error q_3 is $\frac{\partial_{q_3}{}^2}{fref}=\frac{1}{12f_{ref}}$. This enables us to write the expression of the frequency fluctuation $f_{noise}(z)$ as

$$S_{f_{noise}} = \left|H_{noise}(f) f_{ref}\right|^2 \frac{1}{12 f_{ref}} = \frac{\left|1 - z^{-1}\right|^6 f_{ref}}{12} \tag{3-19}$$

In terms of noise contribution, the expression of the phase noise is more relevant than the frequency noise expression. Phase and frequency are related by an integration as $\phi = \int 2\pi f_{\text{instantaneous}} dt$

$$\begin{aligned} S_{\phi, N \leftrightarrow N+1}(z) &= S_{f_{noise}} \cdot S_{\text{integration}} \\ &= \frac{\left|1 - z^{-1}\right|^6 \cdot f_{ref}}{12} \cdot \frac{(2\pi)^2}{\left|1 - z^{-1}\right| {f_{ref}}^2} \\ &= \frac{(2\pi)^2}{12 f_{ref}} \left|1 - z^{-1}\right|^4 rad^2 / Hz \end{aligned} \tag{3-20}$$

In replacing z by $e^{\frac{2 f_{ref}}{f_{ref}}}$, we can get:

$$S_{\phi, N \leftrightarrow N+1}(f) = \frac{(2\pi)^2}{12 f_{ref}} \left|2 \sin(\frac{\pi f}{f_{ref}})\right|^4$$

Generalizing equation (3-20) to any number of modulator sections;

$$S_{\phi, N \leftrightarrow N+1}(f) = \frac{(2\pi)^2}{12 f_{ref}} \left[2 \sin\left(\pi f / f_{ref}\right)\right]^{2(m-1)} rad^2 / Hz \tag{3-21}$$

where m is the number of modulator sections. The phase noise contributed by the quantization noise of modulator for a reference frequency of 16 MHz is plotted with second-order, third-order and fourth-order structures is shown in Fig. 3.14.

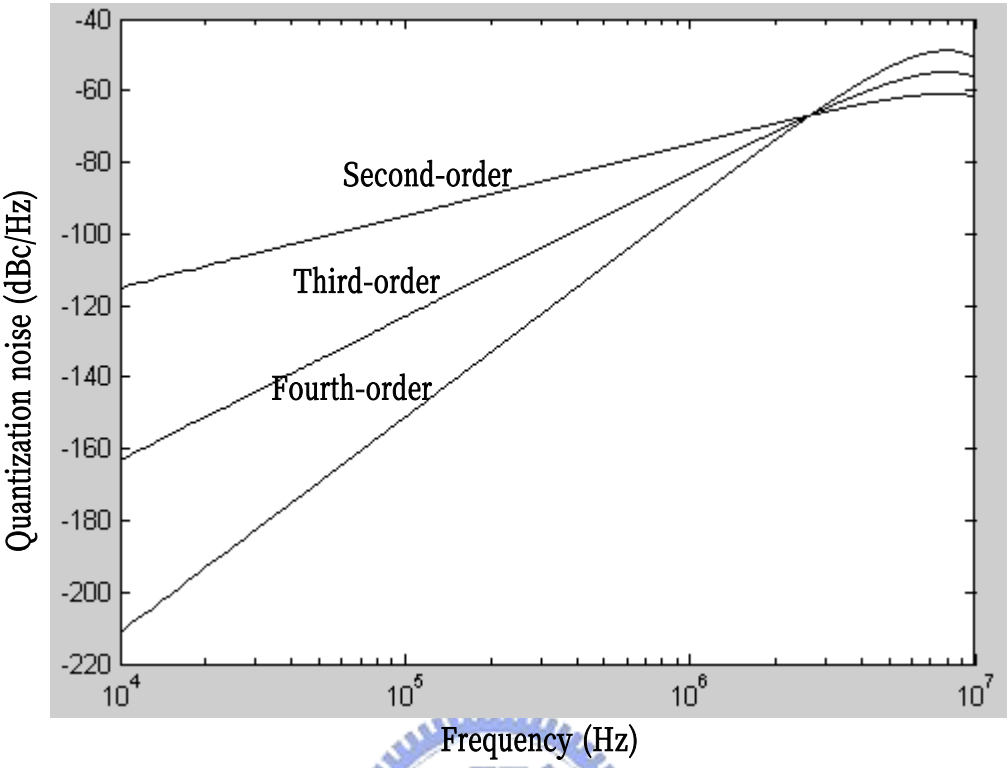


Fig. 3.14. Multi-order delta-sigma noise shapers for reference frequency of 16MHz.

When a MASH structure controls the fractional frequency division, the quantization noise is shaped as shown by equation (3-21). Higher frequencies component are then removed by the low-pass filter in the PLL. Obviously, the spurious performance is improved.

A digital accumulator is a compact realization of DSM. The output of the accumulator is delayed by a latch and fed back to the input of the accumulator as in a delta-sigma modulator. The overflow is a 2-level signal corresponding to the quantized output of the modulator. An example of MASH3 structure is implemented using digital accumulators is shown in Fig. 3.15.

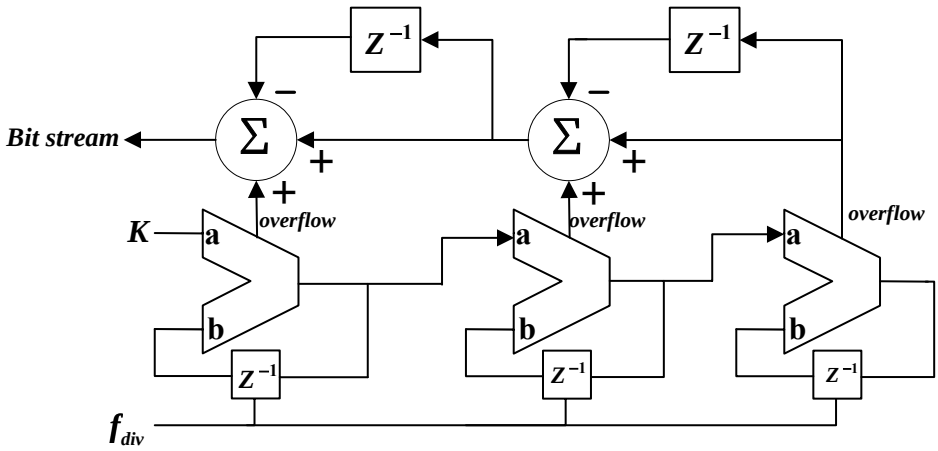


Fig. 3.15. MASH 1-1-1 implementation using digital accumulators.

3.6.3 High-Order ΔΣ-Controlled Fractional-N Synthesizer

The noise shaping technique can also be utilized in fractional-N frequency synthesis applications. A block diagram of a ΔΣ fractional-N synthesizer is shown in Fig. 3.16. The ΔΣ modulator output is on average $K/2^m$ cycles of the reference frequency $\boldsymbol{F_{ref}}$. The resulting output frequency is the $\boldsymbol{F_{out}} = (\boldsymbol{N} + K/2^m)\,\boldsymbol{F_{ref}}$. The modulator output controls the instantaneous division modulus of the prescaler, such that the mean division modulus is $(\boldsymbol{N} + K/2^m)$, with the number (m) of bits of the ΔΣ modulator and the input word (K). The corresponding phase changes at the prescaler output are quantized, leading to possible spurious tones and quantization noise. By selecting higher order ΔΣ modulators, the spurious energy is whitened and shaped to high-frequency noise, which can be removed by the low-pass loop filter. As a result, for a given frequency resolution, an arbitrary high $\boldsymbol{F_{ref}}$ can be chosen, by assigning the proper number of bits K to the modulator. The loop bandwidth is not restricted by the reference spur suppression, resulting in faster settling and higher integratability. Additionally, the division modulus is decreased by a factor $2^{m-\min}$ (with *m_min* the

minimum number of bits for the frequency resolution), so that noise of the PLL blocks, except for the VCO, is less amplified. It is worth pointing out that the delta-sigma modulator can be implemented using all digital architectures thus is easily integrated into single chip and is insensitive to process variation.

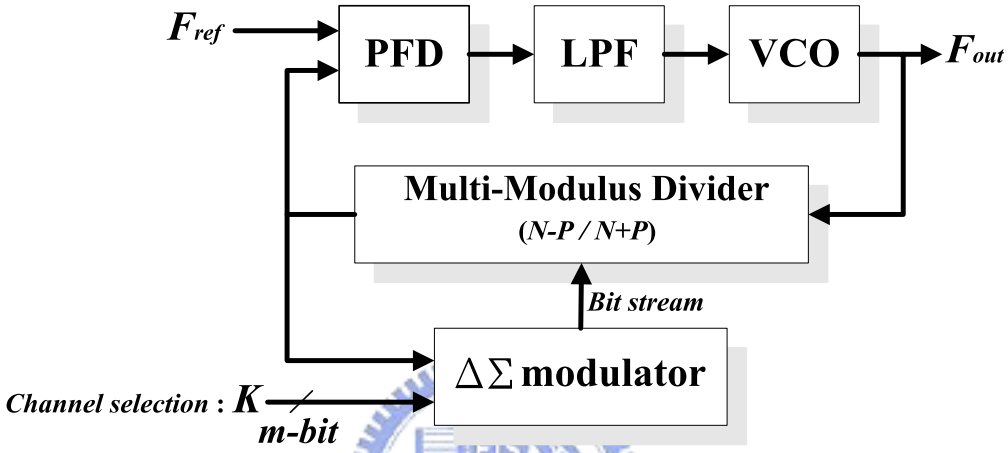


Fig. 3.16. The block diagram of the ΔΣ fractional-N synthesizer.

Chapter 4 Circuit Level Implementation of Frequency Synthesizer

4.1 Synthesizer Architecture

The designed frequency synthesizer for 802.11a transceiver uses ΔΣ fractional-N method. Fig. 4.1 shows the block diagram of the designed frequency synthesizer. It is made up of multi-modulus prescaler and a third-order sigma-delta modulator, which is one of the noise shaping techniques to suppress the fractional spurs occurring at all multiples of the fractional frequency resolution offset. The input bit length of the modulator is chosen as 24-bits which leads to the

$$\text{Frequency resolution} = \frac{f_{ref} \times prescaler}{2^{24}}$$

When the PLL is locked, the RF output frequency is

$$F_{out} = \left(20 + \frac{K}{2^{24}}\right) F_{ref}, \quad F_{ref} = 16\text{MHz}, \quad K < 2^{24}$$

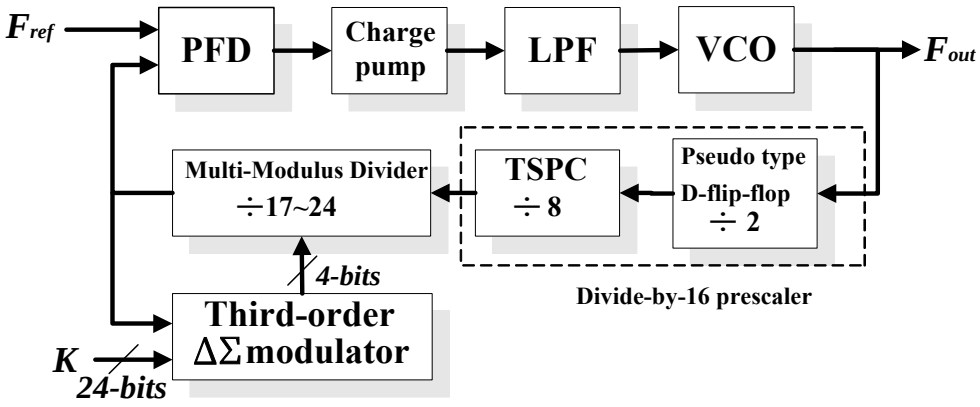


Fig. 4.1. The block diagram of the designed synthesizer.

4.2 The Phase Detector

One of the critical building blocks of the PLL is the phase frequency detector (PFD). An ideal phase detector produces an output signal whose DC value is linearly proportional to the difference between the phases of two periodic inputs. A low precision PFD has a wide dead zone (undetectable phase difference range), which results in increased jitter [19]. The jitter caused by the large dead zone can be reduced by increasing the precision of the phase frequency detector.

Fig. 4.2 shows the relation between dead zone of PFD and the phase error of PLL. If the phase difference of Fref clock and Fdiv clock is smaller than the dead zone, the PFD cannot detect the phase difference. So the phase error signal of PFD will remain zero, resulting in unavoidable phase error between Fref clock and Fdiv clock.

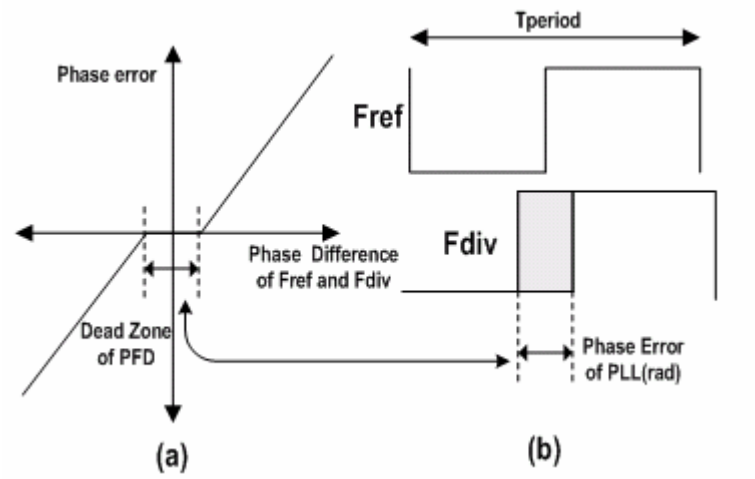


Fig. 4.2. (a) PFD dead zone and (b) PLL jitter.

In order to speed up the operation frequency and to reduce the dead zone, a dynamic logic style PFD was designed and shown in Fig. 4.3. From the circuit diagram of the PFD we can see that the shortened feedback path delay and dynamic operation allow high precision in the high-frequency. In order to avoid dead zone, the

PFD asserts both UP and DW outputs as shown in Fig. 4.4. For in-phase inputs of **Fref** and **Fdiv**, the charge pump will see both UP and DW pulse for the same short period of time. If there is a phase difference between **Fref** and **Fdiv**, the width of UP and DW pulse will be proportional to the phase differences of the inputs. The physical layout of the phase detector is shown in Fig. 4.5 and the performance summary of phase detector is listed in Table 1.

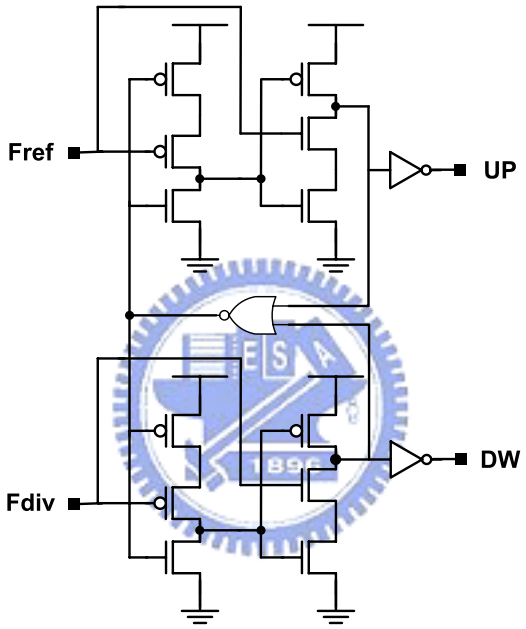


Fig. 4.3. The schematic of the phase detector.

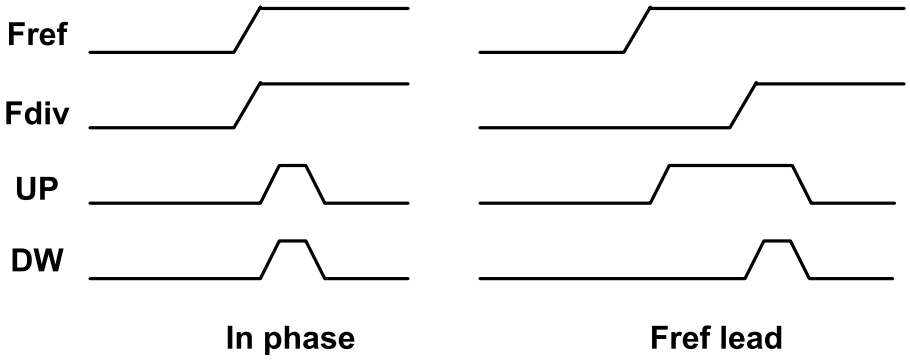


Fig. 4.4. Waveform of the phase detector.

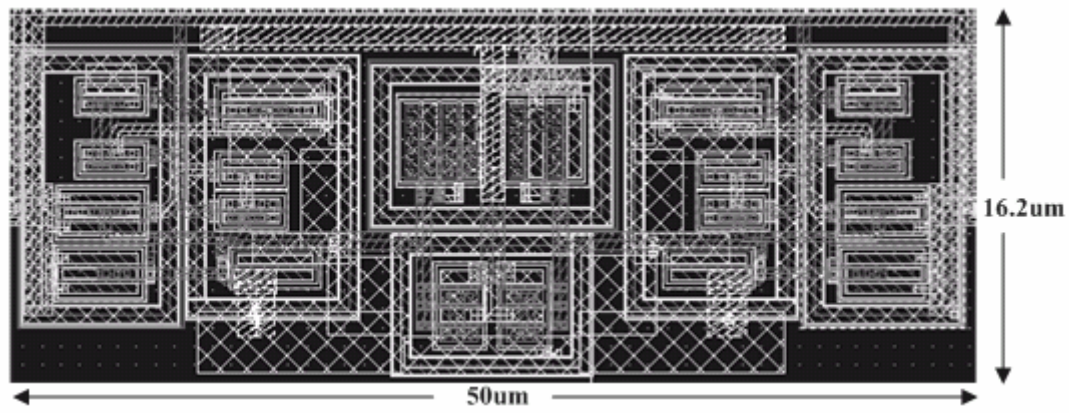


Fig. 4.5. Physical layout of phase detector.

Table 1 Performance summary of phase detector.

Operation frequency	16MHz
Power consumption	0.36mW
Chip area	$50 \times 16.2\ um^2$

4.3 Charge Pump

In a conventional CP of fig. 4.6(a), several spikes occur on the output when the currents are switched on and off as switches M1 and M2 are directly connected to the output. These spikes reflect into the output if no proper actions are taken. As these spikes occur at the reference frequency, they will cause spurs in the PLL output spectrum at an offset from the carrier equal to reference frequency.

In this design, to reduce the reference frequency spurs problem, we use indirectly connected switches M1 and M4 with output and thus the drain node of M2 and M3 is directly connected to the output which shown in Fig. 4.6(b). The current glitches that now occur at the sources of M2 and M3 when switching M1 and M4 would not be directly conveyed to the output node because M2 and M3 are still off when the

glitches occur [20].

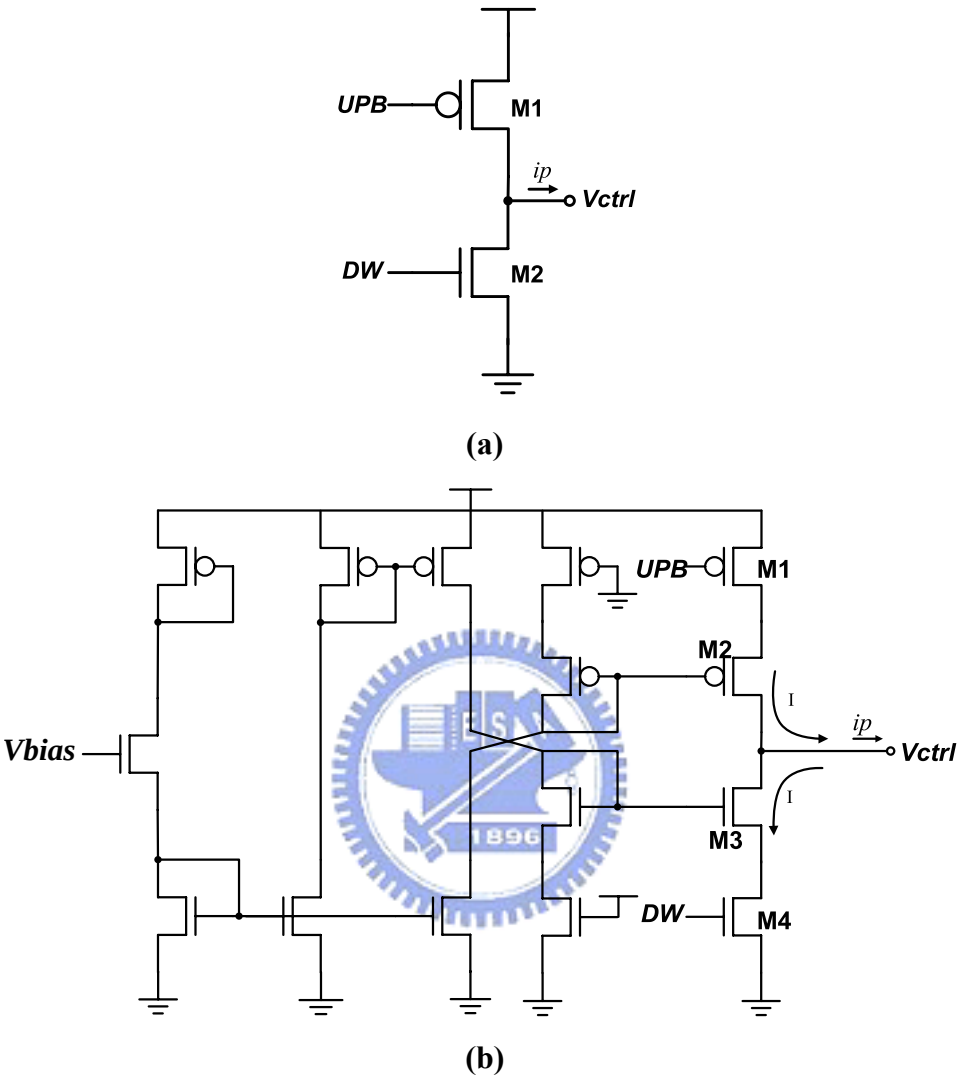


Fig. 4.6. (a) Conventional charge pump (b) The schematic of the current source employed in the charge pump.

The simulated result of charge and discharge current is show in Fig. 4.7. In this simulation UPB and DW signal are 1.8V 16MHz square waves. A capacitor 10nF loads the output of the charge pump. The charge pump positively charges the load capacitor with I_{UP} when M1 turn on, M4 turn off and negatively charges the load capacitor with I_{DW} when M1 turn off, M4 turn on. From the simulation result, the charge and discharge current is almost symmetric when referring to the vertical

centerline (0.9V). It is means that the charge and discharge current match to each other. This better matching between the charge and discharge current will improve the sideband spurs. The physical layout of the charge pump is shown in Fig. 4.8.

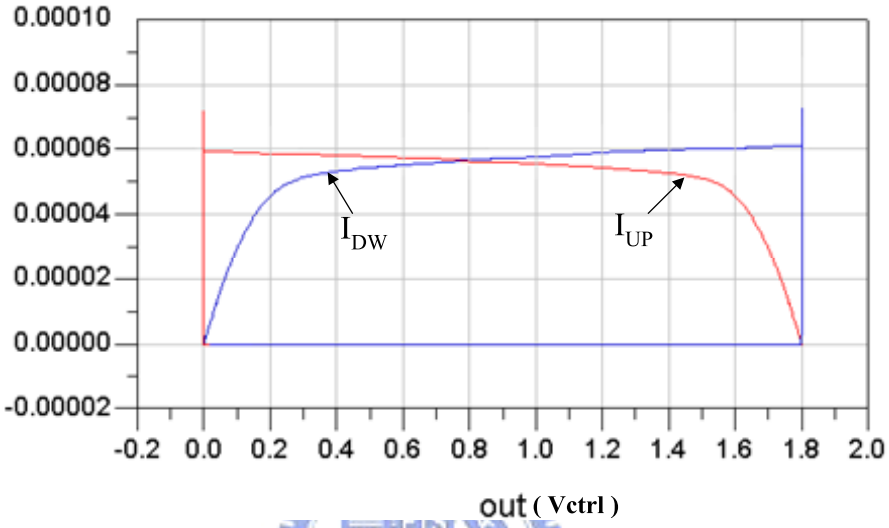


Fig. 4.7 Simulation result of charge and discharge current.

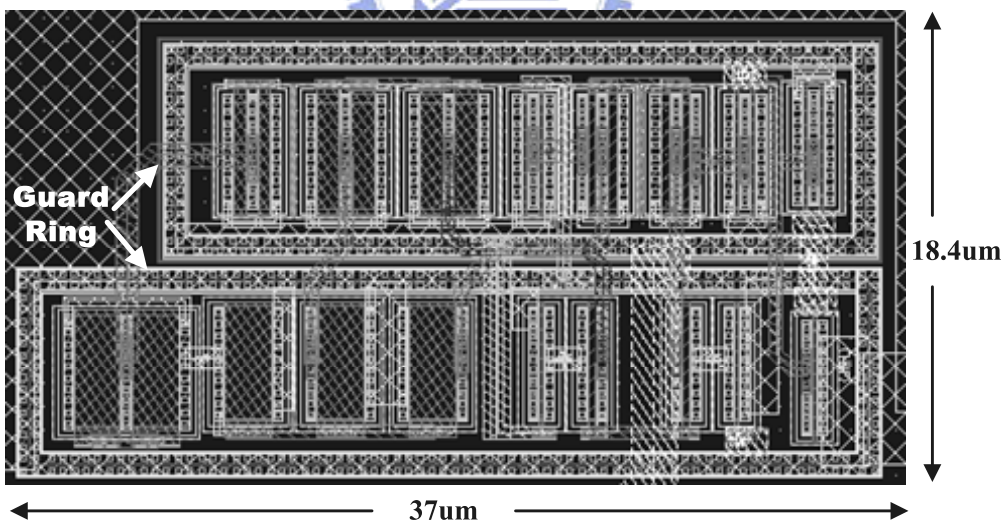


Fig. 4.8. Physical layout of charge pump.

4.4 Loop Filter

The loop filter schematic is shown in Fig. 4.9. It consists of two resistors (R_1 and R_2) and three capacitors (C_1, C_2, and C_3).

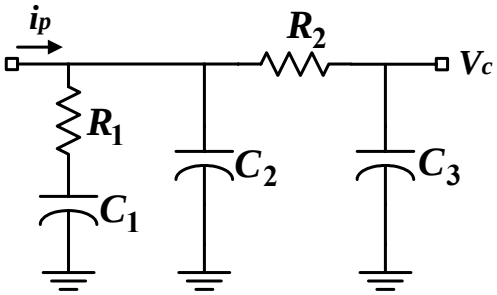


Fig. 4.9. Third-order loop filter.

The transimpedance of this loop filter is

$$Z(s)=\frac{V_c}{I_p}=\frac{1}{s}\cdot\frac{\dfrac{1+s\tau_1}{C_1+C_2+C_3}}{1+s\dfrac{C_1\tau_3+C_2(\tau_1+\tau_3)+C_3\tau_1}{C_1+C_2+C_3}+s^2\tau_1\tau_3\dfrac{C_2}{C_1+C_2+C_3}} \tag{4-1}$$

where $\tau_1 = R_1C_1$ and $\tau_3 = R_3C_3$.

In the filter, there are three poles and one finite zero. The locations of the poles and zero can be approximated for the case of $C_1 >> C_2$, C_3 and $R_1 > R_2$ as

$$\omega_z = \frac{1}{R_1C_1} \tag{4-2}$$

$$\omega_{p1} = 0 \tag{4-3}$$

$$\omega_{p2} \approx \frac{1}{R_1(C_2+C_3)} \tag{4-4}$$

and

$$\omega_{p3} \approx \frac{1}{\dfrac{R_3C_2C_3}{C_2+C_3}}. \tag{4-5}$$

One additional pole at the origin in the PLL comes from the VCO. The PLL -3dB bandwidth ω_{-3dB}, which is equal to its open-loop unity gain ω_u, must be placed somewhere between ω_z and ω_{p2} to obtain a reasonable phase margin for the PLL loop stability. Assuming that $\omega_u = \sqrt{\omega_z\omega_{p2}}$ and $\omega_{p3} >> \omega_u$, then the phase margin

yields

$$\Phi_m \approx \arctan\left(\sqrt{\frac{\omega_{p2}}{\omega_z}}\right) - \arctan\left(\sqrt{\frac{\omega_z}{\omega_{p2}}}\right). \quad (4\text{-}6)$$

In Fig. 4.9, C_1 produces the first pole at the origin for the type-II PLL. This is the largest capacitor, hence, it is a key integration bottleneck of the PLL. R_1 and C_1 are used to generate a zero for loop stability. C_2 is used to smooth the control voltage ripples and to generate the second pole. Usually, the loop filter of the PLL consists of C_1, C_2 and R_1. However, additional RC low pass filter is introduced to reduce any "spurs" caused by the reference frequency and to reduce the high frequency noise which is mainly caused by the undesired narrow pulses from the PFD due to the delay. Table 2 gives the selected component values.

The design value of R_2 and C_3 is optimized based on area on the chip and locking time. The R_2C_3 time constant should be large for a low cutoff frequency. However, if a large R_2 and C_3 is added, the total step response also changes a lot. When the value of R_2 and C_3 is somewhat lower than the one of R_1 and C_2, respectively, the whole response does not change too much. Therefore, the product of R_2 and C_3 should be about half of the R_1 and C_2.

Table 2: PLL pole, zero and loop bandwidth parameters

Reference frequency	f_{ref}	16 MHz
PLL loop bandwidth	K	281 KHz
Zero frequency	f_z	113 KHz
Second pole frequency	f_{p2}	1.21 MHz
Third pole frequency	f_{p3}	7.96 MHz

Phase margin	Φ_m	54°
f_{ref} Attenuation	*SpurAtten*	63.65dB
Elements:	R_1	22 kΩ
	C_1	65 pF
	C_2	4 pF
	R_2	15 kΩ
	C_3	2 pF

4.5 Spiral-Inductor LC-Tank VCO

The quality of an *LC*-tank oscillator relies the quality of the *LC*-tank, which is the most important part of the oscillator concerning its quality. Therefore, the ideal oscillator would have infinite quality factor *LC*-tank. In practice, the quality factor of inductors is not very high in CMOS standard processes. The negative resistance is needed to compensate the tank with energy and sustain the oscillator. A feedback oscillator of Fig. 4.10 shows the implementation of a basic current steered *LC*-tank oscillator, which is designed to keep the transistors always in saturation. When the cross-coupled pair is close to clip the amplitude, one node is high and the other one is low. The negative resistance is typical provided by a cross-coupled pair of PMOS transistors, Q_1 and Q_2. Calculating the impedance seen at the drain of Q_1 and Q_2, it is noted that the positive feedback yields

$$R_{in} = -\frac{2}{g_m} \tag{4-7}$$

Simultaneously, the frequency of this circuit is given by

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}, \tag{4-8}$$

where C represents the sum of all capacitance at the output node. Thus, if $|R_{in}|$ is less than or equal to the equivalent parallel resistance of the tank, the circuit oscillates. This topology is called a "negative-g_m oscillator".

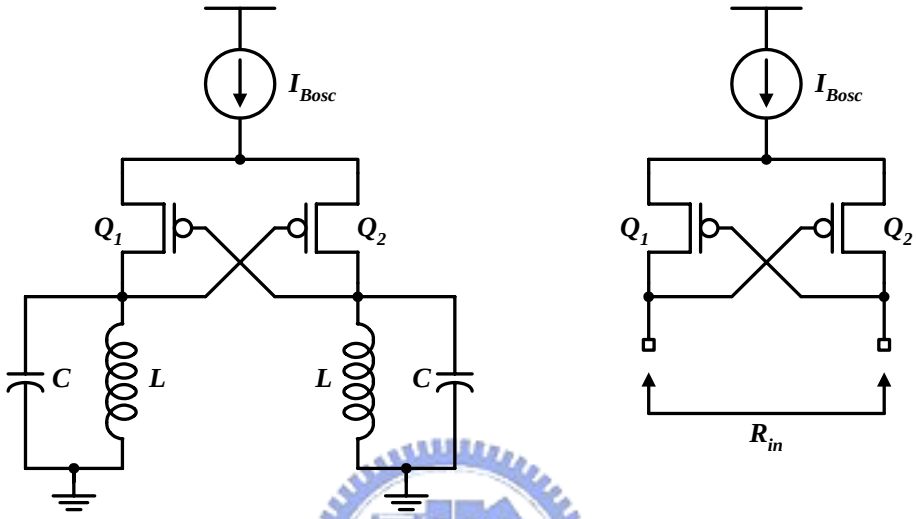


Fig. 4.10. Differential LC-tank oscillator schematic.

The relationship between oscillator phase noise and quality factor can be expressed by Leeson's phase-noise model which is shown in the following.

$$L(\Delta f) = 10\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{f_o}{2Q\Delta f}\right)^2\right]\cdot\left(1+\frac{\Delta f_{1/f^3}}{\Delta f}\right)\right\} \qquad (4\text{-}9)$$

Where $L(\Delta f)$ is SSB noise spectral density in units of dBc/Hz. The symbol k is Boltzman's constant, T is temperature in Kelvin, F is the excess noise factor, f_o is the carrier frequency, $\Delta f_{1/f^3}$ is the corner where the spectrum becomes proportional to $1/f^3$, and P_{sig} is the output signal power of the oscillator.

The designed quadrature VCO schematic is shown in Fig. 4.11 [21]. Since the constant Gm current source can improve the phase noise [22], the constant Gm

current bias circuit is employed to mirror the biasing current into the VCO core. The negative resistor in Fig. 4.11 is realized by two cross-coupled PMOS transistors M1(M3) and M2(M4) to provide enough negative resistance for oscillation. The cathodes of the two junction varactors are connected together. Through *Vc*, the dc bias voltages of the two junctions can be adjusted to change the value of junction capacitance and, thus, the VCO frequency. Since the quadrature error depends on the duty cycle of the VCO, special attention is paid to the symmetry of the VCO layout which is shown in Fig. 4.13, 4.14.

The pair of PMOS transistors is used to generate negative *gm* to overcome the loss of the LC tank, for two reasons. First, in this fabrication process, PMOS has lower device flicker noise than that of the NMOS. Furthermore, the PMOS resides inside an *N*-well and is well isolated from the noisy Si substrate. Despite its lower mobility, PMOS is favored in this design due to low noise considerations. Fig. 4.12 shows the output buffer used to amplify the VCO output. It is a regular open drain circuit with an n-well resistor to bias the gate of the output transistor. The gate bias was set to 1.1V. The output was connected to a bias the tee and fed with 1.8V. The total current dissipation of the output buffer is about 5mA.

The LC tanks of the VCO are formed using a ~0.78313nH circular shape of spiral inductor having center hole 165 μm, metal width 20 μm, turn 1.5, and 812.64fF P+/N-well varactor.

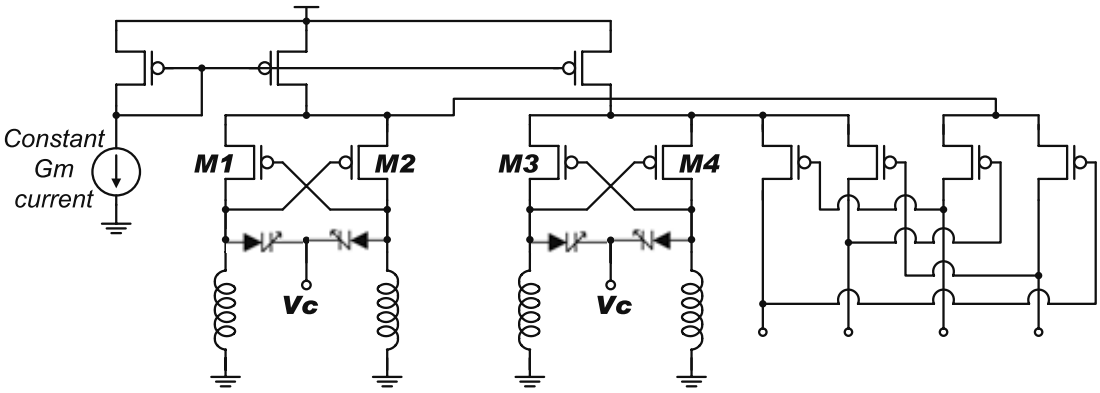


Fig. 4.11. VCO schematic.

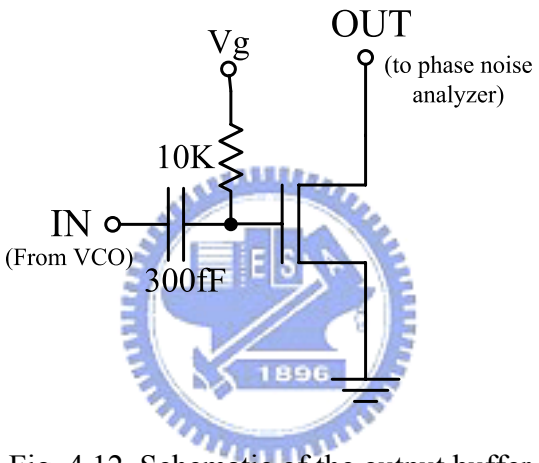


Fig. 4.12. Schematic of the output buffer.

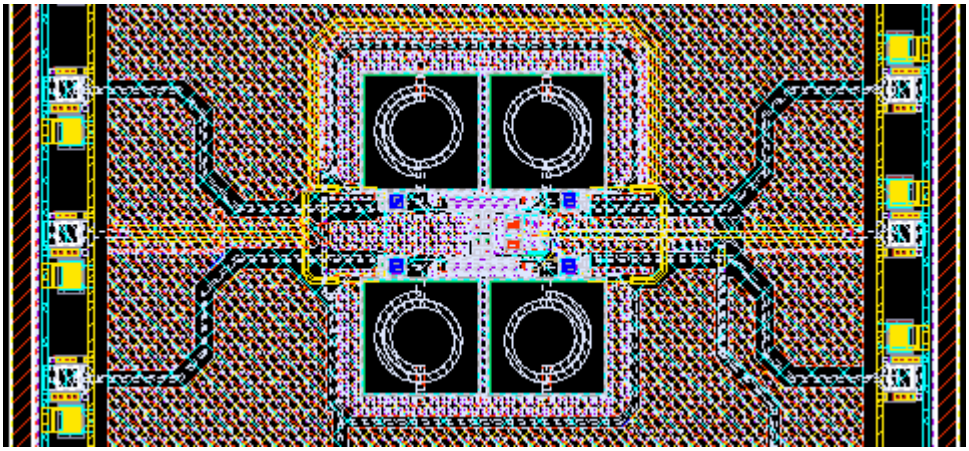


Fig. 4.13. Physical layout of the spiral-inductor LC-tank VCO.

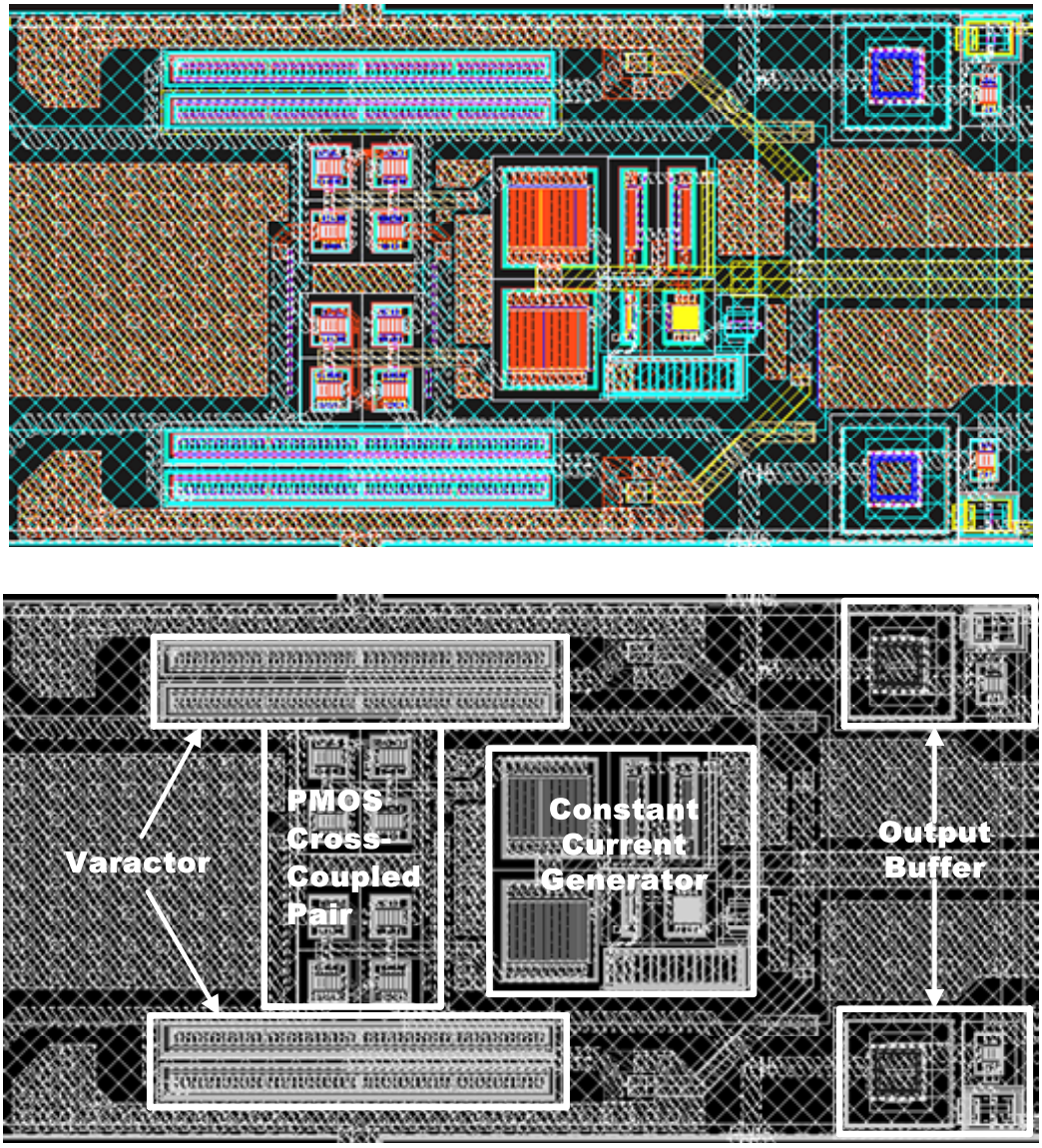
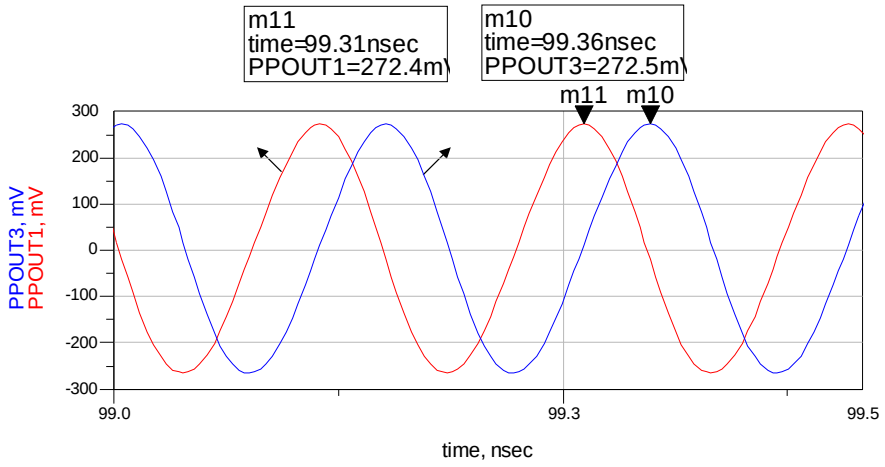
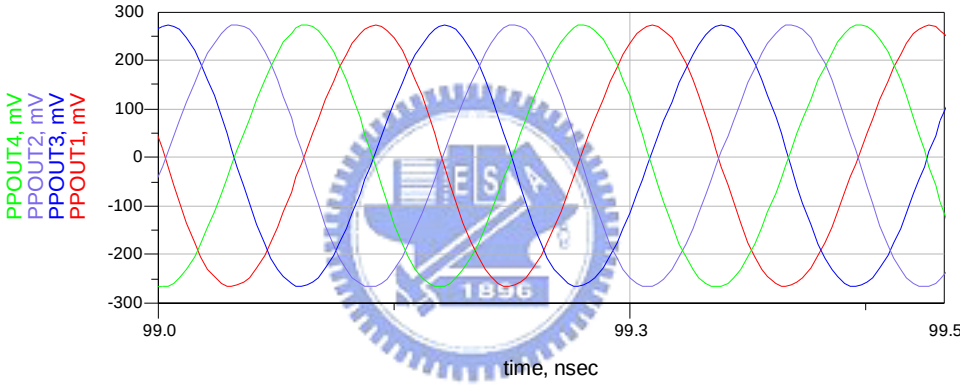


Fig.4.14. Physical layout of VCO (enlarge the center part).

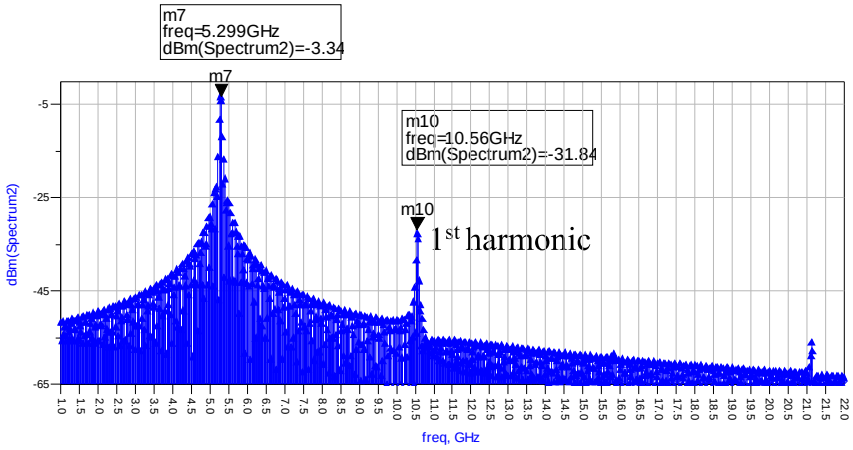
The simulation I, Q channel outputs of the quadrature VCO at voltage control 0.8V are shown in Fig.15. The phase error is less than 0.5° and the amplitude error are less than 0.5%.


m11
time=99.31nsec
PPOUT1=272.4m
m10
time=99.36nsec
PPOUT3=272.5m
m11
m10
PPOUT3, mV
PPOUT1, mV
300
200
100
0
-100
-200
-300
99.0
99.3
99.5
time, nsec

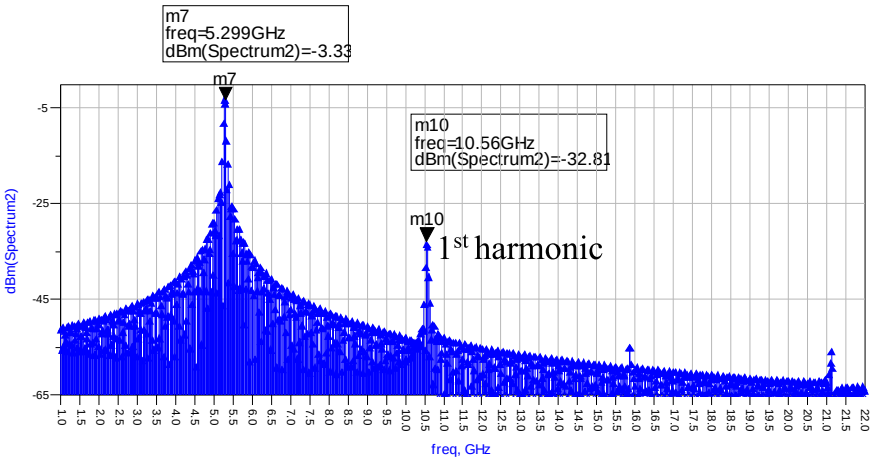
(a)


PPOUT4, mV
PPOUT2, mV
PPOUT3, mV
PPOUT1, mV
300
200
100
0
-100
-200
-300
99.0
99.3
99.5
time, nsec

(b)


m7
freq=5.299GHz
dBm(Spectrum2)=-3.34
m7
m10
freq=10.56GHz
dBm(Spectrum2)=-31.84
m10
1st harmonic
dBm(Spectrum2)
-5
-25
-45
-65
freq, GHz

(c)



(d)

Fig. 4.15. The simulation I, Q channel outputs of the VCO with quadrature phase output (a) single mode (b) differential mode (c) I channel spectrum (d) Q channel spectrum.

The simulated VCO tuning characteristic and output power is shown in Fig. 4.16, Fig. 4.17, respectively. Its tuning range is about 610MHz (from 4.92GHz to 5.53GHz) for 1.8V operation, which yields The VCO gain (K_{VCO}) about 450MHz/V.

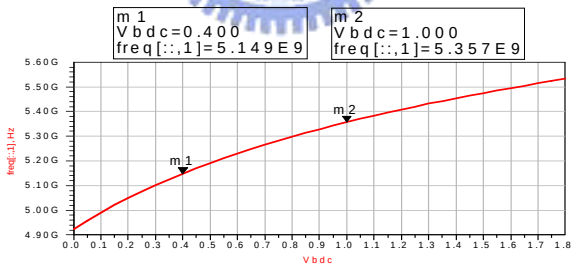


Fig. 4.16. The simulated VCO tuning characteristic.

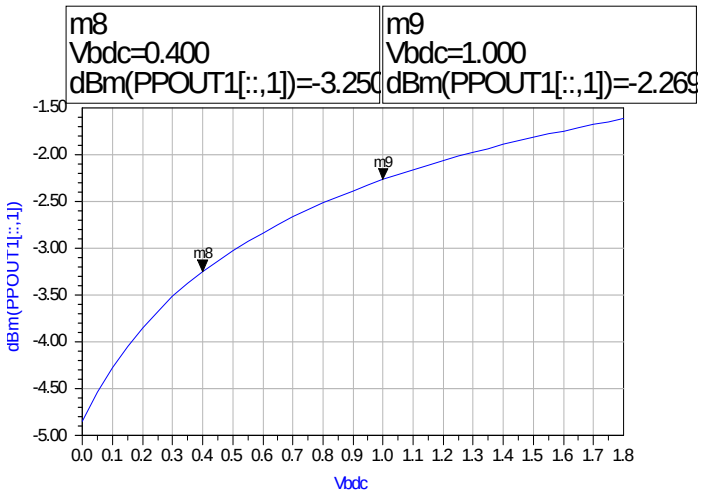


Fig. 4.17. The simulated VCO output power.

Fig 4.18 is phase noise with tuning voltage 0.8V, and phase noise is -92.41dBc/Hz at offset frequency 100KHz. The performance summary of VCO is tabulated in Table 3.

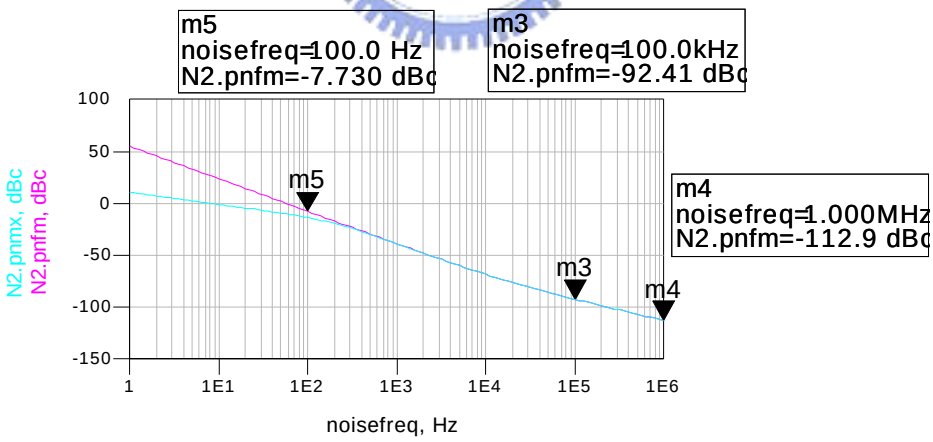


Fig. 4.18. The phase noise simulation of VCO.

Table 3 : Performance summary of VCO.

Parameter	Simulation (TT)

DC supply voltage	1.8V
Varactor type	P+/N-well varactor
Output Power	≈-4dBm
Sweep frequency	4.92~5.53GHz
Sweep voltage	0V~1.8V
Turning range	610MHz
Maximum VCO gain(Kvco)	450MHz / V
Phase noise	-92.42@100KHz -113@1MHz
Power consumption	6mW (core) 21mW (total)
Chip area	900×800 um^2

4.6 Frequency Divider

4.6.1 Divide-By-16 Prescaler

The divide-by-16 circuit essentially has 4 divide-by-2 blocks cascaded one after another. In experience, the prescaler circuit will waste much more power if it direct operates at 5GHz RF signal without a divide-by-two circuit. The prescaler is actually a high-speed digital circuit, implying that its power consumption is proportion to $C_L V^2 f$. The main trade-off in prescaler design is between speed and power. For low power and high speed consideration, the feedback divide-by-16 prescaler is composed of a pseudo-NMOS type divider and a true-single-phase-clock (TSPC) based frequency divider [23]. The challenge was to design the first divide-by-2 circuits in such a manner so that they will have differential outputs and will be able to divide a frequency of around 5.4 GHz. In order to handle RF signal, the first divide-by-2 circuit apply pseudo-NMOS gates enables high-speed operation while providing large

output swing. The pseudo-NMOS circuits use for a pull-up network only one PMOS as resistive load. The PMOS is operated in the strong inversion region by connecting its gate to ground, resulting in the advantage of reduced load capacitance, less interconnection and smaller area over standard CMOS. For the improved performance, we have to pay the cost of higher leakage current and less noise margin compared to the standard CMOS. Fig. 4.19 shows two pseudo-NMOS D-flip-flop (DFF) whose output are connected back to its inputs to form a ÷ 2 stage. In order to have the inputs vary around the switching threshold of the gates, CLK and CLKB are ac coupled through 0.2pf capacitors. An inverter whose input and output are tied together biases the DFF inputs to the correct dc level over process and temperature. Fig. 4.16 shows the result of the simulation of the divide-by-two circuit. Since the divide-by-two input are differential signal (CLK, CLKB), every differential signal path must match with each other. This means we must be careful when device placement and routing. As shown in Fig. 4.21, layout of this circuit is symmetric when referring to the horizontal centerline.

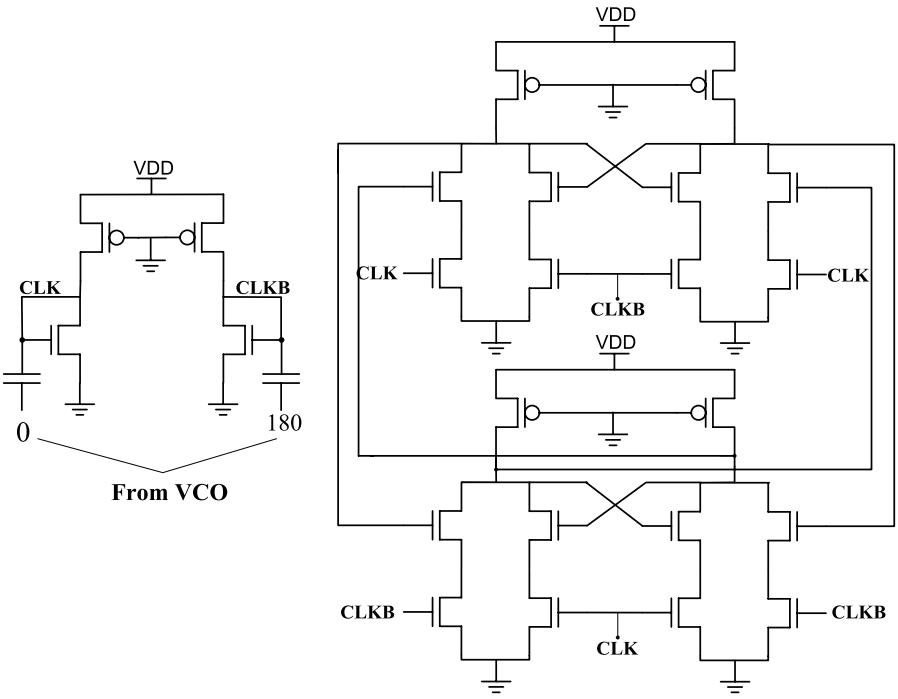
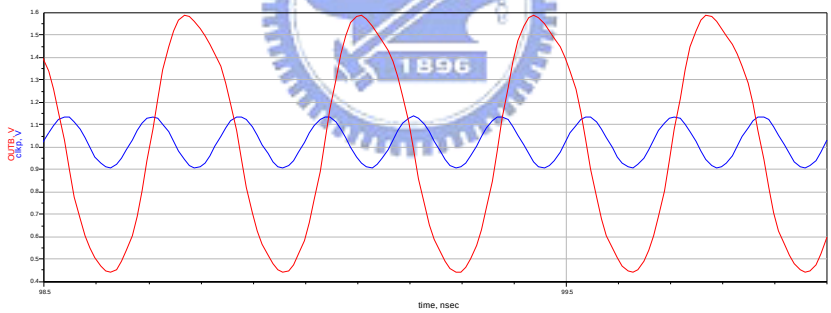


Fig. 4.19. Pseudo-NMOS divide-by-two.



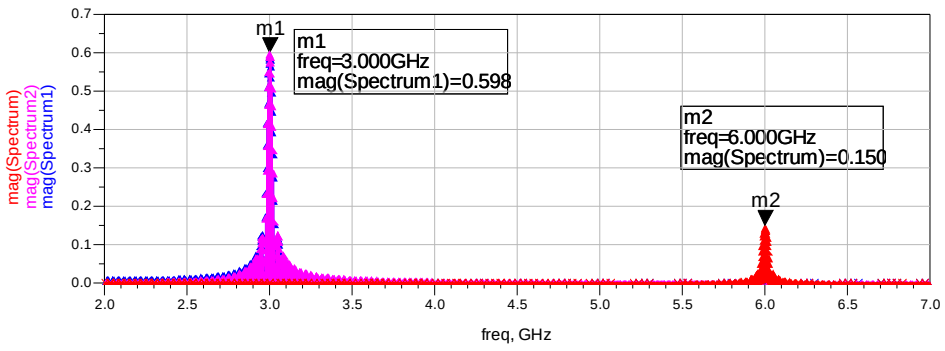


Fig. 4.20 Divide-by-2 circuit simulation output with 6GHz input.

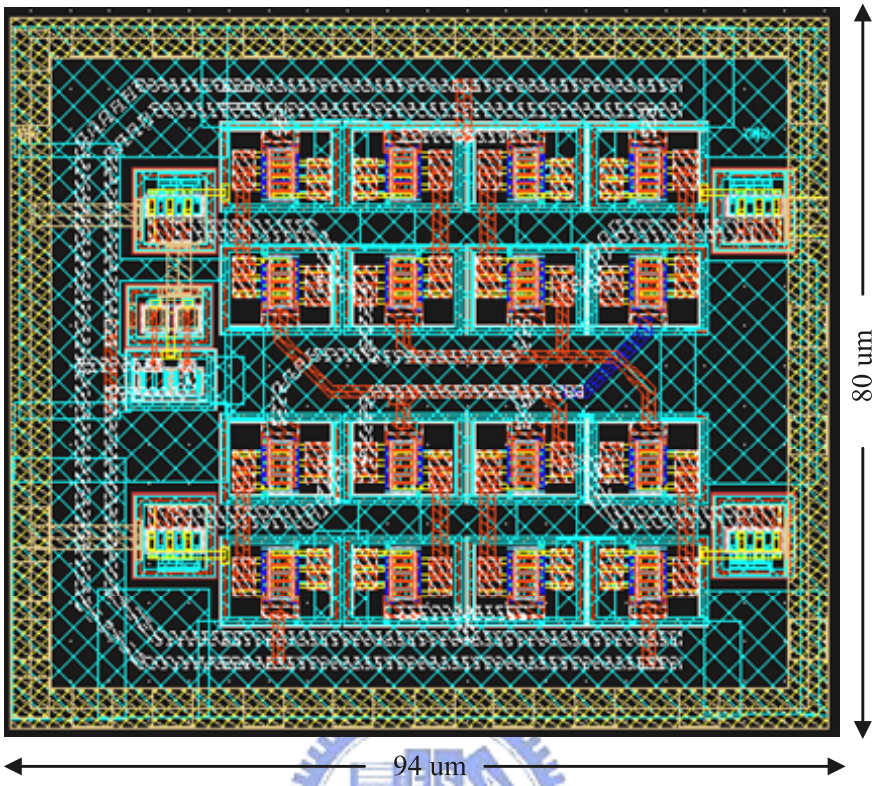


Fig. 4.21. Physical layout of divide-by-two.

Following figure shows the result of the simulation of the divide-by-16 prescaler circuit. It has been calculated that the circuit consumes around 14mA of current. The performance summary of divide-by-16 is listed in Table 4.

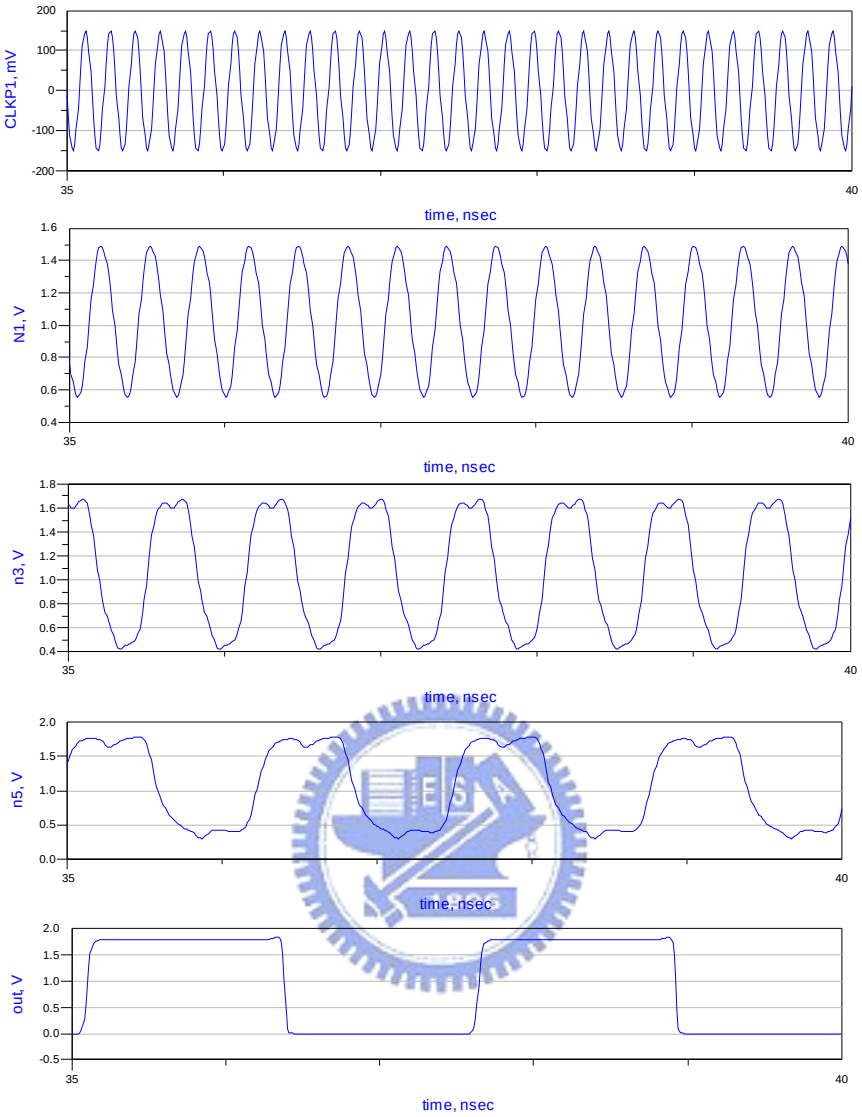


Fig. 4.22. Divide-by-16 circuit simulation output with 6.3 GHz input

Table 4 Performance summary of divide-by-16.

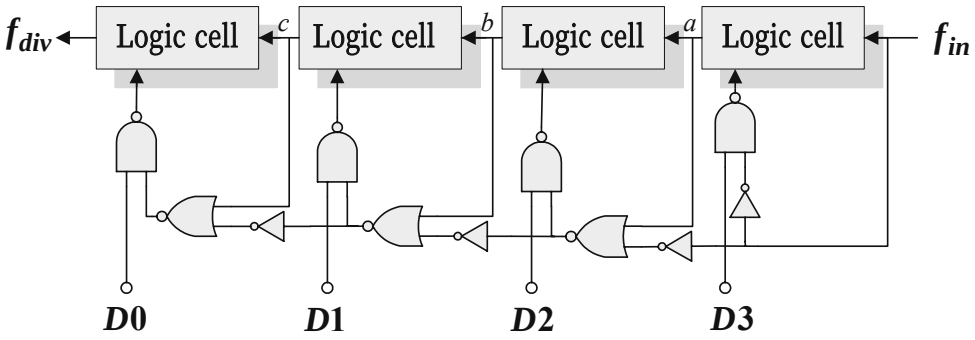
Operation frequency	3GHz
Power consumption	25 mW
Chip area	130×120 um^2

4.6.2 Multi-Modulus Divider

In a MSAH 1-1-1modulator (3-bits output), in order to produce a fractional division ratio of $N = n + \beta$, where 0< β <1, the divider must be capable of dividing by, *n*-3, *n*-2, *n*-1, *n* , *n*+1, *n*+2, *n*+3 *and n*+4 [24] under the control of the delta-sigma modulator output. Thus, to achieve a tuning range from *n*-3 ~ *n*+4, we require an eight modulate (3-bits) from the programmable divider which consist of four asynchronously cascaded dual-modulus-2/3-dividers shown in Fig. 4.23(a). In our design, *n* = 20 and relationship between DSM output, division ratio and control code is shown as Table 5.

Table 5. The relationship between DSM output, division ratio and control code.

Division Ratio	DSM Output	D3	D2	D1	D0
17	-3	0	0	0	1
18	-2	0	0	1	0
19	-1	0	0	1	1
20	0	0	1	0	0
21	1	0	1	0	1
22	2	0	1	1	0
23	3	0	1	1	1
24	4	1	0	0	0



(a)

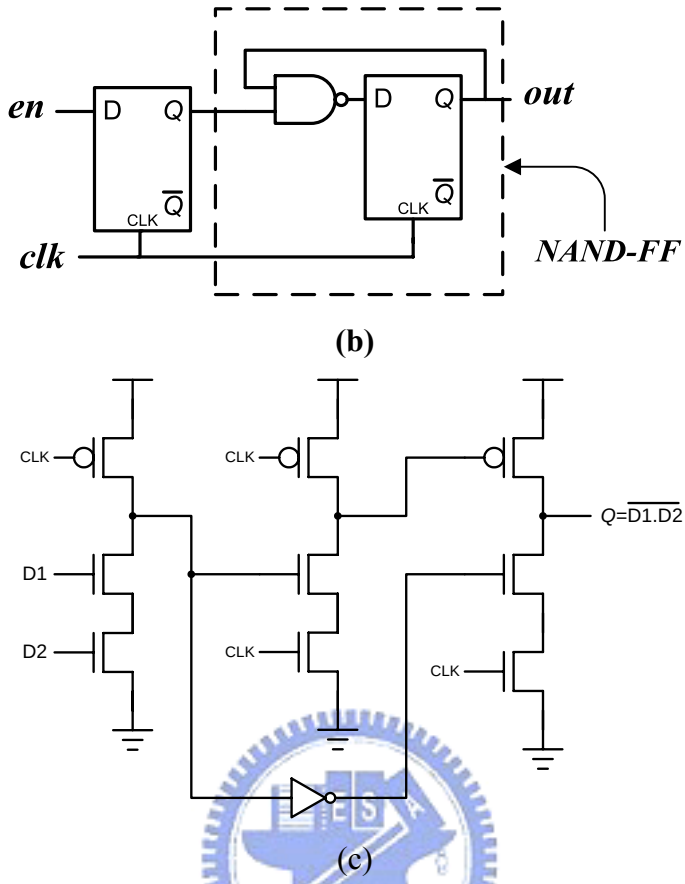
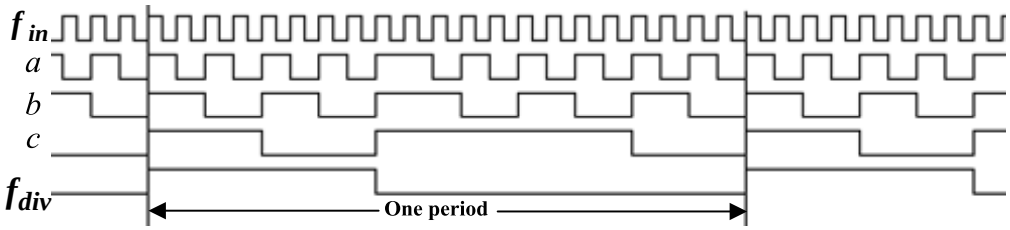


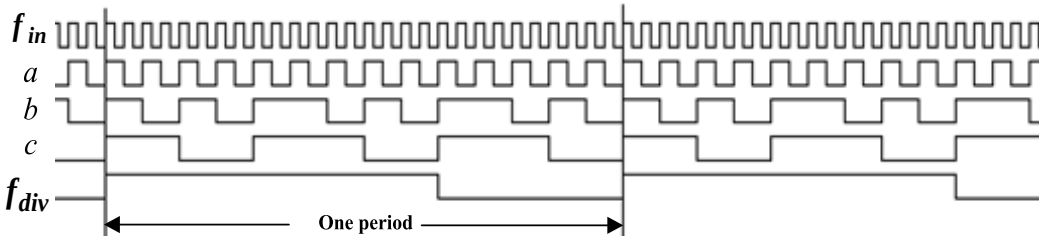
Fig. 4.23. (a) multi-modulus divider (b) Logic cell (c) NAND-FF

The timing diagram of the multi-modulus divider presented as follows are directly controlled by the given control word. In Fig. 4.24, the control word 0101 and 1010 are given and the result is shown in 4.19(a) and 4.19(b), respectively.



(D3, D2, D1, D0 = 0101, divider ratio = 21)

(a)



(D3, D2, D1, D0 = 1010, divider ratio = 26)

(b)

Fig. 4.24 Timing diagram of the multi-modulus divider.

The physical layout of the multi-modulus divider is shown in Fig. 4.25 and the performance is list in Table 6.

Fig. 4.25 Physical layout of multi-modulus divider.

Table 6. Performance summary of multi-modulus divider.

Operation frequency	380MHz
Power consumption	1.8mW
Chip area	213×36 um^2

4.7 Design for Third-Order MASH ΔΣ Modulator

4.7.1 The block diagram of the third-order MASH ΔΣ modulator

The MASH 1-1-1 architecture base on digital accumulators is depicted in Fig. 4.26 [25]. The output of the accumulator is delayed by a latch and fed back to the input of the accumulator as in a delta-sigma modulator. The overflow from the accumulator is usually one bit, i.e., either 0 or 1, so the noise has 8-levels and spreads from -3 to 4 with an average between 0 and 1. The stale input range normalized to the modulus is

from 0 to 1. It's inherently stable. This topology is suitable for pipeline operation for very high clock frequencies.

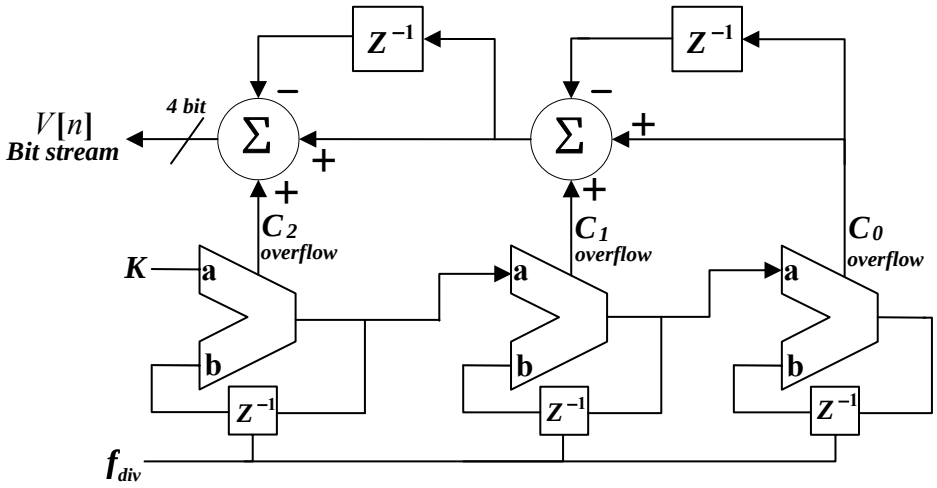


Fig. 4.26. The block diagram of the third-order MASH ΔΣ modulator.

Fig. 4.27 illustrates the circuit realization of the MASH 1-1-1 of Fig. 4.21. Each accumulator employs a pipelined 24-bit adder and a 24-bit register. It can be easily seen that there is a long delay chain between the accumulator overflow outputs, and, therefore, they appear at different time instances. To provide synchronization among the carry overflows, they are captured in 1-bit registers before being forwarded to the error cancellation network. The error cancellation network performs the specific function of canceling the quantization noise from the first two stages and produces a 4-bit wide output.

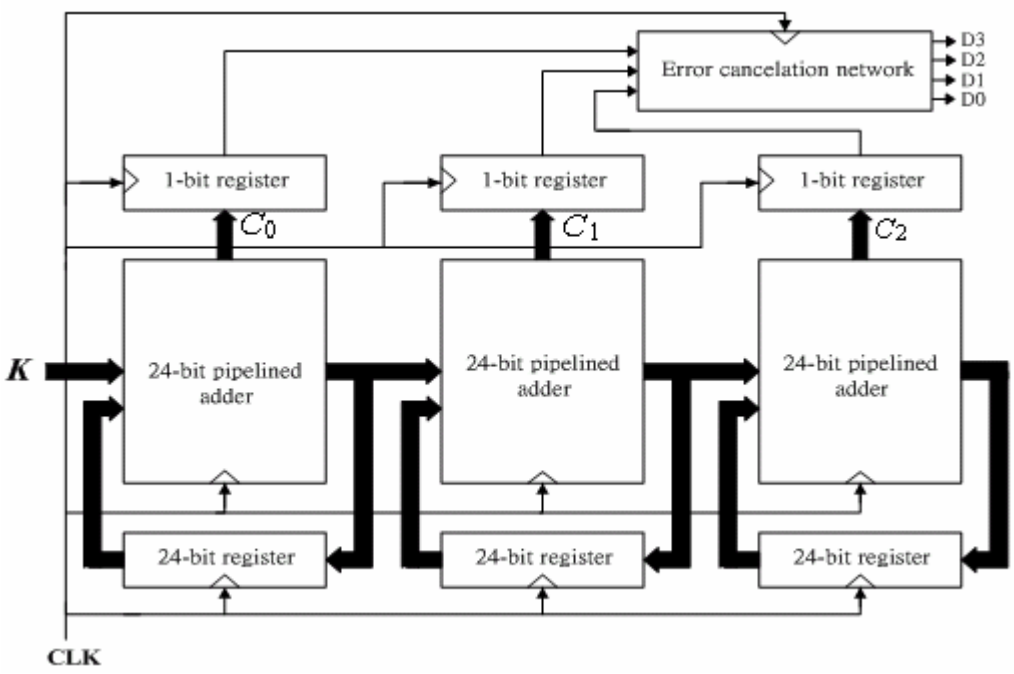


Fig. 4.27. Circuit realization of MASH 1-1-1.

4.7.2 Accumulator Circuit

It should also be noted that in normal pipelined adders, additional registers are required to provide time alignment between the input, delayed carry information, and the output. The bits of both inputs of the adder should be appropriately delayed to synchronize them with the true carry signals. Conversely, the output bits are realigned in time by likewise employing the appropriate delays. Previously, it was reported in [26], that an accumulator is also pipelined in a similar way but without the need of time alignment registers for the second input, since it is taken from the delayed output of the accumulator. A 24-bit example of such a pipelined accumulator is shown in Fig. 4.28. Clearly, this topology operates on general time varying inputs. Since the modulator input is constant for the entire time, the input and output alignment registers can be completely eliminated in Fractional-N frequency synthesis applications. This is because the magnitude of the input to the modulator does not

change with time, and hence, there is no need at all to store the same input bits and their corresponding output bits in the registers for synchronization. Consequently, a pipelined accumulator as shown in Fig. 4.29, without including the time alignment registers at the input and output of the adder, has been successfully utilized in the design of our MASH modulator, resulting in considerable savings in area and power.

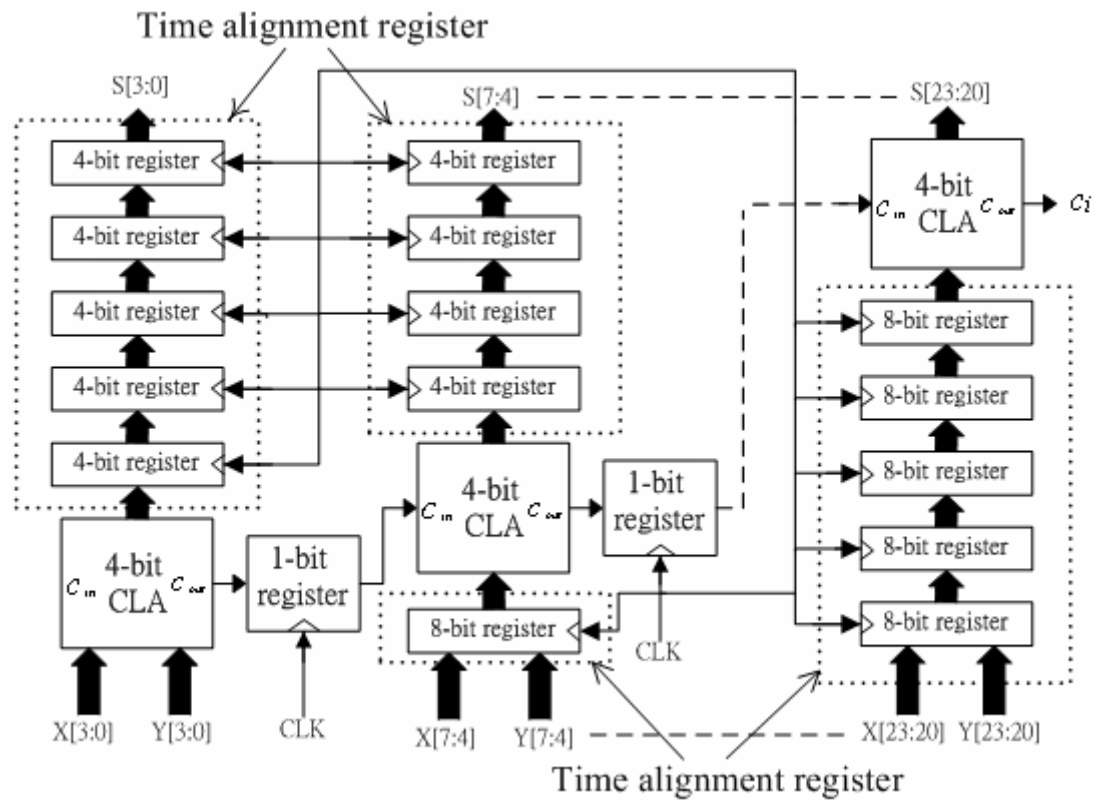


Fig. 4.28. Pipelined accumulator topology.

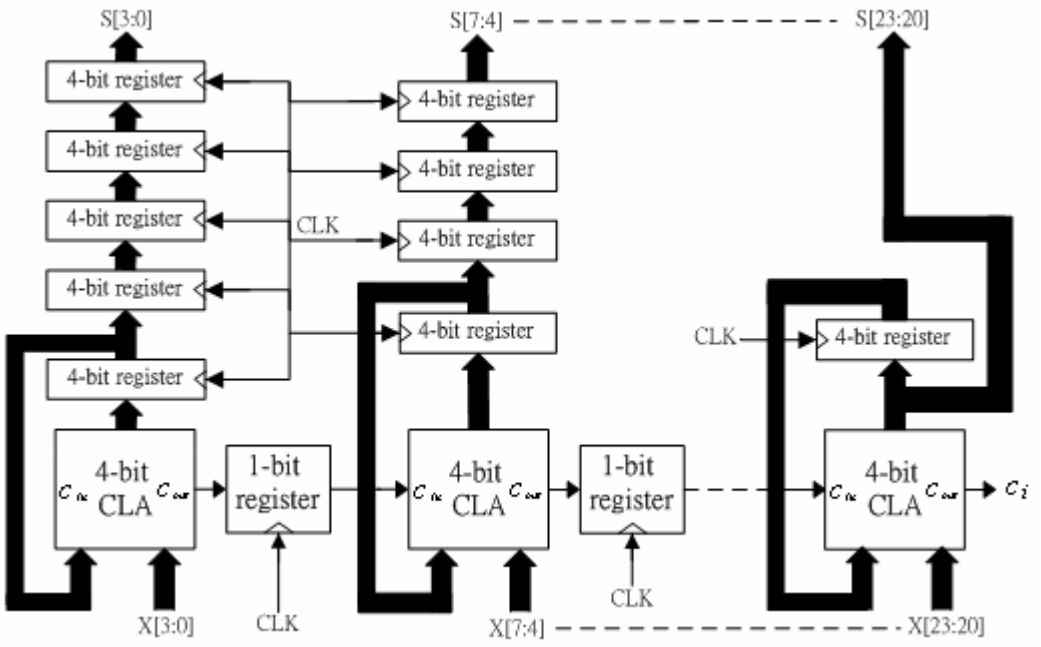


Fig. 4.29. 24-bit pipelined adder for MASH 1-1-1.

4.7.3 Noise Cancellation Network

Fig. 4.30 depicts the logic diagram of the error cancellation network used in the realization of the MASH 1-1-1 of Fig. 4.27. The error cancellation network basically performs the following function

$$V[n]=C_2[n]+C_2[n-2]-2C_2[n-1]+C_1[n]-C_1[n-1]+C_0[n]. \qquad (4\text{-}9)$$

, where C_2, C_1, C_0 are the carry outs of the first, second and third accumulators, respectively. Basically, there are three stages in the error cancellation network. The first stage performs the following operation

$$A[n]=C_2[n]+C_2[n-2]+C_1[n]. \qquad (4\text{-}10)$$

This is accomplished by using a 1-bit two-input carry ripple adder and a simple combinational logic, as shown in Fig. 7. It is clear from the equation (4-10) that can only vary between 0 and +3 and that is why it is necessary to choose a 1-bit adder in

the first stage. In the second stage we desire to perform the $A[n]+B[n]$ operation, where

$$B[n]=-2C_2[n-1]-C_1[n-1]. \tag{4-11}$$

The result obtained in the previous stage (ie., $A[n]$) is directly forward to the second stage by taking the output summation bit and carry of the first stages as the input bits of a 2-bit two-input half adder and a simple combinational logic in this second stage. The third stage is designed to perform one more addition with the $C_1[n]$ to produce the final output.

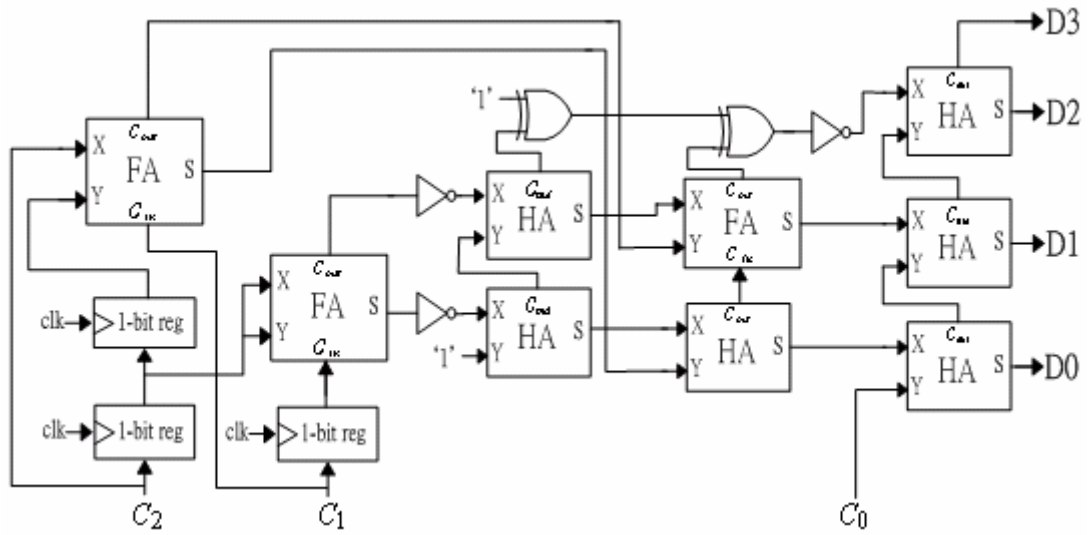


Fig. 4.30. Logic design of error cancellation network.

The output of the MASH is a signed multi-bit (4-bit) number, and two's complement binary number representation was chosen since it allows simple addition and subtraction. However, the 4-bit two's complement system covers the numbers between -8 and +7, while the MASH 1-1-1 produces output levels between -3 and +4. In order to match the requirement, we have coded the output level. The coding table of the MASH output indicating the output bits and their corresponding level is shown

in Table 7.

Table 7. Coding table for the MASH output.

OUTPUT LEVEL	D3	D2	D1	D0
-3	0	0	0	1
-2	0	0	1	0
-1	0	0	1	1
0	0	1	0	0
1	0	1	0	1
2	0	1	1	0
3	0	1	1	1
4	1	0	0	0

4.8 ESD Protection

Electrostatic discharges subject the I/O pins of a semiconductor device to high-voltage, high-current stresses. The stresses can cause long-term reliability problems or catastrophic failure the in I/O circuitry of a chip. ESD protection circuits provide low resistance paths under high-voltage conditions to dissipate the energy in ESD pulses. For 0.18μm process, the voltage limit that gate oxide can tolerate is only about 5V. Without any protection circuit, the MOSFET can be damaged permanently in about 10V potential applied at gate. Fig. 4.31 illustrates the most popular ESD protection circuits in commercial use. Diode chain protection guides the tremendous charge to VDD or GND, and a large gate ground NMOS will break down once a large potential across the VDD and GND, and induces the charge in VDD flows through NMOS to GND.

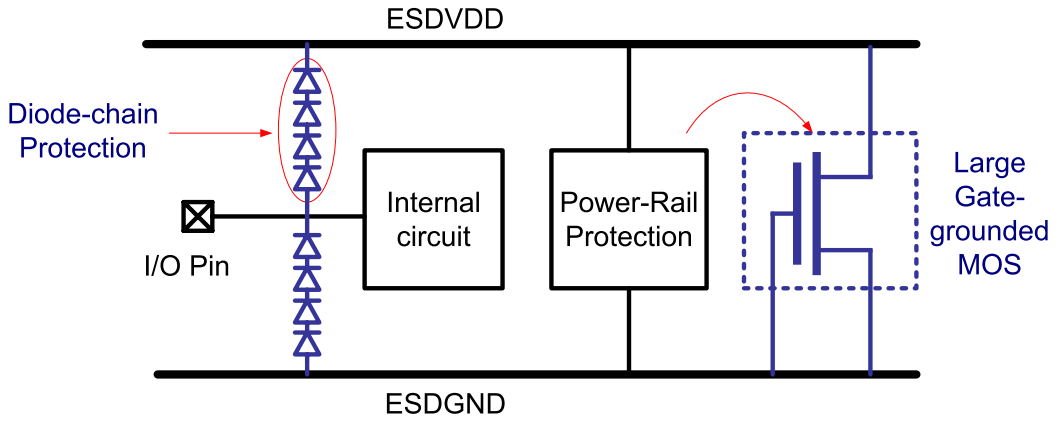


Fig. 4.31 ESD Protection Circuits.

The devices used in ESD own special restrictions. The gate ground MOS shall prevent lightly-doped-drain which is common in deep submicron process. The distance between drain contact and boundary of gate and diffusion must be enlarge too sustain higher static charge. Contacts on guard ring are also prohibited because that makes the break down of ESD device harder. The ESD circuits provided by UMC ensure 3.6kV in human body mode (HBM) test but induce about 40fF nonlinear capacitance in each pad.

4.9 Package Topology

The package used for this design is QFN20D which is produced by SPIL™. The package model for bond-wire is built as Fig 4.32.

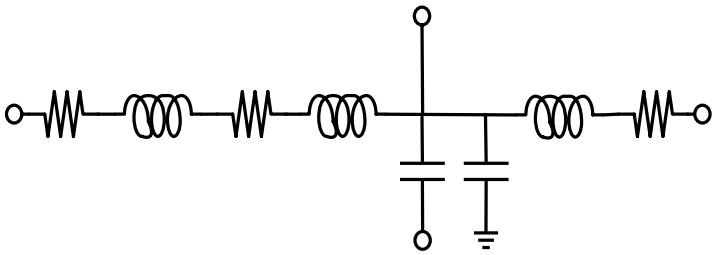


Fig. 4.32 Package Model

The most important issue in bond-wire is serial inductance and parasitic

capacitance between pads. The serial inductance results the DC supply in a non-ideal ac ground while the capacitance between pads causes adjacent pin coupling. The serial inductance is about 1nH/mm with the length of bond-wire and high quality factor compared with on-chip inductor. The model given by SPIL™ explains about 1nH serial inductance for every pin. For DC supply pin, especially VDD and GND, the 1nH parasitic inductor may affect circuit performance or even induce oscillation. So, the more bonds connect with DC supply pin to shunt the inductance smaller is essential. For adjacent pin coupling, a simulation result as Fig. 4.33 shows about -14dB coupling between pads, which is critical to layout design. The signal pads shall be separated as far as possible, and some dc pads such as GND/VDD/Bias must intervene.

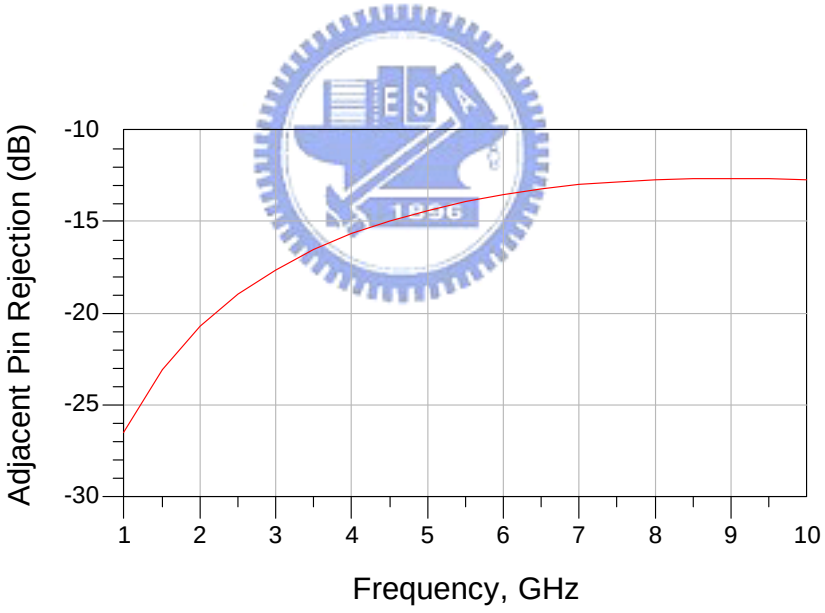
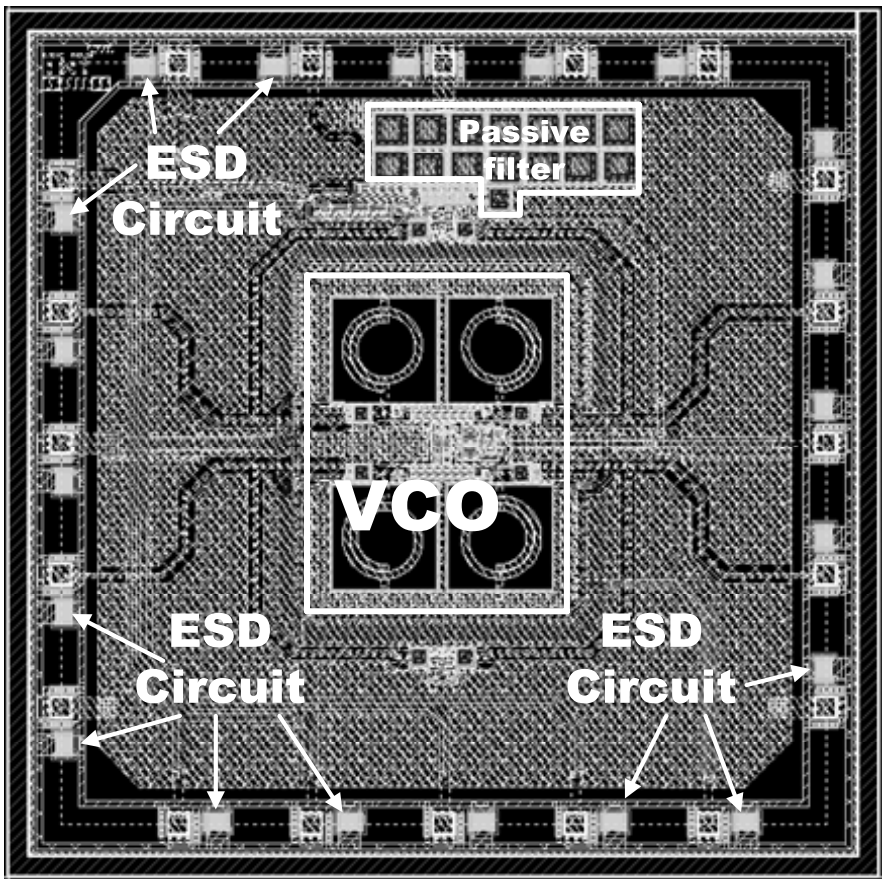


Fig. 4.33 Pin-to-Pin Isolation for Package.

4.10 Integration of Building Blocks

Encircling the die, pads with ESD circuits allocate equally in four sides. The final layout and pin assignment of frequency synthesizer is shown in the Fig. 4.34 and Fig. 4.35, respectively except for the $\Delta\Sigma$ modulator which is implemented in FPGA. All RF signal line is as short as possible to minimize the parasitic capacitance of the signal line. All digital block and RF block have a grounded guarding-ring around them.



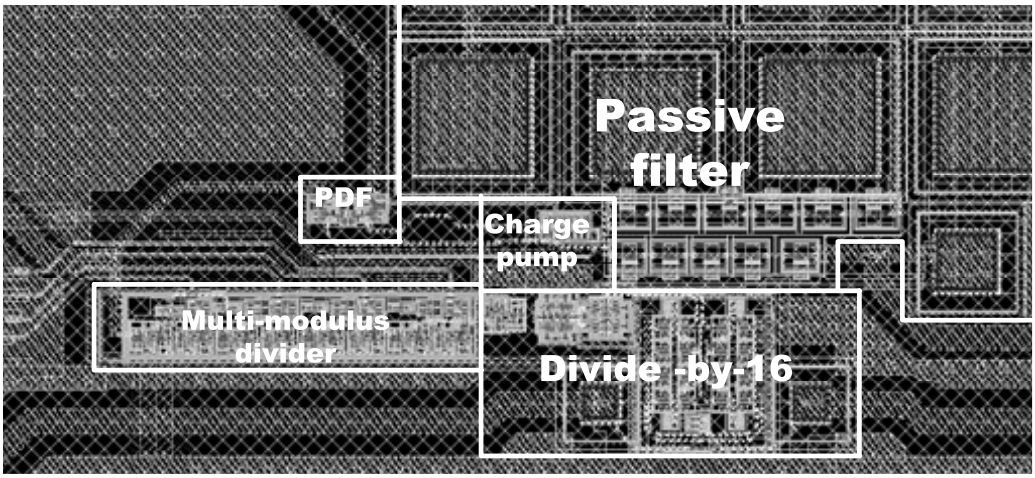


Fig. 4.34. Layout of frequency synthesizer.

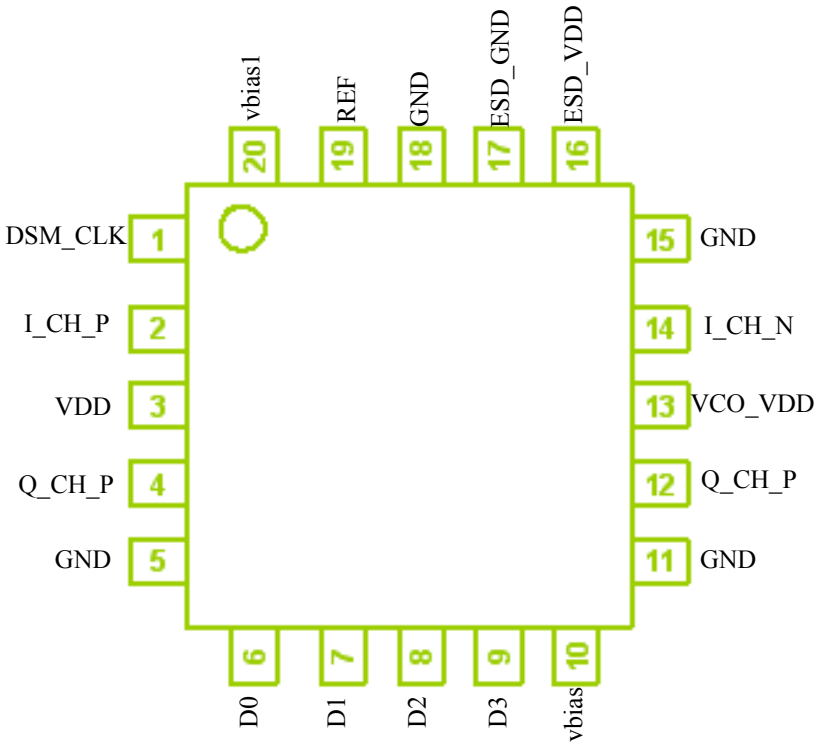


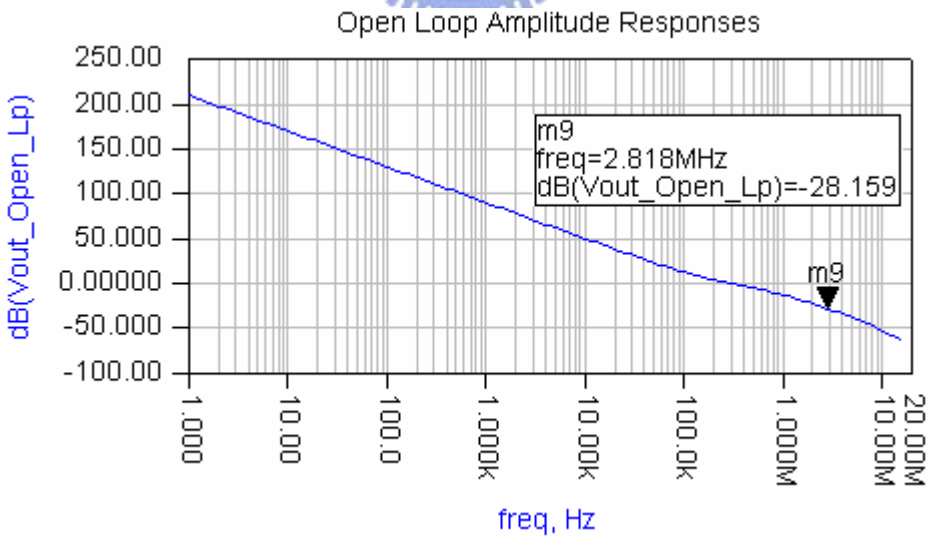
Fig. 4.35. Frequency synthesizer pin assignment.

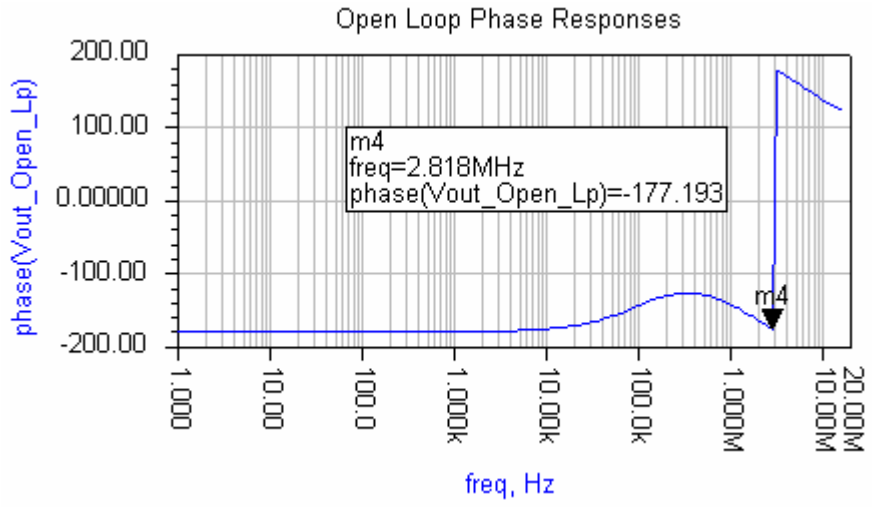
Chapter 5 Behavior Simulation for Frequency Synthesizer

5.1 Open-Loop Analysis

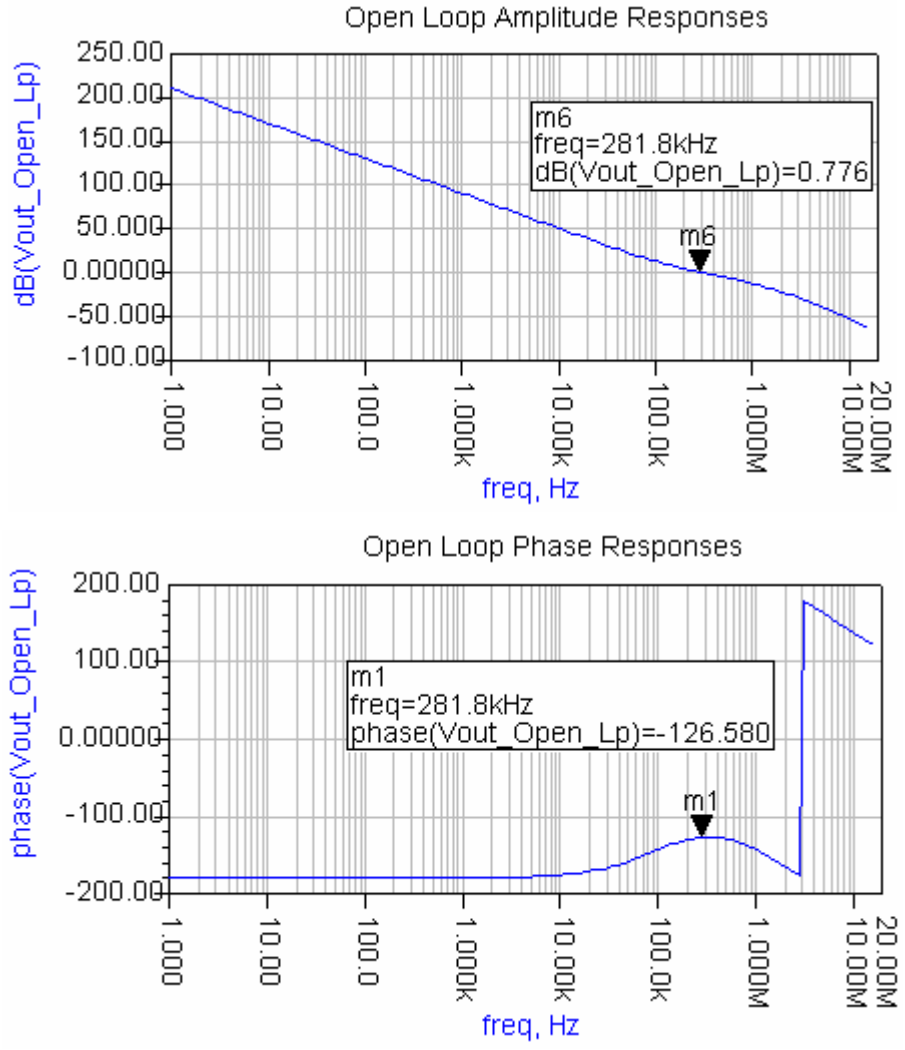
In order to have confidence in the stability of the synthesizer, an open loop analysis is performed to estimate the gain and phase margins. The analysis of theses parameter was performed using the tool of ADS (Advanced design system). From the phase plot in Fig. 5.1(a) we see there is 180° phase shift at ≈2.218MHz. The gain margin is the value at this offset on the gain plot of 5.1(a). In general it is desirable for this value to be greater than 15dB, the reading in this case being ≈29.372dB.

The phase margin is also a measure of relative stability. From the gain plot in Fig. 5.1(b), we can see that 0dB gain occurs at 281.8KHz, which corresponds to a phase margin of 53.4°, phase margin values of ≧45° are usually sufficient.




Open Loop Phase Responses
200.00
100.00
0.00000
-100.00
-200.00
phase(Vout_Open_Lp)
m4
freq=2.818MHz
phase(Vout_Open_Lp)=-177.193
m4
1.000
10.00
100.0
1.000k
10.00k
100.0k
1.000M
10.00M
20.00M
freq, Hz

(a)


Open Loop Amplitude Responses
250.00
200.00
150.00
100.00
50.000
0.00000
-50.000
-100.00
dB(Vout_Open_Lp)
m6
freq=281.8kHz
dB(Vout_Open_Lp)=0.776
m6
1.000
10.00
100.0
1.000k
10.00k
100.0k
1.000M
10.00M
20.00M
freq, Hz
Open Loop Phase Responses
200.00
100.00
0.00000
-100.00
-200.00
phase(Vout_Open_Lp)
m1
freq=281.8kHz
phase(Vout_Open_Lp)=-126.580
m1
1.000
10.00
100.0
1.000k
10.00k
100.0k
1.000M
10.00M
20.00M
freq, Hz

(b)

Fig. 5.1. Bode plots showing open loop gain and phase.

5.2 Closed-Loop Analysis

This was also performed using the tool of ADS, the circuit diagram of which is shown in Fig. 5.2 in which the *Id*, *Kv*, *N* represent the current of charge pump, the gain of VCO and divider respectively. This is a very simple model of a PLL, in fact the open loop analysis was done with the same circuit, with the link back to the phase detector model broken in order to "open" the loop. However, this linear approximation provides an adequate model of a PLL in order to have confidence that the design is close to that required. Fig. 5.3 shows the closed loop frequency response of the synthesizer. The unity gain frequency is ≈281KHz, and the attenuation of the sideband frequency is 64.82dB (the spurious frequency is 16MHz).

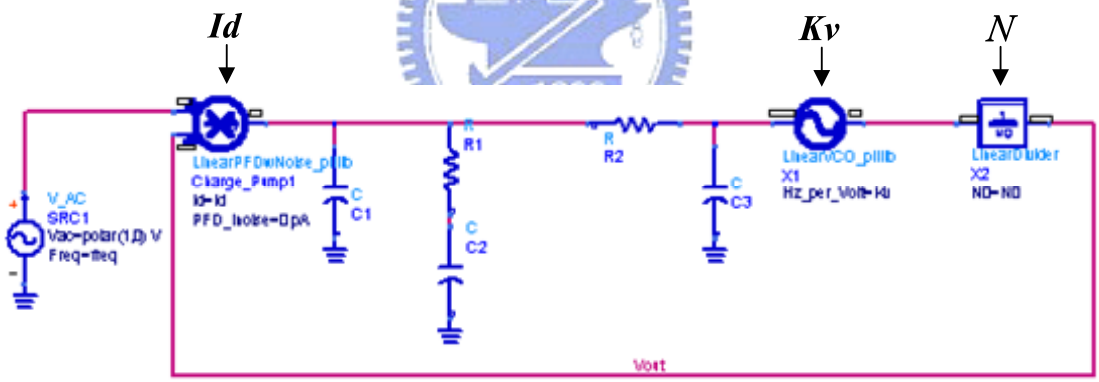


Fig. 5.2. Closed loop simulation of synthesizer.

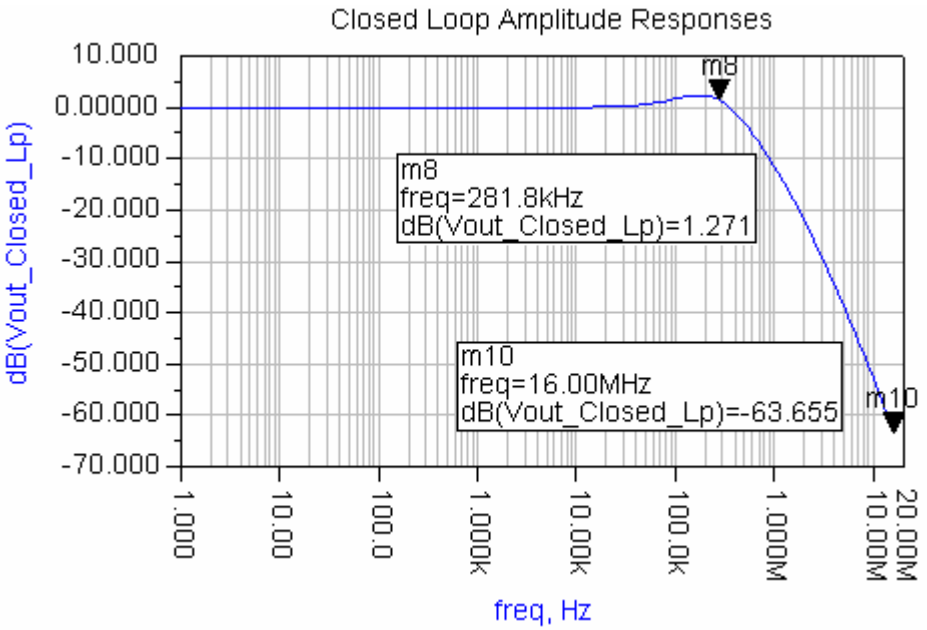
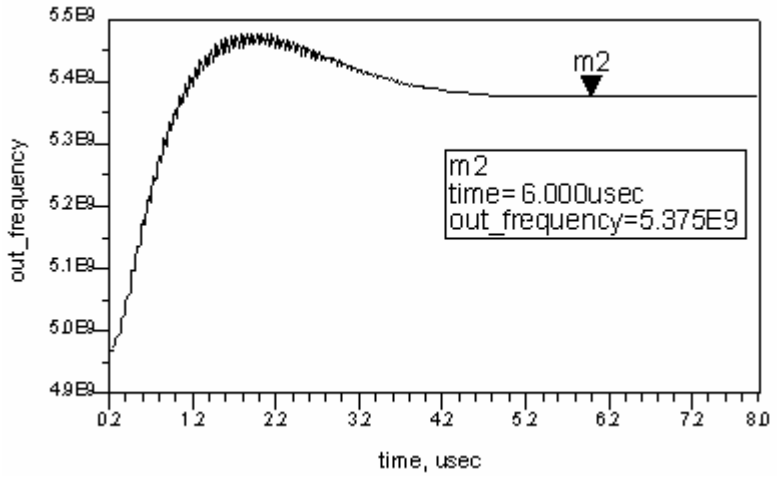


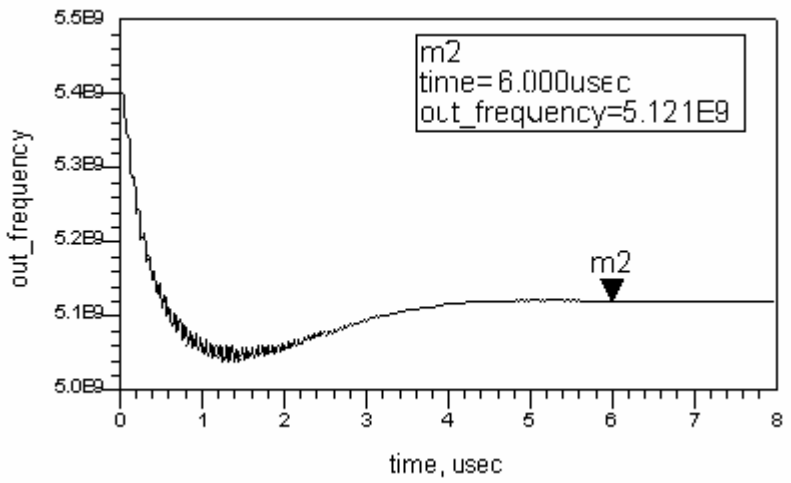
Fig. 5.3. Closed loop frequency response.

5.3 Switching Speed

The locking transient response simulation is shown in Fig. 5.4. The output frequency is from 5.4GHz down to 5.121GHz and the output frequency is from 5.0GHz up to 5.374GHz. We can evaluate the locking time is no more than 6us from the simulation result.



(a)



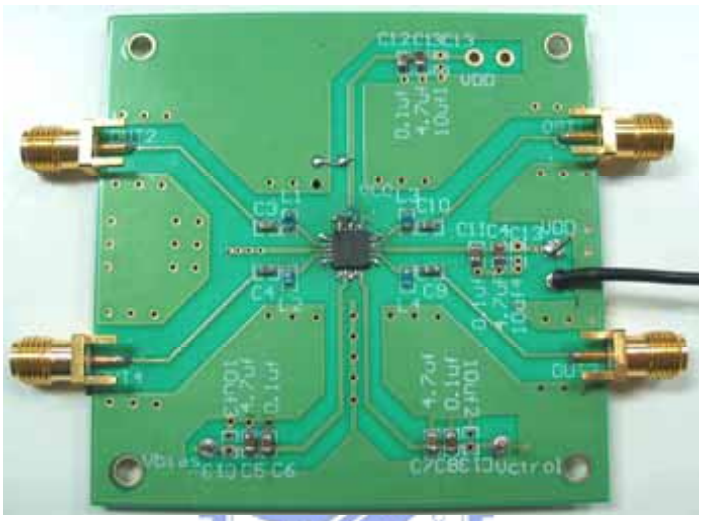
(b)

Fig. 5.4. Worst case lock time characteristics.

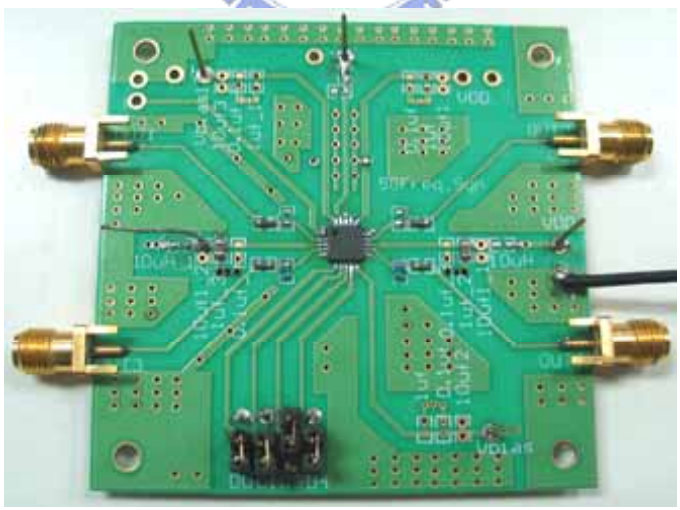
Chapter 6 Measurement Results and Discussions

6.1 Measurement Setup

The designed chip, including the VCO test kit and frequency synthesizer are mounted on the printed circuit board (PCB), respectively and shown in Fig. 6.1.



(a)



(b)

Fig. 6.1 Printed circuit board for (a) VCO test kit (b) frequency synthesizer.

Fig. 6.2 is the instruments setup and overview, including power supplies, spectrum

analyzer, ESG, oscilloscope.

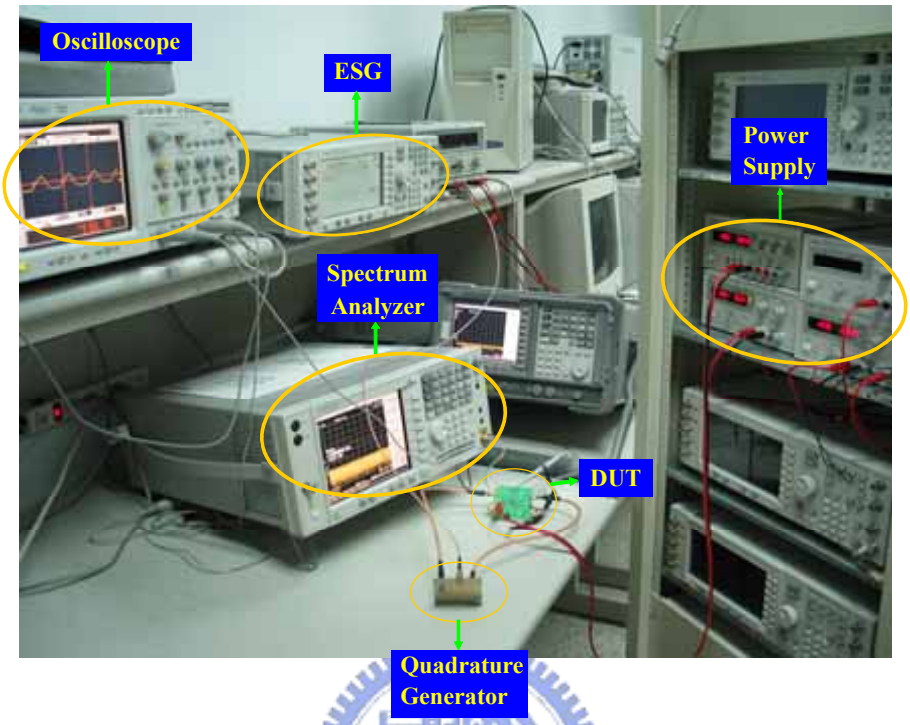


Fig. 6.2 The instruments setup and overview.

6.2 Frequency Divider

The measurement setup for frequency divider and measurement results is shown in Fig. 6.3, Fig. 6.4, respectively. The highest input-frequency of the frequency divider is 5.9GHz.

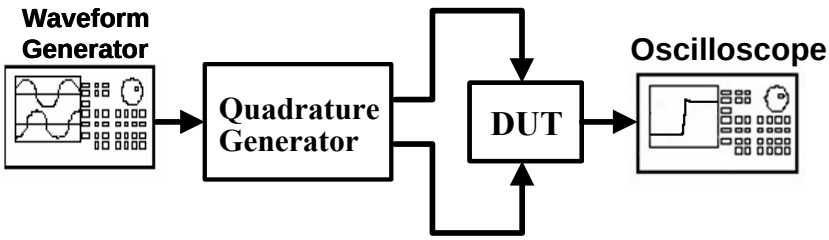
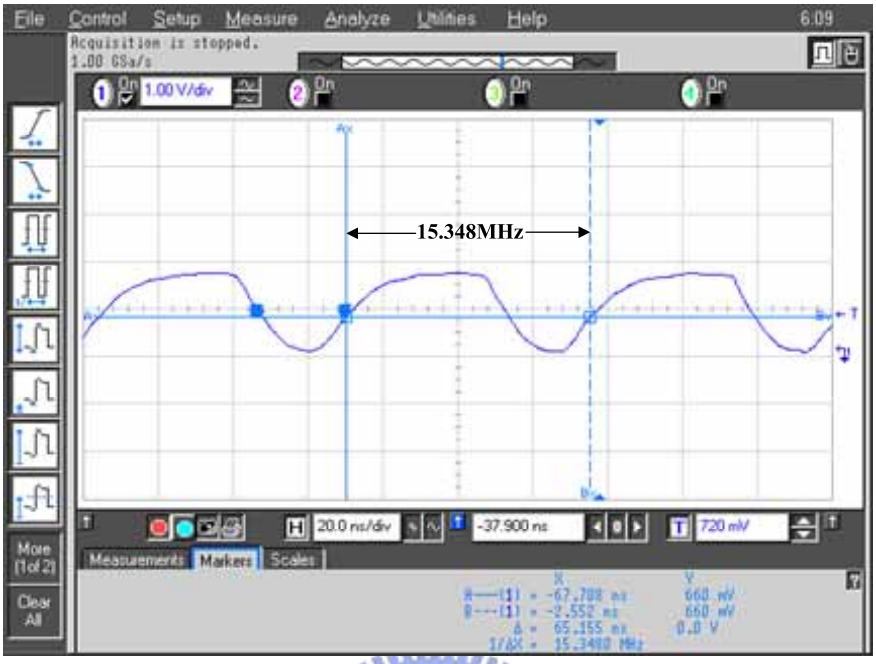
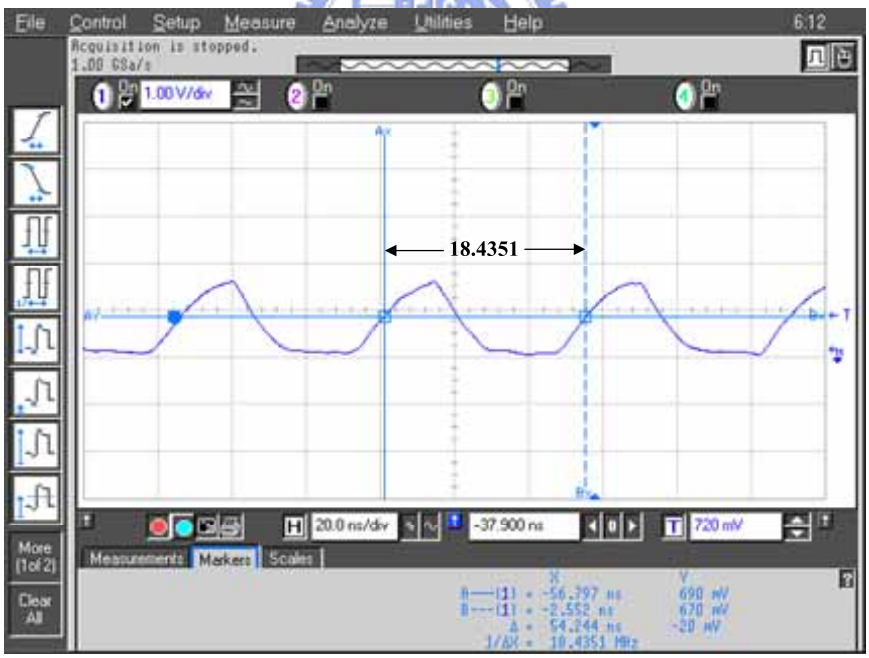


Fig. 6.3 The measurement setup for frequency divider.



(a)



(b)

Fig. 6.4. Measured frequency divider output waveform with 5.9GHz input (a) ÷ 384 (b) ÷320.

6.3 VCO Characteristics

There are some measurement setups for example, for the measurement of VCO, the tuning node should be less noise because of the high sensitivity of this node, besides, the shielding of the chip is required because of avoiding of the noise and spurious tones form environment. There is the diagram of the measurement of VCO as Fig 6.4.

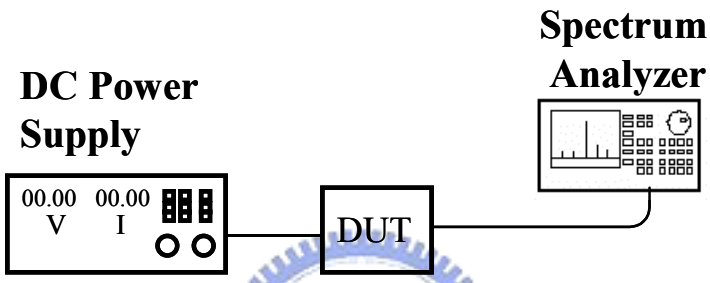
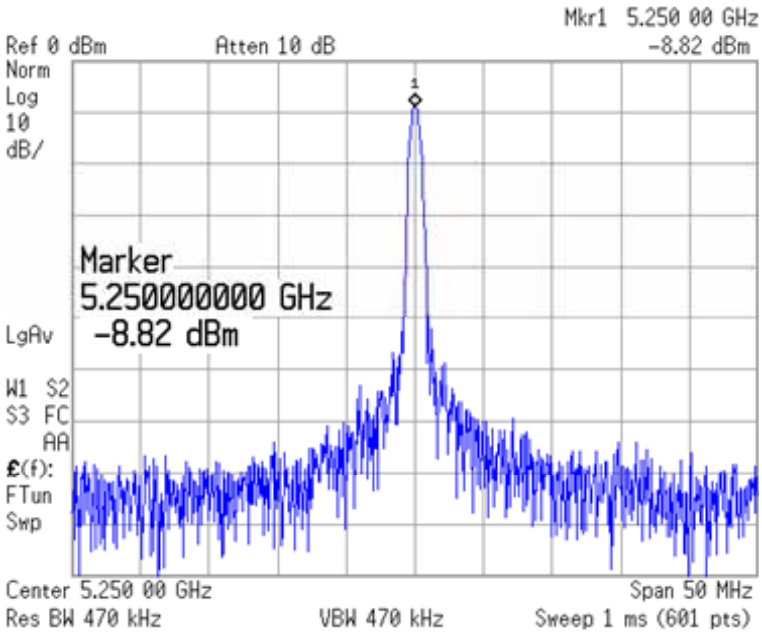
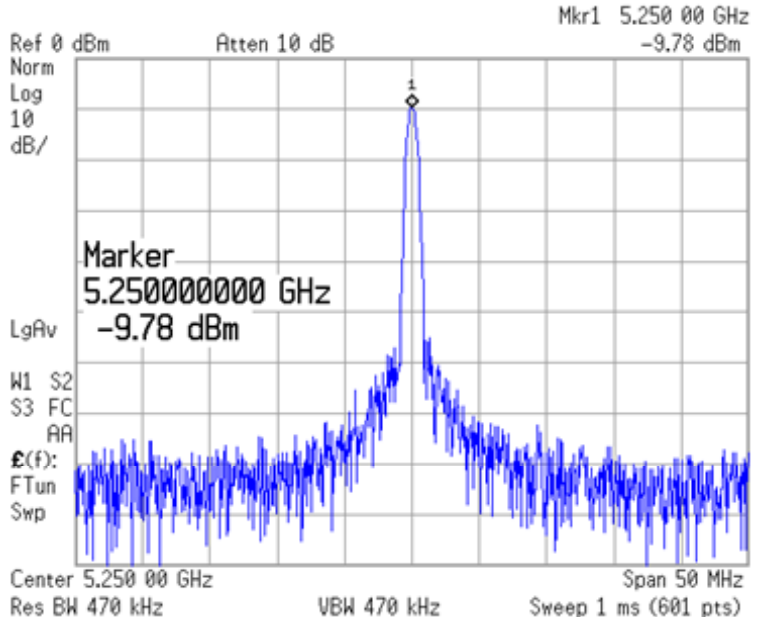


Fig. 6.5 The measurement setup of VCO.

The measured output spectrums are shown in Fig. 6.5, note that the output of I-channel is -8.82dBm and Q-channel is -9.78. There's abut 1dB gain error between them which is the main cause of the cross-coupled pair mismatch of the quadrature VCO. Fig. 6.6 shows the measured tuning range, the measurement result is very close to our simulation curves. The oscillator is tuneable between 4.88~5.436GHz (556MHz tuning range), the maximum K_{VCO} is about 400MHz/V. The measured VCO phase noise is shown in Fig. 6.7. The characteristics of the VCO are summarized in Table 8.



(a)



(b)

Fig. 6.6. Measured VCO output spectrum at 5.25GHz with span=50MHz I-channel (b) Q-channel.

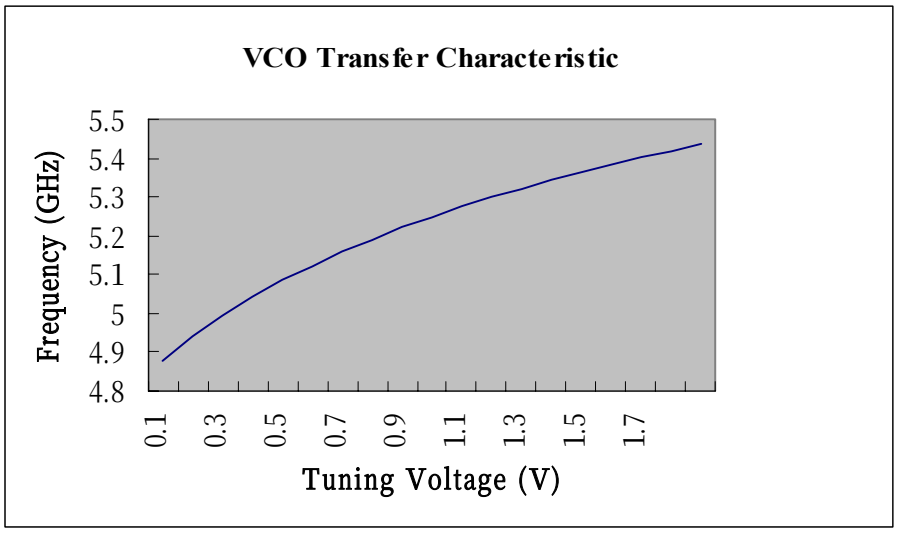
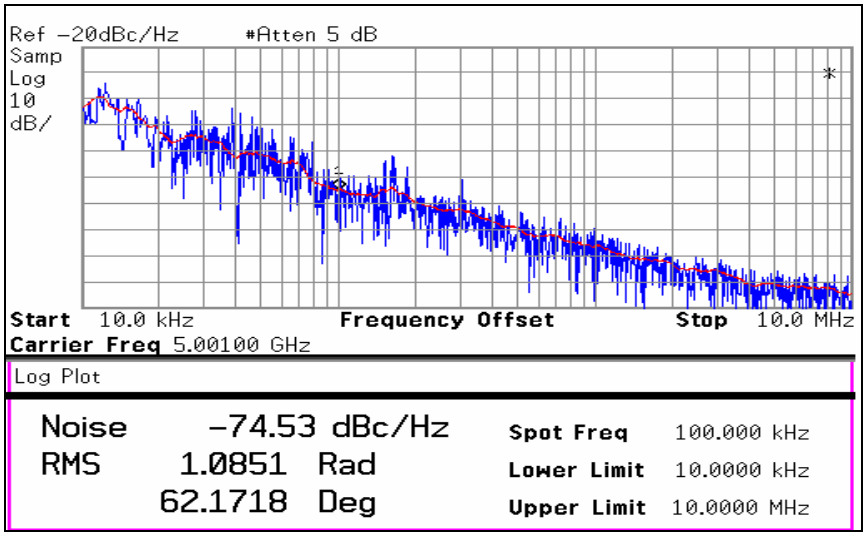
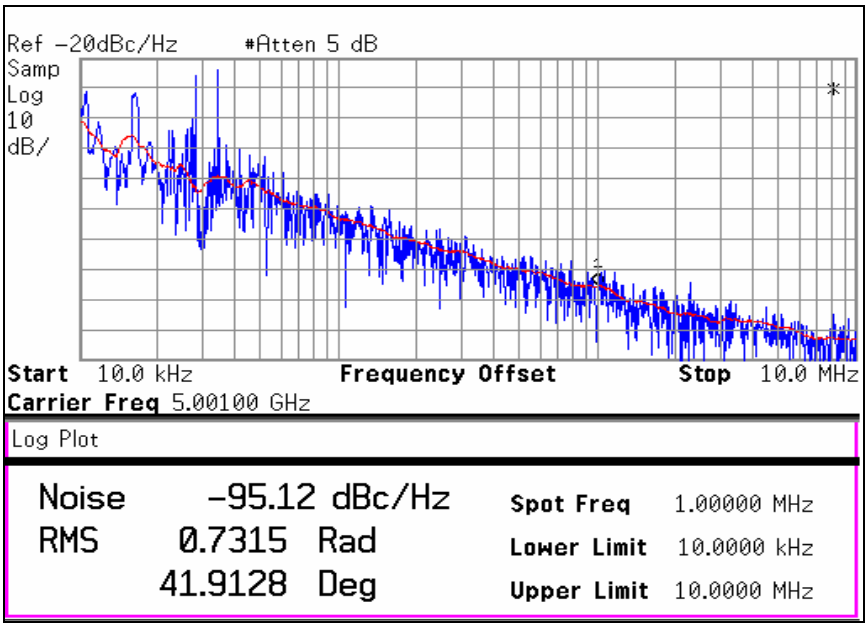


Fig. 6.7. The measured VCO tuning characteristic.



(a)



(b)

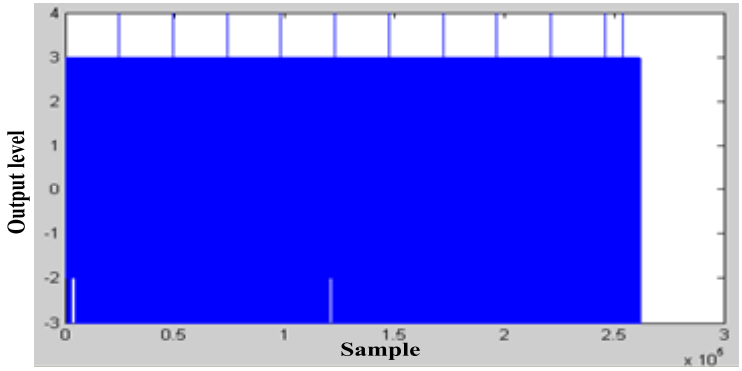
Fig. 6.8. Measured VCO phase noise at offset frequency (a) 100K (b) 1MHz.

Table 8. Summarize the VCO characteristics.

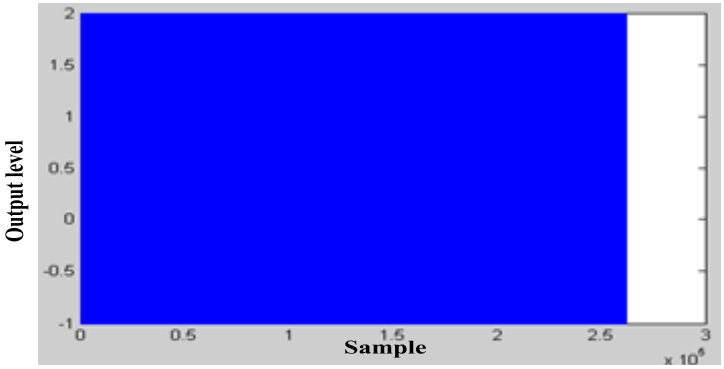
Spec.	Simulation (TT)	Measurement
DC supply voltage	1.8V	1.8V
Varactor type	P+/N-well varactor	P+/N-well varactor
Output Power	-4dBm	-8dBm
Sweep frequency	4.92~5.53GHz	4.88~5.436GHz
Sweep voltage	0V~1.8V	0.1V~1.8V
Turning range	610MHz	556MHz
Maximum VCO gain(Kvco)	450MHz / V	400MHz / V
Phase noise	-92.42@100KHz -113@1MHz	-74.53@100KHz -95.12@1MHz

6.4 Third-Order MASH Delta-Sigma Modulator

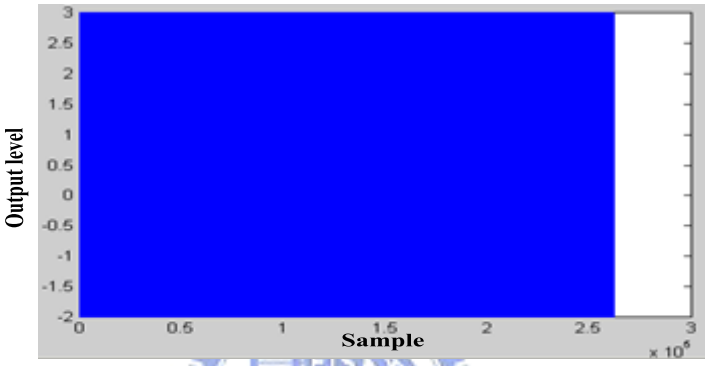
The third-order MASH $\Delta\Sigma$ modulator was measured for all possible values of static input K for 2^{18} samples of modulator output, where a clock frequency of 32 MHz was used. For instance, For a decimal input 4194303, the $\Delta\Sigma$ modulator output level is between -3 to +4 is shown in Fig. 6.8a, which corresponds to 0.25 ($65536/2^{18}$) as a fraction for 2^{18} samples of modulator output the fraction was represented to an accuracy of 99.9999761%. For a decimal input 8388608, the $\Delta\Sigma$ modulator output level is between -1 to +2 is shown in Fig. 6.8b, which corresponds to 0.5 ($131072/2^{18}$) as a fraction for 2^{18} samples of modulator output the fraction was represented to an accuracy of 100%. For a decimal input 12582912, the $\Delta\Sigma$ modulator output level is between -2 to +3 is shown in Fig. 6.8c, which corresponds to 0.75 ($196608/2^{18}$) as a fraction for 2^{18} samples of modulator output the fraction was represented to an accuracy of 100%.



(a)



(b)



(c)

Fig. 6.9. The ΔΣ modulator output level with the values of static input K (a) K = 4194303 (b) K = 8388608 (c) K = 12582912.

Furthermore, these spectra were obtained by (Hanning) windowed 2-point FFT data that was normalized to the single-bit quantization step size, which in our case was one. The measurement results in Fig. 6.9 confirm the 60 dB per decade increase in the spectrum, validating the third-order noise shaping.

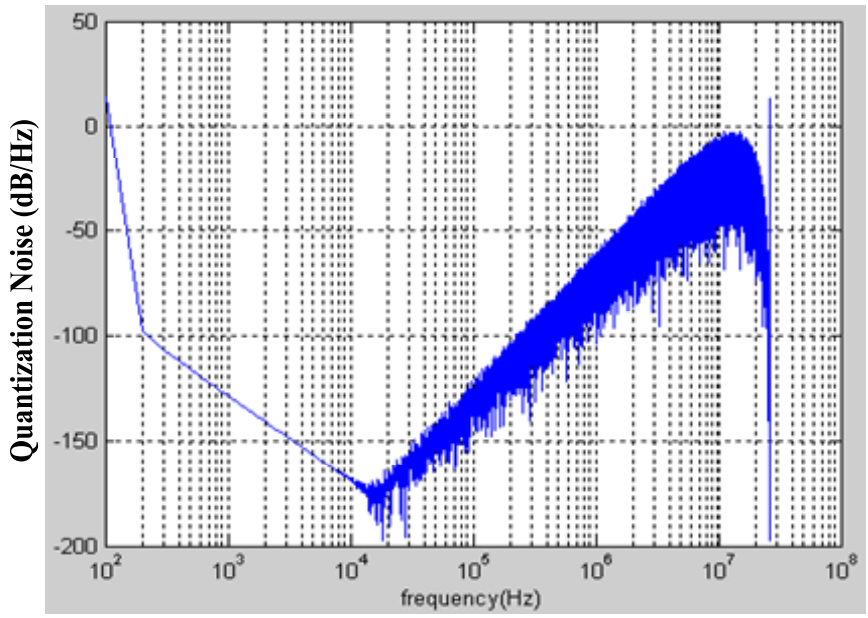


Fig. 6.10. Output spectrum of the third-order delta-sigma modulator.

Table 9 summarizes the performance of proposed synthesizer and some other CMOS frequency synthesizers in recent years for comparison. All of the reported designs are operated at about 5GHz.

Table 9 Recent works of frequency synthesizer at about 5GHz

Author	Ref.[3]	Ref.[4]	Ref.[5]	This work
Power Supply	2.6V	1.5V&2.0V	3.3V	1.8V
Synthesized Frequency	2.6/5.2GHz 5 specing	4.84~4.994 GHz	5.17~5.33 GHz	5.12~5.38 GHz
1'st Stage Prescaler Type	SCL	ILFD	[28]	pseudo-NMOS
Architecture	Integer-N	Integer-N	Integer-N	ΔΣ Fractional-N
Reference frequency	11.5MHz	11MHz	5.875MHz	16MHz
frequency resolution	23.5MHz	22MHz	23.5MHz	16Hz
Locking Time	40us	7.3us	3us	6us
Power Consumption	47mW	25mW	30mW	49mW

Technology	0.4-um CMOS	0.24-um CMOS	0.25-um CMOS	0.18-um CMOS

Note: SCL represent the source-coupled logic.

ILFD represent the injection-locked frequency divider.

From the Table 9, obviously the proposed synthesizer is the only one which can provide fine frequency resolution and meanwhile achieve fast locking time. Furthermore, its phase noise also improved by ΔΣ Fractional-N technology.

Chapter 7 Conclusions and Future Works

7.1 Conclusions

This thesis presents the design of a CMOS ΔΣ fractional-N frequency synthesizer with quadrature phase outputs, which meets the specification for 5.15~5.35GHz frequency band of IEEE 802.11a WLAN applications. The output power is about -5dBm and the phase noise is -112.9 dBc/Hz at the offset frequency 1MHz, the frequency range is about 5120MHz~5376MHz with spacing 16Hz, locking time is about 6 us (simulation result), and total power consumption is about 49mW. The measurement results of this chip show that the VCO tuning range is from 4.88 GHz to 5.436 GHz and the maximum VCO gain is 400MHz/V. The maximum output power is about -8dBm, phase noise is -95.12dBc/Hz at offset frequency 1MHz and the VCO power consumption including output buffer is about 21mW. Regarding to the frequency divider part including prescaler and multi-modulus circuit; the highest input-frequency is 5.9GHz and power consumption is 27mW.

In this thesis also have undertaken the design and FPGA implementation study of a third-order all-digital MASH modulator which operates together with a programmable multi-modulus divider that is be used in this frequency synthesizer. To achieve the desired operation frequency range (16 MHz or higher) while providing low-power dissipation and small area. The pipelining technique was utilized in the design, where the input alignment registers were eliminated by taking advantage of the constant modulator input. The third-order MASH modulator measurement results confirm the 60 dB per decade increase in the spectrum, validating the third-order

noise shaping. Furthermore, for 2^{18} samples of modulator output the fraction was represented to an accuracy of 99.999%.

Over the last years there has been much interest in monolithically transceiver for wireless local area networks, such as 802.11a and 11b [27]. For such multi-standard applications, it is often difficult to cover multiple frequency bands using an integer frequency synthesizer. In order to achieve fine step size to cover the multi-band channel frequencies, one has to lower the reference frequency in an integer-N synthesizer design, which results in high division ratio of the PLL and thus high in-band phase noise. The fractional-N synthesizer allows the PLL to operate with a high reference frequency and meanwhile achieve fine step size. However, this improved performance comes at the penalty of fractional spurious tone. The best solution to remove the fractional spurious components for a synthesizer with fine step size is to employ a delta-sigma noise shaper in the fractional accumulator. The delta-sigma fractional-N architecture will be the best selection for dual-band or multi-band synthesizer designs.

7.2 Future Works

In proposed $\Delta\Sigma$ fractional-N frequency synthesizer, there are still some efforts to do for better system performance. Low power and low phase noise are also important for the wireless local area network (WLAN) applications.

As mention in section 2.1, the spurious tone is one of the important performances in frequency synthesizer. Beside the fractional division, the current mismatch of the charge pump also causes spurious tones. The design of perfect current matching charge pump is importance issue [29], [30].

Dual band or multi-band design is a tendency, for the frequency synthesizer. To cover the desired frequency range, the VCO can be controlled by a binary weighted array of switchable capacitors, with N-bit control, is connected to the resonant tank. The delta-sigma fractional-N architecture can be used for multi-band synthesizer designs with a multi modulus-divider with the wide division range.

Bibliography

[1] IEEE Std 802.11a/D7.0-1999, "Part11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High-speed Physical Layer in the 5GHz Band."

[2] ETSI, "Broadband Radio Access Networks (BRAN); HIPERLAN type 2 technical specification; Physical (PHY) layer," Aug. 1999.

[3] C. Lam and B. Razavi, "A 2.6GHz/5.2GHz frequency synthesizer in 0.4um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, pp. 788-794, May 2000.

[4] H. Rategh, H. Samavati, and T. H. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5GHz wireless LAN receiver," *IEEE J. Solid-State Circuits*, vol. 35, pp. 780-787, May 2000.

[5] X. Yang, T. Wu, and J. McMacken, "A 5GHz fast-switching frequency synthesizer," *IEEE MTT-S International, Microwave Symposium Digest*, Vol. 1 , pp.589-592 June, 2002.

[6] S. Ali and F. Jain, "A low jitter 5.3GHz 0.18um CMOS PLL based frequency synthesizer," *IEEE Radio Frequency Integrated Circuits Symposiums*, pp. 173-176, 2002.

[7] Chih–M. Hung and Kenneth K. O, "A fully integrated 1.5V 5.5GHz CMOS phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 37, pp. 521-525, Apr. 2002.

[8] B. Razavi, Monolithic Phase-Locked Loops and Clock Recovery Circuits:

Theory and Design, *IEEE PRESS*, 1996.

[9] Johan van der Tang, Pepijn van de Ven, D. Kasperkovitz, and Arthur van Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature *LC* oscillator" *IEEE J. Solid-State Circuit,* vol. 37, pp. 657-661, May. 2002.

[10] S.-O. Lee, M. Yoh, J. Lee, and I. Ryu, "A 17mW, 2.5GHz fractional-N frequency synthesizer for CDMA2000," in *Proc. ESSCIRC*'01, 2001.

[11] B. Razavi, *RF Microelectronics*, Pretice-Hall, Inc., 1998.

[12] W.S.Djen, "SA8025 fractional-N synthesizer for 2GHz band applications," Application noet, Philips Semiconductors, 1997.

[13] W. Rhee and A. Ali, "An on-chip phase compensation technique in fractional-N frequency-N frequency synthesis," in *Proc. ISCAS'99*, 1999, pp. 363-366.

[14] V. Reinhardt, "Spur reduction techniques in direct digital synthesizers," in *Proc*. Of *47th Frequency Control Symposium*, 1993, pp. 230-241.

[15] R. Schreier and Y. Yang, "Stability tests for single-bit sigma-delta modulator with second-order FIR noise transfer functions," in Proceedings of the 1992 *IEEE International Symposium Circuits and Systems*, 1992, pp. 1316-1319.

[16] S. Hein and A. Zakhor, "On the stability of interpolative sigma delta modulators," in Proc. ISCAS'91, 1991, pp.1621-1624.

[17] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulaors," *IEEE Trans. of Circuits and System*, vol. 40, no. 8, pp. 461-466, Aug. 1993.

[18] Y. Matsuya, K. Uchimura, A. Lwata, T. Yoshitome, et al, "A 16-bits

Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping" *IEEE journal of Solid State Circuits*, pp, 921-929, Dec. 1987.

[19] Y. Sumi, S. Obote, N. Kitai, R. Furuhashi, H. Ishii, Y. Matsuda, and Y. Fukui, "Dead-zone-less PLL frequency synthesizer by hybrid phase detectors," in *Proc. ISCAS*'99, 1999, pp. 410-414.

[20] C. Hung and Kenneth K.O, "A fully integrated 1.5-V 5.5-GHz CMOS phase-locked loop," *IEEE Journal of Solid-State Circuits*, vol. 37, no 4, April 2002.

[21] M. Tiebout, "Design and optimization of RF CMOS circuits for integrated PLL's and synthesizers," *Analog Circuit Design*, pp.325-337, Kluwer Academic Publishers, 2001.

[22] Chung-Yu Wu and Hong-Sing Kao, "A 1.8GHz CMOS Quadrature Voltage-Controlled Oscillator (VCO) Using the Constant-Current LC Ring Oscillator Structure," *ISCAS'*1998, IV-378~IV-381, 1998.

[23] Jiren Yuan and Christer Svensson, "New Single-clock CMOS latches and flipflops with improved speed and power saving," *IEEE Journal of Solid-State Circuits*, vol. 32, Issue. 1, pp. 62-69, Jan. 1997.

[24] T. P. Kenny, T. A. Riley, N. M. Filiol and M. A. Copeland, "Design and Realization of a digital Modulator for Fractional-N Frequency Synthesis," *IEEE Trans. on Vehicular Tech.*, vol. 48, no. 2, March 1999.

[25] T. A. Riley, M. Copeland and T. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, May 1993, pp. 553-559

[26] M. Perrot, T. Tewksbury, and C. Sodini, "A 27 mW CMOS fractional-N synthesizer using digital compensation for 2.5 Mb/s GFSK modulation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2048–2059, Dec. 1997.

[27] M.Zargari, et al. "A 5-GHz CMOS transceiver for IEEE 802.11a wireless LAN system", *IEEE Journal of Solid-State Circuits*. Vol 37, No. 12, Dec 2002.

[28] R. Y. Chen, "High-speed CMOS frequency divider," *Electronics Letters*, vol. 33, no. 22, pp. 1864-1865, Oct. 1997.

[29] Lizhong Sun, Dale Nelson, "A 1.0V GHz Range 0.13um CMOS Frequency Synthesizer," *IEEE 2001 Custom Integrated Circuits Conference*, pp.327-330.

[30] Thomas H. Lee, Member, *IEEE*, Hirad Samavati and Hamid R. Rategh, "5-GHz CMOS Wireless LANs," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 50, pp. 268-280, NO. 1, Jan 2002.