一個一伏特 2.4-GHz 之改良型兩階式金氧半導體射頻發射器

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摘要

本篇論文主旨在設計一個改良型兩階式 2.4GHz 金氧半導體射頻發射器，此設計除了具有直接昇頻式射頻發射器小面積的優點外，更具有間接昇頻式沒有 LO-pulling 困擾的特性。這是一個應用於 Bluetooth 規格之射頻發射器。這個晶片是使用一標準點 25 微米 1P5M 補式金氧半導體製程，包含了正交相位調變器、四相壓控振盪器及功率放大器。因應低電壓低功率的產品趨勢，此晶片之工作電壓設計為一伏特。此發射器晶片在一伏特工作電壓下，只消耗 52.8 毫安培的電流，且整體面積只佔 1.8 x 1.8 毫米平方。實驗晶片完全整合在標準的 0.25 微米單層多晶矽五層金屬及低阻值基體之互補式金氧半的製程上。由於使用四相正交調變器及四相正交相位輸出之電壓控制振盪器，量測到的本地振盪漏損量、影像拒斥比、二階及三階的失真分別為-37.5 分貝載波、-30.4 分貝載波、-41.0 分貝載波和-50.3 分貝載波。且由於雜訊干擾的抑制設計，其最大雜訊為-38.5 分

貝毫瓦。針對短距離無線通訊應用，此晶片亦整合了功率放大器，由於四相壓控振盪器之螺旋形電感有著較低的品質因數以及 Deep N-well 電晶體的寄生電容效應，此功率放大器輸出功率為-11 分貝毫瓦。經過模擬和實驗證實，本論文中所研發的電路將可應用於一個高整合度、全互補式金氧半製程的無線通訊統之中。如此將可以實現一個低價格、小體積的行動通訊裝備。在未來將針對其他的射頻元件做進一步整合，而成為一個完整的收發器。

A 1-V 2.4-GHz CMOS Transmitter with Improved Two-Step Architecture

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ABSTRACT

A 2.4-GHz transmitter with improved two-step architecture combines the advantages of the direct-conversion transmitter and the two-step transmitter. No LO-pulling and small size are the main features of this transmitter, and it is designed for Bluetooth applications. This proposed chip is fabricated in a standard 0.25μm single-poly-five-metal CMOS process, and it consists of a quadrature modulator, a quadrature VCO, and a power amplifier. For the product trend of low power & low voltage, the transmitter is designed for 1 Voltage power supply. The transmitter chip drains only 52.8mA from a 1 V power supply voltage, and the chip size only 1.8mm x 1.8mm. With the quadrature modulator and VCO structure, the measured LO leakage, image rejection, second-order distortion and third-order distortion of the modulated signal at the output of transmitter achieve –37.5dBc, -30.4dBc, -41.0dBc, and –50.3dBc, respectively, and the out of band maximum emission is –38.5dBm. The power amplifier is also integrated for short-range wireless communications. The

output power is only -11dBm because of the loss coming from the lower quality factor of the VCO's spiral inductor and the parasitical capacitor of the deep N-well NMOS. It is believed that the proposed high performance RF transmitter front-end circuits can be applied to an all-CMOS wireless communication system. Thus low-cost small-size mobile equipment can be implemented. Further research on the integration of other transceiver components will be conducted in the future.

誌　　謝

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謝謝所有關心過我的人。

鄭建祥

九十三年初夏

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INTRODUCTION

1.1BACKGROUND

Today, people can communicate with each other very convenient by the rapidly developed mobile communication systems such as PHS、GSM、and W-CDMA. In the same way, the growing popularity of notebook computers demands high data-rate wireless local area network (LAN) systems. Many existing wireless LAN operate in the 2.4-GHz ISM band. These products can achieve maximum data-rate of 54Mbits/s (802.11g). More and more electronic device will connect each other by Bluetooth and WLAN device. Wireless product will become the dominant product in the future.

There are four important features on the modern product trend. They are low cost, worldwide market supporting, environment protection, and in mobile/portable device. The wireless product is the same, too.

RF transmitter is a key block of wireless communication system. In modern RF mobile transmitter systems, it is a challenge in SOC, which considers the CMOS process, high integration, small size and no discrete component. It should also have the features of low voltage and low LO pulling.

1.2 REVIEW ON TRANSMITTER DESIGN

For process technology, using Si bipolar or GaAs FET technology has implemented several structures of RF transmitter for obtain better high frequency characteristics. Recently, due to the fast development of deep sub micron CMOS technology, it becomes feasible to implement RF transceiver for medium distance wireless communication applications.

For the transmitter architecture, the direct-conversion and two-step transmitter are the main structures, the detail description is listed below.

1.2.1 Conventional Direct-Conversion Transmitter Design

Fig.1 shows the block diagram of the conventional direct-conversion transmitter [1]~[4]. It consists of a modulator, a power amplifier, and a matching network. In this architecture, both modulation and up-conversion are accomplished at the same time by the direct-conversion modulator. The power amplifier provides the required power for transmission.

The main advantages of the conventional direct-conversion transmitter are low power and low cost, due to the simple architecture used. Comparing to the two-step transmitter, which requires two LO signals, the conventional direct-conversion architecture requires only a VCO as a local oscillation. In addition, the outputs of the transmitter and the VCO have the same frequency; the phenomenon of LO pulling

will arise. Huge reductions in LO pulling by the PA can be realized if an offset synthesizer is used instead of an LO operating directly at the desired RF carrier frequency. Recently there has been increasing research interests and efforts on the design of CMOS direct-conversion transmitters.

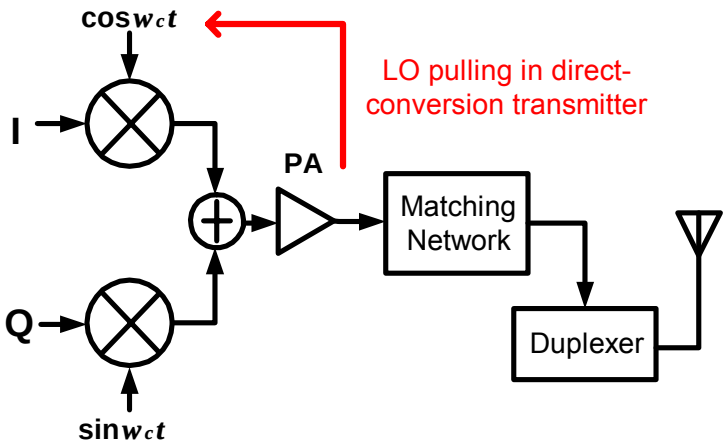


Fig.1 Conventional direct-conversion transmitter

1.2.2 Improved Direct-Conversion Transmitter Design

Fig.2 shows the block diagram of the improved direct-conversion transmitter [5]. It consists of two VCOs, a bandpass filter, a phase splitter, a quadrature modulator, a power amplifier, and a matching network.

Due to the LO pulling being a risk in the conventional direct-conversion transmitter, the improved direct-conversion transmitter uses two VCOs to generate required frequency. The required frequency is far away the LO's frequency, and the LO pulling

problem is solved. The drawback of the structure is that two VCOs and a bandpass filter are required.

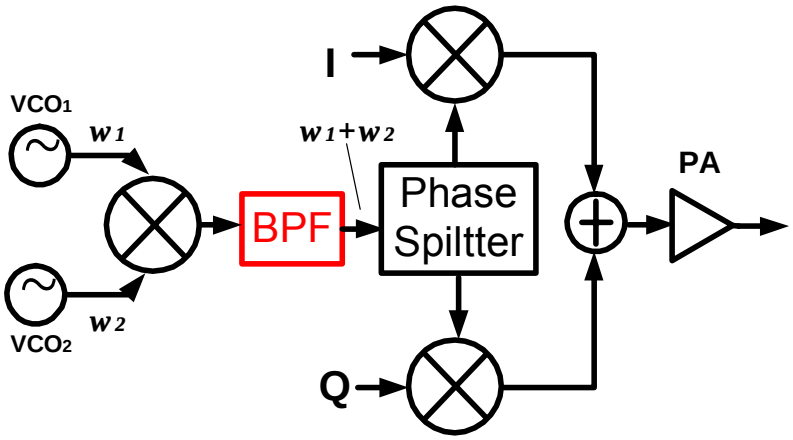


Fig.2 Improved direct-conversion transmitter

1.2.3 Conventional Two-Step Transmitter Design

Fig.3 shows the block diagram of the transmitter with a two-step conversion [6]. The transmitter shown in Fig.3 consists of a modulator, an IF filter, an up-conversion mixer, a RF filter, a power amplifier, and a matching network. The two-step transmitter allows modulation at low frequencies to be converted up to radio frequencies in steps, but requires filters that may be difficult to implement in integrated form. The role of matching network is to provide maximum power transfer to the antenna and filter out-of-band components that result from the nonlinear ties in the modulator and the power amplifier.

In a two-step transmitter, the IF frequency is required; implying that the LO frequency is not equal to the RF frequency; hence, the occurrence of LO pulling

phenomenon will be seldom. Because the frequency of modulator output is low, the VCO can provide high phase accuracy under this operating frequency. The modulator can output high quality modulated signals so that the data rate can be increased. Many transmitters have been designed by using two-step structure to achieve high quality RF signals, but they still suffer several drawbacks such as: 1.) Circuit is more complex, i.e. two LO signals are required in the two-step transmitter. 2.) Power dissipation is increased due to more circuits used. 3.) More off-chip components are required, such as IF filter.

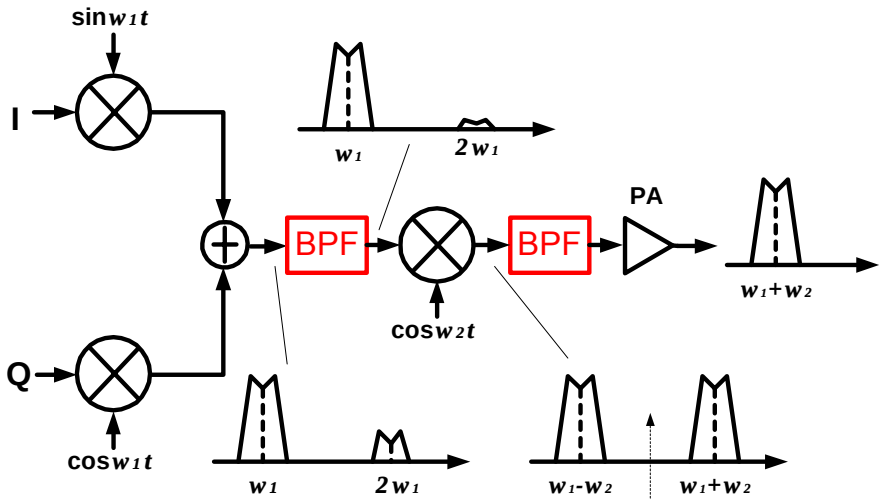


Fig.3 Conventional two-step transmitter

1.2.4 Improved Two-Step Transmitter Design

Fig.4 shows the improved two-step transmitter [7]. The transmitter uses the quadrature structure to suppress the image signals, and then the discrete bandpass filters are not required. But, two LOs are still required.

Due to a shortcoming, I-Q mismatch causes the transmitter unable to reject image signal entirely. Asymmetry on layout, process variation or parasitic degrades the image rejection capability. For mismatch consideration, layout and design strategies are proposed to achieve high performance of image rejection.

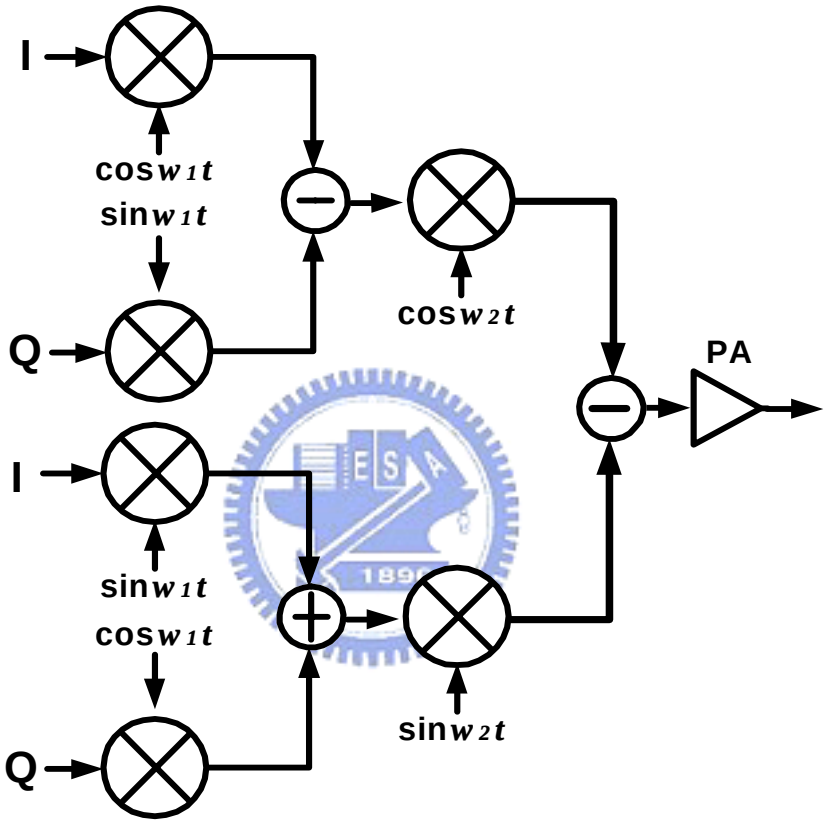


Fig.4 Improved two-step transmitter

1.2.5 Low voltage Design

Equipment consuming low power has become a new trend in circuit design. Extending the sustainability on operating time for battery-based devices is a hot topic

to researchers. The feature is especially expected for portable equipments. Implementing circuits with supplying lower voltage is a familiar way to save power. The way can be realized by more advanced fabrication technology with higher cost. In addition, innovation on design methodology also achieves the purpose. There are two receiver realized with 1-V supply [9], [10]. One performs low power consumption and high integration. The other exhibits high linearity.

For the transmitter, the design of low voltage supply is still a big challenge. The low voltage supply constrains the number of cascaded MOS devices. Each MOS device occupies a DC-voltage drop to sustain working in saturation region. Voltage swing margin is also an essential consideration in analog circuit design. Moreover, maintaining linearity, power gain and noise performance is a big problem in low-voltage design. There are two transmitter realized with 1-V supply [3], [11]. One using distributed circuit performs high efficiency. The other using SOI (Silicon-On-Insulator) process exhibits low power consumption.

One performs low power consumption and high integration. The other exhibits high linearity.

Due to the parasitic capacitor, the low voltage design in transmitter is still difficult. In the present papers, there are four low voltage technology used.

(1) Deep N-well & Substrate bias

For reducing body effect, deep N-well & Substrate bias are used in low voltage design.

(2) Low V_{TH} Device

By process improved, the low V_{TH} device can efficiently reduce the threshold voltage, but the disadvantage is that the device has a big size because its length is longer than the normal MOS device.

(3) DAT (Distributed Active Transformer) [11]

The DAT is implemented in PA design; it uses the active transformer in Input/Output network for efficient power. Due to differential push-pull topology and circuit symmetry, the device can work under low voltage, but the drawback is big size.

(4) SOI (Silicon on insulator) [3]

SOI is a new process technology in preventing the parasitic capacitor effect. It can be used in low voltage, low power design, but the special process is still a drawback.

1.3 MOTIVATION

In this thesis, we want to design a single chip, low-voltage, bluetooth class III CMOS RF transmitter. The improved two-step structure is employed to avoid LO

pulling, and the quadrature structure in the second-stage is employed to eliminate the discrete bandpass filters. Under this structure, we design the IF frequency at the middle of the RF frequency, and only a quadrature VCO is used to reduce the chip area and the power consumption. The quadrature modulator is employed to suppress image signal, and adopting differential circuits reduce the even-order distortion effect. This design of transmitter will base on a 1.2-GHz reused VCO, a two-step quadrature modulator and a power amplifier with 1-V low power technique. 1-V of power supply is used for low-voltage, low-power applications.

1.4 MAIN RESULTS

The man results of the designed transmitter can avoid the LO pulling. In this structure, no discrete bandpass filters are required. The transmitter consumes only 52.8mW and occupies the chip area of 1.8x1.8mm².The functions of 1-V 2.4-GHz transmitter are designed and measured for meeting the required specifications of bluetooth class III. The post-simulation / measurement results are:

(1) Output Power: 0dBm / -11dBm

(2) LO leakage: -44dBc / -37.5dBc

(3) Image rejection: -32.1dBc / -30.4dBc

(4) LO+2BB: -71.9dBc / -41dBc

(5) LO+3BB: -49.9dBc / -50.3dBc

(6) Out of band spurious: -58.2dBm / -56.3dBm (Idle mode)

(7) Out of band spurious: -43.5dBm / -38.5dBm (Operation mode)

1.5 ORGANIZATION OF THIS THESIS

Chapter 1, the background and motivation of this research are presented. The direct-conversion and two-step transmitters are also reviewed on, and the both structures' advantages are compared.

In Chapter 2, the architecture design and the design consideration is proposed. The operational principle and block diagram are also shown; finally, the potential risk and improvement are discussed.

In Chapter 3, the circuit of the transmitter including quadrature VCO, two-step modulator, power amplifier are proposed in Section 3.1, 3.2, and 3.3. Then the whole transmitter is presented in Section 3.4. The last, the simulation results are listed in Section 3.5.

In Chapter 4, the CMOS transmitter layout circuits are described. The chip testing and experimental result are shown in the following subsections.

In Chapter 5, the conclusions and the future works are given.

Chapter2

ARCHITECTURE DESIGN

The design in chapter 2 sets targets that a transmitter working under 1-V voltage supply, meeting bluetooth specification, no LO pulling noise, and being small form factor.

2.1 DESIGN CONSIDERATION

2.1.1 Specifications In Bluetooth

Bluetooth is an important development in the wireless communication systems. The bluetooth standard defines short-range wireless connection between mobile phones, PDA, notebook PC and other portable devices. This technology uses the unlicensed 2.4GHz~2.4835GHz ISM band, and supports a moderate data rate of 1 Mb/s. The data rate is improved to 12Mb/s in Bluetooth 2.0. The modulation scheme is Gaussain binary FSK (GFSK). It has seventy-eight RF channels with 1MHz bandwidth / per channel. It specifies a 2.4-GHz frequency-hopped spread-spectrum system that enables the users to easily connect to a wide range of computing and telecommunication devices. Devices in the distance of ten meters can connect each other by this technique.

There are several specifications of wireless application that our design of RF transmitters must satisfy. First the adjacent channel power ratio (ACPR) which regulates the spurious emissions must be low enough to avoid interfere other channel.

The definition of the Adjacent Channel Power Ratio means the power ratio of the signal channel and the adjacent channel. See Fig.5. In bluetooth v1.0b specification [12], the power level of spurious emissions must below –20dBc in ±550KHz frequency offset. See Table. I

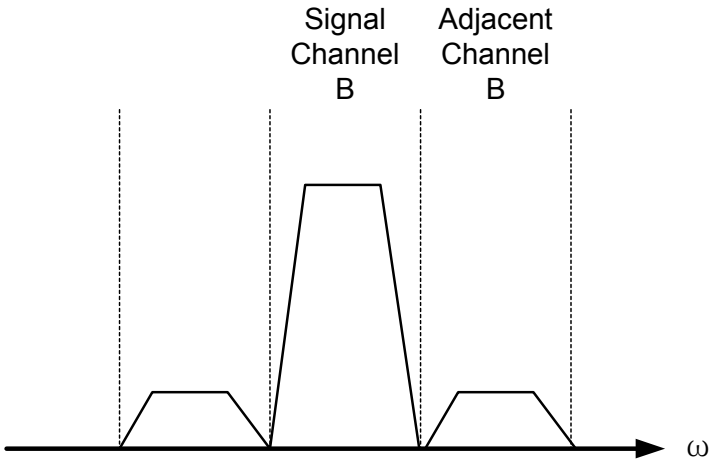


Fig.5 Adjacent channel power ratio

Table I In-band spurious

Frequency offest	**Transmit Power**
±550KHz	-20dBc
$\lvert M - N \rvert = 2$	-20dBm
$\lvert M - N \rvert \geq 3$	-40dBm

In Table I, the transmit spectrum mask for Bluetooth's ACPR is also named as the In-band Spurious Emission. Please see Fig.6. The In-band Spurious Emission is defined in the RF regulations. For the USA, FCC parts 15.247, 15.249, 15.205 and 15.209 are applicable regulations. For Japan, RCR STD-33 applies and, for Europe, ETSI 300 328.

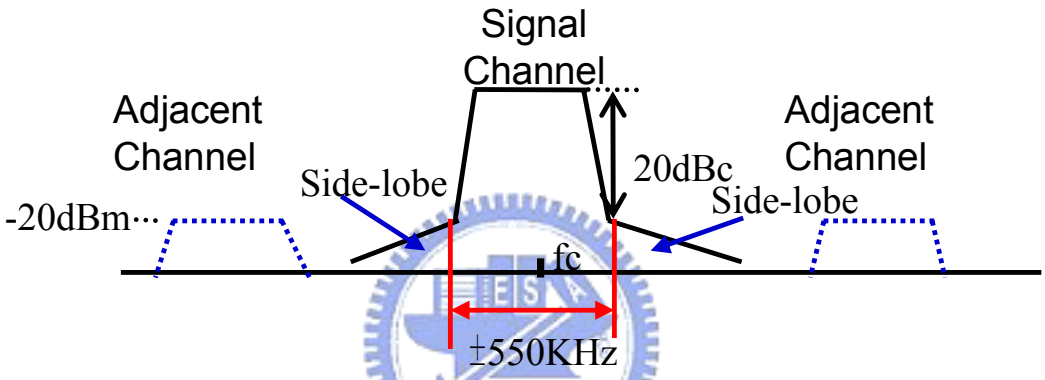


Fig.6 In-band spurious mask

In these regulations, the spurious emission can be divided as the in-band spurious emission and the out-of-band spurious emission. The spurious emission, in-band and out-of-band, is measured with a frequency hopping transmitter hopping on a single frequency; this means that the synthesizer must change frequency between receive slot and transmit slot, but always returns to the same transmit frequency.

For the out-of-band spurious emission, the measured power should be measured in a 100 kHz bandwidth, and the emission requirement can be defined at Table II. Fig.7 is out of band limit.

Table II Out-of-band spurious emission requirement

Frequency band	Operation mode	Idle mode
30-MHz~1-GHz	-36dBm	-57dBm
1-GHz~12.75GHz	-30dBm	-47dBm
1.8-GHz~1.9-GHz	-47dBm	-47dBm
5.15-GHz~5.3-GHz	-47dBm	-47dBm

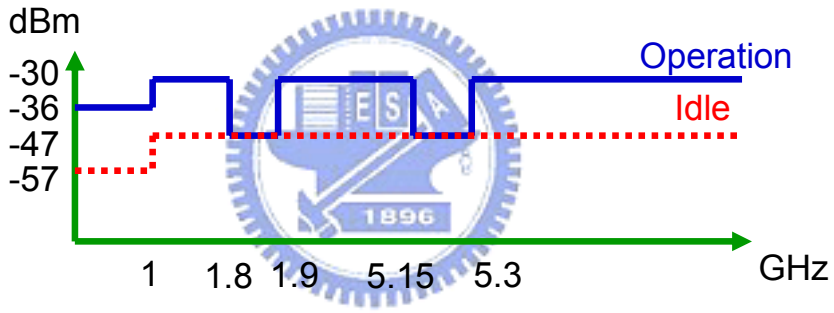


Fig.7 Out of band spurious limit

There are three kinds of power level in the Bluetooth v1.0b. For power class 1, the power amplifier should deliver 20dBm (100mW) output power to the antenna. For power class 2, the power amplifier should deliver 4dBm (2.5mW) output power to the antenna, and for power class 3, the power amplifier should deliver 0dBm (1mW) output power to the antenna. See Table III and Fig.8.

Table III Three power classes of bluetooth

Power class	Maximum output power	Nominal output power	Minimum output power
1	20dBm	N/A	0dBm
2	4dBm	0dBm	-6dBm
3	0dBm	N/A	N/A

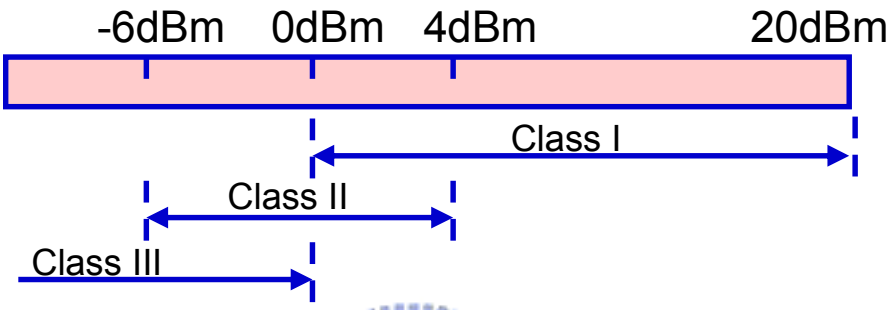


Fig.8 Three power classes of bluetooth

2.1.2 Small Size

To achieve all-in-one chip, the small size is an important key. The two-step structure has good performance, but it has a huge size. Designing a small size of two-step structure has lots of benefits not only on function integration but also on cost requirement.

In this thesis, small size components or reusing architectures are usually applied under this consideration, an even-stage Ring Oscillator is planned to be the quadrature VCO. Even-stage Ring Oscillator using only two spiral inductors for quadrature output has efficiently decreased the chip size. It has the other advantages of low power dissipation, low phase error, and large bandwidth, but high phase noise

[13]-[20].

Another way in reducing size is VCO reuse. The VCO frequency is planned at 1.2GHz. Under two-step configuration, the baseband signals convert up to 1.2GHz, then to 2.4GHz, and the 1.2GHz VCO is reused during both conversions. Please see Fig.9.

The last, two quadrature modulations are applied in baseband to IF band modulator and IF band to RF band modulator. This makes the structure “filterless”

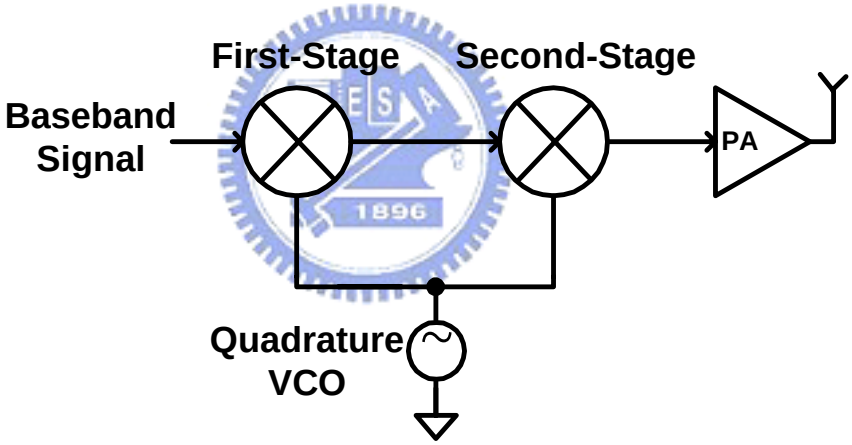


Fig.9 VCO reuse

2.1.3 LO Pulling Avoiding

The power amplifier is the most power hungry device in RF transceiver, so the efficiency of PA must be good enough to reduce power dissipation. In SOC design consideration, the direct-conversion structure of transmitter is a good solution for

reducing chip size, but the main issue in the implementation of direct-conversion transmitters is “LO pulling” or “injection locking” problem, which is a phenomenon that the frequency of the local oscillator is influenced by the power amplifier. As show in Fig.10, this issue arises because the power amplifier output is a spectrum close to the LO frequency with high power, and when the power of the leakage of PA output to oscillator is higher than a level, the LO frequency will be injected and locked by the power amplifier output frequency, a wrong frequency for LO.

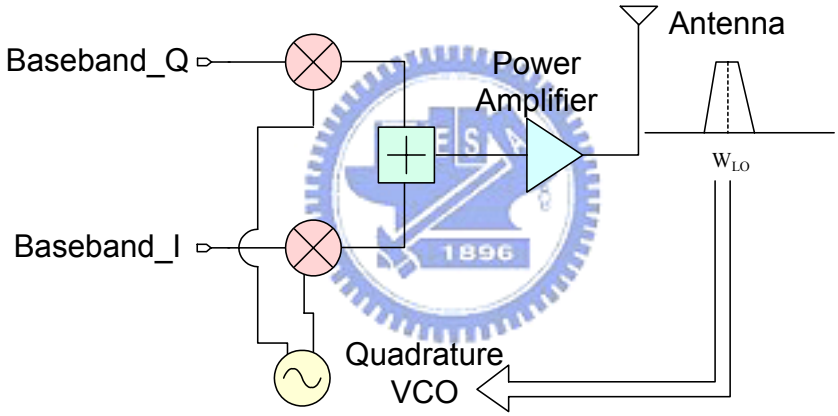


Fig.10 LO pulling phenomenon

It is a trade-off between chip size and noise interference. Two-step transmitter can relax the “LO pulling” problem but it has a large size. In our design, two-step structure can be performed for avoiding LO pulling.

In this thesis, a 1.2-GHz VCO is designed. We set the LO at 1.2GHz to get the best solution of LO pulling among all two-step transmitters. See Fig.11. The LO frequency is 1.2-GHz, the baseband signals up-convert to the IF signals. The IF

frequency is 1.2-GHz. The IF signals up-convert to the RF signals. The RF frequency is 2.4-GHz. The 1.2GHz VCO can be interfered the less by the 2.4GHz power amplifier.

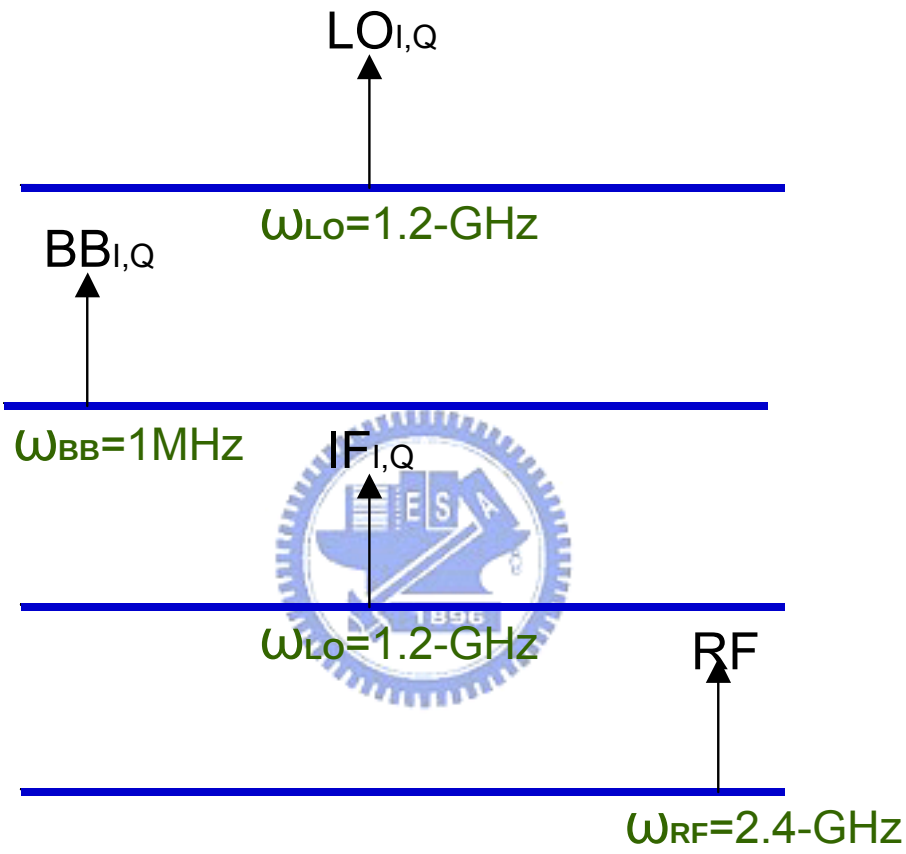


Fig.11 The Frequency plan of the transmitter

2.1.4 Less Noise

First, because the main noise feedback and couple path is the substrate in CMOS technique, the power amplifier is designed to be a fully differential architecture to alleviate the substrate-coupling phenomenon. The substrate noise frequency is twice

the operating frequency in a fully differential configuration, resulting in a reduced interference [21]. See Fig.9.The Fig.12 shows a simple differential amplifier. When the operating frequency of Vin+ and Vin- is fs, the frequency of substrate noise at node S is 2fs.

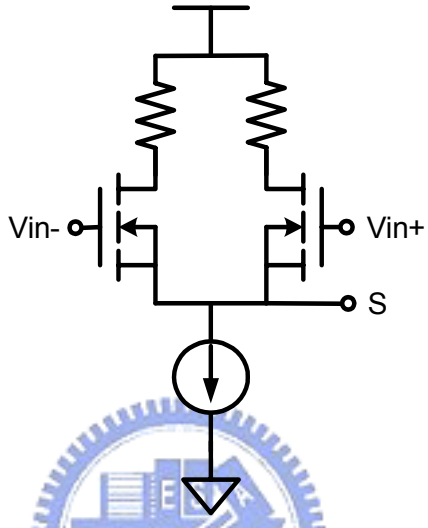


Fig.12 Simple differential amplifier

Second, the double guard ring and deep-Nwell techniques are used. The technique is often used in a mix-mode IC layout technique to isolate the analog circuits and digital circuits. We use the double guard ring and deep-Nwell to be a shield for separating the local oscillator, mixer, and power amplifier.

The last, three kinds of independent power-ground systems in VCO, mixer, and PA are applied for noise isolation.

2.2 DESIGN STRUCTURE AND OPERATIONAL PRINCIPLE

2.2.1 Design Structure

"A 1V 2.4GHz CMOS RF Transmitter With Improved Two-Step Architecture" is designed. The block diagram is shown on Fig.13.

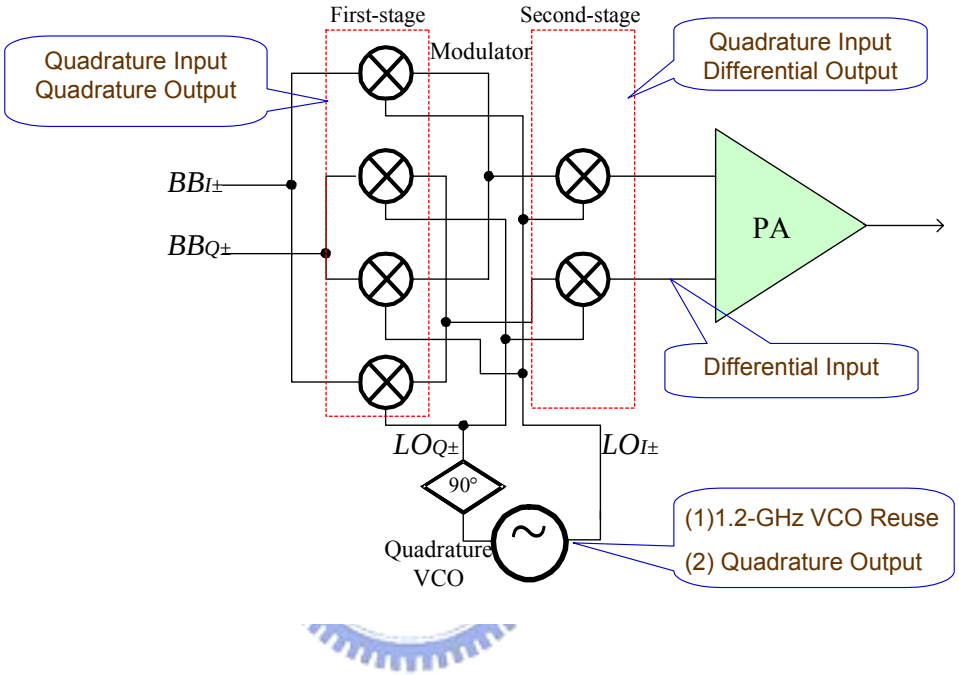


Fig.13 Block diagram

It contains one quadrature VCO, one two-step modulator, and one power amplifier. The quadrature VCO have four phase-shift signals: 0°., 90°, 180°, 270°, which work as carry frequency to be converted the baseband signals twice. The two-step modulator consists of the first-stage modulator and the second-stage modulator. The first-stage modulator accepts four input baseband signals and four LO signals, then converts to four IF output signals. The four IF output signals is still kept as four phase-shift signals: 0°., 90°, 180°, 270°. The second-step modulator receives the

IF signals and four LO signals, then converts to RF differential output pair. The power amplifier gets the differential signals and provides maximum power to the antenna.

2.2.2 Operational Principle

◆ *Quadrature VCO*

The block diagram of proposed new quadrature VCO is shown in Fig.14 where the fully differential ring oscillator plus two LC-tank loads L1C1and L2C2 are used in conjunction with two negative resistors -R1 and -R2 to generate quadrature output waveforms.

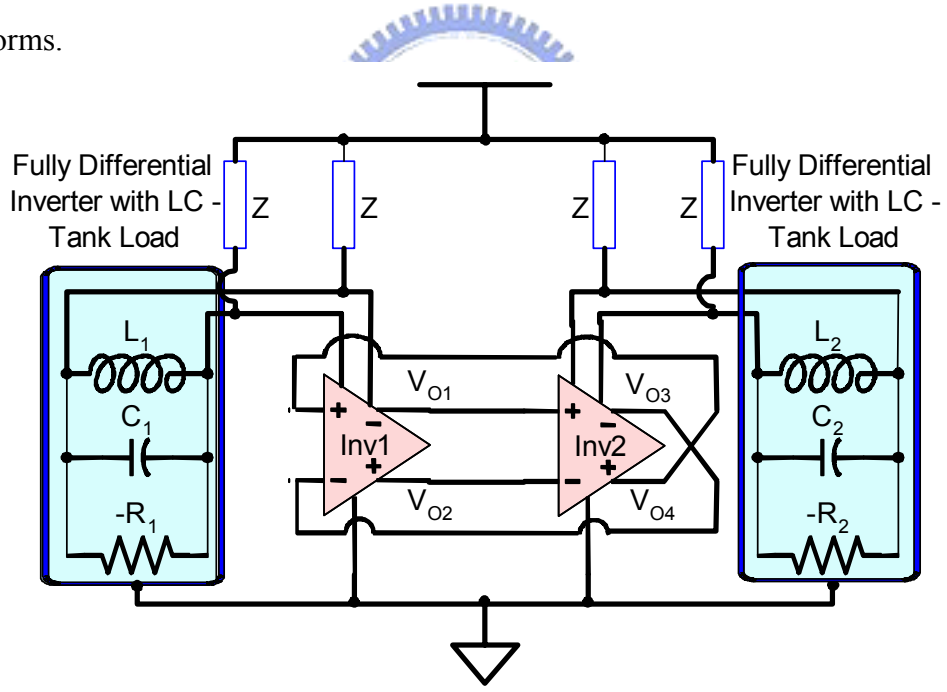


Fig.14 Block diagram of VCO

The LC-tank loads are used to reduce the phase noise of the two-stage ring oscillator. The output waveforms at the differential output nodes of Inv1 are 90° out of

phase from those at the differential output nodes of Inv2. Thus, these two differential output waveforms are synchronized in quadrature phases [22]-[26]. By incorporating the LC-tank loads into two-stage ring oscillator, the performance of this proposed quadrature VCO is significantly improved with respect to the following specifications: phase noise, frequency stability, and supply voltage sensitivities. In the proposed quadrature VCO, the oscillation frequency is determined by the effective values of the L and C and is described as

$$f_C = \frac{1}{2\pi\sqrt{LC}} \qquad (1)$$

Basically, a spiral inductor having high quality factor can provide the quadrature VCO with large swing, low phase noise, and low power dissipation. Since LC-tank composes of a spiral inductor and an N+/N-well varactor, both circuit components are in need of high quality factor because the phase noise of LC oscillators is inversely proportional to the quality factor of LC-tank. Using a similar derivation as reported in [27] a first-order estimate for the phase noise at a frequency offset $\triangle f$ from the carrier frequency f_C can be derived for a fully integrated VCO as

$$L\{\Delta f\} = kT(1+\alpha F)Z_o(\frac{1}{Q})(\frac{f_C}{\Delta f})^2(\frac{1}{V_{rms}^2}) \qquad (2)$$

Where $Z_0 = \sqrt{L/C}$ is the characteristic impedance of the tank, Q is the quality factor of the tank, F is the noise factor of the CMOS negative resistor, α is the number of times the negative conductance exceeds the tank loss to assure the start-up, Vrms is

the RMS value of the oscillation voltage, k is the Boltzmann's constant, and T is the absolute temperature. The quality factor of the tank is defined as

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = 2\pi \frac{L}{R} f_C \qquad (3)$$

Substituting (1), (3), and $Z_0 = \sqrt{L/C}$ into (2)

$$L\{\Delta f\} = kT(1+\alpha F)(\frac{1}{2\pi\Delta f})^2 \frac{R}{LC}(\frac{1}{V_{rms}^2}) \qquad (4)$$

It is remarkable that phase noise is slightly dependent on f_C, that is the phase noise over the tuning range would be nearly constant. This is because when the output is tuned at lower frequencies, the product of the L and C is increased and the output amplitude (Vrms) is decreased, the total variance of the phase noise is very small. On the other hand, when the output is tuned at higher frequencies, the product of the L and C is decreased and the output amplitude is increased, the result is the phase noise has only a small variance. From (4), the phase noise can be improved either by increasing the quality factor of the LC-tank (reducing the effective tank resistance equally), increasing the output voltage swing of the VCO, or reducing the noise factor of the MOS transistors. The noise of the power supply will also increase the phase noise when the power supply sensitivity of the VCO is poor. Necessitating the power supply generated by a separate voltage regulator with decouple filtering. Another advantage associated with the proposed structure is that only two *LC*-tank loads are required. Thus, product yield is increased due to the reduction of chip area designated

for only two rectangular spiral inductors and the manufacturing cost is reduced as well. If two waveforms of the fully differential inverters with *LC*-tank loads are out of phase from each other (180°), the output voltage waveforms of the fully differential inverters with *LC*-tank loads are synchronized in quadrature phases. In order to make the waveform out of phase, the constant current sources are used to concurrently bias these two fully differential inverters. This technique can improve the accuracy of both phase and amplitude simultaneously.

◆ *Two-Step Modulator*

The two-step modulator is a very complicated structure, which converts four baseband signals and four LO signals to four IF signals, then converts the four IF signals and the same four LO signals to two differential RF signals. We use mathematical skill to simplify the phenomenon. Suppose

Quadrature LO input: $\cos\omega_{LO}t$ 、$-\cos\omega_{LO}t$ 、$\sin\omega_{LO}t$ 、$-\sin\omega_{LO}t$

Baseband input: I、$-I$、Q、$-Q$

Then, combine quadrature LO and baseband signals into IF signals.

$$I*\cos\omega_{LO}t+Q*\sin\omega_{LO}t+(-I)*(-\cos\omega_{LO}t)+(-Q)*(-\sin\omega_{LO}t)$$

$$=2I\cos\omega_{LO}t+2Q\sin\omega_{LO}t \qquad (5)$$

$$Q*\cos\omega_{LO}t+(-I)*\sin\omega_{LO}t+(-Q)*(-\cos\omega_{LO}t)+I*(-\sin\omega_{LO}t)$$

$$= 2Q\cos\omega_{LO}t - 2I\sin\omega_{LO}t \quad (6)$$

$$(-I)*\cos\omega_{LO}t + (-Q)*\sin\omega_{LO}t + I*(-\cos\omega_{LO}t) + Q*(-\sin\omega_{LO}t)$$

$$= -(2I\cos\omega_{LO}t + 2Q\sin\omega_{LO}t) \quad (7)$$

$$(-Q)*\cos\omega_{LO}t + I*\sin_{LO}t + Q*(-\cos\omega_{LO}t) + (-I)*(-\sin\omega_{LO}t)$$

$$= -(2Q\cos\omega_{LO}t - 2I\sin\omega_{LO}t) \quad (8)$$

Equation (5), (6), (7), (8) are the IF signals. The IF signals combine the quadrature LO signals again and gets the RF signals.

$$\{\cos\omega_{LO}t(2I\cos\omega_{LO}t + 2Q\sin\omega_{LO}t) + \sin\omega_{LO}t(2Q\cos\omega_{LO}t - 2I\sin\omega_{LO}t)$$

$$+ (-\cos\omega_{LO}t)[-(2I\cos\omega_{LO}t + 2Q\sin\omega_{LO}t)] + (-\sin\omega_{LO}t)[-(2Q\cos\omega_{LO}t - 2I\sin\omega_{LO}t)]\}$$

$$= 2\{[I\cos^2\omega_{LO}t + I(1-\sin^2\omega_{LO}t) + 2Q\sin\omega_{LO}t\cos\omega_{LO}t]$$

$$+ [I(\cos^2\omega_{LO}t - 1) - I\sin^2\omega_{LO}t + 2Q\sin\omega_{LO}t\cos\omega_{LO}t]\}$$

$$= 2\{(I\cos^2\omega_{LO}t - I\sin^2\omega_{LO}t + 2Q\sin\omega_{LO}t\cos\omega_{LO}t + I)$$

$$+ (I\cos^2\omega_{LO}t - I\sin^2\omega_{LO}t + 2Q\sin\omega_{LO}t\cos\omega_{LO}t - I)\}$$

$$= 2\{(I\cos 2\omega_{LO}t + Q\sin 2\omega_{LO}t + I) + (I\cos 2\omega_{LO}t + Q\sin 2\omega_{LO}t - I)\}$$

$$= 4(I\cos 2\omega_{LO}t + Q\sin 2\omega_{LO}t) = S_{RF}(+) \quad (9)$$

Sameness

$$S_{RF}(-) = -4(I\cos 2\omega_{LO}t + Q\sin 2\omega_{LO}t) \qquad (10)$$

Noticed (5), (6), (7), (8), the four equations are the first-converted results of baseband signals and LO signals. (9), (10) are the RF output signals and have a 180° phase delay for each other.

In the above mathematical identification, the two-step modulator's phenomenon is really working.

◆ *Power Amplifier*

For Bluetooth class III, 1V power supply and 0dBm output power consideration, a design concept of the class A power amplifier will be shown. Fig.12 shows the conceptual model of a class A power amplifier. In fig.15, the matching network is tuned to obtain the maximum output power. When the PA output power is maximum, we define that Rin=Ropt, the optimal resistance.

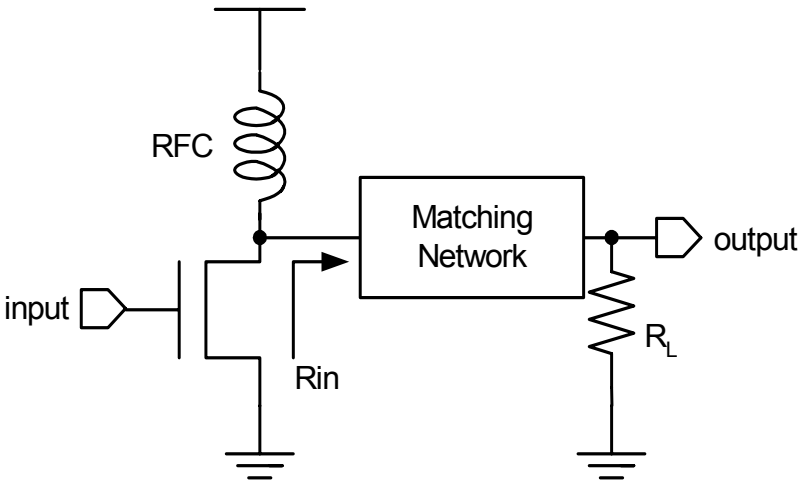


Fig.15 Conceptual model of a class A power amplifier

In a class A power amplifier operation, the transistor plays the role of a current source. Fig.16 shows the basic I-V curve of a NMOS. Imax means the maximum current of the transistor; Imin means the minimum current of the transistor. Vmax means the maximum voltage difference between the drain and source of the transistor. Vmin means the minimum voltage difference between the drain and source of the transistor. Therefore, the transistor voltage swing and current swing is shown as:

$$Transistor\ Voltage\ Swing = Vmax - Vmin \tag{16}$$

$$Transistor\ Current\ Swing = Imax - Imin \tag{17}$$

The adjust resistance Ropt for full ac swing is:

$$Vmax - Vmin = Ropt\ (Imax - Imin) \tag{18}$$

From (18), Ropt can be determined:

$$Ropt = \frac{Vmax - Vmin}{Imax - Imin} \tag{19}$$

From (16) (17), the root mean square voltage and current can be shown:

$$Vrms = \frac{Vmax - Vmin}{2\sqrt{2}} \tag{20}$$

$$Irms = \frac{Imax - Imin}{2\sqrt{2}} \tag{21}$$

The output power can be expressed:

$$Pout = VrmsIrms = \frac{(Vmax - Vmin)(Imax - Imin)}{8} \tag{22}$$

The Vdc, Idc, dc power is shown as:

$$Vdc = \frac{(Vmax + Vmin)}{2} \tag{23}$$

$$Idc = \frac{(Imax + Imin)}{2} \tag{24}$$

$$Pdc = \frac{(Vmax + Vmin)(Imax + Imin)}{4} \tag{25}$$

Form (22) and (25), the drain efficiency is:

$$Eff_{\text{drain}} = \frac{Pout}{Pdc} = 0.5\frac{(\text{Vmax} - \text{Vmin})(\text{Imax} - \text{Imin})}{(\text{Vmax} + \text{Vmin})(\text{Imax} + \text{Imin})} \tag{26}$$

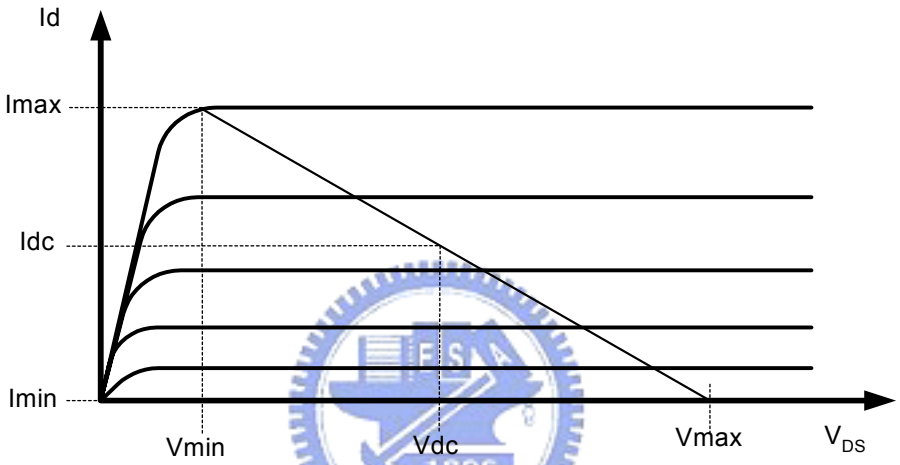


Fig.16 I-V curve of a NMOS

2.3POTENTIAL RISK AND IMPROVEMENT SOLUTIONS

◆ *Potential Risk*

The transmitter with two-step architecture has some potential risks maybe happening.

First, the third harmonic of first-stage modulator is 3.6GHz, which will be converted to 4.8GHz and 2.4GHz by 1.2GHz LO in second-stage modulator. It will interfere with the desired signal. Please see Fig.17.Second, the LO leakage on

first-stage modulator is 1.2GHz, which will be converted to 0GHz and 2.4GHz by 1.2GHz LO in second-stage modulator. It will interfere with the desired signal.

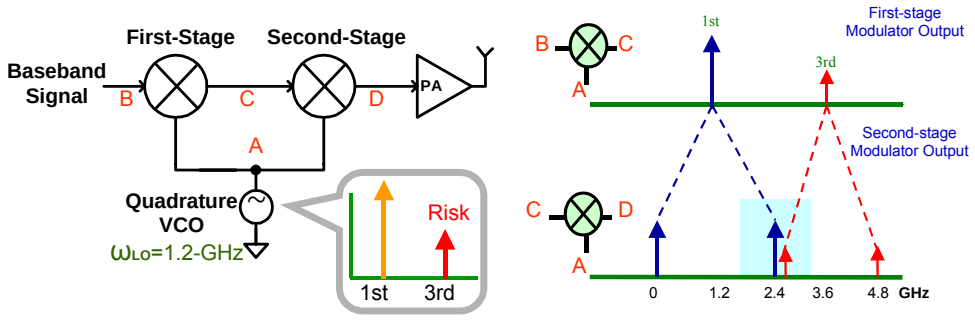


Fig.17 Potential risk

The last, the noise of the power supply will increase the phase noise when the power supply sensitivity of the VCO is poor. Necessitating the power supply generated by a separate voltage regulator with decouple filtering. But, the voltage regulator with decouple filtering is usually implemented on PCB board; the voltage deviation caused by bond-wire will still affect the VCO. See (27)

$$\Delta V = L\frac{dI}{dt} \qquad (27)$$

ΔV is the voltage deviation, L is the bond-wire's inductor.

◆ *Improvement Solutions*

For the first potential risk, the third harmonic of first-step modulator is coming from the third harmonic of VCO. Small piece capacitors are added on VCO output and first- stage modulator output during circuit design for filtering the third

harmonic.In VCO simulation, optimizing the swing voltage of the oscillation is very important. We will show it in the post-simulation result.

For the second potential risk, it is hard to prevent the leakage. The parasitic capacitor “Cgd” of the MOS is the main path of the leakage. Selecting the suitable size of the MOS and monitoring the leakage are important during the simulation.

For the last potential risk, we add capacitance all over the IC and bonding the power and ground wires as many as possible.

Chapter3

CIRCUIT DESIGN AND SIMULATION

3.1 QUADRATURE VCO

Fig.18 shows the CMOS circuit realization of a quadrature VCO, consists of two fully-differential inverters with *LC*-tank load plus cascoded negative resistor, where the cross-coupled MOS transistorsMV1, MV2, MV3, MV4 can form a positive feedback loop to realize the negative resistor. The negative resistance is used to compensate the loss of the resonator so that the resonator can sustain its oscillation. Since the quality factor of a rectangular spiral inductor is inferior to that of a bonding wire [28], MOS transistors MV1, MV2, MV3, MV4 need to have wider channel width to provide enough negative transconductance. And the transconductance of MV1, MV2, MV3, MV4 is chosen to be larger than the required minimum, to further guarantee the success of getting adequate oscillations under possible variations caused by process, power supply voltage, and temperature.

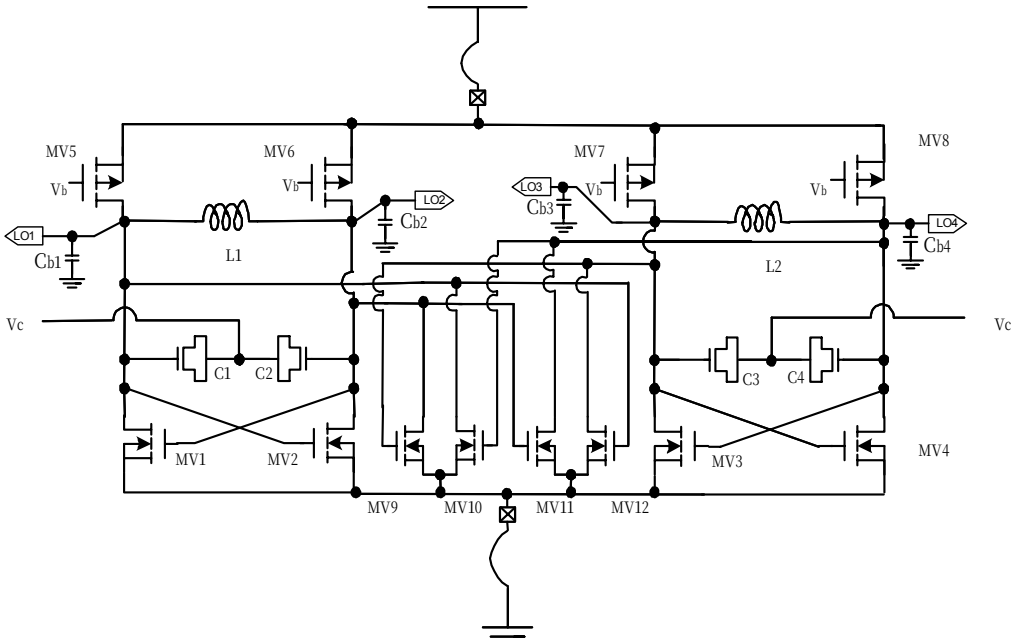


Fig.18 Quadrature VCO

The *LC*-tank consists of rectangular spiral inductors L1, L2, N+/N-well varactor C1, C2, C3, C4 and the parasitic capacitances of MV1, MV2, MV3, MV4, MV5, MV6, MV7, MV8, MV9, MV10, MV11, and MV12. The inductance is designed to be as large as possible for lower power dissipation while retaining a satisfactory tuning range for frequency. The control voltage V_C is applied to provide a reverse bias for varactor.

The fully differential inverters formed by MOS transistors MV9, MV10, MV11, and MV12 are the main building blocks in the two-stage ring oscillator to be used as the phase controller. Thus, there will be a 90° shift between the two differential outputs of the two coupled fully-differential inverters. In order to achieve highly accurate quadrature phases, the total current of the load circuit must be constant. The

MOS transistors MV5, MV6, MV7, MV8 are designed to be the current sources and the loads. For this design, only an inductor replaces two pull-up inductors, it can reduce the VCO size efficiently. Please see Fig.19.

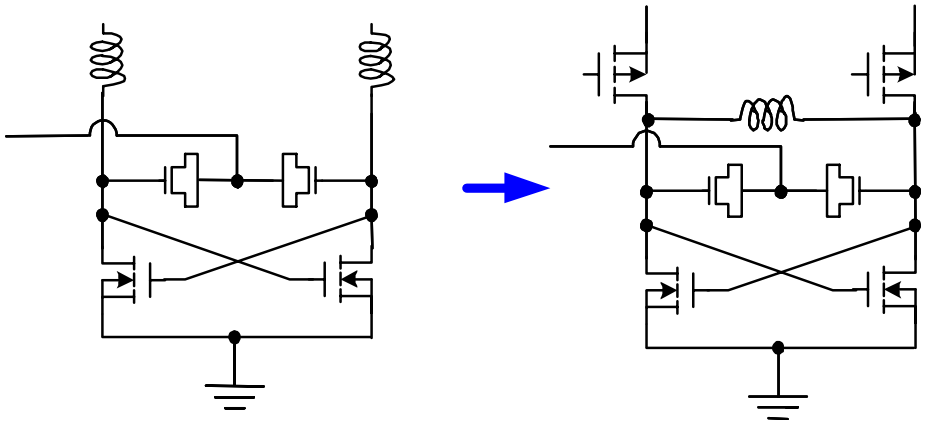


Fig.19 Two pull-high inductors are replaced by one cross inductor

The MOS transistors MV5, MV6, MV7, MV8 acts as constant-current sources controlled by the bias voltage V_b. They can improve the phase accuracy of the quadrature oscillation. Table IV gives a summary of the device dimensions and component values of the quadrature VCO.

Table IV Parameter information of VCO

MV1~MV4 (W/L)	**160 μ m/0.24 μ m**
MV5~MV8 (W/L)	**350 μ m/0.24 μ m**
MV9~MV12 (W/L)	**30 μ m/0.24 μ m**
L_1, L_2	**7.28nH**

Two rectangular spiral inductors L_1 and L_2, as presented in Fig.14, are fabricated

by using the top metal layer from a CMOS process. And their quality factor is approximately 5.6 at 1.2 GHz. The model of the rectangular spiral inductor can be presented as Fig.20.

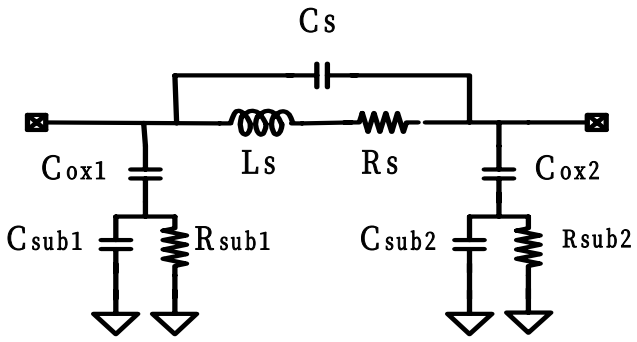


Fig.20 The model of the rectangular spiral inductor

Ls is the inductance of the spiral inductor, Rs is the parasitic series resistance of spiral inductor, Rsub1, Rsub2 are the silicon substrate resistance, Csub1, Csub2 are the oxide capacitance between spiral inductor and substrate, and Cs is the overlap capacitance between spiral inductor and the center-tap underpass.

3.2 TWO-STEP MODULATOR

In section 2.2.2, the two-step modulator has been proved to be working by mathematics. In this section, the two-step modulator will be realized.

A basic multiplieris designed and proposed in [8]. See Fig.21. From ideal square-law, the output can be expressed as:

$$IF_I - \overline{IF}_I = Z_0 \cdot (I_1 + I_2 + I_3 + I_4 - I_5 - I_6 - I_7 - I_8)$$

$$= 8Z_0 \cdot K \cdot (BB_I \cdot LO_I + BB_Q \cdot LO_Q) \quad (28)$$

Where, Z0 is the equivalent output impedance; $K = 0.5\mu_0 C_{ox}(w/L)$; μ_0 is the low-field mobility.All developments for the up-converter are originally based on square-law. Because of channel pinched-off, a MOS device works in saturation region. If a short-channel device is employed in circuit implementation, another mechanism causing saturation is involved [29]. In a short-channel device, velocity saturation occurs before pinched-off. Taking velocity saturation and mobility degradation into consideration, (38) presents an advanced formula modified from the ideal square-law, where ν_{sat} denotes saturated velocity and θ is a fitting parameter approximately equaling to $\frac{10^{-7}}{thickness-of-gate-oxide} V^{-1}$

$$I_D = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\frac{(V_{GS}-V_T)^2}{1+(\frac{\mu_0}{2v_{sat}L}+\theta)(V_{GS}-V_T)}$$

$$\approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}[1-(\frac{\mu_0}{2v_{sat}L}+\theta)(V_{GS}-V_T)](V_{GS}-V_T)^2 \quad (29)$$

The result indicates that the gate voltage of the MOS devices should be kept low enough to avoid short-channel effect.

From equation (29), if the short-channel effects are considered, the equation (28) can be expressed as:

$$IF_I - \overline{IF}_I = 8Z_0 \cdot (K - 3K' \cdot C) \cdot (BB_I \cdot LO_I + BB_Q \cdot LO_Q) \quad (30)$$

Where, VDCs is the dc voltage at the source; VDCG is the dc voltage at the gate; Z0 is the equivalent output impedance; $K = 0.5\mu_0 C_{ox}(w/L)$; $K' = K \cdot [\mu_0 / 2v_{sat} \cdot L) + \gamma]$;

$C = |VDC_G - VDC_S - V_{th}|$; v_{sat} is the saturation velocity; μ_0 is the low-field mobility;

$\gamma = (10^{-7} / t_{ox})^{-1}$

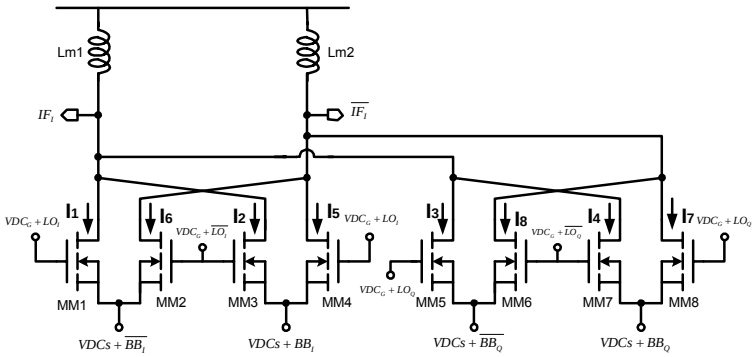


Fig.21 The basic multiplier

Fig. 22 is the block diagram of the basic multiplier. From equation (5), (6), (7), (8), (9), (10), the two-step modulator can be built by the basic multiplier. The block diagram is shown in Fig. 23.

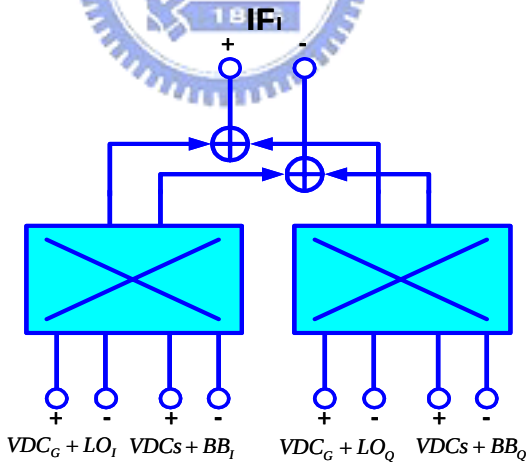


Fig.22 The block diagram of the basic multiplier

In Fig. 23, the RF signals can be derived from equation (30) and expressed as:

$$RF = 64[Z_0 \cdot (K - 3K' \cdot C)]^2 \cdot (LO_I{}^2 \cdot BB_I - LO_Q{}^2 \cdot BB_I + 2LO_I \cdot LO_Q \cdot BB_Q) \quad (31)$$

In equation (31), Let $LO_I = \cos\omega_{LO}t$; $LO_Q = \sin\omega_{LO}t$; $BB_I = I$; $BB_Q = Q$,

the equation can be expressed as:

$$RF = 64[Z_0 \cdot (K - 3K^{'} \cdot C)]^2 \cdot (I \cdot \cos 2\omega_{LO}t + Q \cdot \sin 2\omega_{LO}t) \qquad (32)$$

Equation (32) is the same form with equation (9). The basic multiplier can realize the two-step modulator.

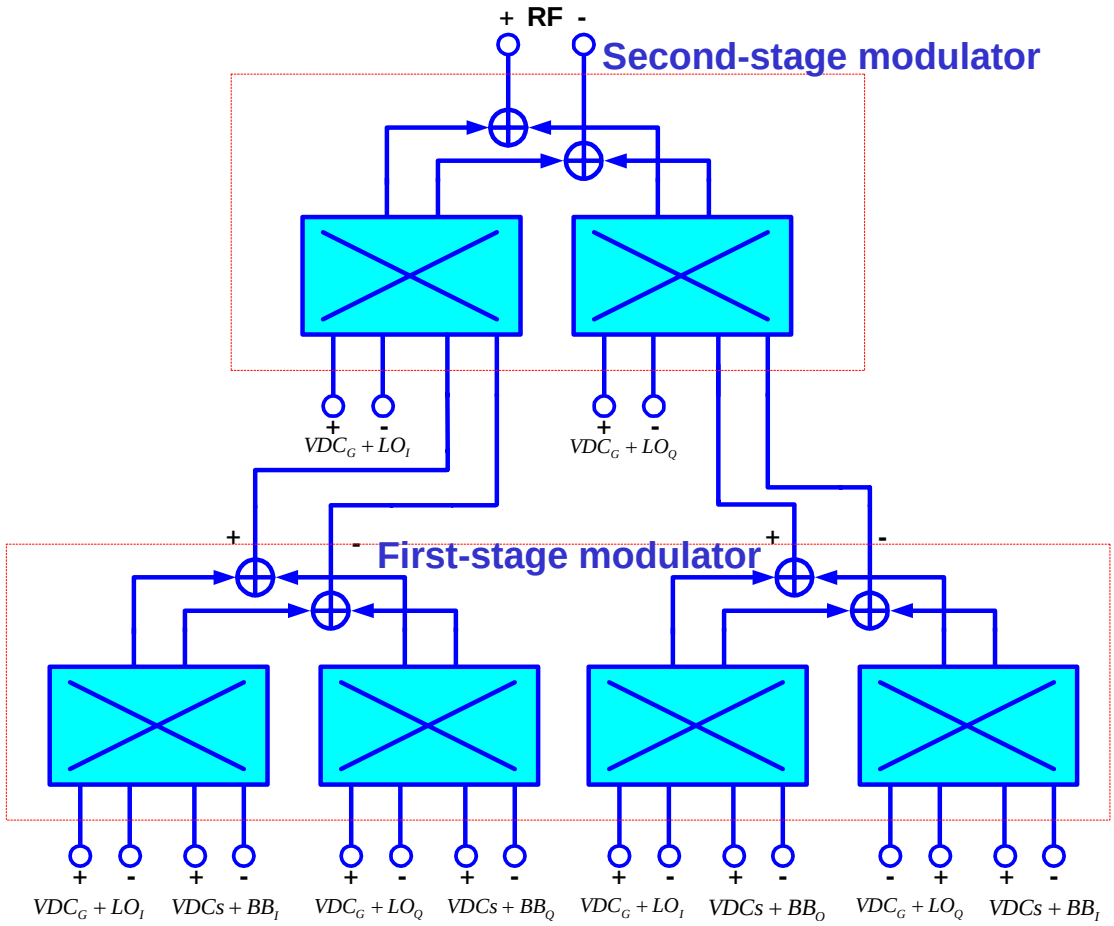


Fig.23 Two-step modulator

Finally, Using Fig.18 to realize the whole two-step modulator in Fig.20. After simplifying, the result is presented in Fig.24.

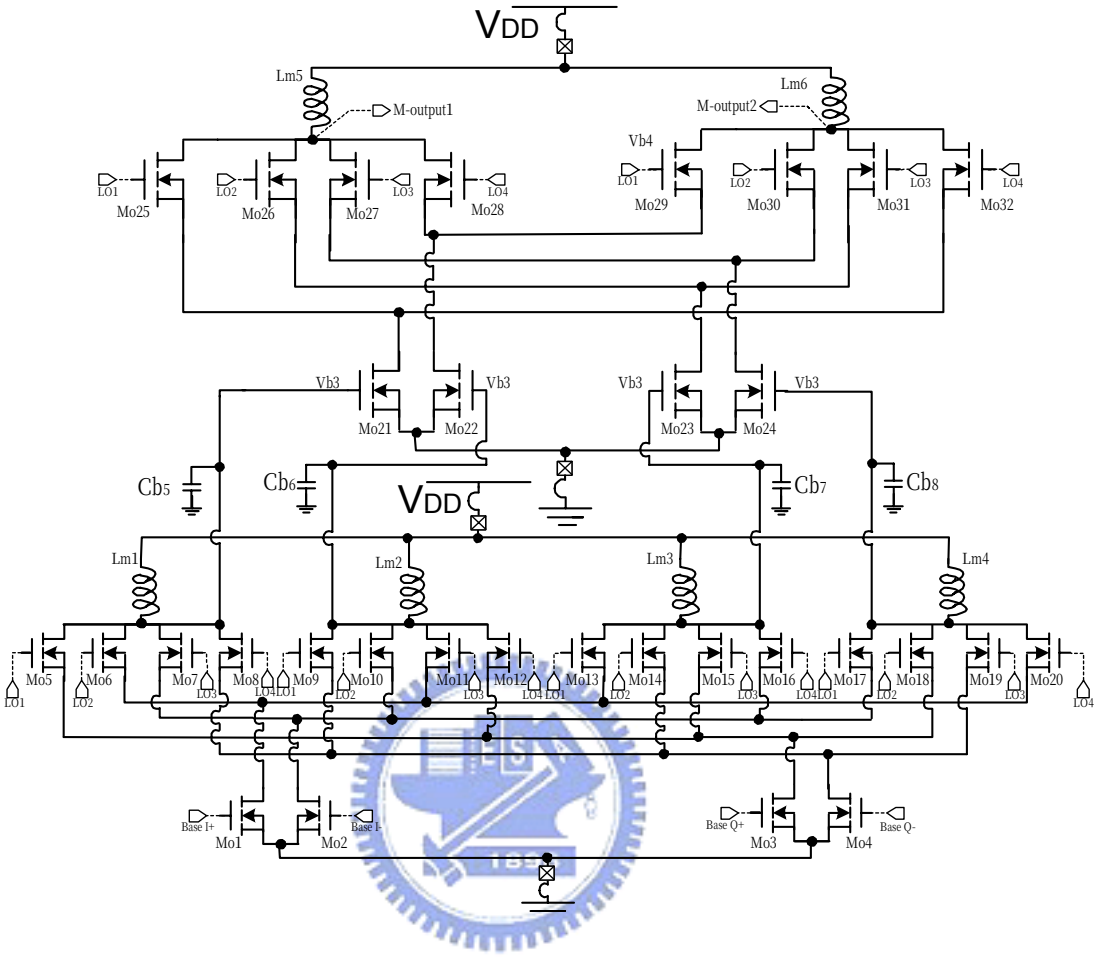


Fig.24 Realization circuit of two-step modulator

There are four quadrature inputs from LO signals, four quadrature inputs from baseband signals, and four quadrature outputs to IF band at first-stage modulator. At second-stage modulator, there are four quadrature inputs from LO signals, four quadrature inputs from first-stage modulator, and two differential outputs to RF band. To realize the circuit, minimum 32 pieces of MOS are need.

Since the output signal of the modulator is in the 2-3GHz ranges, the LC-tank loads are selected to tune out the parasitic capacitance at the output nodes. The body

effect is not appearing in the modulator, because the deep N-Well process is used and both the sources and the bodies of MOSFETs are short together. So all the threshold voltages, V_T is identical with the same V_{T0}.

The improved two-step modulator uses the quadrature structure in the second-stage to suppress image signals. Mismatch on phase and magnitude will affect the image rejection. For MOS component, AD means drain area, AS means source area, PD means peripheral length of drain, PS means peripheral length of source, NRS means parasitic resistor of source, NRD means parasitic resistor of drain; the variation of parameters could result the mismatch. Monte Carlo simulation is a good method to predict the mismatch. Table V gives a summary of the device dimensions and component values of the modulator.

Table V Parameter information of modulator

Mo1~Mo4 (W/L)	**320 μ m/0.24 μ m**
Mo5~Mo20 (W/L)	**160 μ m/0.24 μ m**
Mo21~Mo24 (W/L)	**80 μ m/0.24 μ m**
Mo25~Mo32 (W/L)	**40 μ m/0.24 μ m**
Lm1~Lm4	**Nr=6.5**
Lm5~Lm6	**Nr=3.5**

3.3 POWER AMPLIFIER

In this work, a cascade differential power amplifier is implemented for obtaining

moderate output power. If the signal swing at the input of the power amplifier is small, the output power will be small and the efficiency will be poor for certain. So, the output swing of the quadrature modulator is required to provide large signal for power amplifier. The power amplifier is designed to be Class-A. Compared to the single-ended power amplifier, the differential topology has the advantages of increasing output power, even harmonic cancellation, and alleviating the problem of substrate coupling. Another advantage of the differential topology is the frequency of the noise in substrate that couple from power amplifier is twice the frequency of the signal. Fig.25 shows the realization circuit of power amplifier.

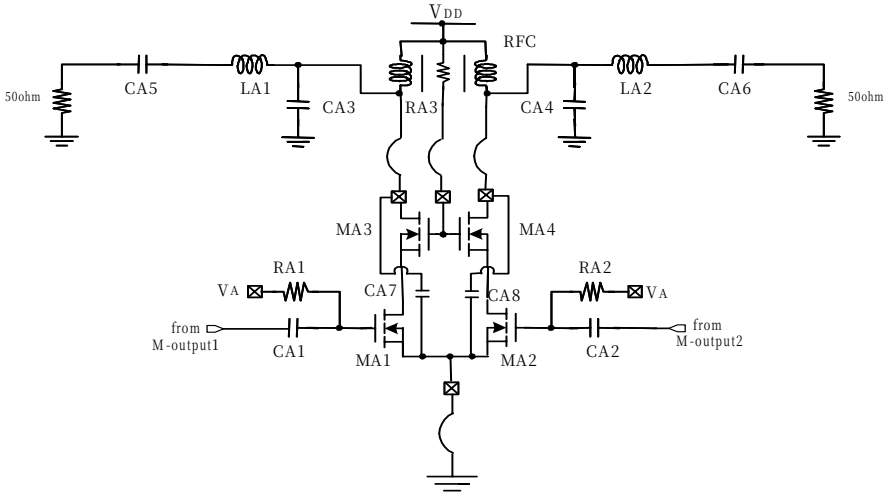


Fig.25 Realization circuit of power amplifier

This power amplifier is a cascaded, fully balanced amplifier. The cascoded architecture (M_{A1}, M_{A2}, M_{A3}, M_{A4}) is used here to avoid oxide breakdown problem. The fully balanced amplifier has the advantage of suppressing even order harmonics, and has better immunity against noise from the power supply and substrate. RFC is

the quarter-wave transmission line choke to achieve high efficiency. The C_{A3}, C_{A4}, C_{A5}, C_{A6}, L_{A1}, L_{A2} play the role of matching network. The DC bias V_A is set to achieve the best efficiency and maximize delivered power. A balun is required to convert the output differential signals to single-ended signal for measurement.

The parasitic inductance and capacitance of the bonding wires and pads will degrade the performance of the power amplifier seriously. Thus these parasitic components must be taken into account during the design of the power amplifier. In general, the parasitic components of output bonding wires and pads must be merged into the matching network to achieve the best efficiency and maximize output power. Because the realistic behaviors of these parasitic components are difficult to predict, the output-matching network for the power amplifier usually needs fine tuning before the chip is measured.

The component values, channel dimensions of MOS devices of Fig.22 are summarized in Table VI.

Table VI Parameter information of PA

M_{A1}~M_{A4} (W/L)	**700 μm/0.24 μm**
R_{A1}~R_{A3}	**2kΩ**
C_{A1}, C_{A2}, C_{A5}, C_{A6}	**1pF**
C_{A3}, C_{A4},	**1.5pF**
C_{A7}, C_{A8},	**0.3pF**
L_{A1}~L_{A2}	**1nH**

3.4 TRANSMITTER REALIZATION

This section describes the designed transmitter circuit implemented on a single chip, based on fully differential configuration and double-quadrature architecture. Fig.26 is the complete circuit of the transmitter.

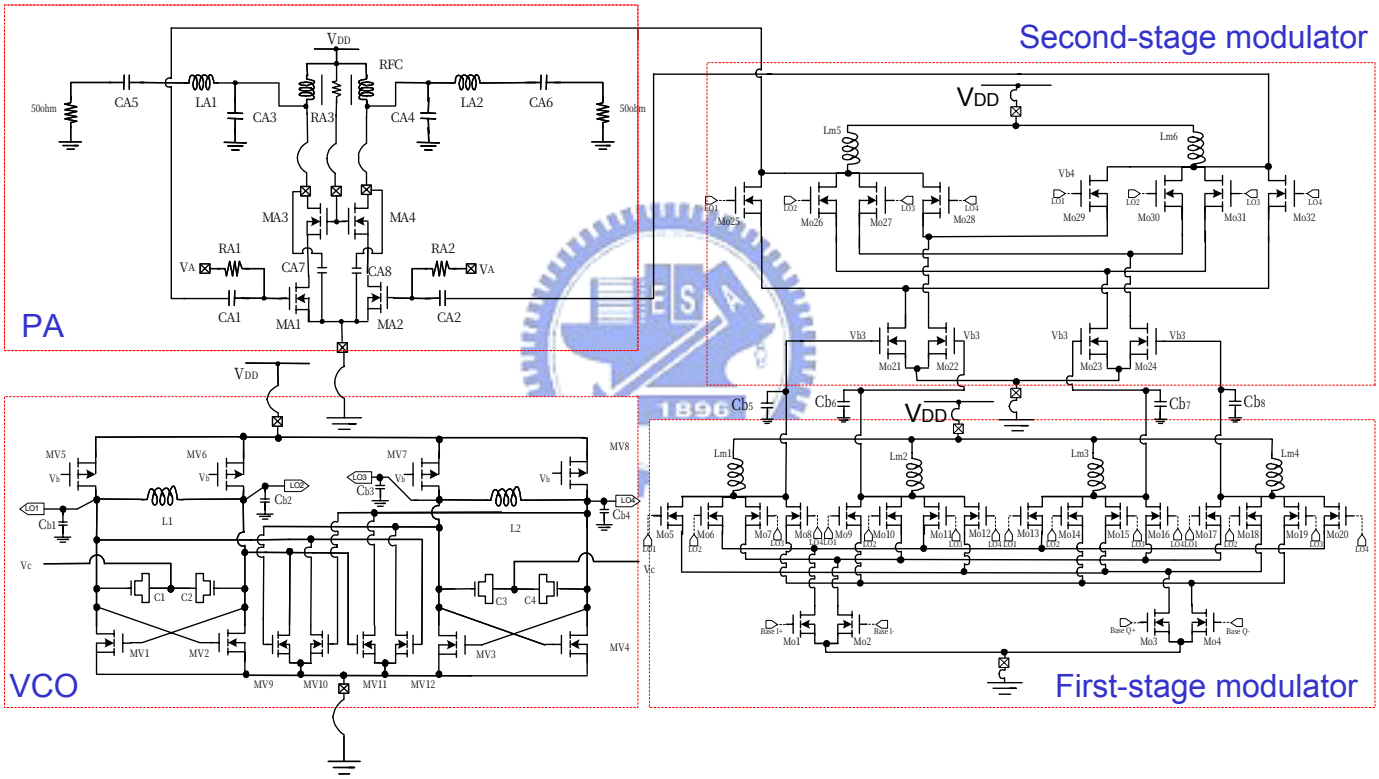


Fig.26 The complete circuit of the transmitter

1-V power supply is no doubt a challenge on .25- μ m technology in many conventional circuit structures. The number of cascaded MOS devices, in practice, is kept less than three. However, that only confirms all MOS devices operating normally on required DC status. Another obstacle is voltage swing. Fortunately, a character of

inductor can be applied to overcome the swing restriction. The circuit usually applies inductors for proper load. An inductor provides sufficiently high load impedance while resonating with an equivalent parallel capacitor. In addition, even if one terminal is connected to power supply, voltage swing of the other terminal can exceed the supplied voltage. All inductors employed are spiral inductors made of top thick metal; varactors are N+/n-well structure; resistors are polysilicon resistors with silicide blocks. To avoid body effect, all N-MOS devices contain deep n-well for equal voltage potential between respective bodies and sources. The model is supported by TSMC.

Due to the reuse of VCO, the chip size can be greatly reduced to 1.8mm x1.8mm.

3.5 SIMULATION RESULTS

This 2.4-GHz transmitter is simulated by using HSPICE, and is designed by TSNC 0.25μm 1P5M CMOS technology with a 1v supply voltage. The result of the post layout simulation is shown in this section.

Fig.27 shows the quadrature waveform of VCO. Fig.28 is the waveform of first-stage modulator and second-stage modulator, where the dwell time of second-stage modulator is half of first-stage modulator. Fig.29 is the output waveform of PA, where base-band signal is carried on 2.4-GHz.

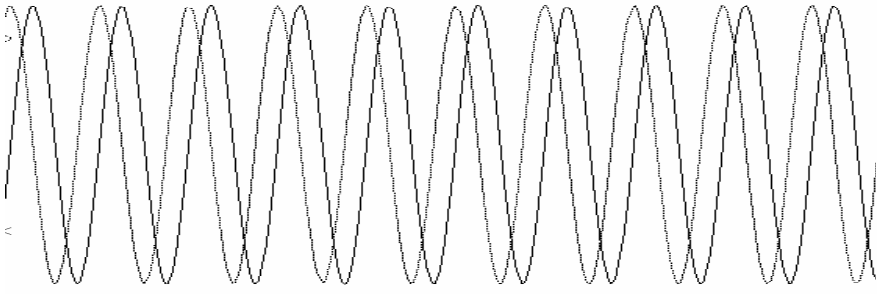


Fig.27 The quadrature waveform of VCO

Fig.28 The waveform of first-stage modulator and second-stage modulator

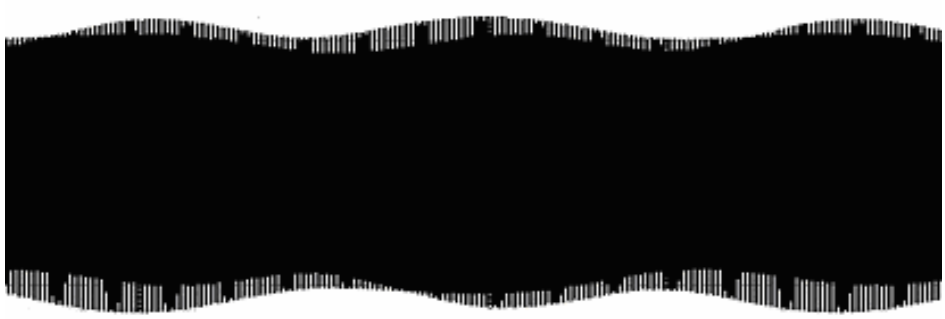


Fig.29 The output waveform of PA

Fig.30 shows the tuning range of VCO, it starts at 2402-MHz and stops at 2648-MHz, and the control voltage is 0V~1V. The VCO supply voltage is 1-V. The tuning range is 246-MHz. Fig.31 is the phase noise of VCO; it is -98dBc/Hz when

offsetting 100-KHz, -120dBc/Hz when offsetting 1-MHz. Due to the model of resistor being an ideal resistor, the thermal noise cannot be expressed in this simulation, so no corner in the curve of phase noise.

For VCO phase & magnitude error simulation, the Monte Carlo is setting as channel length: 0.24u ± 0.02u, channel width: 10u±0.03u, V_{TH} (NMOS): 0.5486611V ±0.06V, V_{TH} (PMOS): -0.6146093V±0.05V, distribution: uniform. The maximum magnitude error is 2.3mV, the minimum magnitude error is 0.4mV, the maximum phase error is 0.129°; the minimum magnitude error is 0.024°.

For Transmitter phase & magnitude error simulation, the Monte Carlo is setting as channel length: 0.24u ± 0.02u, channel width: 10u±0.03u, V_{TH} (NMOS): 0.5486611V±0.06V, V_{TH} (PMOS): -0.6146093V±0.05V, distribution: uniform. The maximum magnitude error is 5.3mV, the minimum magnitude error is 0.6mV, The maximum phase error is 0.221°, the minimum magnitude error is 0.035°. The image rejection: $IRR = \frac{(\Delta A/A)^2 + \theta^2}{4} = -40.4dB$. Please see Table VII.

Table VII Monte Carlo result

	Magnitude error		Phase error	
	Minimum	Maximum	Minimum	Maximum
VCO	0.4mV	2.3mV	0.024°	0.129°
Transmitter	0.6mV	5.3mV	0.035°	0.221°

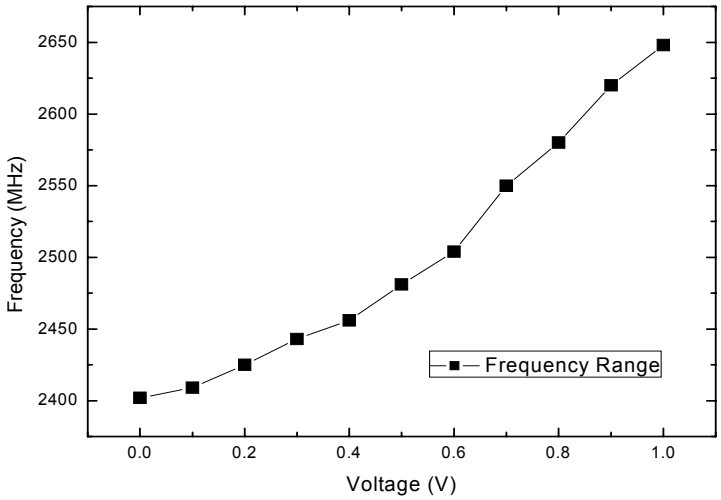


Fig.30 The tuning range of VCO

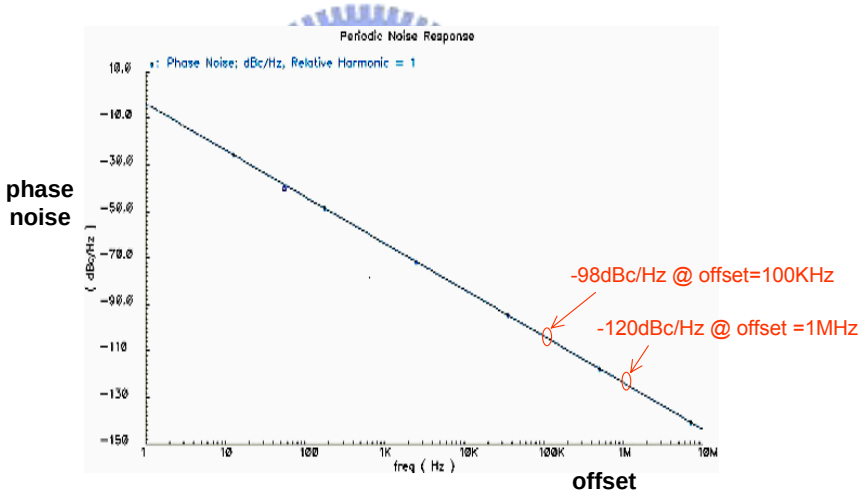


Fig.31 The phase noise of VCO

Fig.32 shows the conversion gain of modulator. The first-stage conversion gain is 5.9dB, and the second-stage conversion gain is 4.2dB. For modulator isolation simulation, it is shown in Fig.33. When signal is input at port1, the leakage signal will be found at port2 and port3. When signal is input at port3, the leakage signal will be

found at port4 and port5. Table VIII shows the result of leakage. The worst leakage signal is –67.1dB at port5 when the signal is input at port3.

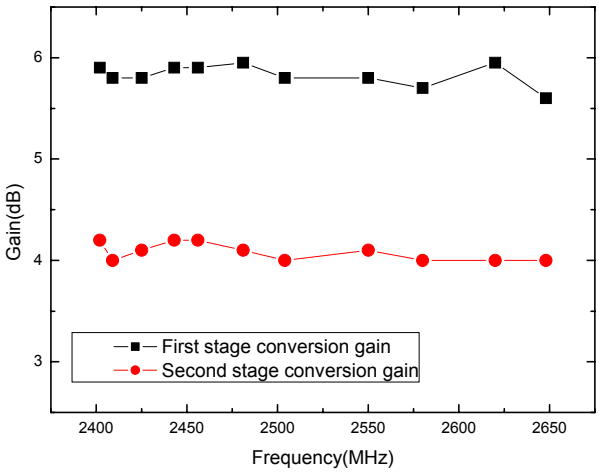


Fig.32 The conversion gains of modulator

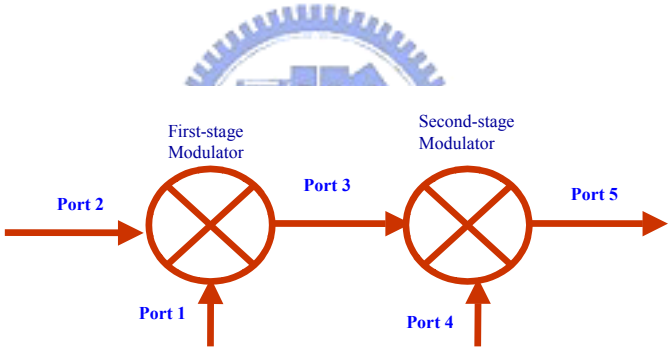


Fig.33 Modulator isolation simulation

Table VIII Modulator isolation result

	First-stage Modulator		Second-stage Modulator
port1(*in*) port2(*out*)	-84.4dBc	port4(*in*) port3(*out*)	-80.3dBc
port1(*in*) port3(*out*)	-89.3dBc	port4(*in*) port5(*out*)	-90.2dBc
port2(*in*) port1(*out*)	-97.9dBc	port3(*in*) port5(*out*)	-67.1dBc
port2(*in*) port3(*out*)	-70.2dBc	port3(*in*) port4(*out*)	-71.5dBc

Fig.34 shows the in band spurious emission, it contains LO leakage, Image

Rejection, IM2 (LO+2BB), IM3 (LO+3BB). The input signal is 70mv peak-peak at 50MHz, and the LO leakage is –44dBc, the image rejection is –32.1dBc, the LO+2BB is –71.9dBc, the LO+3BB is –49.9dBc.

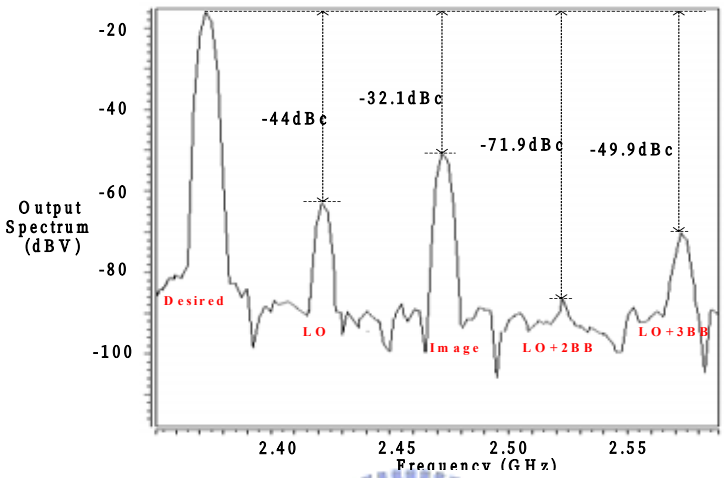


Fig.34 In band spurious emission

Fig.35 shows the out of band spurious emission. The 1.2-GHz emission is –58.2dBm, the 3.6-GHz emission is –43.5dBm, the 4.8-GHz emission is –59.1dBm the 6.0-GHz emission is –66.3dBm, the 7.2-GHz emission is –42.8dBm. All emissions can meet bluetooth specification.

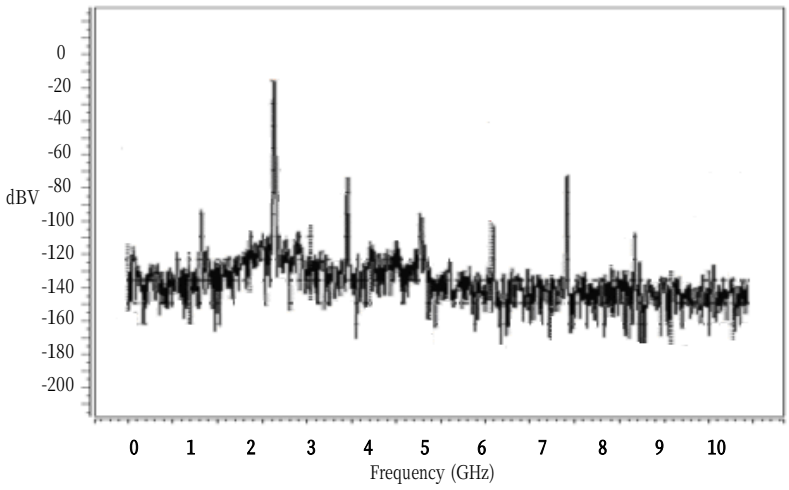


Fig.35 Out of band spurious emission

Fig.36 shows the linearity of PA. The IIP3 is 3.7dBm, and the OIP3 is 5.2dBm.

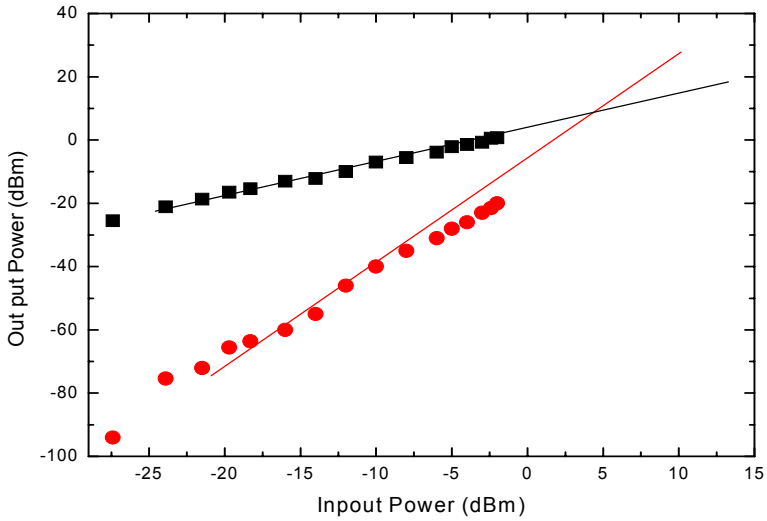


Fig.36 Linearity of PA

Fig.37 is the drain efficiency and PAE of PA. It is about 12.85% and 10.73%

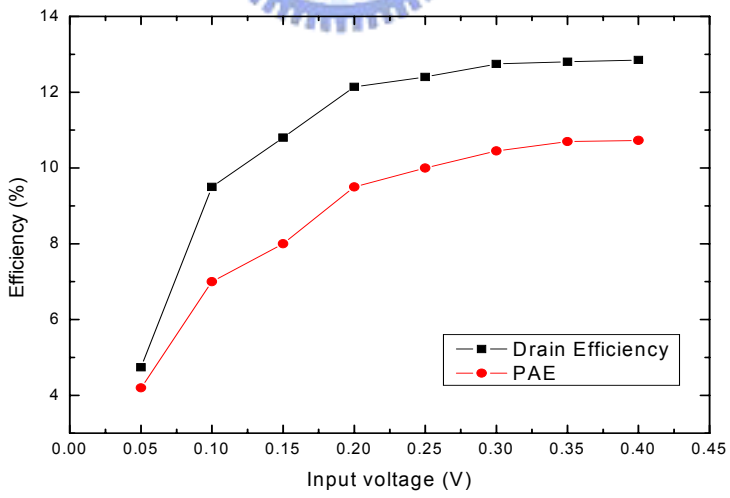


Fig.37 Drain efficiency and PAE

For stable consideration, the real part of Z22 is large than 0Ω from 0.8-GHz to 3.6-GHz. The S22 is below 0dB from 0.8-GHz to 3.6-GHz. For unconditional stable,

the K factor and Delta factor are simulated, and the result is

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}\,S_{21}|} > 1 \text{ and } |\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \text{ from 0.8-GHz}$$

to 3.6-GHz. They are shown Fig. 38, Fig 39, Fig 40, Fig 41, and the design circuit is a stable circuit.

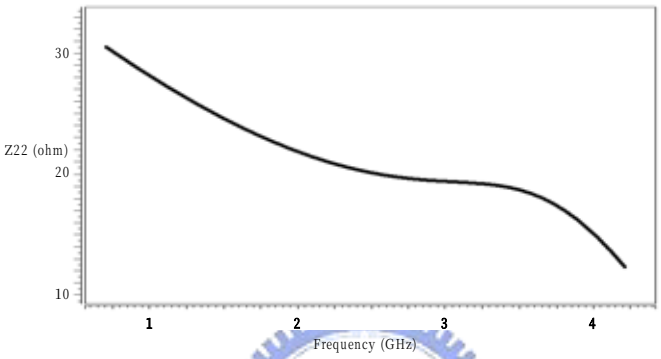


Fig.38 R {Z22}

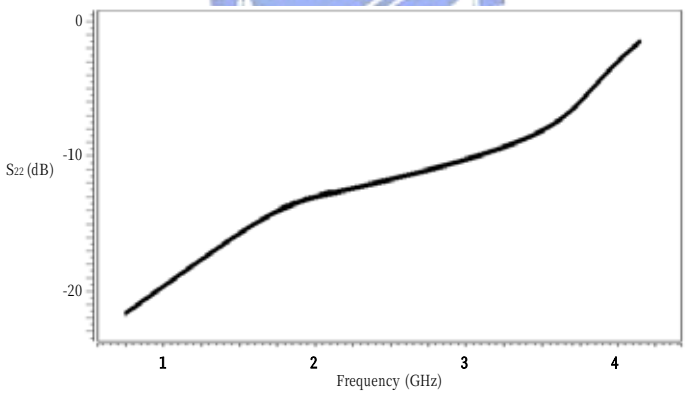


Fig.39 S22

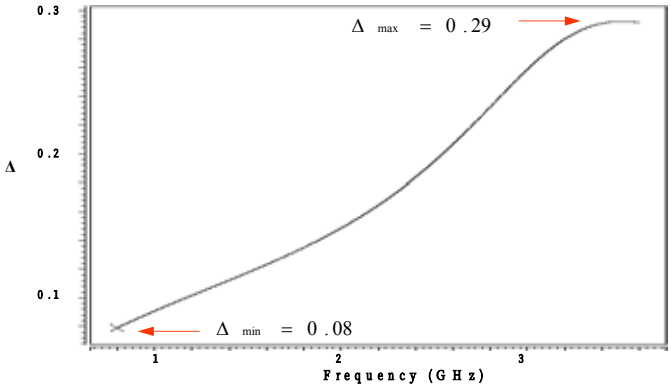


Fig.40 Δ

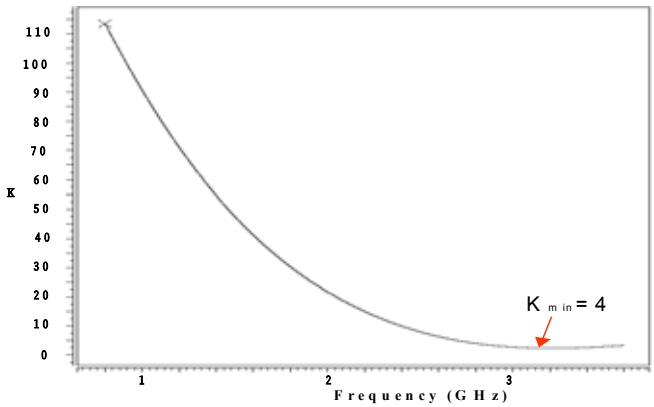


Fig.41 K factor

Table IX, Table X, Table XI, Table XII, Table XIII, Table XIV, shows the reliability simulation results. The deviations of output power & output frequency are simulated by four corner condition for process deviation, by 0°C~50°C change for thermal & environment temperature deviation, by 1V ±10% for power supply deviation.

Table IX Output power versus process deviation

	TT	FF	SS	SF	FS
Output Power	*3.1*	*6.9*	*0.02*	*0.58*	*4.2*
Bias	(0.2V)	(0.2V)	(0.05V)	(0.35V)	(0.15V)

Table X Output power versus temperature

	0°	25°	50°
Output Power	*5.5*	*3.1*	*2.1*
Bias	(0.2V)	(0.2V)	(0.2V)

Table XI Output power versus power supply

	1.1V (+10%)	1V (100%)	0.9V (-10%)
Output Power	*5.6*	*3.1*	*-7.6*
Bias	(0.3V)	(0.2V)	(0.2V)

Table XII Frequency versus process deviation

	TT	FF	SS	SF	FS
Frequency	*2.46*	*2.51*	*2.43*	*2.39*	*2.49*
(VCT Bias)	(0.6V)	(0.6V)	(0.6V)	(0.6V)	(0.6V)

Table XIII Frequency versus temperature

	0°	25°	50°
Frequency	*2.48*	*2.46*	*2.45*
(VCT Bias)	(0.6V)	(0.6V)	(0.6V)

Table XIV Frequency versus power supply

	1.1V (+10%)	1V (100%)	0.9V (-10%)
Frequency	*2.52*	*2.46*	*2.43*
(VCT Bias)	(0.6V)	(0.6V)	(0.6V)

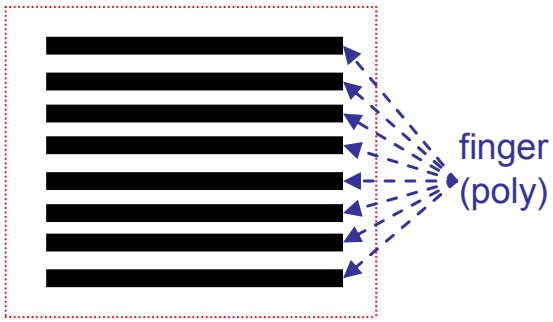
Due to the bigger layout size of RF MOS model, we use the mixed mode of MOS model to design this transmitter. In the future, if the work frequency is at 5GHz or above the frequency, using the exact RF model in design is necessary. At the end of this section , we re-simulation the transmitter with RF model and find that: (1) The tuning range is 2402MHz~2648MHz in mixed mode and 2377MHz~2595MHz in RF model. (2) The output power is 0.02dBm~6.9dBm in mixed mode and –1.2dBm~6.7dBm in RF model. Please see Table XV. Table XVI is the final summery list.

Table XV Compare mixed mode and RF model

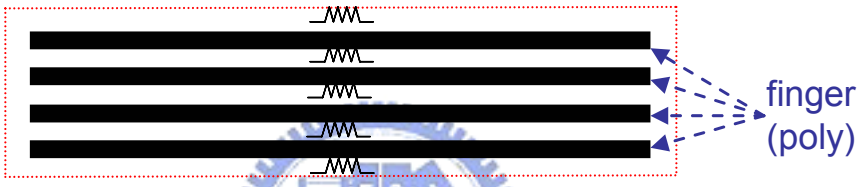
	Frequency (MHz)		Output Power (dBm)	
	Minimum	Maximum	Minimum	Maximum
Mixed mode model	2402	2648	0.02	6.9
RF model	2377	2595	-1.2	6.7

In the layout of RF MOS device, the optimal numbers of finger is important. The MOS device should have the optimal numbers of finger to make its size into a squire. If reducing the numbers of finger, the finger will be long, the parasitic resistor of poly will increase, and it will affect the output current. If increasing the numbers of

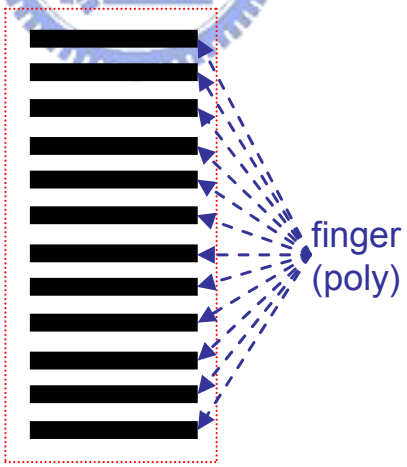
finger, the MOS device will be affected by process variation seriously. Please see Fig. 42.



The optimal numbers of finger to make the size of the MOS into a squire



The parasitic resistor of long finger reduce the current of MOS



The performance of the MOS will be affected easily by process variation.

Fig.42 The optimal numbers of finger

Table XVI The summery of post-simulation

Technology		TSMC 0.25um1P5M CMOS
Spec.		Bluetooth Class III
Supply voltage		1V
VCO	Tuning frequency range	2402~2648MHz
	VCO phase noise	-120dBc/Hz@1MHz
	Phase error	0.102°
	Magnitude error	1.5mV
	DC current of VCO	13.70mA
Modulator	First-Modulator Conversion Gain	5.9dB
	Second-Modulator Conversion Gain	4.2dB
	Modulator Isolation	< -67.1dBc
	DC current of Modulator	17.10mA
PA	Unconditional Stable: △	0.21 (<1)
	Unconditional Stable: K	17.23(>1)
	Drain Efficiency	12.85%
	IIP3	3.7dBm
	OIP3	5.2dBm
	DC current of PA	17.42mA
Transmitter	LO leakage	-44dBc
	Image Rejection	-32.1dBc
	LO+2BB	-71.9dBc
	LO+3BB	-49.9dBc
	S22	< 0dB

	R {Z22}	**> 0Ω**
	Output Power	**3.5dBm**
	Power consumption	**48.22mW**
	Frequency deviation	**5.4%**
	Out of band spurious@ 1.2GHz	**-58.2dBm (<-47dBm)**
	Out of band spurious @ 7.2GHz	**-42.8dBm (<-30dBm)**
	Chip Size	**1812umx1787um**

Chapter4

EXPERIMENTAL RESULTS

The chip, a transmitter that integrates quadrature modulator, quadrature VCO and power amplifier in the same chip, is designed and fabricated. This chapter is presenting chip layout, measurement setup and experimental results. Measured performances are taken into discussion and comparison with post-simulations.

4.1 LAYOUT DESCRIPTIONS

All N-MOS devices are arranged with deep n-well technique supported by TSMC .25-μm single-poly-five-metal (1P5M) CMOS technology. The technique allows source and substrate of an individual N-MOS to be connected to avoid body effect. As all circuits are fully differential configuration, the components are disposed symmetrically as far as possible. Dummy gates and dummy resistors are equipped at the margins of every MOS device and resistor respectively to cope with process variation.

The whole chips, excluding pads, are surrounded with double guard rings for stable electric potential on substrate. Every spiral inductor keeps proper distances with the others and the core circuit to prevent mutual inductance and disturbance on circuit working. Signal paths should be as short as possible in metal route to alleviate

transmission line effect. Any DC pad is recommended not to locate between two differential-signal pads so that signal lines, connected to signal pads with bond-wires, on the external board is not restricted by DC lines. Wide metal lines are used for drain and source of the PA output transistor to reduce the parasitic components, i.e. inductance and resistance, and increase current handling capability. To lower the resistance and higher the current density in the output paths, the output paths are connected with stacked metal layers connected with a maximum number of vias, to ensure the huge current will not cause electron migration problem.

Fig.43 shows the transmitter layout. The chip area of the transmitter is 1812μm×1787μm ,including pads.

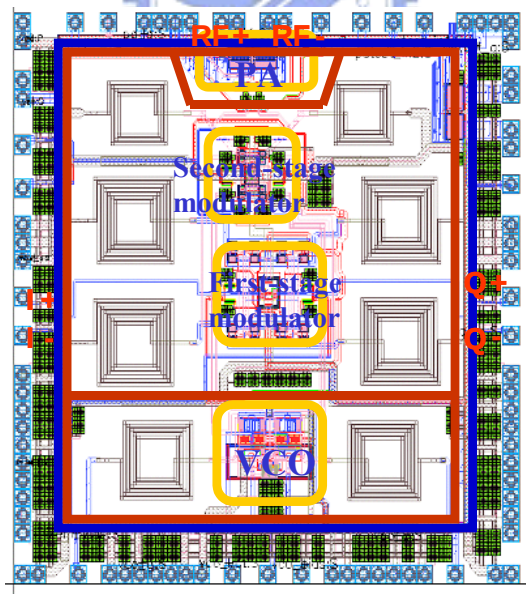


Fig.43 Transmitter layout

4.2MEASUREMENT SETUP

The measurement setup of transmitter and the respective bonding boards are

shown in Fig.44.

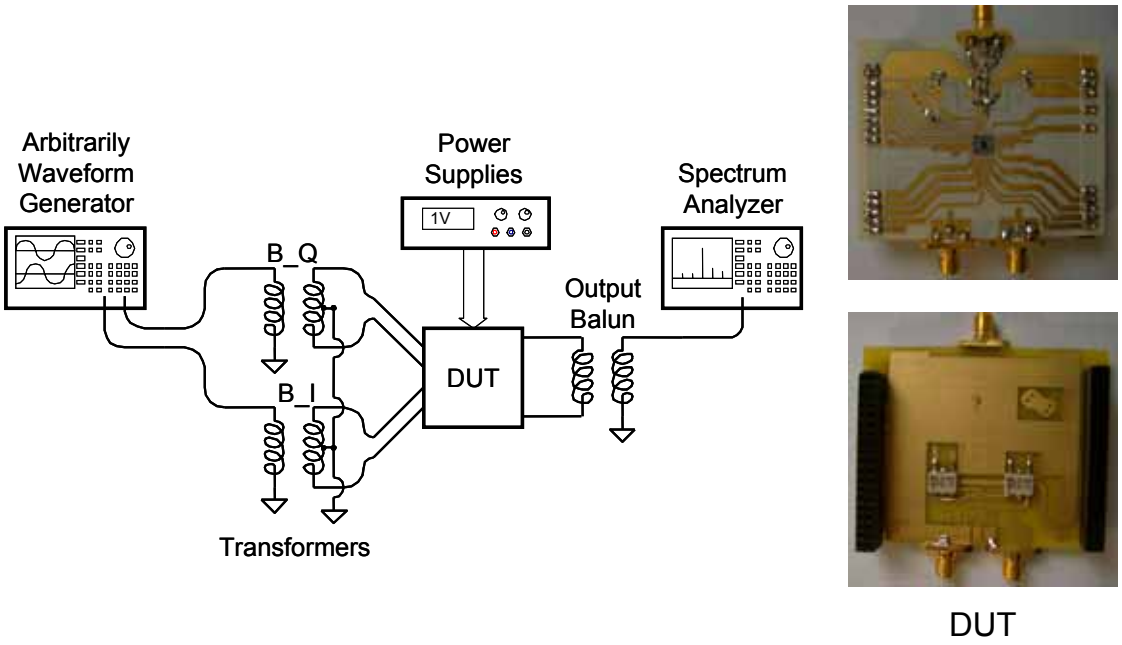


Fig.44 Measurement setup of transmitter

In Fig.44, the arbitrarily waveform generator generates the baseband I/Q signals with 90 degree phase delay. The output balun converts differential signal to single again, and send it into the spectrum analyzer. The output power will be shown on the spectrum analyzer screen.

The transformers used in Fig.44 is made by Minicircuits, the model number is ADT2-1T. Fig.45 shows the configuration type of the transformer. The insertion loss and the return loss are shown in Fig.46 and47, respectively.

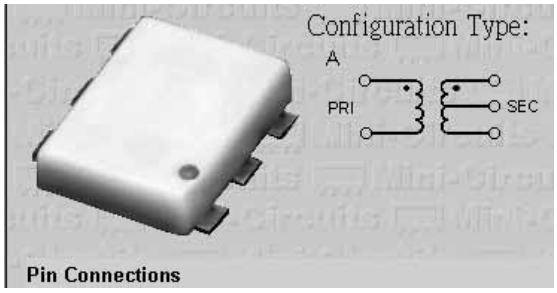


Fig.45 Minicircuits transformer ADT2-1T

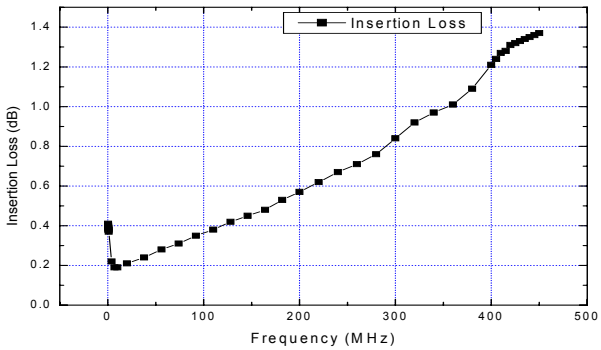


Fig.46 The transformer insertion loss versus frequency

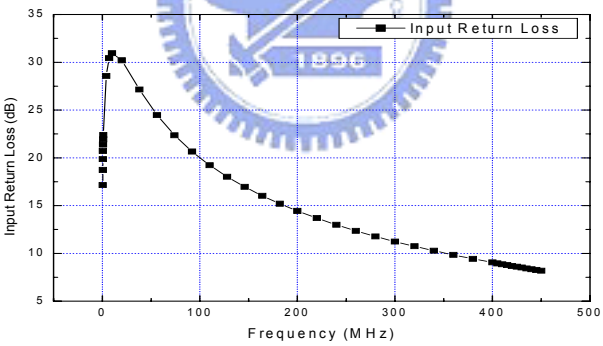


Fig.47 The transformer input return loss versus frequency

The balun used in Fig.44 is made by Advanced Ceramic X Corporation. The part number is BL2012- 10B2450. The balun photo is shown in Fig.48. Fig.49, Fig.50, and Fig.51 show the Insertion Loss and Return Loss, provided by Advanced Ceramic X Corporation.

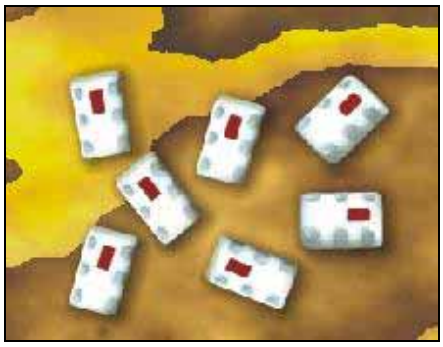


Fig.48 The balun photo

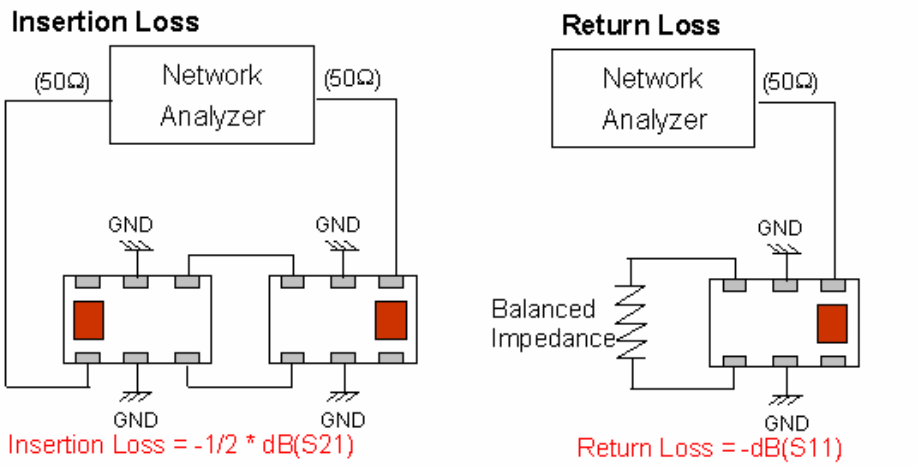


Fig.49 Insertion loss and return loss measuring diagram

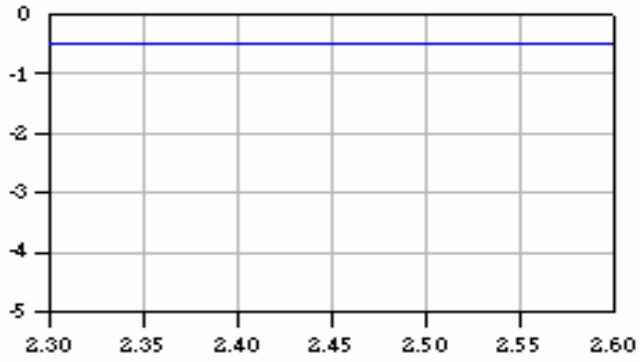


Fig.50 Insertion loss of the balun

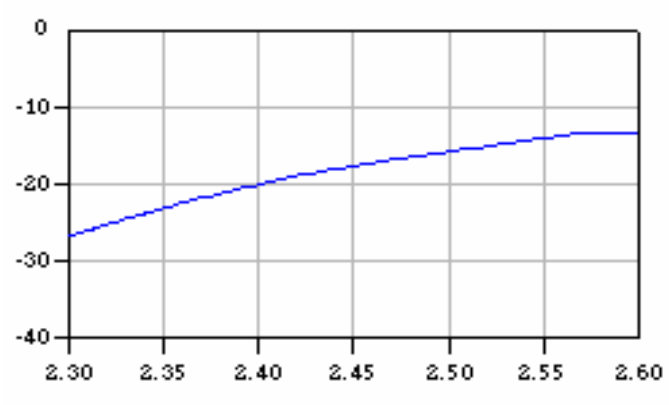


Fig.51 Return loss of the balun

The transmitter chip is bare dies and need to be bonded on board. The chip microphotograph is shown in Fig.52. Every bias terminal is fed externally for flexible adjustment. Three parallel capacitors, 0.1 μF, 10uF and 1000μF, connect the voltage source and ground to filter noise from the power supply.

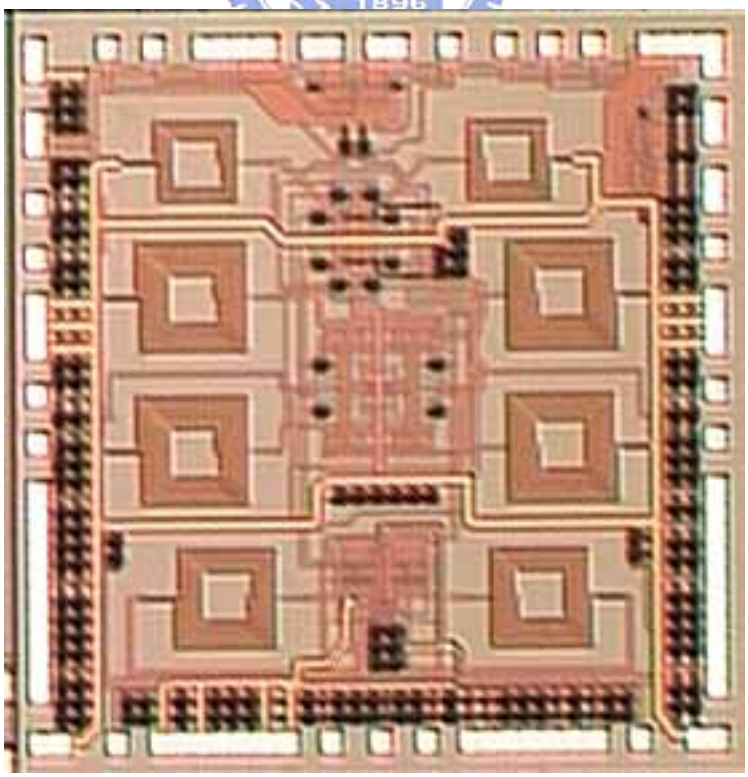


Fig.52 The chip microphotograph

4.3 EXPERIMENTIAL RESULTS

Fig. 53 shows the tuning range of VCO. It is 2580-MHz~2796-MHz by 0V~1V control voltage. The range is 216-MHz, and the frequency is shift-up 180-MHz than post-simulation. Fig.54 is the phase noise of VCO, and it is –87.39dBc/Hz by offset 100KHz, –95dBc/Hz by offset 1MHz. In this transmitter design, there is no output buffer at VCO. The measured phase noise is the LO leakage signal in the output port of PA. The measured phase noise has been modulated in the two-step modulator, the measured data is worse than the simulation's data. The phase noise in post-simulation is –98dBc/Hz at 100KHz offset and –120dBc/Hz at 1MHz offset. The phase noise can express as: $L\{\Delta f\} = kT(1+\alpha F)Z_0(\frac{1}{Q})(\frac{f_c}{\Delta f})^2(\frac{1}{V_{rms}^2})$, where k: Boltzmann's constant, T: absolute temperature, α : the number of times the negative conductance exceeds the tank loss to assure the start-up, F: the noise factor of the CMOS negative resistor. Due to the Q factor reducing, the phase noise is higher than post-simulation. The DC current of VCO is 18.5mA, and the DC current of modulator is 15.1mA.

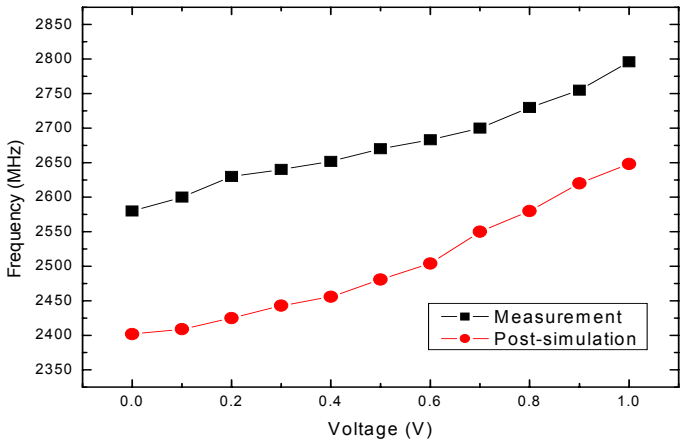


Fig.53 The tuning range of VCO

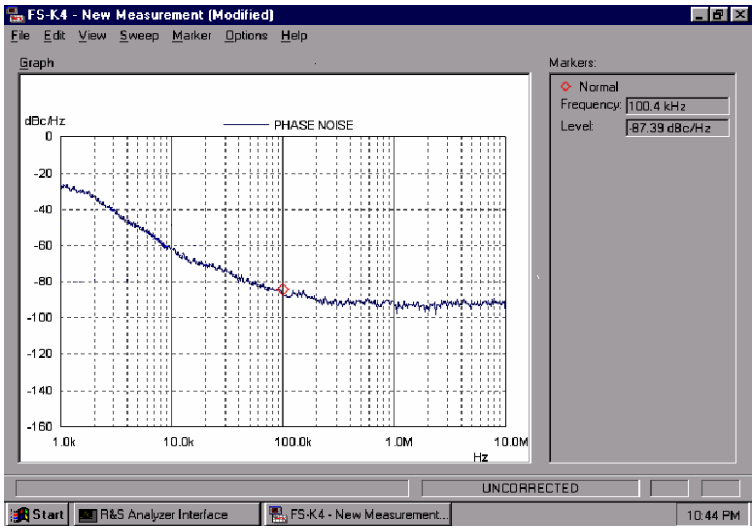


Fig.54 The phase noise of VCO

Fig. 55 is the S11 of PA; it is about –10.1dB at 2.6GHz. It explains most of power coming from modulator will go into the PA. Fig. 56 is the P-1 dB of the PA; the value is about –0.5dBm. Fig. 57 shows the two input tones of PA, they are 2.59-GHz and 2.6-GHz. Fig. 58 is the measurement result, the IIP3 is 11dB and the OIP3 is 11.8dBm. Fig.59 is the ACPR of PA. It can meet the Bluetooth specification. The DC

current of PA is 19.2mA.

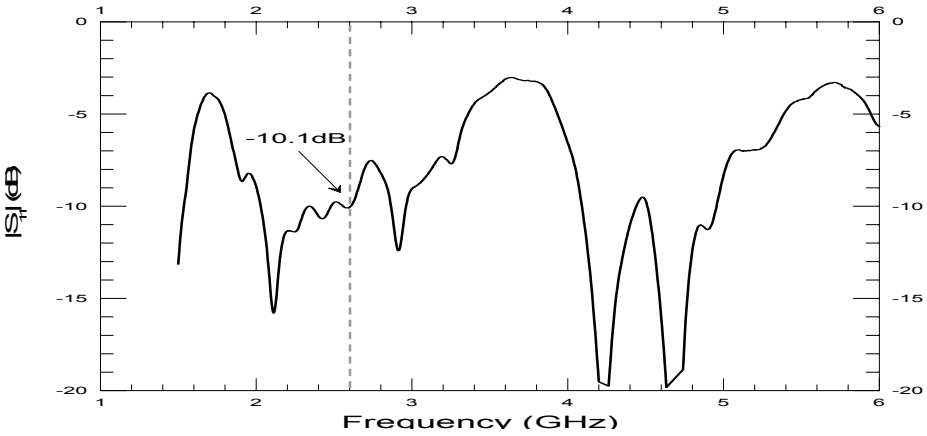


Fig.55 The S11 of PA

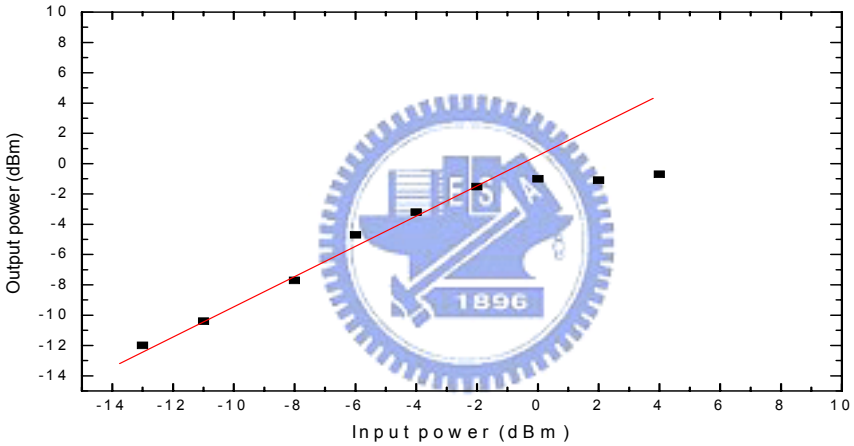


Fig.56 The P-1dB of PA

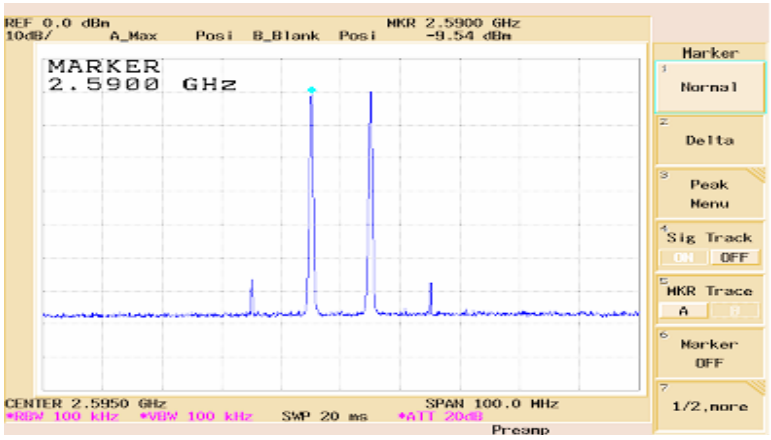


Fig.57 Two tones of IP3

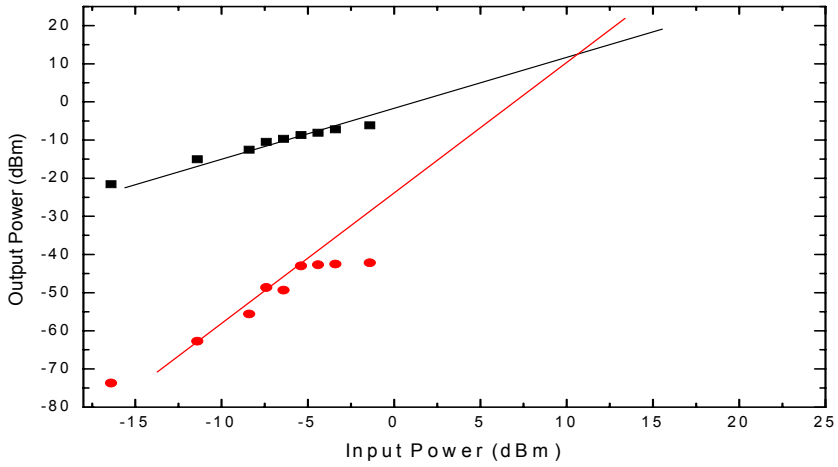


Fig.58 IP3 of PA

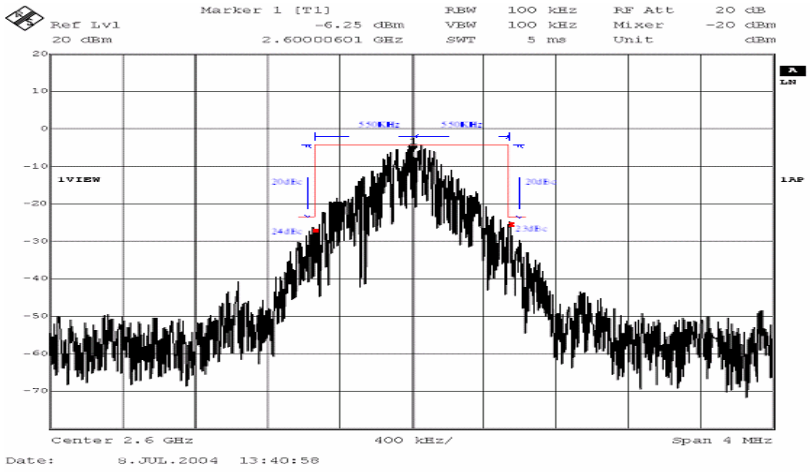


Fig.59 ACPR of PA

Fig. 60 is the in band spurious emission of transmitter, the LO leakage is –37.5dBc, the image rejection is –30.4dBc, the LO+2BB is –41dBc, and theLO+3BB is –50.3dBc. They can meet the –20dBc specification of Bluetooth. The out of band spurious emission is shown at Fig.61. The emission is –56.3dBm at 1.3GHz, -38.5dBm at 3.9dBm, -50.2dBm at 5.2GHz, -53.8dBm at 6.5GHz, -44.2dBm at 7.8GHz. The Bluetooth limit is shown at Fig.62. The blue line is operation mode

limit; the red line is the idle mode limit. This is a transmitter structure and it should meet the operation mode limit, but the 1.3GHz spurious should meet the idle mode limit, too, because of it coming from VCO leakage and existing in the two modes. All emissions can meet the Bluetooth's specification.

Fig. 63 is the output power of transmitter. The optimal input baseband signals are 100mV (peak to peak). If the input baseband signals are much smaller than the optimal signals, the noise will affect the signals. If the input baseband signals are much larger than the optimal signals, the linearity will become worse. The input optimal 100mV signal can get the maximum output power. Re-compensating the 3dB cable and balun lose, the output power is only –11dBm at 2612MHz. The post-simulation is about 0dBm. The main causes of power loss will be discussed in the next section.

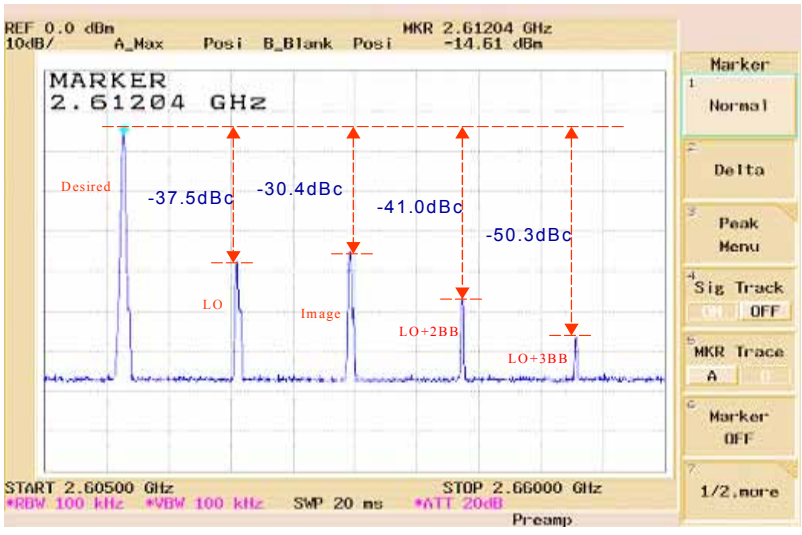


Fig.60 In band spurious emission of transmitter

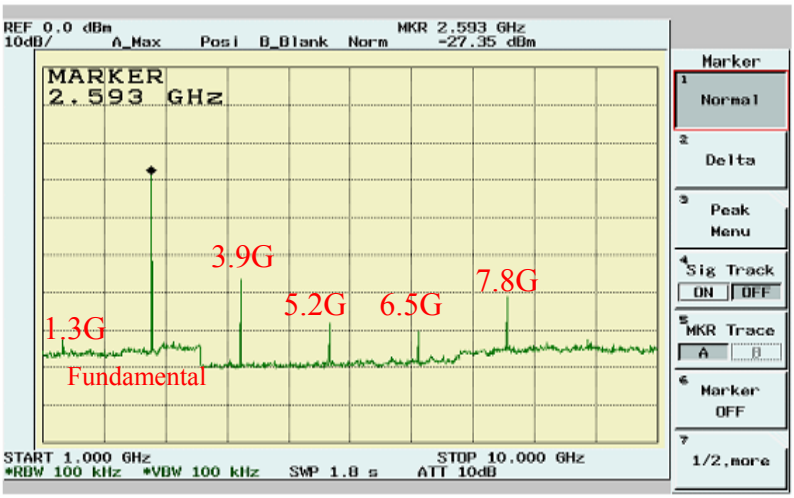


Fig.61 Out of band spurious emission of transmitter

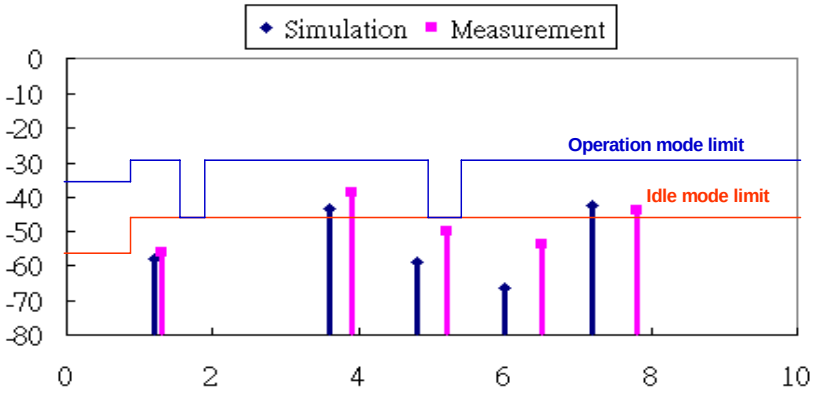


Fig.62 The limit of out of band spurious emission

Fig.63 The output power of transmitter

4.5 EXPERIMENTIAL DISCUSSIONS

The output power of the transmitter is only –11dBm. The main causes of power loss are two: (1) the reducing Q factor of the VCO's spiral inductor (2) the parasitic capacitors of the deep N-well.

(1) The reducing Q factor of the VCO's spiral inductor.

Fig.64 shows the layout of the VCO's spiral inductor, the lead of inductor is too long to ignore the parasitic resistor. We use the ADS momentum to find this problem. In Fig.65, two spiral inductors are setting. The reference one is the standard TSMC 5.5 turns inductor. The other one is this design's inductor. Excitation is at port1, and the signal is received at port2. The relative permittivitys of silicon and oxide are 11.8 and 4.

Fig.66, Fig.67 are the simulation's results. In the result, the resistor increases 50% at 1.2GHz, the inductor reduces 0.23nH at 1.2GHz, and the Q factor reduces 1.5 at 1.2GHz. Fig.68 is the result of re-simulating the Q factor's deviation by H-spice. When the resistor is increasing 50%, the output power will be reduced to –5dBm~-6dBm.

The Q factor is reduced and the magnitude of the VCO is also reduced. When increasing the voltage of VCO's power-supply from 1-V to 1.5-V, the magnitude of

the VCO is arising and the output power will increase from –11dBm to –6dBm. It can prove the issue. Fig.69 shows the relationship of output power and supply voltage.

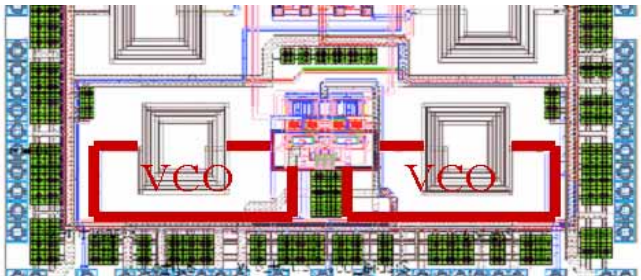


Fig.64 The layout of VCO

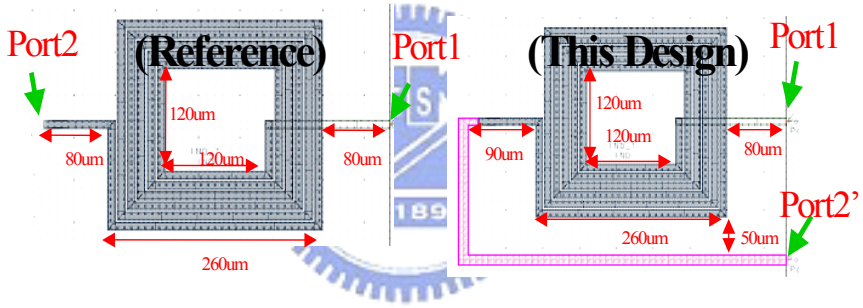


Fig.65 Simulation by ADS Momentum

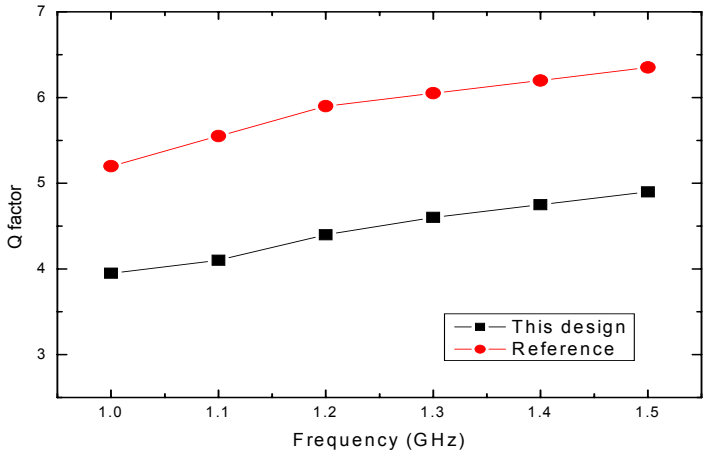


Fig.66 The Q factor of ADS Momentum simulation result

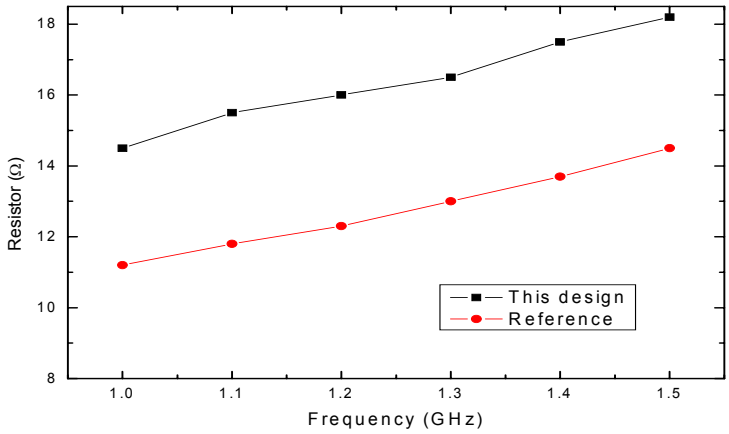


Fig.67 The resistor of ADS Momentum simulation result

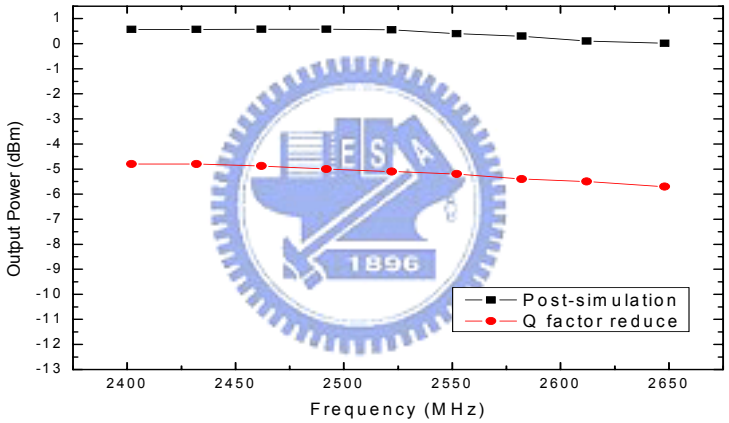


Fig.68 Re-simulation the effect of Low Q

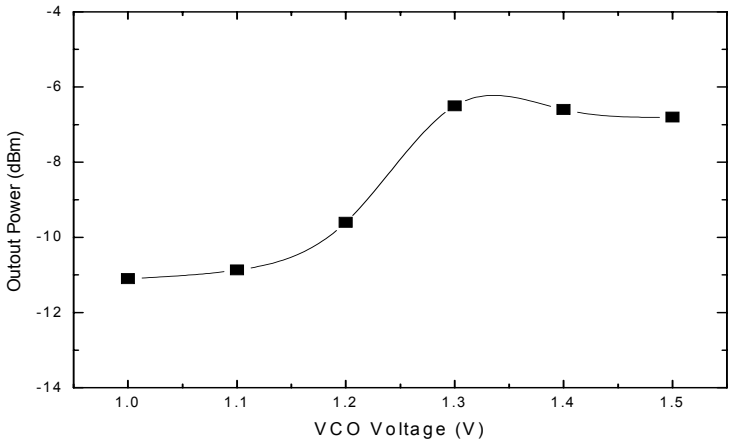


Fig.69 Increase the voltage of VCO's power supply

(2) The parasitic capacitors of the deep N-well.

Fig.70 shows the structure of the deep N-well MOS. In this structure, the depletion capacitor exists on the interface of p-well/ n-well and p-well/ deep n-well. Due to the short circuit of source and substrate, the depletion capacitor can be shown in Fig.71, and it does affect on the output waveform of the cascoded MOS. The depletion capacitor on PA is about 1.88pF, on first-stage modulator is about 1.71pF, and on second-stage modulator is about 0.73pF.

Fig.72 is the re-simulation result of output power and frequency. The upper line is the post-simulation's result, and the output power is about 0dBm. The middle line is the re-simulation's result of reduced Q factor, and the output power is about -5dBm. The lower line is the re-simulation's result of reduced Q factor and parasitic capacitor, and the output power is about -10dBm. We can find the output power is very similar to the measurement.For the depletion capacitor issue, we can use the substrate bias to solve it. In Fig.73 the substrate is biased at 0.4-V, and re-simulate again. The result is shown in Fig.74. In Fig.74, when the circuit is re-designed as substrate bias, the output power will arise from –5dBm to 0dBm similar to the result of post-simulation. Table XVII is the summery of the measurement.

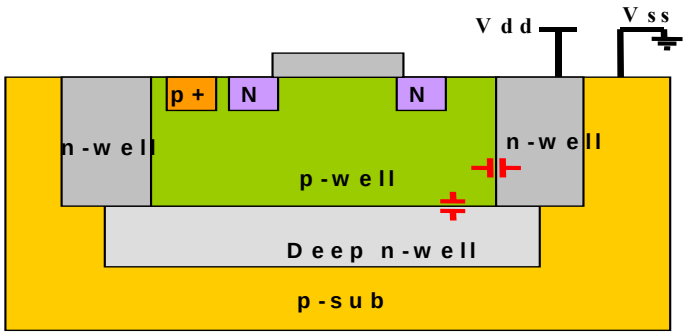


Fig.70 The structure of deep N-well

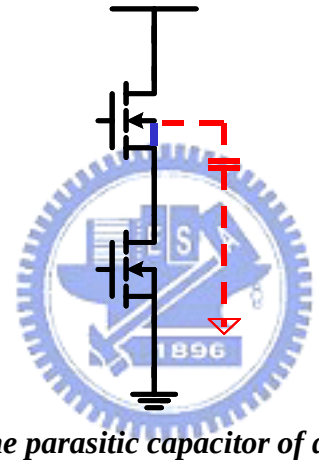


Fig.71 The parasitic capacitor of deep N-well

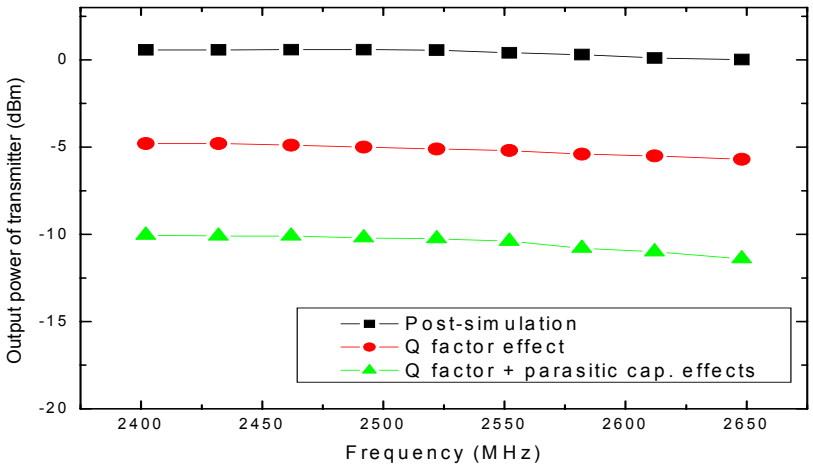


Fig.72 Re-simulation the two factors of output power

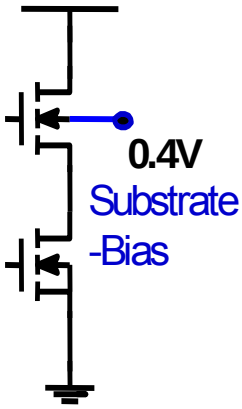


Fig.73 Substrate bias

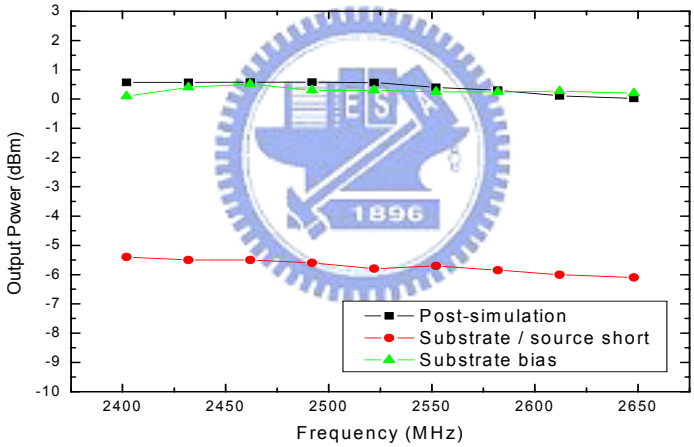


Fig.74 Substrate bias re-simulation

Table XVII The summery of measurement

Parameter		Post-Simulation	Measurement	Bluetooth Spec.
VCO	Frequency Range	2.4-GHz ~	2.58GHz ~ 2.79GHz	2.4GHz ~ 2.483GHz
	Tuning Range @ Vc=0~1V	250MHz	210MHz	83.5MHz
	Phase Noise @100KHz &1MHz	-98, -120 (dBc/Hz)	-87.39, -95 (dBc/Hz)	--
	DC current of VCO	13.7mA	18.5mA	--
Modulator	DC current of Modulator	17.10mA	15.1mA	--
PA	ACPR	--	22dBc	20dBc
	P-1	-1.5dBm	-0.5dBm	--
	IIP3	3.7dBm	11dBm	--
	OIP3	5.2dBm	11.8dBm	--
	DC current of PA	17.42mA	19.2mA	--
Transmitter	LO leakage	-44dBc	-37.5dBc	-20dBc
	Image Rejection	-32.1dBc	-30.4dBc	-20dBc
	LO+2BB	-71.9dBc	-41.0dBc	-20dBc
	LO+3BB	-49.9dBc	-50.3dBc	-20dBc
	Output Power (SS-FF)	0.02~6.9dBm	-11dBm	0dBm (ClassIII)
	Power consumption	48.22mW	52.8mW	--
	Spurious@ 1.2GHz (Idle)	-58.2dBm	-56.3dBm	-47dBm
	Spurious @ 3.6GHz (Operation)	-43.5dBm	-38.5dBm	-30dBm
	Supply voltage	1V	1V	--
	Die Size	1812umx1787um		--
	Technology	TSMC 0.25um 1P5M CMOS		--

Chapter5

CONCLUSIONS AND FUTURE WORKS

5.1 CONCLUSIONS

In this thesis, a 1-V 2.4-GHz RF transmitter, which integrates two modulators, a VCO, and a PA in a single chip is designed, fabricated and measured.

The improved two-step architecture is used to eliminate off-chip bandpass filters.

Only one VCO is used to reduce the power consumption and chip area.

Using the 1-V of power supply, the designed transmitter is suitable for low-voltage, low-power wireless applications.

The effects of Q factor in inductors and capacitors in deep N-well are included to analyze the differences between measurement and simulation results.

It is fabricated in a standard 0.25μm 1P5M CMOS process without any additional process tweaking. The prototype transmitter chip consumes only 1.8x1.8 mm^2 of active area. The operation current of the fabricated transmitter is 52.8mA from a 1V power supply voltage.

The measured LO leakage, image ratio, LO+2BB, LO+3BB of the modulated

signal at the output of transmitter is –37.5dBc, -30.4dBc, –41dBc, -50.3dBc, respectively.

The measured out of band spurious is –38.5dBm.

The output power is only -11dBm.Through measured results, the performance of the proposed CMOS RF transmitter has been verified to be well suitable for short-range communication applications and can meet Bluetooth output power level class III (-30dBm~0dBm).

5.2 FUTURE WORKS

In the implementation of "A 1V 2.4GHz CMOS Transmitter with Improved Two-Step Architecture" has been realized. However, the output power is low than expectancy. In the future, we will tapeout the re-design IC to work at 1-V supply voltage and have 0dBm output power.

The power loss is mainly caused by the low quality factor of the spiral inductor. This drawback can be resolved by using advanced IC technologies, which has thick metal layer or copper metal layer process. In addition, the optimal metal width of the spiral inductor and the special structure of the spiral inductor can also improve the quality factor of spiral inductor. In simulation, the parasitic resistor on the lead of spiral inductor should be concerned.

The second factor of the power loss is the parasitic capacitor of the deep N-well. Using substrate bias or adding a resistor between source and substrate can resolve this drawback. Thus, the power loss will be decreased due to the parasitic capacitor disappearance.

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