國 立 交 通 大 學

材料科學與工程學系

博 士 論 文

應用在金氧半電晶體之原子層沉積氧化鋁與砷化銦鎵、砷化銦介面之研究

Study of Atomic Layer Deposition Al_2O_3/InGaAs, InAs Interfaces for MOSFET Application

研 究 生： TRINH HAI DANG（金海光）

指導教授： 張 翼 博士

中 華 民 國 一 百 年 八 月

Study of Atomic Layer Deposition Al_2O_3/InGaAs, InAs Interfaces for MOSFET Application

研 究 生：金海光　Student: Trinh Hai Dang

指導教授：張 翼 博士　Advisor: Prof. Edward Yi Chang

國立交通大學

材料科學與工程研究所

博士論文

A Dissertation

Submitted to Department of Materials Science and Engineering

College of Engineering

National Chiao Tung University

In Partial Fulfill of the Requirements

For the Degree of

Doctor of Philosophy

August 2011

Hsinchu, Taiwan, Republic of China

中華民國 一 百 年 八 月

摘要

本論文集中研究減少 InGaAs 和 InAs 原生氧化層藉由使用數種表面處理和氣體退火條件去改善原子氣相沉積（ALD）Al_2O_3/InGaAs, Al_2O_3/InAs 介面品質。三甲基鋁（TMA）製程及濕式化學溶液製程這兩種製程的結合與影響被提出。

使用乾式 TMA 來減少 InGaAs, InAs 表面的原生氧化層只有在第一次脈衝有效，接下來便無效。本研究中指出原生氧化層可以被顯著的移除，藉由使用濕式化學溶液製程，例如 HCl 或 sulfide(硫化物)。然而，結合兩種方法（濕式化學溶液製程與 TMA 預先處理）對於 InGaAs,InAs 表面處理是最為有效的方式。

Al_2O_3/InAs MOSCAPs 的電性指出對於改善 Al_2O_3/InAs 介面品質 HCl 加上 TMA 比起 sulfide 加上 TMA 是更有效果的。這個結果是由以下實驗觀察所得：ALD Al_2O_3 薄膜在 200˚C 下沉積。300˚C 下沉積 ALD Al_2O_3 薄膜再次驗證。同時本研究模擬 Al_2O_3/InAs 結構在低頻的 C-V。結果顯示界面缺陷密度（D_{it}）分佈表現出 U 形在最小的 D_{it} 分佈位於 InAs 傳導帶最低處,i.e. 類施體陷阱在此能隙裡支配。這些類施體陷阱會顯著的減少藉由使用濕式化學溶液製程加上 TMA 預先處理。

藉由使用濕式化學溶液製程加上 TMA 預先處理和在純氫氣裡沉積後退火，對於 $Al_2O_3/In_{0.53}Ga_{0.47}As$ 界面品質有顯著提昇。使用 ex-situ 方法，強力的 C-V 反轉行為第一次被觀察到在 $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP。低 D_{it} 分佈可藉由模擬觀察到，同時模擬及電導法可確認最小 D_{it} 值 ~10^{11} $eV^{-1}cm^{-2}$。

Al_2O_3/InGaAs,InAs 的電性表現不僅受與表面處理方法影響，同時也跟半導體本身性質有關。這些半導體參數例如：能隙、電子遷移率及 Al_2O_3/InGaAs 結構的 C-V、I-V 本質濃度特性都被討論。

ABSTRACT

This dissertation concentrates on the study of the reduction of InGaAs and InAs native oxides by using several kinds of surface treatments and gas annealing conditions to improve the atomic layer deposition (ALD) Al_2O_3/InGaAs, Al_2O_3/InAs interfaces qualities. Effects of trimethyl aluminum (TMA) treatment, wet chemical surface treatments, and a combination of these two kinds of treatments are investigated.

The use of dry TMA treatment for the reduction of InGaAs, InAs native oxides at surface was only effective in the first pulse and then it became effectless. The study shows that the native oxides could be significantly removed by using wet chemical solution treatments such as HCl or sulfide. However, the combination of wet chemical solution treatments plus TMA pretreatment is the most effective way for InGaAs, InAs surface treatment.

Electrical characterization of Al_2O_3/InAs MOSCAPs showed that the HCl plus TMA treatment was more effective in the improvement of Al_2O_3/InAs interface quality than that of sulfide plus TMA treatment. This conclusion was observed for the samples which were deposited with ALD Al_2O_3 films at 200°C and was confirmed again for the samples deposited with ALD Al_2O_3 films at 300°C. Low-frequency C-V simulations were performed for the Al_2O_3/InAs structures and the extracted interface traps density D_{it} profiles present a U-shape with the minimum of the D_{it} profiles located around the InAs conduction band minimum, i.e. donor-like traps dominates inside the bandgap. These donor-like traps were significant reduced by using wet chemical plus TMA treatments.

By using the chemical solution plus TMA treatment along with post deposition annealing in pure H_2 gas, a significant improvement of Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface quality was obtained. A strong C-V inversion behavior was first time observed in Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSCAP by using an ex-situ method. Low D_{it} profile extracted by simulation was observed and the minimum D_{it} value of ~10^{11} $eV^{-1}cm^{-2}$ was confirmed by both simulation and conductance method.

The electrical characteristics of Al_2O_3/InGaAs, InAs not only depend on the surface treatment methods but also depend on the properties of semiconductors themselves. The effect of semiconductor parameters such as bandgap, electron mobility, and intrinsic concentration on the C-V, I-V characteristics of Al_2O_3/InGaAs structures are discussed.

ACKNOWLEDGMENTS

The author gratefully acknowledges Chiao Tung University (NCTU), Taiwan and the Compound Semiconductor Device Laboratory (CSD Lab), NCTU, Taiwan for supporting this research.

I firstly would like to express my deep gratitude to my supervisor, Prof. Edward Yi Chang for his guidance, support and patience during my Ph.D time at CSD Lab. I appreciate the freedom in research he provided and the taking care he intended for me at the beginning I joined NCTU. He is always kind to me and his encouragement was a driving force for me in study. I really admire his ability in working and research.

This work could not succeed without the support of some people to them I'd like to give my thanks. I am really indebted to Dr. Lin Yueh Chin, Wong Yuen Yee, Yu Chih Chieh (ITRC), Dr. Kuo Chien I, Nguyen Hong Quan, Dr. Lin Kung Liang, and Tran Binh Tinh for their constant help of experiments and valuable discussions. Thanks to them not only in the research but also the good friendships and the fun they brought to me, especially Yuen Yee, Hong Quan. I also appreciate Dr. Chung Yu Lu, Dr. Chang Chia Ta, Hsieh Yi Fan, Dr. Chang Chia Yuan, Chung Chen Chen, and Chiu Yu-Sheng for their kindly supports of experiments.

Many thanks to my colleagues and good friends including Le Minh Thu, Bui Duc Tinh, Dai Van Truong, Do Thi Hien, Oh Chi Way, Nguyen Chi Lang for the enjoyable times we shared together. Thanks also to my NCTU-FSA team including Maria, Sumer, Martin, Leo, and Korniyenko and NCTU-VSA members for the wonderful extracurricular activities, parties and jolly football matches. My Ph.D. time would be less meaningful without them.

Last but not least, this work dedicates to my dearest parents, my wife and my brothers. I wish to thank to my parents who are always beside me all time and give me a strong hope and belief. Thanks to my wife, Them who has been brought to me the love, happiness and joy. I am so happy to have her in my life. Thanks to my younger brothers, Tat Dat and Trong Duc for their fondness for me. They are also a motive power for me to strive for this work.

DEDICATION

To

My dearest Parents, my Wife, and my Brothers

CONTENTS

Abstract (Chinese) i

Abstract (English) ii

Acknowledgment iii

Dedication iv

Contents v

List of figures viii

List of tables xiv

List of symbols xv

List of acronym xvii

1. INTRODUCTION 1

1.1. An Overview of planar Si-based CMOS Technology 2

1.2. High k, metal gate solutions 4

1.3. Scaling challengers and future trends 9

1.3.1. Scaling challengers 9

1.3.2. Future trends 10

1.4. III-V compound semiconductors for CMOS technology: motivation, challenges and current progress 11

1.4.1. Motivation 11

1.4.2. Challengers 14

1.4.3. Current progress 15

1.5. Problem statement and objective of the dissertation 17

1.6. Organization of the dissertation 18

References 19

2. FABRICATION AND CHARACTERIZATION METHODS 25

1.2. Fabrication techniques 26

2.1.1. Atomic layer deposition (ALD) 26

2.1.2. Electron beam evaporation 30

2.2. Fabrication process 31

2.3. Analytical techniques ... 33
2.3.1. X-ray photoelectron spectroscopy (XPS) ... 33
2.3.2. High-resolution transmission electron spectroscopy (HRTEM) ... 39
2.4. Electrical techniques ... 41
2.4.1. Capacitance-voltage (C-V), conductance voltage (G-V) measurements ... 41
2.4.2. Current-voltage (I-V, J-V) measurements ... 45
2.4.3. Conductance and conductance map methods ... 46
References ... 51

3. EFFECTS OF WET CHEMICAL AND TMA TREATMENTS ON THE INTERFACE PROPERTIES IN ALD OF AL_2O_3 ON INAS ... 52
3.1. Introduction ... 53
3.2. Experiment ... 53
3.3. Results and discussion ... 54
3.3.1 Effect of TMA treatment ... 54
3.3.2. A combination of wet chemical treatments and TMA pretreatment ... 56
3.4. Conclusions ... 60
References ... 61

4. ELECTRICAL CHARACTERIZATION OF AL_2O_3/N-INAS MOSCAPS WITH VARIOUS SURFACE TREATMENTS ... 64
4.1. Introduction ... 65
4.2. Experiment ... 65
4.3. Results and discussion ... 66
4.3.1. X-ray photoelectron spectroscopy ... 66
4.3.2. Capacitance-voltage characteristics ... 67
4.3.3. Simulation and D_{it} profiles extraction ... 69
4.4. Conclusions ... 70
References ... 72

5. THE INFLUENCES OF SURFACE TREATMENT AND GAS ANNEALING CONDITIONS ON THE INVERSION BEHAVIORS OF THE ATOMIC LAYER DEPOSITION AL_2O_3/N-$IN_{0.53}GA_{0.47}AS$ MOSCAP ... 74

5.1. Introduction ... 75
5.2. Experiment ... 75
5.3. Results and discussion ... 76
5.3.1. Capacitance-voltage characterization ... 76
5.3.2. X-ray photoelectron analysis ... 78
5.3.3. D_{it} extraction by simulation and conductance methods ... 80
5.4. Conclusions ... 81
References ... 83

6. INVESTIGATION OF ELECTRICAL CHARACTERISTICS OF AL_2O_3/N-$IN_XGA_{1-X}AS$ (X = 0.53, 0.7) AND INAS CAPACITORS ... 85
6.1. Introduction ... 86
6.2. Experiment ... 86
6.3. Results and discussion ... 87
6.3.1. X-ray photoelectron spectroscopy analysis ... 87
6.3.2. High-resolution transmission electron microscopy micrographs ... 87
6.3.3. Electrical characteristics ... 89
6.4. Conclusions ... 93
References ... 95

7. CONCLUSIONS ... 97

Biography ... 99

List of publications ... 100

LIST OF FIGURES

Figure 1.1. "The number of transistors incorporated in a chip will approximately double every 24 months": Moore's Law Timeline (solid) and the number of transistors per chip in Intel's products (line plus symbols). The inset is Moore's original prediction graph in 1965 2

Figure 1.2. Scaling of logic technology node and correspond transistor's physical gate length (According to Intel's introduction until 2009 and ITRS update 2008) 3

Figure 1.3. Leakage current versus voltage for various thicknesses of SiO_2 layers 5

Figure 1.4. At the gate oxide thickness of 1.2 nm (5 layer of atoms), the wave describing the probable location of an electron is broader than the gate oxide and the electron can simply appear on the other side of gate oxide, means that direct tunneling of electrons through the insulation. New high k gate oxide is needed to plug the leak 5

Figure 1.5. Static dielectric constant versus band gap for candidate gate oxides 6

Figure 1.6. a-Electron density in PolySi gate is not large enough to screen the effect of high k dipoles on semiconductor lattice points, lead to strong phonon-electron scattering; b-Experimental evidence of phonon scattering in the high k dielectric. The net value of the temperature (T) sensitivity factor, $d(1/\mu_{eff})/dT$, is negative when coulombic scattering dominates and positive when phonon scattering dominates. [21]; c-Metal gate with high electron density can screen out the vibrations, reduce effect of phonon scattering; d-Experimental (symbols) and simulation (dash lines) data show the improvement of electron mobility by using high k/metal gate stack 8

Figure 1.7. The improvements of leakage current and drive currents by using high k metal gate generations 9

Figure 1.8. Illustration of the exponential decrease in switching energy (left) and the simultaneously increasing device power density (middle) as a consequence of device downscaling. The increase of power density causes of power consumption issue, lowering supply voltage is not an easy way to reduce power consumption due to the increase of off state current, I_{off} (right) 10

Figure 1.9. Non-planar transistors: Double-gate transistor (left) and tri-gate transistor (right) 10

Figure 1.10. Electron velocities as a function of field of Si, Ge and III-V compound semiconductors. III-V compound semiconductors exhibit high saturation velocity at low electric field 11

Figure 1.11. III–V HEMTs characteristics compared with standard silicon MOSFETs a, Intrinsic gate delay. b, Normalized energy-delay product of n-channel InSb and InGaAs HEMTs 14

Figure 2.1. The 8 inch ALD system at instrument technology and research center (ITRC), Hsinchu, Taiwan. This system was mostly used for the deposition of high k oxides in this work 26

Figure 2.2. Schematic illustration describing an ALD deposition cycle leading to the formation of a binary oxide film consisting of metal (•) and oxygen (◦) atoms. L refers to the precursor ligand 27

Figure 2.3. Schematic describing the alternating TMA and H_2O pulses in ALD chamber leading to form sequence Al_2O_3 layers 28

Figure 2.4. Scheme of (a) ALD processing window limited by (b) precursor condensation, (c) insufficient reactivity, (d) precursor decomposition and (e) precursor desorption. If deposition rate is dependent on the number of available reactive sites as in (f), no actual ALD window is observed 28

Figure 2.5. Saturation of surface reactions in ALD processes is experimentally verified by observing that the deposition rate per cycle stabilizes to a constant level with increasing precursor pulse time or dose 30

Figure 2.6. Schematic of electron beam evaporation system for metal deposition 31

Figure 2.7. The Al_2O_3/InGaAs, InAs MOSCAPs structures used in this work 31

Figure 2.8. Process flow of Al_2O_3/InGaAs, InAs MOSCAPs fabrication, focusing on the interface engineering 32

Figure 2.9. Surface irradiated by sufficient energy X-ray photon beam will emit photoelectrons: phenomenon (left) and principle schematic (right) 33

Figure 2.10. (a) The X-ray photon transfers its energy to a core-level electron leading to photoemission from the n-electron initial state. (b) The atom, now in an (n-1)-electron state, can reorganize by dropping an electron from a higher energy level to the vacant core hole. (c) Since the electron in (b) dropped to a lower energy state, the atom can rid itself of excess energy by ejecting an electron from a higher energy level. This ejected electron is referred to as an Auger electron. The atom can also shed energy by emitting an X-ray photon, a process called X-ray fluorescence 35

Figure 2.11. XPS survey scan of Al_2O_3/InAs sample, the inset shows As 3d spectra 36

Figure 2.12. Schematic design of an X-ray photoelectron spectrometer 37

Figure 2.13. The energy level diagram for an electrically conducting sample that is grounded to the spectrometer. The Fermi levels of the sample and spectrometer are aligned ($E_{F(s)} = E_{F(sp)}$) so that E_B is referenced with respect to E_F. The measurement of E_B is independent of the sample work function, φ_s, but is dependent on the spectrometer work function, φ_{sp} 38

Figure 2.14. The control windows of XPSPEAK software, version 4.1........................... 39

Figure 2.15. Principle schematic of a transmission electron microscopy (TEM)............. 40

Figure 2.16. Rectangular approximation method used by 4156C 43

Figure 2.17. QSCV measurement sequence 44

Figure 2.18. Band diagram of an n-type MOS structure with a bias voltage V_G applied between metal and semiconductor 46

Figure 2.19. Equivalent circuits for conductance measurements: (a) MOSCAP with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit, (d) including series r_s resistance and tunnel conductance G_t 47

Figure 2.20. G_p/ω versus frequency of an $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP device 49

Figure 2.21. a-G/Aωq as a function of frequency at different gate bias voltages, A is area of MOSCAP; b- G/Aωq contours as a function of both frequency and gate voltage, a more efficient and intuitive way to visualize the movement of Fermi level 50

Figure 2.22. Characteristic trapping frequencies for electron in n-$In_{0.53}Ga_{0.47}As$ at different temperatures 50

Figure 3.1. XPS spectra of As 3d and In $3d_{5/2}$ InAs samples: a-bare chip without surface treatment and after 1, 5, 10 cycles of in situ TMA pretreatment (b-d), followed by 20 cycles (~2 nm) of ALD Al_2O_3 deposition 55

Figure 3.2. XPS As 3d and In $3d_{5/2}$ spectra of InAs samples after a-HCl and b-$(NH_4)_2S$ treatments and the wet-chemical-treated samples after 10 cycles of TMA pretreatment followed by 20 cycles of ALD Al_2O_3 (c and d) 57

Figure 3.3. Multiple frequency C-V responses and bidirectional curves at frequency of 1 MHz for 10nm ALD Al_2O_3/n-InAs MOSCAP structures: a-Pure TMA pretreatment, b-HCl treatment plus TMA pretreatment, c-sulfide treatment plus sulfide pretreatment. The frequency dispersions per decade are 2.3, 1.8, and 2.3% for samples in sequence a to c, respectively 58

Figure 3.4. a- C-V responses at frequency of 1 MHz for samples with different surface treatments. b- Leakage current density versus gate voltage (J-V) of the same samples ... 59

Figure 4.1. The In $3d_{5/2}$ and As $2p_{3/2}$ XPS spectra of a- native-oxide-covered InAs surface; b- 1.5 nm ALD Al_2O_3/HCl+TMA treated InAs interface; c- 1.5 nm ALD Al_2O_3/sulfide+TMA treated InAs interface. Native oxides including In_2O_3, As_2O_3, and As_2O_5 were significantly reduced after the use of surface treatments 66

Figure 4.2. Multi-frequency C-V responses (solid lines) and QSCV curves (dashed lines) in a- control sample, b- HCl plus TMA sample, and c- sulfide plus TMA treated sample of 18 nm ALD Al_2O_3/InAs MOSCAPs; d- QSCV curves of all three samples, for comparison 67

Figure 4.3. Leakage currents versus gate voltage of samples 68

Figure 4.4. a- Experimental data (symbols), simulated C-V curves (solid lines) of ALD 18 nm Al_2O_3/n-InAs MOSCAP samples with various surface treatments. Interface state density profiles of all three samples, extracted from simulation, are shown as well: b-control sample, c- HCl plus TMA treated sample, d- sulfide plus TMA treated sample .. 70

Figure 5.1. Multi-frequency C-V responses in a- TMA treated-; b- sulfide + TMA treated Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs, with post deposition annealing in N_2 gas. The inset in figure 5.1b shows the conductance - voltage (G-V) characteristics of the sample S2....... 76

Figure 5.2. a- Multi a frequency C-V responses in sulfide + TMA treated Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs, with post deposition annealing in H_2 gas; b- The temperature dependent C-V responses at 10 kHz of the same sample. The inset in Fig. 5.2a shows the conductance-voltage (G-V) characteristics; the inset in Fig. 5.2b shows the temperature dependent C-V responses at 1 kHz 77

Figure 5.3. The As $2p_{3/2}$, In $3d_{5/2}$, Ga $2p_{3/2}$ XPS spectra of a- Native oxide-covered InGaAs surface; b- TMA treated sample, with ALD Al_2O_3, as deposited; c- sulfide + TMA treated sample, with ALD Al_2O_3, as deposited; d- TMA treated sample, with ALD Al_2O_3, after PDA in N_2; e- Sulfide + TMA treated sample, with ALD Al_2O_3, after PDA in N_2; f- Sulfide + TMA treated sample , with ALD Al_2O_3, after PDA in H_2. 79

Figure 5.4. a-The comparison of QSCV responses of sample S1, sample S2 and sample S3 and ideal C-V curve (without D_{it}) obtained by simulation. The inset shows the leakage of samples for ensuring the accuracy of measurement; b- and c- The G_p/ω - f curves of sample S1 and sample S2, where G_p is the parallel conductance and ω is the measured angular frequency.. 80

Figure 5.5. a- Quasi-static C-V data of sample S2 and S3 (symbols) are fitted well with corresponding simulated data (solids). The ideal C-V curve is also showed as well (dash line); b- “U-shape” Dit profiles of samples S2 and S3 extracted from simulation 81

Figure 6.1. a- Parameters of InGaAs compound and schematic of Al_2O_3/n-InGaAs MOSCAPs structures with the In content is 0.53, 0.7, and 1; b- Summary of process flow for MOSCAP fabrication 87

Figure 6.2. As 3d and In $3d_{5/2}$ XPS spectra of (a) native-oxide-corvered InAs surface and (b) 1.5 nm Al_2O_3/InGaAs, InAs structures, as deposition. After using surface treatment and oxide depositon, As-related oxides were reduced to under XPS detection level, the Ga-O and In-O bonds were also significant removed.. 88

Figure 6.3. High-resolution transmission electron microscopy micrographs of 13nm ALD Al_2O_3/InGaAs structures after PDA at 400^oC in forming gas, showing abrupt Al_2O_3/InGaAs, InAs interfaces 88

Figure 6.4. Capacitance voltage responses at measured frequency of 1 MHz of $Al_2O_3/In_xGa_{1-x}As$ MOSCAPs with different In content 89

Figure 6.5. Multi-frequency and bidirectional C-V responses of of $Al_2O_3/In_xGa_{1-x}As$ MOSCAPs with different In content 90

Figure 6.6. Multi-frequency C-V responses and conductance contours G_p/ω (f, V) at different temperatures (77 K, 180 K and 300 K) of $Al_2O_3/In_{0.53}Ga_{0.47}As$. Peaks of conductance shows the traces of Fermi level movement (solid lines) 91

Figure 6.7. Multi-frequency C-V responses and conductance contours Gp/ω (f, V) at different temperatures (77 K, 180 K and 300 K) of $Al_2O_3/In_{0.7}Ga_{0.3}As$, $Al_2O_3/InAs$ MOSCAPs. Conductance contours are closed due to the contribution of inversion layer and thus, the Fermi level traces could not show up 92

Figure 6.8. a- leakage current increases with increasing of In content in InGaAs. The Flower-Nordheim plot for b- $Al_2O_3/In_{0.53}Ga_{0.47}As$, c- $Al_2O_3/In_{0.7}Ga_{0.3}As$ and d-$Al_2O_3/InAs$ structures 93

LIST OF TABLES

Table 1.1. Band gap, bulk carrier mobility, and intrinsic carrier density of Si, Ge and III-V compounds 12

Table 2.1. Relationships between characteristics and advantages of ALD 29

LIST OF SYMBOLS

Symbol	Unit	Description
A	m^2	Area
C_{dep}	F/m^2	MOS capacitance in depletion
C_{it}	F/m^2	Interface trap capacitance
C_{ox}	F/m^2	Oxide capacitance
C_m	F/m^2	Measured capacitance
C_s	F/m^2	Semiconductor capacitance
D_{it}	$eV^{-1}m^{-2}$	Interface trap density, interface states density
ΔE	eV	Energy difference between a trap and a band
E_B	eV	Electron binding energy
E_C	eV	Conductance band minimum level
E_g	eV	Semiconductor bandgap
E_i	eV	Intrinsic energy level
E_F	eV	Fermi level
E_V	eV	Valence band maximum level
ε_0	F/m	Vacuum dielectric permittivity
ε_{SiO_2}	-	Relative dielectric permittivity (dielectric constant) of SiO_2
ε_k	-	Relative dielectric permittivity (dielectric constant) of high k materials
f	Hz	Frequency
G_p	S	Parallel conductance
G_m	S	Measured conductance
I_d	A, A/m	Drain current in a MOSFET
I_g	A	Gate current in a MOSCAP structure
k	J/K	Boltzmann’s constant
m_e	kg	Electron mass
m*	kg	Effective electron mass
n_i	m^{-3}	Intrinsic carrier concentration
N_A	m^{-3}	Density of acceptor dopant atoms
N_C	m^{-3}	Density of states in conductance band

Symbol	Unit	Description
N_D	m^{-3}	Density of donor dopant atoms
N_V	m^{-3}	Density of states in valence band
ω	Hz	Angular frequency
q	C	Elementary charge
Q_M	C	Metal charge in MOSCAP structure
Q_s	C	Semiconductor charge in MOSCAP structure
σ	m^2	Trap capture cross section
T	K, ^oC	Temperature
t_{ox}	m	Oxide thickness
τ_{it}	s	Interface trap time constant
V_F	V	Flat band voltage of MOSCAP
V_G	V	Gate voltage in a MOSCAP
v_{th}	m/s	Thermal velocity of a charge carrier
μ, μ_n, μ_p	m^2/V.s	Mobility, mobility of electrons and holes
χ	eV	Electron affinity

LIST OF ACRONYMS

Symbol	Description
ALD	Atomic Layer Deposition
ALE	Atomic Layer Epitaxy
ALCVD	Atomic Layer Chemical Vapor Deposition
CMOS	Complement Metal Oxide Semiconductor
C-V	Capacitance-Voltage
CET	Capacitance Equivalent Thickness
EOT	Equivalent Oxide Thickness
ESCA	Electron Spectroscopy for Chemical Analysis
HRTEM	High-resolution Transmission Electron Microscopy
G-V	Conductance-Voltage
I-V	Current-Voltage
MBE	Molecular Beam Epitaxy
MOS	Metal Oxide Semiconductor
MOSCAP	Metal Oxide Semiconductor Capacitor
MOSFET	Metal Oxide Semiconductor Transistor
PDA	Post Deposition Annealing
PMA	Post Metal Annealing
QSCV	Quasi-static Capacitance-Voltage
TMA	Trimethyl Aluminum
XPS	X-ray Photoelectron Spectroscopy

Chapter 1

INTRODUCTION

This chapter begins with describing briefly the evolution of semiconductor industry from its commencement to present. Downscaling the parameters of devices according to Moore's Law is the key feature to continue the development of complementary metal-oxide-semiconductor (CMOS) technology. High k metal gate is a revolutionary change in the CMOS technology up to now. The scaling challenges and future trends in CMOS research are also discussed in this chapter. The motivation, challenges and current progress of high k/III-V MOSFET-one of the possible solution for future CMOS technology, are presented. Finally, the last part of this chapter presents the problems statement of the study on Al_2O_3/InGaAs interface engineering and the organization of this dissertation.

1.1.An Overview of planar Si-based CMOS Technology

In November 2009, Intel announced that it would state production of microprocessors based on the newest 32 nm generation of logic technology [1]. This latest innovation in semiconductor industry demonstrates the progress of complementary metal-oxide-semiconductor (CMOS) technology from its commencement to present. The progress of semiconductor industry depends closely on the development of the metal-oxide-semiconductor field effect transistor (MOSFET), the key component in integrated circuits.

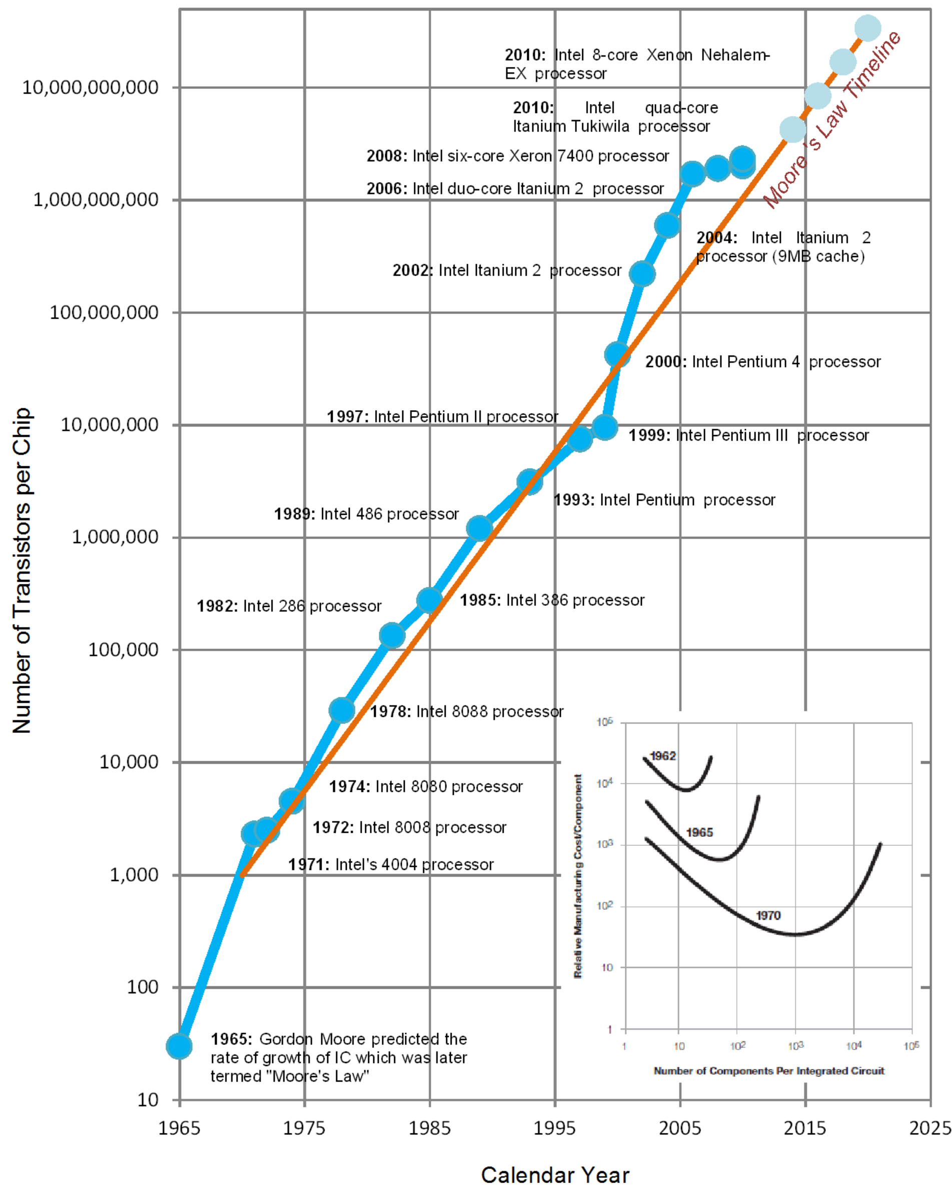


Figure 1.1. "The number of transistors incorporated in a chip will approximately double every 24 months": Moore's Law Timeline (solid) and the number of transistors per chip in Intel's products (line plus symbols). The inset is Moore's original prediction graph in 1965 [2].

Looking back to the past, the first transistor was invented by Brattain, Barden and Shockley in 1947 and the first integrated circuit was made independently of germanium by Jack Kilby in 1958 and of silicon by Robert Noyce in 1959. The first MOSFET on a silicon substrate was invented by Kahng and Atalla in 1960, 30 years after its principle was proposed by Lilienfield in 1930. Because SiO_2/Si interface has very good quality and stability which allows the fabrication of high performance MOSFET, CMOS technology has been based on the high quality SiO_2/Si interface.

In 1965 Electronics Magazine published a paper by Gordon Moore in which he predicted that the number of transistors incorporated in a chip will approximately double every 24 months [2]. This prediction is general known as Moore's Law (Moore's original prediction graph is shown in the inset of Fig. 1.1). Moore's Law has been guiding principle for the semiconductor industry for over 40 years [3], since Intel Corporation was co-founded by Gordon Moore and Robert Noyce in 1968. From that time, by downscaling device feature size, semiconductor industry has passed several generations and made a rapid pace of improvements in its products. Figure 1.1 shows the Moore's Law time line and the number of transistors per chip of Intel's products [2, 4]. The transistors per chip doubled after 2-years cadence has been preserved up to now. The number of transistors per chip was thousands in the early-1970s and has increased rapidly to billions recently.

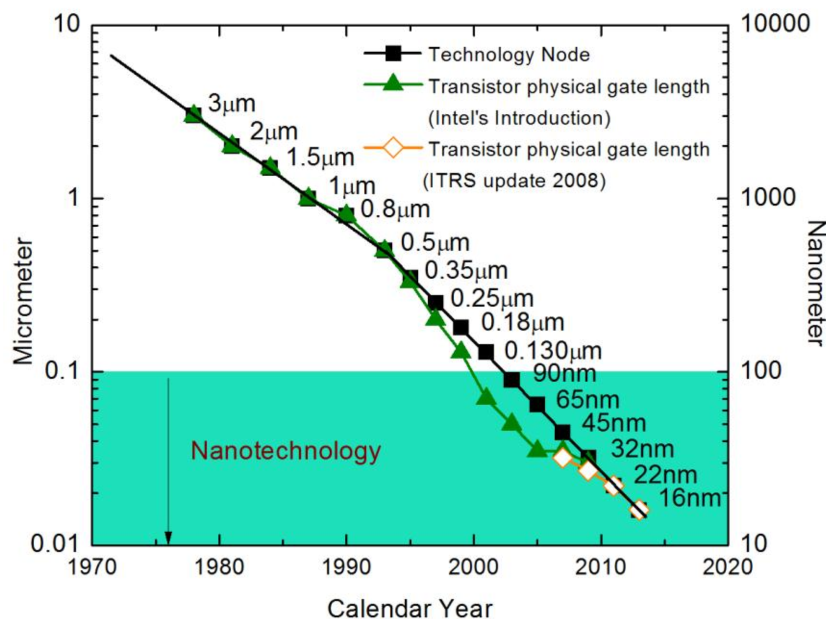


Figure 1.2. Scaling of logic technology node and correspond transistor's physical gate length (According to Intel's introduction until 2009 and ITRS update 2008)

Downscaling is the only effective way to increase the transistors density and to achieve high performance and low power consumption of logic CMOS operation. The MOSFET gate length and gate oxide thickness are the two critical parameters when shrinking its vertical and horizontal dimensions. To avoid short channel effect and maintain the electrostatic control of the channel when scaling gate length, the gate oxide thickness has to scale proportionally. As shown in Fig. 1.2, recently, the equivalent oxide thickness (EOT) and gate length have been reduced to 0.9 nm and 30 nm, respectively, in the 32 nm generation [1]. According to the International Technology Roadmap for Semiconductor 2008 (ITRS), the expected transistor's physical gate length for the next 22 nm generation is 20-22 nm in the end of 2011 and 16 nm for the following generation (Fig. 1.2).

Previously, the new generations of transistor technology had been developed simply by shrinking its vertical and horizontal dimensions. Since beginning of 2000s, the downscaling has not been so smooth any more. The 130 nm generation required the replacement of aluminum interconnects by cooper for lower resistance. The 90 nm generation used the strained silicon transistor for performance improvement. The 45nm generation introduced revolutionary high k dielectric and metal gate for improved performance and lower leakage current. The 32 nm generation requires a 2nd generation of high k metal gate transistors for future improvements in performance and power consumption. The introduction of high k metal gate technology is regarded as the biggest transistor advancement in 40 years by Intel's Co-Founder Gordon Moore.

1.2. High k, metal gate solutions

As mention above, reduction of gate oxide thickness always accompanies with the downscaling of CMOS technology. So far, we had no problem with the scaling thickness of SiO_2 or SiON as gate oxides and that had achieved MOSFET's devices with excellent performance. However, when the thickness of oxide reduces to smaller than 1.2 nm, the leakage problem becomes serious. At that thickness the leakage current becomes too high due to the direct tunneling of electrons through oxide (Fig. 1.3) [5, 6]. This high value of leakage current does not meet fully the requirement given by ITRS. Moreover, the reliability of the device is hampered by the time-dependent dielectric breakdown of ultra-thin oxide layer [7, 8], as well as by bias temperature instabilities [9].

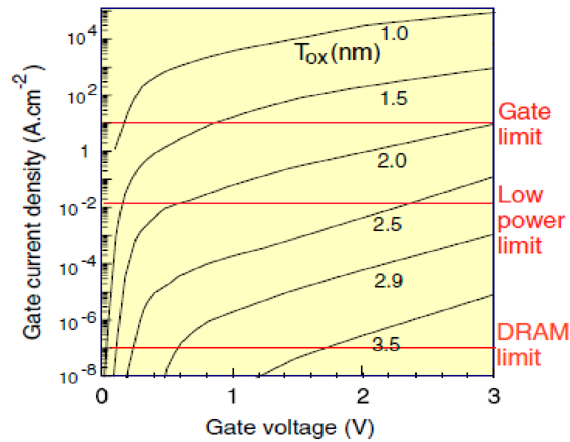


Figure 1.3. Leakage current versus voltage for various thickness of SiO_2 layers [5, 6]

A MOSFET is a capacitance-operated device, where the source-drain current depends on the gate capacitance:

$$C = \frac{\varepsilon_o \varepsilon_k A}{t} \tag{1.1}$$

where ε_o is the permittivity of free space, ε_k is the relative permittivity, A is the area and t is oxide thickness. Since the leakage current is much dependent on the oxide thickness, to maintain the high value of capacitance with thick gate oxide, the value of ε_k need to increase. That means the gate oxide of silicon device has to be replaced by other materials with higher ε_k value, called high k oxides. High k value, in other words, can be described as physical thick but electrically thin materials [10]. Fig 1.4 shows the direct tunneling problem can be solved by replacing SiO_2 (SiON) with a physically thicker layer of high k materials [5, 10].

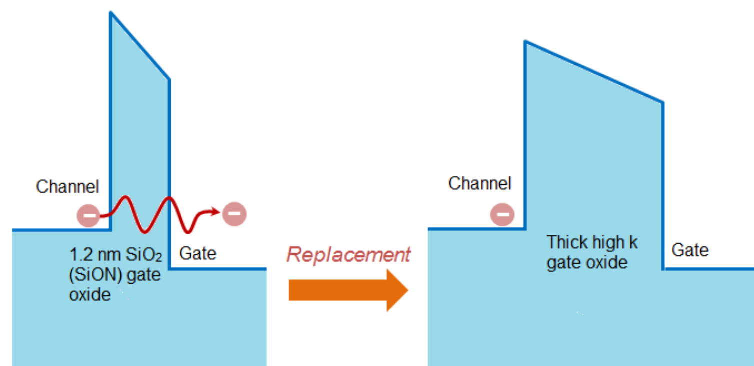


Figure 1.4. At the gate oxide thickness of 1.2 nm (5 layer of atoms), the wave describing the probable location of an electron is broader than the gate oxide and the electron can simply appear on the other side of gate oxide, meaning that direct tunneling of electrons through the insulation. New high k gate oxide is needed to plug the leak [10]

The concept of equivalent thickness oxide (EOT) is used to define an "electrical thickness" of new high k gate oxide [11]. The EOT refers to the thickness of any dielectric (t_k) scaled by the ratio of its dielectric constant (ε_k) to that of SiO_2 (ε_{SiO_2})

$$EOT = t_k \frac{\varepsilon_{SiO_2}}{\varepsilon_k} = t_k \frac{3.9}{\varepsilon_k} \tag{1.2}$$

The extraction of EOT requires to fit capacitance-voltage (C-V) characteristics of the MOS structure, taking into account quantum confinement effect in accumulation and inversion layer [12]. Besides, another useful quantity for comparison between gate dielectrics is the capacitance equivalent thickness (CET), which is defined as [12]:

$$CET(V) = \frac{\varepsilon_o \varepsilon_{SiO_2}}{C(V)} = \frac{3.9\varepsilon_o}{C(V)} \tag{1.3}$$

where C is the capacitance (per unit area) of MOS structure measured at a given gate bias. The extraction of CET does not require to fit C-V data, but depends on the chosen gate bias. CET can also be influenced by gate leakage in leaky devices [12].

The interest in high k dielectric research to replace SiO_2 started in the 1980s and renewed in the mid-1990s when the problem of leakage has become more serious. Figure 1.5 shows the parameters (dielectric constant versus band gap) of the candidate oxides [5, 13].

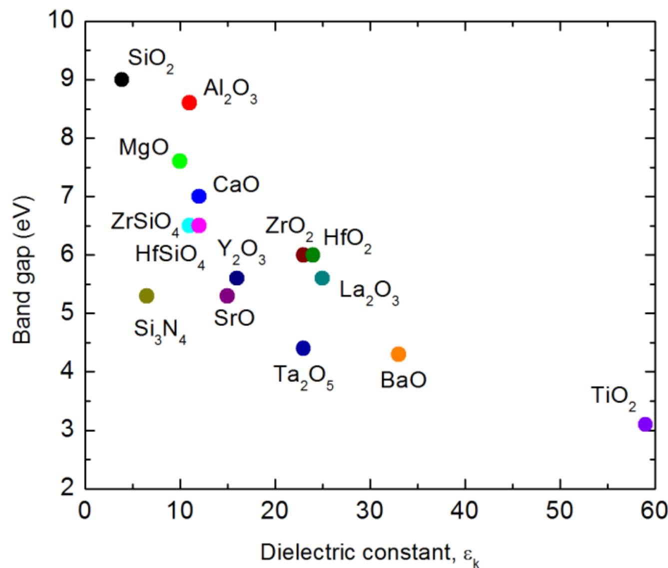


Figure 1.5. Static dielectric constant versus band gap for candidate gate oxides [5, 13]

In general, the relationship between dielectric constant and the band gap is reverse as shown in Fig. 1.5. Thus, the selected high k oxide has to be trade-off between dielectric

constant and band gap. Band gap must be large enough to have conductance band (CB) and valence band (VB) offsets with semiconductor over 1 eV to minimize the carriers' injection into its bands [5, 12]. In practice, the CB offset is smaller than VB offset, so that this limits the choice of oxide to those with band gaps over 5 eV [5, 12, 13]. The relative dielectric constant should be somewhere between 10 and 30. Besides, other important requirements for selecting high k also have to be considered, including: thermodynamic stability with Si (and also future channel materials), low interface charge traps (typically less than 10^{11} $eV^{-1}cm^{-2}$), low bulk electrically active defects, and kinetically stable and compatible to process at high temperature [5, 12].

In terms of band gap and ε_k values, many high k materials have been selected for study for gate oxide application including Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3, and various lanthanides as well as their silicates and aluminates [13-16]. After thorough research, HfO_2 and its silicate, $HfSiO_x$ have emerged as promising candidates because of their excellent thermal stability with Si. HfO_2 with a ε_k value between 16-20, energy band gap of about 5.4 eV, CB and VB offsets with Si of 1.5 eV and 3.4 eV respectively, has been used for the 45 nm and the recent 32 nm generations.

Transistors with high k gate dielectric were processed with pretty much identical to the existing transistor with SiO_2 (SiON) gate dielectric. However, it was found that, high k gate dielectric transistors had suffered a few problems including (1) it took more voltage to turn them on than it should have, and (2) once the transistor was on, the charge move sluggishly though them, slowing the device's switching speed [10]. The first problem is known as Fermi level pinning (FLP) at polysilicon gate and high k dielectric interface [10, 17]. The effective work function (EWF) of polysilicon could not be altered easily by doping when it was used with high k dielectric. It was found that the EWF of polysilicon/HfO_2 stack is determined by Si-Hf bonds instead of Fermi level of polysilicon gate [17]. The EWF of polysilicon in that case was fixed at certain point near the Si conductance band edge, resulting in very high threshold voltage V_{th} in PMOS devices. The second problem is known as low charge-carrier mobility or the channel mobility degradation when using high k gate dielectrics [18, 19]. Essentially, high k materials are made up of dipoles and having a large polarization. This large polarization leads to strong vibrations in a semiconductor's crystal lattice (phonons), resulting in the increase of electron-scattering (Fig. 1.6.a) and thus, reducing their mobility [20]. Research by M. V. Fischetti et al. also showed that the metal gate with high electron density can screen out

the effect of phonons on channel electrons (Fig. 1.6.c) [10, 20]. Experimental data by R. Chau et al. shows clearly effect of phonon-electron scattering by using high k/polySi gate stack (Fig. 1.6.b) and the electron mobility can be improved by using high k/metal gate stack (Fig. 1.6.d) [21]. Besides, the bond between the high k dielectric and the metal gate would be so much better than that between high k and polySi. Thus, the use of gate metal with sufficient value of work function can eliminate the FLP problem of polysilicon gate and allow moderating the threshold voltage of devices. By using gate metal, it is also possible to achieve lower CET value at inversion regime, lower gate resistance, and eliminate the boron penetration into the dielectric and transistor channel as suffering in case of polySi gate.

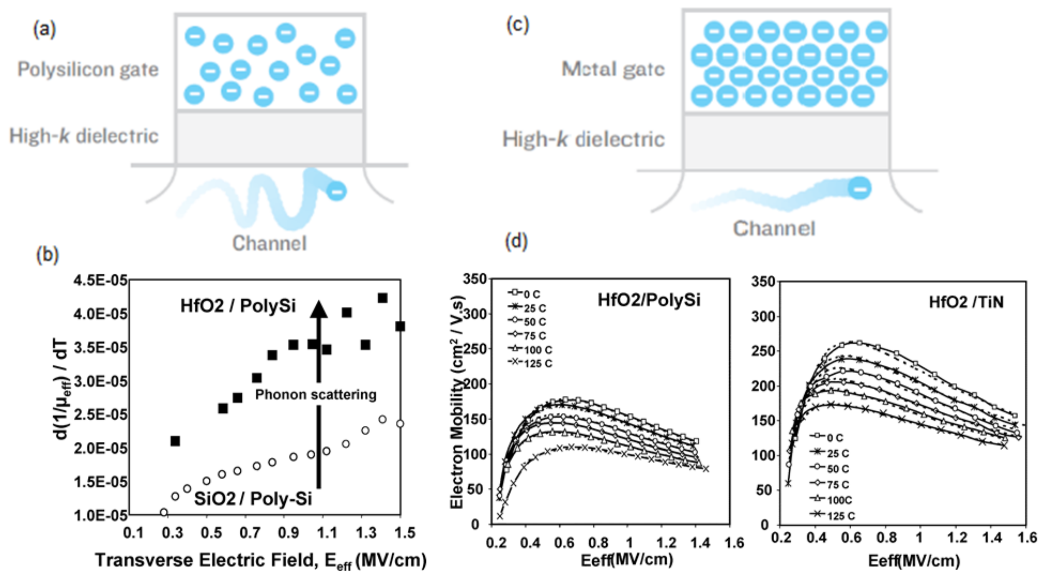


Figure 1.6. a-Electron density in PolySi gate is not large enough to screen the effect of high k dipoles on semiconductor lattice points, lead to strong phonon-electron scattering; b-Experimental evidence of phonon scattering in the high k dielectric. The net value of the temperature (T) sensitivity factor, $d(1/\mu_{eff})/dT$, is negative when coulombic scattering dominates and positive when phonon scattering dominates. [21]; c-Metal gate with high electron density can screen out the vibrations, reduce effect of phonon scattering; d-Experimental (symbols) and simulation (dash lines) data show the improvement of electron mobility by using high k/metal gate stack [21].

So far, we have discussed about the replacement of high k dielectric for SiO_2 (SiON) to solve leakage problem. Then, the problems suffering from high k/ Si channel and high k/polySi contact have been also discussed and gate metal replaces for polySi is a solution for these problems. For conclusions, let us take a look to see how good the improvements of devices are for the generations of high k metal gate MOSFETs (Fig. 1.7) [22-24].

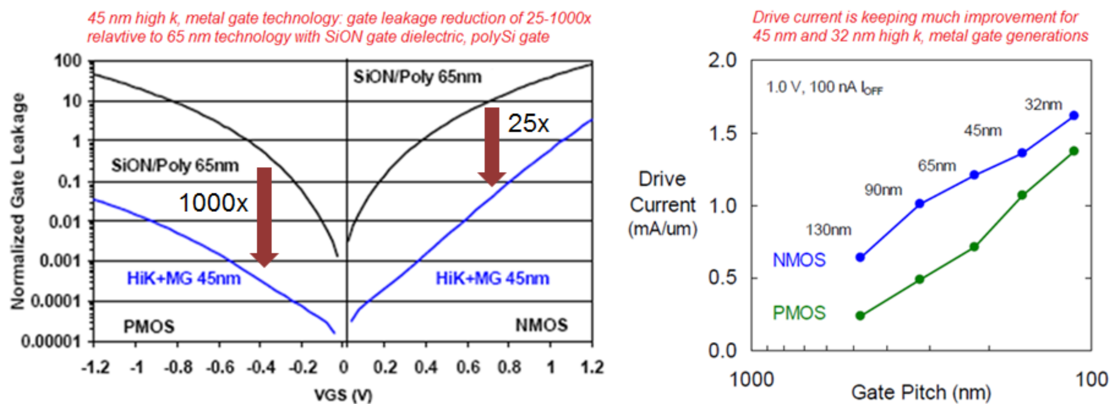


Figure 1.7. The improvements of leakage current and drive currents by using high k metal gate generations [22-24]

1.3. Scaling challenges and future trends

1.3.1. Scaling challengers

Beyond the 32 nm generation, the CMOS technology faces a number of scaling challenges which need to be addressed. Off-state current, I_{off} increases from the degraded drain-induces barrier lowering (DIBL) and subthreshold slope (SS). These degradations cause by short channel effect (SCE) which leads to limitation for the effective gate length, l_{eff} shorter than 15 nm [25]. The decrease of gate oxide thickness for better channel control accompanies with a penalty of increased leakage current and increased channel doping concentration. The increase of channel doping concentration results in the decrease of carrier mobility (due to impurity scattering) and the increase of random dopant fluctuations which leads to degrading the minimum operating voltage. Decreasing gate pitch increases the parasitic capacitance contribution for both contact to gate and epi to gate thus increase overall gate capacitance. Decreasing source/drain opening size results in increasing drain resistance, thus decreasing drive current [22, 25].

The power consumption is also the limiting factor of the logic MOS [26]. As downsizing the device's features, the switching energy of MOSFETs decrease but the power density increases (see Fig. 1.8) and thus, cause of system power consumption [27]. One of effective way to decrease the dynamic power consumption is lowering supply voltage. However, in order to reduce supply voltage, the threshold voltage has to be reduced. This results in the significant increase of off- state current due to the increase of the subthreshold leakage current with low threshold voltage (Fig. 1.8, right) [26].

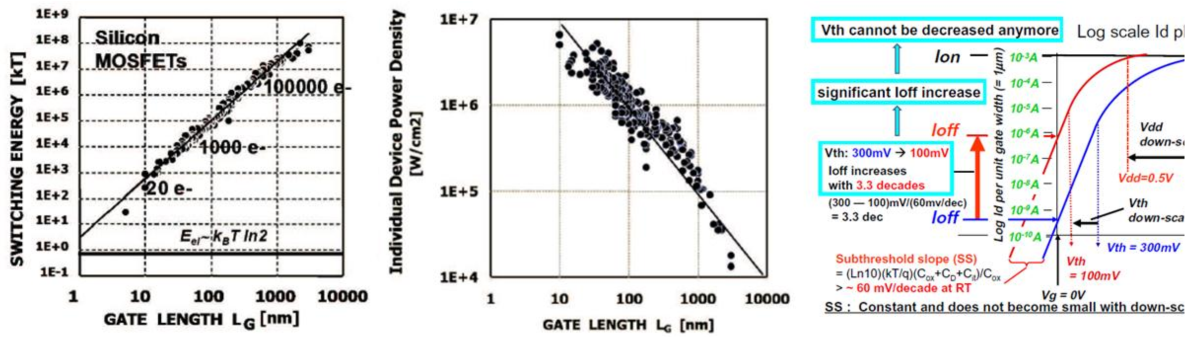


Figure 1.8. Illustration of the exponential decrease in switching energy (left) and the simultaneously increasing device power density (middle) as a consequence of device downscaling [27]. The increase of power density causes of power consumption issue, lowering supply voltage is not an easy way to reduce power consumption due to the increase of off state current, I_{off} (right) [26].

1.3.2. Future trends

For future CMOS technology, the interests have been focused on both structures and materials. In term of structures, the transition from present planar structure to non-planar structure such as multiple gate or multiple channel FET (MuGFETs or MuCFETs) has been proposed to deal with SCE degradation. These devices include double gate FET (DGFETs), tri gate FET, surround gate FET, and Si nanowire (Fig. 1.9) [3, 22, 26, 28]. A significant improvement of SCE and short-channel characteristics with high drive current performance has been demonstrated in tri gate transistors. These results demonstrate that the benefits of all different silicon innovations can be combined to extend and continue the CMOS scaling and performance trends [28]. The non-planar Si CMOS technology is expected to apply for 22 nm node and may be for 16 nm node generations. Beyond 16 nm, silicon will suffer its fundamental limits and will no longer provide the performance improvement of devices for downscaling.

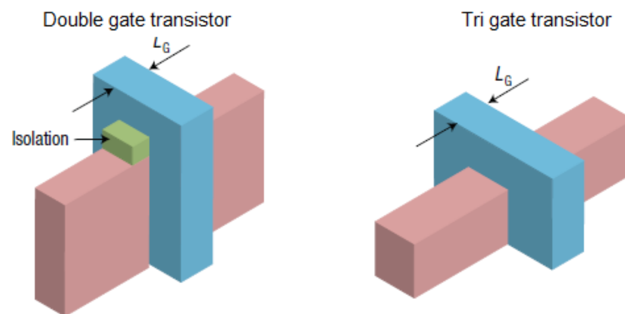


Figure 1.9. Non-planar transistors: Double-gate transistor (left) and tri-gate transistor (right) [28]

In term of materials, much interest has been generated and good progress has been made in the research of non-silicon electronic materials for future logic applications, and their integration onto the silicon platform. The most studied materials are Ge, III-V compound semiconductors such as GaAs, InGaAs, InAs, and InSb, semiconductor nano wire, carbon nanotubes (CNTs), and graphene. In general, these materials have significantly higher intrinsic carriers (electron or hole) mobility than Si, and they have potential for enabling the future high-speed applications at very low power-supply voltages. Among these materials, Ge and III-V compounds are the most mature and practical because they can be integrated into a Si CMOS front-end process more easily than the other alternatives. Moreover, the knowledge about III-V compounds is much more than others because they have been used in communication and optoelectronic products for a long time. The ITRS's 2009 version predicted that III-V/Ge will replace Si as channel materials in 16 nm node CMOS technology and beyond. The advantages of III-V's properties against Si as channel material will be discussed in the next part.

1.4. III-V compound semiconductors for CMOS technology: motivation, challenges and current progress

1.4.1. Motivation

The key advantage of III-V compound semiconductors as compared to Si is their high electron mobility and high low-field saturation velocity. The electron mobility enhancement in III-V compounds comes from their lower electron effective mass than that of Si. Figure 1.10 and table 1.1 show electron drift velocities versus electric field and the parameters (carrier mobility, band gap, intrinsic density) of Si, Ge and III-V compounds.

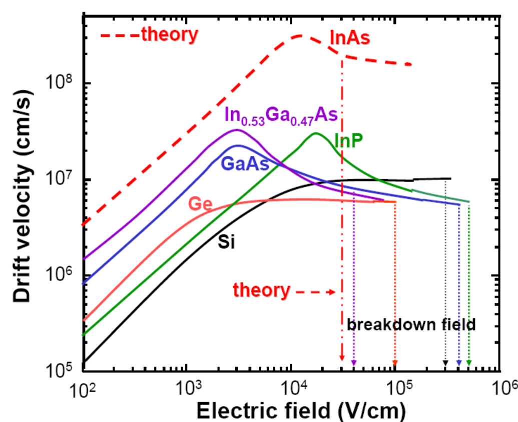


Figure. 1.10. Electron velocities as a function of field of Si, Ge and III-V compound semiconductors. III-V compound semiconductors exhibit high saturation velocity at low electric field

Table. 1.1. Band gap, bulk carrier mobility, and intrinsic carrier density of Si, Ge and III-V compounds (data from reference [29])

	Si	**Ge**	**GaAs**	**$In_{0.53}Ga_{0.47}As$**	**$In_{0.7}Ga_{0.3}As$**	**InAs**	**InSb**
Band gap, E_g (eV)	1.12	0.66	1.424	0.74	0.588	0.354	0.17
Bulk e mobility cm^2/V s	1400	3900	8500	12000	20000	40000	77000
Bulk hole mobility cm^2/V s	450	1900	400	300	300÷400	500	850
Intrinsic concentration cm^{-3}	10^{10}	2×10^{13}	2.1×10^{6}	6.3×10^{11}	10^{13}	10^{15}	2×10^{16}
Conduction band DOS cm^{-3}	3.2×10^{19}	1.0×10^{19}	4.7×10^{17}	2.1×10^{17}	-	8.7×10^{16}	4.2×10^{16}

In very short channel length MOSFETs, the carriers exhibit quasi-ballistic transport. In this case the drive current is not depended on saturation velocity but is determined by carrier injection from the source to drain, i.e. injection velocity, v_{inj} [30]. The carrier injection relates directly to the carrier mobility at low field and thus, the concept of mobility continues to have relevance to ultra-short channel MOSFETs [30]. The use of III-V materials as an alternative channel for Si is due to their advantages in two major requirements for high-performance logic devices: increased speed and reduced power consumption while the integration density keeps increasing [31].

In term of device's speed, the intrinsic delay time τ_i can be approximated as:

$$\tau_i \approx \frac{Q}{I_{Dsat}} \approx C_G \frac{V_D}{I_{Dsat}} \quad (1.4)$$

which assumes switching the channel charge Q on the gate capacitance C_G by a constant "ON" drain current I_{Dsat} between two logic states with a voltage swing across the channel equal to power supply voltage. The current is measured in saturation with equal gate and drain voltage, $V_{GS}=V_{DS}=V_D$. For channel materials comparison, it is good enough to approximate the intrinsic delay time as:

$$\tau_i \approx \frac{L_G}{v_{inj}} \quad (1.5)$$

The extrinsic delay time τ_{ext} can be estimate as:

$$\tau_{ext} \approx C_{ext} \frac{V_D}{I_{Dsat}} \quad (1.6)$$

where C_{ext} is total capacitance including gate capacitance C_G and interconnect parasitic capacitance. Because III-V compound have low effective mass and high electron mobility, the injection velocity in these materials is much higher than that of silicon, as shown in Fig. 1.10 and table 1.1 (injection velocity was measured ~ 2.5-3 × 10^7 cm/s in InGaAs and InAs, at least two time higher than strain n-Si MOSFETs [32, 33]). According to equations (1.4), (1.5) and (1.6), this high injection velocity explains why III-V MOSFETs are expected to get higher switching speed, higher drive current than Si MOSFETs.

In term of power, MOSFETs have mostly capacitive input impedance and a certain energy is require to recharge the gate capacitance [31]. The charging energy depends on distribution of carrier in the channel and capacitance change below threshold. Therefore, it is assumed that the dynamic energy is proportional to $C_g V_D^2$ per bit and it combines with intrinsic delay time τ_i to become intrinsic energy-delay product (EDP_i):

$$EDP_i = \frac{C_G V_D^2 \tau_i}{W} \qquad (1.7)$$

where W is the channel width. Related to materials properties, the switching energy is proportional to Q^2/C_g or just $\propto n^2$ (n is the electron concentration in the channel, proportional to electron effective mass m^*) for intrinsic power, if only the channel materials-related are considered and $C_{ext} V_D^2$ if large extrinsic capacitance is charging. Then the intrinsic and extrinsic energy-delay products can be expressed through the materials-related parameters:

$$EDP_i \propto \frac{n^2}{v_{inj}} \propto m^{*\frac{5}{2}} \text{ and } EDP_{ext} \propto \frac{V_D^3}{n v_{inj}} \propto \frac{V_D^3}{\sqrt{m^*}} \qquad (1.8)$$

From here, it is clear to see that the III-V channel is considerably more favorable than Si in reducing energy-delay products even in the architectures with large parasitic. This because in the ballistic regime (ultra-short channel) with large parasitic, EDP improvement results from the ability to get high drain current at low voltage overdrive V_D-V_T where V_T is threshold voltage. Due to high low field electron mobility in III-V compounds, the supply voltage V_D can be reduced while the value of V_T can keep relative high to maintain low threshold leakage current i.e., low static power [31].

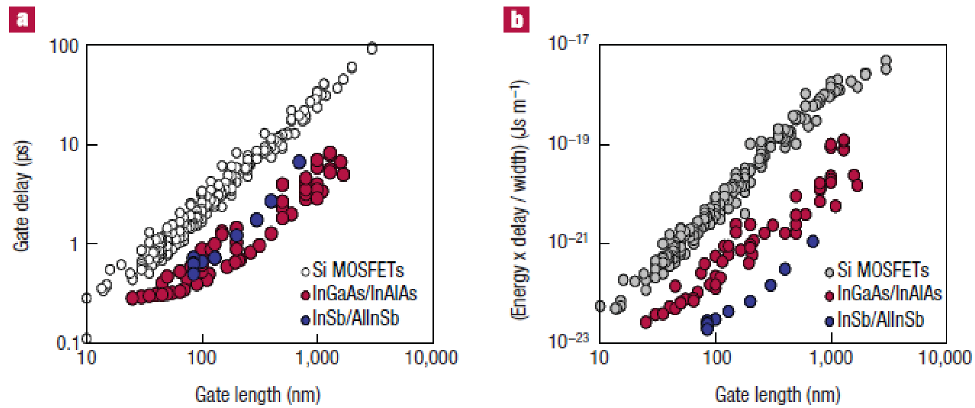


Figure. 1.11. III–V HEMTs characteristics compared with standard silicon MOSFETs a, Intrinsic gate delay. b, Normalized energy-delay product of n-channel InSb and InGaAs HEMTs [28, 34]

For highlight the advantages of III-V compounds in speed and power improvements, recent work on InGaAs, InSb n-channels high electron mobility transistors (HEMTs) have demonstrated the significantly reduction of gate intrinsic delay as well as EDPs as compared to standard Si MOSFETs (Fig. 1.11) [28, 34]. Both n- and p- channel InSb HEMTs have been demonstrated very high speed at a low supply voltage of only 0.5 V [35, 36]. Compared with state-of-the-art silicon transistors, these n-channel III–V transistors show either a 1.5-fold improvement in intrinsic speed performance at the same power, or 10-fold reduction in power for the same speed performance [35]. The p-channel HEMTs also show either a 2-fold improvement in intrinsic speed performance at the same power, or 10-fold reduction in power for the same speed performance as compared to p-channel Si MOSFETs [36].

Another advantage of III-V materials is the band structure. InGaAs, InAs compounds have large band off-set with the barrier and large separation between high electron-effective-mass L- and X-valleys and low electron-effective-mass Γ-valley. This allows to get high number of electrons in the Γ-valley and consequently get high drive current [31].

1.4.2. Challenges

Although III-V based MOSFETs give a significantly advantages for future CMOS technology, there are some challenges which need to be addressed. Although band structure have large separation between valleys, III-V materials have low density of state (DOS) in the low effective-mass Γ-valley (Tab. 1.1) [29]. This low DOS tends to reduce inversion charge (Q_{inv}) and hence reduce drive current. The small direct band gap of III-V

MOSFETs inherently gives rise to very large band to band tunneling (BTBT) leakage current as compared to Si. They also have a high permittivity and hence are more prone to short channel effect (SCE). Non-planar technique may also need to be applied to III-V MOSFETs to improve the electrostatics with scaling [28].

The integration of high k on III-V for future MOSFETs is an indispensable progress for research since high k/ Si MOSFETs had been introduced for 45 nm and 32 nm generations. Even the current researches on III-V HEMTs have been shown very significant merits for future transistors [28, 34-36], the leakage is still a serious problem and the architecture of MOSHEMTs with the introduction of high-k materials on top of channel seems to be a good solution. It was recognized that at III-V surfaces, Fermi level is always pinned at a fixed position, called surface Fermi level pinning (FLP) [37]. It has been then realized the FLP problem has related to the poor native oxides at III-V's interfaces [38]. For instance, GaAs native oxide consists of As- and Ga-related oxides (As_2O_3, As_2O_5, Ga_2O_3, Ga_2O_5, Ga_2O, etc). These poor native oxides lead to very high interface traps density which consequently pins Fermi level at a fixed position. When introducing high k on III-V, the FLP at high k/ III-V interface has imposed a key challenge to the development of surface-channel inversion-model III-V MOSFETs. For more than four decades, to solve FLP issue, research efforts have been focused on the surface treatments i.e. reducing/eliminating and passivation the re-oxidation of III-V's native oxides before/during the high k deposition. Although some significant results have been achieved, the understanding of interface problems is still limited and FLP issue is still a hot topic for researchers working on III-V MOSFETs.

1.4.3. Current progress

Since FLP issue is a key challenge to the development of high k/ III-V MOSFETs, various in-situ and ex-situ passivation methods have been developed in order to improve high k/ III-V interface and let the free-movement of Fermi level. The first in-situ approach is the deposition of the gate dielectric on freshly grown III-V's surfaces (GaAs, InGaAs). For instance, in a multi-chamber molecular beam epitaxy (MBE) system, III-V epi-layers are transformed from III-V chamber to oxide chamber without exposed to air [39-41]. The in-situ process with ultra-high vacuum (UHV) e-beam deposition of Ga_2O_3/Gd_2O_3 (GGO) gate dielectric has shown remarkable improvement of GGO/GaAs interface with low interface density, smaller than 10^{11} $eV^{-1}cm^{-2}$ [39, 40]. The use of this

process for 1μm gate length InGaAs MOSFETs devices have achieved outstanding performance with maximum drain current of 1.05 A/mm, transconductance of 714 mS/mm, and a peak mobility of 1300 cm^2/V.s [42]. In-situ gases treatment is another interesting approach [43-45]. Period to gate dielectric deposition, III-V's surfaces are treated by gases (such as H_2, N_2, NH_3, H_2S, etc), using thermal or plasma processes. Although some significant results were achieved [43], the use of this method is still limited. This may be due to the effect of the surface damage during plasma process.

The ex-situ processes widely used for research due to it is simpler than in-situ process. Moreover, from manufacturing perspective, an ex-situ process flow has its incentive. There are many ex-situ approaches have been demonstrated for research but they can be divided into two groups: using chemical solutions and using interfacial passivation layers (IPLs). For the first approach, chemical solution such as HCl, HF, NH_4OH, $(NH_4)_2S$, HBr, etc., have been used before the deposition of gate dielectric [46-48]. By using chemical solutions, III-V native oxides could be eliminated. Moreover, the use of sulfide treatment can prevent the re-oxidation of native oxides at surface. By using this method, the improvement of high k/III-V interface with the unpinning of Fermi level has been clearly demonstrated. High performance inversion-mode InGaAs MOSFETs based on this surface treatment method have been demonstrated with high drain current of 1.1 A/mm and extrinsic transconductance of 1.1 S/mm [48, 49]. Interfacial passivation layers (IPL) is another interesting approach. This method has been developed by using very thin layers of Si, Si/Ge, Ge, SiN, AlN, etc., [50-58] between gate dielectric and III-V channels. The use of IPLs has shown the improvement of interface quality and gave a promising device performance. However, the contribution to increasing EOT may limit the use of IPLs for future MOSFETs.

Atomic layer deposition (ALD) has been a mainstream method for high k deposition. This is an ex-situ, robust, and manufacturable process, which attracts wider interests in academia and industry. Besides good oxide quality, well thickness control, the ALD is also known with a "self-cleaning" effect of precursors and provide a high quality of high k/III-V interfaces [59]. Up to now, all high performance inversion-mode high k/III-V MOSFETs devices were based on or related to this high k deposition method [42, 48, 49]. The ALD method, which had been used in manufacturing for 45 nm and 32 nm high k/ Si generations, is believed to be a mainstream technique for future high k/III-V MOSFETs.

After a long time research, considerable progress have been made in MOSFETs performance. However, there are still many problems need to be overcome. For instance, the smallest gate length of the working devices is still limited at above 100 nm; the I_{on}/I_{off} ratio, subthreshold slope (SS), and drain-induced barrier lowering (DIBL) values are still high when scaling down gate length into deep submicron [60]. In future, like Si, non-planar technique needs to be applied for III-V MOSFETs. Besides, efforts must be continued to improve high k/III-V interface quality, source/drain junction engineering, etc.

Besides the study on MOSFETs, III-V HEMTs device is the other promising and interesting approach for the future devices. These devices with two dimensional electron gas (2DEG) transport on an almost perfect channel allow to get a very high performance. In fact, the p- and n- short channel high In-content InGaAs, InAs, InSb HEMTs have shown very high drain current at very low supply voltage (as low as 0.5 V) [35, 36, 61, 62]. Based on these significant results, efforts are continuing in order to realize the performance of HEMTs (MOSHEMTs) for future high speed, low power digital application.

1.5. Problem statement and objective of the dissertation

This work focuses on study the effect of surface treatments, gas annealing conditions on the interface properties of $Al_2O_3/In_xGa_{1-x}As$ (x= 0.53, and 0.7), InAs structures. Since the effective of $(NH_4)_2S$ and HCl surface treatments have been compared in high k/GaAs, the discussion of these surface treatments on high k/InGaAs (with In content higher than 0.5) and high k/InAs is not investigated in details. The "self-cleaning" effect by ALD precursor such as trimethyl aluminum (TMA) has been studied on GaAs, InGaAs but the extension for studying on InAs has not been studied yet, especially on the electrical characteristics. Besides the surface treatments, gas annealing condition is the other important process to improve the interface as well as oxide qualities. From these points of view, the following objectives are addressed in this work:

- Studying the "self-cleaning" effect of TMA on InAs surface and comparing the effective of $(NH_4)_2S$ and HCl chemical surface treatments in combination with TMA pretreatment on the Al_2O_3/InGaAs, InAs interface properties.
- Systematic investigation the effect of N_2, H_2 annealing conditions on electrical properties of Al_2O_3/n-InGaAs. Developing a simple method to get low Al_2O_3/n-InGaAs interface density.

- Comparing the electrical properties of Al_2O_3/n-$In_xGa_{1-x}As$ (x = 0.53, and 0.7) and n-InAs MOS structures.

1.6. Organization of the dissertation

The dissertation is organized in 7 chapters, including the introduction, MOSCAPs fabrication process and characterization methods, and a main achievements and discussions according to the objectives of this work.

Chapter 2. The MOSCAPs fabrications process and characterization methods will be presented in this chapter. X-ray photoelectron spectroscopy (XPS), and high resolution transmission electron microscopy (HRTEM) are used for analyzing the high k/InGaAs, InAs interfaces. Capacitance-voltage (C-V), conductance-voltage (G-V), and current-voltage (I-V) characteristics were used for the electrical characterization. Conductance and conductance map methods, used to extract interface state and study the movement of Fermi level, are also presented in this chapter.

Chapter 3. Self-cleaning effect on the reduction of InAs' native oxides by using TMA precursor is dicussed. The combination of ex-situ chemical solutions (including $(NH_4)_2S$ and HCl) surface treatments and in-situ TMA pretreatment on Al_2O_3/n-InAs MOSCAP structure are also studied.

Chapter 4. Based on the study in chapter 3, this chapter continues to improve the interface quality of Al_2O_3/n-InAs by optimizing ALD process. This study confirms the advantages of the HCl plus TMA treatment as compared to sulfide plus TMA treatment in the improvement Al_2O_3/InAs interface. Especially, by using simulation, the interface density profile is first time presented for Al_2O_3/InAs structure.

Chapter 5. This chapter investigates the influences of surface treatments and gas annealing conditions on the inversion behaviors of the ALD Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs. Simple method to get low Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ interface density has developed: using sulfide plus TMA treatment and annealing in H_2 gas.

Chapter 6. A comparison of Al_2O_3/n-$In_xGa_{1-x}As$ (x = 0.53, and 0.7) and n-InAs MOSCAPs is presented in this chapter. The comparison bases on the properties of InGaAs and InAs themselves.

Chapter 7. General conclusions

References

[1] Intel white paper, "Introducion to Intel's 32nm process technology," source: http://download.intel.com/pressroom/kits/32nm/westmere/Intel_32nm_overview.pdf

[2] G. E. Moore, "Cramming more components onto integrated circuits," Electronics **38** (1965).

[3] Robert Chau, Mark Doczy, Brian Doyle, Suman Datta, Gilbert Dewey, Jack Kavalieros, Ben Jin, Matthew Metz, Amlan Majumdar, and Marko Radosavljević, "Advanced CMOS transistors in the nanotechnology era for high-performance, low-power logic applications," in ICSICT 2004, 26-30 (2004) .

[4] Source: http://www.intel.com/technology/mooreslaw/ and http://en.wikipedia.org/wiki/Transistor_count.

[5] R. Jobertson, "High dielectric constant gate oxides for metal oxide Si transistors," Rep. Prog. Phys. **69**, 327-396 (2006).

[6] S. H. Lo, *et al.*, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," IEEE Electron Device Lett. **18**, 209-211 (1997).

[7] R. Degraeve, N. Pangon, B. Kaczer, T. Nigam, G. Groeseneken, and A. Naem, "Temperature acceleration of oxide breakdown and its impact on ultra-thin gate oxide reliability," in VLSI Sym.Tech.Dig., 59-60 (1999).

[8] J. H. Stathis and D. J. DiMaria, "Reliability projection for ultra-thin oxides at low voltage," in IEDM '98 Tech. Dig., 167-170 (1998).

[9] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," J. Appl. Phys. **94**, 1-18 (2003).

[10] M. Bohr, R. Chau, T. Ghani, and K. Mistry, "The high k solution," IEEE spectrum, 29-35 (2007).

[11] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-kappa gate dielectrics: Current status and materials properties considerations," J. Appl. Phys. **89**, 5243-5275 (2001).

[12] M. Houssa, L. Pantisano, L.-A° . Ragnarsson, R. Degraeve,T. Schram, G. Pourtois, S. De Gendt, G. Groeseneken, and M.M. Heyns, "Electrical properties of high-[kappa] gate dielectrics: Challenges, current issues, and possible solutions," Mat. Sci. and Eng.: R: Reports **51**, 37-85 (2006).

[13] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," J. Vac. Sci. Technol. B **18**, 1785-1791 (2000).

[14] L. Manchanda, W. H. Lee, J. E. Bower, F. H. Baumann, W. L. BroIwn, C. J. Case, R. C. Keller, Y. 0. Kim, E. J. Laskowski, M. D. Morris, R. L. Opila, P. J. Silverman, T. W. Sorsch and G. R. Weber, "Gate quality doped high K films for CMOS beyond 100 nm: 3-10

nm Al_2O_3 with low leakage and low interface states," in IEDM '98 Tech. Dig., 605-608 (1998).

[15] G. D. Wilk and R. M. Wallace, "Stable zirconium silicate gate dielectrics deposited directly on silicon," Appl. Phys. Lett. **76**, 112-114 (2000).

[16] W'en-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, Katsunori Onishi, Tat Ngai, Sanjay Banerjee, and Jack C. Lee, "MOSCAP and MOSFET characteristics using ZrO_2 gate dielectric deposited directly on Si," in IEDM '99 Tech. Dig., 145-148 (1999).

[17] Christopher C. Hobbs, Leonardo R. C. Fonseca, Andrey Knizhnik, Veeraraghavan Dhandapani, Srikanth B. Samavedam, William J. Taylor, John M. Grant, LuRae G. Dip, Dina H. Triyoso, Rama I. Hegde, David C. Gilmer, Ricardo Garcia, Darrell Roan, M. Luke Lovejoy, Raghaw S. Rai, Elizabeth A. Hebert, Hsing-Huang Tseng, Steven G. H. Anderson, Bruce E. White, and Philip J. Tobin, "Fermi-level pinning at the polysilicon/metal oxide interface-Part I," IEEE Trans. Electron Devices **51**, 971-977 (2004).

[18] E.P. Gusev, D.A. Buchanan, E. Cartier, A. Kurnar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P.C. Jamison, D.A. Neumayer, M. Copel, M.A. Gribelyuk, H. Okom-Schmidt, C. D'Emic, P.Kozlowski, K. Chan, N. Bojarczuk, L-A. Ragnarsson, P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin high-K gate stacks for advanced CMOS devices," in IEDM'01 Tech. Dig., 20.1.1-20.1.4 (2001).

[19] Jack C. Lee, H. J. Cho, C. S. Kang, S. Rhee, Y. H. Kim, R. Choi, C. Y. Kang, C. Choi, and M. Abkar, "High-k dielectrics and MOSFET characteristics," in IEDM '03 Tech. Dig., 4.4.1-4.4.4 (2003).

[20] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal--oxide--semiconductor systems with a high-kappa insulator: The role of remote phonon scattering," J. Appl. Phys. **90**, 4587-4608 (2001).

[21] Robert Chau, Suman Datta, Mark Doczy, Brian Doyle, Jack Kavalieros, and Matthew Metz, "High-k/metal-gate stack and its MOSFET characteristics," IEEE Electron Device Lett. **25**, 408-410 (2004).

[22] S. Tyagi, C. Auth, I. Ban, P. Chang, R. Chau, T. Ghani, C-H. Jan, J. Kavalieros, K. Kuhn, J. Maiz, K. Mistry, and I. Post, "Future device scaling - Beyond traditional CMOS," in IEDST '09 Workshop, 1-4 (2009).

[23] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks , R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas,

T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," in IEDM' 07 Tech. Dig., 247-250 (2007).

[24] S. Natarajan, M. Armstrong, M. Bost, R. Brain, M. Brazier, C-H Chang, V. Chikarmane, M. Childs, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, I. Jin, C. Kenyon, S. Klopcic, S-H. Lee, M. Liu, S. Lodha, B. McFadden, A. Murthy, L. Neiberg, J. Neirynck, P. Packan, S. Pae, C. Parker, C. Pelto, L. Pipes, J. Sebastian, J. Seiple, B. Sell, S. Sivakumar, B. Song, K. Tone, T. Troeger, C. Weber, M. Yang, A. Yeoh, and K. Zhang, "A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171 μm^2 SRAM Cell Size in a 291Mb Array," in IEDM' 08 Tech. Dig., 1-3 (2008).

[25] K. J. Kuhn, "Moore's Law Past 32nm: Future Challenges in Device Scaling," in IWCE '09 Workshop, 1-6 (2009).

[26] H. Iwai, "Roadmap for 22 nm and beyond (Invited Paper)," Microelectron. Eng. **86**, 1520-1528, (2009).

[27] K. Martens, "Electrical Charaterization and Modeling of Ge/III-V - Dielectric Interfaces," PhD Dissertation, IMEC, Belgium, 2009.

[28] R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, "Integrated nanoelectronics for the future," Nat. Mater. **6**, 810-812 (2007).

[29] Source: http://www.ioffe.ru/SVA/NSM/

[30] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," IEEE Electron Device Lett. **18**, 361-363 (1997).

[31] Serge Oktyabrsky, and Peide D. Ye, *Editors* "Fundamentals of III-V Semiconductor MOSFETs," Spring, ISBN 978-1-4419-1546-7, 199-204 (2010).

[32] G. Dewey, M. K. Hudait, K. Lee, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, and R. Chau, "Carrier Transport in High-Mobility III-V Quantum-Well Transistors and Performance Impact for High-Speed Low-Power Logic Applications," IEEE Electron Device Lett. **29**, 1094-1097 (2008).

[33] G. Dewey, R. Kotlyar, R. Pillarisetty, M. Radosavljevic, T. Rakshit, H. Then, and R. Chau, "Logic Performance Evaluation and Transport Physics of Schottky-Gate III-V Compound Semiconductor Quantum Well Field Effect Transistors for Power Supply Voltages (V_{CC}) Ranging from 0.5V to 1.0V," in IEDM' 09 Tech. Dig. 1-4 (2009).

[34] R. Chau, S. Datta, and A. Majumdar, "Opportunities and Challenges of III-V Nanoelectronic for High-speed, Low-power Logic Applications," in IEEE CSICS Challen. Tech. Dig., 17 (2005).

[35] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, "85nm gate length enhancement and depletion mode InSb quantum well transistors for ultra high speed and very low power digital logic applications," in IEDM' 05 Tech. Dig., 763-766 (2005).

[36] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding, and R. Chau, "High-performance 40nm gate length InSb p-channel compressively strained quantum well field effect transistors for low-power (V_{CC}=0.5V) logic applications," in IEDM' 08 Tech. Dig., 1-4 (2008).

[37] J. L. Freeouf and J. M. Woodall, "Schottky barriers: An effective work function model," Appl. Phys. Lett. **39**, 727-729 (1981).

[38] L. J. Brillson, M. L. Slade, R. E. Viturro, M. K. Kelly, N. Tache, G. Margaritondo, J. M. Woodall, P. D. Kirchner, G. D. Pettit, and S. L. Wright, "Absence of Fermi level pinning at metal-$In_xGa_{1-x}As$(100) interfaces," Appl. Phys. Lett. **48**, 1458-1460 (1986).

[39] M. Passlack, M. Hong, and J. P. Mannaerts, "Quasistatic and high frequency capacitance--voltage characterization of Ga_2O_3-GaAs structures fabricated by in situ molecular beam epitaxy," Appl. Phys. Lett. **68**, 1099-1101 (1996).

[40] M. Passlack, M. Hong, and J. P. Mannaerts, "C-V and G-V characterization of in-situ fabricated Ga_2O_3-GaAs interfaces for inversion/accumulation device and surface passivation applications," Solid-State Electron. **39**, 1133-1136 (1996).

[41] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen and A. Y. Cho, "Demonstration of enhancement-mode p- and n-channel GaAs MOSFETS with $Ga_2O_3(Gd_2O_3)$ As gate oxide," Solid-State Electron. **41**, 751-1753 (1997).

[42] T. D. Lin, H. C. Chiu, P. Chang, L. T. Tung, C. P. Chen, M. Hong, J. Kwo, W. Tsai, and Y. C. Wang, "High-performance self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistor with $Al_2O_3/Ga_2O_3(Gd_2O_3)$ as gate dielectrics," Appl. Phys. Lett. **93**, 033516 (2008).

[43] A. Callegari, P. D. Hoh, D. A. Buchanan, and D. Lacey, "Unpinned gallium oxide/GaAs interface by hydrogen and nitrogen surface plasma treatment," Appl. Phys. Lett. **54**, 332-334 (1989).

[44] H-L. Lu, L. Sun, S-J. Ding, M. Xu, D.W. Zhang, and L-K. Wang, "Characterization of atomic-layer-deposited Al_2O_3/GaAs interface improved by NH_3 plasma pretreatment," Appl. Phys. Lett.**89**, 152910 (2006).

[45] E. O'Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, P. K. Hurleya, B. Brennan, G. Hughes, and S. B. Newcomb "In situ H_2S passivation of $In_{0.53}Ga_{0.47}As$/InP metal-oxide-semiconductor capacitors with atomic-layer deposited HfO_2 gate dielectric," Appl. Phys. Lett. **92**, 022902 (2008).

[46] Yi Xuan, H-C. Lin, and P. D. Ye, "Simplified Surface Preparation for GaAs Passivation Using Atomic Layer-Deposited High-k Dielectrics," IEEE Trans. Electron Devices **54**, 1811-1817 (2007).

[47] Davood Shahrjerdi, Emanuel Tutuc, and Sanjay K. Banerjee, "Impact of surface chemical treatment on capacitance-voltage characteristics of GaAs metal-oxide-semiconductor capacitors with Al_2O_3 gate dielectric," Appl. Phys. Lett. **91**, 063501 (2007).

[48] Y. Q. Wu, M. Xu, R.S. Wang, O. Koybasi, and P. D. Ye, "High Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with maximum G_m exceeding 1.1 mS/μm: New HBr Pretreatment and Channel Engineering," in IEDM' 09 Tech. Dig. 1-4, (2009).

[49] Y. Xuan, Y. Q. Wu, and P. D. Ye, "High-Performance Inversion-Type Enhancement-Mode InGaAs MOSFET With Maximum Drain Current Exceeding 1 A/mm," IEEE Electron Device Lett. **29,** 294-296 (2008).

[50] Hyoung-Sub Kim, Injo Ok, Manhong Zhang, Changhwan Choi, Tackhwi Lee, Feng Zhu, Gaurav Thareja, Lu Yu, and Jack C. Lee, "Ultrathin HfO_2 (equivalent oxide thickness = 1.1 nm) metal-oxide-semiconductor capacitors on n-GaAs substrate with germanium passivation," Appl. Phys. Lett. **88**, 252906 (2006).

[51] Hyoung-Sub Kim, Injo Ok, Manhong Zhang, Tackhwi Lee, Feng Zhu, Lu Yu, and Jack C. Lee, "Metal gate-HfO_2 metal-oxide-semiconductor capacitors on n-GaAs substrate with silicon/germanium interfacial passivation layers," Appl. Phys. Lett. **89**, 222903 (2006).

[52] C.L. Hinkle, M. Milojevic, E.M. Vogel, and R.M. Wallace, "Surface passivation and implications on high mobility channel performance (Invited Paper)," Microelectron. Eng. **86**, 1544-1549 (2009).

[53] Hock-Chun Chin, Ming Zhu, Ganesh S. Samudra, and Yee-Chia Yeoz, "n-Channel GaAs MOSFET with TaN/HfAlO Gate Stack Formed Using In Situ Vacuum Anneal and Silane Passivation," J. Electrochem. Soc. **155**, H464-H468 (2008).

[54] Hock-Chun Chin, Ming Zhu, Xinke Liu, Hock-Koon Lee, Luping Shi, Leng-Seow Tan, and Yee-Chia Yeo, "Silane–Ammonia Surface Passivation for Gallium Arsenide Surface-Channel n-MOSFETs" IEEE Electron Device Lett. **30**, 110-112 (2009).

[55] Hock-Chun Chin, Xinke Liu, Xiao Gong, and Yee-Chia Yeo, "Silane and Ammonia Surface Passivation Technology for High-Mobility $In_{0.53}Ga_{0.47}As$ MOSFETs," IEEE Trans. Electron Devices **57**, 973-979 (2010).

[56] Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu,1 S. Park, J. Yum, H. Zhao, Jack C. Lee, Prashant Majhi, N. Goel, W. Tsai, C. K. Gaspe, and M. B. Santos, "A study of metal-oxide-semiconductor capacitors on GaAs, $In_{0.53}Ga_{0.47}As$, InAs, and InSb substrates using a germanium interfacial passivation layer," Appl. Phys. Lett. **93**, 062111 (2008).

[57] Fei Gao, S. J. Lee, Rui Li, S. J. Whang, S. Balakumar, D. Z. Chi, Chia Ching Kean, S. Vicknesh, C. H. Tung, and D.-L. Kwong, "GaAs p- and n-MOS devices integrated with novel passivation (plasma nitridation and AlN-surface passivation) techniques and ALD-HfO_2/TaN gate stack," in IEDM' 06. Tech. Dig., 1-4, (2006).

[58] H. Hasegawa and M. Akazawa, "Surface passivation technology for III-V semiconductor nanoelectronics," Appl. Surf. Sci. **255**, 628-632 (2008).

[59] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," Appl. Phys. Lett. **92**, 071901 (2008).

[60] Y. Q. Wu, W. K. Wang, O. Koybasi, D. N. Zakharov, E. A. Stach, S. Nakahara, J. C. M. Hwang, and P. D. Ye, "0.8-V Supply Voltage Deep-Submicrometer Inversion-Mode $In_{0.75}Ga_{0.25}As$ MOSFET" IEEE Electron Device Lett. **30**, 700-702 (2009).

[61] Chien-I Kuo, Heng-Tung Hsu, Edward Yi Chang, Chia-Yuan Chang, Yasuyuki Miyamoto, Suman Datta, Marko Radosavljevic, Guo-Wei Huang, and Ching-Ting Lee, "RF and Logic Performance Improvement of $In_{0.7}Ga_{0.3}As$/InAs/$In_{0.7}Ga_{0.3}As$ Composite-Channel HEMT Using Gate-Sinking Technology," IEEE, Electron Device Lett. **29**, 290-293 (2008).

[62] D.-H. Kim and J. A. d. Alamo, "30-nm InAs Pseudomorphic HEMTs on an InP Substrate With a Current-Gain Cutoff Frequency of 628 GHz," IEEE, Electron Device Lett. **29**, 830-833 (2008).

Chapter 2

FABRICATION AND CHARACTERIZATION METHODS

This chapter focuses on the description of the film deposition techniques, fabrication processes and characterization techniques used for analysis in this dissertation. Atomic layer deposition (ALD) and electron beam evaporation techniques were used for the high k gate deposition and metal deposition, respectively. Since the study focuses on high k/ III-V interface, some electrical and physical characterization techniques were used. The electrical characterization techniques described are capacitance-voltage, conductance-voltage and current-voltage measurements. The analytical characterization techniques discussed are x-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HRTEM).

2.1. Fabrication techniques

2.1.1. Atomic layer deposition (ALD)

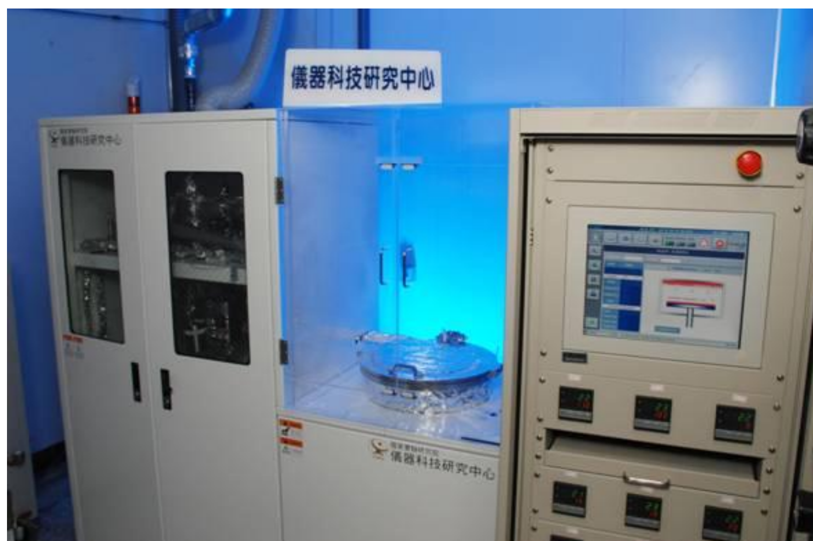


Figure 2.1. The 8 inch ALD system at instrument technology and research center (ITRC), Hsinchu, Taiwan. This system was mostly used for the deposition of high k oxides in this work

Principles

Atomic layer deposition (ALD), also known as atomic layer epitaxy (ALE) or atomic layer chemical vapor deposition (ALCVD), can be considered as an advanced variant of the well-known chemical vapor deposition (CVD) technique. The ALD was developed in Finland by T. Suntolan and coworkers in 1974 to meet the industrial needs for producing high-quality and long-life thin film electroluminescent (TFEL) displays [1].

The principles of the ALD for thin film growth emphasize the aspects of a self-limiting mechanism. The distinct feature of ALD is that the film is grown through sequential saturated surface reactions that are realized by pulsing the two (or more) precursors into the reactor alternately, one at a time, separated by purging or evacuation steps [2]. In other words, in ALD, the growth of thin films takes place by surface-controlled growth cycles. An ideal growth cycle consists of (1) exposure of the substrate surface to the pulse of the first gaseous precursor and its chemisorption onto the surface, (2) inert gas purge to remove the unreacted precursor, (3) introduction of the second precursor followed by surface reaction between the precursors to produce the desired film material, and finally (4) inert gas purge to expel the excess of precursor and volatile reaction by-products (Fig. 2.2) [3].

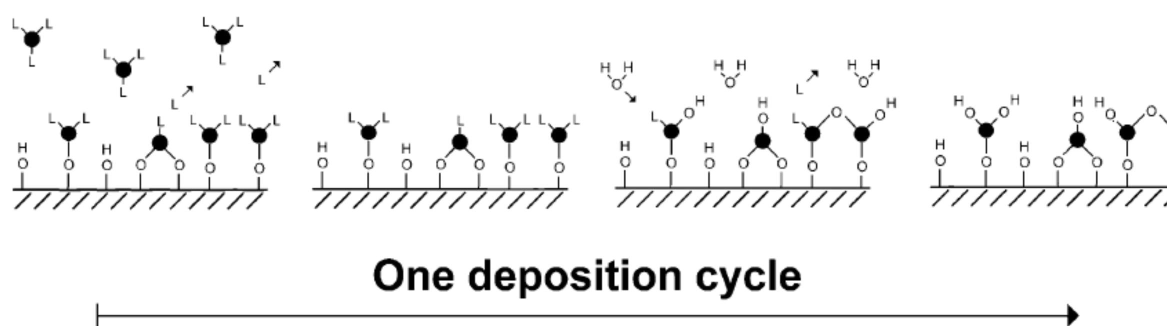
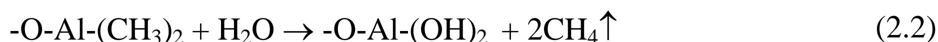


Figure 2.2. Schematic illustration describing an ALD deposition cycle leading to the formation of a binary oxide film consisting of metal (•) and oxygen (◦) atoms. L refers to the precursor ligand [3]

The process of the deposition of Al_2O_3 by ALD uses tri-methyl aluminum (TMA) and H_2O as precursors. The deposition process schematic is shown in Fig. 2.3 [4]. Starting surface always adsorbs H_2O vapor in air, forming hydroxyl (OH) groups. After loading into ALD reactor, TMA is pulsed into reaction chamber and reacts with hydroxyl groups (step 1):

$$\text{-OH} + Al(CH_3)_3 \rightarrow \text{-O-Al-}(CH_3)_2 + CH_4\uparrow \tag{2.1}$$

Reactions continue until the surface is passivated, results in forming a layer of $-Al-(CH_3)_2$ on the surface. TMA does not react with itself, terminating the reaction to one layer (step 2). The excess TMA and CH_4 product is then purged away by inert gas to finish the first half of cycle. In the second half of cycle, the H_2O vapor precursor is pulsed into the chamber. H_2O reacts with dangling methyl groups on the new surface forming Al-O bridges and hydroxyl surface groups (step 3):



$$\text{-O-Al-}(CH_3)_2 + H_2O \rightarrow \text{-O-Al-}(OH)_2 + 2CH_4\uparrow \tag{2.2}$$

H_2O does not react with OH groups causing one perfect hydroxyl terminal layer. The excess H_2O and CH_4 production are purged away by inert gas (step 4). A new cycle is started with (OH) functional groups surface and TMA pulse. By this way Al_2O_3 film is formed. The bottom-left of the Fig. 2.2 shows the finished Al_2O_3 film after 3 ALD cycles. The overall reaction of TMA and H_2O in the formation of Al_2O_3 oxide is described as [4, 5].

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4\uparrow \tag{2.3}$$

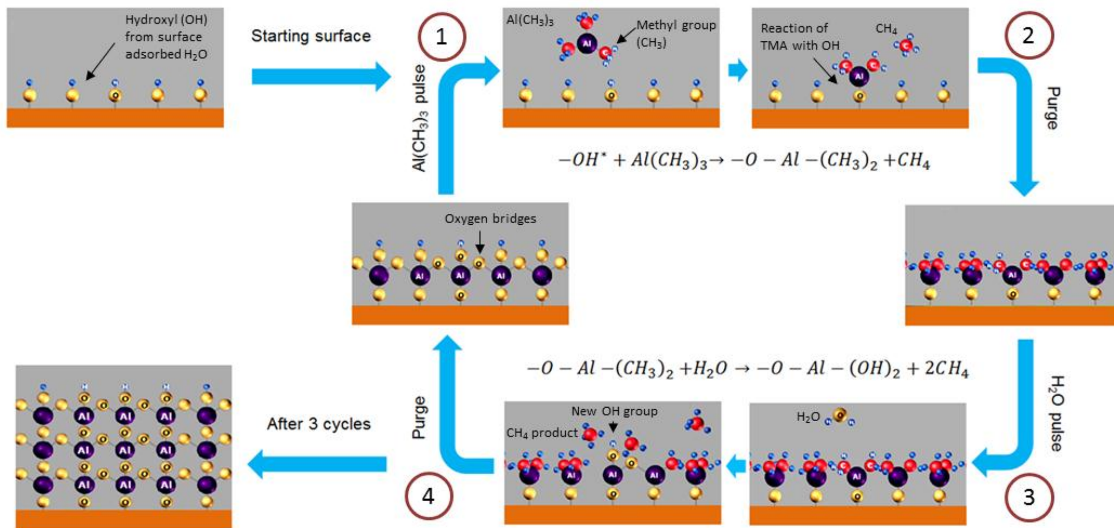


Figure 2.3. Schematic describing the alternating TMA and H_2O pulses in ALD chamber leading to form sequence Al_2O_3 layers [4].

The ALD growth temperature is dictated by precursor chemistry, to a regime where the surface-limited reactions occur. Reactivity of the metal precursor mainly determines the temperature range where ALD growth occurs. In addition to self-liming growth, a region of temperature with a constant deposition rate, a so-called ALD window, is often observed (Fig. 2.4) [3]. Except some few cases, the ALD windows are often reasonably wide, can extend over hundreds of degrees [2].

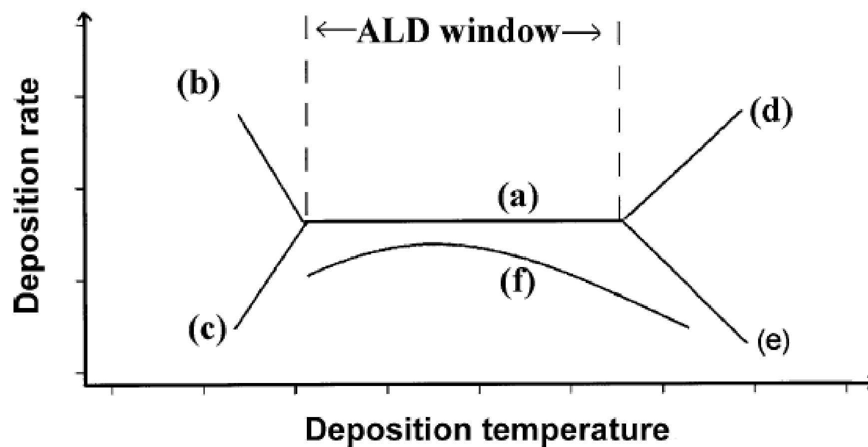


Figure 2.4. Scheme of (a) ALD processing window limited by (b) precursor condensation, (c) insufficient reactivity, (d) precursor decomposition and (e) precursor desorption. If deposition rate is dependent on the number of available reactive sites as in (f), no actual ALD window is observed [3]

Advantages and limitations

The surface-controlled growth mode produces some obvious advantages as summarizing in the table 2.1 [2]. Among them the fact that the precursor pulse length, i.e., dose, has no effect on the growth rate provided that the surface is saturated, i.e., all available surface sites are occupied by the precursor molecules (Fig. 2.5) [2, 3]. Furthermore, because the growth is by cycles, the thickness control is facile and is achieved by monitoring the number of ALD cycles. Similarly, uniform doping is easy to accomplish by replacing, at a desired interval, the growth cycle by a doping cycle [2, 3].

Table 2.1. Relationships between characteristics and advantages of ALD [2]

Characteristic feature of ALD	Implication for film deposition	Practical advantage
Self-limiting growth process	Film thickness is dependent only on the number of deposition cycles	Accurate and simple thickness control
	No need for reactant flux homogeneity	Large area capability Large batch capability Excellent conformality No problems with inconstant vaporization rates of solid precursors Good reproducibility Straightforward scale-up
	Atomic level control of material composition	Capability to produce sharp interfaces, nanolaminates and superlattices Possibility to interface modification
Separate dosing of reactants	No gas phase reactions	Allows a use of precursors highly reactive towards each other, thereby enabling effective precursor utilization and short cycle times
	Sufficient time is given to complete each reaction step	High quality materials are obtained at low deposition temperatures
Processing temperature windows are often wide	Processing conditions of different materials are readily matched	Straightforward preparation of multilayer structures in a continuous process

Another advantageous and inherent feature of ALD originates from its surface-controlled nature which allows substrates of various sizes and geometries to be uniformly coated [2, 3]. The preparation of multicomponent and multilayer materials is further facilitated since the ALD windows are often wide which allows binary processes easy to combine [2]. The alternate supply of the precursors in the well-separated pulses ensures that the precursors never meet in the gas phase. This eliminates risks of gas phase reactions with possible detrimental consequences such as particle formation [2].

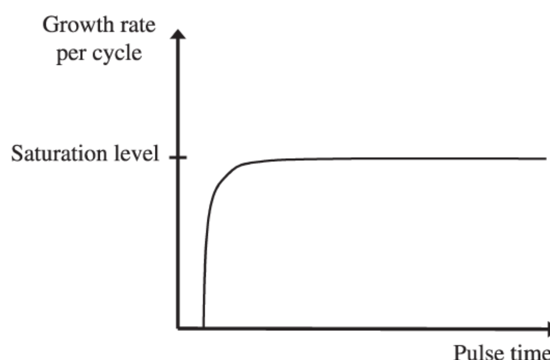


Figure 2.5. Saturation of surface reactions in ALD processes is experimentally verified by observing that the deposition rate per cycle stabilizes to a constant level with increasing precursor pulse time or dose [2].

The main disadvantage of ALD is the low deposition rate which is a direct consequence of layer by layer film growth. In addition, ALD does not produce a full monolayer of a film in one deposition cycle but only a fraction of thereof. Thus, ALD is a relatively slow technique when a thick film, hundreds of nanometers or more, needs to be deposited. Typically, the deposition rate is in the range of 100-300 nm per hour. However, for the high k gate oxide application which needs very thin film, the deposition rate restrictions are somewhat more relaxed than most other areas.

2.1.2. Electron beam evaporation

The electron beam evaporation method is used for metal deposition. A wide variety of materials including refractory metal (such as tungsten), low vapor pressure metal (such as platinum), and alloys can be evaporated. The schematic of electron beam evaporation system is shown in Fig. 2.6. The process begins under a vacuum of 10^{-5} torr or less. A tungsten filament inside the electron gun is heated. When the filament becomes hot enough, it begins to emit electrons. These electrons form a beam which is accelerated due

to high voltage dc power (~10 kV). Electron beam is then deflect and focused on the metal source to be evaporated by means of a magnetic or electric fields. The electron beam strikes the target surface and transforms the kinetic energy into thermal energy. This is the energy which vaporizes the metal target. The metal vapor is then deposited on the sample.

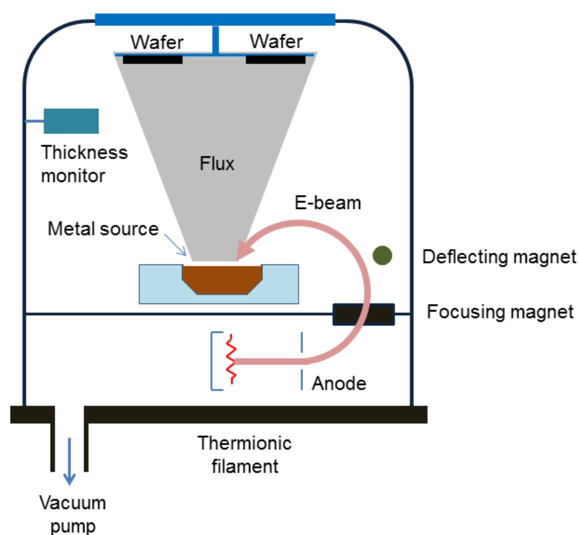


Figure 2.6. Schematic of electron beam evaporation system for metal deposition

2.2. Fabrication process

The process for MOSCAPs fabrication in this work was based on ALD and e-beam evaporation techniques. Figure 2.7 shows the Al_2O_3/InGaAs, InAs MOSCAPs structures used in this study. Epi-layers of n-$In_{0.53}Ga_{0.47}As$, n-$In_{0.7}Ga_{0.3}As$, and InAs were commercial molecular beam epitaxy (MBE) grown on n^+-InP wafers by the IQE company.

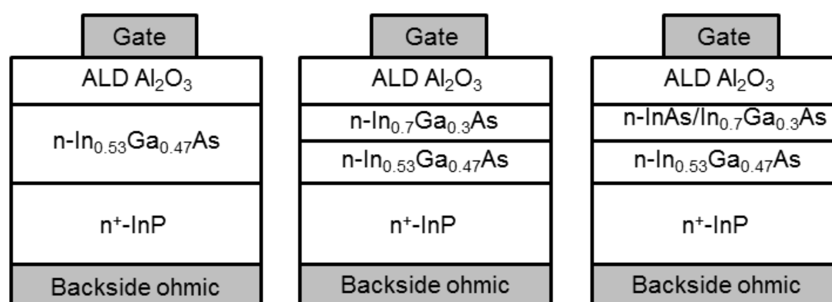


Figure 2. 7. The Al_2O_3/InGaAs, InAs MOSCAPs structures used in this work

Generally, the procedure can be described in Fig. 2.8. The InGaAs, InAs surfaces were first degreased by acetone (ACE) and iso-propanol (IPA) and followed by blown dry by N_2 gun. After that, ex-situ chemical solutions treatments were performed in order to minimize surface native oxides. HCl and $(NH_4)_2S$ solutions were used as chemical solutions. In ALD chamber, in-situ pretreatment step was carried out by pulse several TMA/N_2 cycles before deposition of Al_2O_3. After that, post deposition annealing (PDA) was performed following by the deposition of backside ohmic contact and gate metal by e-beam evaporators. Au/Ge/Ni/Au and Ti/Pt/Au were always used as back side ohmic and gate metals contact. Finally, post metallization annealing (PMA) was performedto complete the fabrication process.

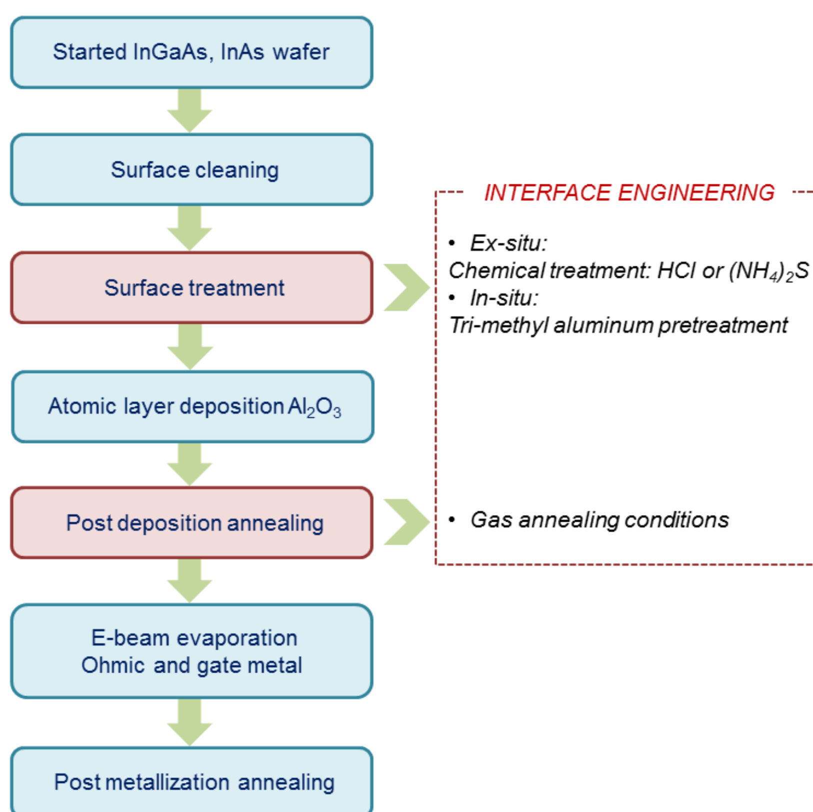


Figure 2.8. Process flow of Al_2O_3/InGaAs, InAs MOSCAPs fabrication, focusing on the interface engineering

Since this work focused on the improvement of Al_2O_3/InGaAs, InAs interfaces, the surface treatments and PDA steps were carefully studied. The details of surface treatment methods and gas annealing conditions will be described in the following chapters. After fabricating, MOSCAPs were characterized by multi-frequency capacitance-voltage (C-V),

conductance-voltage (G-V), quasi static C-V (QSCV), and current-voltage (I-V, J-V) measurements.

2.3. Analytical techniques

2.3.1. X-ray electron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis (ESCA), is one of the most powerful and common chemical analysis techniques, especially for surface and interface analysis. XPS is based on the photoelectric effect in which the binding energy (E_B) of a core-level electron is overcome by a sufficient impinging soft X-ray photon, and the core-level electron is excited and rejected from atom, called photoelectron (Fig. 2.9) [6]. Determining the kinetic energy of photoelectron, i.e., binding energy E_B will give meaningful chemical information of an analyzed sample.

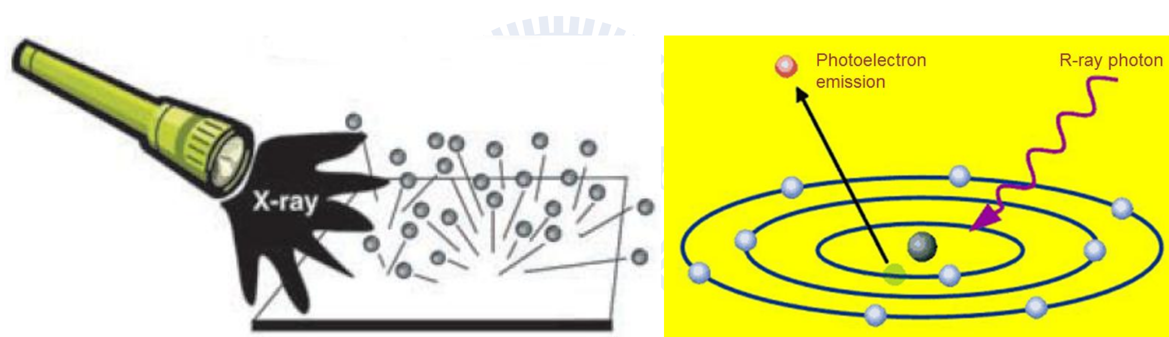


Figure 2.9. Surface irradiated by sufficient energy X-ray photon beam will emit photoelectrons: phenomenon (left) and principle schematic (right) [7, 8]

<u>Historical</u>

The photoelectric effect was first observed by Heinrich Hertz in the 1880s. He noticed that metal contacts in electrical systems, when exposed to light, exhibit an enhanced ability to spark [7]. The photoelectron effect was then confirmed and studied more details by the experiments of Hallwachs in 1888, and J. J. Thompson in 1899. Finally, in 1905, Einstein, using Planck's 1900 quantization of energy concept, correctly explained all these observations - photons of light directly transferred their energy to electrons within an atom, resulting in the emission of the electrons without energy loss [7]. By this quantum theory development, Einstein was awarded the Nobel Prize in 1921.

The photoelectric effect has been then applied as an analytical method. In 1914, Robinson and Rawlinson reported recognizable gold photoemission spectrum. In 1951, Steinhardt and Serfass first applied photoemission as an analytical tool. Throughout the 1950s and 1960s, Kai Siegbahn developed the instrumentation and theory of ESCA to give us the method we use today. Siegbahn also coined the term 'electron spectroscopy for chemical analysis' later modified by his group to 'electron spectroscopy for chemical applications.' In 1981, Kai Siegbahn was rewarded for his contributions with the Nobel Prize in Physics [6, 7].

Principle

When a photon impinges upon an atom, one of following phenomena may happen: (1) photon can pass through with no interaction, (2) photon is scattered by an atomic orbital electron, and (3) photon interacts with an atomic orbital electron with total energy transfer to electron, leading to electron emission from atom (Fig. 2.9, right). If the photon is scattered, the phenomenon is referred to as "Compton scattering". If the photon interacts with the electron, the phenomenon describes the photoemission process, a basic of XPS. To let the core-level electron emits from atom, the impinged photon energy, hν needs to be higher than the electron binding energy, E_B. Electrons emitted from atoms by this process are called photoelectrons. The kinetic energy of a photoelectron, KE is simply described by the Einstein's equation:

$$E_B = h\nu - KE \quad (2.4)$$

One can measure the kinetic energy of photoelectron the binding energy is obtained according to equation (2.4). The value of E_B will provides valuable information about photo-emitting atom.

The emission of core-level electron will result in the rearrangement of atomic orbitals and the emission of Auger electron or X-ray photon as described in Fig. 2.10 [7]. Binding energy of the ejected photoelectron depends on the final state configurations after photoemission [6, 7].

The concept of the binding energy of an electron in an atom requires elaboration. A negatively charged electron will be bound to the atom by the positively charged nucleus. The closer the electron is to the nucleus, the more tightly it is expected to be bound. Binding energy will vary with the type of atom (i.e., a change in nuclear charge) and the

addition of other atoms bound to that atom (bound atoms will alter the electron distribution on the atom of interest). Different isotopes of a given element have different numbers of neutrons in the nucleus, but the same nuclear charge. Changing the isotope will not appreciably affect the binding energy. Weak interactions between atoms such as those associated with crystallization or hydrogen bonding will not alter the electron distribution sufficiently to change the measured binding energy. Therefore, the variations in the binding energy that provide us with the chemical information content of XPS are associated with covalent or ionic bonds between atoms. These changes in binding energy are called binding energy shifts or chemical shifts.

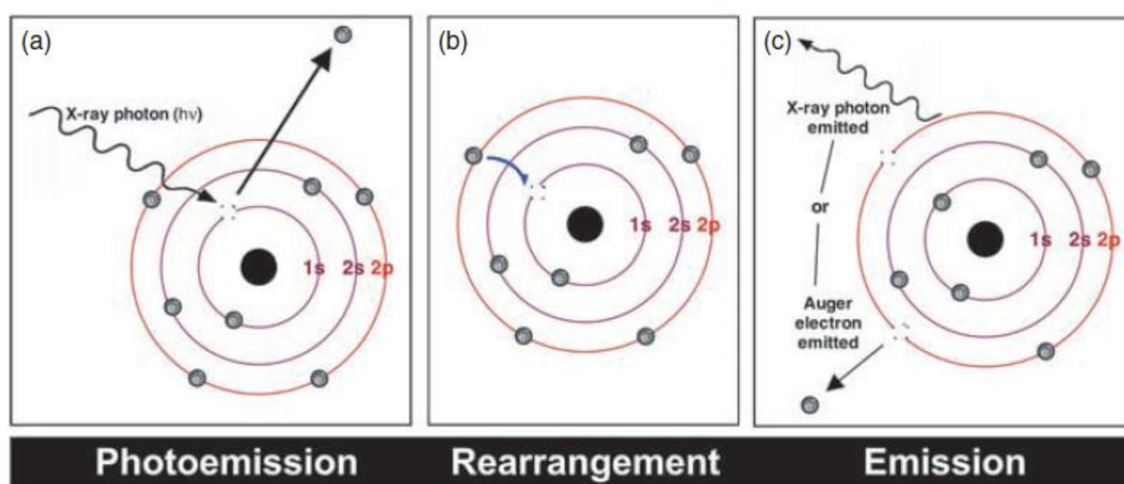


Figure 2. 10. (a) The X-ray photon transfers its energy to a core-level electron leading to photoemission from the n-electron initial state. (b) The atom, now in an (n-1)-electron state, can reorganize by dropping an electron from a higher energy level to the vacant core hole. (c) Since the electron in (b) dropped to a lower energy state, the atom can rid itself of excess energy by ejecting an electron from a higher energy level. This ejected electron is referred to as an Auger electron. The atom can also shed energy by emitting an X-ray photon, a process called X-ray fluorescence

The varying of binding energy with the type of atom and the chemical shifts are the key features of XPS. With these features, XPS enables qualitative elemental identification the entire periodic table save H and He. Chemical bonds between atoms are also identified. Simple identification can be achieved by recording low resolution spectra over a broad binding energy range, called survey scans. Figure 2.11 shows a XPS survey scan of an ALD 1.5 nm Al_2O_3/InAs sample as an example. The inset shows the peak's separation of As-In and As-O bonds due to chemical shift in As 3d XPS spectra.

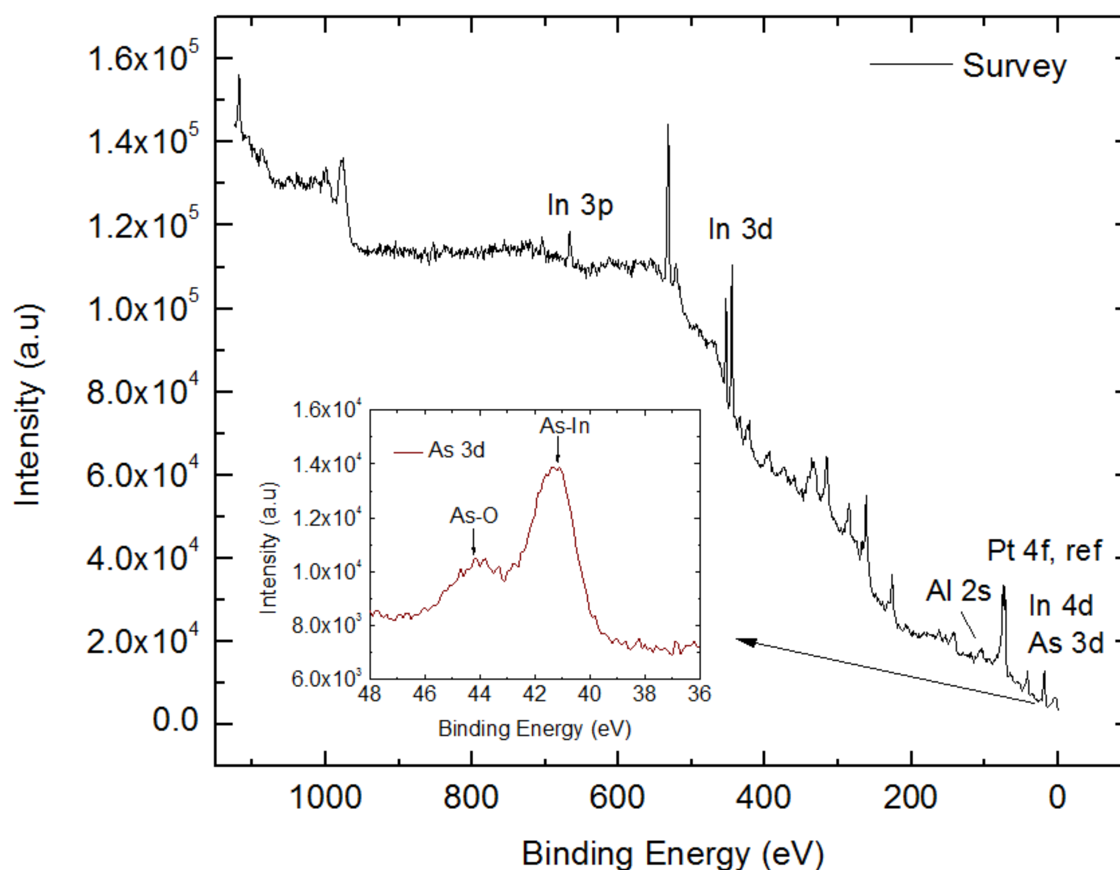


Figure 2.11. XPS survey scan of Al_2O_3/InAs sample, the inset shows As 3d spectra

Figure 2.12 presents a simplified schematic diagram of an X-ray photoelectron spectrometer. The photons generated from the X-ray source impinge upon the sample, resulting in the ejection of photoelectrons from sample. The photoelectrons are collected by electron optics and directed into an electron energy analyzer where they are sorted by energy. The number of electrons per energy interval is then transduced to a current by an electron detector. The photocurrent is subsequently converted and processed into a spectrum by suitable electronics. The experiment is typically performed under ultra-high vacuum (UHV) conditions, about 10^{-9}-10^{-11} torr. This high vacuum is needed in order to maintain sample surface integrity (the surface gas adsorption) and minimize the scattering of photoelectrons by others gas molecules [6]. Due to the relatively short inelastic mean free path in the irradiated material and the typical kinetic energies possessed by the photoelectrons, only the photoelectrons produced in the top several mono-atomic-layers of the sample are observed as their characteristics energies. Thus, the XPS is typically useful for surface and interface analysis.

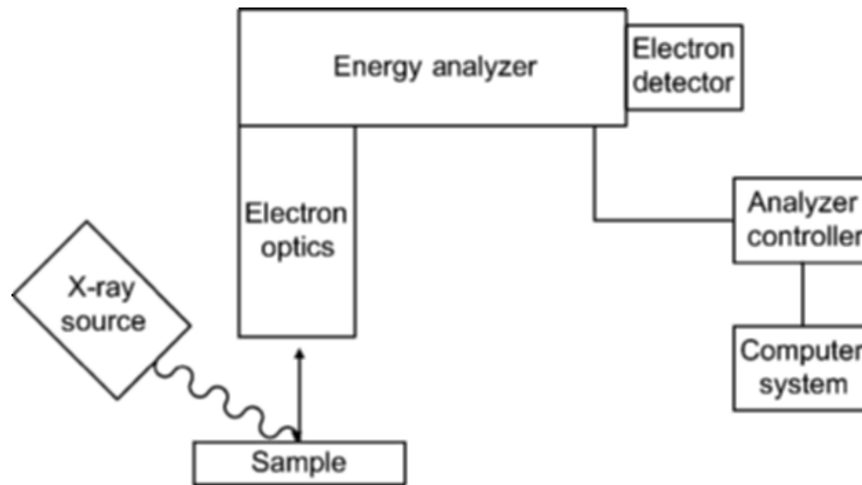


Figure 2.12. Schematic design of an X-ray photoelectron spectrometer

As discussed before, binding energy, E_B of photoelectron is determined by measuring the kinetic energy of photoelectron, KE. To measure photoelectron KE for different kinds of materials, samples are placed in electrical contact with the spectrometer (in case sample is conductance), typically by grounding both the sample and the spectrometer. By this way, the Fermi level, E_F of both the sample and spectrometer is putted at the same energy level (Fig. 2.13). The binding energy, referenced to Fermi level is then determined through measured KE and the work function of spectrometer ϕ_{sp} by the following equation (see Fig. 2.13):

$$E_B^F = h\nu - KE - \phi_{sp} \quad (2.5)$$

For the case of insulating samples, as photoelectrons are emitted after X-ray bombardment, the sample becomes positive charge and cannot compensate as conducting samples. As a result, the Fermi level of the sample and spectrometer may be different, leading to error in the binding energies calculated from the photoelectrons' kinetic energies. In this case, "charge neutralization" or "charge compensation" process is needed to compensate the accumulation positive charges. The use of flood guns which provide a source of low energy electrons to take place of the ejected photoelectrons is a common technique [6, 7]. Additionally, the differential charging may also be reduce through placing addition sources such as placing of metallic wall surrounding the sample, placing the sample on a conductive platform, and mixing the sample with another substance [6].

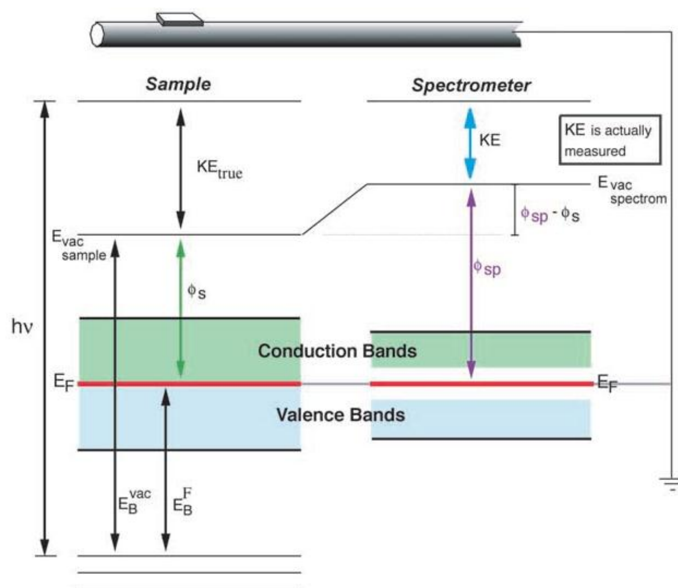


Figure 2.13. The energy level diagram for an electrically conducting sample that is grounded to the spectrometer. The Fermi levels of the sample and spectrometer are aligned ($E_{F(s)} = E_{F(sp)}$) so that E_B is referenced with respect to E_F. The measurement of E_B is independent of the sample work function, φ_s, but is dependent on the spectrometer work function, φ_{sp}

Peak fitting

To detail the information from XPS spectra, the area and E_B of each subpeak for a given orbital must be determined. Typically, the spacing between subpeaks is similar to peak width (~1 eV). Hence, it is rare when individual subpeaks are completely separated in an experimental spectrum. This requires the use of a peak fitting procedures to resolve the desired peak parameters. Parameters used in such procedures include the background, peak position, peak width, and peak shape (Gaussian, Lorenzian, asymmetric, or mixture thereof).

In this work, the XPSPEAK software, version 4.1 is used for the peak fitting (see Fig. 2.14). After loading the experiment data file, the background of spectrum is set. The most common method which is used to model the background (inelastic scattering) was developed by Shirley, called Shirley's background model. Others background models are Tougaard background model and linear background model. After setting background, adding/adjusting processes can procedure. The software provides some features which allow user to adjust the number of peaks as well as peaks' parameters such as peak type, peak position, FWHM, % Lorentzian-Gaussian, etc. The details about software as well as the guide of using is supported free and can be found online [9].

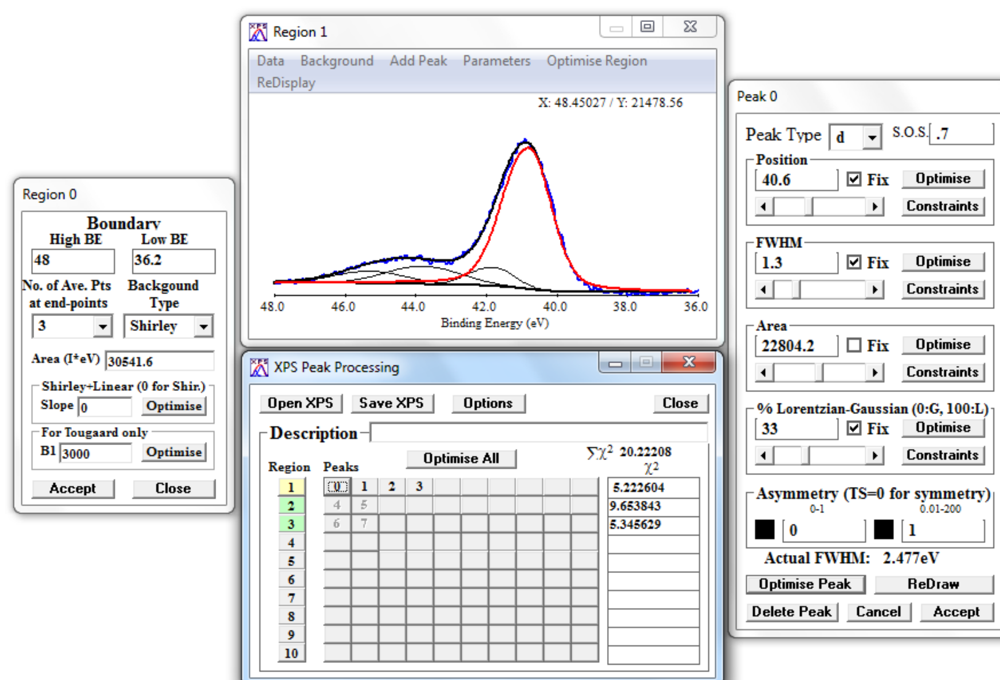


Figure 2.14. The control windows of XPSPEAK software, version 4.1

2.3.2. High-resolution transmission electron microscopy (HRTEM)

High-resolution transmission electron microscopy (HRTEM) is a powerful analysis technique in the structural characterizations of thin films and multilayered heterostructres. The principle of HRTEM is somewhat similar to that of an optical microscope, but the electron beam and electromagnetic lenses are used instead of invisible light beam and optical lenses. The schematic of a TEM is shown in Fig. 2.15. The technical explanation of typical TEMs working can be described as follows [10]. Essentially, the electron source is an electron gun which produces a beam of monochromatic electrons. The electrons' energy is typically from 100 keV to 1 MeV, depending on the resolution level. This e-beam is focused on a small, thin, coherent beam by the use of condenser lenses 1 and 2. The first lens largely determines the "spot size", the general size range of the final spot that strikes the sample. The second condenser lens actually changes the size of spot on the sample, changing it from a wide dispersed spot to a pinpoint beam. The beam is then restricted by the condenser aperture which knocking out high angle electrons. After that, the beam strikes the specimen and parts of it are transmitted. This transmitted portion is focus by the objective lens into an image. Optional objective and selected area metal apertures can restrict the beam; the objective aperture enhancing contrast by

blocking out high-angle diffracted electrons, the selected area aperture enabling the user to examine the periodic diffraction of electrons by ordered arrangements of atoms in the sample. The image is passed down the column through the intermediate and projector lenses, being enlarged all the way. The image strikes the phosphor image screen and light is generated, allowing the user to see the image. The darker areas of the image represent those areas of the sample that fewer electrons were transmitted through (they are thicker or denser). The lighter areas of the image represent those areas of the sample that more electrons were transmitted through (they are thinner or less dense).

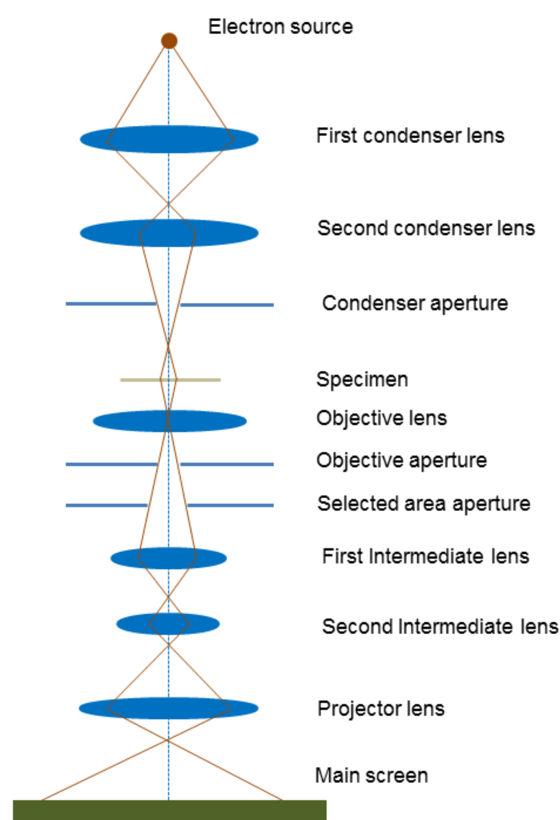


Figure 2.15. Principle schematic of a transmission electron microscopy (TEM)

Since the method using electron transmission, the thickness of specimen is required extremely small (10-100nm) to let electrons transmit. The preparation of such a thin sample is the most difficult and key step to succeed in characterization. Electrons transmit through the specimen; they suffer coherent scattering from the crystalline atoms and incoherent scattering at grain boundaries, defects, amorphous particles, etc. The former is used to form a diffraction pattern of the specimen to study the crystalline quality and the epitaxial nature of the thin film. The incoherent scattering effect that leads to a spatial

variation in the intensity of the primary transmitted beam is used to study the microstructure of the thin film in terms of grain boundaries, defects and amorphous particles. The primary and diffracted beams emerging from the thin film specimen pass through the objective lens to form the first image. By using the amplitude contrast of the primary beam or a single diffraction beam, bright field or dark field imagines of specimen can be obtained. By using the phase contrast between the primary the primary beam and one or more of the diffracted beams, high-resolution images can be obtained. This technique is used for studying the atomic structures in multilayer films. In this work, it is used to examine the Al_2O_3/InGaAs, InAs interfaces.

2.4. Electrical techniques

2.4.1. Capacitance-voltage (C-V), conductance-voltage (G-V) measurements

Multi-frequency C-V and G-V measurements

The multi-frequency C-V and G-V characteristics of MOSCAPs were measured by using an Agilent HP4284A precision LCR meter. The parallel model was chosen to obtain both measured capacitance (C_m) and conductance (G_m) in the same time. The capacitance versus gate voltage was determined by superimposing a small-amplitude sinusoidal ac voltage v on the bias dc voltage V. The ac frequency can vary from 20 Hz to 1MHz with typically 10-50 mV amplitude. The capacitance is then defined by

$$C_m = \frac{dQ_M}{dV} = -\frac{dQ_s}{dV} \tag{2.6}$$

where Q_M and Q_s are the metal and semiconductor charge. The conductance is simultaneous determined by

$$G_m = \frac{dI}{dV} \tag{2.7}$$

where I is the current through the MOSCAP device

The LCR meter measures the device impedance i.e., ratio of the output ac current to the input ac voltage of parallel G-C circuit. The impedance Z is expressed as

$$Z = \frac{G_m}{G_m^2 + (\omega C_m)^2} - \frac{j\omega C_m}{G_m^2 + (\omega C_m)^2} \tag{2.8}$$

The first term is a conductance which is in phase with the input ac signal. The second term is a susceptance which is out of phase 90° with the input. By feeding the output to a phase detector and dissociating the complex impedance into 0° and 90° phases, G_m and C_m are obtained.

The multi-frequency C-V and G-V characteristics are meaningful data which can extract the film properties such as dielectric constant, equivalent oxide thickness, fixed traps, electron traps, mobile charges, substrate doping concentration, etc. Especially, these characteristics support the data to calculate interface state density D_{it} which is one of the most importance parameter of MOSCAP devices. The method of extraction of D_{it} using these data will be presented in the following section. During the C-V and G-V measurements, some issues such as leakage current, substantial series resistance should be considered since they can affect to the accuracy of measured data. A small signal ac data is also suggested to use in order to avoid the dependent of measured capacitance and conductance on ac amplitude. Typically, the ac amplitude in the range 10-50 mV is applicable.

The temperature dependent C-V and G-V characteristics were also performed in this work. For the measurement at temperature higher than room temperature (RT), the chuck which holds samples was heated and cooling water was introduced to keep the temperature at certain value during the measurement. For temperature lower than RT, the samples were hold in a chamber which was introduced gas of liquid nitrogen (77 K). The holder sample chuck was also heated if the measured temperature needs to be higher than 77 K. The temperature dependent measurements we used in order to extract the D_{it} of Al_2O_3/InGaAs at different energy level within InGaAs bandgap and to study the effective Fermi level movement by conductance map method. The details will be presented elsewhere.

Quasi-static C-V measurement

Quasi-static C-V (QSCV) measurement is the technique which allows us to get the full low frequency C-V curve. In this technique, dc bias is varied slowly to let minority carriers as well as slow interface traps can response [11, 12]. The classical QSCV method uses a linear voltage ramp and calculates the capacitance from the following equation:

$$C = \frac{I_{dis}}{dV/dt} \tag{2.9}$$

However, obtaining a successful QSCV measurement using this technique usually entails some trial and error to select proper hold time and ramp rate. To solve this problem, this work used an Agilent 4156C precision analyzer which applies a step voltage technique instead of linear ramp technique to obtain the QSCV measurement. In general, this method is easier and quicker to perform than linear ramp method. Moreover, the 4156C has a unique current compensation feature that enables the measurement of leaky gate oxides [11].

The voltage step QSCV method calculates capacitance from the differential charge required to change the capacitor voltage by an amount ΔV. The charge Q of capacitor has the relation with an applied voltage V by Q = CV. Thus, when the applied voltage change from V_0 to V_1, the charge on the capacitor must change from Q_0 to Q_1 (assuming C is constant). That means when the applied voltage changes by Vstep (=V_0-V_1), the total charge must also change by ΔQ. This change of charge can be determined by integrating current i:

$$\Delta Q = \int idt \tag{2.10}$$

The Agilent 4156C calculates this area using the rectangular approximation method as shown in Figure 2.16.

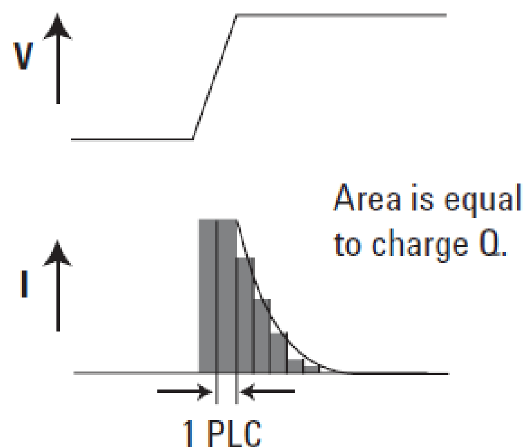
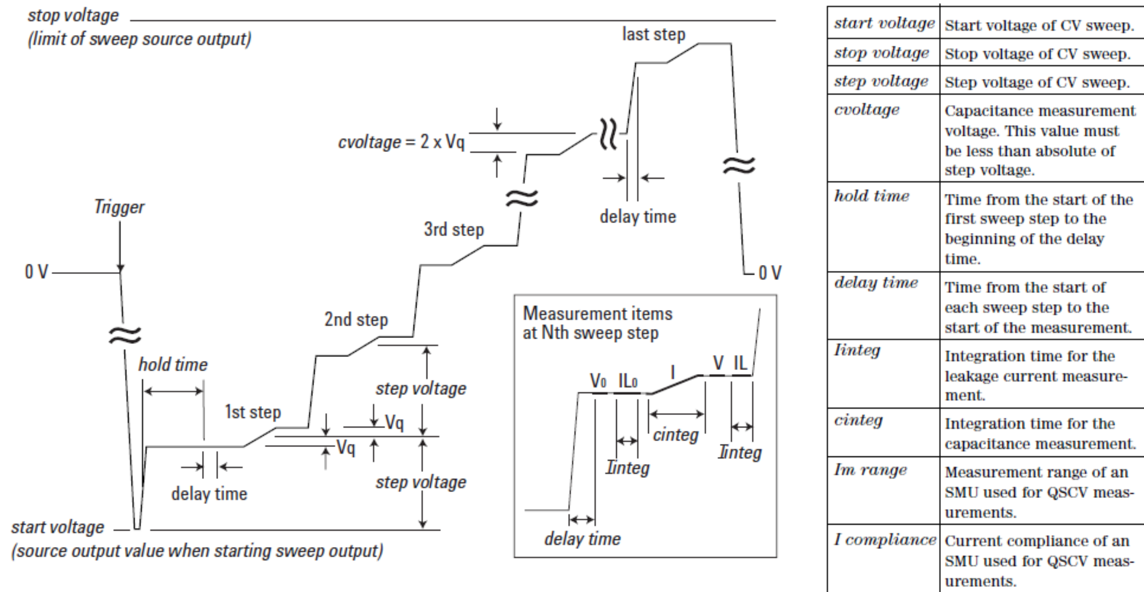


Figure 2.16. Rectangular approximation method used by 4156C [11]

The width of each rectangle is equivalent to one power line cycle (PLC). Thus the actual equation used in calculating the change in charge is:

$$\Delta Q \approx \sum I_k \Delta t_{PLC} \tag{2.11}$$

The 4156C uses two different step voltages to measure capacitance. Figure 2.17 shows the actual voltage wave form forced on the capacitor during a QCSV measurement. The step voltage term determines the points along the total CV sweep where the capacitance is to be measured. The cvoltage term refers to the voltage step applied to the capacitor at each point along the capacitance measurement curve (cvoltage < step voltage)



start voltage	Start voltage of CV sweep.
stop voltage	Stop voltage of CV sweep.
step voltage	Step voltage of CV sweep.
cvoltage	Capacitance measurement voltage. This value must be less than absolute of step voltage.
hold time	Time from the start of the first sweep step to the beginning of the delay time.
delay time	Time from the start of each sweep step to the start of the measurement.
Iinteg	Integration time for the leakage current measurement.
cinteg	Integration time for the capacitance measurement.
Im range	Measurement range of an SMU used for QSCV measurements.
I compliance	Current compliance of an SMU used for QSCV measurements.

Figure 2.17. QSCV measurement sequence [11]

The QSCV measurement operation is as follows:

1. After the QSCV measurement trigger, the SMU forces start voltage.
2. Change the output to (start voltage+step voltage–Vq) and wait for hold time.
3. Wait for delay time.
4. Measure output voltage V0.
5. Measure leakage current IL0.
6. Start the AD conversion and change the output voltage by cvoltage. The AD conversion continues for cinteg.
7. Measure the output voltage V.

8. Measure leakage current IL.
9. Calculate the capacitance over k power line cycles (PLCs) using the following equation:

$$C = \frac{\Delta Q_{Cap}}{\Delta V} = \frac{\Delta Q_{total} - \Delta Q_{leak}}{\Delta V} = \frac{(\sum I_k \Delta t_{PLC}) - [0.5(IL - IL_0)(2.cinteg - (j - 0.5).\Delta t_{PLC}]}{V - V_0} \quad (2.12)$$

j∈ {1, 2, 3, …k}and j is the PLC in which the VAR1 SMU is no longer in current compliance (I compliance).

10. Change the output to (start voltage+2_step voltage–Vq) and wait for delay time. This is similar to the step 3.
11. Continue the steps between 4 and 10 until the last step.
12. After the QSCV sweep completes, the output voltage is changed to 0 V.

The leakage current should be small, in the range of 1nA for the accurate capacitance measurement. However, if the leakage current too large, the QSCV curve can be still determined by using leakage compensation feature. More details about the measurement can be found from ref [11].

2.4.2. Current-voltage (I-V, J-V) measurement

Current-voltage characteristic of MOSCAP's structures were measured using a Keithley 4200 semiconductor analyzer. The current densities at different gate voltages or electric fields are measured by applying a ramped or stepwise dc bias on the top gate electrode of a MOSCAP. The III-V substrate contact, i.e., backside contact, should be electrically grounded. This was done by grounding the aluminum chuck in our experiment. To realize this measurement configuration, the tungsten (W) probe that contacts the top gate electrode has to function as both a voltage source and a current detector at the same time.

Similar to the quasi-static C-V measurements, both a displacement component and a leakage component contribute to the measured current when using a ramped voltage sweep. In the case of I-V measurements, however, the displacement current contribution has to be minimized to avoid the screening effect. A very slow voltage ramp, e.g., 0.01 V/second, should be applied to reduce the displacement current, especially at the low voltage range where the leakage current is very small. Another approach is to use a

stepwise voltage sweep with a long delay time, e.g., 1-2 seconds. However, the delay time should not be set too large either to avoid an excessive electron trapping during this constant voltage stress

2.4.3. Conductance and conductance contour methods

Conductance method is one of the most sensitive methods to determine interface trap densities. This method, proposed by Nicollian and Goetzberger in 1967, is also the most complete method because it yields D_{it} in the depletion and weak inversion portion of the bandgap, the capture cross-sections for majority carriers, and information about surface fluctuations [12]. Firstly, let us describe the capture-emission process by interface traps. The band diagram of a typical MOSCAP is shown in Fig. 2.18, where a gate voltage V_G is applied between the metal and the semiconductor, which fixes the value of the surface Fermi level (surface potential) [13].

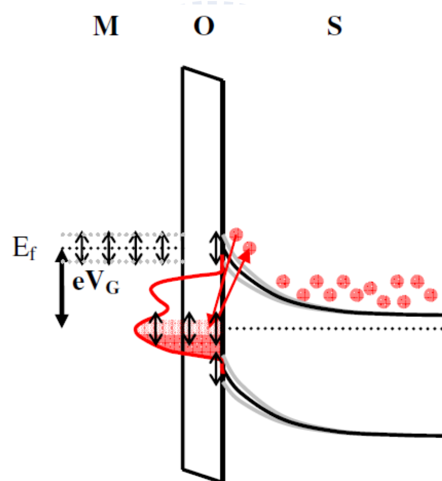


Figure 2. 18. Band diagram of an n-type MOS structure with a bias voltage V_G applied between metal and semiconductor [13].

A hypothetical interface state distribution at the semiconductor/oxide interface is also shown on the band diagram. The C-V measurements consist in applying on top of the static gate bias voltage a small sinusoidal voltage with frequency f and amplitude of the order of 10-50 mV. This small periodic gate voltage causes the bands and the surface potential in the semiconductor to periodically move up and down, causing the interface traps lying around the value of the surface potential to fill and empty. Only if the traps around the surface potential have a characteristic response time that is of the order of the measurement frequency f can interact with the measurement ac signal and affect the total impedance of

the MOS capacitor. Therefore, the characteristic times related to carrier trapping and emission is very important properties which should be studied in detail. The characteristic time τ_{it} with which a trapped charge in a semiconductor is emitted from a trapping state of energy E_t can be determined from standard Fermi–Dirac statistics and is given by

$$\tau_{it} = \frac{1}{v_{th}\sigma N}\exp\left(\frac{\Delta E}{kT}\right) \quad (2.13)$$

where ΔE is the energy difference between the majority carrier band-edge energy and the trapping state energy E_t, k is the Boltzmann constant, T is the semiconductor temperature, σ is the capture cross-section of the trapping state, v_{th} is the thermal velocity of the majority charge carriers, and N is the density of states in the majority carrier band. The capture cross-section σ can vary from 10^{-12} to 10^{-20} cm^2. Nevertheless, the largest majority of trapping states has capture cross-sections of the order of 10^{-14}-10^{-15} cm^2 [13, 14]. From this characteristic emission time τ_{it}, one can directly derive the characteristic response frequency $f = 1/2\pi\tau_{it}$ of the corresponding trapping state, knowing the depth of the trapping state in the bandgap.

The conductance technique is based on measuring the equivalent parallel conductance G_p of an MOSCAP as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

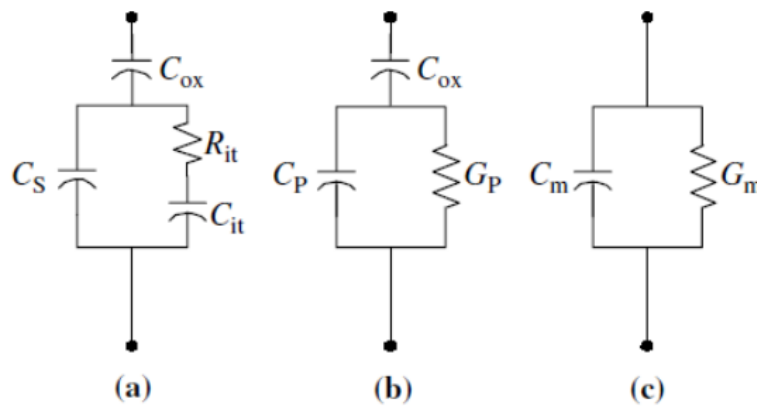


Figure 2.19. Equivalent circuits for conductance measurements: (a) MOSCAP with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit, (d) including series r_s resistance and tunnel conductance G_t

Figure 2.19a presents the equivalent circuit of an MOSCAP which is appropriate for the conductance method [12]. This circuit consists of oxide capacitance C_{ox}, semiconductor capacitance C_s, and the interface trap capacitance C_{it}. The resistance R_{it} presents an energy loss due to the capture and emission of carriers by interface traps. Conveniently, the circuit in Fig. 2.19(a) is replaced by that of Fig. 2.19(b), where C_p and G_p can be expressed as

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \tag{2.14a}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \tag{2.14b}$$

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ (f is measurement frequency) and $\tau_{it} = R_{it}C_{it}$ is the interface trap time constant, given by equation (2.12).

The conductance is measured as a function of frequency and plotted as G_p/ω versus ω. From equation (2.14b), G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$. Equations (2.14a) and (2.14b) are for interface traps with a single energy in the bandgap. Interface traps at the oxide/semiconductor interface, however, are continuously distributed in energy throughout the semiconductor bandgap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level. In this case, an approximate expression giving the interface trap density in terms of the measured maximum conductance is [12]

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \tag{2.15}$$

Capacitance meters generally assume the device to consist of the parallel C_m-G_m combination in Fig. 2.19(c). A circuit comparison of Fig. 2.19(b) to 2.19(c) gives G_p/ω in terms of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}}{G_m^2 + \omega^2(C_{ox} - C_m)^2} \tag{2.16}$$

Figure 2.20 shows the dependent of measured G_p/ω versus measured frequency of an $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP as an example. From the peak of curve, the value of D_{it} can be extracted according to the equation (2.15). From the value of frequency f_{max} =

$1/2\pi\tau_{it}$ at that G_p/ω is maximum, the position of trap level can be estimated by using equation (2.12).

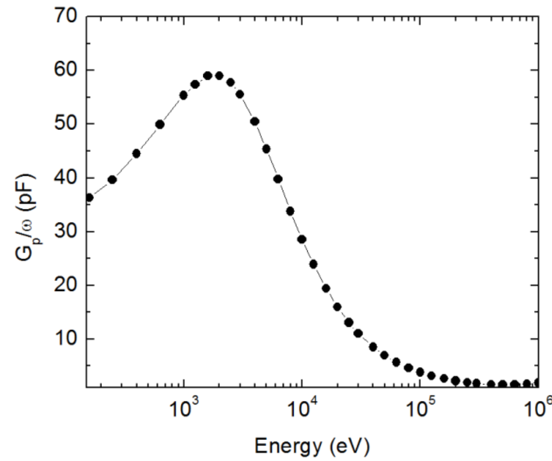


Figure 2. 20. G_p/ω versus frequency of an $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP device

Determining the maximum of G_p/ω as a function of frequency for different bias voltages, for which the device is in depletion, will provide us with a measure of the interface state density as a function of the position in the bandgap. The linear relationship between D_{it} and G_p/ω holds only for interface state densities for which $G_p/\omega < C_{ox}$. For interface state densities where G_p/ω approaches C_{ox}, the value indicated by $G_p/\omega q$ is only a lower bound of the true D_{it} [15].

In order to get a continuous picture of the movement of surface potential and the interface distribution, the conductance contour or conductance map method was developed by G. Brammertz et al. [13]. This method is essentially a plot of G_p/ω contours as a function of measured frequency and bias voltage for MOSCAP samples. The frequency for which the maximum in the conductance data for every gate bias occurs corresponds to the characteristic frequency of the trapping states at the energy position in the vicinity of the surface Fermi level position at that precise gate bias. Therefore, following the maxima in the conductance map visualizes how the surface Fermi level moves over the energy gap as the gate bias is varied [14]. Figure 2.21 show the dependent of G_p/ω on the frequencies at different gate bias and the corresponding G_p/ω contour of an Al_2O_3/GaAs MOSCAP device as an example. Clearly, the conductance map shows the conductance data in a more efficient and intuitive way, as it allows visualizing the movement of the surface Fermi level as the gate bias is varied [13].

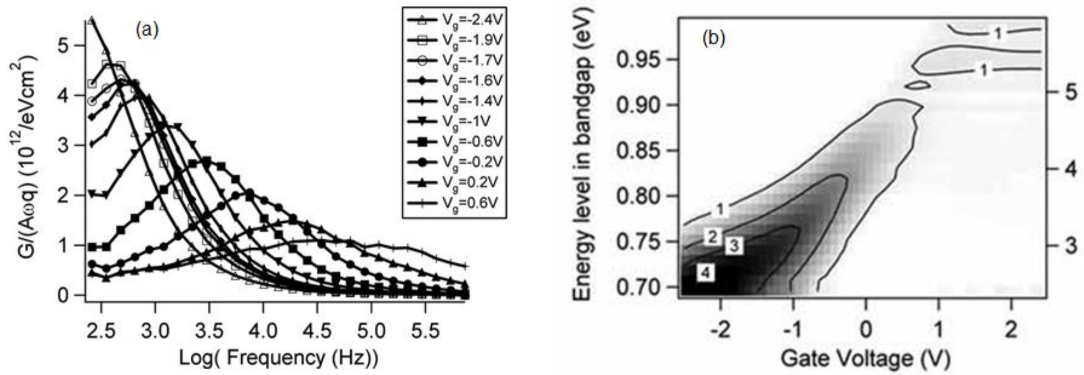


Figure 2.21. a-G/Aωq as a function of frequency at different gate bias voltages, A is area of MOSCAP; b- G/Aωq contours as a function of both frequency and gate voltage, a more efficient and intuitive way to visualize the movement of Fermi level [13].

Figure 2.22 shows the relationship between response frequency $f = 1/2\pi\tau_{it}$ and corresponding trapping state energy level which derives from equation (2.13), for the case of n-$In_{0.53}Ga_{0.47}As$. The value capture cross-section is $\sigma = 10^{-14}$ cm^2 and other parameters of InGaAs in eq. (2.13) are from ref. [16]. Due to the limited of typical measured frequency range, 100 Hz - 1 MHz, the measurement at room temperature can only extract the interface trapping state lying at 0.25 - 0.49 eV above $In_{0.53}Ga_{0.47}As$ band edge (Fig. 2. 22). To extend the energy range of interface trapping states determination, C-V and G-V measurements need to perform at different temperature. In the InGaAs case, lower temperature measurements are needed as shown in Fig. 2.22. This allows us to extract the interface trapping states lying near the InGaAs conduction band.

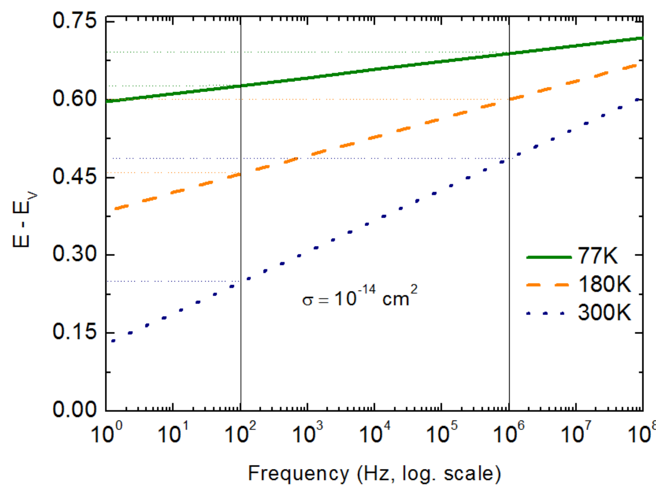


Figure 2.22. Characteristic trapping frequencies for electron in n-$In_{0.53}Ga_{0.47}As$ at different temperatures.

References

[1] T. Suntola and J. Antson, US Patent 4 058 430 (1977).

[2] M. Houssa, *Editor*, "High-k Gate Dielectrics," IOP Publishing Ltd, ISBN 0 7503 0906 7, 17-22 (2004).

[3] Marco Fanciulli, and Giovanna Scarel, *Editors*, "Rare Earth Oxide Thin Films," Springer, ISBN-10 3-540-35796-3, 15-17 (2007).

[4] Source: http://www.cambridgenanotech.com/

[5] H.R. Huff, and D.C. Gilmer, *Editors*, "High Dielectric Constant Materials, VLSI MOSFET Applications," Springer, ISBN 3-540-21081-4, 379-391 (2005).

[6] D. R. Vij, *Editor*, "Handbook of Applied Solid State Spectroscopy," Springer, ISBN-13: 978-0387-32497-5, 486-507 (2006).

[7] J. C. Vickerman, and Ian. S. Gilmore, *Editors*, "Surface analysis: the principal techniques," John Wiley and Sons Ltd, ISBN 978-0-470-01763-0, 47-109 (2009).

[8] Source: http://www.almaden.ibm.com/st/scientific_services/materials_analysis/xps/.

[9] Source: http://www.uksaf.org/software.html

[10] Source: http://www.unl.edu/CMRAcfem/."

[11] Source: http://cp.literature.agilent.com/litweb/pdf/5988-1025EN.pdf.

[12] D. K. Schroder, "Semiconductor Material and Device Characterization," John Wiley and Sons, Inc., ISBN-13: 978-0-471-73906-7,321-323 (2006).

[13] G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, "Capacitance--Voltage Characterization of GaAs--Oxide Interfaces," J. Electrochem. Soc. **155**, H945-H950 (2008).

[14] G. Brammertz, H.-C. Lin, K. Martens, D. Mercier, S. Sioncke, A. Delabie, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, "Capacitance-voltage characterization of GaAs-Al_2O_3 interfaces," Appl. Phys.Lett. **93**, 183504 (2008).

[15] Koen Martens, Chi On Chui, Guy Brammertz, Brice De Jaeger, Duygu Kuzum, Marc Meuris, Marc M. Heyns, Tejas Krishnamohan, Krishna Saraswat, Herman E. Maes, and Guido Groeseneken, "On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates," IEEE Trans. Electron Devices **55**, 547-556, (2008).

[16] Source: http://www.ioffe.ru/SVA/NSM/

Chapter 3

EFFECTS OF WET CHEMICAL AND TMA TREATMENTS ON THE INTERFACE PROPERTIES IN ALD OF AL_2O_3 ON INAS

In this chapter, the reduction of native oxides on an InAs surface using various wet and dry chemical treatments, including hydrochloric acid (HCl) treatment, sulfide treatment, and in situ trimethyl aluminum (TMA) treatment before the atomic layer deposition (ALD) of Al_2O_3 on InAs are studied. X-ray photoelectron spectrum (XPS) results show that the effect of surface cleaning by TMA was apparent almost after the first pulse but that TMA cleaning is not as effective as wet chemical surface cleaning. The combination of wet chemical treatment and TMA pretreatment is the most effective method for InAs surface cleaning, as indicated by the XPS analysis. Capacitance - voltage (C-V) and current density - voltage (J-V) characteristics on metal-oxide-semiconductor capacitance (MOSCAP) structures were also investigated to evaluate the Al_2O_3/n-InAs interface quality after different surface treatments, and the results are consistent with the XPS analysis.

3.1. Introduction

In the continuous downscaling of complementary metal-oxide-semiconductor (CMOS) technology, the III-V metal-oxide-semiconductor transistor (MOSFET) with high-k dielectric materials is one of the best candidates for the 22 nm generation of CMOS technology and beyond [1, 2]. However, the poor gate oxide /III-V interface quality has delayed the development of III-V MOSFETs. Much effort has been focused on reducing the native oxide effect on the III-V surface such as by depositing Si, Ge, and Si-Ge interfacial passivation layers [3-5], ammonium sulfide passivation before oxide deposition, and hydroxylation of the surface [6]. Recently, the "self-cleaning" of the interfacial oxide by trimethyl aluminum (TMA) precursor was proposed for the atomic layer deposition (ALD) of oxide films on III-V compounds such as GaAs [7-9], InGaAs [10, 11], and InSb [12, 13]. Although there are some reports on the MOS properties of ALD high-k dielectric materials on InAs [14-17], the effect of the ALD precursor on the reduction of native oxides on the InAs surface has not been sufficiently studied. In this work, the effect of wet chemical treatment compared with TMA pretreatment is studied. We also investigate in detail the effect of TMA pretreatment in conjunction with chemical treatment on the reduction of InAs surface oxides

3.2. Experiment

The samples used in this study were a molecular beam epitaxy grown n-InAs/$In_{0.7}Ga_{0.3}As$/$In_{0.53}Ga_{0.47}As$ (2-5x10^{17} /cm^3 doping) structure on n-InP wafers. After degreasing in acetone and iso-propanol, the native-oxide-covered samples were loaded into an ALD chamber. In situ TMA pretreatments was done by using 1, 5, and 10 cycles of TMA/N_2 (half ALD cycles) with a duration of 0.2 s for a TMA pulse and 5 s for a N_2 pulse. After that, Al_2O_3 films (TMA/N_2/H_2O/N_2 with periods of 0.2 s/5 s/0.2 s/5 s) were deposited over 20 growth cycles. The thickness of the Al_2O_3 film estimated from the number of growth cycles, is about 2 nm. High-purity N_2 was used as a purging gas and the wafers were kept at a temperature of 200°C during both pretreatment and deposition processes. In addition, two kinds of chemical surface treatments, i.e., HCl treatment and sulfide $(NH_4)_2S$ treatment were also carried out before 10 cycles of TMA pretreatment and ALD Al_2O_3 deposition. The HCl treatment was performed for 1min using HCl : H_2O (1 : 10) solution followed by rinsing in water for 1 min and blowing dry by N_2 gas. For $(NH_4)_2S$ treatment, the samples went through HCl treatment first, followed by 20 min in

$(NH_4)_2S$: H_2O (1 : 3) solution; after that, the samples were rinsed for 1 min in water and blown dry by N_2 gas. X-ray photoelectron spectrum (XPS) measurements were performed in a commercial Microlab 350 XPS system equipped with an Al Kα source in an ultra-high-vacuum chamber (~10^{-9} Torr) with a 60° take-off angle.

The MOS capacitance (MOSCAP) structures were fabricated on untreated, HCl-treated, and sulfide-treated samples with 10 half cycles of TMA pretreatment followed by 10nm ALD Al_2O_3 deposition at 200 ^oC. Postdeposition annealing (PDA) was performed at 400 ^oC for 30 s in N_2. After that, Ti/Pt/Au gate metal and Au/Ge/Ni/Au back side ohmic metal were deposited, followed by postmetal annealing (PMA) at 400 ^oC for 30 s in N_2. The capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured using an HP4284A LCR meter and a Keithley 4200 semiconductor analyzer system, respectively.

3.3. Results and discussion

3.3.1. Effect of TMA treatment

First of all, the effect of TMA treatment on InAs was investigated. Figure 3.1 illustrates the As $3d_{3/2, 5/2}$ and In $3d_{5/2}$ spectra of a bare native-oxide-covered sample without surface treatment (Fig. 3.1a) and the samples after different cycles of TMA pretreatments with subsequent ~2 nm ALD Al_2O_3 depositions (Figs. 3.1b – 3.1d). These spectra were fitted using the XPSPEAK software package (version 4.1) with a Gaussian - Lorentzian (GL) line shape. The features of As 3d spectra include peaks corresponding to As-In, and As-As bonds and the two native oxides of As_2O_3 and As_2O_5. The main doublet peak at ~ 40.3 eV corresponds to the As-In substrate bonding, taking into account the splitting with a spacing of 0.7 eV [18]. Since the As-As peak's position shifts to 1.0 eV higher, the two other peaks, which shift to 3.4 eV and 4.7 eV higher are assigned to As^{3+}-O and As^{5+}-O bonds, respectively [19]. The In $3d_{5/2}$ spectra show In-As bonding at the position of ~ 444.4 eV, meanwhile the In-O bond shifts to 0.8 eV higher [19].

The decrease of the intensity of As-O and In-O bonds in spectra b, c, and d compared with that in Fig. 3.1a reveals that native oxides were reduced by the TMA pretreatment. The reduction of native oxides was due to ligand-exchange reactions of TMA with native oxides, as proposed in previous reports on GaAs and InSb materials [8, 9, 12, 13]. When purging into ALD chamber, TMA reacts with the native oxides, i.e., In_2O_3, As_2O_3, and

As_2O_5. As shown in Fig. 3.1, the As^o bonds did not change significantly and In^o bonds were not detectable while employing TMA pretreatment. Thus, the products of reactions were expected to be volatile compounds of $In(CH_3)_3$, $As(CH_3)_3$ and $As(CH_3)_5$ rather than elemental arsenic and indium, as indicated by the following hypothetical reactions:

$$2Al(CH_3)_3 + As_2O_3 \rightarrow Al_2O_3 + 2As(CH_3)_3\uparrow \quad (3.1)$$

$$10Al(CH_3)_3 + 3As_2O_5 \rightarrow Al_2O_3 + 6As(CH_3)_5\uparrow \quad (3.2)$$

$$2Al(CH_3)_3 + In_2O_3 \rightarrow Al_2O_3 + 2In(CH_3)_3\uparrow \quad (3.3)$$

Very similar reactions between TMA and InSb native oxides were proposed by Hou et al., [13]. The production of Al_2O_3 in reactions between TMA and GaAs native oxides was also observed by Milojevic et al., [9]. The volatile products would be carried away by N_2 purging.

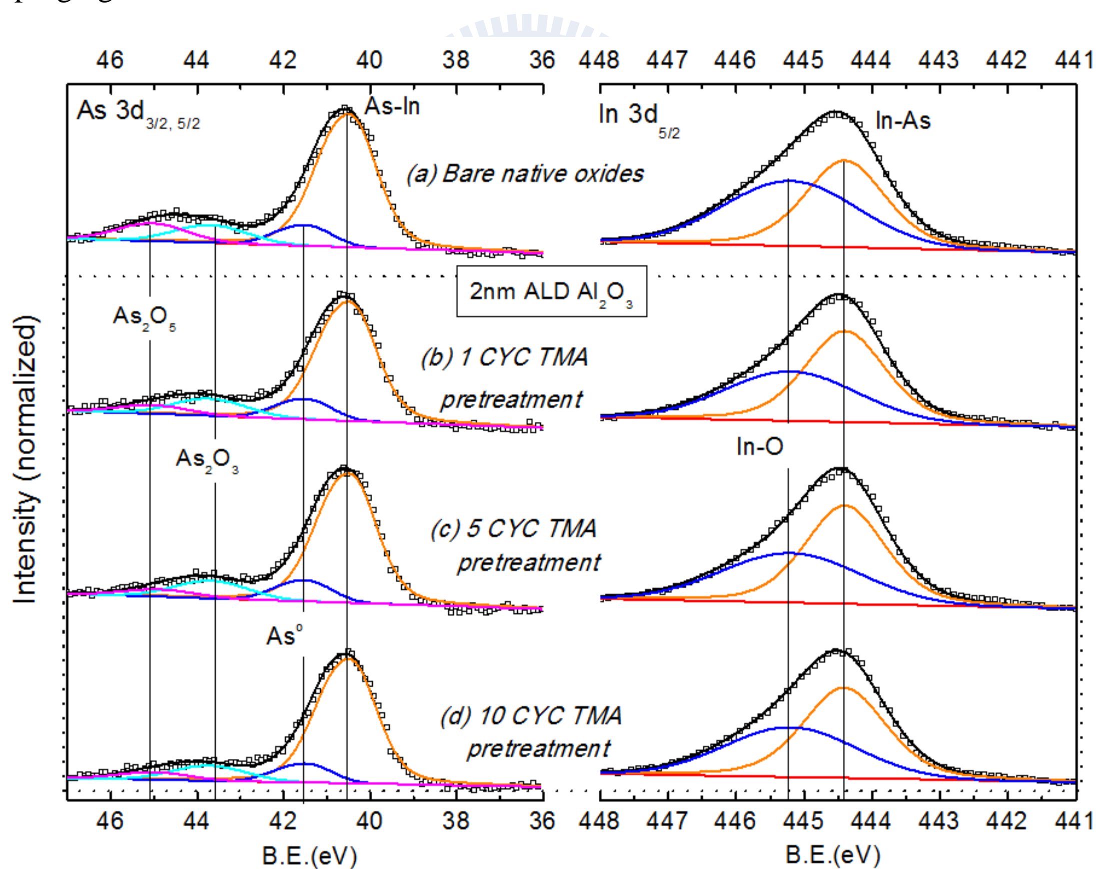


Figure 3.1. XPS spectra of As 3d and In $3d_{5/2}$ InAs samples: a-bare chip without surface treatment and after 1, 5, 10 cycles of in situ TMA pretreatment (b-d), followed by 20 cycles (~2 nm) of ALD Al_2O_3 deposition.

TMA cleaning became less effective after the first TMA exposure pulse, as indicated by the very similar As $3d_{3/2, 5/2}$ and In $3d_{5/2}$ XPS spectra of samples with 1, 5, and 10 cycles of TMA (Figs. 3.1b - 1d). After the first TMA pulse, a layer of Al_2O_3 was formed on top of the sample and prevented the further reaction between TMA and native oxides. The result implies that even if as many as 100 cycles of TMA pulses were employed [13], the effect of TMA on surface cleaning would be similar to that of 1 cycle of TMA pulses. It has been proposed that the reduction of trivalent oxides of arsenic and gallium by TMA is more significant than the reduction of other oxides [8, 9]. This seems contradictory to our experiment in which the reduction of As_2O_5 is more significant than that of As_2O_3 as shown in Fig. 3.1. This can be explained by considering that the distribution of As_2O_5 is concentrated at the top of the native-oxide-covered InAs. This phenomenon was also observed in thermal and UV treatments of GaAs and InAs using XPS angular-resolved measurements [20].

3.3.2. A combination of wet chemical treatments and TMA pretreatment

Figure 3.2 shows the As $3d_{3/2, 5/2}$ and In $3d_{5/2}$ XPS spectra of the InAs surface after different wet chemical treatments (Figs. 3.2a and 2b) and after wet chemical treatments followed by 10 cycles of TMA pretreatment and ~ 2 nm Al_2O_3 deposition (Figs. 3.2c and 3.2d). The $(NH_4)_2S$-treated surface shows the same chemical species as the HCl-treated surface but with an additional peak in the As 3d spectrum at ~1.6 eV above the As-bulk peak, which is assigned to As-S bonds [19]. The peak separation between In-O and In-S is very small (~0.1 to 0.2 eV) [19], thus, it is difficult to differentiate these two bonds from the In $3d_{5/2}$ spectrum.

As shown in Fig. 3.2a and 2b, the reduction of As_2O_5 bonding to below the detection level of XPS was observed after both kinds of surface treatments. Moreover, the As_2O_3 oxide signal could not be detected in the sulfide-treated sample and was significantly reduced in the HCl-treated sample. From these results, it is clearly seen that the As-related oxides were effectively reduced when subjected to chemical surface treatment compared with samples with pure TMA pretreatment only. Although the reduction of In-O (S) bonds was not as effective as that of As-O bonds in both chemical surface treatments, these bonds decreased in number by approximately 40% compared with those by the TMA pretreatment.

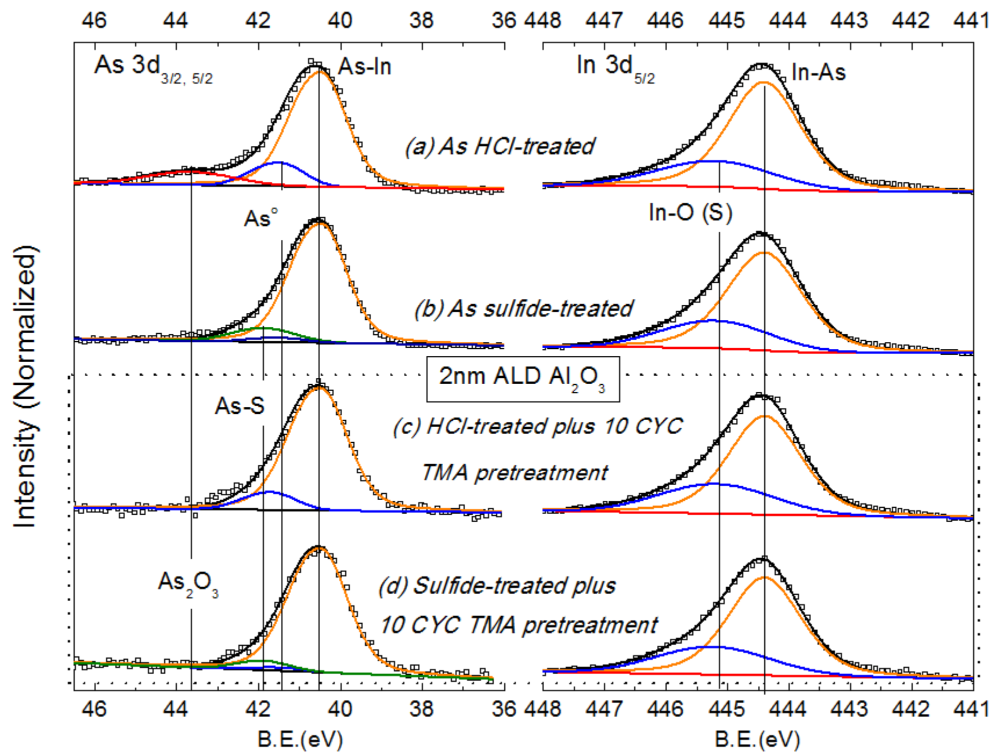


Figure 3.2 XPS As 3d and In $3d_{5/2}$ spectra of InAs samples after a-HCl and b-$(NH_4)_2S$ treatments and the wet-chemical-treated samples after 10 cycles of TMA pretreatment followed by 20 cycles of ALD Al_2O_3 (c and d).

Figures 3.2c and 3.2d show the As $3d_{3/2,\ 5/2}$ and In $3d_{5/2}$ spectra of the wet-chemical-treated samples following 10 cycles of TMA treatment and 2nm ALD Al_2O_3 deposition. The residual As_2O_3 after HCl treatment was removed by the TMA pretreatment as shown in Fig. 3.2c. In the sulfide-treated sample, after the TMA pretreatment, the As-S bonding was also reduced as indicated in Fig. 3.2d. The results imply that the combination of chemical treatments and TMA pretreatment may be an effective way to remove native oxides.

Figure 3.3 shows the multiple-frequency C-V characteristics of the MOSCAP structures as well as the corresponding bidirectional C-V responses at a frequency of 1 MHz. The frequency dispersion in the accumulation and depletion regions is relatively low for all samples, i.e., < 2.3% per decade in accumulation. Moreover, the C-V hysteresis near the flat band voltage was also small (≤ 100 mV) as shown in Fig. 3.3. This indicates a low D_{it} within the upper half of the InAs band gap. In the inversion region, a “low-frequency” C-V response is observed at a frequency of as high as 1 MHz for all samples (Fig. 3.3).

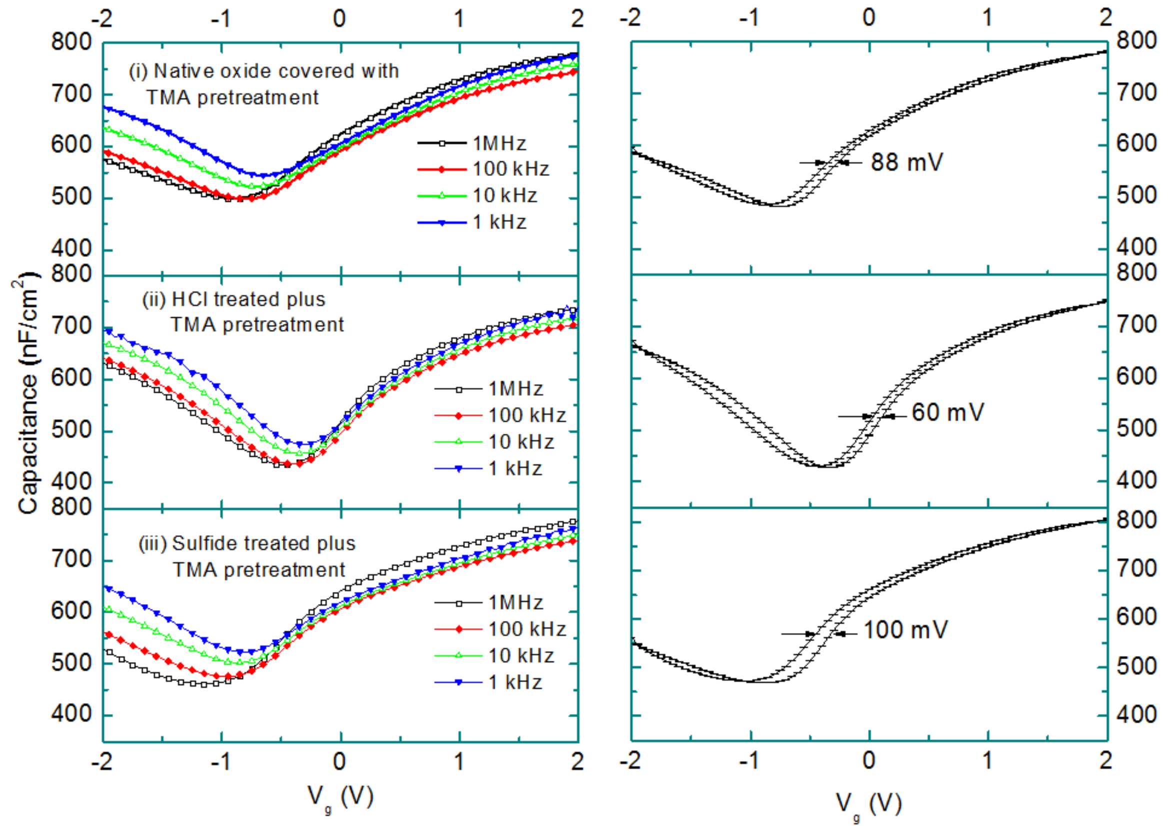


Figure 3.3. Multiple frequency C-V responses and bidirectional curves at frequency of 1 MHz for 10nm ALD Al_2O_3/n-InAs MOSCAP structures: a-Pure TMA pretreatment, b-HCl treatment plus TMA pretreatment, c-sulfide treatment plus sulfide pretreatment. The frequency dispersions per decade are 2.3, 1.8, and 2.3% for samples in sequence a to c, respectively.

Although InAs has a narrow band gap with a short minority response time, the low-frequency C-V behavior at a high frequency is not necessarily only due to a field-controlled inversion. It also has a contribution from interface trap charge states at the lower part of the InAs band gap [21]. While the C-V measurement in the accumulation region shown here cannot be used to estimate the contribution of these two phenomena, there are some indicators to compare the interface quality of the samples as follows.

In depletion region, the C-V responses of the samples with different surface treatments at a frequency of 1 MHz are shown in Fig. 3.4a. The contribution of interface trap density to the depletion capacitance can be estimated using the following equation [22]

$$C_{dep} = \left(\frac{1}{C_{ox}} + \frac{1}{C_b + C_{it}} \right)^{-1} \quad (3.4)$$

where C_{ox} is the oxide capacitance, C_b is the space-charge region capacitance, and C_{it} is

the interface trap capacitance.

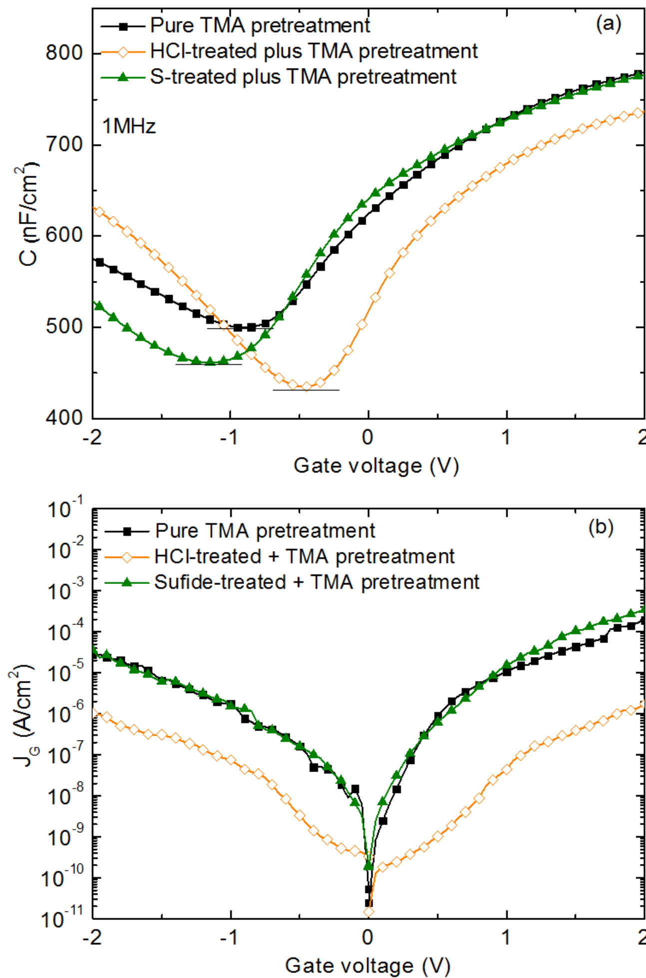


Figure 3.4. a- C-V responses at frequency of 1 MHz for samples with different surface treatments. b- Leakage current density versus gate voltage (J-V) of the same samples.

The pure-TMA-pretreated sample and the sulfide-plus-TMA-treated sample showed very similar values of C_{ox} (Fig. 3.4a). Moreover, the calculated differences between the applied voltage in the depletion region and the flat band voltage ($V_{app,\ dep}$-V_{flat}) of these two samples were also similar (around 0.65 V), i.e., they had similar values of surface potential and C_b [23]. Thus, a higher value of C_{dep} in the pure-TMA-pretreated sample implies a higher value of C_{it} compared with the sulfide-plus-TMA-treated sample. This is consistent with the XPS results, which indicate that significant amounts of As-related oxides and In-related oxides still remained after TMA pretreatment. Comparing the two samples with wet chemical treatment before TMA pretreatment, the HCl-treated sample seems to exhibit better electrical properties with smaller hysteresis (60 mV compared to 100 mV), a smaller stretch-out, and a smaller frequency dispersion in the inversion region,

as shown in Figure 3.3 and Fig. 3.4a. The J_g-V curves of samples are shown in Fig. 3.4b. The leakage current density in the HCl-treated sample is the smallest ($\leq 2x10^{-6}$ $A.cm^{-2}$) and is two orders lower than that of the other samples ($\leq 2x10^{-4}$ $A.cm^{-2}$) within ±2 V gate bias range. The leakage current is affected by interface-trap-assisted tunneling and/or interface-induced conductance band offset lowering between the high-k and III-V compounds [24]. A lower leakage current implies a smaller effect of interface trap. This indicates that a better Al_2O_3 /InAs interface quality was achieved by HCl treatment plus TMA pretreatment. The interface trap densities near the middle of the gap are about $4x10^{12}$, $2x10^{12}$, and $2.5x10^{12}$ $eV.cm^{-2}$ for the pure-TMA-treated, HCl-plus-TMA-treated and sulfide-plus-TMA-treated samples, respectively, as determined by Hill's method [25].

3.4. Conclusions

TMA treatment for the reduction of native oxides was not as effective as wet chemical surface cleaning process and most of the effect of the TMA cleaning process resulted from the first TMA pulse. The combination of either HCl treatment or sulfide treatment with TMA pretreatment gives better Al_2O_3/InAs interfacial quality than pure TMA pretreatment alone, as indicated by XPS as well as C-V and J-V electrical measurement results. Furthermore, surface cleaning by HCl treatment plus TMA pretreatment was more effective than by sulfide treatment plus TMA pretreatment.

References

[1] R. Chau, S. Datta, and A. majumdar, "Opportunities and Challenges of III-V Nanoelectronic for High-speed, Low-power Logic Applications," IEEE CSIC Syposium Technical Digest **17** (2005).

[2] P. D. Ye, "Beyond Silicon's Elemental Logic," IEEE Spectrum **45**, 42-47 (2008).

[3] H.-S. Kim, I. Ok, M. Zhang, C. Choi, T. Lee, F. Zhu, G. Thareja, L. Yu, and J. C. Lee, "Ultrathin HfO_2 (equivalent oxide thickness = 1.1 nm) metal-oxide-semiconductor capacitors on n-GaAs substrate with germanium passivation," Appl. Phys. Lett. **88**, 252906 (2006).

[4] H.-S. Kim, I. Ok, M. Zhang, T. Lee, F. Zhu, L. Yu, and J. C. Lee, "Metal gate-HfO_2 metal-oxide-semiconductor capacitors on n-GaAs substrate with silicon/germanium interfacial passivation layers," Appl. Phys. Lett. **89**, 222903 (2006).

[5] S. Koveshnikov, W. Tsai, I. Ok, J. C. Lee, V. Torkanov, M. Yakimov, and S. Oktyabrsky, "Metal-oxide-semiconductor capacitors on GaAs with high-k gate oxide and amorphous silicon interface passivation layer," Appl. Phys. Lett. **88**, 022106 (2006).

[6] D. Shahrjerdi, E. Tutuc, and S. K. Banerjee, "Impact of surface chemical treatment on capacitance-voltage characteristics of GaAs metal-oxide-semiconductor capacitors with Al_2O_3 gate dielectric," Appl. Phys. Lett. **91**, 063501 (2007).

[7] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, "HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," Appl. Phys. Lett. **86**, 152904 (2005).

[8] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," Appl. Phys. Lett. **92**, 071901 (2008).

[9] M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, H. C. Kim, E. M. Vogel, J. Kim, and R. M. Wallace, "Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces," Appl. Phys. Lett. **93**, 252905 (2008).

[10] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, "Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3," Appl. Phys. Lett. **87**, 252104 (2005).

[11] C. H. Chang, Y. K. Chiou, Y. C. Chang, K. Y. Lee, T. D. Lin, T. B. Wu, M. Hong, and J. Kwo, "Interfacial self-cleaning in atomic layer deposition of HfO_2 gate dielectric on $In_{0.15}Ga_{0.85}As$," Appl. Phys. Lett. **89**, 242911 (2006).

[12] C. H. Hou, M. C. Chen, C. H. Chang, T. B. Wu, and C. D. Chiang, "Interfacial Cleaning Effects in Passivating InSb with Al_2O_3 by Atomic Layer Deposition," Electrochem. Solid-State. Lett. **11**, D60-D63 (2008).

[13] C. H. Hou, M. C. Chen, C. H. Chang, T. B. Wu, C. D. Chiang, and J. J. Luo, "Effects of Surface Treatments on Interfacial Self-Cleaning in Atomic Layer Deposition of Al_2O_3 on InSb," J. Electrochem. Soc. **155**, G180-G183 (2008).

[14] H.-S. Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. C. Lee, P. Majhi, N. Goel, W. Tsai, C. K. Gaspe, and M. B. Santos, "A study of metal-oxide-semiconductor capacitors on GaAs, $In_{0.53}Ga_{0.47}As$, InAs, and InSb substrates using a germanium interfacial passivation layer," Appl. Phys. Lett. **93**, 062111 (2008).

[15] N. Li, E. S. Harmon, J. Hyland, D. B. Salzman, T. P. Ma, Y. Xuan, and P. D. Ye, "Properties of InAs metal-oxide-semiconductor structures with atomic-layer-deposited Al_2O_3 Dielectric," Appl. Phys. Lett. **92**, 143507 (2008).

[16] D. Wheeler, L. E. Wernersson, L. Fröberg, C. Thelander, A. Mikkelsen, K. J. Weststrate, A. Sonnet, E. M. Vogel, and A. Seabaugh, "Deposition of HfO_2 on InAs by atomic-layer deposition," Microelectron. Eng. **86**, 1561-1563 (2009).

[17] Y.-C. Wu, E. Y. Chang, Y.-C. Lin, C.-C. Kei, M. K. Hudait, M. Radosavljevic, Y.-Y. Wong, C.-T. Chang, J.-C. Huang, and S.-H. Tang, "Study of the inversion behaviors of $Al_2O_3/In_xGa_{1-x}As$ metal-oxide-semiconductor capacitors with different In contents," Solid-State. Electron. **54**, 37-41 (2010).

[18] D. Y. Petrovykh, J. M. Sullivan, and L. J. Whitman, "Quantification of discrete oxide and sulfur layers on sulfur-passivated InAs by XPS," Surf. Interface. Anal. **37**, 989-997 (2005).

[19] L. Geelhaar, R. A. Bartynski, F. Ren, M. Schnoes, and D. N. Buckley, "Photoluminescence and x-ray photoelectron spectroscopy study of S-passivated InGaAs(001)," J. Appl. Phys. **80**, 3076-3082 (1996).

[20] G. Hollinger, R. Skheyta-Kabbani, and M. Gendry, "Oxides on GaAs and InAs surfaces: An x-ray-photoelectron-spectroscopy study of reference compounds and thin oxide layers," Phys. Rev. B **49**, 11159 (1994).

[21] K. Martens, C. Chi On, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates," IEEE Trans. Electron Devices **55**, 547-556 (2008).

[22] D. K. Schroder, "Semiconductor Material and Device Characterization," John Wiley and Sons, Inc., ISBN-13: 978-0-471-73906-7, 321-323 (2006).

[23] S. M. Sze and K. K. Ng, "Sermiconductor Devices," John Wiley and Sons, Inc., 206, (2007).

[24] V. V. Afanas'ev and A. Stesmans, "Energy band alignment at the (100)Ge/HfO_2 interface," App. Phys. Lett. **84**, 2319-2321 (2004).

[25] G. K. Dalapati, T. Yi, L. Wei-Yip, M. Hoe Keat, and C. Byung Jin, "Electrical and Interfacial Characterization of Atomic Layer Deposited High-κ Gate Dielectrics on GaAs for Advanced CMOS Devices," IEEE Trans. Electron Devices **54**, 1831-1837 (2007).

Chapter 4

ELECTRICAL CHARACTERIZATION OF Al_2O_3/N-INAS MOSCAPS WITH VARIOUS SURFACE TREATMENTS

Ex-situ sulfide and HCl wet chemical treatments in conjunction with in-situ trimethyl aluminum (TMA) pretreatment were performed before the deposition of Al_2O_3 on n-InAs surfaces. X-ray photoelectron spectroscopy analyses show a significant reduction of InAs native oxides after different treatments. Capacitance-voltage (C-V) characterization of Al_2O_3/n-InAs structures shows that the frequency dispersion in accumulation regime is small (<0.75% per decade) and does not seem to be affected significantly by the different surface treatments, whereas the latter improves depletion and inversion behaviors of the nMOS capacitors. The interface trap density profiles extracted from simulation show mainly donor-like interface states inside the InAs bandgap and in the lower part of the conduction band. The donor-like traps inside the InAs bandgap and in the lower part of the conduction band were significantly reduced by using wet chemical plus TMA treatments, in agreement with C-V characteristics.

4.1. Introduction

High electron mobility and high low-field drift velocity GaAs, InGaAs and InAs compounds have been considered as potential candidates to replace Si as a channel material for future complementary metal-oxide-semiconductor (CMOS) technology nodes. Compared to numerous studies of high k/GaAs and InGaAs structures, the study of the high k/InAs structure is still relatively unexplored [1-9]. Beside the application in the inversion mode MOS field effect transistor (MOSFET), the application of InAs as a channel for MOS high electron mobility transistor (MOSHEMT) devices is also very promising. Recent report about InAs "XOI" transistors with thermal growth $InAsO_x$ oxide had also given very significant results [10]. Among a few reports about high-k/InAs structures, studies about the reduction of InAs native oxides and simulation of narrow band gap high-k/InAs MOS capacitors (MOSCAP) have been presented recently [1-5]. Some experimental studies have been reported as well [5-8] but the influence of surface treatments on the capacitance-voltage (C-V) behavior of high k/InAs MOSCAP structure have not been investigated in details yet. In this work, we study the electrical characteristics of atomic layer deposition (ALD) Al_2O_3/n-InAs with various surface treatments, including sulfide and HCl treatment in conjunction with an *in situ* trimethyl aluminum (TMA) pretreatment [1, 11, 12]. Experimental results and C-V simulations [13] are combined to investigate the electrical properties of Al_2O_3/InAs MOSCAP structures. Effects of surface treatments on the C-V behavior in accumulation, depletion and inversion regimes are discussed.

4.2. Experiment

The wafers used in this work consist of 2 x 10^{17} cm^{-3} Si-doped n-type 5nm strained InAs - 3nm $In_{0.7}Ga_{0.3}As$ - 100nm $In_{0.53}Ga_{0.47}As$ multilayer stacks grown by molecular beam epitaxy (MBE) on n-type InP substrates, supplied by the IQE company. The nominal doping uniformity is better than 1%.The wafers were degreased in acetone and isopropanol at room temperature (RT) before surface treatments. HCl treatment was used by dipping samples in HCl (38 %) : H_2O (1 : 10) solution for 1 min followed by rinsing in deionized (DI) water. For sulfide treatment, the sample first underwent HCl treatment, and was then dipped in the $(NH_4)_2S$ (20 %) : H_2O (1 : 3) solution for 20 min followed by rinsing in DI water. After that, the control sample (native-oxide-covered InAs surface without treatment), HCl-treated sample, and sulfide-treated sample were loaded into the

ALD chamber for the same run. In ALD chamber, temperature of samples was increased and kept at 300°C. After that, ten pulses of TMA/N_2 were employed for in situ TMA self-cleaning [1, 11, 12] before the deposition of Al_2O_3. The number of ALD Al_2O_3 cycles for MOSCAPs fabrication and XPS measurement were 180 cycles (~ 18 nm) and 15 cycles (~ 1.5 nm) respectively. Samples used for MOSCAPs fabrication were annealed at 400°C in N_2 for 30 s. After that, Ti/Pt/Au gate metal and Au/Ge/Ni/Au back side ohmic contact metal were deposited, followed by annealing at 400°C in N_2 for 30 s.

4.3. Results and discussion

4.3.1. X-ray photoelectron spectroscopy

XPS analysis was performed using a commercial Microlab 350 system equipped with an Al K_α source. Fig. 4.1 shows the In $3d_{5/2}$ and As $2p_{3/2}$ XPS spectra of the InAs native-oxide-covered surface, the Al_2O_3/HCl plus TMA treated InAs interface, and the Al_2O_3/sulfide plus TMA treated InAs interface.

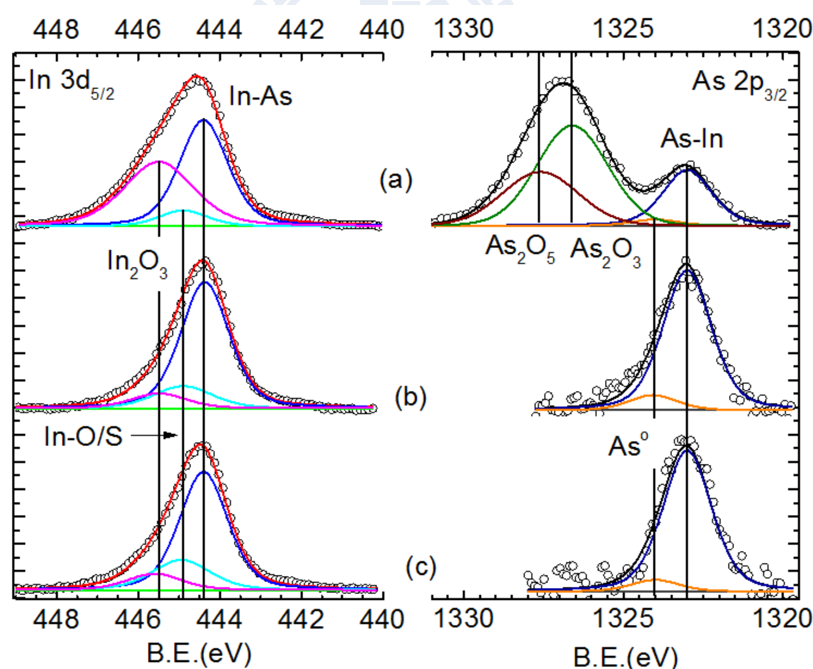


Figure 4.1. The In $3d_{5/2}$ and As $2p_{3/2}$ XPS spectra of a- native-oxide-covered InAs surface; b- 1.5 nm ALD Al_2O_3/HCl+TMA treated InAs interface; c- 1.5 nm ALD Al_2O_3/sulfide+TMA treated InAs interface. Native oxides including In_2O_3, As_2O_3, and As_2O_5 were significantly reduced after the use of surface treatments.

For both surface treatments, As-related oxides were removed to below the XPS detection level (Fig. 4.1, As $2p_{3/2}$ spectra). In $3d_{5/2}$ spectra indicate a similar effect for the

two kinds of treatments through a significant reduction of In_2O_3. In^{1+} chemical state signal seems to be slightly increased for both samples but more significantly in the sulfide plus TMA treated sample due to the contribution of In-S bonds [1].

4.3.2. Capacitance-voltage characteristics

Figure 4.2 shows the multi-frequency C-V responses and quasi-static C-V (QSCV) curves of 18 nm Al_2O_3/n-InAs MOSCAP samples. The multi-frequency C-V measurement was made using an HP4284A LCR meter, and QSCV curves were acquired using an Agilent precision 4156C analyzer. Measured leakage currents were smaller than 10^{-9} A/cm^2 in the range ± 3.5 V gate bias for all samples, ensuring they did not influence the QSCV measurements (see Fig. 4.3). In the accumulation regime, the multi-frequency responses do not show the obvious difference in frequency dispersion between samples. As shown in Figs. 4.2a - 2c, the values of frequency dispersion of samples are small, in the range of 0.65-0.75% per decade. These low frequency dispersions including the control sample indicate that surface treatments do not seem to affect significantly the C-V responses in the accumulation regime.

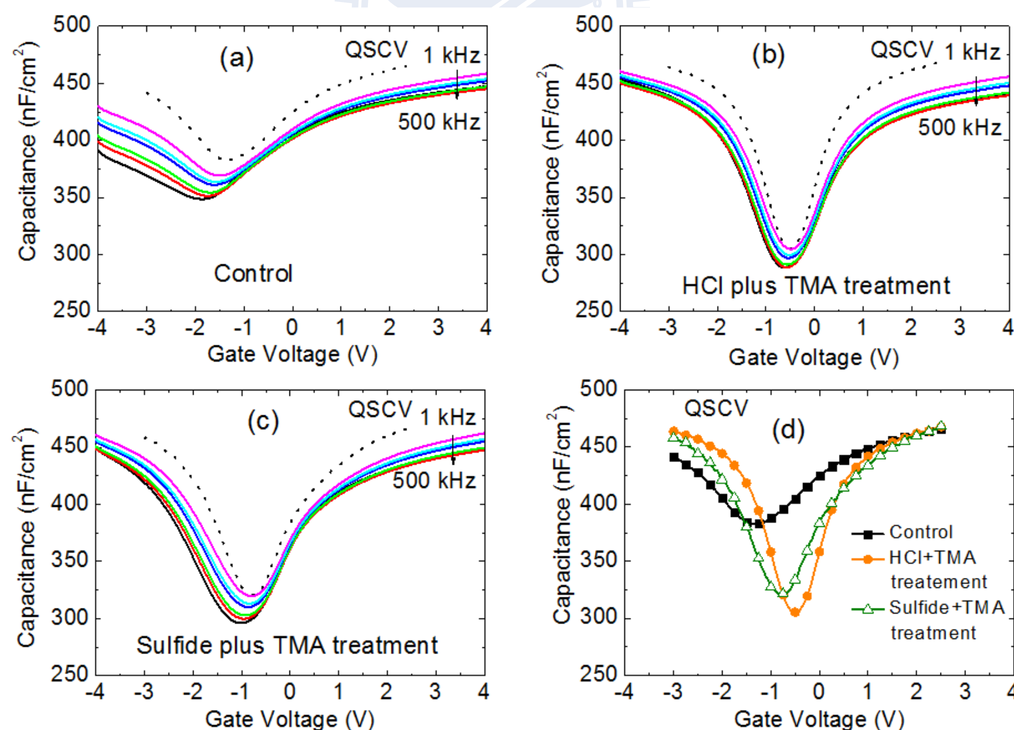


Figure 4.2. Multi-frequency C-V responses (solid lines) and QSCV curves (dashed lines) in a- control sample, b- HCl plus TMA sample, and c- sulfide plus TMA treated sample of 18 nm ALD Al2O3/InAs MOSCAPs; d- QSCV curves of all three samples, for comparison

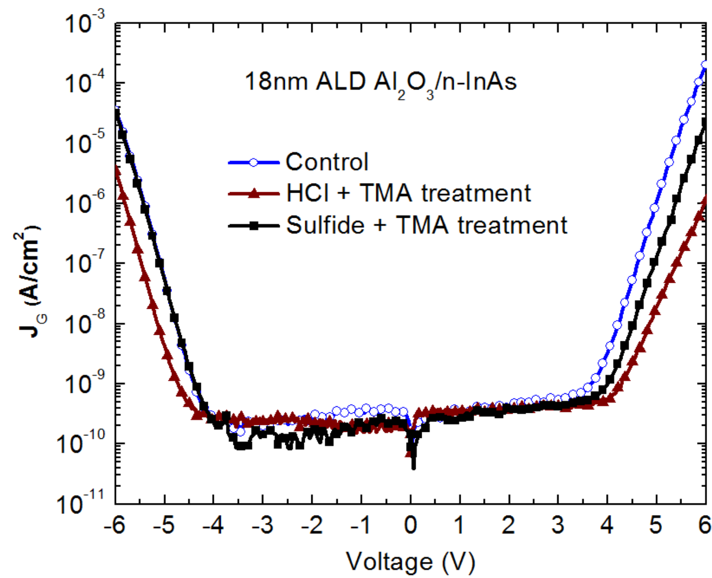


Figure 4.3. Leakage currents versus gate voltage of samples

Low frequency-like C-V behavior is observed for all samples in the whole range of measured frequencies. This behavior originates from the short minority carrier response time (τ_R) in very low band gap, high intrinsic density material as InAs. As shown in Figs. 4.2a and 2d, the control sample exhibits high value of depletion capacitance (C_{dep}) in depletion regime which reveals large value of interface trap capacitance (C_{it}). Large frequency dispersion in inversion regime in this sample as shown in Fig. 4.2a also implies high contribution of interface traps. In chemicals plus TMA treated samples, nice C-V curves with small frequency dispersion in inversion regime are observed (Figs. 4.2b - 2c). In Fig. 4.2d, smaller C_{dep} of these two samples compared to the control sample indicates that the contribution of C_{it} is reduced.

Out of the two chemical plus TMA treated samples, the HCl plus TMA sample exhibits better electrical characteristics as compared to the sulfide plus TMA treated sample, with smaller frequency dispersion in inversion regime and smaller stretch out (Figs. 4.2b-2d). This result seems contradictory to most of reports on high k/ GaAs (InGaAs) but it is consistent with the report on HfO_2/InAs structure [7]. Moreover, previous report had shown that during thermal process sulfur atoms could diffuse into InAs [14], resulting in the change of doping concentration at ultrathin InAs layer near high k/InAs interface. This change may also influence the electrical properties of the sulfide plus TMA treated sample.

4.3.3. Simulation and D_{it} profiles extraction

Low frequency CV-simulations were performed by full numerical solution of the Poisson equation:

$$\frac{d^2V(x)}{dx^2} = \frac{e[(N_d - N_a + p(x) - n(x)]}{\varepsilon_s} \quad (4.1)$$

where N_d and N_a are the donor and acceptor concentrations in the semiconductor, n(x) and p(x) are the electron and hole densities and ε_s is the dielectric constant. The model used is one-dimensional using simple finite difference discretization and Cauchy boundary conditions at the semiconductor-oxide interface. The full heterostructure of the device has been taken into account. At the InAs top surface, the charge due to interface states is taken into account as well, similar to the approach in [13]. The interface state density (D_{it}) at the InAs/high-k interface was varied, until a good fit to the experimental data was obtained. For the electron density approximation, a model using a correction for the non-parabolicity of the conduction band was used [15]:

$$n = \frac{2N_C}{\sqrt{\pi}} \int_0^{\infty} \frac{\varepsilon^{\frac{1}{2}}(1+\alpha\varepsilon)^{\frac{1}{2}}(1+2\alpha\varepsilon)}{1+\exp(\varepsilon-\phi)} d\varepsilon \quad (4.2)$$

where, $\varepsilon = (E-E_C)/kT$ is the normalized electron kinetic energy, $\phi = (E_F-E_C)/kT$ is the reduced Fermi energy, N_C is the effective density of states in the conduction band, and α is the nonparabolicity factor:

$$\alpha = \frac{1}{\varepsilon_g}\left(1 - \frac{m_e}{m_0}\right)^2 \quad (4.2)$$

here, m_e is the electron effective mass, m_0 is the free electron mass and $\varepsilon_g = (E_C-E_V)/kT$ is the normalized bandgap.

All experimental QSCV curves (symbols) were well fitted by the simulations (solid lines). D_{it} profiles of samples extracted from simulation are shown in Figs. 4.4b-4d, where the estimated error bars of the extracted D_{it} are shown as well. Errors were estimated and taken into account due to the following reasons: (i) error on metal work function, (ii) charge quantization effects which were not included in the simulation and (iii) uncertainty

on absolute value of oxide capacitance, C_{ox}. The derived D_{it} profiles present a U-shape with minimum in D_{it} profile located around the conduction band minimum (E_C) for all samples. The interface state density shows strong similarities with the $In_{0.53}Ga_{0.47}As/Al_2O_3$ D_{it} profile [13]. It can be clearly seen that the two different surface treatments significantly reduce the donor-like traps over the full energy region as compared to the control sample (Figs. 4.4b-4d). The D_{it} of the sulfide treated plus TMA sample shows slightly higher values of donor-like traps as compared to the HCl plus TMA treated sample, as expected from the general C-V characteristics of these two samples with deeper depletion of the HCl treated sample as compared to the $(NH_4)_2S$ treated sample.

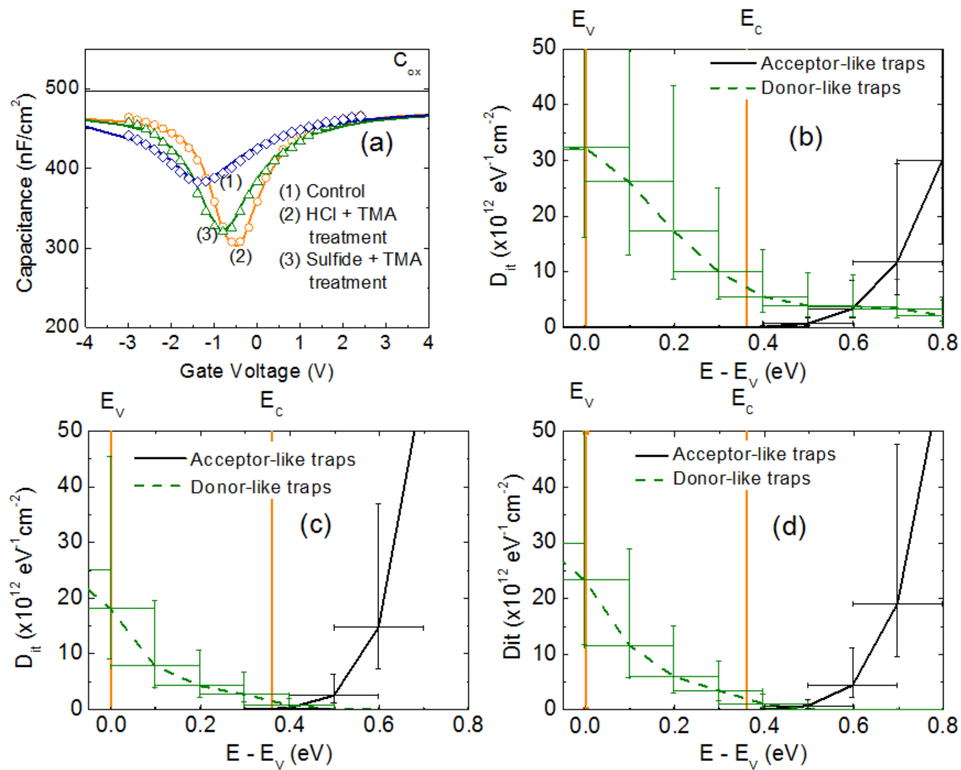


Figure 4.4. a- Experimental data (symbols), simulated C-V curves (solid lines) of ALD 18 nm Al2O3/n-InAs MOSCAP samples with various surface treatments. Interface state density profiles of all three samples, extracted from simulation, are shown as well: b- control sample, c- HCl plus TMA treated sample, d- sulfide plus TMA treated sample.

4.4. Conclusions

We have examined the effect of surface treatments on the physical and electrical properties of the Al_2O_3/n-InAs structures. The effect of interface states on accumulation

capacitance behavior is small and does not depend on the surface treatments. In contrast, the C-V characteristics of Al_2O_3/n-InAs in depletion and inversion region were significantly improved by surface treatments. The D_{it} profiles extracted from simulation shows a significant reduction of donor-like traps after surface treatments in complete InAs bandgap, as well as in the lower part of conduction band. Results also revealed that HCl plus TMA treatment has stronger effect on the reduction of donor-like traps than sulfide plus TMA treatment.

References

[1] A. P. Kirk, M. Milojevic, J. Kim, and R. M. Wallacea, "An in situ examination of atomic layer deposited alumina/InAs(100) interfaces," Appl. Phys. Lett. **96**, 202905 (2010).

[2] R. Timm, A. Fian, M. Hjort, C. Thelander, E. Lind, J. N. Andersen, L.-E. Wernersson, and A. Mikkelsen, "Reduction of native oxides on InAs by atomic layer deposited Al_2O_3 and HfO_2," Appl. Phys. Lett. **97**, 132904 (2010).

[3] Abigail Lubow, Sohrab Ismail-Beigi, and T. P. Ma, "Comparison of drive currents in metal-oxide-semiconductor field-effect transistors made of Si, Ge, GaAs, InGaAs, and InAs channels," Appl. Phys. Lett. **96**, 122105 (2010).

[4] Erik Lind, Yann-Michel Niquet, Hector Mera, and Lars-Erik Wernersson, "Accumulation capacitance of narrow band gap metal-oxide-semiconductor capacitors," Appl. Phys. Lett. **96**, 233507 (2010).

[5] Hai-Dang Trinh, Edward Yi Chang, Yuen-Yee Wong, Chih-Chieh Yu, Chia-Yuan Chang, Yueh-Chin Lin, Hong-Quan Nguyen, and Binh-Tinh Tran "Effects of Wet Chemical and Trimethyl Aluminum Treatments on the Interface Properties in Atomic Layer Deposition of Al_2O_3 on InAs," Jpn. J. Appl. Phys. **49**, 111201 (2010).

[6] Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Jack C. Lee, Prashant Majhi, N. Goel, W. Tsai, C. K. Gaspe, and M. B. Santos, "A study of metal-oxide-semiconductor capacitors on GaAs, $In_{0.53}Ga_{0.47}As$, InAs, and InSb substrates using a germanium interfacial passivation layer," Appl. Phys. Lett. **93**, 062111 (2008).

[7] D. Wheeler, L.-E. Wernersson, L. Fröberg, C. Thelander, A. Mikkelsen, K.-J. Weststrate, A. Sonnet, E.M. Vogel, and A. Seabaugh, "Deposition of HfO_2 on InAs by atomic-layer deposition," Microelectron. Eng. **86**, 1561-1563 (2009).

[8] Yun-Chi Wua, Edward Yi Chang, Yueh-Chin Lin, Chi-Chung Kei, Mantu K. Hudait, Marko Radosavljevic, Yuen-Yee Wong, Chia-Ta Chang, Jui-Chien Huang, and Shih-Hsuan Tang, "Study of the inversion behaviors of $Al_2O_3/In_xGa_{1-x}As$ metal-oxide-semiconductor capacitors with different In contents," Solid-State Electron. **54**, 37-41 (2010).

[9] Ning Li, Eric S. Harmon, James Hyland, David B. Salzman, T. P. Ma, Yi Xuan, and P. D. Ye, "Properties of InAs metal-oxide-semiconductor structures with atomic-layer-deposited Al_2O_3 Dielectric," Appl. Phys. Lett. **92**, 143507 (2008).

[10] Hyunhyub Ko, Kuniharu Takei, Rehan Kapadia, Steven Chuang, Hui Fang, Paul W. Leu, Kartik Ganapathi, Elena Plis, Ha Sul Kim, Szu-Ying Chen, Morten Madsen, Alexandra C. Ford, Yu-Lun Chueh, Sanjay Krishna, Sayeef Salahuddin, and Ali Javey, "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," Nature **468**, 286-289 (2010).

[11] M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, H. C. Kim, E. M. Vogel, J. Kim,nand R. M. Wallace, "Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces," Appl. Phys. Lett. **93**, 252905 (2008).

[12] H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, "The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor," Appl. Phys. Lett. **97**, 042903 (2010).

[13] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces," Appl. Phys. Lett. **95**, 202109 (2009).

[14] Johnny C. Ho, Alexandra C. Ford, Yu-Lun Chueh, Paul W. Leu, Onur Ergen, Kuniharu Takei, Gregory Smith, Prashant Majhi, Joseph Bennett, and Ali Javey, "Nanoscale doping of InAs via sulfur monolayers," Appl. Phys. Lett. **95**, 072108 (2009).

[15] Viktor Ariel-Altschul, Eliezer Finkman, and Gad Bahir, "Approximations for carrier density in nonparabolic semiconductors," IEEE Trans. Electron Devices **39**, 1312-1316 (1992).

Chapter 5

THE INFLUENCES OF SURFACE TREATMENT AND GAS ANNEALING CONDITIONS ON THE INVERSION BEHAVIORS OF THE ATOMIC LAYER DEPOSITION AL_2O_3/N-$IN_{0.53}GA_{0.47}AS$ MOSCAP

In this chapter, the inversion behaviors of atomic-layer-deposition (ALD) Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors are studied by various surface treatments and post deposition annealing using different gases. By using the combination of wet sulfide and dry trimethyl aluminum surface treatment along with pure hydrogen annealing, a strong inversion capacitance-voltage (C-V) response is observed, indicating a remarkable reduction of interface trap state density (D_{it}) at lower half-part of $In_{0.53}Ga_{0.47}As$ band gap. This low D_{it} was confirmed by the temperature independent C-V stretch-out and horizontal C-V curves, simulation and conductance methods. The x-ray photoelectron spectroscopy spectra (XPS) further confirm the effectiveness of hydrogen annealing on the reduction of native oxides.

5.1. Introduction

High carrier mobility III-V compound semiconductors are regarded as one of the best channel materials for the high performance low power complementary metal-oxide-semiconductor (CMOS) transistor application [1]. Among III-V compounds, the ternary alloy $In_{0.53}Ga_{0.47}As$ lattice matched to InP is one of the most attractive materials to be used due to its high low-field electron mobility and high saturation velocity [2]. Although many significant results were achieved on the fabrication of devices incorporation high dielectric constant (high k) materials on III-V channel [3, 4], the high trap state density (D_{it}) at high k/III-V compounds interface remains a main challenge. It is still too high to be implemented into upcoming technology nodes below 22nm causing threshold voltage shifts and instabilities as well as a reduction in the effective channel mobility [5].

Recently, Lin et al. reported the true inversion behavior in Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor (MOSCAPs) by using sulfide treatment and post-deposition anneal (PDA) in forming gas [6]. This implies low interface states at upper-half band gap of p-$In_{0.53}Ga_{0.47}As$. For n-type InGaAs material, a similar result has not yet been achieved. There are many reports studying on atomic layer deposited different kind of high k materials such as ZrO_2 [2, 7], Al_2O_3 [6, 8], HfO_2 [9-12], $AlLaO_3$ [13] on n-$In_{0.53}Ga_{0.47}As$ with various surface treatments. However, the results always exhibited the "bump" on capacitance-voltage (C-V) curves in inversion region, implying high interface trap states at lower-half part of band gap. In this letter, we examine the inversion behavior of C-V curves on atomic layer deposition (ALD) Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs by using the combination of ex-situ sulfide solution surface treatment and in-situ trimethyl aluminum (TMA) pretreatment. Strong inversion layer was achieved after using this treatment and H_2 gas post deposition annealing.

5.2. Experiment

The wafers used in this study were solid source molecular beam epitaxy (MBE) grown 100nm n-$In_{0.53}Ga_{0.47}As$ layer ($5 \times 10^{17}/cm^3$ doping) on n^+-InP substrates. After degreasing in acetone and iso-propanol, the native-oxide-covered sample without surface treatment (sample S1) and the sample after wet sulfide treatment were loaded into the ALD chamber. The wet sulfide treatment was performed using 1min HCl : H_2O = 1:10 solution followed by 20min $(NH_4)_2S$ (20%) : H_2O = 1:3 solution at room temperature. In the ALD chamber, in-situ TMA pretreatments had been employed by using 10 cycles of TMA/N_2

(half ALD cycles) followed by the growth of 180 cycles (~18nm) of Al_2O_3 films. High purity N_2 was used as purging gas and wafers were kept at 300°C during both pretreatment and deposition processes. After oxide deposition, sample S1 and sulfide-treated sample (sample S2) were both annealed at 500°C in N_2 gas for 10 min. Another sulfide-treated sample (sample S3) was post deposition annealed at 500°C in H_2 gas for 10 min. Ti/Pt/Au gate metal was subsequently deposited and formed by lift-off process. Finally, Au/Ge/Ni/Au back side ohmic contact was deposited and post deposition annealed at 400°C in N_2 gas for 30s.

The multifrequency capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics were measured using an HP4284A LCR meter. The quasi-static C-V (QSCV) curves were done by using an Agilent 4156C precision analyzer. The x-ray photoelectron spectroscopy (XPS) measurement was also performed to probe chemistry at the oxide/n-InGaAs interfaces. The measurement used a commercial Microlab 350 XPS system equipped with an Al Kα source.

5.3. Results and discussion

5.3.1. Capacitance-voltage characterization

For the samples with post deposition annealing in N_2 (samples S1 and S2), the C-V multi-frequency responses (1kH-1MHz) are shown in Fig. 5.1, the inset in Fig 5.1b is the corresponding conductance-voltage (G-V) curves of sample S2.

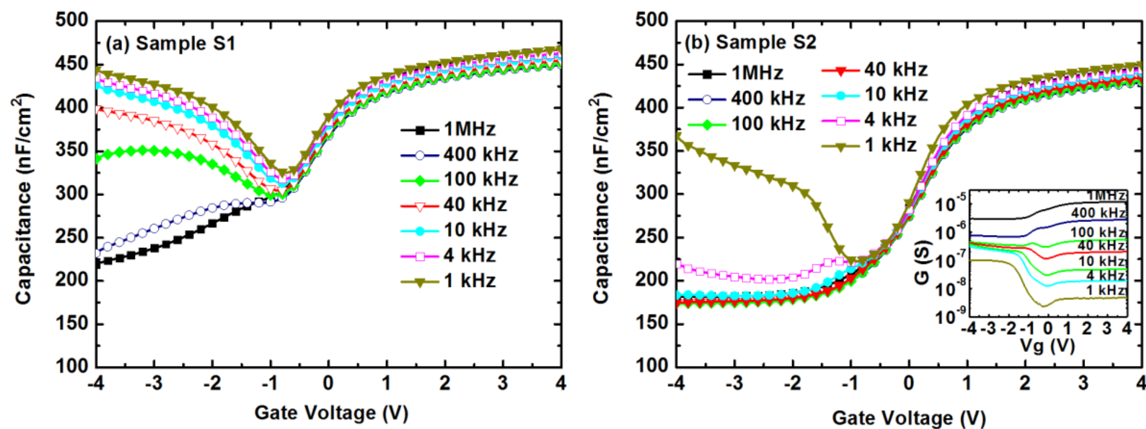


Figure 5.1. Multi-frequency C-V responses in a- TMA treated-; b- sulfide + TMA treated Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs, with post deposition annealing in N_2 gas. The inset in figure 5.1b shows the conductance - voltage (G-V) characteristics of the sample S2.

At the gate voltage ranges from -4V to -1V, sample S1 exhibits inversion bumps at high frequency and low frequency-like behavior at frequency smaller than 10 kHz as shown in Fig. 5.1a. This C-V response is similar to previous reports [9-11, 13, 14] and it is believed this behavior dominated by the high interface trapping states [9, 10, 14]. The C-V curves of sample S2 shows low frequency behavior with inversion carrier layer occurred at a frequency around 4 kHz. The observed inversion layer originates from (i) the abrupt change of C-V curves from depletion region to inversion region and (ii) the absent of the G-V peaks at frequency smaller than 10 kHz (see the inset in Fig. 5.1b). The absent of G-V peaks indicates that the contribution of interface trap loss to the conductance is virtually masked by the contribution of inversion carrier loss [15]. The appearance of the inversion layer implies the reduction of trapping states at lower half-part of the bandgap.

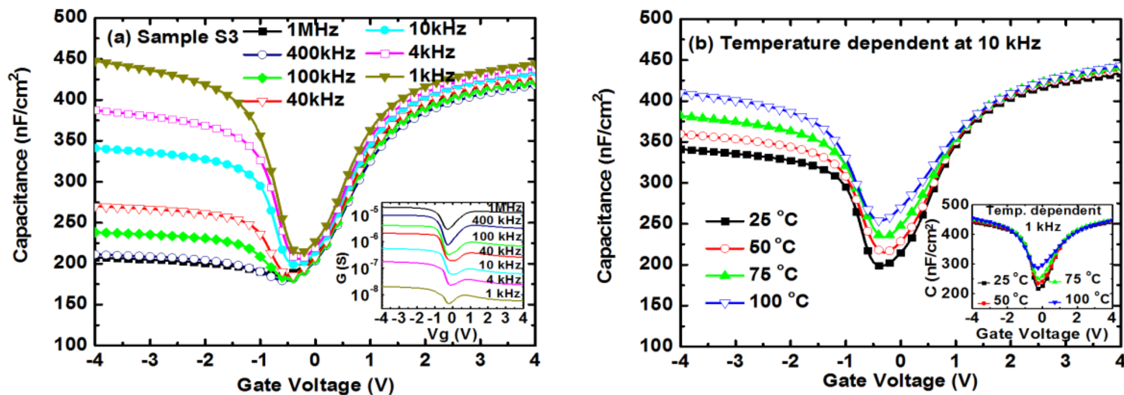


Figure 5.2. a- Multi a frequency C-V responses in sulfide + TMA treated Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs, with post deposition annealing in H_2 gas; b- The temperature dependent C-V responses at 10 kHz of the same sample. The inset in Fig. 5.2a shows the conductance-voltage (G-V) characteristics; the inset in Fig. 5.2b shows the temperature dependent C-V responses at 1 kHz.

Figure 5.2a shows the multi-frequency C-V responses of sample S3, the inset in this figure shows the corresponding G-V curves. “Low-frequency” C-V behavior with “flat”, no “bump” inversion response at frequency as high as 1 MHz indicates that the minority carriers (holes) could be generated and freely moving to form an inversion layer. This is confirmed by the absence of G-V peaks due to the inversion carrier loss as shown in the inset in Fig. 5.2a. The “free” inversion generation implies large decrease of interface trapping effect i.e. a significant reduction of interface traps density at lower half-part of InGaAs band gap. High inversion capacitance equal to oxide capacitance (C_{ox}) was obtained at frequency around 1 kHz (Fig. 5.2a), implying that at this value of frequency,

minority carriers response freely to signal and forms a fully inversion layer. This result is consistent with previous report [11], which estimated the response time,τ_R of minority carrier in n-$In_{0.53}Ga_{0.47}As$ is about 10^{-3} s.

Figure 5.2b shows the C-V characteristics measured at 10 kHz at different temperatures for sample S3. The increase of minority carrier response time, τ_R versus temperature is clearly seen as evidenced by the increase of inversion capacitance. At frequency of 1 kHz, a fully inversion layer is formed, thus, the inversion capacitance becomes independent of temperature (the inset in Fig. 5.2b). As show in Fig. 5.2b, the accumulation capacitance is almost unchanged and the C-V curves do not shift horizontally with the temperature. The inset in Fig. 5.2b shows clearly the identical C-V stretch-out at different temperatures. These characteristics further confirm the reduction of interface charge trap density.

5.3.2. X-ray photoelectron analysis

The As $2p_{3/2}$, In $3d_{5/2}$ and Ga $2p_{3/2}$ XPS spectra of the native oxide-covered InGaAs surface, the Al_2O_3/InGaAs interface as deposited and after post deposition annealing in N_2 and H_2 gases are shown in Fig. 5.3a - 5.3f, respectively. Although TMA treatment is effective in the reduction of As-O and Ga-O bonds as shown in Fig. 5.3b, the amount of native oxides is still significant. A strong surface cleaning effect was made by using sulfide treatment followed by TMA pretreatment as indicated by the decrease of the native oxides signals in Fig. 5.3c. By using TMA pretreatment, further removal of the native oxides is expected after sulfide treatment [16]. From Fig. 5.3d and Fig. 5.3e, it is clearly seen that the decrease of As_2O_3 oxide results in the increase relative signal of the Ga-related oxides after annealing in N_2. For the sample with TMA treatment only, significant amount of As_2O_3 oxide is still remaining (Fig. 5.3d). In contrast, as shown in Fig. 5.3f, by using H_2 annealing, the As_2O_3 was almost completed removed while the reduction of Ga-related oxides also occurred but with a slightly increase of Ga-O/S bonds. The In-related oxides seem to be stable after both N_2 and H_2 annealing as indicated by the very similar In $3d_{5/2}$ spectrum of the samples before and after annealing.

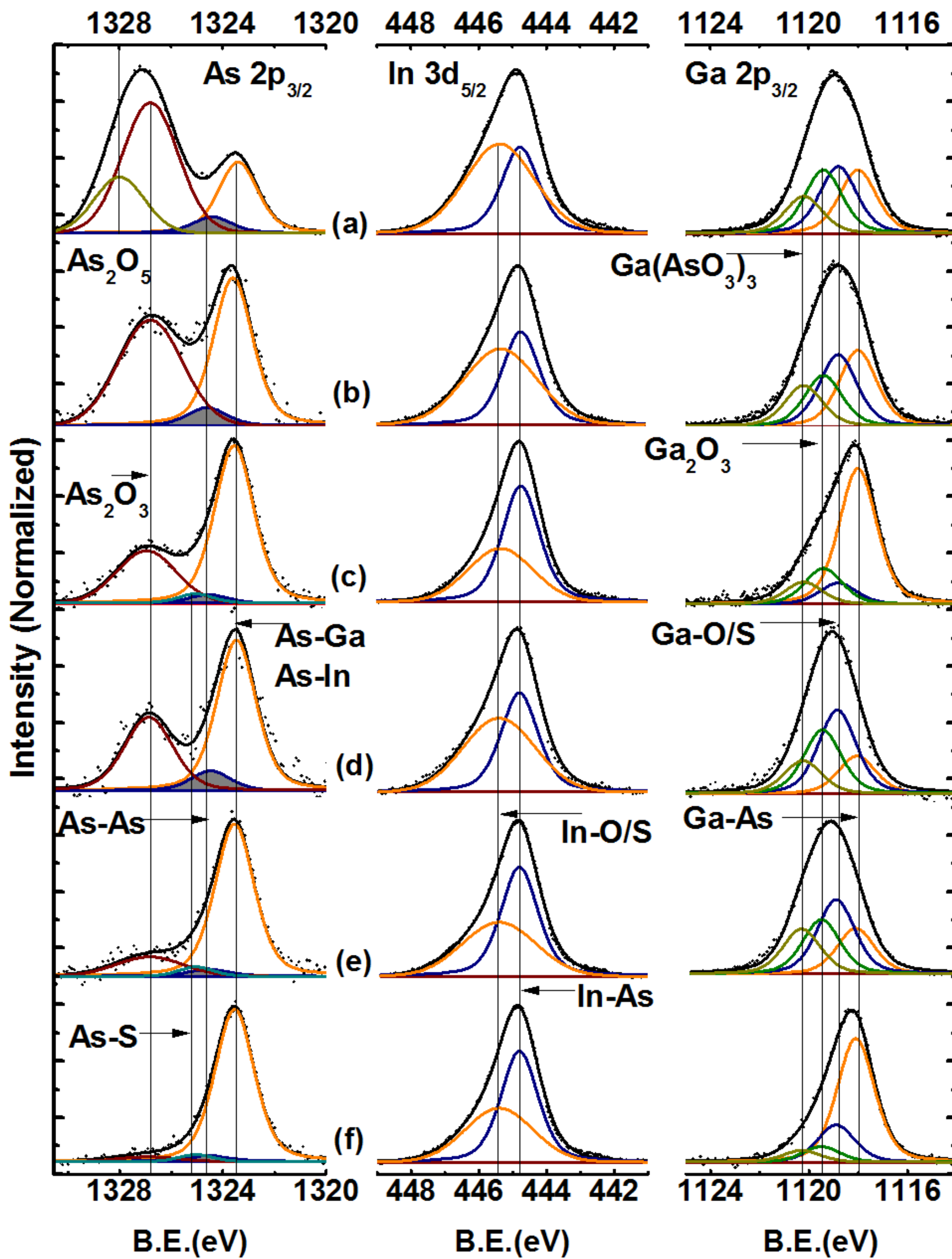


Figure 5.3. The As $2p_{3/2}$, In $3d_{5/2}$, Ga $2p_{3/2}$ XPS spectra of a- Native oxide-covered InGaAs surface; b- TMA treated sample, with ALD Al_2O_3, as deposited; c- sulfide + TMA treated sample, with ALD Al_2O_3, as deposited; d- TMA treated sample, with ALD Al_2O_3, after PDA in N_2; e- Sulfide + TMA treated sample, with ALD Al_2O_3, after PDA in N_2; f- Sulfide + TMA treated sample , with ALD Al_2O_3, after PDA in H_2.

5.3.3. D_{it} extraction by simulation and conductance methods

Figure 5.4a shows the QSCV responses of samples and the ideal C-V curves of Al_2O_3/InGaAs MOSCAP. Low leakage currents of samples were measured to ensure they did not affect the accuracy of measurement. The simulation was the same with the approach in [17] and was represented in chapter 4 for the Al_2O_3/InAs MOSCAP structure. From the figure, the simulation results of oxide/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs shows that the C-V curve of ideal device without any interface state density has an asymmetrical sharp with higher slope at negative voltage side and low minimum capacitance value, C_{min}. According to this result, the C-V characteristic of sample S3 indicates that this curve approach closest to the ideal curve as compared to either S1 or S2 (Fig. 5.4a). By comparison, the evidence of high interface state density in sample S1 exhibited by the observation of highest value of C_{min} as well as accumulation capacitance, C_{acc}.[17]

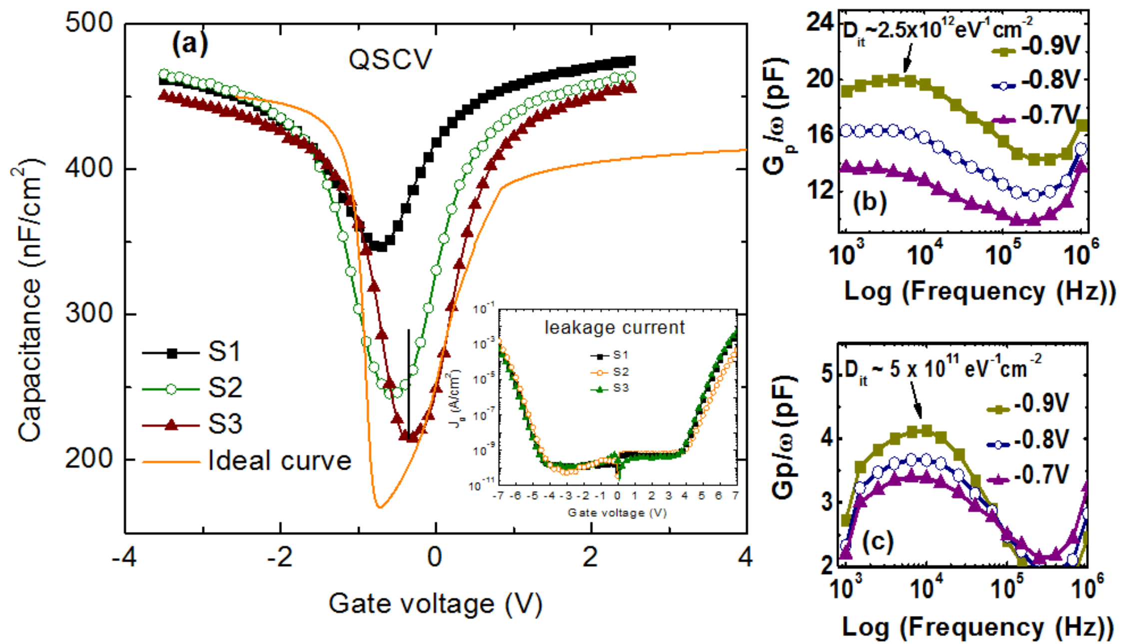


Fig. 5.4. a-The comparison of QSCV responses of sample S1, sample S2 and sample S3 and ideal C-V curve (without D_{it}) obtained by simulation. The inset shows the leakage of samples for ensuring the accuracy of measurement; b- and c- The G_p/ω - f curves of sample S1 and sample S2, where G_p is the parallel conductance and ω is the measured angular frequency.

The conductance method with the application limited to the depletion region is used to estimate the interface trap density near midgap of sample S1 and sample S2.[18] From the Gp/ω versus frequency curves shown in Fig. 4(b) - 4(c), the values obtained are about

2.5×10^{12} $eV^{-1}cm^{-2}$ and 5×10^{11} $eV^{-1}cm^{-2}$, respectively for sample S1 and S2. For sample S3, the inversion layer occurred at frequency as high as 1 MHz and the use of conductance method will overestimate. The D_{it} value of this sample, however, can evaluate by simulation as follows.

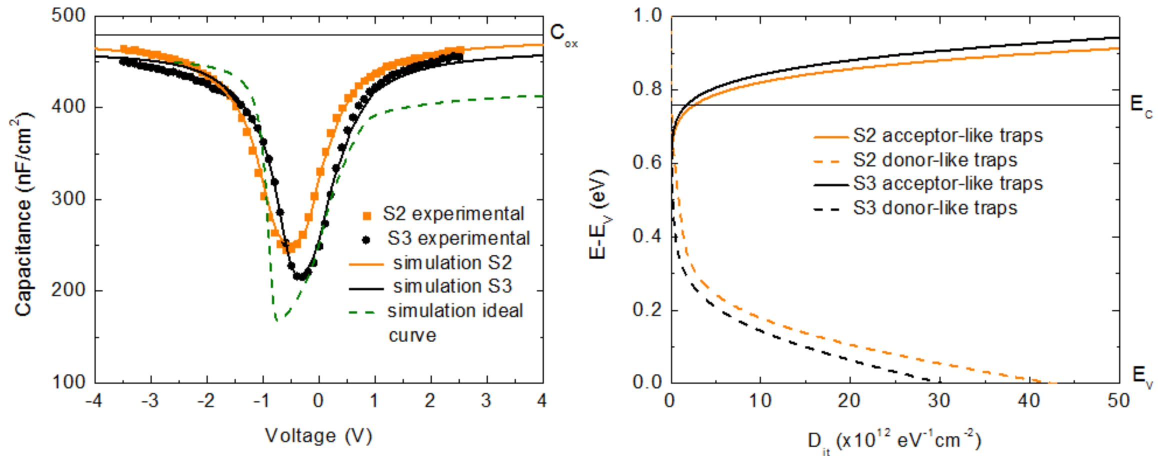


Figure 5.5. a- Quasi-static C-V data of sample S2 and S3 (symbols) are fitted well with corresponding simulated data (solids). The ideal C-V curve is also showed as well (dash line); b- "U-shape" D_{it} profiles of samples S2 and S3 extracted from simulation.

Based on QSCV data of samples, the simulations with D_{it} were performed for sample S2 and S3 as shown in Figure 5.5. As shown in Fig. 5.5a, simulated curves are fitted well with experimental data. The extracted D_{it} profiles of these two samples show a "U-shape" with low D_{it} values at energy positions of 0.4 eV to near InGaAs conduction band (Fig. 5.5b). The smallest value of D_{it} of sample S2 is about 2.5×10^{11} $eV^{-1}cm^{-2}$, in agreement with conductance method. Obviously, the D_{it} profile of sample S3 is lower than that of the sample S2 with the significant reduction of D_{it} at lower half InGaAs bandgap. Minimum value of 6×10^{10} $eV^{-1}cm^{-2}$ is obtained for this sample.

5.4. Conclusions

In conclusion, the effects of various surface treatments and different gas annealing conditions on the electrical characteristics of ALD Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors were studied. We report the true inversion channel in Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor structure by using the combination of ex-situ sulfide treatment and in-situ TMA pretreatment passivated surface and post deposition annealing in pure H_2 gas. Both C-V and XPS data show a strong effect of H_2 annealing on the reduction of interface trapping states. D_{it} extraction from simulation and conductance method is consistent with each

other and low interface D_{it} profiles with minimum value smaller than 10^{11} $eV^{-1}cm^{-2}$ were obtained. A true inversion behavior supports an evidence of the free movement of Fermi level at lower half-part band gap. However, further work is needed verify if it is a truly unpinned Fermi level.

References

[1] R. Chau, S. Datta, and A. majumdar, "Opportunities and Challenges of III-V Nanoelectronic for High-speed, Low-power Logic Applications," IEEE CSIC Syposium Technical Digest, 17 (2005).

[2] S. Koveshnikov, N. Goel, P. Majhi, H. Wen, M. B. Santos, S. Oktyabrsky, V. Tokranov, R. Kambhampati, R. Moore, F. Zhu, J. Lee, and W. Tsai "$In_{0.53}Ga_{0.47}As$ based metal oxide semiconductor capacitors with atomic layer deposition ZrO_2 gate oxide demonstrating low gate leakage current and equivalent oxide thickness less than 1 nm," Appl. Phys. Lett. **92**, 222904 (2008).

[3] Y. Q. Wu, Student, W. K. Wang, O. Koybasi, D. N. Zakharov, E. A. Stach, S. Nakahara, J. C. M. Hwang, and P. D. Ye, "0.8-V Supply Voltage Deep-Submicrometer Inversion-Mode $In_{0.75}Ga_{0.25}As$ MOSFET," IEEE Electron Device Lett. **30**, 700-702 (2009).

[4] G. Dewey, R. Kotlyar, R. Pillarisetty, M. Radosavljevic, T. Rakshit, H. Then, and R. Chau, "Logic Performance Evaluation and Transport Physics of Schottky-Gate III-V Compound Semiconductor Quantum Well Field Effect Transistors for Power Supply Voltages (V_{CC}) Ranging from 0.5V to 1.0V," in IEDM' 09 Tech. Dig., 1-4 (2009).

[5] C. L. Hinkle, M. Milojevic, E. M. Voge, and R. M. Wallace, "The significance of core-level electron binding energies on the proper analysis of InGaAs interfacial bonding," Appl. Phys. Lett. **95**, 151905 (2009).

[6] Han-Chung Lin, Wei-E. Wang, Guy Brammertz, Marc Meuris, and Marc Heyns, "Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator," Microelectron. Eng. **86**, 1554-1557, (2009).

[7] Roman Engel-Herbert, Yoontae Hwang, Joël Cagnon, and Susanne Stemmer, "Metal-oxide-semiconductor capacitors with ZrO2 dielectrics grown on $In_{0.53}Ga_{0.47}As$ by chemical beam deposition," Appl. Phys. Lett. **95**, 062908 (2009).

[8] Byungha Shin, Joël Cagnon, Rathnait D. Long, Paul K. Hurley, Susanne Stemmer, and Paul C. McIntyre, "Unpinned Interface Between Al_2O_3 Gate Dielectric Layer Grown by Atomic Layer Deposition and Chemically Treated n-$In_{0.53}Ga_{0.47}As$(001)," Electrochem. Solid-State Lett. **12**, G40-G43 (2009).

[9] É. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, and P. K. Hurley, "Temperature and frequency dependent electrical characterization of $HfO_2/In_xGa_{1-x}As$ interfaces using capacitance-voltage and conductance methods," Appl. Phys. Lett. **94**, 102902 (2009).

[10] E. O'Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, P. K. Hurley, B. Brennan, G. Hughes, and S. B. Newcomb,"In situ H_2S passivation of $In_{0.53}Ga_{0.47}As$/InP metal-oxide-semiconductor capacitors with atomic-layer deposited HfO_2 gate dielectric," Appl. Phys. Lett. **92**, 022902 (2008).

[11] Y. C. Chang, M. L. Huang, K. Y. Lee, Y. J. Lee, T. D. Lin, M. Hong, J. Kwo, T. S. Lay, C. C. Liao, and K. Y. Cheng, "Atomic-layer-deposited HfO_2 on $In_{0.53}Ga_{0.47}As$: Passivation and energy-band parameters," Appl. Phys. Lett. **92**, 072901 (2008).

[12] R. D. Long, É. O'Connor, S. B. Newcomb, S. Monaghan, K. Cherkaoui, P. Casey, G. Hughes, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, and P. K. Hurley, "Structural analysis, elemental profiling, and electrical characterization of HfO_2 thin films deposited on $In_{0.53}Ga_{0.47}As$ surfaces by atomic layer deposition," J. Appl. Phys. **106**, 084508 (2009).

[13] N. Goel, P. Majhi, W. Tsai, M. Warusawithana, D. G. Schlom, M. B. Santos, J. S. Harris and Y. Nishi, "High-indium-content InGaAs metal-oxide-semiconductor capacitor with amorphous $LaAlO_3$ gate dielectric," Appl. Phys. Lett. **91**, 093509 (2007).

[14] Yoontae Hwang, Mark A. Wistey, Joël Cagnon, Roman Engel-Herbert, and Susanne Stemmer, "Metal-oxide-semiconductor capacitors with erbium oxide dielectrics on $In_{0.53}Ga_{0.47}As$ channels," Appl. Phys. Lett. **94**, 122907 (2009).

[15] M. Passlack, M. Hong, and J. P. Mannaerts, "C-V and G-V characterization of in-situ fabricated Ga_2O_3-GaAs interfaces for inversion/accumulation device and surface passivation applications," Solid-State Electron. **39**, 133-1136 (1996).

[16] M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, H. C. Kim, E. M. Vogel, J. Kim,nand R. M. Wallace, "Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces," Appl. Phys. Lett. **93**, 252905 (2008).

[17] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces," Appl. Phys. Lett. **95**, 202109 (2009).

[18] D. K. Schroder, "Semiconductor Material and Device Characterization," John Wiley and Sons, Inc., ISBN-13: 978-0-471-73906-7, 321-323 (2006).

Chapter 6

INVESTIGATION OF ELECTRICAL CHARACTERISTICS OF AL_2O_3/N-$IN_XGA_{1-X}AS$ (X = 0.53, 0.7) AND INAS CAPACITORS

In this chapter, the electrical properties of Al_2O_3/n-InGaAs MOS capacitors with In content of 0.53, 0.7 and 1 (InAs) are investigated. Higher In content materials usually have lower band gap, higher electron mobility and higher intrinsic carrier density. These properties lead to the different electrical properties for the $Al_2O_3/In_xGa_{1-x}As$ structures. Result shows small C-V frequency dispersion in accumulation (< 1% per decade) which mostly due to border traps in Al_2O_3. Shorter minority carrier response time and smaller C-V hysteresis are observed for the $In_xGa_{1-x}As$ materials with the increase of In content. Conductance contours show the trace of Fermi level movement for $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure but not for $Al_2O_3/In_{0.7}Ga_{0.3}As$ and Al_2O_3/InAs structures. The D_{it} profile shows low interface density located in range 0.4 - 0.74 eV above $In_{0.53}Ga_{0.47}As$ valence band maximum. The influence of holes and electrons tunneling on the increase of leakage current with the increase of In content is discussed.

6.1. Introduction

High-k/III-V structure has been extensively studied recently in order to realize the 22 - 16 nm node and beyond complement metal-oxide-semiconductor (MOS) technology [1]. Regardless of long term effort by community, the high trap density at high-k/III-V interface (D_{it}) due to III-V native oxides is still a challenge. The passivation of high-k/III-V interface is away needed in order to reduce the D_{it}. Recent reports indicated that the D_{it} not only depends on the passivation method but also influence by III-V compounds themselves [2]. The study of high-k/n-InGaAs structure with In content from 0 to 0.53 showed a significant reduction of capacitance-voltage (C-V) frequency dispersion at accumulation region as In content reaches 0.53 [3]. In this work, we extend to study the electrical properties of high-k/n-InGaAs structures with the In content varies from 0.53 to 1. The change of electrical properties of atomic layer deposition (ALD) Al_2O_3/n-InGaAs structures with increase of In content such as frequency dispersion, hysteresis, D_{it} distribution, leakage current, and minority carrier response time are discussed.

The study results in chapter 3 and chapter 4 demonstrated clearly the effect of HCl plus TMA treatment on the improvement of Al_2O_3/n-InAs interface. In this work, this kind of surface treatment is also used for the investigation.

6.2. Experiment

Figure 6.1a illustrates the parameters of InGaAs [4] and structures of Al_2O_3/InGaAs MOS capacitors with different In content. The epi-layers with doping concentration of $2x10^{17}$ cm^{-3} were grown by molecular beam epitaxy (MBE) method on n^+ InP substrates. The process for MOSCAP fabrication is described in Fig. 6.1.b. Wafers were degreased by acetone and isopropanol before using HCl solution to remove native oxides. In ALD chamber, in situ trimethyl aluminum (TMA) clean was used by employing several TMA/N_2 pulses before the deposition of 13 nm Al_2O_3 at 300 ^oC using TMA and H_2O as precursors. The in-situ TMA cleaning is effective in further remove of native oxides [5-8]. After that, samples were post oxide deposition annealed at 400 ^oC in forming gas (5% H_2 95% N_2) for 10 min. Finally, Ti/Pt/Au gate metal and Au/Ge/Ni/Au back side contact were deposited followed by post metal deposition annealing at 400 ^oC in N_2 gas for 30s. The MOSCAPs were characterized by multi-frequency C-V measurement using an Agilent HP 4284A precision LCR meter and I-V measurement using a Keithley 4200 semiconductor analyzer. Al_2O_3/InGaAs, InAs interfaces were analyzed by X-ray

photoelectron spectroscopy (XPS) measurement and high-resolution transmission electron microscopy.

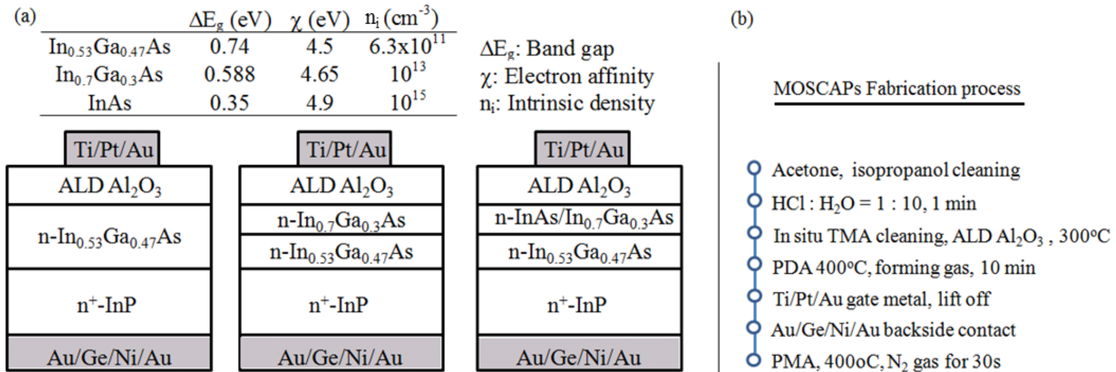


Figure 6.1. a- Parameters of InGaAs compound [4] and Schematic of Al_2O_3/n-InGaAs MOSCAPs structures with the In content is 0.53, 0.7, and 1; b- Summary of process flow for MOSCAP fabrication.

6.3. Results and discussion

6.3.1. X-ray photo electron spectroscopy analysis

Figure 6. 2 illustrates the As 3d, In $3d_{5/2}$ and Ga $2p_{3/2}$ X-ray photoelectron spectroscopy (XPS) spectra of the native-oxide-covered InGaAs, InAs surfaces and Al_2O_3/InGaAs, InAs interfaces after HCl plus TMA treatment following ALD 1.5 nm Al_2O_3 deposition. The As 3d spectra show the reduction of As_2O_3 and As_2O_5 to below the detection level of XPS for all samples after surface treatment and Al_2O_3 deposition. In- and Ga-related oxides of samples using surface treatment were also significant removed as indicating by the decrease of In $3d_{5/2}$ and Ga $2p_{3/2}$ spectra's shoulders which contributed by native oxides (see the In $3d_{5/2}$, Ga $2p_{3/2}$ spectra, Fig. 6.2).

6.3.2. High-resolution transmission electron microscopy micrographs

Cross-sectional HRTEM micrographs of the samples are shown in Fig. 6.3. Normally, an air-exposed InGaAs, InAs have native oxide layers with thickness of above 2nm [9]. Here, the samples show an abrupt transition from InGaAs, InAs to Al_2O_3 without interface layers. These imply that most of native oxides were removed and the rest layers are not identified by HRTEM, in consistent with XPS results. The InGaAs, InAs substrates structures are highly order up to the interface as seen from their periodic lattice images and the interface morphologies exhibit good thermal stability after PDA at 400°C. Al_2O_3 films are amorphous as shown in the figure and the thickness of oxide films estimated

from TEM graphs are about 13.2 nm, in consistent with the estimation from number of ALD cycles (13 nm).

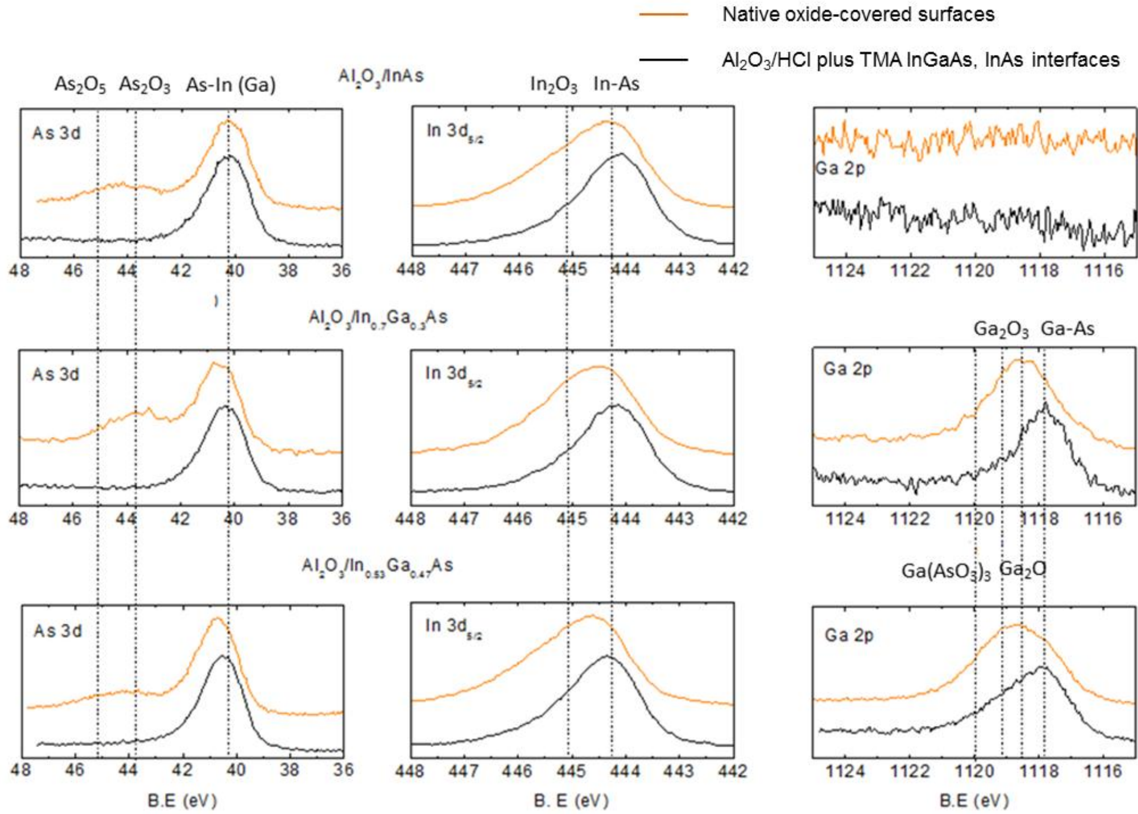


Figure 6.2. As 3d and In $3d_{5/2}$ XPS spectra of (a) native-oxide-corvered InAs surface and (b) 1.5 nm Al_2O_3/InGaAs, InAs structures, as deposition. After using surface treatment and oxide depositon, As-related oxides were reduced to under XPS detection level, the Ga-O and In-O bonds were also significant removed.

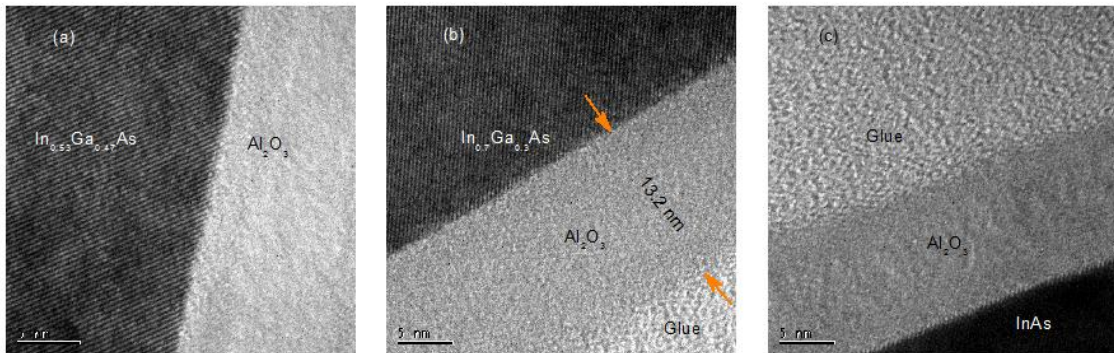


Figure 6.3. High-resolution transmission electron microscopy micrographs of 13nm ALD Al_2O_3/InGaAs structures after PDA at 400°C in forming gas: a-$Al_2O_3/In_{0.53}Ga_{0.47}As$, b-$Al_2O_3/In_{0.7}Ga_{0.3}As$, and c-$Al_2O_3$/InAs, showing abrupt Al_2O_3/InGaAs, InAs interfaces.

6.3.3. Electrical characteristics

The C-V responses of MOSCAP structures at the frequency of 1MHz is shown in Fig. 6.4. When In content increases, the C-V responses change from high-frequency to low-frequency C-V behaviors. For the case of InAs, strong inversion layer is observed at high frequency of 1 MHz. This implies that the minority carrier (holes) response time, τ_R decreases with increasing of In content. The minority carrier response time can be described by the relationship $\tau_R \sim \tau_T/n_i$ [10], where τ_T is the carrier life time and n_i is the intrinsic carrier concentration. The intrinsic carrier concentration n_i increases rapidly with the increasing of In content, from ~6.3×10^{12} cm^{-3} for $In_{0.53}Ga_{0.47}As$ to ~10^{15} cm^{-3} for InAs as shown in Fig. 6.1 [4]. This explains the minority carrier responses faster when In content is higher.

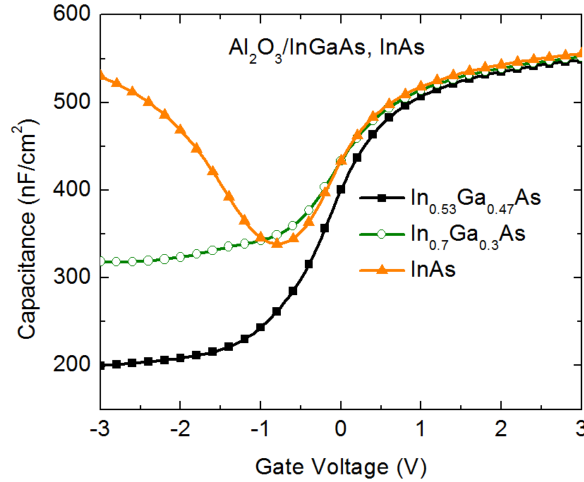


Figure 6.4. Capacitance voltage responses at measured frequency of 1 MHz of $Al_2O_3/In_xGa_{1-x}As$ MOSCAPs with different In content

The multi-frequency C-V responses of MOSCAP structures shown in Fig. 6.5 indicate small frequency dispersion in accumulation region (< 1.1% per decade). With doping concentration N_D of $2x10^{17}$ cm^{-3}, the Fermi level lies very close to $In_{0.53}Ga_{0.47}As$ conduction band edge (about 0.0013 eV below E_C) and ~0.022 eV above InAs conduction band edge [4, 11]. Thus, in the accumulation region, due to the band bending, the Fermi level at Al_2O_3/InGaAs, InAs interface would lie inside conduction bands. In this case, traps response time can be determined by.

$$\tau_{it} = \frac{1}{v_{th}\sigma N} \tag{6.1}$$

where, σ is the capture cross-section of the trapping state, v_{th} is the thermal velocity of the majority charge carriers, and N is the density of states in the majority carrier band. The traps response time determined by (6.1) is very small, order of 10^{-10} s, corresponding to response frequencies of order of several hundred MHz. With that very high response frequency, the contribution of traps to the frequency dispersion cannot be realized with traditional C-V measurement (frequencies in range of 100 Hz – 1 MHz). In this case, the frequency dispersion is mostly due to the contribution of border traps which locate near interface, inside oxide. Effects of border traps on Al_2O_3/InGaAs, InAs structure are very similar as indicated by very similar frequency dispersion values (Fig 6.5).

Bidirectional C-V responses show the reduction of hysteresis with the increase of In content (Fig. 6.5), implying the reduction of traps effect. This results can be explained by the Empirical model which proposed by P. D. Ye [2, 12]. According to this model, when increasing In content, the bandgap is decreased and it will lead to decrease total density of traps and hence their effect is reduced.

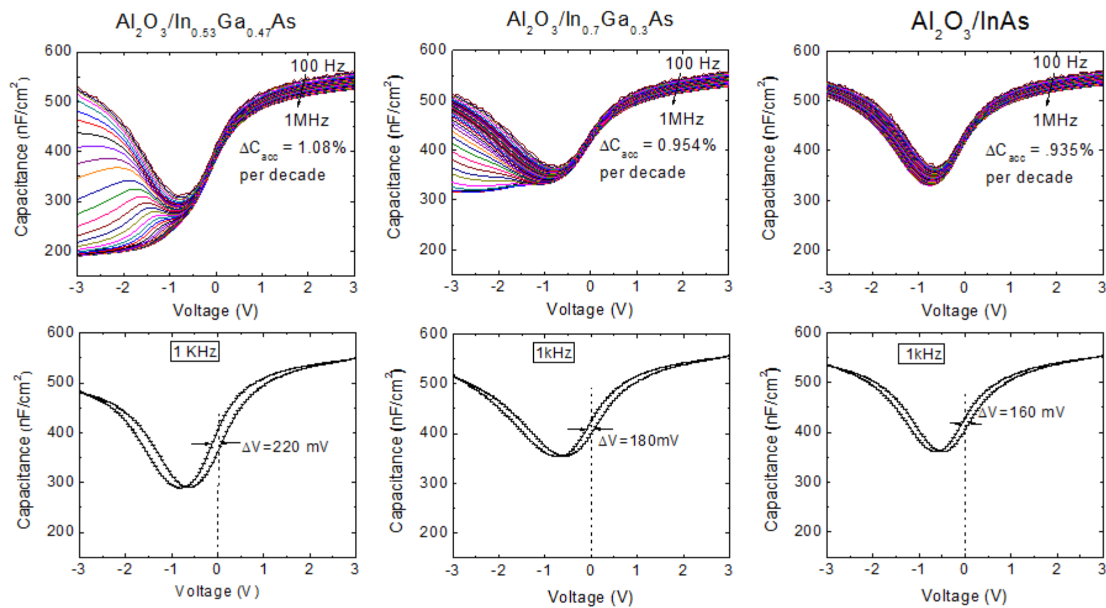


Figure 6.5. Multi-frequency and bidirectional C-V responses of of $Al_2O_3/In_xGa_{1-x}As$ MOSCAPs with different In content

Temperature dependent C-V, G-V measurements were performed at 77K, 180K, and 300K for all samples. Figure 6.6a shows the multi-frequency C-V and conductance maps G_p/ω at different temperatures of Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ structure. These measurements enable to extract the interface traps at different energy positions inside the bandgap as

shown in Fig. 6.6b. Except weak inversion C-V responses at frequency of smaller than 4 kHz at room temperature, high-frequency curves are observed in all range of measured frequencies (1kHz-1MHz) and temperatures. This allows us to ensure the accuracy of the extracted conductance contours. From the conductance map, the traces of movement of Fermi level (solid lines, Fig. 6.6a, conductance contours) are observed clearly as the gate voltage is varied, indicating unpinning Fermi level in $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs. Figure 6 shows the D_{it} profile of $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure obtained by simulation [13] and conductance method [14]. Both two method show low D_{it} of 10-2×10^{11} eV^{-1}cm^{-2} at the energy position from 0.4 to 0.74 eV above valence band minimum and D_{it} increase at the lower half of the $In_{0.53}Ga_{0.47}As$ bandgap. Notice that in this work the PDA temperature was performed at 400°C to optimize the quality of Al_2O_3/InAs interface [15]. For $Al_2O_3/In_{0.53}Ga_{0.47}As$, lower D_{it} profile of was achieved for the sample annealed at 500°C (see chapter 5).

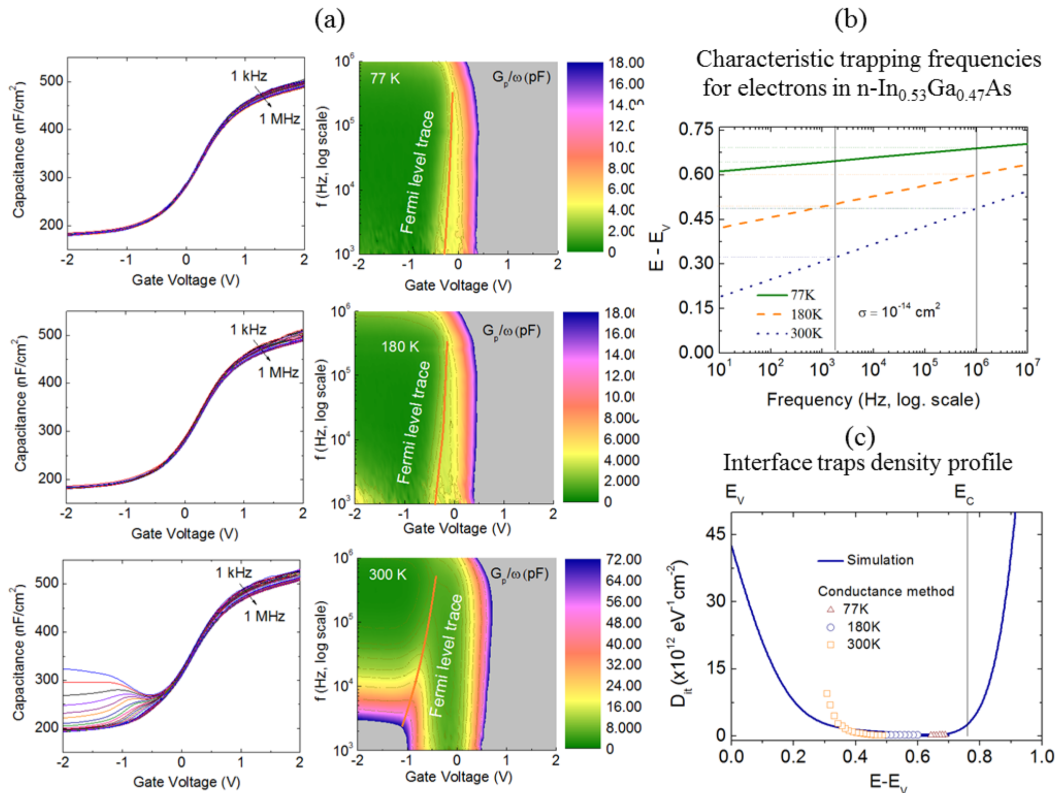


Figure 6.6. a-Multi-frequency C-V responses and conductance contours G_p/ω (f, V) at different temperatures (77 K, 180 K and 300 K) of $Al_2O_3/In_{0.53}Ga_{0.47}As$. Peaks of conductance shows the traces of Fermi level movement (solid lines); b-Characteristic trapping frequencies for electrons in n-$In_{0.53}Ga_{0.47}As$; c-The interface trap density profile of $Al_2O_3/In_{0.53}Ga_{0.47}As$ extracted by conductance method is good agreement with that extracted by simulation.

Figure 6.7 shows the multi-frequency C-V responses and corresponding conductance contours of $Al_2O_3/In_{0.7}Ga_{0.3}As$ and $Al_2O_3/InAs$ structures. As shown in the figure and Fig. 6.4, high-frequency C-V responses seem not to be observed even temperature was cooled down to 77K. Since inversion layers always respond all range of measured frequencies and temperatures, their contribution to the conductance will hide the accuracy of conductance method. As can see in the figure, the conductance contours are always closed due to the contribution of inversion carriers. Thus, the extraction of D_{it} as well as the traces of Fermi level is not obtained. To eliminate the contribution of inversion layer, the application of full conductance method is needed [16].

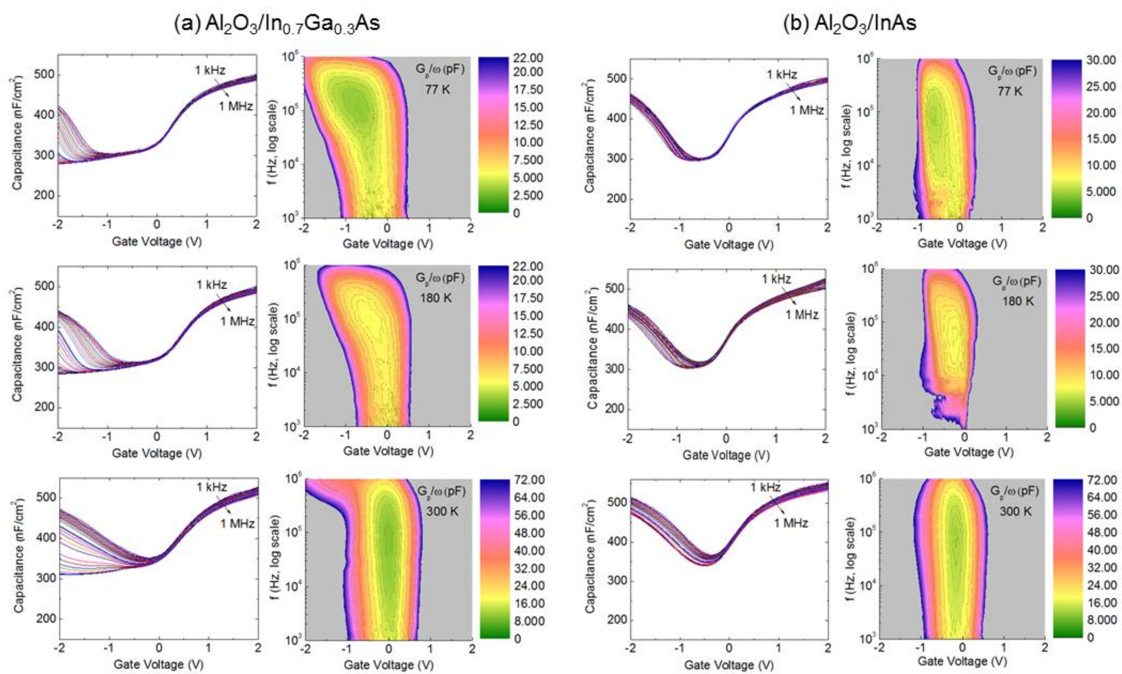


Figure 6.7. Multi-frequency C-V responses and conductance contours Gp/ω (f, V) at different temperatures (77 K, 180 K and 300 K) of a-$Al_2O_3/In_{0.7}Ga_{0.3}As$, and b-$Al_2O_3/InAs$ MOSCAPs. Conductance contours are closed due to the contribution of inversion layer and thus, the Fermi level traces could not show up.

The leakage current increases with the increase of In content as shown in Fig. 6.8a. With the increase of In content, the intrinsic carrier density increases rapidly (parameters shown in Fig. 6.1). Thus at native gate bias, the increase of holes tunneling from semiconductor though oxide to gate metal will result in the increase of leakage current. At positive gate voltage, electrons transfer from semiconductor through the oxide to gate metal. The larger In content in InGaAs, the smaller electron effective mass is, thus, it more susceptible to electrons tunneling through oxide.

The leakage current of samples are plotted in the Flower-Nordheim (FN) form as show in Fig. 6.8b-d [17, 18]. The linear relation of $\ln(1/E_{ox}^2)$ vs $1/E_{ox}$ indicates the FN tunneling at high electric field. The slope is expressed by:

$$S = \frac{d[\ln(1/E_{ox}^2)]}{d(1/E_{ox})} = \frac{4\sqrt{2m^*}}{3q\hbar}\phi^{3/2} \quad (6.2)$$

where m* is electron effective mass within Al_2O_3 and ϕ is the tunneling barrier height. From the measured slope, assume the effective mass m* = 0.23m_e [19], the barrier heights are evaluated to be 1.89 eV, 1.97 eV and 2.07 eV for $Al_2O_3/In_{0.53}Ga_{0.47}As$, Al_2O_3/In0$_{.7}Ga_{0.3}$As and $Al_2O_3/InAs$, respectively.

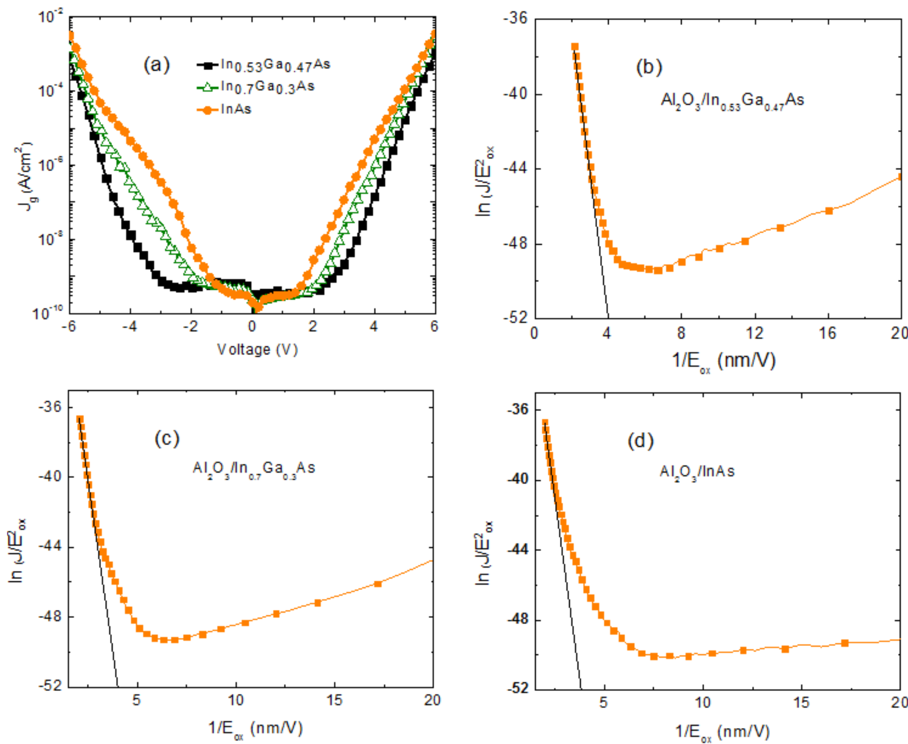


Figure 6.8. a- leakage current increases with increasing of In content in InGaAs. The Flower-Nordheim plot for b- $Al_2O_3/In_{0.53}Ga_{0.47}As$, c-$Al_2O_3/In_{0.7}Ga_{0.3}As$ and d-$Al_2O_3/InAs$ structures.

6.4. Conclusions

We have studied the material and electrical characteristics of ALD $Al_2O_3/InGaAs$ structures, with In content of 0.53, 0.7, and 1. XPS analysis shows the significant reduction of native oxides after HCl plus TMA treatment. HRTEM micrographs showed abrupt $Al_2O_3/InGaAs$, InAs interface layers. Multi-frequency C-V responses show low frequency dispersion in accumulation region. These frequency dispersions seem mostly

due to border traps in oxide rather than due to interface traps. Conductance method and simulation results showed the low interface trap density distribution at energy position of 0.4 to 0.74 eV above valence band of InGaAs. The conductance contours trace the movement of Fermi level at varied gate bias for the case of $In_{0.53}Ga_{0.47}As$ but not for $In_{0.7}Ga_{0.3}As$ and InAs due to the contribution of inversion layer. The increase of leakage current in In-rich $Al_2O_3/In_xGa_{1-x}As$ structures indicated larger probability of holes and electrons tunneling though oxide due to the increase of intrinsic carrier density and the reduction of electron effective mass in In-rich samples.

References

[1] R. Chau, S. Datta, and A. majumdar, "Opportunities and Challenges of III-V Nanoelectronic for High-speed, Low-power Logic Applications," IEEE CSIC Syposium Technical Digest 17 (2005).

[2] P. D. Ye, "Main determinants for III-V metal-oxide-semiconductor field-effect transistors (invited)," J. Vac. Sci. Technol. A **26**, 697-704, (2008).

[3] É. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, and P. K. Hurley, "Temperature and frequency dependent electrical characterization of $HfO_2/In_xGa_{1-x}As$ interfaces using capacitance-voltage and conductance methods," Appl. Phys. Lett. **94**, 102902 (2009).

[4] Source: http://www.ioffe.ru/SVA/NSM/.

[5] H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, "The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor," Appl. Phys. Lett. **97**, 042903 (2010).

[6] Hai-Dang Trinh, Edward Yi Chang, Yuen-Yee Wong, Chih-Chieh Yu, Chia-Yuan Chang, Yueh-Chin Lin, Hong-Quan Nguyen, and Binh-Tinh Tran "Effects of Wet Chemical and Trimethyl Aluminum Treatments on the Interface Properties in Atomic Layer Deposition of Al_2O_3 on InAs," Jpn. J. Appl. Phys. **49**, 111201 (2010).

[7] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," Appl. Phys. Lett. **92**, 071901 (2008).

[8] M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, H. C. Kim, E. M. Vogel, J. Kim, and R. M. Wallace, "Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces," Appl. Phys. Lett. **93**, 252905 (2008).

[9] Y. C. Chang, M. L. Huang, K. Y. Lee, Y. J. Lee, T. D. Lin, M. Hong, J. Kwo, T. S. Lay, C. C. Liao, and K. Y. Cheng, "Atomic-layer-deposited HfO_2 on $In_{0.53}Ga_{0.47}As$: Passivation and energy-band parameters," Appl. Phys. Lett. **92**, 072901 (2008).

[10] E. H. Nicollian and J. R. Brews, "MOS Physics and Technology," John Wiley and Sons, ISBN 0-471-08500-6, 139 (1982).

[11] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," John Wiley & Sons, ISBN-I 3: 978-0-47 1-1 4323-9, 19-20 (2007).

[12] Serge Oktyabrsky, and Peide D. Ye, *Editors* "Fundamentals of III-V Semiconductor MOSFETs," Spring, ISBN 978-1-4419-1546-7, 178-181 (2010).

[13] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at In0.53Ga0.47As/oxide interfaces," Appl. Phys. Lett. **95**, 202109 (2009).

[14] G. Brammertz, H.-C. Lin, K. Martens, D. Mercier, S. Sioncke, A. Delabie, W. E. Wang,M. Caymax, M. Meuris, and M. Heyns, "Capacitance-voltage characterization of GaAs–Al_2O_3 interfaces," Appl. Phys. Lett. **93**, 183504 (2008).

[15] Ning Li, Eric S. Harmon, James Hyland, David B. Salzman, T. P. Ma, Yi Xuan, and P. D. Ye, "Properties of InAs metal-oxide-semiconductor structures with atomic-layer-deposited Al_2O_3 Dielectric," Appl. Phys. Lett. **92**, 143507 (2008).

[16] K. Martens, C. Chi On, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates," IEEE Trans. Electron Devices **55**, 547-556 (2008).

[17] T. S. Lay, M. Hong, J. Kwo, J. P. Mannaerts, W. H. Hung, and D. J. Huang, "Energy-band parameters at the GaAs- and GaN-Ga_2O_3(Gd_2O_3) interfaces," Solid-State Electron. **45**, 1679-1682 (2001).

[18] M. L. Huang, Y. C. Chang, Y. H. Chang, T. D. Lin, J. Kwo, and M. Hong, "Energy-band parameters of atomic layer deposited Al_2O_3 and HfO_2 on $In_xGa_{1-x}As$," Appl. Phys. Lett. **94**, 052106 (2009).

[19] Davood Shahrjerdi,a Emanuel Tutuc, and Sanjay K. Banerjee, "Impact of surface chemical treatment on capacitance-voltage characteristics of GaAs metal-oxide-semiconductor capacitors with Al_2O_3 gate dielectric," Appl. Phys. Lett. **91**, 063501 (2007).

Chapter 7

CONCLUSIONS

This dissertation has focused on characterization and improvement of the atomic layer deposition Al_2O_3/InGaAs, InAs interfaces. In order to improve the interfaces quality, various combinations of ex-situ chemical treatments and in-situ TMA pretreatment were used and compared. Besides, the effect of annealing conditions on the interfaces quality was also studied. The followings are the conclusions of this work.

We have studied the effect of TMA treatment on the native-oxide-covered, HCl-treated, and sulfide-treated n-InAs surfaces. The effect of TMA on the reduction of InAs native oxides was apparent almost after the first TMA pulse but significant amount of native oxides still remain if only TMA treatment was used. The combination of HCl or sulfide wet chemical treatments with dry TMA pretreatment made a strong effect in the reduction of InAs native oxides. Native oxides were significant removed by wet chemical surface treatments and further reduction was achieved by TMA treatment. Electrical characterization of Al_2O_3/n-InAs MOSCAPs with different kind of surface treatments showed that Al_2O_3/InAs interface quality with HCl plus TMA treatment was better than that using sulfide plus TMA treatment.

By deposition of Al_2O_3 at 300^oC, the quality of Al_2O_3/InAs interfaces was improved significantly. C-V characteristics of Al_2O_3/n-InAs exhibited strong inversion behaviors and low frequency dispersion in both inversion and accumulation regimes. Low-frequency simulations were performed and Al_2O_3/InAs interface trap states profiles were extracted. The derived D_{it} profiles present a U-shape with a minimum in the D_{it} profiles located around the InAs conduction band minimum, i.e. donor-like traps are dominant inside bandgap. These donor-like traps were significant reduced by using wet chemical

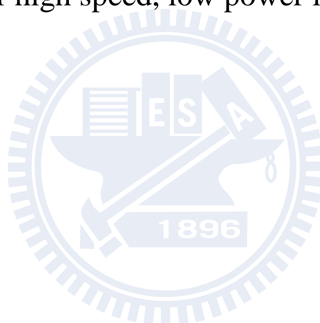
plus TMA treatments. In addition, this study confirmed again the HCl plus TMA treatment is more effective than sulfide treatment in the improvement Al_2O_3/InAs interface quality.

The influence of surface treatment and gas annealing conditions on the inversions behaviors of Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs structures has been studied. By using sulfide plus TMA treatment along with post deposition annealing in pure H_2 gas at 500°C, Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs exhibit strong inversion C-V responses. This behavior in Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs was first time observed by using an ex-situ method. In this study, beside the surface treatment, the H_2 gas treatment also showed strong effect in the improvement of Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface quality, especially in the reduction of interface traps at lower-half $In_{0.53}Ga_{0.47}As$ bandgap. Low D_{it} profiles were observed by simulation and the minimum D_{it} value of $\sim 1\times10^{11}$ $eV^{-1}cm^{-2}$ was confirmed by both simulation and conductance method.

The electrical properties of Al_2O_3/$In_xGa_{1-x}As$ MOSCAPs structures with different In content of 0.53, 0.7 and 1 (InAs) have been investigated. Higher In content materials usually have lower band gap, higher electron mobility and higher intrinsic carrier density. These properties lead to the different electrical properties for the Al_2O_3/$In_xGa_{1-x}As$ structures. Results showed clearly the decrease of minority carrier response time τ_R with the increase of In content. C-V frequency dispersions in accumulation regions seem mostly due to border traps in oxide rather than due to interface traps. The conductance contours at different temperatures trace the movement of Fermi level at varied gate bias for the case of $In_{0.53}Ga_{0.47}As$ but not for $In_{0.7}Ga_{0.3}As$ and InAs due to the contribution of inversion layer. Al_2O_3/$In_{0.53}Ga_{0.47}As$ D_{it} profile extracted by conductance method is in good agreement with that extracted by simulation. The increase of leakage current in In-rich Al_2O_3/$In_xGa_{1-x}As$ structures indicated larger probability of holes and electrons tunneling though oxide due to the increase of intrinsic carrier density and the reduction of electron effective mass in In-rich samples.

BIOGRAPHY

Trinh Hai Dang was born in Thanh Hoa, Vietnam in October 1979. He received his bachelor of physics degree in Faculty of Physics, Hanoi National University of Education (HNUE), Hanoi, Vietnam in July 2001 and Master of Science degree in International Training Institute for Materials Science (ITIMS), Hanoi University of Technology (HUT), Hanoi, Vietnam in July 2003. He worked at Faculty of Physics, HNUE, Hanoi, Vietnam as a lecture from August 2001 to January 2007. From February 2007 to present, he enrolled into the Doctoral program at Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan under the guidance of Prof. Dr. Edward Yi Chang. His research interests include high k/III-V interface engineering and III-V MOSFET application for high speed, low power logic devices.



LIST OF PUBLICATIONS

Journal Articles

1. H. D. Trinh, G. Brammertz, E. Y. Chang, C. I. Kuo, C. Y. Lu, Y. C. Lin, H. Q. Nguyen, Y. Y. Wong, B. T. Tran, K. Kakushima, and H. Iwai, “Electrical Characterization of Al_2O_3/n-InAs Metal-Oxide-Semiconductor Capacitors with Various Surface Treatments,” IEEE Electron Device Lett. **32**, 752-754 (2011).
2. Hai-Dang Trinh, Edward Yi Chang, Yuen-Yee Wong, Chih-Chieh Yu, Chia-Yuan Chang, Yueh-Chin Lin, Hong-Quan Nguyen, and Binh-Tinh Tran, “Effects of Wet Chemical and Trimethyl Aluminum Treatments on the Interface Properties in Atomic Layer Deposition of Al_2O_3 on InAs,” Japanese J. Appl. Phys. **49**, 111201 (2010).
3. H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, “The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor,” Appl. Phys. Lett. **97**, 042903 (2010).
4. 張翼 金海光 謝廷恩 張嘉華 林岳欽, “高介電氧化層/三五族金屬氧化物半導體場效電晶體：發展近況,” (E. Y. Chang, H. D. Trinh, T. G. Xie, C. H. Chang, Y. C. Lin, “High k/III-V Metal Oxide Semiconductor Field Effect Transistors: Current Status”), Taiwan nano newsletter **23**, 37-41 (2010).
5. Shih-Hsuan Tang, Edward Yi Chang, Mantu Hudait, Jer-Shen Maa, Chee-Wee Liu, Guang-Li Luo, Hai-Dang Trinh, and Yung-Hsuan Su, “High quality Ge thin film grown by ultrahigh vacuum chemical vapor deposition on GaAs substrate,” Appl. Phys. Lett. **98**, 161905 (2011).
6. C.-T. Chang, T.-H. Hsu, E.Y. Chang, Y.-C. Chen, H.-D. Trinh and K.J. Chen, “Normally-off operation AlGaN/GaN MOS-HEMT with high threshold voltage,” Electron. Lett. **46**, 1280-1281 (2010).
7. C.-Y. Chang, H.-T. Hsu, E. Y. Chang, H.-D. Trinh, and Y. Miyamoto, “InAs-Channel Metal-Oxide-Semiconductor HEMTs with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric,” Electrochem. Solid-State Lett. **12**, H456-H459 (2009).

8. Nguyen Minh Thuy, Do Thi Sam, Trinh Hai Dang and Le Van Hong. "Electrical properties of superconducting Bi-2212 thick films," J. Magnetism and Magnetic Material **262**, 526-531 (2003).

Conferences

1. C. C. Yu, H. D. Trinh, B. H. Liu, C. C. Kei, C. N. Hsiao, D. P. Tsai, "Dielectric Performance of Post Deposition Treated Al_2O_3 Films Prepared by Using Parallel-Plate Electrode PEALD," the AVS 58th Annual International Symposium and Exhibition, Nashville, Tennessee, USA, Oct 30 - Nov 4, 2011 (accepted).
2. H. D. Trinh, E.Y. Chang, C. I. Kuo, H. Q. Nguyen, K. L. Lin, Y. Y. Wong, C. C. Chung, Y. C. Lin, C. H. Chang, Y. S. Chiu, B. T. Tran, and C. L. Nguyen, "Atomic Layer Deposition of Al_2O_3/n-$In_xGa_{1-x}As$ structures with different In content (x = 0.53-1)," *the 38th International Symposium on Compound Semiconductors (ISCS 2011)*, Berlin, Germany, May 22-26, 2011.
3. H. Q. Nguyen, E. Y. Chang, H. D. Trinh, H.W. Yu, Y.Y. Wong, H. H. Vu, T. B. Tran, K. L. Lin, C. C. Chung, C. H. Hsu, W .C. Wang and C. L Nguyen, "High quality 1eV InGaAs on GaAs substrate for inverted metamorphic solar cell by MOCVD," *the 38th International Symposium on Compound Semiconductors (ISCS 2011)*, Berlin, Germany, May 22-26, 2011.
4. Yuen-Yee Wong, Edward Yi Chang, Wei-Ching Huang, Hai-Dang Trinh, Chun-Yen Chang, "Reduction of Parallel Conduction at the Regrowth Interface of GaN Template Using Nitridation," *the 38th International Symposium on Compound Semiconductors (ISCS 2011)*, Berlin, Germany, May 22-26, 2011.
5. B. Tran, E. Chang, K. Lin, H. Nguyen, and H. Trinh, "The Growth of High Quality $In_{0.4}Ga_{0.6}N$ Film on Si(111) Substrate without Phase Separation for Photovoltaic Device Applications," *the 219th ECS Meeting in Montreal,* Canada, May *1 - 6, 2011 (accepted).*
6. Y. Wong, E. Chang, W. Huang, H. Trinh, T. Yang, J. Chang, J. Ku, and C. Chen, "Reduction of Parallel Conduction at the Regrowth Interface of GaN Template Using Nitridation," *the 219th ECS Meeting in Montreal*, Canada, May 1 - 6, 2011 (accepted).
7. H. D. Trinh, E. Y. Chang, G. Brammertz, C. Y. Lu, H. Q. Nguyen, B. T. Tran, "Experimental and modeling on atomic layer deposition Al_2O_3/n-InAs metal-oxide-

semiconductor capacitor with various surface treatments," *the China Semiconductor Technology International Conference 2011 (CSTIC 2011)*, Shanghai, China, March 15-17, 2011, (Online: *ECS Transactions*, vol. 34, pp. 1041-1046, 2011) (invited)

8. Hai-Dang Trinh, Edward Yi Chang, Chih-Chieh Yu, Yuen-Yee Wong, Hong-Quan Nguyen, Kung-Liang Lin, Yueh-Chin Lin, Chien-I Kuo, Binh-Tinh Tran, Chi-Lang Nguyen, Yu-Sheng Chiu, Chen-Chen Chung, "Characterization of electrical properties of atomic layer deposition Al_2O_3 on n-$In_{0.53}Ga_{0.47}As$ using conductance method and simulation," *2011 Annual Meeting of the Physical Society of ROC*, Tainan, Taiwan, Jan 25, 2011 (local conference).
9. Yuen-Yee Wong, Edward Yi Chang, Wei-Chin Huang, Hai-Dang Trinh, Hong-Quan Nguyen, "Suppression of Parallel Conduction at the Regrowth Interface of GaN Template Using Nitrogen Plasma Treatment," *2011 Annual Meeting of the Physical Society of ROC*, Taipei, Taiwan, Jan 25, 2011 (local conference).
10. Hong-Quan Nguyen, Edward -Yi Chang, Hung-Wei Yu, Yuen-Yee Wong, Hai-Dang Trinh, Binh -Tinh Tran, Kung-Liang Lin, Chen-Chen Chung, Wei-Chieh Wang, Chi-Lang Nguyen, "The Growth and Investigation of $In_{0.3}Ga_{0.7}As$ on GaAs by MOCVD," *2011 Annual Meeting of the Physical Society of ROC*, Taipei, Taiwan, Jan 25, 2011 (local conference).
11. Binh-Tinh Tran, Edward-Yi Chang, Kung-Liang Lin, Hong-Quan Nguyen and Hai-Dang Trinh, "The Growth and Investigation of $In_{0.3}Ga_{0.7}As$ on GaAs by MOCVD," *2011 Annual Meeting of the Physical Society of ROC*, Taipei, Taiwan, Jan 25, 2011 (local conference).
12. Binh-Tinh Tran, Edward-Yi Chang, Kung-Liang Lin, Kartika Chandra Sahoo, Hsiao-Yu Lin, Nguyen Minh Thuy, Hong-Quan Nguyen, Hai-Dang Trinh, "Influence of Growth Temperatures of AlN Buffer Layers on the Crystalline Quality of GaN Film Grown on Si(111) by Metal Organic Chemical Vapor Deposition," *The 5th International Workshop on Advanced Materials Science and Nanotechnology (IWAMSN 2010)*, Hanoi, Vietnam – November 09-12, 2010.
13. Hai-Dang Trinh, Edward Yi Chang, Yuen-Yee Wong, Chia-Yuan Chang, Chih-Chieh Yu, "Electrical Characteristics of Atomic Layer Deposition Al_2O_3 on n-InAs with various surface treatments," *2010 Annual Meeting of the Physical Society of ROC*, Tainan, Taiwan, February 2-4, 2010 (local conference).

14. H. D. Trinh, E. Y. Chang, Y. Y. Wong, C. Y. Chang, C. C. Yu, "Self-cleaning Effects on Atomic Layer Deposition (ALD) of Al_2O_3 on InGaAs with Several Surface Treatments," *2009 International Conference on Solid State Devices and Materials (SSDM2009)*, Sendai, Japan, October 7-9, 2009.

15. C. Chang, E. Chang, W. Huang, Y. Su, H. Trinh, H. Hsu and Y. Miyamoto, "InAs-Channel Metal-Oxide-Semiconductor HEMTs with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric," *216th ECS Meeting in Vienna*, Austria, October 4-9, 2009 (Online: *ECS Transactions*, vol. 25, pp. 87-92, 2009).

16. Hai-Dang Trinh, Edward Yi Chang, Yuen-Yee Wong, Binh-Tinh Tran, Chih-Chieh Yu, Chi-Chung Kei, Wen-Hao Cho, "Impact of surface treatment and self-cleaning effects on atomic layer deposition (ALD) of Al_2O_3 on InAs," *the 9th Conference on Atomic Layer Deposition*, Monterey, California, USA, July 19-22, 2009.

17. N.V. Minh, V. Vien, N.T.M. Hien, V.S. Noh, J. Kim, I.S. Yang, N.T. Dung, T.H. Dang, D.D.Bich, N.C. Khang, N.M.Thao, N.T.Khoi "Nanosize Co doped anatase TiO_2: Raman spectroscopy and structural studies," *1st IWOFM - 3rd IWONN Conference*, Halong, Vietnam, December 6-9, 2006 , pp. 661-662

18. Nguyen Van Minh, Trinh Hai Dang, Luc Huy Hoang, Nguyen Van Hung, Nguyen Minh Thuy, Do Thi Sam, Tran Minh Thi, Nguyen The Khoi "Raman scattering of $Bi_2Sr_2CaCu_{1-x}Co_xO_{8+\delta}$ and $Bi_2Sr_2Ca_2Cu_{3-x}Co_xO_{10+\delta}$ systems," *the WHISMAS-04*, Hanoi, Vietnam, 2004, pp. 113-118.

19. Tran Minh Thi, Trinh Hai Dang et al. "Effect of the substitution of Co for Cu on electrical properties of (Bi/Pb) 2223" superconducting compound," *the WHISMAS-04*, Hanoi, Vietnam, 2004, pp. 224-229.

Patents

1. E. Y. Chang, Y. C. Lin, C. H. Chang, and H. D. Trinh, 於半導體上沉積絕緣層的方法及於該沉積之前的表面處理方法, Taiwan patent application No. 100117873.