國 立 交 通 大 學

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利用凝膠轉塗佈法製備高介電常數鈦酸鎳閘極介電質層於複晶矽薄膜電晶體之研究

Study on Polysilicon Thin-Film Transistors with High-κ $NiTiO_3$ Prepared by Sol-Gel Spin Coating Method

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摘 要

在此論文裡，利用新穎低溫技術凝膠旋塗佈法製備具高介電常數的鈦酸鎳介電質層，並對五百到九百度不同溫度熱退火後的樣品做材料與物理特性分析，接著將所得之電性結果應用在複晶矽薄膜電晶體上做進一步之研究。從 X 光繞射光譜分析圖可得知此塗佈上去的鈦酸鎳介電質層的結晶溫度大約介於六百與七百度之間。掃描式探針顯微鏡所顯示在經過不同溫度熱退火之後的鈦酸鎳介電質層的表面形貌，藉此可發現當溫度高於六百度後，樣品的表面粗操度會隨著溫度上升而產生劇烈的劣化現象。由化學分析電子能譜儀的結果顯示，所有的樣品都含有鎳-氧與鈦-氧兩種金屬氧化鍵，另外又發現在低溫兩百度烘烤會有氫氧化物的存在。而更進一步的化學分析電子能譜儀分析確定了此塗佈上去並經過六百度熱退火的介電質層的原子濃度比例，[Ni]：[Ti]：[O]約為 1：1：3。利用高解析度穿透式電子顯微鏡所拍之影像與對應的電容電壓曲線圖，求得介電質鈦酸鎳的介電常數的範圍值約介於 36~42 之間。此外，由電容電壓曲線圖可看出鈦酸鎳介電質具有較薄的電容等效厚度與較高的閘極電容密度。

接下來將凝膠旋塗佈法應用於固相再結晶複晶矽薄膜電晶體上，且鈦酸鎳介電質層經過五百、六百與七百度三種溫度的快速熱退火處理。從種種電性量測結果得知，經過五百

度熱處理的樣品明顯電性優於其它六百與七百度熱處理的樣品。之後，取五百度熱處理樣品另外做氨電漿處理發現，經過氨電漿鈍化處理的電晶體在元件性能以及臨界電壓下降特性上都有顯著的改善。此論文所提出製程薄膜電晶體的技術即便沒有添加其它電漿處理或是先進窄製程窗相結晶技術，都能擁有不錯的電性結果。

Study on Polysilicon Thin-Film Transistors with High-κ $NiTiO_3$ Prepared by Sol-Gel Spin Coating Method

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ABSTRACT

In this thesis, the high-κ $NiTiO_3$ dielectrics are prepared at different annealing temperatures from 500°C to 900°C by a sol-gel spin coating method, which is a novel low-temperature technique to form thin films. The X-ray diffraction (XRD) spectrum describing the crystallization temperature of the spin-on dielectric is between 600°C and 700°C. The scanning probe microscope (SPM) images display that the surface roughness abruptly increases with the annealing temperature higher than 600°C. The electron spectroscopy for chemical analysis (ESCA) exhibits the metal-oxide bonds of Ni-O and Ti-O in all samples and the hydroxides in 200°C-baking sample. Besides, the ESCA also proves that the atomic concentration ratio of the spin-on dielectric with 600°C-RTA treatment is [Ni]:[Ti]:[O] ~ 1:1:3. The high dielectric constant (High-κ) of the $NiTiO_3$ material calculated to be in a range of 36 ~ 42 is extracted from the high-resolution transmission electron microscopy (HR-TEM) image and the corresponding *C-V*

curves. The *C-V* curves shows that the $NiTiO_3$ gate dielectric can achieve a thin capacitance equivalent thickness (CET) and high gate capacitance density.

The solid-phase crystallized (SPC) poly-Si TFTs with a $NiTiO_3$ gate dielectric prepared by the sol-gel spin coating method with 500°C, 600°C and 700°C-RTA treatments have been demonstrated. The electrical characteristics of the poly-Si TFTs with $NiTiO_3$ gate dielectric (poly-Si $NiTiO_3$ TFTs) at 500°C annealing temperature are better than that at 600°C and 700°C-RTA treatments. The device performance and threshold-voltage rolloff properties of the poly-Si $NiTiO_3$ TFTs with 500°C-RTA treatment can be significantly improved with a NH_3 plasma passivation. The proposed poly-Si $NiTiO_3$ TFTs crystallized by the SPC technique could possess good electrical properties even without additional plasma treatments or other advanced phase crystallization techniques with narrow process window.

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Chapter 1

Introduction

Firstly in this chapter, we will explain why the traditional silicon dioxide should be replaced by high-κ gate dielectrics. Then, the fundamental properties of high-κ materials and the requirements for analyzing high-κ gate dielectrics will be introduced. Afterward we will introduce the sol-gel spin coating method used in this thesis and summary of thin-film transistors. Finally, we will introduce the advantages of the plasma treatment for polycrystalline-silicon thin-film transistors (poly-Si TFTs) with high-κ gate dielectrics.

1.1 High-κ Gate Dielectrics Development

In order to enhance the operating speed of the complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC), the high dielectric constant (High-κ) gate dielectrics have been massively investigated to replace conventional silicon dioxide (SiO_2) as the gate dielectric in metal-oxide-semiconductor field-effect transistor (MOSFET) in the past decades [1-13]. Better performance and reduced cost make the scaling of MOSFETs to consist with the famous Moore's law [14], which predicts the trend of the quantity of transistors integrated in a chip as shown in figure 1.1[15]. Channel length scaling enhances the operating speed of devices to ensure the excellent controll ability of gates, but short channel effects [16][17] are getting more obvious. Therefore, the thickness of the gate dielectric must become thinner to suppress short channel effects.

A SiO_2 was used as a gate dielectric when the invention of MOS technology was applied till 0.18 μm due to its good integrity and excellent SiO_2/Si interface properties since 1960. Before 1990, many textbooks represented that the scaling limitation of oxide for a gate

dielectric was 3 nm or thicker. But in 1994, the researchers in Toshiba incorporation showed that the devices of well behavior with a 1.5-nm-thick gate oxide were practical as short channel length [18]. However, the significant increase in gate leakage is still suppressed from gate oxide for further work.

As the thickness of SiO_2 film is smaller than 2 nm, the gate leakage increases markedly. Accordingly, the silicon oxynitride (SiO_xN_y) material replaces SiO_2 material effectively as the major gate dielectric option after 0.18-μm node, and the quantity of incorporated nitrogen increases with decreasing thickness. But SiO_xN_y reached its thickness limitation about 1.2 nm until 2003 as shown in figure 1.2 [19]. There is no obvious fabrication progress to apply to gate dielectric scaling. Consequently, high-κ dielectrics may begin to be used for both low operating power (LOP) and low standby power (LSTP) of 45-nm node in 2008.

From Eq. (1-1) [20][21], we can know that the advantages of thinning gate dielectric are not only to suppress short channel effect and maintain threshold voltage, but also enhance the driving current of the transistors. It's a pity that there are some problems when gate dielectric becomes thinner.

$$I_{D,\text{sat}} = \mu_{\text{eff}} \left(\frac{W}{2L}\right)\left(\frac{\varepsilon_{\text{ox}}}{t_{\text{eq}}}\right)(V_G - V_T)^2 \quad , \quad V_{D,\text{sat}} \geq V_G - V_T \tag{1-1}$$

For example, the thickness of the gate dielectric to 70-nm-node technology is about 10 Å as a few layers of SiO_2 molecules. While the extremely thin gate oxide layer is scaled less than 20 Å, significant leakage current increases because of stress-induced leakage current (SILC) or gate-induced drain leakage (GIDL), and boron penetration occurs for pMOSFETs as shown in figure 1.3 [22]. In addition, the mechanism of gate-leakage current has been led from F-N tunneling changing to direct tunneling. Eq. (1-2) [20] is the relationship between the leakage current of direct tunneling and the thin film thickness of the gate dielectric.

$$I_{DT} \propto \exp\left(-2t_{\text{dielectric}} \sqrt{\frac{2m^* q}{\hbar^2}\left\{ \Phi_B - \frac{V_{\text{dielectric}}}{2} \right\}} \right) \tag{1-2}$$

Hence, the leakage current would increase as the thickness of the gate oxide layer becomes thinner, and result in the large consumption of device's power. Besides, the uncontrollable uniformity of the thickness in fabrication causes the variations of the electric properties. This problem is disallowed in advanced integrated circuit manufacture. Moreover, there are reliability issues such as hot carrier effects, process-induced oxide damage, time-dependent dielectric breakdown (TDDB), electrostatic discharge (ESD) damage and negative-bias-temperature instability (NBTI) for pMOSFETs.

In order to solve these issues, many high-κ materials used to replace gate dielectric of SiO_2 were proposed continually such as silicon nitride (Si_3N_4), silicon oxynitride (SiO_xN_y), aluminum oxide (Al_2O_3) and hafnium dioxide (HfO_2), and some high-κ dielectrics reported in the literatures are listed in table 1.1 [19]. High-κ gate dielectric possesses thicker physical film and thinner equivalent oxide thickness (EOT) so that the problems of the uniformity of an extremely thin gate silicon dioxide layer were unraveled and the leakage current of direct tunneling was suppressed as shown in figure 1.4 [19].

From Eq. (1-3) [20], we can find that after a SiO_2 layer is replaced by a high-κ material (ignoring quantum mechanical and depletion effects from a Si substrate and gate), gate capacitance not only maintains quite high value but also enhances greatly the device's driving current.

$$C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{eq}}} = \frac{\varepsilon_{\text{high-}\kappa}}{t_{\text{high-}\kappa}} \tag{1-3}$$

Nickel-titanium oxide ($NiTiO_3$) [23] material owns quite high dielectric coefficient, which is estimated around 40, and appears to be a very promising high-κ gate dielectric for future ultra-large scale integrated devices.

1.2 Requirements for High-κ Materials as a Gate Dielectric

In order to replace gate SiO_2 dielectric effectively, the alternative high-κ materials have to possess some required properties for the next generation. In this section, we are about to discuss the necessary conditions for this issue.

1.2.1 Dielectric Constant and Barrier Height

As previous discussion, high dielectric constant (High-κ) insulator could reduce the gate-leakage current because of its thick enough physical thickness. The range of dielectric constant is better between 20 and 80 due to fringing-induced barrier lowering (FIBL), and the EOT thinner than 1.0 nm is the best. This effect brings about the disadvantages of operating voltage lowering, slow device's driving speed and over high power consumption. [24]

For normal high-κ gate dielectric layers, the leakage mechanism is dominated by intrinsic properties and affected by extrinsic properties. The intrinsic properties of the insulator include the energy band gap (E_g), the dielectric constant (κ) and the conduction offset (ΔE_c). The extrinsic properties contain physical thickness, film morphology, the deposition methods, the environmental temperature and the applied electrical field on the insulator. Several mechanisms of basic electronic conduction in insulators are listed in table 1.2 [16]. Consequently, the direct tunneling current is markedly suppressed by increasing physical thickness and the conduction band offset.

1.2.2 Thermal Stability

In the early period, the high-κ metal oxide systems have unstable interfaces with silicon substrate (Si-sub) because the insulators would react with Si to form an unsuitable interfacial layers which will cause the reduced effective oxide thickness and degrade the carrier mobility [20]. Therefore, it is important to realize the thermodynamics of these systems and thereby try to prevent the formations of the interfaces with Si-sub.

Because Si-sub wafers will endure some high temperature processes after depositing high-κ dielectrics on Si-sub, the possible interfacial reactions between high-κ dielectric and Si-sub are given as the following:

$$Si + MO_x \rightarrow M + SiO_2 \quad (1\text{-}4)$$

$$Si + MO_x \rightarrow MSi_x + SiO_2 \quad (1\text{-}5)$$

$$Si + MO_x \rightarrow MSi_x + MSiO_x \quad (1\text{-}6)$$

$$Si + \text{stable } MO_x + O_2 \rightarrow \text{stable } MO_x + SiO_2 \quad (1\text{-}7)$$

(M: metal, MO_x: high-κ metal oxide, MSi_x: metal silicide, $MSiO_x$: metal silicate)

Although the interfacial metal-silicon products are usually detrimental to the gate oxide performance, the metal silicate shown in Eq. (1-6) is even helpful in some aspects. Taking HfO_2 and $HfSiO_4$ for instance, the interface and crystallization temperature of $HfSiO_4$ are sharper and higher than those of HfO_2, respectively [20][25].

In addition, Eq. (1-7) describes that excess oxygen atoms diffuse through the metal-oxide dielectric to the substrate and react with silicon at high temperature. This reaction produces unsatisfactory interfacial layer more easily in the ultrathin film regime. Hence, in order to precisely control the EOT of the high-κ dielectric and obtain better interface, we have to discover certain high-κ metal oxides which possess excellent thermal stability with Si-sub at high temperature.

1.2.3 Interface Quality

A definite goal of any potential high-κ gate dielectrics is to have a sufficiently high-quality interface with Si channel, as close as possible to that of SiO_2. The SiO_2 gate dielectric has a midgap interface state density $D_{it} \sim 2\times10^{10}$ states/cm^2 [16]. However, the most studied high-κ materials are proposed $D_{it} \sim 10^{11}$-10^{12} (states/cm^2), a order larger at $V_G = \pm1$

V without sensitive to temperature, and flat-band voltage shift ΔV_{FB} > 300 mV [20]. Therefore, it is the same important to choose better quality interface like that of SiO_2 and higher capacitance due to high-κ material.

1.2.4 Film Morphology

The works by Kuo-Hsing Kao *et al.* investigated the film morphology of high-κ dielectric $CoTiO_3$ and identify the relation between thin-film characterization and high temperature annealing [26]. There is no peak of crystalline $CoTiO_3$ in XRD spectrum observed before 700°C-annealing as shown in figure 1.5. Then, the crystallization of $CoTiO_3$ in SPM images starts to appear and the oxide grains grow up with increasing temperature as shown in figure 1.6. Because grain boundaries present as high leaky paths, it is expected to find a material which remains in an amorphous phase even if the film undergoes high temperature processes.

1.2.5 Process Compatibility

There are several investigated methods to form a high-κ gate dielectric as the following: 1) physical vapor deposition (PVD) [27]; 2) chemical vapor deposition (CVD) [28]; 3) molecular beam epitaxy (MBE) [29]; 4) sol-gel spin coating [26].

The mostly used PVD techniques are e-gun evaporator and sputtering. Although the two PVD methods could be operated at normal temperatures for unlimited substrate materials, the poor step coverage is the biggest challenge to be improved for depositing a uniform layer. However, the inevitable plasma damage leads to the surface damage and thereby produces unacceptable interfacial states [20].

CVD briefly contains metal organic chemical vapor deposition (MOCVD), jet vapor deposition (JVD) and atomic layer deposition (ALD). Although most of CVD methods have been proven to possess steeper step coverage, the ALD method seems to be more promising to

deposit better-quality high-κ gate dielectrics. Furthermore, the throughput and the requirements for instrument are considered particularly, so the ALD method is better than MOCVD and MBE methods [20].

1.3 Sol-Gel Spin Coating Method

In the recent years, many technologies have been proposed to form high-κ gate dielectrics, such as e-gun evaporator, sputtering, MOCVD, ALD, JVD and MBE. However, the sol-gel spin coating method still attracts much attention, and it is used to the high-κ gate dielectric films, memory charge trapping layers and active channel of oxide-based transistors as shown in figure 1.7 [26][30-33].

In the sol-gel processes, hydrolysis, condensation, and polymerization, the step-by-step formation causes a metal-oxide network. And there is an capturing feature of sol-gel spin coating method and an ability to compound into new types of high-κ materials, called "inorganic-organic hybrid" [34].

The sol-gel spin coating method could be executed easily in a normal pressure environment rather than in a high vacuum system, and the spin coating to form the thin-film structure is simpler than initial approaches mentioned because of its more low-priced precursors and instruments. The temperature of this method is low enough to be compatible with plastic substrates, and oxide-based semiconductors have been also applied to be active layers of thin-film transistors (TFTs) as shown in figure 1.8 [35-41].

This study principally makes use of the sol-gel spin coating method to form the high-κ gate dielectrics and we will apply this dip-coating method in the fabrication procedure of the polycrystalline silicon (poly-Si) TFTs.

1.4 Summary of Thin-Film Transistors

Although the concept of a thin-film field-effect transistor was presented as early as 1935 [42], the first functional thin-film transistor (TFT) was reported by P. K. Weimer in 1961 [43]. After that, TFTs have been intensively researched for possible electronic and display applications. The first active-matrix liquid-crystal display (AMLCD) was composed of CdSe TFTs and nematic liquid crystal [44]. Although there are many successful demonstrations of CdSe TFT LCDs, the industry production was retarded until the report on the feasibility of doping amorphous Si (α-Si) by the glow discharge technique in 1975 was introduced [45].

Since then, α-Si TFT LCDs have become the mainstream for mass-produced AMLCDs for several reasons. First, the characteristics of α-Si TFTs are remarkably well matched to the requirements of liquid-crystal driving, since they have a low off current with good on/off ratios. Second, both the gate insulator and the α-Si layers can be deposited in the same plasma-enhanced chemical vapor deposition (PECVD) system, so that contamination of the critical interface can be avoided. Eventually, α-Si TFTs can be made at low temperatures (250°C-350°C), thus allowing the use of inexpensive glass substrates [46].

Even if the α-Si TFTs possess aforementioned advantages, the most serious drawback is the low carrier mobility in the range of 0.5-1.0 cm^2/V-s. This makes α-Si TFTs sufficient only for switching devices for each pixel in a display, and cannot meet the desired specifications for high-resolution panels. In addition, the α-Si TFT is not compatible with the CMOS process.

The problem of the low carrier mobility in α-Si TFTs can be got over by introducing polycrystalline silicon (poly-Si) replacing α-Si as a semiconductor layer of TFTs. Besides the higher carrier mobility, there are several advantages of poly-Si TFT LCDs. First, the driver circuitry can be integrated on the display's substrate to realize the system on panels (SOP). Thus, the size of the total panel and cost, including drivers and related procedures, are

reduced compared to the α-Si TFT LCDs. Second, the driver contact number of the poly-Si TFT LCD is more than one order of magnitude smaller than that of the α-Si:H TFT LCD. Third, the poly-Si TFT plate has a smaller pixel size and larger aperture ratio in each pixel than that of the α-Si:H TFT plate. Higher mobility means that the pixel charging can be achieved by a smaller-size TFT, so that it contributes more pixel area for light transmission. Finally, TFT LCD with self-alignment and COMS process compatibility can be achieved [47][48].

Because the process of high-temperature poly-Si TFTs is as high as 900°C, the expensive quartz substrates are necessary. Due to the limited profitability of quartz substrate size, most typical applications for high-temperature poly-Si TFT-LCDs are panels for projection displays, because the panel size is limited to small sizes. For low-temperature poly-Si TFTs (LTPS TFTs), the maximum fabrication temperature is below 600°C and hence, low-cost glass substrates could be employed. This would bring about the production of large-area displays such as monitors and televisions [49]. Therefore, LTPS TFTs have attracted much attention due to their increasing application in high-resolution flat displays such as active-matrix liquid-crystal displays (AMLCDs) [50-54], active-matrix organic light-emitting diode (AMOLED) displays [55-58]. In addition, for the recent reported papers, ZnO is presently attracting much attention due to its possibilities for replacing α-Si that has been widely used as the channel layer in conventional TFTs [32][36][37][38].

Among the many barriers to the low-temperature process of LTPS TFTs, the formation of poly-Si films is the most important issue. There are several methods to fabricate a low-temperature poly-Si film, described as the following:

1.4.1 Solid-Phase Crystallization

Solid-phase crystallization (SPC) is usually performed at 600°C temperature annealing [59]. The SPC occurs through the processes of nucleation and grain growth, and both

processes are characterized by specific activation energies. For the SPC of α-Si by homogeneous nucleation, the activation energy of grain growth is less than that of nucleation [60]. Thereby, the amount of the nucleation relative to grain growth decreases with reducing annealing temperature. In order to enlarge the grain size, it is desirable to minimize the nucleation/grain growth ratio, and the SPC is typically done at a low temperature [61]. However, the SPC process is time-consuming about 20 hours for the crystallization of the α-Si film to the poly-Si film. Besides, such poly-Si films have a high density of intra-grain defects which lead to decrease the field-effect mobility and increase the threshold voltage of the TFTs [62].

1.4.2 Metal-Induced Lateral Crystallization

With some metals added to the α-Si films, the crystallization temperature can be lowered to below 600°C, and this phenomenon is known as metal-induced crystallization (MIC) [63]. Metals such as Au, Al, Sb and In, which form eutectics with Si, or metals such as Pd, Ti and Ni, which form silicides with Si, have been added to α-Si films to enhance the nucleation rate. During the MIC process, metal atoms dissolved in α-Si films may weaken Si bonds and enhance the nucleation of crystalline Si [64]. Some results were reported to be effective in lowering the crystallization temperature down to 500°C. However, an undesirable metal contamination at the channel region results in the poor electrical properties of the devices. A new method which can reduce metal contamination, called metal-induced lateral crystallization (MILC), has been reported for Pd, where large grains over several tens of microns are achieved [65]. Moreover, many groups have proposed TFTs to be successful in terms of device characteristics and mass productivity with MILC poly-Si, using pure Ni [66][67], Ge [61] and Ni-Co alloys [68].

1.4.3 Excimer Laser Annealing

Excimer laser annealing (ELA) is considered to be the most promising method for the fabrication of LTPS TFTs [69][70][71]. The ELA method is performed by melting α-Si with high-power pulsed laser irradiation. The irradiated α-Si film is then cooled and solidified as a crystal. During the melt-growth period, however, the solidification velocity is too high for the film to form nuclei and to grow sufficiently. For this reason, the grain size of the poly-Si film is not large enough. Besides, non-uniformity of grain size and narrow process window make it difficult to achieve uniform TFTs performance.

To realize this, some techniques such as the bridge method [72], low-temperature substrate heating during laser irradiation [73] and two-step laser crystallization [74] have been proposed to reduce the solidification velocity. In addition, for gaining higher mobility, lateral crystallization is one of the techniques used. The laser beam intensity is spatially modified over the α-Si to control the solid/liquid interface, causing lateral crystallization of the film. With this technique, the field-effect mobility of TFTs more than 300 cm^2/V-s can be achieved [75].

1.5 Plasma Treatment

According to Moore's law, the significant scale of the transistors is going to shrinking quickly. Nowadays in order to satisfy two requirements of high operating speed and high integrated density, introducing high-κ materials will be the best choice to replace the gate silicon dioxide layer in the future generations. Although high-κ materials improve many kinds of problems in reducing the thickness of the conventional gate silicon dioxide layer, oppositely it results several thorny questions to be resolved. The questions are as the following: 1) Low-κ interfacial layers are produced. When high-κ materials are deposited, oxygen diffuses the loose thin films. Then the oxygen would react with Si-sub to form low

quality silicon dioxide and/or metal oxides and limit the EOT scaling down. 2) There are amounts of fixed charges existing in high-κ thin films and resulting in threshold voltage shift to degrade the gate controllability. 3) Carrier mobility degrades. When high-κ thin film is deposited on the Si-sub surface, there are lots of dangling bonds produced from lattice mismatch. For this reason, the electrons moving in the channel are also affected by Coulomb's scattering, and the driving current degrades. 4) Crystallization temperature is low. The changed phase in high fabrication temperature makes thin films crystallize to increase the probability of leakage current and impurity penetration, e.g. boron penetration. Because of this, many groups suggested to insert a step of surface plasma treatment into the fabrication procedure.

In terms of electrical and optical properties of polycrystalline silicon thin-film transistors (poly-Si TFTs), grain boundaries and intragranular defects exert a profound influence on device characteristics and degrade carrier transport. These defects have been measured by electron spin resonance (ESR) and identified as silicon dangling bonds [76]. In order to obtain device-grade material, it is essential to minimize the dangling-bond density. Commonly, this is achieved by the incorporation of hydrogen which effectively passivates Si dangling bonds and thus improves the electrical properties of the material [77][78]. Afterward several groups proposed an oxygen plasma treatment of poly-Si TFTs which significantly improves the device performance. Furthermore, combinations of H_2 and O_2 plasma treatments to poly-Si TFTs were found to be more efficient than just a hydrogen or oxygen plasma [79][80][81]. Besides, the NH_3-plasma passivation was employed to enhance both the electrical reliability and the thermal stability of the poly-Si TFTs.

A hydrogenation process has been utilized to reduce the poly-Si film trap states to improve device performance. However, the poly-Si TFTs characteristics after hydrogen passivation suffer from serious instability issue due to weak Si-H bonds, causing inferior reliability for product applications. Accordingly, the NH_3-plasma passivation after gate oxide

deposition can improve the electrical properties of the poly-Si TFTs because of the passivation effect of hydrogen and nitrogen radicals [82][83][84]. In our study, we will apply the NH_3 plasma treatment to our fabrication procedure to compare with the poly-Si TFTs without this process, and the more detail results and discussion with this treatment will be demonstrated in the fourth chapter.

1.6 Polysilicon Thin-Film Transistors with High-κ Gate Dielectrics

As aforementioned in section 1.4, low-temperature polycrystalline silicon thin-film transistors (LTPS-TFTs) have been used for active-matrix liquid crystal displays (AMLCDs) and system on panel (SOP) on glass substrate as pixel switch devices and driving integrated circuits instead of amorphous silicon (α-Si), because the field effect mobility (μ_{FE}) in poly-Si is significantly higher than that in amorphous silicon. So that complementary metal-oxide-semiconductor (CMOS) devices with suitably high driving currents could be achieved in poly-Si TFTs. However, the highest temperature of TFTs fabrication procedure for the application of SOP is limited to the melting point of the glass substrate. Therefore, it is difficult to develop high-performance LTPS-TFTs with low threshold voltage (V_{TH}), low subthreshold swing (*S.S.*), low gate leakage current (I_G) and high driving current ($I_{D,sat}$) to drive the liquid crystal of the large area panel, and these electrical properties have to be necessary urgently to the next generation. In order to enhance the driving current of poly-Si TFTs and break through this challenge, a thinner gate oxide must be used to increase the gate capacitance density. However, a higher gate leakage current would be introduced when the thickness of the gate oxide becomes thinner. Besides, low quality silicon dioxide (SiO_2) deposited by using a low-temperature manufacture instrument, plasma-enhanced chemical vapor deposition (PECVD), is generally employed as a gate dielectric of the traditional LTPS-TFTs. To compare with low quality SiO_2, high-κ gate dielectrics could possess better

quality and be more proper to replace the conventional low-temperature SiO_2. Many high-k materials have been used to suppress the gate leakage current and to enhance the transconductance (G_m). Among these dielectric materials, $NiTiO_3$ could be the promising candidate of the future high-κ gate dielectric because of its high permittivity (κ ~ 40). In the following chapters, poly-Si TFTs with a $NiTiO_3$ gate dielectric prepared by sol-gel spin coating method will be introduced particularly.

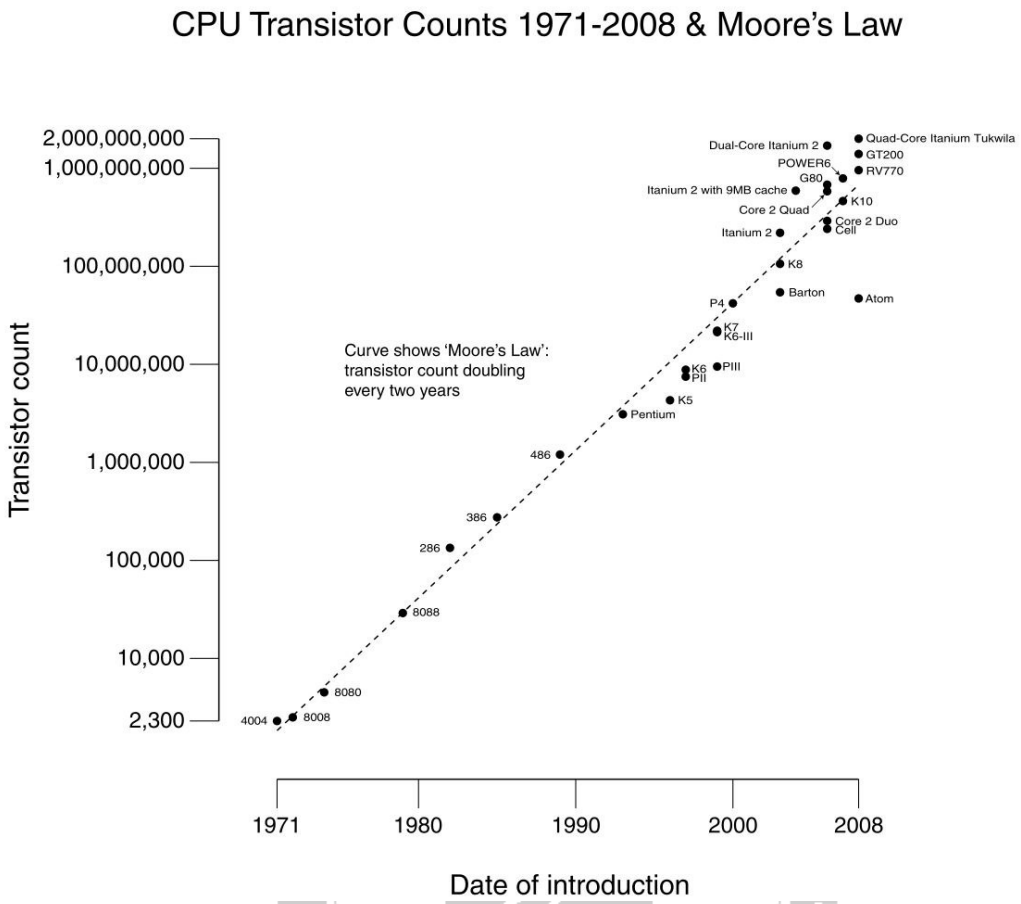


Figure 1.1 Transistor counts for integrated circuits plotted against their dates of introduction. Curve shows Moore's law - the doubling of transistor counts every two years.

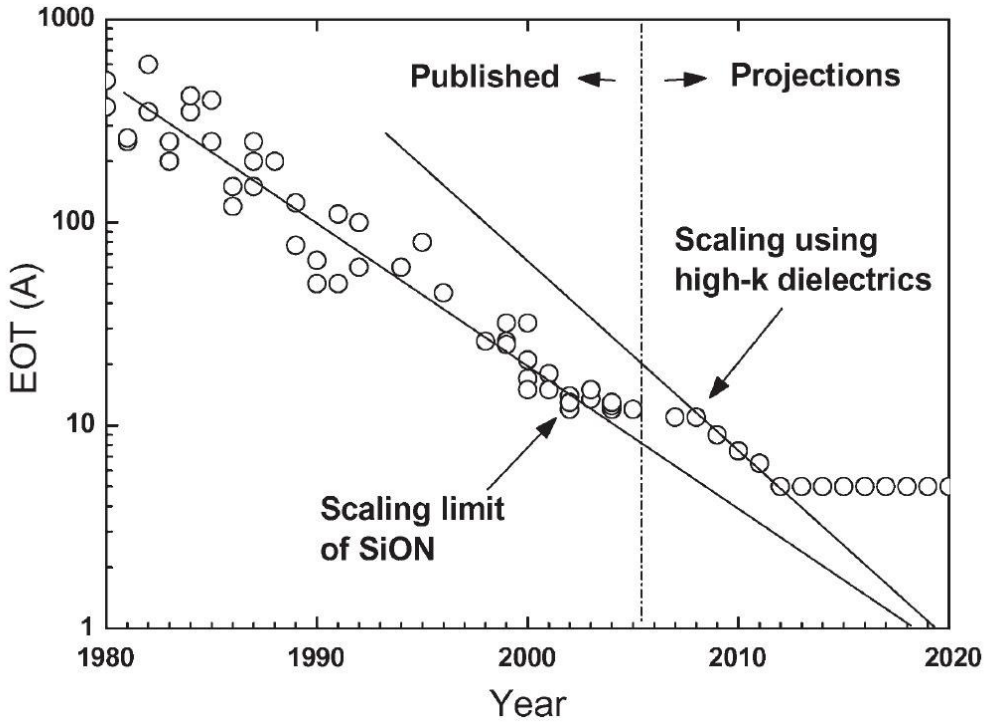


Figure 1.2 Trend of gate-oxide-thickness scaling over the past five technology generations from the 0.18-μm to 65-nm nodes.

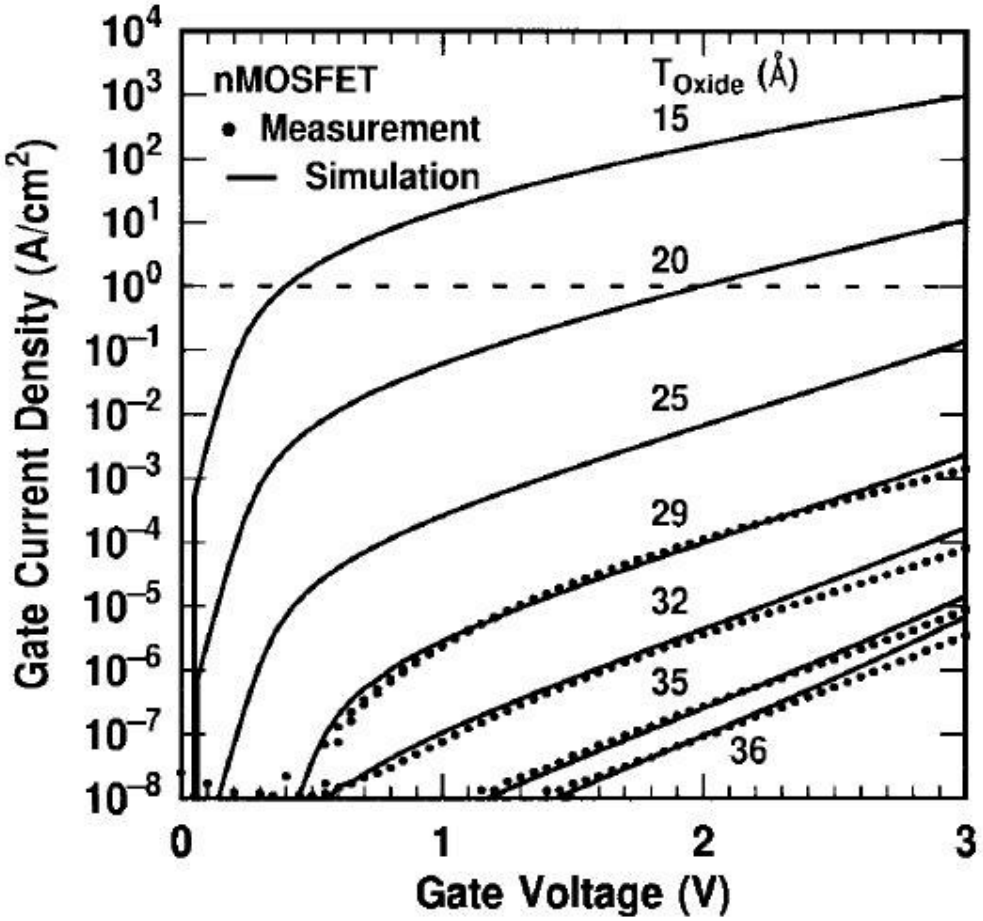


Figure 1.3 Measurement and simulation of direct tunneling currents under inversion conditions of nMOSFET's.

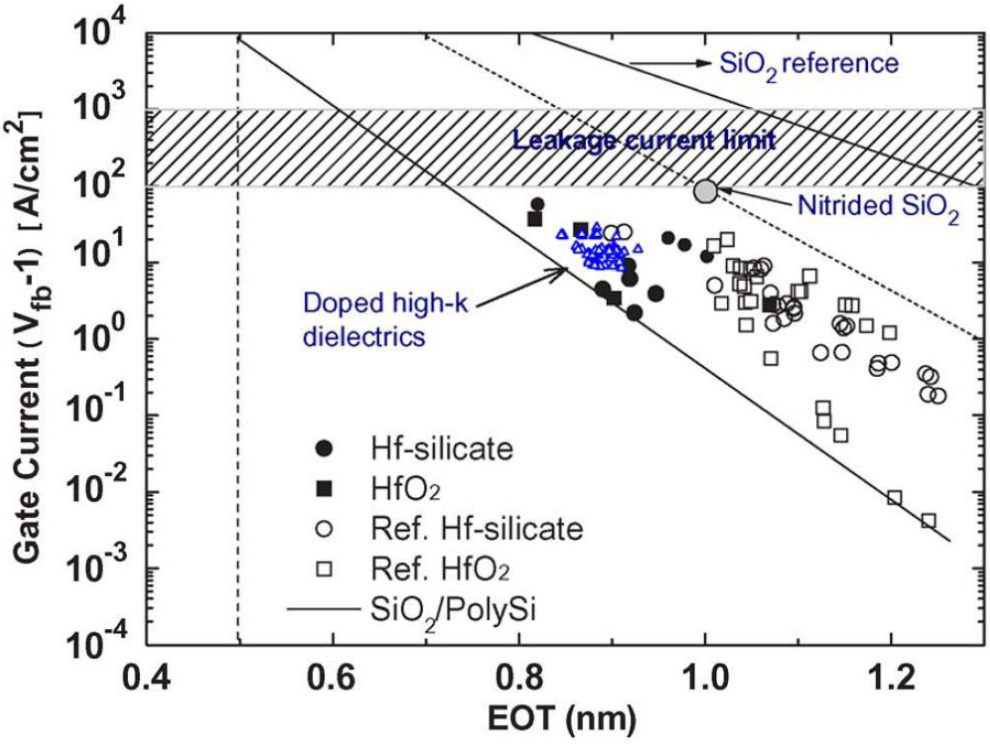


Figure 1.4 Leakage-current values of various high-κ dielectrics at subnanometer EOT. The leakage current was measured at accumulation (V_{fb} − 1 V) in the nMOS devices.

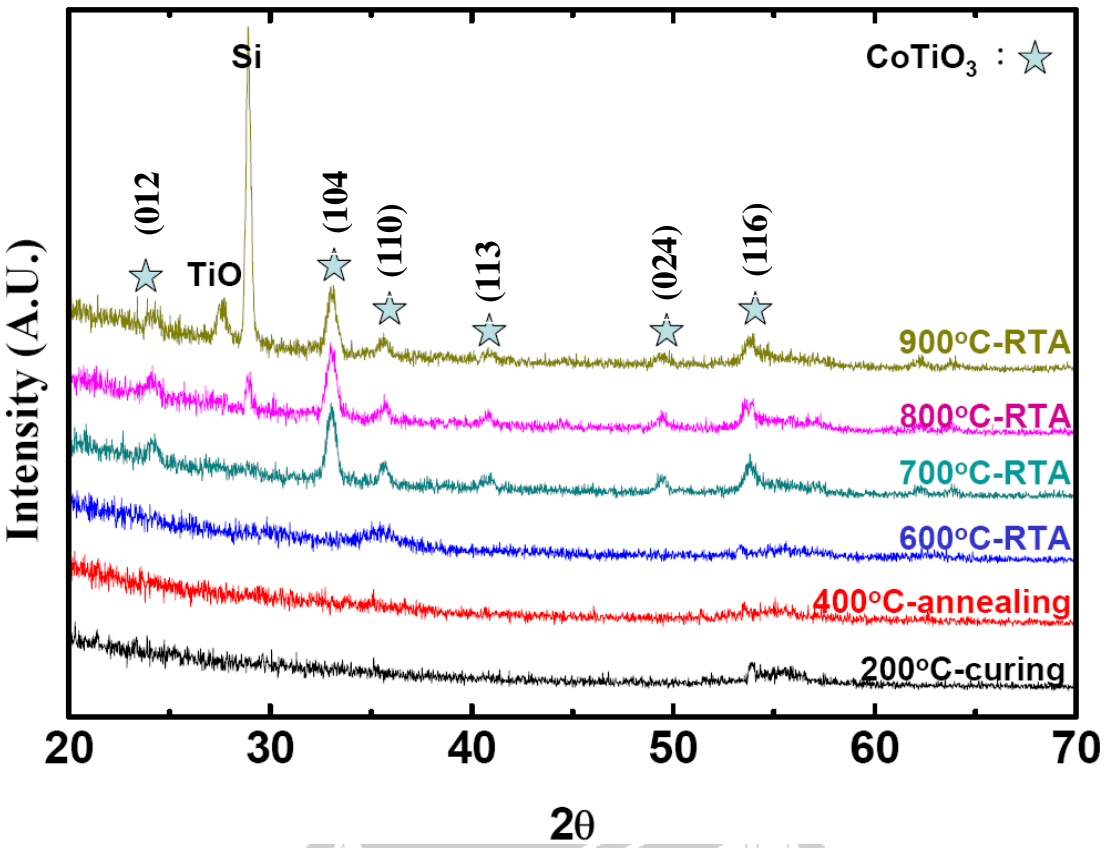


Figure 1.5 XRD spectrum of spin-on $CoTiO_3$ films. The marked peaks correspond to crystallized $CoTiO_3$ phases.

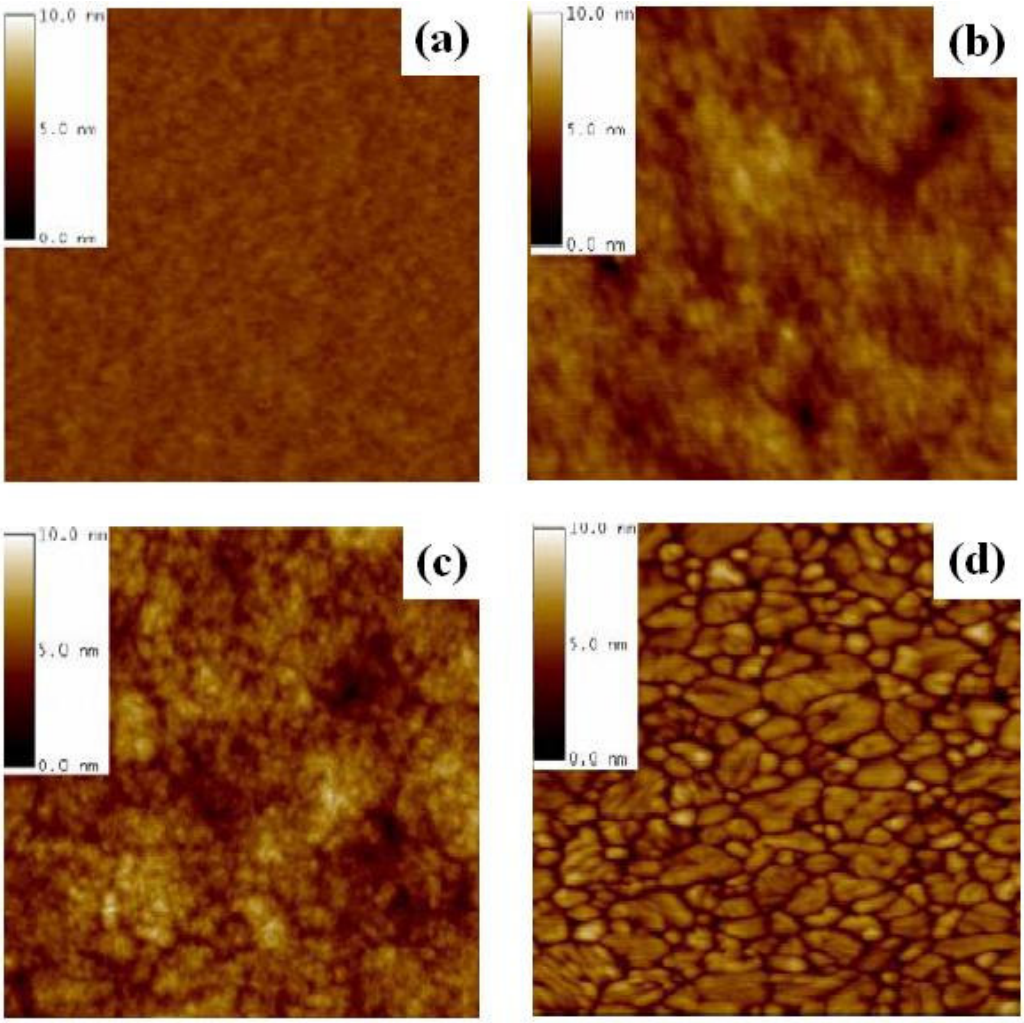


Figure 1.6 SPM images of spin-on $CoTiO_3$ films with various thermal treatments at (a)600°C, (b)700°C, (c)800°C, (d)900°C. The image size is 1 μm by 1 μm.

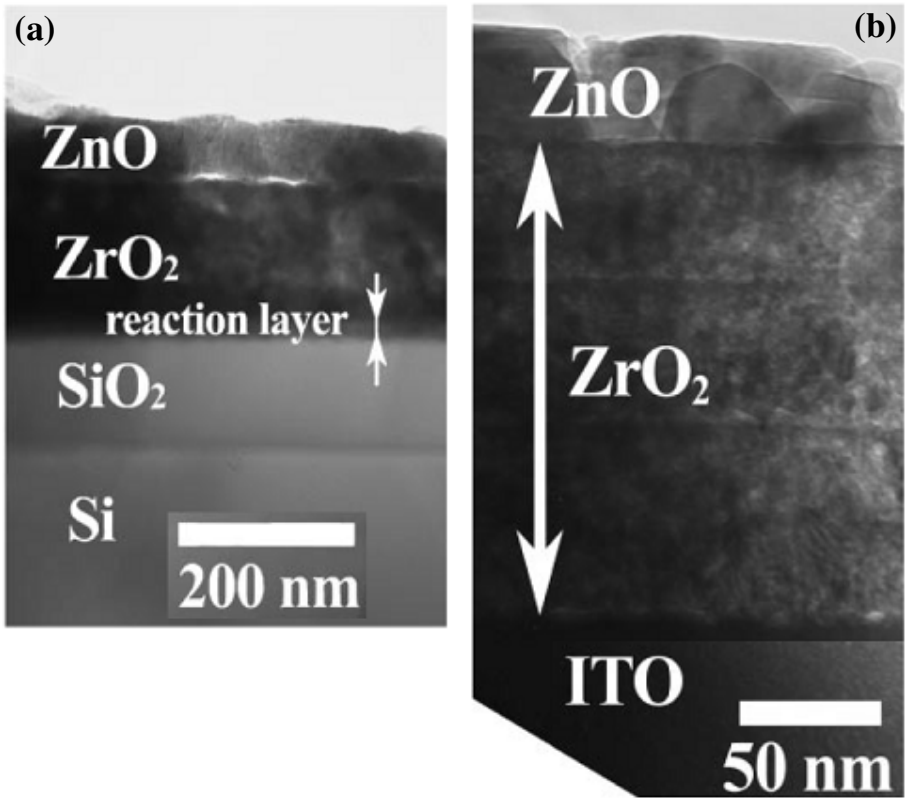


Figure 1.7 Transmission electron micrograph of (a) $ZnO/ZrO_2/SiO_2/Si$ multilayered film heated at 900°C and (b) $ZnO/ZrO_2/ITO/glass$ multilayered film heated at 600°C.

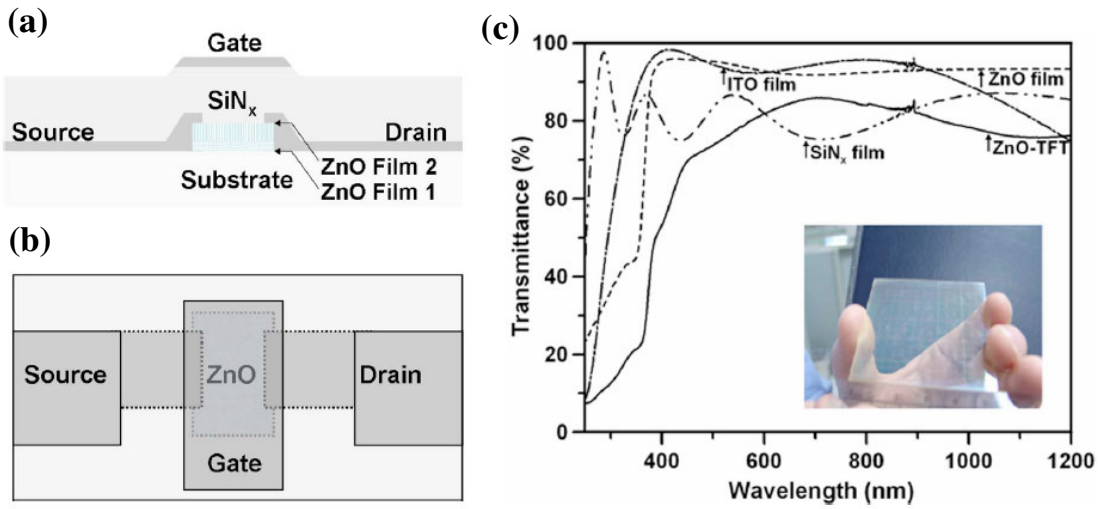
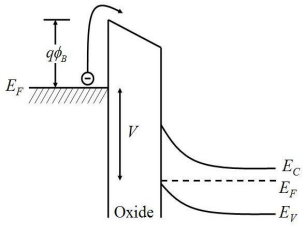
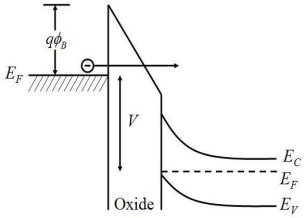
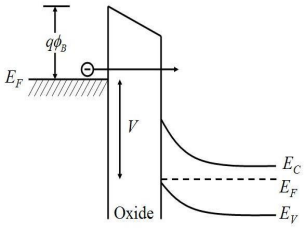
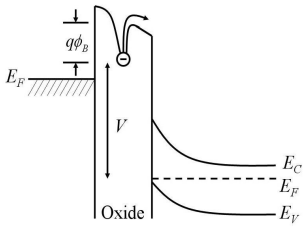
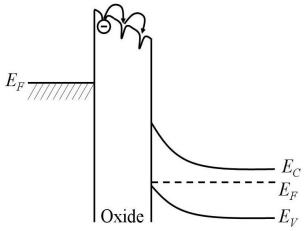
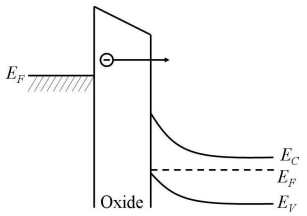


Figure 1.8 Top-gate structure of ZnO-TFT in (a) crosssectional schematic, (b) top view schematic and (c) optical transmission spectra.

Table 1.1 High-κ gate dielectric materials with a dielectric constant reported in the literatures.

Material	ε	Material	ε	Material	ε
Al_2O_3	8-11.5	$LaAlO_3$	23.8-27	TaON	
$Al_xSi_yO_z$		$LaLuO_3$	32	Ta_2O_5-TiO_2	
(Br, Sr)TiO_3	200-300	$LaScO_3$	22-30	TiO_2(rutile)	86-95
$BeAl_2O_4$	8.3-9.43	La_2O_3-SiO_2	5-16	TiO_2-SiO_2	
CeO_2	16.6-26	$MgAl_2O_4$	8.3-9.4	TiO_2/Si_3N_4	
$CeHfO_2$	10-20	Pr_2O_3	14.9	Y_2O_3	8-11.6
$CoTiO_3$	45-50	$PrAlO_3$	25	$Y_xSi_yO_z$	
$DyScO_3$	22	$NdAlO_3$	22.5	ZrO_2	22.2-28
$EuAlO_3$	22.5	Sc_2O_3	13	Zr-Al-O	12-18
$GdScO_3$	22	Si_3N_4	7	Zr silicate	11-12.6
HfO_2	26-30	$SmAlO_3$	19	(Zr, Hf)$SnTiO_4$	40-60
Hf silicate	11	$SrTiO_3$	150-250	Ta_2O_5-TiO_2	
La_2O_3	18-20.8	Ta_2O_3	25-45	Y_2O_3	8-11.6

Table 1.2 Conduction mechanism in insulator with expression and band diagram.

Mechanism	Expression	Band Diagram
Schottky Emission	$J \propto T^2 \exp\left[\frac{q}{kT}\left(a\sqrt{V}-\phi_B\right)\right]$	
Fowler-Nordheim Tunneling	$J \propto V^2 \exp\left(-\frac{b}{V}\right)$	
Direct Tunneling	$J_{DT} \propto \exp\left(-2t_d\sqrt{\frac{2m^*q}{\hbar^2}\left\{\Phi_B-\frac{V_d}{2}\right\}}\right)$	
Frenkel-Poole Emission	$J \propto V \exp\left[\frac{q}{kT}\left(2a\sqrt{V}-\phi_B\right)\right]$	
Hopping (Ohmic) Conduction	$J \propto V \exp\left(-\frac{c}{T}\right)$	
Ionic Conduction	$J \propto \frac{V}{T}\exp\left(-\frac{d}{T}\right)$	

Chapter 2

Experiment Procedures

In this chapter we will illustrate the device fabrication processes of capacitors and polycrystalline-silicon thin-film transistors (poly-Si TFTs) with figures and list the instruments for material and physical properties measurements.

2.1 Device Fabrication

2.1.1 Capacitors

In this thesis, $NiTiO_3$ films were formed by a sol-gel spin coating method in a controlled surroundings, where was kept at temperature of 22°C and relative humidity of 43%. In the beginning, (100) p-type single crystal silicon wafers with resistivity in the range of 1-10 Ω-cm were prepared as substrates. Firstly, the bare silicon wafers were cleaned by standard RCA steps followed by a dilute-HF dip to remove the native silicon dioxide. Then, the liquid precursor for $NiTiO_3$ was directly spun on Si substrates at about 3000 revolutions per minute, and the spin speed was maintained for 30 seconds. However, the precursor elements of nickel and titanium were nickel acetate tetrahydrate $Ni(OOCCH_3)_2 \cdot 4H_2O$ and titanium isopropoxide $Ti(OCHC_2H_6)_4$, respectively. These two precursors were dissolved in 2-methoxyethanol for the spin coating method. After the precursor was spun on substrates, in order to remove the solvent, the samples were baked step by step at different curing temperatures in atmosphere on a hotplate as shown in figure 2.1. And the procedure (coating-and-baking) was repeated for 5 times due to for poly-Si TFTs fabrication. Then, the spin-on $NiTiO_3$ films were oxidized at 400°C in N_2/O_2 ambient with 50-sccm airflow for 10 min. In order to investigate the characteristics of the high-κ $NiTiO_3$ material as gate dielectric after high temperature

treatment, rapid thermal annealing (RTA) was performed. The samples were annealed at temperatures of 500°C, 600°C, 700°C, 800°C, and 900°C for 30 seconds in N_2 ambient. Photolithography was used to define gate areas and then TaN metal was deposited on the top of the samples by reactive DC-sputtering. Lift-off was performed to fabricate the MIS capacitors. Finally, ohmic contacts were formed by thermal evaporation of 300-nm-thick aluminum (Al) electrode on the backside of the samples. The process flow of a capacitor was shown in figure 2.2.

2.1.2 Polycrystalline-Silicon Thin-Film Transistors

In this section, we will make a description on the process flow of thin-film transistors with sol-gel spin coating $NiTiO_3$ films and the main fabrication steps were summarized as shown in figure 2.3. In the beginning, all wafers proceeded from using the traditional RCA cleaning to remove any contaminations, native oxide, and atomic scale roughness. Subsequently, a 500-nm thermal oxide grown on 6-inch silicon wafers by using a horizontal furnace was used to simulate the glass substrate of the active matrix liquid crystal display (AMLCD). And then, an undoped amorphous silicon (α-Si) film with a 50-nm thickness was deposited on the 500-nm thermal oxide by using a low-pressure chemical vapor deposition (LPCVD) system in silane (SiH_4) ambient with a pressure of 350 mtorr at 560 ℃ as shown in figure 2.3(a). After a 24-hour annealing at 600°C by using the conventional solid-phase crystallization (SPC) method due to its low-production cost and good grain-size uniformity, amorphous silicon became to poly-crystalline silicon (poly-Si). Active area region was patterned by photolithography and then source/drain region were formed by using BF_2 ion implantation as shown in figure 2.3(b). The following steps were to spin $NiTiO_3$ material as a gate dielectric on poly-Si films by using the sol-gel spin coating method for 5 times as the aforementioned step. Then, the spin-on $NiTiO_3$ films were oxidized at 400°C in N_2/O_2 ambient by using a horizontal furnace with 50-sccm airflow for 10 min, and afterward the

samples were just annealed at 500°C, 600°C, and 700°C for 30 seconds in N_2 ambient. A 200-nm-thickness TaN metal was deposited on the top of the samples by reactive DC-sputtering at 600 mtorr with a DC power of 1500 watt and patterned as the gate electrode by photolithography as shown in figure 2.3(c). A 400-nm tetraethoxylsilane (TEOS) oxide film used as an inter-layer dielectric (ILD) layer was deposited by using a plasma-enhanced chemical vapor deposition (PECVD) system at 300°C. Then contact holes were opened and etched by by using a buffered oxide etching (BOE) solution as shown in figure 2.3(d). Aluminum (Al) electrode with 600-nm thickness was deposited by e-gun evaporator, and then the aluminum pads were lithographically patterned. Subsequently, metal pads were etched by using a TCP metal etcher, and thus the poly-Si TFTs with a high-κ $NiTiO_3$ gate dielectric prepared by sol-gel spin coating method were accomplished as shown in figure 2.3(e). Eventually, an NH_3 plasma treatment was performed at 350°C for 30 min for partial samples, which were the poly-Si $NiTiO_3$ TFTs with a 500°C-RTA treatment after the Al gate electrode formation in order to compare to the samples without NH_3 plasma treatment.

2.2 Material and Physical Properties Measurements

The microstructure of spin-on $NiTiO_3$ films and silicon substrate were investigated by JEOL JEM-2010F field emission transmission electron microscope (TEM) equipped with Link ISIS-300 energy dispersive X-ray analyzer (EDS). And the TEM EDS with a 0.23-nm electron beam size was used to perform chemical analysis qualitatively.

The property of crystallization of spin-on $NiTiO_3$ film with different annealing temperatures was identified by PANalytical X'Pert Pro X-ray diffraction system under normal atmosphere. Optical module with X-ray mirrors and a parallel plate collimator was used to perform gracing incident X-ray diffraction (angle of incidence $\theta_i \sim 1^\circ$). The beam source originated from Cu $K\alpha$ radiation with a 0.154-nm wavelength and this beam source was

operating at 1.8 kW.

Surface morphology of spin-on $NiTiO_3$ film with different annealing temperatures was obtained by Veeco multimode scanning probe microscope (MMAFM) at normal atmosphere. The highest resolution in X-Y plane and Z direction were about 1.5 nm and few angstroms, respectively. And the tip curvature radius was about 2 nm.

A ULVAC-PHI Quantera high resolution X-ray photoelectron spectrometer (HR-XPS) with 180° spherical capacitor analyzer was used to analyze quantitatively the chemical composition of the dielectrics $NiTiO_3$ prepared by sol-gel coating method.

The capacitance-voltage (*C-V*) curves and current-voltage (*I-V*) curves of capacitors were measured in the same probe station by using HP 4284 and Keithly 4200, respectively.

2.3 Equation Derivation and Electrical Parameters Extraction

In this section, we firstly formulate a general drain current for thin-film transistor by using gradual channel approximation (GCA) model, which the variation of the electrical field along the channel is much less than the corresponding variation perpendicular to channel. Hence, the inversion charges density (Q_{inv}) could be simplified to the 1-D form of Possion's equation. The current-voltage characteristic of the thin-film transistor could be calculated by estimating the elemental resistance *dR* and the elemental segment *dy* of the conducting channel given by

$$dV = I_{DS}dR = I_{DS}\frac{dy}{W\mu_{EF}|Q_{inv}(y)|} \tag{2-1}$$

, where *W* is the channel width and μ_{EF} is the field-effect mobility. Then, integrate Eq. (2-1) from source (*V=0* at *y=0*) to drain (*V=*V_{DS} at y=*L*). The drain current could be expressed as

$$\int_0^L I_{DS}dy = \mu_{FE}W\int_0^{V_{DS}}|Q_{inv}|dV \quad \rightarrow \quad I_{DS} = \mu_{FE}\frac{W}{L}\int_0^{V_{DS}}|Q_{inv}|dV\ . \tag{2-2}$$

Following, we use the charge-sheet approximation model, which assumes that the inversion charges (Q_{inv}) are located at the silicon surface as a sheet of charges with no potential dropping or band bending across the inversion layer, to derive drain current as

$$Q_{inv} = Q_S - Q_{dep} = -C_{ins}\left(V_{GS} - V_{fb} - 2\psi_B - V\right) + \sqrt{2\varepsilon_{Si} q N_B \left(2\psi_B + V\right)} \tag{2-3}$$

, where Q_S is the total surface charge density, Q_{dep} is the depletion charge density, V_{fb} is the flat band voltage, the surface potential ψ_S is pinned at $\psi_S = 2\psi_B + V(y)$, C_{ins} is the gate capacitance density of insulator layer, ε_{Si} is the dielectric constant of silicon, and N_B is the effective channel dpoant in active channel of the thin-film transistor. Substituting Eq. (2-3) into Eq. (2-2) and carrying out the integration, the drain current (I_{DS}) could be presented by

$$I_{DS} = \mu_{FE}\frac{W}{L}\int_0^{V_{DS}} |Q_{inv}| dV = \mu_{FE} C_{ins}\frac{W}{L}\left\{\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{m}{2}{V_{DS}}^2\right\} \tag{2-4}$$

, where the body-effect coefficient m and the threshold voltage V_{TH} are

$$m = 1 + \frac{\sqrt{\varepsilon_{Si} q N_B / 4\psi_B}}{C_{ins}} \text{ and } V_{TH} = V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{Si} q N_B \psi_B}}{C_{ins}}, \text{ respectively.} \tag{2-5}$$

When the device works in saturation region, the I_{DS} is independent on V_{DS}, which means

$$\frac{dI_{DS}}{dV_{DS}} = \left(V_{GS} - V_{TH}\right) - mV_{DS} = 0 \;\rightarrow\; V_{DS} = V_{DS,sat} = \left(\frac{V_{GS} - V_{TH}}{m}\right). \tag{2-6}$$

Substituting Eq. (2-6) into Eq. (2-4), the saturation current $I_{DS,sat}$ could be written as

$$I_{DS,sat} = \mu_{FE} C_{ins}\frac{W}{L}\frac{\left(V_{GS} - V_{TH}\right)^2}{2m} \tag{2-7}$$

In $m = 1$ case, the Eq. (2-4) and Eq. (2-7) could be simplified by

$$I_{DS,lin} = \mu_{FE} C_{ins}\frac{W}{L}\left[\left(V_{GS} - V_{TH,lin}\right)V_{DS} - \frac{1}{2}{V_{DS}}^2\right] \quad \text{for linear operation} \tag{2-8}$$

and

$$I_{DS,sat} = \frac{1}{2}\mu_{FE} C_{ins}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \quad \text{for saturation operation, respectively.} \tag{2-9}$$

Secondly, we will introduce the extractions of the device electrical parameters. An automatic measurement system, ICS software, combined a personal computer (PC), Agilent-4156 semiconductor parameter analyzer, Agilent-4285 precision LCR meter, Agilent E5250A low leakage switch mainframe, and a probe station is used to measure the drain-source current versus gate-source voltage (I_{DS}-V_{GS}) curves and the drain-source current versus drain-source voltage (I_{DS}-V_{DS}) curves of the fabricated thin-film transistors. The electrical parameters of thin-film transistors, for examples on the threshold voltage (V_{TH}), the subthreshold swing (*S.S.*) and the field-effect mobility (μ_{FE}), are also extracted to estimate the benefits of integrating high-κ $NiTiO_3$ gate dielectric or nitrogen incorporation.

According to the thin-film transistor theory described in Eq. (2-8), in the linear regime, $V_{DS} < V_{GS} - V_{TH,lin}$, and the drain current ($I_{DS,lin}$) could be described as

$$I_{DS,lin} = \mu_{FE} C_{ins} \frac{W}{L}\left(V_{GS} - V_{TH,lin}\right)V_{DS} \tag{2-10}$$

Thus, the transconductance (G_m) in the linear regime is given by

$$G_m = \frac{\partial I_{DS,lin}}{\partial V_{GS}} = \mu_{FE} C_{ins} \frac{W}{L} V_{DS} \tag{2-11}$$

Therefore, the field-effect mobility in the linear regime ($\mu_{FE,lin}$) could be obtained as

$$\mu_{FE,lin} = \frac{L}{W}\frac{1}{C_{ins}}\frac{1}{V_{DS}} G_m \Big|_{V_{DS}\sim 0.1V} \tag{2-12}$$

, where the drain-source voltage (V_{DS}) is usually set at 0.1 V. Because the inversion carriers in the active channel layer could be easily drained out with enough high carrier mobility at low drain bias, we calculate the field-effect mobility in the linear regime ($\mu_{FE,lin}$) for low-temperature polycrystalline silicon (LTPS) TFT device. The transfer curve of LTPS TFT device, drain current ($I_{DS,lin}$) versus gate-source voltage (V_{GS}), is measured at V_{DS} = 0.1 V, and then $\mu_{FE,lin}$ could be obtained by using Eq. (2-12).

For extraction convenience, the threshold voltage (V_{TH}) is defined as the gate voltage required a normalized drain current of $I_{DS,N}$ = *(W/L)* × 100 nA at V_{DS} = 0.1 V. The ON/OFF

current ratio ($I_{ON,\,max}/I_{OFF,\,min}$) and the subthreshold swing (*S.S.*) present the switching and the gate-controlled capabilities of TFT device, respectively. In this work, the ON/OFF current ratio of LTPS TFT device is defined as that ratio of the maximum on-state current to the minimum off-state current at V_{DS} = 1 V. The subthreshold swing is measured at the inverse of the maximum slope in the plot of drain current (in denary logarithm) versus gate-source voltage (V_{GS}).

By integrating the depletion charges (Q_{dep}) in active channel with the charge-sheet approximation , the subthreshold current ($I_{DS,SUB}$) in the subthreshold region (at a small V_{DS} ~ 0.1 V) could be derived as the following equation:

$$I_{DS,SUB} = \mu_{FE} C_{ins} \frac{W}{L} \sqrt{\frac{q\varepsilon_{Si} N_B}{2\psi_S}} \left(\frac{k_B T}{q}\right)^2 \left(\frac{n_i}{N_B}\right)^2 \exp\left(\frac{q\psi_S}{k_B T}\right) \tag{2-13}$$

, where the surface potential ψ_S could be expressed in terms of V_{GS}

$$V_{GS} = V_{fb} + \psi_S + \frac{\sqrt{2\varepsilon_{Si} q N_B \psi_S}}{C_{ins}}. \tag{2-14}$$

Considering $\psi_S \sim 2\psi_B$ in the subthreshold region, the Eq. (2-14) could be expand to the square-root term around $2\psi_B$ as

$$V_{GS} = V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{Si} q N_B \psi_B}}{C_{ins}} + \left(1 + \frac{\sqrt{\varepsilon_{Si} q N_B / 4\psi_S}}{C_{ins}}\right)\left(\psi_S - 2\psi_B\right) = V_{TH} + m\left(\psi_S - 2\psi_B\right) \tag{2-15}$$

, where the body-effect coefficient m is

$$m = 1 + \frac{\sqrt{\varepsilon_{Si} q N_B / 4\psi_S}}{C_{ins}} = 1 + \frac{C_{dep}}{C_{ins}} \tag{2-16}$$

and C_{dep} is the depletion capacitance density. Substituting Eq. (2-16) into Eq. (2-13) yields the subthreshold current as a function of V_{GS}

$$I_{DS,SUB} = \mu_{FE} C_{ins} \frac{W}{L}(m-1)\left(\frac{k_B T}{q}\right)^2 \exp\left(\frac{q\left(V_{GS} - V_{TH}\right)\psi_S}{m k_B T}\right). \tag{2-17}$$

Consequently, the subthreshold swing (*S.S.*) could be presented following equation:

$$S.S. = \left[\frac{d \log_{10} I_{DS,SUB}}{dV_{GS}} \right]^{-1} = 2.3 \frac{mk_B T}{q} = 2.3 \frac{k_B T}{q} \left(1 + \frac{C_{dep}}{C_{ins}} \right). \quad (2\text{-}18)$$

If we consider the effective interface trap-state densities $N_{it} = qC_{it}$ substituting into Eq. (2-18), the subthreshold swing (*S.S.*) neglected the depletion charges ($Q_{dep} = q \times C_{dep}$) could be rewritten as

$$S.S. = \left[\frac{d \log_{10} I_{DS,SUB}}{dV_{GS}} \right]^{-1} = 2.3 \frac{k_B T}{q} \left(1 + \frac{C_{dep} + C_{it}}{C_{ins}} \right) \sim 2.3 \frac{k_B T}{q} \left(1 + \frac{qN_{it}}{C_{ins}} \right). \quad (2\text{-}19)$$

Therefore, the maximum interface states density ($N_{SS,max}$) presents the interface quality between the dielectric and the active channel layer of TFT device could be calculated from the *S.S.* without the depletion capacitance as

$$N_{SS,\max} = \left[\frac{S.S.}{2.3} \left(\frac{q}{k_B T} \right) - 1 \right] \left(\frac{C_{OX}}{q} \right). \quad (2\text{-}20)$$

In pentacene-based organic TFT device case, because its inversion carriers in the active channel could not be easily drained out the device with a low carrier mobility at a low drain bias, its parameters are usually extracted in the saturation regime ($V_{DS} > V_{GS} - V_{TH}$) as

$$I_{DS,sat} = \frac{1}{2} \mu_{FE} C_{ins} \frac{W}{L} \left(V_{GS} - V_{TH} \right)^2. \quad (2\text{-}21)$$

The Eq. (2-21) could be transposed by V_{GS} as

$$V_{GS} = V_{TH} + \sqrt{2I_{DS,sat}} \sqrt{\frac{L}{\mu_{FE} C_{ins} W}}. \quad (2\text{-}22)$$

Hence, the threshold voltage (V_{TH}) could be determined from the maximum slope in the square-root plot ($I_{DS}^{1/2}$–V_{GS}) of the transfer characteristic and we fit a straight line to the $I_{DS}^{1/2}$–V_{GS} curve at the point extrapolated to I_{DS} = 0. Following, substitute the obtained V_{TH} from Eq. (2-22) back into Eq. (2-21), and then the field-effect mobility in the saturation regime ($\mu_{FE,sat}$) of the organic TFT device could be obtained as

$$\mu_{FE,sat} = 2I_{DS,sat}\frac{L}{C_{ins}W}\frac{1}{(V_{GS}-V_{TH})^2}. \quad (2\text{-}23)$$

Strictly speaking, the Eq. (2-23) is valid only when the mobility is constant. In fact, $\mu_{FE,sat}$ is dependent on the gate-source bias (V_{GS}). The Eq. (2-23) is only used for estimating an approximated value for the field-effect mobility calculation of organic TFT devices.

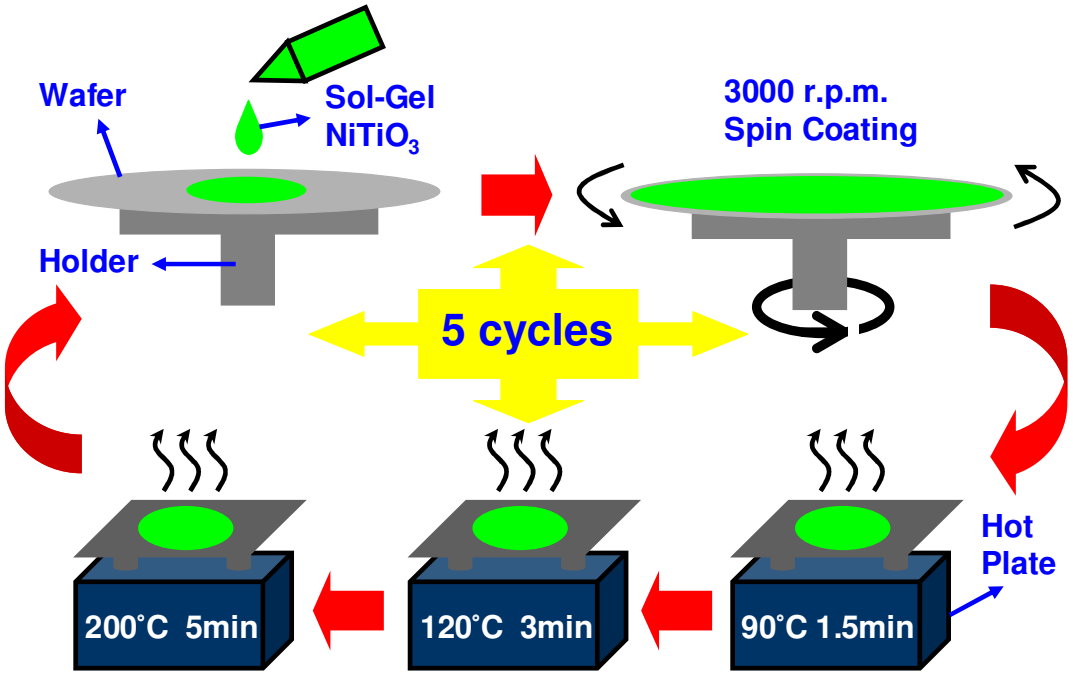


Figure 2.1 The process flow of the sol-gel spin coating method to form a high-κ $NiTiO_3$ film.

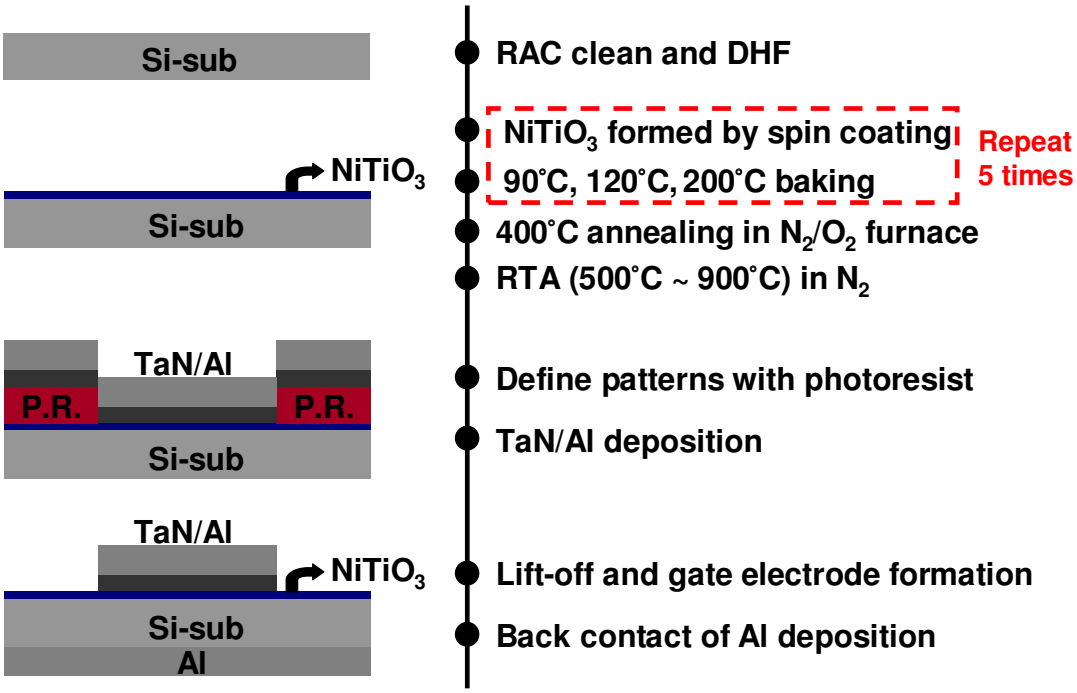
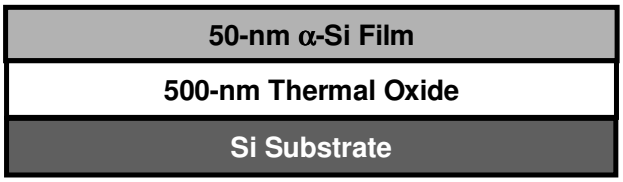
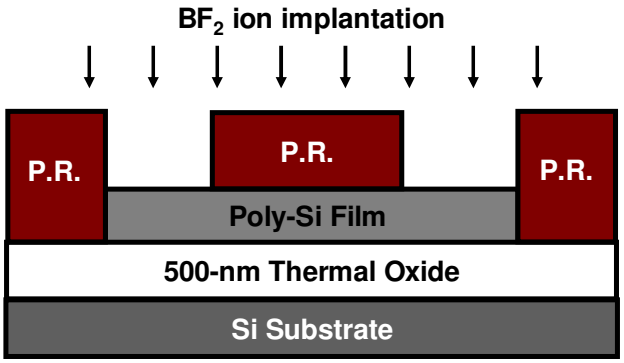


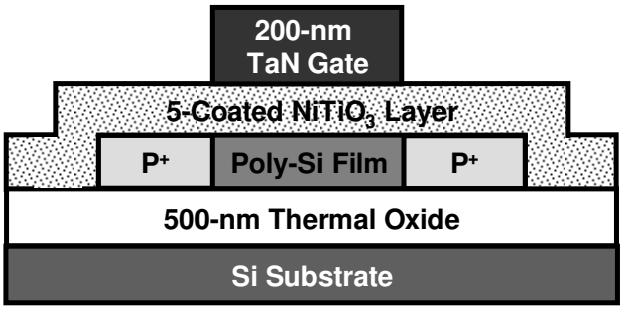
Figure 2.2 The main process flow of sol-gel spin coating method to form a $NiTiO_3$ capacitor.



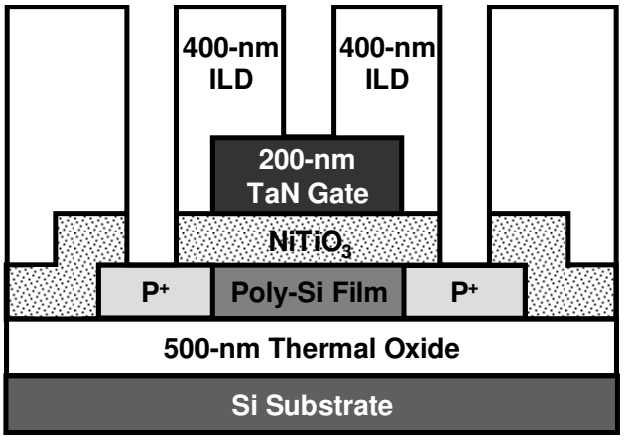
(a) Thermal oxidation, α-Si film deposition.



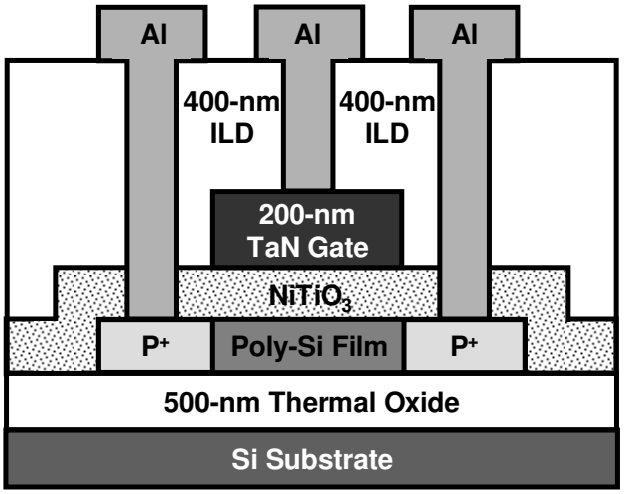
(b) SPC annealing, active region patterning, source and drain ion implantation.



(c) Source and drain activation, 5-coated $NiTiO_3$ layer formed, and TaN metal deposition and patterning as a gate electrode.



(d) ILD layer deposition and contact holes opening.



(e) Al metal deposition and patterning as metal pads.

Figure 2.3 The main process flow of the thin-film transistor with sol-gel spin coating $NiTiO_3$ films.

Chapter 3

Material and Physical Characteristics of Capacitors

In this chapter, we will firstly report the material characteristics of spin-on $NiTiO_3$ thin films analyzed by High-Resolution Transmission Electron Microscope (HR-TEM), Grazing Incident X-Ray Diffraction (GI-XRD), Scanning Probe Microscope (SPM), Auger Electron Microscope (AEM), and Electron Spectroscopy for Chemical Analysis (ESCA). Afterward we will report the physical characteristics of that such as dielectric permittivity, *C-V* and *I-V* properties.

3.1 Surface Morphology

As mentioned in section 1.2.4, it is common that the surface morphology of high-κ dielectric is still flat even if it undergoes high temperature treatment. PANalytical X'Pert Pro X-ray diffraction system and Veeco Dimension 5000 Scanning Probe Microscope (D5000) are used to analysis surface morphology of films after different high temperature annealing.

Figure 3.1 gives the GI-XRD spectrum of the $NiTiO_3$ thin films with different temperature treatments. There are no marked signals to be detected for samples which are treated at temperatures below 700°C, and this phenomenon displays that spin-on $NiTiO_3$ films are amorphous phases initially. Consequently, the samples are annealed at temperatures above 700°C, and signals of crystallized $NiTiO_3$ phases are exhibited. This suggests the crystallization temperature of spin-on $NiTiO_3$ films begin between 600 ~ 700°C.

Figure 3.2 to figure 3.8 present the SPM images of $NiTiO_3$ films with different high temperature treatments. From figure 3.2 to figure 3.8 are the flatten and 3-D images of samples which are baked or annealed at 200°C, 400°C, 500°C, 600°C, 700°C, 800°C, and 900°C, respectively. The extended dark regions were found in the images of samples annealed

from 700°C to 900°C. The serious cracks of spin-on $NiTiO_3$ films could be discovered at temperatures of 800°C and 900°C as shown in figure 3.7 and figure 3.8, respectively. And figure 3.9 describes that the roughness of samples abruptly becomes serious while annealing temperature is higher than 600°C.

3.2 Auger Electron Microscope

The incorporation of carbon element in a gate dielectric would degrade the effective dielectric constant [85]. Thus Auger depth profile is used to analyze the elements in spin-on $NiTiO_3$ insulator with 600°C annealing treatment. It could be observed that the signal of carbon element merely exists at the start of analysis, i.e. at the surface of the sample as shown in figure 3.10. Because the surface carbon may be detected from the absorption of the residual in the surrounding air, we assume that there is no carbon element in the dielectric formed by sol-gel spin coating method.

In this analysis, because we have no reference sample to derive the relative sensitivity factor for the evaluating atomic concentration in depth profile, there is an error in the atomic percentage in the figure 3.10. In spite of this deviation, the qualitative composition result could be acceptable.

3.3 Electron Spectroscopy for Chemical Analysis

There is no doubt that the spin-on dielectrics only contain nickel, titanium and oxygen elements, and this is confirmed by Auger depth profile in section 3.2. Nevertheless, we still have no idea on the chemical properties and atomic concentration ratio of $NiTiO_3$ material prepared by sol-gel spin coating as a gate dielectric. In this section, we will use electron spectroscopy for chemical analysis (ESCA) to get more information of this $NiTiO_3$ material.

Figure 3.11 to figure 3.13 show the ESCA results of the dielectrics formed by sol-gel spin coating method, and the dielectric under analysis is 1-coated with 600°C annealing treatment. From figure 3.11 to figure 3.13 are the ESCA spectra of nickel 2*p* orbit, titanium 2*p* orbit and oxygen 1*s* orbit, respectively. The spectrum of oxygen 1*s* orbit as shown in figure 3.13 presents that there may be two kinds of metal-oxygen bonds with lower binding energy near 530.5 eV, e.g. Ni-O and Ti-O for all samples. However, the broader binding energy distribution for the sample annealed at 200°C may be resulted from hydroxides in the dielectric [86]. We also notice that there are two shake-up peaks with higher binding energy than two main peaks ($2p_{3/2}$ and $2p_{1/2}$) in the Ni spectrum as shown in figure 3.11.

In order to confirm the atomic concentration ratio of the dielectric prepared by sol-gel spin coating method, more detailed ESCA analysis for the spin-on dielectric annealed at 600°C is performed. After background removal by Shirley method and curve fitting for metal-oxygen bonds (oblique line area) in oxygen spectrum, we integrate the intensity from 854 to 887 eV for nickel spectrum, from 453 to 468 eV for titanium spectrum and 526 to 535 eV for oxygen spectrum as shown in figure 3.14. The relative sensitivity factors for nickel, titanium and oxygen are 2.83, 1.47 and 0.66, respectively. And the atomic concentration ratio is obtained as,

$$[\mathrm{Ni}]:[\mathrm{Ti}]:[\mathrm{O}] = \frac{AC_{\mathrm{Ni}}}{SF_{\mathrm{Ni}}}:\frac{AC_{\mathrm{Ti}}}{SF_{\mathrm{Ti}}}:\frac{AC_{\mathrm{O}}}{SF_{\mathrm{O}}} = \frac{1727944.7}{2.83}:\frac{929800.15}{1.47}:\frac{1219826.5}{0.66}$$

$$\approx 1:1.03:3.02$$

Therefore, the atomic concentration ratio is almost close to 1:1:3.

3.4 Dielectric Permittivity

As many researches were proposed in the recent ten years, it is easy to form an interfacial layer between high-κ materials and silicon substrate, and it is imprecise and

difficult to exactly extract the κ value of $NiTiO_3$ material from measuring capacitance. In order to estimate the dielectric constant of $NiTiO_3$ thin film, a thermal oxidation was used to grow a high quality SiO_2 thin film before the $NiTiO_3$ dielectric was spun on the wafers as shown in figure 3.15, which shows the HR-TEM image of $Si/SiO_2/NiTiO_3/Al$ structure. Then the *C-V* characteristics of both $Si/SiO_2/NiTiO_3/TaN$ and $Si/SiO_2/TaN$ capacitors were demonstrated in figure 3.16, and the well-behaved *C-V* characteristics could be observed for the both of the two capacitors without flat-band voltage shift. The capacitance equivalent thickness (CET) is extracted from *C-V* curves at 100 kHz without considering quantum mechanical and depletion effect from Si-sub. The CET of gat dielectric layers of $SiO_2/NiTiO_3$ and SiO_2 structures are 6.59 nm and 5.27 nm, respectively. Furthermore, the TEM image of figure 3.15 displays that the physical thicknesses of 1-coated high-κ dielectric and thermal oxide are a range of 12.0 ~ 14.0 nm and about 5.3 nm, respectively. As a result, the exact dielectric constant of the $NiTiO_3$ thin film is calculated to be in the range of 36 ~ 42, which is expectable value of the $NiTiO_3$ films fabricated by directly thermal oxidizing the deposited Ni/Ti films formed by physical vapor deposition method [23]. Moreover, the hysteresis characteristics of the $NiTiO_3$ gate dielectric is 46 mV for flat-band voltage shift after repeating ±3 V forward and reverse stresses for several times as shown in figure 3.17.

3.5 Device Performance

Figure 3.18 exhibits the *C-V* characteristics of $NiTiO_3$ gate dielectrics with different temperature treatments. The sample with 600°C-RTA (Rapid Thermal Annealing) treatment demonstrates a steeper *C-V* slope in the depletion region, which implies a better $NiTiO_3$/Si-sub interface. The RTA temperatures up to 600°C cause flatter *C-V* curves which may be due to sub-stoichiometric interfacial-oxide growth and thermal stress.

Figure 3.19 shows the *I-V* characteristics of $NiTiO_3$ gate dielectrics with different

temperature treatments. The leakage current density increases largely with raising annealing temperature from 600°C to 900°C, even though the *C-V* curves suggest a larger capacitance equivalent thickness for samples annealed at high temperatures. This could be interpreted by the cracks and crystallization of $NiTiO_3$ thin films [87]. We sum up the fundamentally electrical behaviors of spin-on $NiTiO_3$ gate dielectrics as functions of annealing temperatures as shown in figure 3.20. Consequently, the leakage current density decreases with raising temperature from 200°C to 600°C because of the denser $NiTiO_3$ thin films, and the property of the material annealed at 600°C possesses the thinnest capacitance equivalent thickness. Eventually, table 3.1 summarizes the extracted the capacitance equivalent thickness, leakage current density, and the surface roughness of the $NiTiO_3$ thin films formed by sol-gel spin coating method with different temperature treatments.

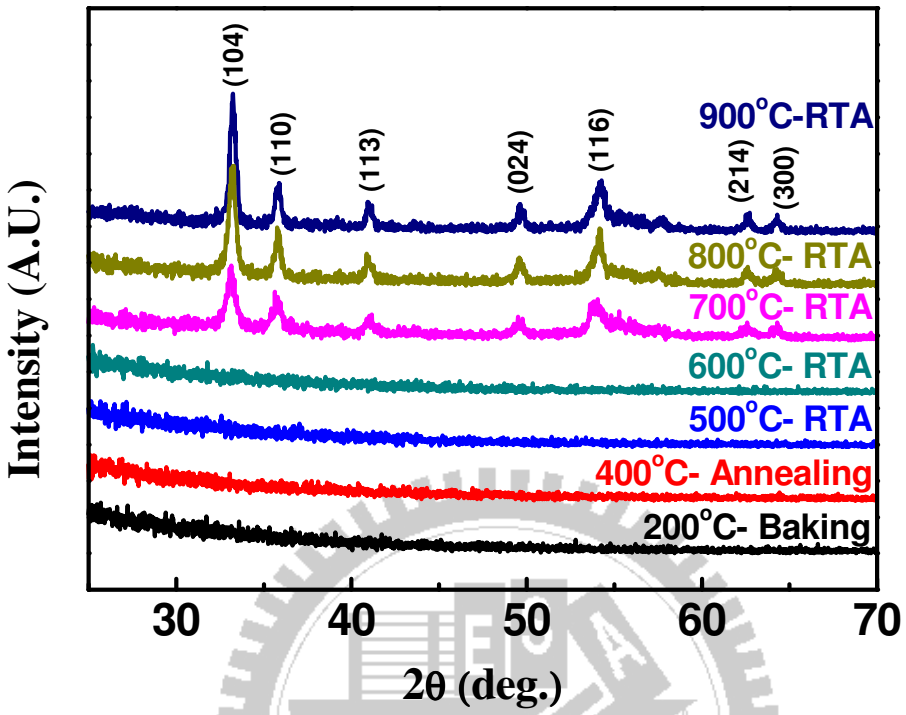


Figure 3.1 XRD spectrum of spin-on $NiTiO_3$ with different temperature treatments. The significant peaks correspond to crystallized $NiTiO_3$ phases.

Figure 3.2 SPM images of spin-on $NiTiO_3$ films with different thermal treatments at 200°C. The image size is 1μm by 1μm.

Figure 3.3 SPM images of spin-on $NiTiO_3$ films with different thermal treatments at 400°C. The image size is 1μm by 1μm.

Figure 3.4 SPM images of spin-on $NiTiO_3$ films with different thermal treatments at 500°C. The image size is 1μm by 1μm.

Figure 3.5 SPM images of spin-on $NiTiO_3$ films with different thermal treatments at 600°C. The image size is 1μm by 1μm.

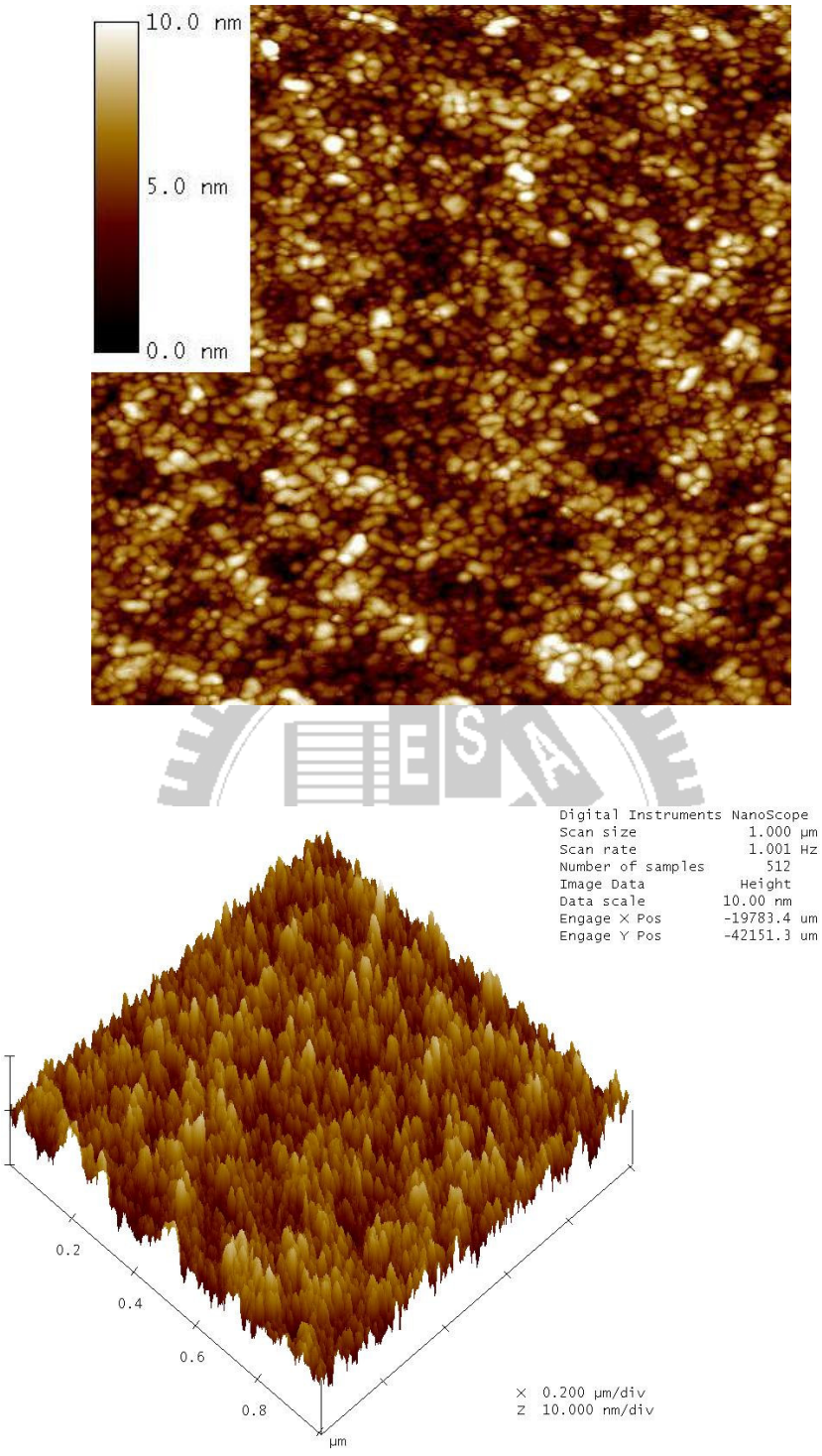


Figure 3.6 SPM images of spin-on $NiTiO_3$ films with different thermal treatments at 700°C. The image size is 1μm by 1μm.

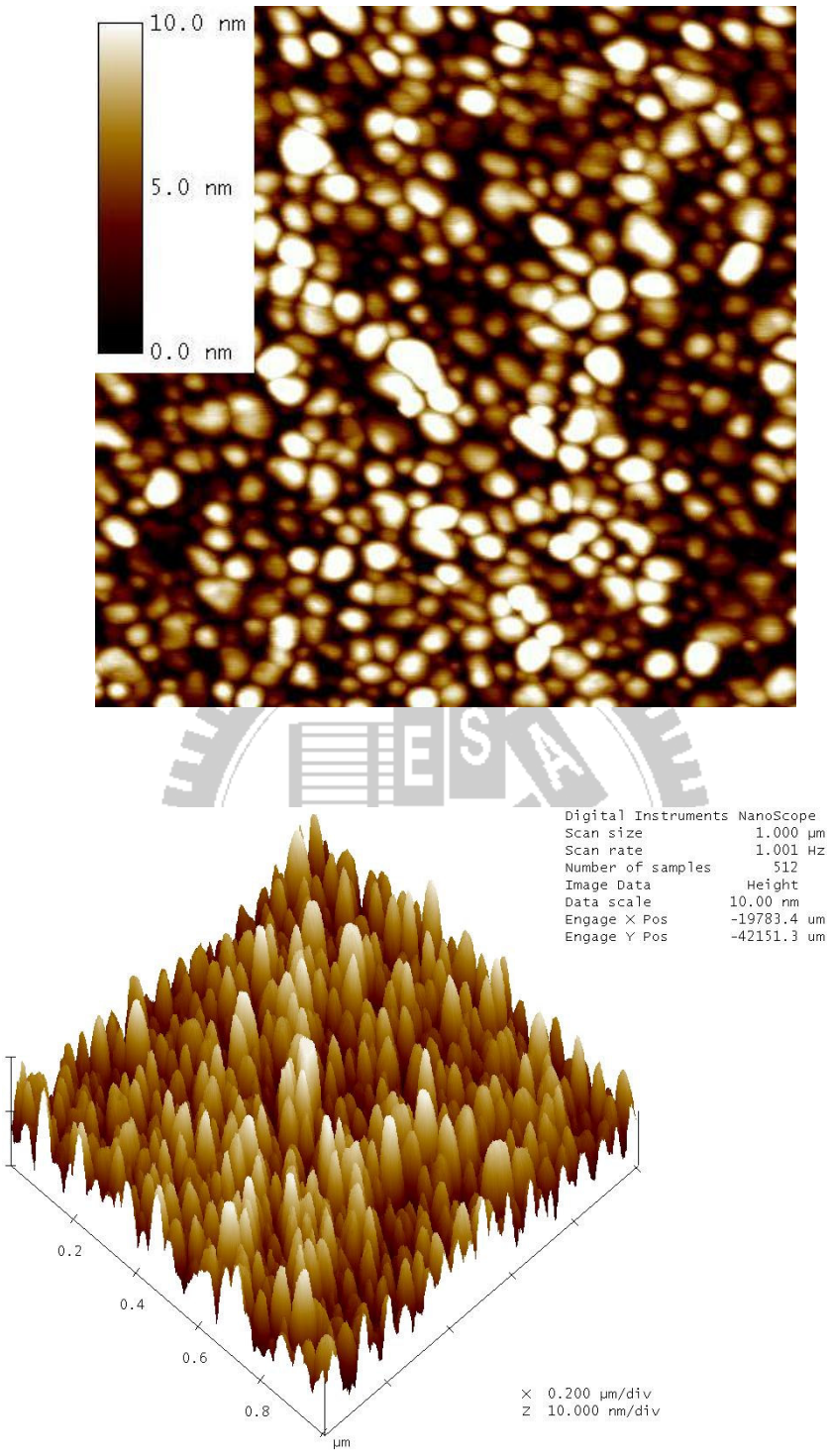


Figure 3.7 SPM images of spin-on $NiTiO_3$ films with different thermal treatments at 800°C. The image size is 1μm by 1μm.

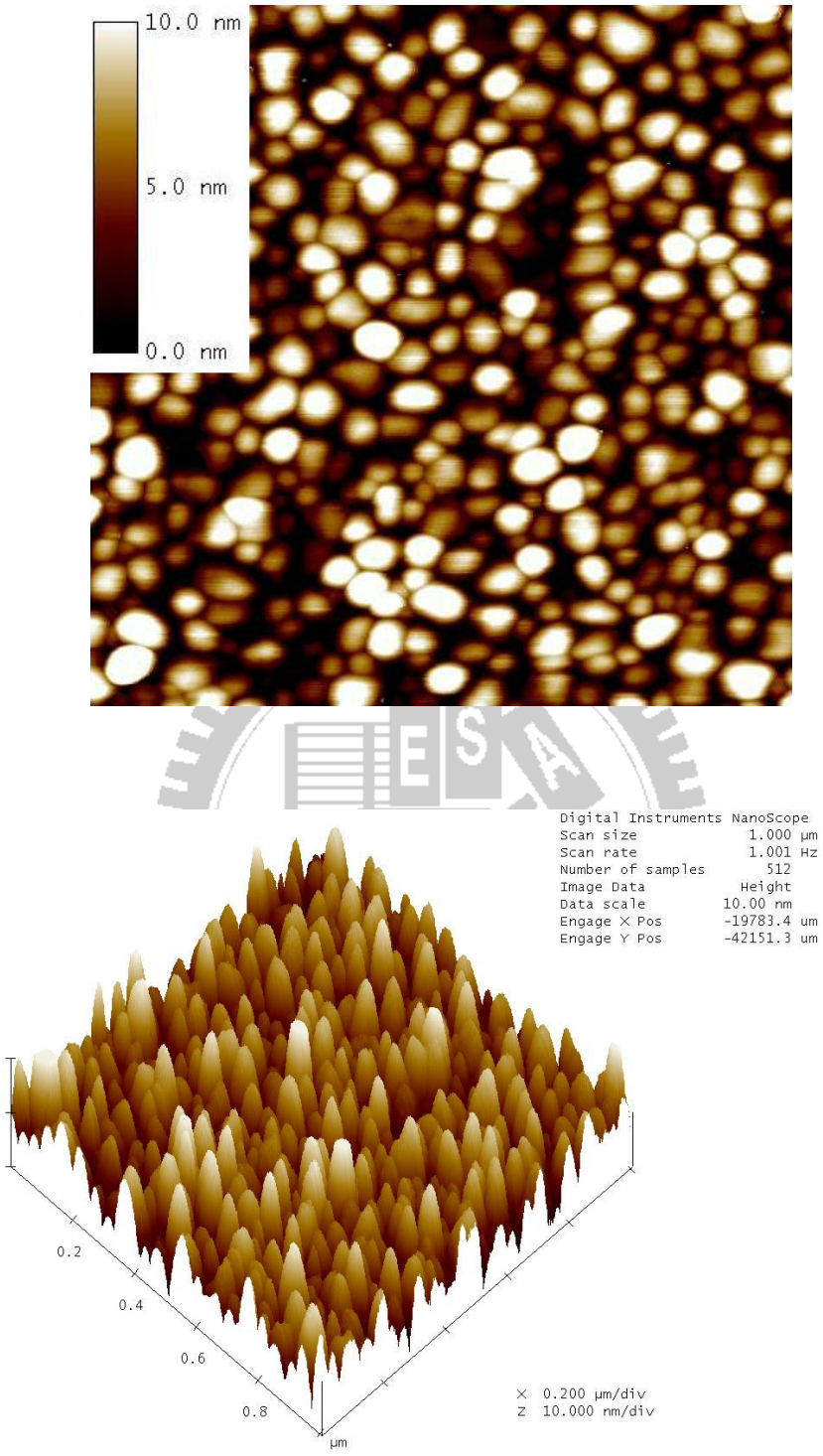


Figure 3.8 SPM images of spin-on $NiTiO_3$ films with different thermal treatments at 900°C. The image size is 1μm by 1μm.

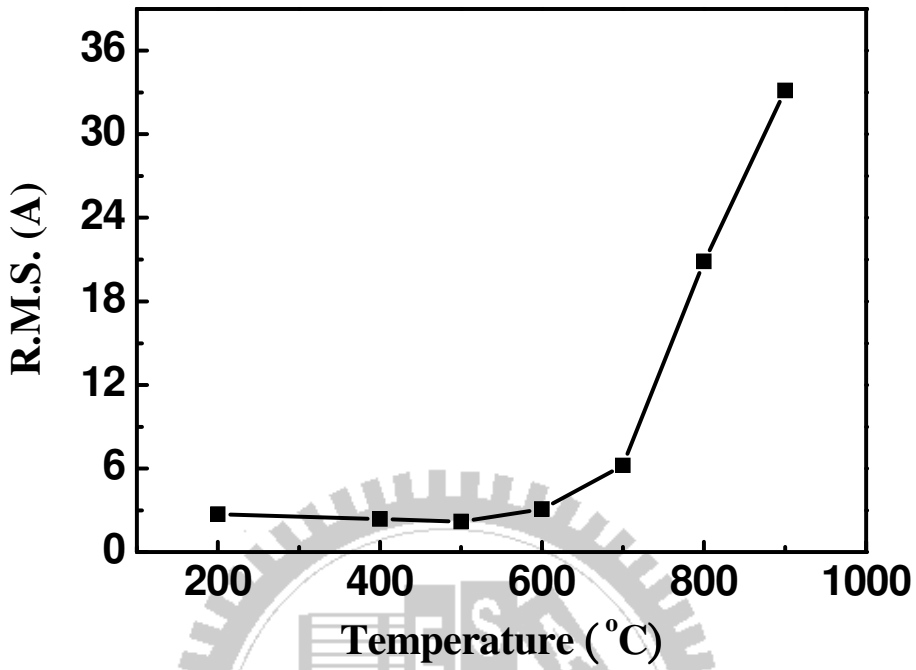


Figure 3.9 Surface roughness of spin-on $NiTiO_3$ dielectric as a function of annealing temperature.

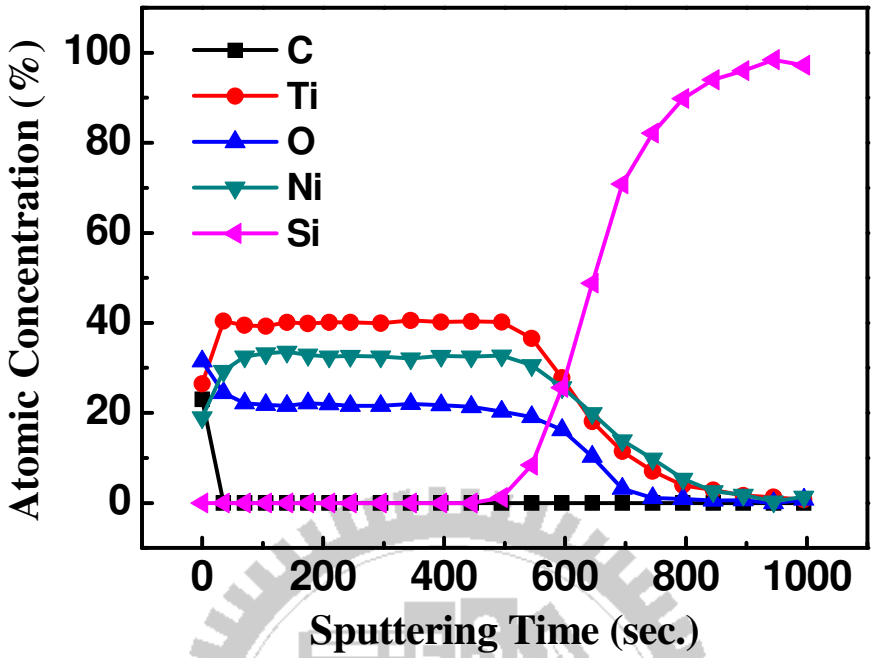


Figure 3.10 Auger depth profile of spin-on $NiTiO_3$ dielectric annealed at 600°C.

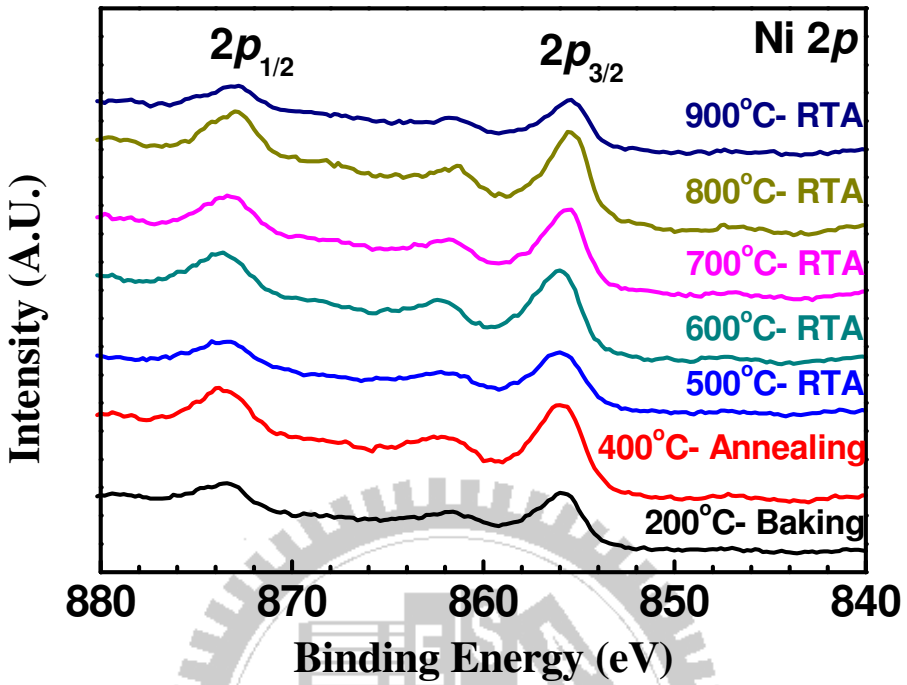


Figure 3.11 ESCA spectrum of nickel element with different annealing temperatures.

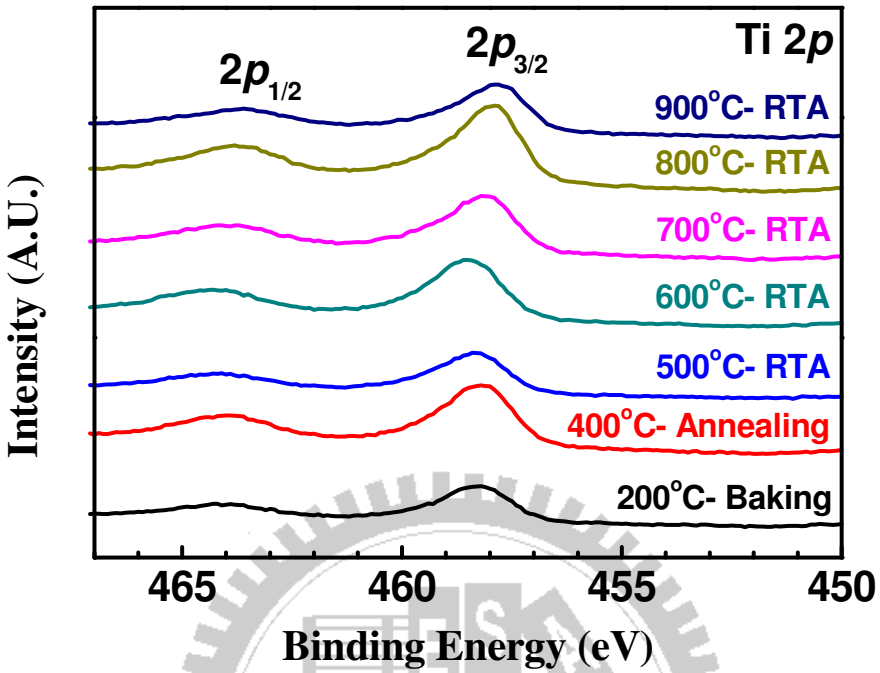


Figure 3.12 ESCA spectrum of titanium element with different annealing temperatures.

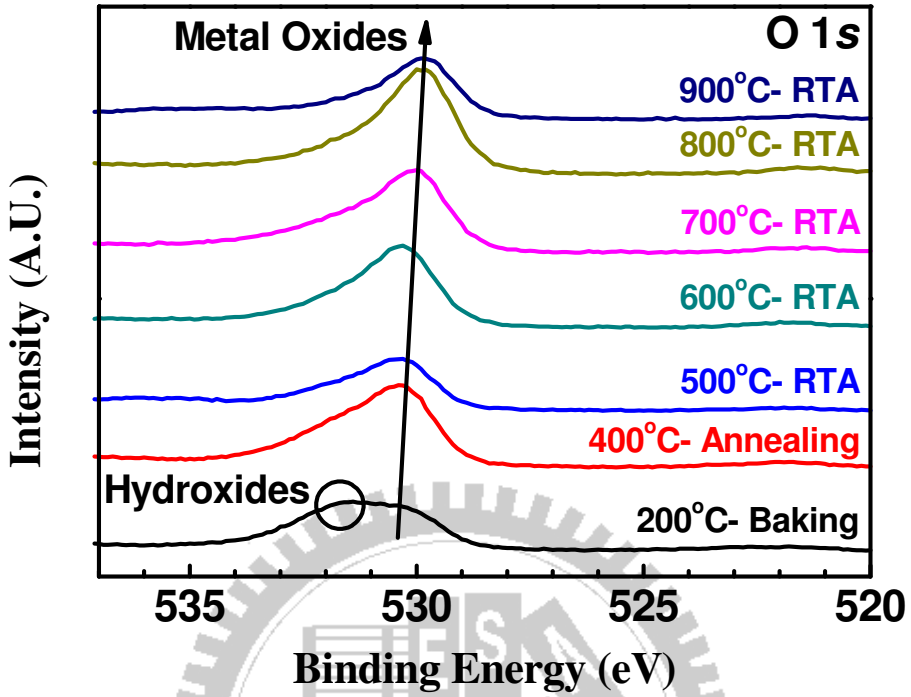


Figure 3.13 ESCA spectrum of oxygen element with different annealing temperatures.

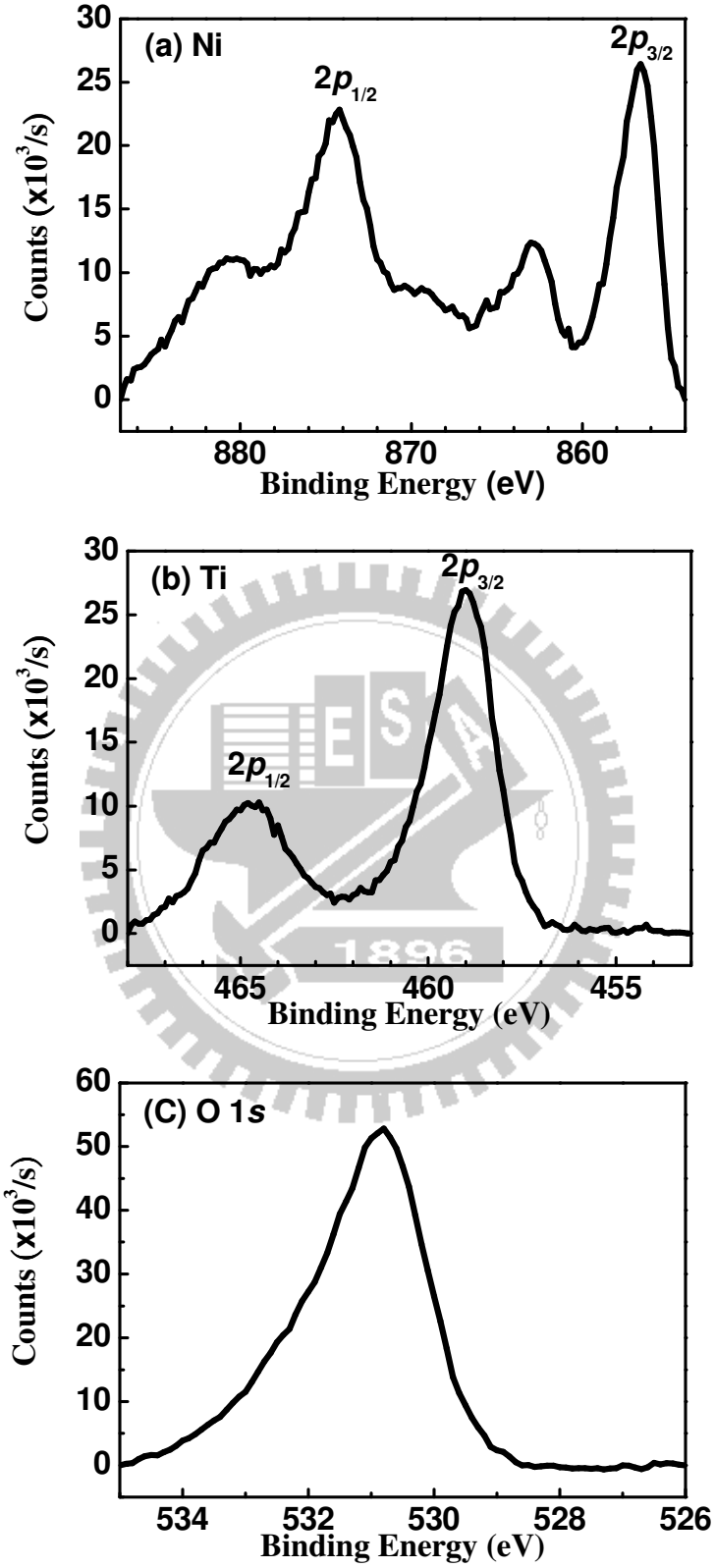


Figure 3.14 ESCA spectra of (a) Ni 2*p*, (b) Ti 2*p* and (c) O 1*s* for the spin-on $NiTiO_3$ dielectric annealed at 600°C.

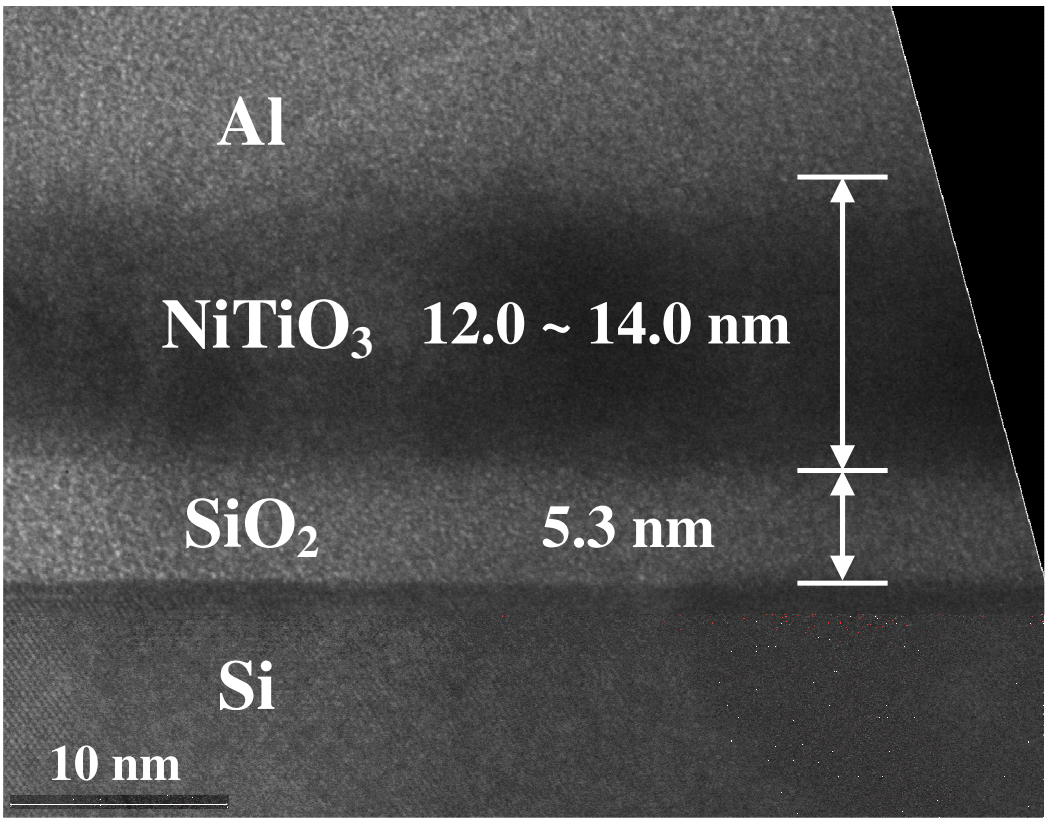


Figure 3.15 TEM micrograph of 1-layer $NiTiO_3$ film spin-coated on a high-quality thermal SiO_2 layer and annealed at 600°C.

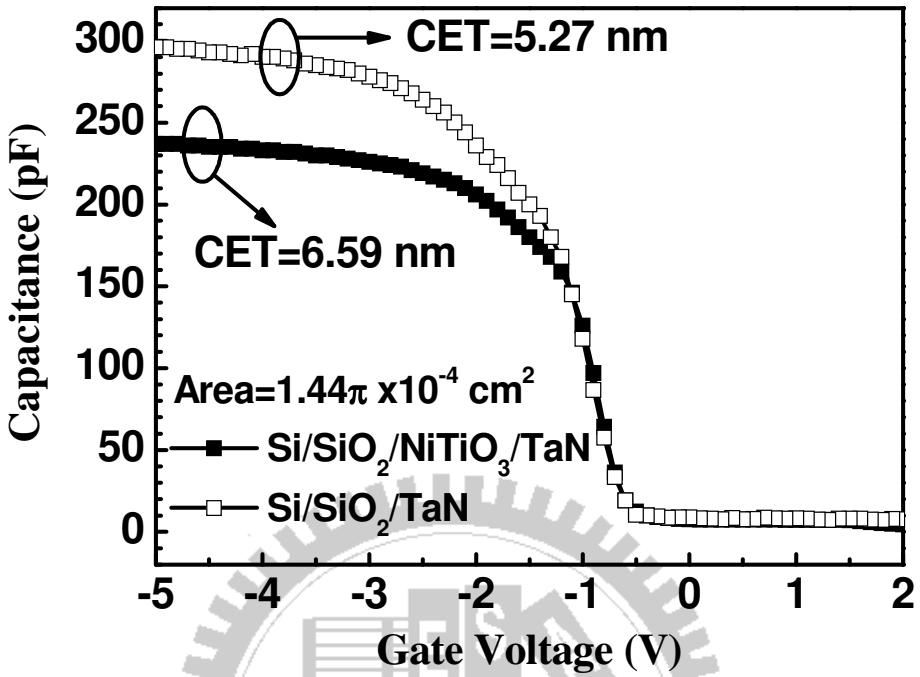


Figure 3.16 *C-V* curves of capacitors with $Si/SiO_2/NiTiO_3/TaN$ and $Si/SiO_2/TaN$ stack structures.

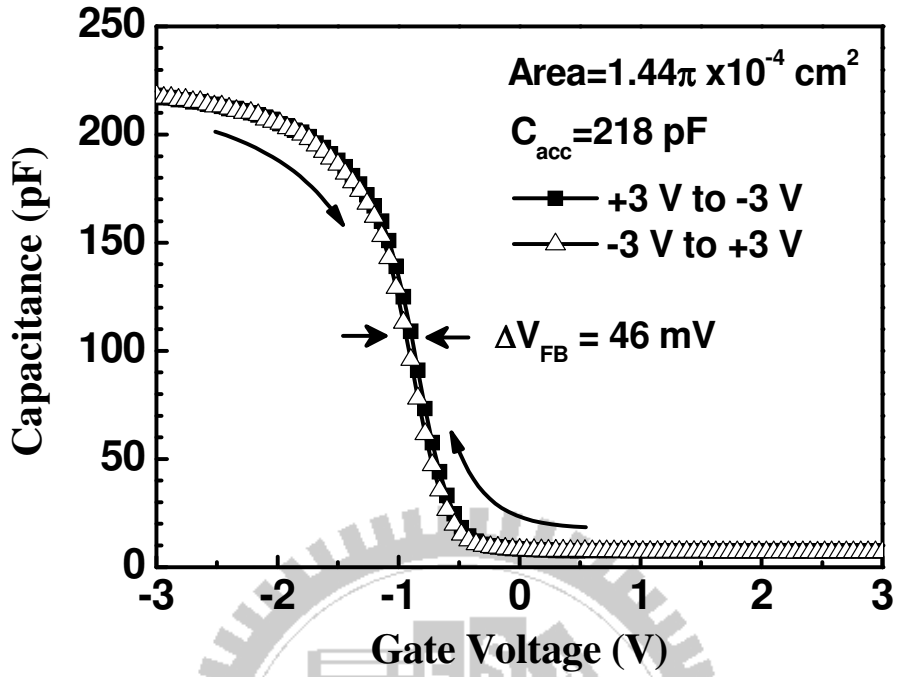


Figure 3.17 *C-V* curves of the $NiTiO_3$ gate dielectric after forward and reverse switching for hysteresis loop shift.

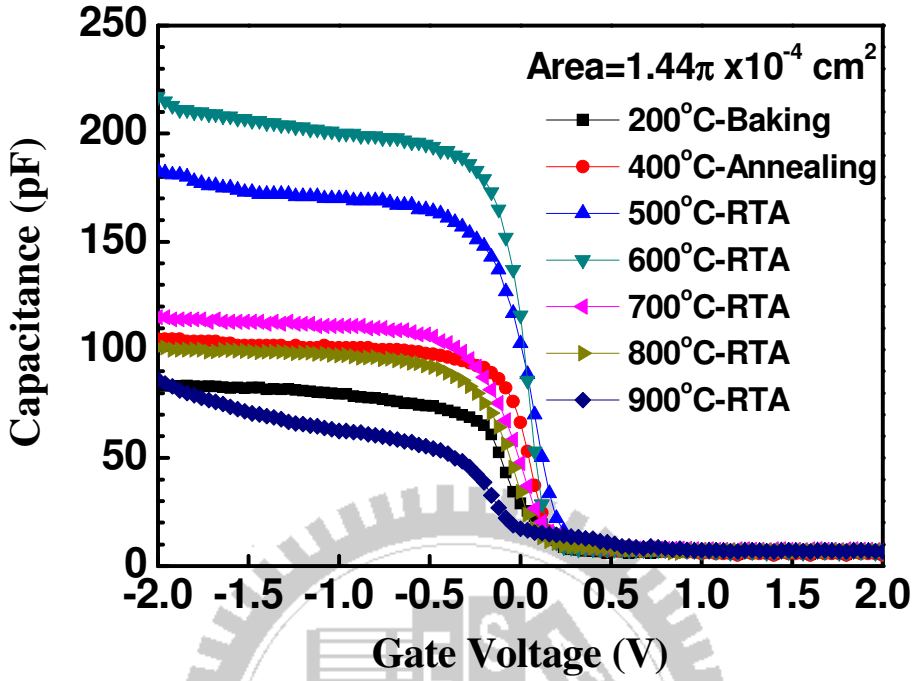


Figure 3.18 *C-V* curves of spin-on $NiTiO_3$ films with different thermal treatments.

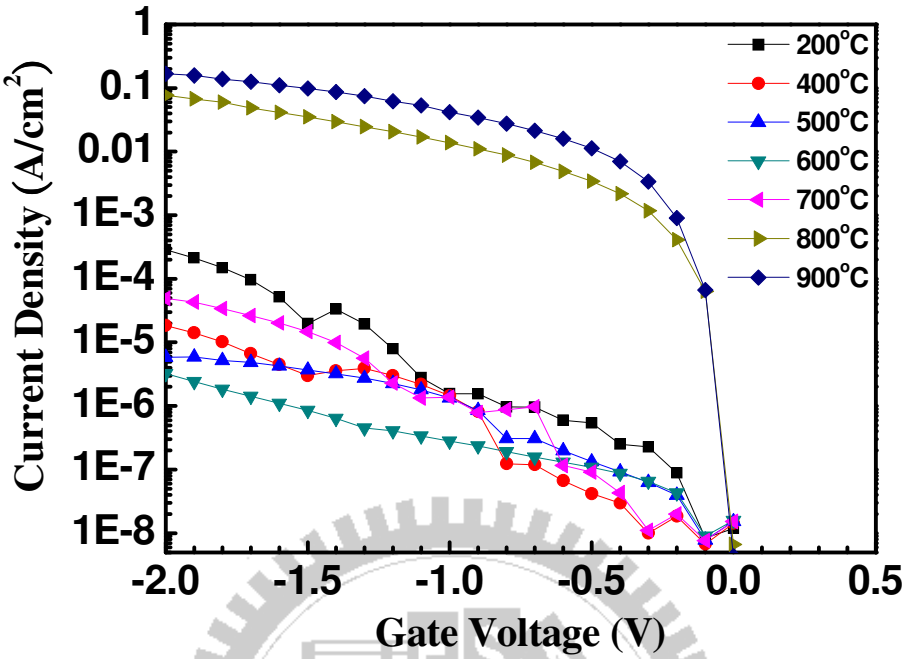


Figure 3.19 *I-V* curves of spin-on $NiTiO_3$ films with different thermal treatments.

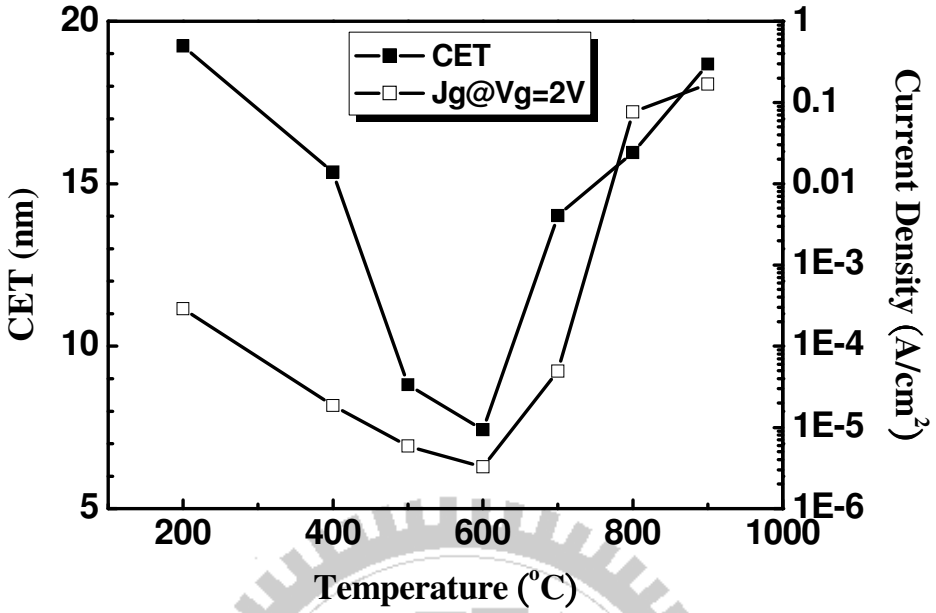
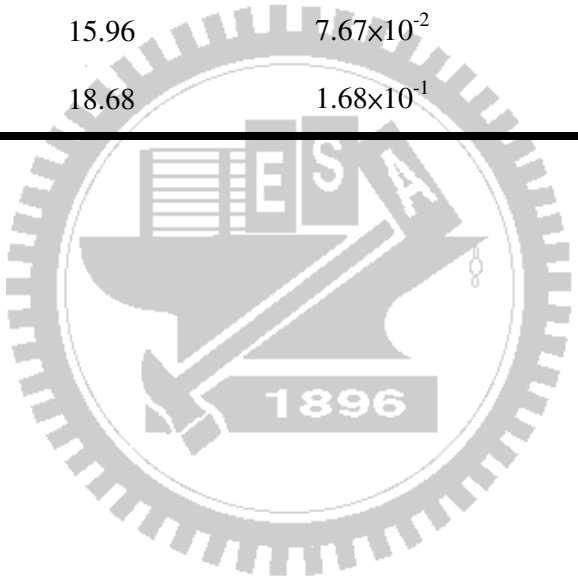


Figure 3.20 Capacitance equivalent thickness (CET) and current density of spin-on $NiTiO_3$ gate dielectrics as functions of annealing temperatures.

Table 3.1 The sum of capacitance equivalent thickness, leakage current density, and roughness value for $NiTiO_3$ films after different temperature treatments.

Temperature	CET (nm)	J (A/cm^2) @ V = 2 V	R.M.S. (Å)
200°C-Baking	19.24	2.89×10^{-4}	2.72
400°C-Annealing	15.35	1.86×10^{-5}	2.37
500°C-RTA	8.81	5.89×10^{-6}	2.18
600°C-RTA	7.43	3.25×10^{-6}	3.09
700°C-RTA	14.02	4.90×10^{-5}	6.22
800°C-RTA	15.96	7.67×10^{-2}	20.85
900°C-RTA	18.68	1.68×10^{-1}	33.14



Chapter 4

Electrical Characteristics of Thin-Film Transistors

High-performance poly-Si TFTs with a low operating voltage, a low subthreshold swing, a high driving capability and a low gate-leakage current are required for achieving high-speed display driving circuits. Because the conventional solid-phase crystallized poly-Si TFTs with continued scaling SiO_2 gate dielectric can not satisfy these demands [88], integrating metal gate on high dielectric constant (High-κ) gate dielectric with poly-Si TFTs has received lots of attention for maintaining a higher gate capacitance density, a lower gate-leakage current and a much more induced carrier density [89-95]. A novel technique, sol-gel spin coating method, to prepare for gate dielectric or active channel has been reported in the recent years [26][30][32][33].

In this chapter, we will report the device performance of poly-Si TFTs with high-κ $NiTiO_3$ gate dielectric prepared by sol-gel spin coating method. The electrical characteristics such as I_{DS}-V_{GS} curves, I_{DS}-V_{DS} curves and threshold-voltage rolloff will be demonstrated with different annealing temperatures and compare to the conditions of NH_3 plasma treatment.

4.1 Device Performance for Different Thermal Treatments

Figure 4.1 shows the typical transfer characteristics (I_{DS}-V_{GS}) for the proposed poly-Si TFTs with a $NiTiO_3$ gate dielectric prepared by dip-coating method annealed at different treatment temperatures and the measurement condition is the dimension of width/length (W/L) = 20 μm/ 20 μm at V_{DS} = −1 V. The threshold voltage (V_{TH}) is defined as the gate voltage required a normalized drain current of I_{DS} = (W/L)×100 nA at V_{DS} = −0.1 V. The ON/OFF current ratio (I_{ON}/I_{OFF}) is defined as that ratio of the maximum on-state current to the minimum off-state current at V_{DS} = −1 V. The driving current of poly-Si $NiTiO_3$ TFTs with a

500°C-RTA treatment is better than the others. The threshold voltage of the poly-Si $NiTiO_3$ TFTs with annealing temperature at 500, 600 and 700°C is around −0.93, −1.18 and −1.25 V, respectively. The subthreshold swing (*S.S.*) of that with annealing temperature at 500, 600 and 700°C is around 245, 253 and 460 mV/dec., respectively. The field-effect mobility (μ_{FE}) of that with annealing temperature at 500, 600 and 700°C is around 11.96, 10.62 and 4.19 cm^2/V-s, respectively. The I_{ON} / I_{OFF} ratio of that with annealing temperature at 500, 600 and 700°C is around 2.61×10^6, 5.96×10^5 and 1.32×10^3, respectively. However, the undesirable gate-induced drain leakage (GIDL) currents of the poly-Si $NiTiO_3$ TFTs are found markedly, especially under continuously decreasing gate bias. The inferior GIDL currents may be attributed to the higher electric field near the drain junction owing to the higher gate capacitance density of the high-κ $NiTiO_3$ gate dielectric, and the GIDL current issue could be solved by applying lightly doped drain structure [96].

The typical output characteristics (I_{DS}-V_{DS}) of the proposed poly-Si $NiTiO_3$ TFTs prepared by sol-gel spin coating method annealed at different treatment temperatures are demonstrated in figure 4.2. The scale size of the devices is channel length (L) and channel width (W) of 20 μm and 20 μm, respectively. As we can see, the driving current of the poly-Si $NiTiO_3$ TFTs with a 500°C-RTA treatment (about 7.3 μA) is approximately two times larger than that with a 600°C-RTA treatment (about 3.1 μA) and nine times larger than that with a 700°C-RTA treatment (about 0.77 μA) at V_{DS} = −2 V and the gate drive of $V_{GS} - V_{TH}$ = −1 V. The driving current obviously decreases with increasing the annealing temperature. The output characteristic of the sample with a 500°C-RTA treatment is the best due to the relatively high capacitance density induced the higher mobility and smaller threshold voltage.

It is evident that the electrical properties of the sample with a 500°C-RTA treatment are the best, and the result of the poly-Si TFTs is different from that of the capacitors analyzed previously. We suppose that it might result form the variation of the fabrication process in Metal-RTA instrument. Because Metal-RTA instrument executes at an uncontrollable

temperature range, this reason might brings about the sample with a 600°C-RTA treatment to be slightly crystallized in advance. In addition, the capacitor characteristics of 500°C and 600°C-RTA treatments are approximate, the device performance of the poly-Si TFTs with a crystallized 600°C-$NiTiO_3$ gate dielectric degrades remarkably.

4.2 Threshold-Voltage Rolloff for Different Thermal Treatments

In order to investigate the short-channel effects of the poly-Si $NiTiO_3$ TFTs and the poly-Si tetraethoxysilane (TEOS) TFTs, which is deposited a 700-nm thickness of the TEOS gate dielectric, the threshold-voltage rolloff properties are shown in figure 4.3. The threshold voltage of the poly-Si TFTs with TEOS gate dielectric is decreased with continuously scaling down channel length, dominated by the reduction of grain-boundary trap states. In contrast, the poly-Si TFTs with $NiTiO_3$ gate dielectric displays a high gate capacitance density to rapidly fill up the grain-boundary trap states and keeps the superior turn-on characteristics, and thus the threshold-voltage rolloff properties could be controlled well. The electrical characteristics of poly-Si $NiTiO_3$ TFTs with 500, 600 and 700°C-RTA temperature treatments are summarized as listed in table 4.1, and the capacitance equivalent thickness (CET) values are estimated from the measurements of the capacitors at the same temperatures in the previous chapter.

4.3 Device Performance with NH_3 Plasma Treatment

Figure 4.4 shows the transfer characteristics (I_{DS}-V_{GS}) of the poly-Si $NiTiO_3$ TFTs with and without NH_3 plasma treatment after a 500°C-RTA treatment, and the measurements are performed at drain voltage of V_{DS} = −1 V. The drawn channel width (W) and channel length (L) are 20 μm and 20 μm, respectively. The parameters of the devices, including threshold

voltage, subthreshold swing and field-effect mobility are extracted at V_{DS} = −0.1 V, and the ON/OFF current ratio is defined as that ratio of the maximum on-state current to the minimum off-state current at V_{DS} = −1 V. The drain current in the saturation region ($I_{DS,\,sat}$) is extracted at the gate drive of $V_{GS} - V_{TH}$ = −1 V. The threshold voltage (V_{TH}) is defined as the gate voltage required to achieve a normalized drain current of I_{DS} = (W/L)×100 nA. The detailed device parameters of NH_3-plasma-treatment and control poly-Si $NiTiO_3$ TFTs are summarized in table 4.2.

Accordingly, the electrical performances of the poly-Si $NiTiO_3$ TFT with NH_3 plasma treatment are markedly improved compared with those of the control poly-Si $NiTiO_3$ TFT. With NH_3 plasma treatment, the poly-Si $NiTiO_3$ TFT exhibits significant performance improvements in terms of the threshold voltage decreased from −0.93 to −0.86 V and the subthreshold swing reduced from 245 to 238 mV/dec.. It is known that the many trap states, associated with the Si dangling bonds at the grain boundaries, would strongly affect the threshold voltage and subtreshold swing [97]. Thus, the introduction of nitrogen radicals dissociated from NH_3 plasma into the active channel would result in interface state passivation and the formation of strong Si–N bonds in place of the weak Si–Si and/or Si–H bonds, leading to improve the device performance of poly-Si $NiTiO_3$ TFTs in comparison with those without NH_3 plasma treatment [84]. In addition, the maximum on-state current and the on/off current ratio of the poly-Si $NiTiO_3$ TFT with NH_3 plasma treatment are also superior to those of the control poly-Si $NiTiO_3$ TFT. The corresponding on/off current ratios for NH_3-plasma-treatment and control poly-Si $NiTiO_3$ TFTs are 8.53×10^6 and 2.61×10^6, respectively. The on/off current ratios of the poly-Si $NiTiO_3$ TFT with NH_3 plasma treatment is six times larger than that of the control poly-Si $NiTiO_3$ TFT.

The field-effect mobility is extracted from the transconductance value at V_{DS} = −0.1 V. The field-effect mobility of NH_3-plasma-treatment poly-Si $NiTiO_3$ TFT (around 18.72 cm^2/V-s) is higher than that of the control poly-Si $NiTiO_3$ TFT (around 11.96 cm^2/V-s), and is

approximately 56% enhancement in the maximum field-effect mobility. Note that the tail states near the Si bandedge resulted from the strain bonds in the poly-Si and at the $NiTiO_3$/poly-Si interface would greatly affect the field-effect mobility [84]. This feature implies that the NH_3 plasma treatment might not only passivate the Si dangling bonds but also relieve the Si strain bonds. The proposed poly-Si TFTs crystallized by SPC technique could possess good electrical properties even without additional other plasma treatments, e.g. hydrogen (H_2) plasma, oxygen (O_2) plasma, nitrogen (N_2) plasma, etc., or other advanced phase crystallization techniques with narrow process window [98][99].

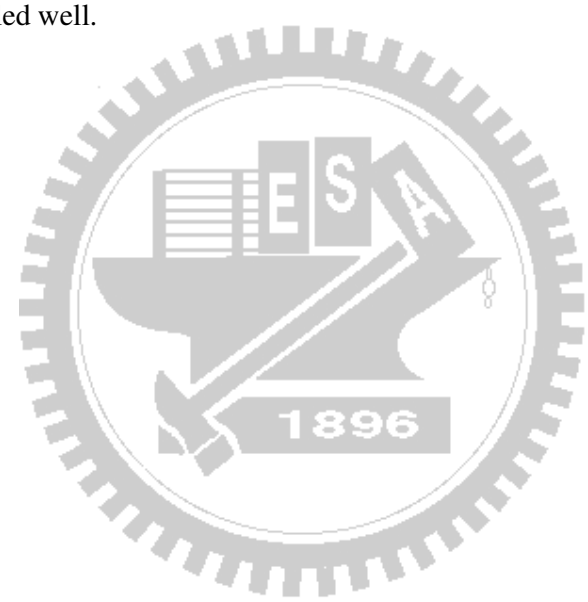
However, the undesirable GIDL currents of the poly-Si $NiTiO_3$ TFTs are still found markedly, especially under continuously decreasing gate voltage. The GIDL current of the NH_3-plasma treatment poly-Si $NiTiO_3$ TFT (about 1.63×10^{-10} A) is slightly lower than that of the control poly-Si $NiTiO_3$ TFT (about 3.51×10^{-10} A) under applying voltages of V_{GS} = 0.5 V and V_{DS} = −0.1 V. This result suggests that the incorporation of NH_3 particles into the poly-Si channel might passivate the trap states, thereby causing lower GIDL current under a relative high electric field.

Figure 4.5 displays the output characteristics (I_{DS}-V_{DS}) of the NH_3-plasma-treatment and the control poly-Si $NiTiO_3$ TFTs. With NH_3 plasma treatment, the poly-Si $NiTiO_3$ TFT exhibits great enhancement in the on-state driving current under gate drive of $V_{GS} - V_{TH}$ from −0.4 V to −1 V by an interval of −0.2 V. The $I_{DS,\,sat}$ current of the NH_3-plasma-treatment poly-Si $NiTiO_3$ TFT (about 26.9 μA) is three times larger than that of the control poly-Si $NiTiO_3$ TFT (about 7.3 μA). The NH_3 plasma passivation of trap states might lead to higher field-effect mobility, thus presenting an evident improvement on the driving capability.

4.4 Threshold-Voltage Rolloff with NH_3 Plasma Treatment

In order to investigate the short-channel effects of the poly-Si $NiTiO_3$ TFTs with and

without NH_3 plasma treatment after a 500°C-RTA treatment, the threshold voltage as a function of channel length with fixed channel width of 20 μm are shown in figure 4.6. The threshold voltage of the poly-Si TFTs with traditional SiO_2 gate dielectric is decreased with continuously scaling down channel length, called the threshold-voltage rolloff effect, dominated by the reduction of grain-boundary trap states [100]. In contrast, the poly-Si TFTs with $NiTiO_3$ gate dielectric reveals a high gate capacitance density to rapidly fill up the grain-boundary trap states and maintains the superior turn-on characteristics, demonstrating a better threshold-voltage rolloff characteristic. Thus the threshold-voltage rolloff properties could also be controlled well.



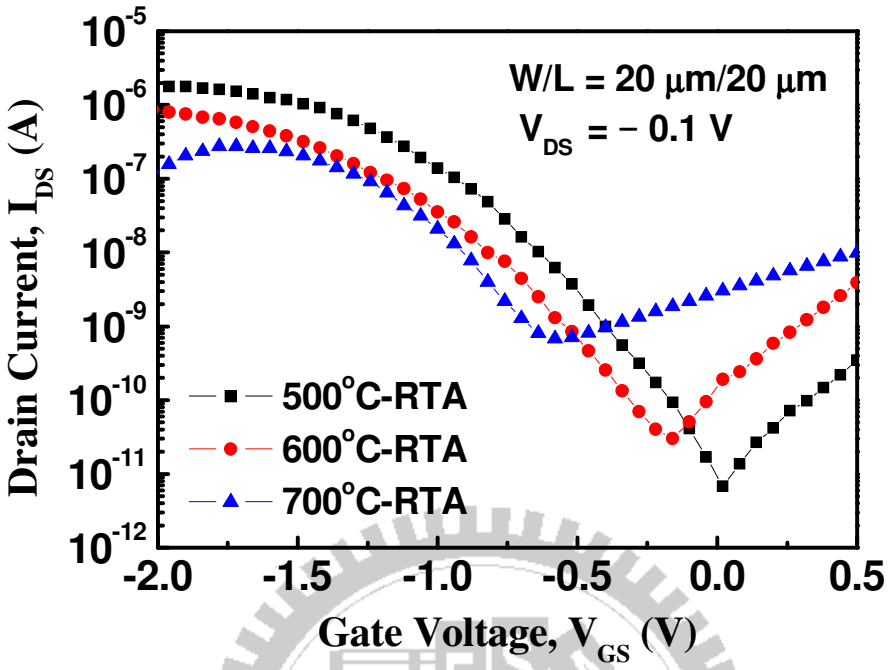


Figure 4.1 The typical transfer characteristics of the poly-Si $NiTiO_3$ TFTs prepared by sol-gel spin coating method annealed at different treatment temperatures.

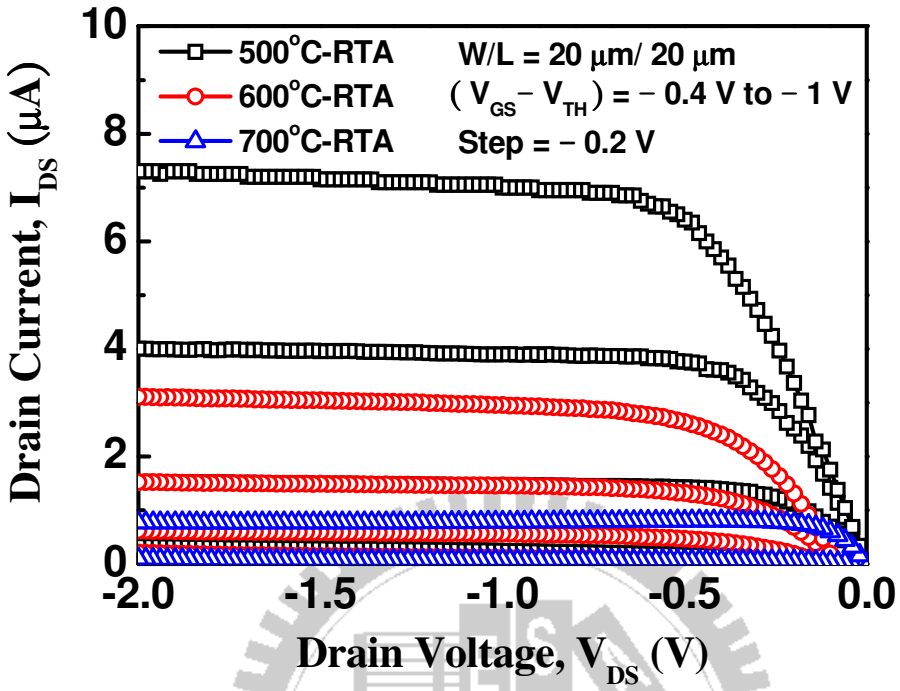


Figure 4.2 The typical output characteristics of the poly-Si $NiTiO_3$ TFTs prepared by sol-gel spin coating method annealed at different treatment temperatures.

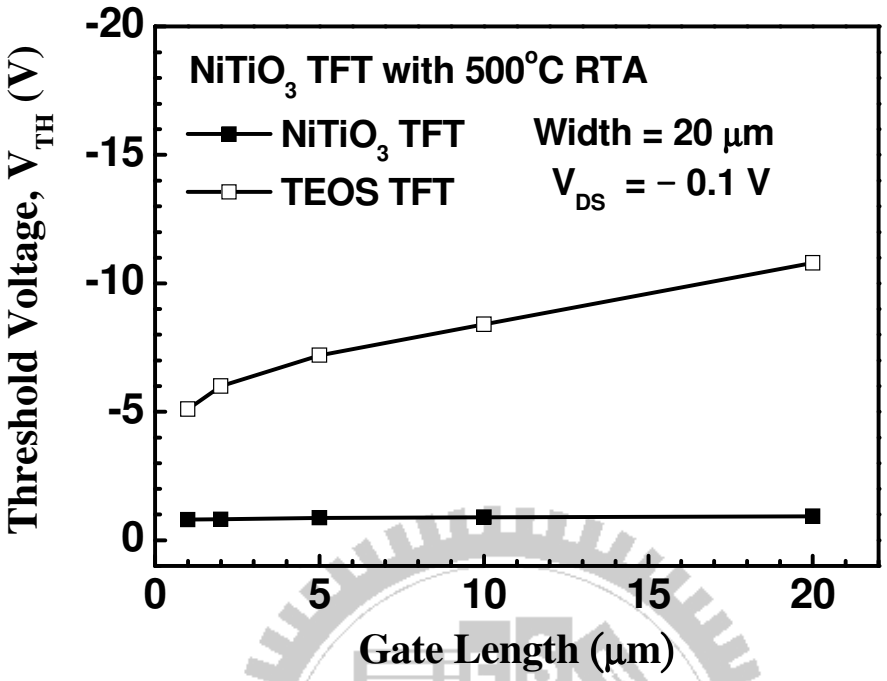


Figure 4.3 The threshold-voltage rolloff properties of the poly-Si $NiTiO_3$ TFTs and the poly-Si TEOS TFTs.

Table 4.1 The sum of electrical characteristics for poly-Si $NiTiO_3$ TFTs with 500, 600 and 700°C-RTA temperature treatments.

Temperature	CET (nm)	V_{TH} (V)	*S.S.* (mV/dec.)	μ_{FE} (cm^2/V-s)	I_{ON}/I_{OFF} Ratio
500°C	7.2	−0.93	245	11.96	2.61×10^6
600°C	8.5	−1.18	253	10.62	5.96×10^5
700°C	13.6	−1.25	460	4.19	1.32×10^3

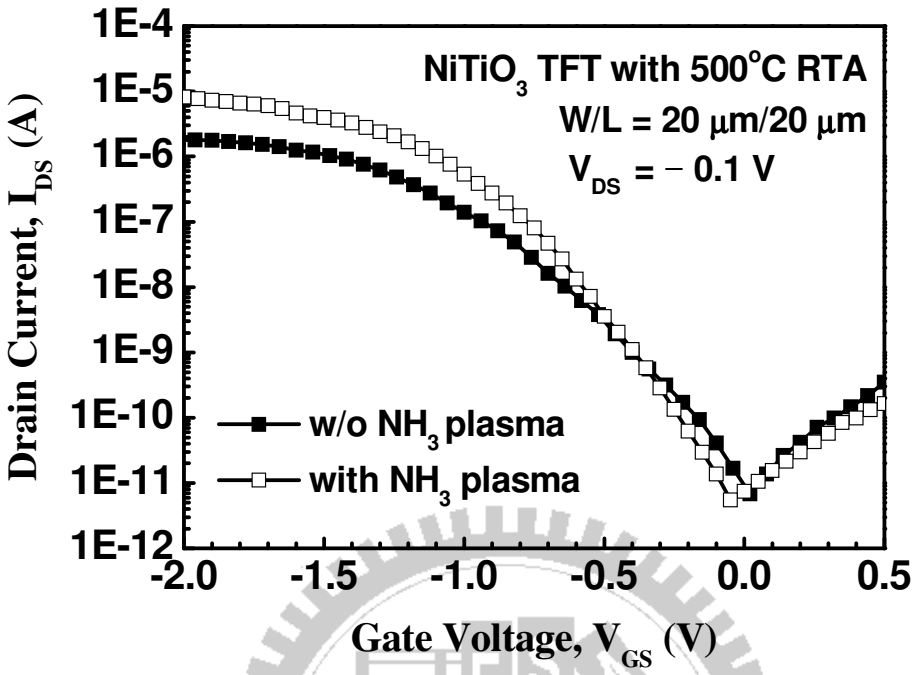


Figure 4.4 The typical transfer characteristics of poly-Si $NiTiO_3$ TFT at 500°C thermal annealing compared to NH_3 plasma treatment.

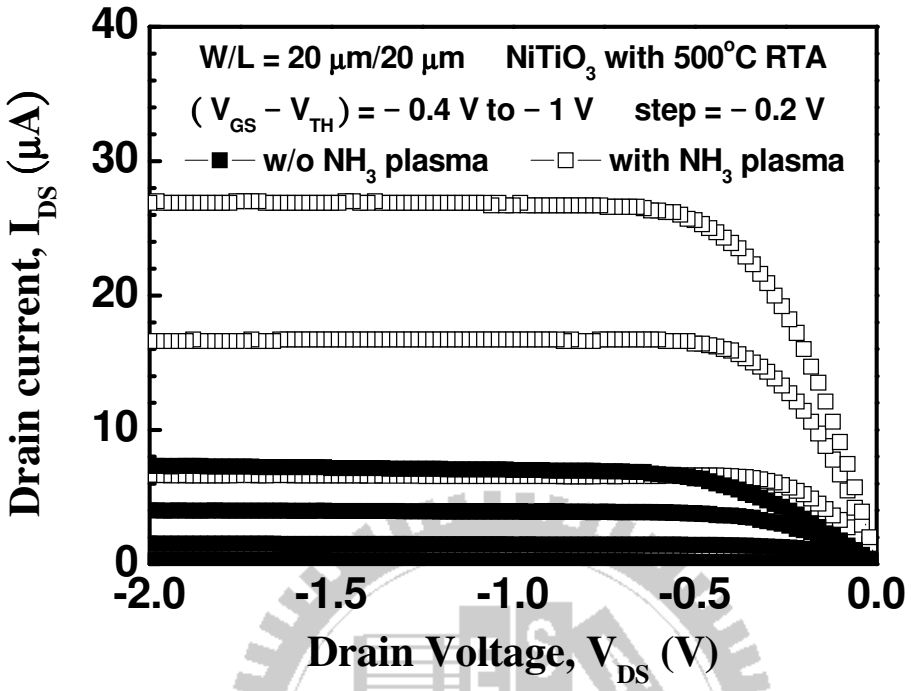


Figure 4.5 The typical output characteristics of poly-Si $NiTiO_3$ TFT at 500°C thermal annealing compared to NH_3 plasma treatment.

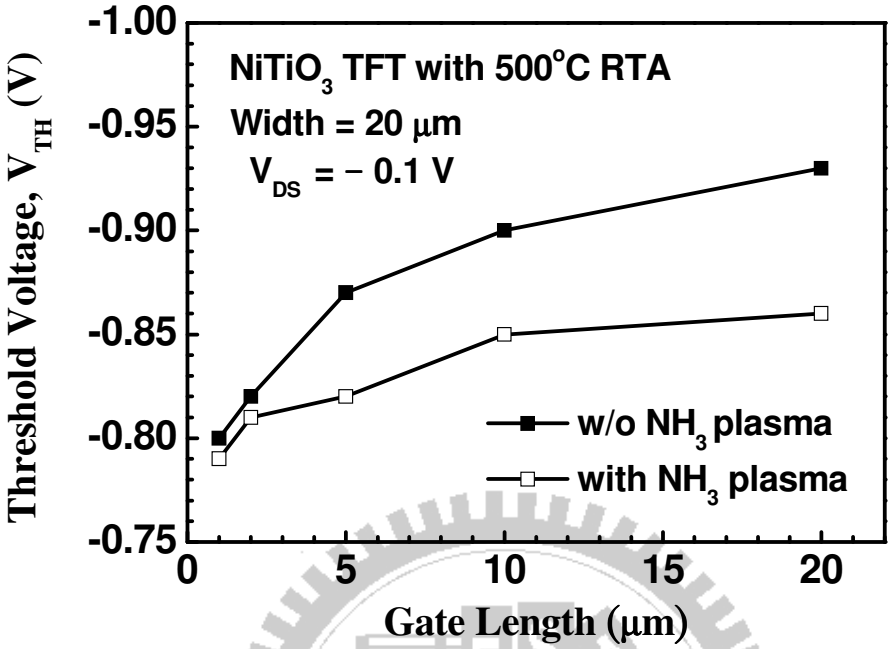


Figure 4.6 The threshold-voltage rolloff properties of poly-Si $NiTiO_3$ TFT at 500°C thermal annealing compared to NH_3 plasma treatment.

Table 4.2 The sum of electrical characteristics for poly-Si $NiTiO_3$ TFT at 500°C thermal annealing compared to NH_3 plasma treatment.

Fabrication Procedure	V_{TH} (V)	*S.S.* (mV/dec.)	μ_{FE} (cm^2/V-s)	I_{ON}/I_{OFF} Ratio	$I_{DS,\,sat}$ (μA)
NH_3-Plasma Treatment $NiTiO_3$ TFT	−0.86	238	18.72	8.53×10^6	26.9
Control $NiTiO_3$ TFT	−0.93	245	11.96	2.61×10^6	7.3

Chapter 5

Conclusions and Further Works

In this chapter, we will summarize the critical consequences of capacitors and polycrystalline-silicon thin-film transistors with high-κ $NiTiO_3$ gate dielectrics prepared by sol-gel spin coating method as mentioned in previous chapters and make conclusions for this thesis.

5.1 Conclusions

In this thesis, the SPC poly-Si TFTs with high-κ $NiTiO_3$ gate dielectric successfully prepared by sol-gel spin coating method are studied. The sol-gel spin coating method is a novel low-temperature technique to form thin films of gate dielectric or active channel at room temperature. We initially analyze the material properties of spin-on $NiTiO_3$ thin films and the electrical characteristics of the capacitors with $NiTiO_3$ insulators. Then we apply this $NiTiO_3$ material in fabrication of gate dielectric for poly-Si TFTs to go a step further.

The dielectric $NiTiO_3$ films prepared by sol-gel spin coating technique are formed at different annealing temperatures from 500°C to 900°C. The X-ray diffraction (XRD) spectrum describes the crystallization temperature of the spin-on dielectric is between 600°C and 700°C. The scanning probe microscope (SPM) images display the surface morphology of the spin-on dielectric at different temperature treatments, and the surface roughness abruptly increases with the annealing temperature higher than 600°C. The electron spectroscopy for chemical analysis (ESCA) exhibits two kinds of metal-oxide bonds such as Ni-O and Ti-O in samples and the hydroxides in 200°C-baking sample. Besides, the ESCA also proves that the atomic concentration ratio of the spin-on dielectric with a 600°C-RTA treatment is [Ni]:[Ti]:[O] ~ 1:1:3. The high dielectric constant (High-κ) of the $NiTiO_3$ material calculated to be in a range

of 36 ~ 42 is extracted from the high-resolution transmission electron microscopy (HR-TEM) image and the corresponding *C-V* curves. The $NiTiO_3$ gate dielectric can achieve thin capacitance equivalent thickness (CET) and high gate capacitance density. By analyzing the *C-V* and *I-V* curves of the capacitors with the spin-on $NiTiO_3$ dielectric, we presume that the crystallization temperature of the $NiTiO_3$ material occurs near 650°C.

The SPC poly-Si TFTs with $NiTiO_3$ gate dielectric prepared by sol-gel spin coating method with 500°C, 600°C and 700°C-RTA treatments have been successfully demonstrated for the first time. The electrical characteristics of the poly-Si TFTs with $NiTiO_3$ gate dielectric (poly-Si $NiTiO_3$ TFTs) at 500°C annealing temperature are better than those at 600°C and 700°C-RTA treatments, including lower threshold voltage, steeper subthreshold swing, higher field-effect mobility and higher driving capability. With NH_3 plasma treatment, the hydrogen and nitrogen radicals can be introduced into the poly-Si films and $NiTiO_3$ gate dielectric/poly-Si channel interface to passivate the grain-boundary trap states. For this reason, the device performance and threshold-voltage rolloff properties of the poly-Si $NiTiO_3$ TFTs with a 500°C-RTA treatment can be significantly improved with NH_3 plasma passivation. The proposed poly-Si $NiTiO_3$ TFTs crystallized by SPC technique could possess good electrical properties even without additional other treatments, e.g. hydrogen (H_2) plasma, oxygen (O_2) plasma, nitrogen (N_2) plasma, etc., or other advanced phase crystallization techniques with narrow process window.

According to the results of this thesis, the $NiTiO_3$ material is a promising candidate for high-κ gate dielectric in the next generation, and the SPC poly-Si $NiTiO_3$ TFTs can be available for achieving high-speed display driving circuit applications.

5.2 Further Works

The high-κ $NiTiO_3$ material using as gate dielectric and applying in SPC poly-Si TFTs

are not the best condition and application. It is worthy to improve the integrity of the $NiTiO_3$ gate dielectric prepared by dip-coating technique in low temperature process. There are some interesting and important methods about poly-Si TFTs to be further investigated:

1) As being described in chapter 2, the $NiTiO_3$ dielectric with 600°C-RTA treatment is the best temperature condition, but it is not good enough for application to devices. In order to obtain the best thin-film characteristics, it is important to split more temperature condition between 500°C to 700°C to optimize the metal-oxide-semiconductor properties.
2) In chapter 3, the high-κ $NiTiO_3$ material is a good gate-dielectric candidate for high-performance poly-Si TFTs. However, the off-state gate-induced drain leakage (GIDL) currents of the poly-Si $NiTiO_3$ TFTs are somewhat large. The inferior GIDL currents and the on-state electrical characteristics could be further improved by using different device structures such as lightly doped drain (LDD) and field-induced drain (FID), and adopting advanced crystallization techniques such as metal-induced lateral crystallization (MILC) and excimer laser annealing (ELA) crystallization.
3) Deposition of NH_3 plasma treatment provides a good passivation on trap states near the $NiTiO_3$ gate dielectric/poly-Si channel interface. High-density plasma (HDP) and electron-cyclotron resonance (ECR) plasma are suggested to further dissociate the NH_3 into hydrogen and nitrogen radicals, and improve the efficiency of plasma passivation.
4) In addition to NH_3 plasma treatment, the other gases can also be introduced into fabrication procedures such as hydrogen (H_2), oxygen (O_2), nitrogen (N_2). Some gases for pretreatment and some for post-treatment are all appropriate processes to bring into practice.

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Study on Polysilicon Thin-Film Transistors with High-κ $NiTiO_3$ Prepared by Sol-Gel Spin Coating Method