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博 士 論 文

多重應力閘極之新穎應力記憶技術製作在 n
型金氧半場效電晶體之研究

A Study of Novel Stress Memorization Technique
on nMOSFETs by Multiple Strain-Gate
Engineering

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摘要

在本研究中，我們利用多重應力閘極之新穎應力記憶技術製作在 n 型金氧半場效電晶體來改善其電子遷移率及驅動電流，這項技術能有效克服在高密度元件電路上利用應力技術所面臨之製程整合問題，搭配上堆疊的閘極結構及預置的閘極離子佈植技術，分別達成改善 n 型金氧半場效電晶體之電子遷移率達 22% 及 31%。

在第二個階段，我們進一步對這項技術做最佳化的實驗，並試著改善由於應力所造成之元件可靠度的退化，我們實驗了不同劑量的離子佈植來增強電子通道的應力以進一步改善電子遷移率，我們發現閘極氧化層可靠度退化的程度正比於閘極離子佈植的劑量。另外，我們也實驗不同的熱退火技術應用在應力記憶技術中，我們利用提高熱退火的溫度來達到額外改善電子遷移率達 6%，再者，我們應用雙重退火技術，更進一步的將電子遷移率增強 12%，此外，應用高溫熱退火技術能有效改善閘極氧化層的可靠度，而且這兩種熱退火技術也都能改善元件熱載子效應之可靠度。我們更進一步的探討當這項技術運用在動態臨限電壓場效電晶體(DTMOS)時元件的特性，當同時運用這項應力技術與動態臨限電壓場效電晶體結構，我們可以更進一步的改善元件的驅動電流及電子遷移率達 60%，並且可以得到較低的臨限電壓。

在第三個階段我們針對此應力技術對於溫度變化的效應做一系列的檢測與分析，我們從低溫-40 度到高溫 120 度的溫度區間分析元件的特性及可靠度，我們發現利用這個新穎的應力技術及多重應力閘極結構來改善電子遷移率在高溫的環境下，電子遷移率改善的幅度會縮小，縮小的幅度會隨著溫度愈高而愈顯著，而且在室溫時應力效果愈大的實驗條件，在高溫時縮小的幅度也愈大，這個現象並不是來自於臨限電壓在高溫時的改變所造成，我們認為是應力在高溫的環境中減弱所導致，而我們從低溫到高溫的分析結果也驗證了這個推論。最後我們針對零溫度係數對於此應力技術的影響來作分析與討論，零溫度係數的閘極電壓 $V_g(\text{ZTC})$ 會因為較強的應力而降低，這個原因是來自於較強的應力元件改善其電子遷移率的同時，應力會造成矽能階隙(Si energy band gap)縮小而降低了元件的臨限電壓，使得零溫度係數的閘極電壓也隨之下降，這是對於元件與電路設計有利的結果，從以上的分析結果我們發現利用這個新穎的應力技術搭配多重應力閘極結構對於溫度的敏感度會比沒有施加應力的元件來的高，且應力愈大，敏感度也愈高，這個結果有助於了解在探討利用應力改善載子遷移率時，溫度效應的變化對於元件特性的影響。

A Study of Novel Stress Memorization Technique on nMOSFETs by
Multiple Strain-Gate Engineering

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Abstract

To extend carrier mobility improvement by strain engineering in high density and small gate space CMOS circuits, we have proposed a new stress memorization technique (SMT) that uses strain proximity free technique (SPFT) to demonstrate mobility improvement through multiple strain-gate engineering. The electron mobility of nMOSFETs with SPFT exhibits a 15% increase over counterpart techniques. Compared with conventional SMT, SPFT avoids the limitation of stressor volume for performance improvement in high density CMOS circuits. We found that optimization of stacked gate structure in combination with SPFT can improve mobility further to 22% more than a single-poly-Si gate structure without SPFT. We also found that the pre-amorphous layer (PAL) gate structure in combination with SPFT can improve mobility further, to 31% greater than standard devices. Moreover, an additional 30% mobility enhancement can be achieved by using dynamic threshold voltage MOS (DTMOS) and combining PAL gate structure with SPFT, respectively. Gate dielectric

and channel-hot-carrier reliability are also analyzed. Our results show mobility improvement by SPFT, a slightly increased gate leakage current, and degraded channel-hot-carrier reliability. Gate leakage and gate dielectric interface states can be effectively improved by optimizing thermal annealing process in SPFT. Furthermore, we found that the gain in electron mobility in the SPFT in combination with PAL gate structure decreases at high temperatures. Gate dielectric interface states and ionized gate impurities inducing carrier scattering will play important roles when operating devices under high temperature conditions. Zero temperature coefficient (ZTC) is also discussed for designing CMOS circuit work over an operated temperature. It is found that the $V_g(\text{ZTC})$ is decreased when using SPFT and in combination with PAL gate structure. Strong correlation between $V_g(\text{ZTC})$ and device threshold voltage (V_{th}) appears to explain this phenomenon. Moreover, insignificant V_{th} deviation is found in SPFT and in combination with PAL gate structure at various temperatures. Gate dielectric interface traps and channel strain degradation may be the root causes of decreasing gain in electron mobility for SPFT with PAL gate structure under high temperature conditions.

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