Chapter 1. Introduction

1.1 General Background

As the scaling of CMOS structure reaches its fundamental limits, the improvement of carrier mobility has been intensively studied by introducing strain in the channel region. This has been demonstrated in a strained Si devices on SiGe substrate which have been used the lattice mismatch between Si and SiGe. Theoretical calculations indicate that Si strained in biaxial tension should exhibit a higher mobility than bulk Si. The tensile strain induced quantization in the MOS inversion layer formed by the triangular potential well splits the six-fold degenerate Si conduction band minimum into a two-fold (Δ_2) and a four-fold (Δ_4) degenerate band. A self-consistent Schrödinger-Poisson solution was used to determine the sub-band splitting. The population of the Δ_2 and Δ_4 bands is then the total number of electrons in all of their respective sub-bands. The energy difference ΔE between Δ_2 and Δ_4 bands will determine the total relative population of the bands. Since electrons preferentially populate the Δ_2 band, which is lower in energy, the electron mobility enhancement due to the stronger population primarily reflects the reduction in inter valley phonon scattering, and the reduced in-plane effective mass in this band [1-7]. However, the fabrication of the conventional strained Si devices is more complicated, such as forming a relaxed SiGe buffer layer. Recent studies have shown that the uniaxial

strained channel from a contact etch stop layer (CESL) and embedded SiGe (eSiGe) in the source/drain area [8-11]. Stress memorization technique (SMT) has been reported to enhance electron mobility on nMOSFETs and has been widely studied using a variety of approaches [12-14]. However, most previous studies have demonstrated the performance boost without considering the scalability of the gate density. As the scaling of design rules such as poly pitch shrinks in high density SRAM circuits (as shown in Fig. 1-1), mobility enhancement will be limited by stressor volume and process integration issues. The introduction of longitudinal tensile stress and vertical compressive stress into the channel region are well known principles of mobility enhancement in nMOSFETs [15]. However, longitudinal tensile stress will be limited as the stressor volume reaches its saturation point, causing performance degradation [16]. Moreover, poor metal salicide formation and contact process integration issues will be induced by stressor residue in high density CMOS circuits, as illustrated in Fig. 1-2.

In this work, we propose a strain proximity free technique (SPFT) to circumvent the limitation of stressor volume for performance improvement in high density circuits. A stacked a-Si/poly-Si gate structure has been reported to enhance channel stress and electron mobility [17]. We have proposed a pre-amorphous layer (PAL) gate structure using implantation process to further improve performance on nMOSFETs.

Dynamic threshold voltage MOS (DTMOS), which lowers the threshold voltage of MOSFETs only in active operation, is proposed for high speed and low power applications [18-19]. DTMOS realizes a higher saturation current in active mode and a lower leakage current in standby mode. We have applied DTMOS and combined it with SPFT to demonstrate further performance improvement without increasing standby power consumption. Gate oxide and channel hot carrier reliability are also discussed for characterizing performance improvement and device reliability on the strain engineering. Temperature dependence of electron mobility in the strain gate structure is also discussed. In order to extend the applications of devices operating across wide temperature ranges, analysis of the electrical properties at various temperatures is required. Phonon scattering dominating electron mobility at high temperatures by lattice vibration is a well known mechanism in Si. We have found that the gain in electron mobility in SPFT in combination with PAL gate structure decreases at high temperatures. Gate dielectric and Si interface properties are investigated to explain this phenomenon. Furthermore, zero-temperature-coefficient (ZTC) point, which is an important parameter for CMOS circuits work over an operated temperature, is also discussed in order to check strain dependence of temperature effect on the SPFT in combination with PAL gate structures.

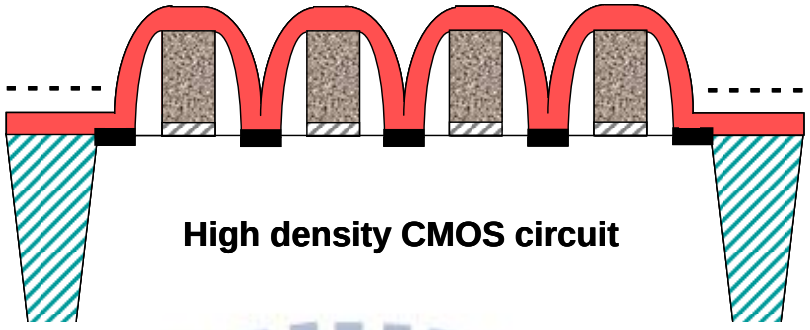


Fig. 1-1

1-2 Thesis Organization

This dissertation is divided into five chapters as follows:

In chapter 1, a brief general background of strained Si device is introduced to describe the various characteristics. Then we discuss recent studies in stress memorization technique (SMT) and motivation of our study. The organization throughout this dissertation is described here.

In chapter 2, we proposed a strain proximity free technique (SPFT) to avoid the limitation of stressor volume for performance improvement in high density CMOS circuits. Device performance, reliability and material analysis of SPFT is discussed in this section.

In chapter 3, we have demonstrated an improvement of electron mobility and Ion-Ioff performance on nMOSFET using SPFT in combination with stacked gate structure. It utilizes a stacked poly-Si structure with combining a different grain size

of poly-Si by controlling the process conditions. Channel hot carrier reliability is also discussed for characterizing device reliability on the strain engineering.

In chapter 4, we have proposed a pre-amorphous layer (PAL) gate structure using implantation process to further improve performance on nMOSFETs. We have applied DTMOS and combined it with SPFT to demonstrate further performance improvement without increasing standby power consumption. Gate oxide and channel hot carrier reliability are also discussed in this section.

In chapter 5, the temperature dependence of electron mobility and current drivability in SPFT are discussed. Furthermore, zero-temperature-coefficient (ZTC) point, which is an important parameter for CMOS circuits work over an operated temperature, is also discussed in order to check strain dependence of temperature effect on the SPFT and DTMOS SPFT in combination with PAL gate structures.

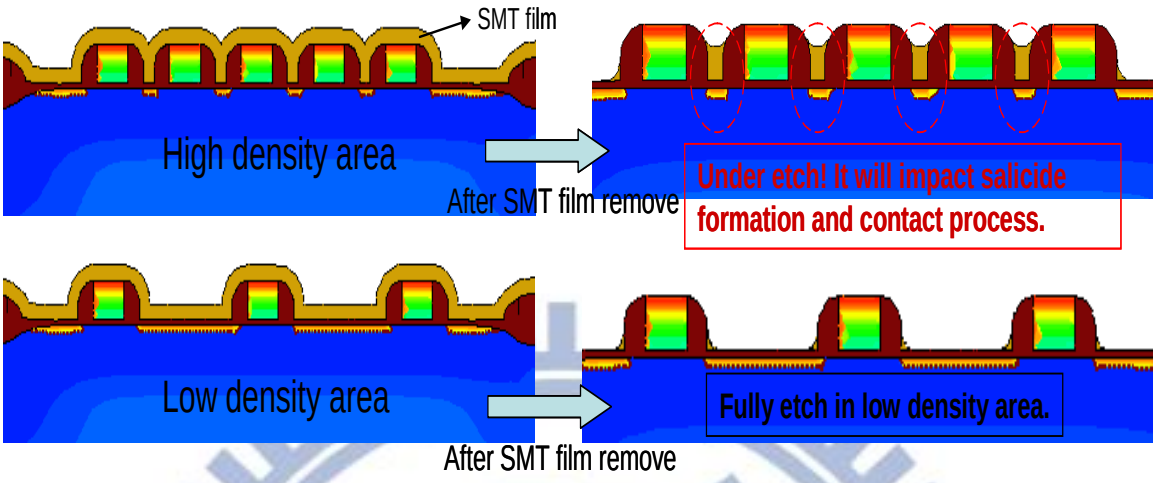


Fig. 1-2 Process integration issues by stressor remain in high density circuits

Chapter 2. Strain Proximity Free Technique (SPFT)

2.1 Introduction

In pursue of high speed circuit applications, mobility enhancement by local stressor engineering in high performance CMOS transistors has been intensively studied, using techniques such as dual contact etch stop layer (DCESL) and embedded SiGe (eSiGe) in the source/drain area. Recently, stress memorization technique (SMT) has been reported to enhance electron mobility on nMOSFETs and widely studied by different methods. However, most previous studies have demonstrated the performance boost without considering the scalability of the gate density. As the scaling of design rules such as poly pitch shrinks in high density SRAM circuits (as shown in top of the Fig. 2-1.), mobility enhancement will be limited by stressor volume and process integration issues. Introducing longitudinal tensile stress and vertical compressive stress into the channel region are the well known principles of mobility enhancement on nMOSFETs. However, longitudinal tensile stress will be limited as the stressor volume reaches its saturation point, causing performance degradation. Moreover, poor metal salicide formation and contact process integration issues will be induced by stressor residue in high density CMOS circuits. In this work, we proposed a strain proximity free technique (SPFT) to avoid the limitation of stressor volume for performance improvement in high density CMOS circuits. The SPFT is processed before gate

patterning. It can avoid the limitation of stressor volume in small gate pitch devices. The SPFT shows significant electron mobility improvement and device performance boost. Gate dielectric and channel hot carrier reliability is also discussed in this section.

2.2 Experiments

nMOSFETs were fabricated on 6-in wafers with resistivity of 15-25 Ω-cm. After the RCA cleaning process, 2.5 ± 0.1 nm gate-oxide and poly-Si 200nm were grown in a vertical furnace. Then, the stacked gate structure was built using pre-amorphous implantation (PAI) by arsenic atom implantation. The arsenic energy and dosage in the experiment was 30KeV $1x10^{15}cm^{-2}$. The SPFT, whose process flow of SPFT is illustrated in Fig. 2-1, is proposed in order to introduce stress into the channel region. Before patterning on the poly-Si gate, the SPFT is introduced by high tensile stressor deposition, rapid thermal annealing (RTA) and stressor removed processes. The stressor of SPFT in this experiment is a high tensile thermal CVD SIN film of thickness 100nm. The stress level of this film is near 1.3GPa. 2-step dry and wet etching was used in the stressor removal process. After gate patterning, source/drain extension (SDE) implantation, side wall spacer and S/D formation are processed. A 100nm thermal CVD tensile SiN CESL is deposited on all transistors. After inter layer

dielectric (ILD) film deposition and contact patterning, a four-level metallization (Ti-TiN-Al-TiN) was carried out in PVD system.

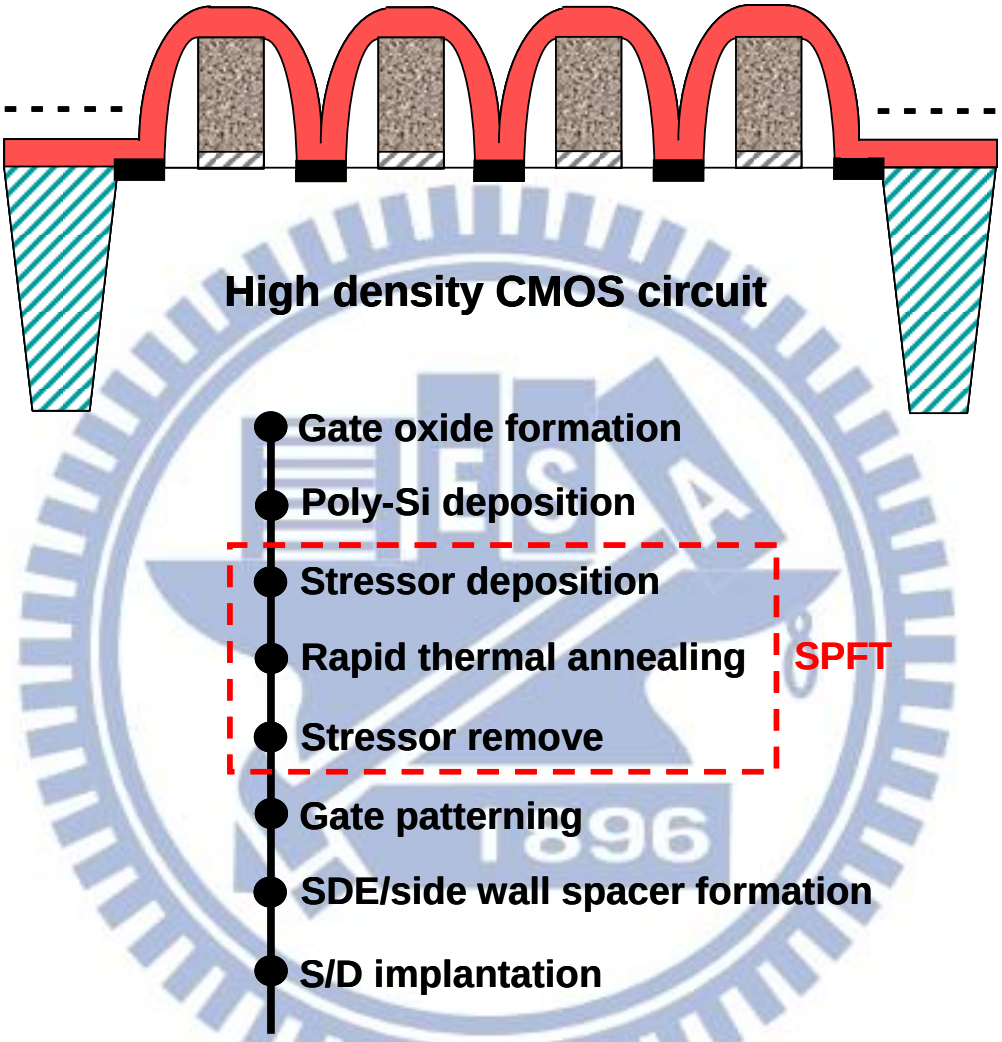


Fig. 2-1 Process flow of SPFT

2.3 Results and Discussions

The gate oxide reliability is confirmed by testing breakdown voltage (VBD). The SPFT shows a comparable VBD (=5V) performance to the standard devices. The C-V characteristics of SPFT are illustrated in Fig. 2-2. The SPFT and combines SPFT with PAI show comparable capacitance to standard devices. The gate oxide thickness of SPFT and SPFT with PAI is 26.5+/-0.3A which is comparable to standard devices. The performance improvement for the nMOSFET is illustrated in Fig. 2-3. The SPFT shows a 16% mobility improvement on device channel width/length = 10/0.4um. The corresponding Ion characteristic of SPFT is also shown in the inset in Fig. 2-3. The SPFT shows a 9% Ion improvement at Ioff = 20pA, compared to that of the standard devices.

Since the SPFT is applied to introduce stress into the channel region before gate patterning, it can avoid the problems of stressor volume and small gate pitch in high density circuits. We have split conventional SMT with the same stressor material and thickness in this experiment. The SPFT shows a comparable device performance to the typical SMT. A qualitative model is proposed to explain the mechanism of SPFT. In Ref.[20,21,22], it was reported that the vertical compressive stress is the major component of stress in SMT processes. In the SPFT approach, the RTA has transferred the high tensile stress from the disposable stressor to the gate poly-Si, resulting in the

inducing of a plastic strain in the poly-Si. To compensate this external stress from the disposable stressor, a very high vertical compressive strain is induced in the poly-Si. The deformation of the poly-Si is expanded in the longitudinal direction and compressed in the vertical direction. This further creates the longitudinal tensile stress and vertical compressive stress in the Si channel. After stressor removal, the high longitudinal tensile stress and vertical compressive stress may be memorized in the channel region. This mechanism appears to explain the increased stress resulting from use of SPFT to enhance electron mobility.

The gate length (L_{gate}) dependence of mobility improvement is shown in Fig. 2-4. The mobility improvement of nMOSFETs is getting obviously in short L_{gate} region. This result is similar to the previous publications that the strain dependence of mobility improvement is more obviously in small gate length devices. Furthermore, a significant improvement of mobility on combining SPFT with PAI is found, as shown in Fig. 2-4. It appears that SPFT with PAI can further increase mobility to 18%. The I_d-V_d characteristics of SPFT and SPFT with PAI are shown in Fig. 2-5. I_d improvement of 10% and 12% may be achieved when using both SPFT and combining SPFT with PAI structure, respectively. The mechanism of the stress enhancement in SPFT with PAI may be as follows: the re-crystallization of the PAI region during the SPFT process leads to shrinkage of the total thickness of the stacked gate and results in

a residual compressive strain. The SPFT with PAI structure with optimization of pre-amorphous implant depth and dosage, provide more vertical compressive stress and longitudinal tensile stress to the channel region. From our AFM and SEM pictures (as shown in Fig 2-6 and 2-7), the mean grain size of the typical poly-Si is 77~106nm and the SPFT with PAI is 64~86nm. This result is similar to the data demonstrates in previous studies on SMT [23]. The poly-Si shows a smaller grain size after processing SMT. The gate length dependence of I_d improvement shows a consistent trend with mobility improvement, as shown in Fig. 2-8. Higher I_d improvement can be achieved in small gate length devices by using SPFT and combining SPFT with PAI. The threshold voltage Vt_lin and Vt_sat of SPFT and SPFT with PAI are shown in Fig. 2-9 and 2-10. The SPFT and SPFT with PAI show -15~-20mV Vt_lin and -10~-15mV Vt_sat lower than standard devices. It is suspected by strain inducing energy band gap narrowing and decreasing the threshold voltage. The sub-threshold swing of SPFT and SPFT with PAI is illustrated in Fig. 2-11. Both of SPFT and SPFT with PAI show comparable swing ~85mV/V to standard devices. The drain induced barrier lowing (DIBL) of SPFT and SPFT with PAI are also comparable to standard devices. The dependence of the channel-hot-carrier reliability is shown in Fig. 2-12 and 2-13. We found that the shift of the threshold voltage ($\triangle V_{th}$) and transconductance ($\triangle$Gm) is slightly higher in SPFT and SPFT with PAI as a function of the stress time. This result

is attributed to the improved drain current under the same bias conditions and induced higher substrate current. Since mobility enhancement is related to the stress induced energy bandgap narrowing, it will accompany modification of the impact ionization rate and channel hot carriers in the Si substrate.

2.4 Summary

We have proposed a multiple strain-gate engineering that utilizes the SPFT and a stacked gate structure by using PAI. The electron mobility and current drivability may be improved by controlling the SPFT process and the thickness of the stacked gate structure. Channel hot carrier reliability is slightly degraded as the channel stress is increased. Without the limitation of stressor volume in high density CMOS circuits, we believe this scheme that combines SPFT with a stacked gate structure will serve as an important guide for continued improvement in future CMOS technology.

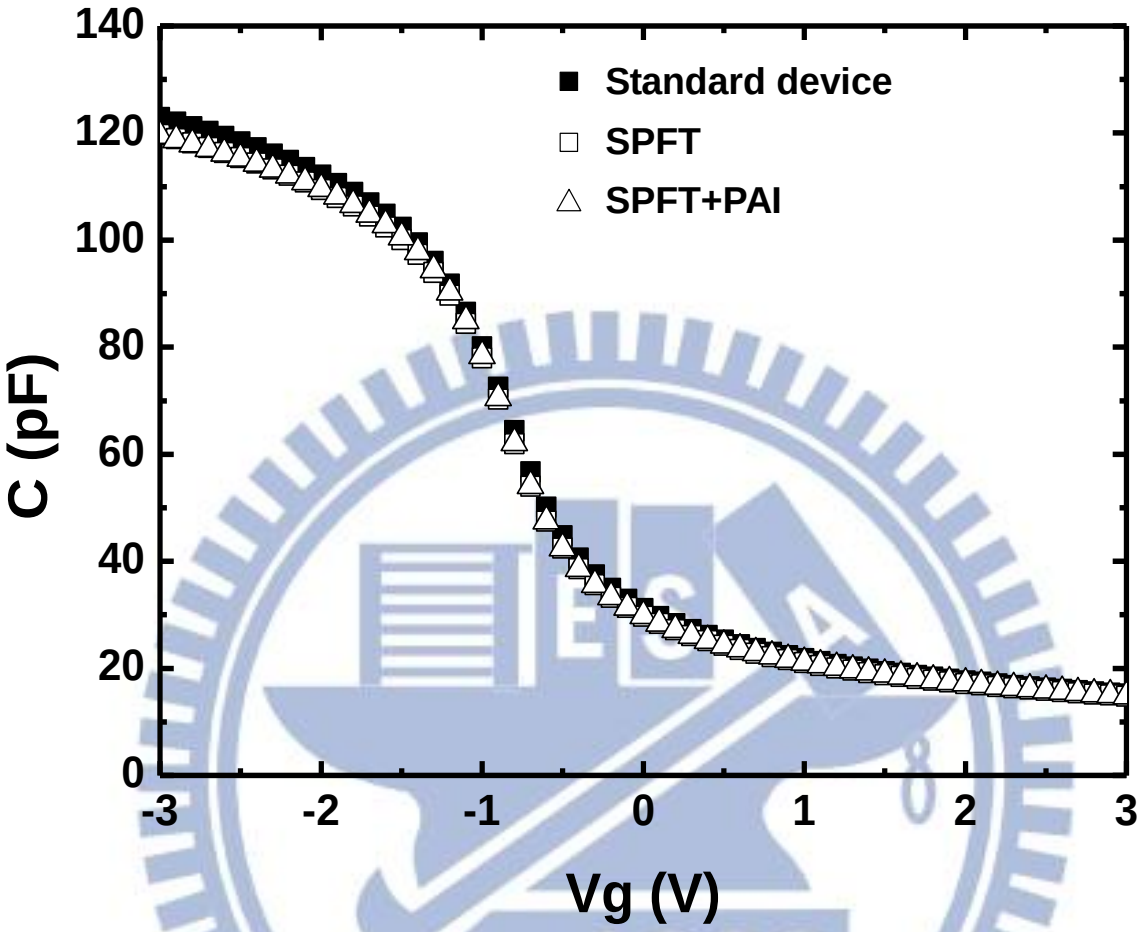


Fig. 2-2 C-V characteristics for SPFT and SPFT+PAI

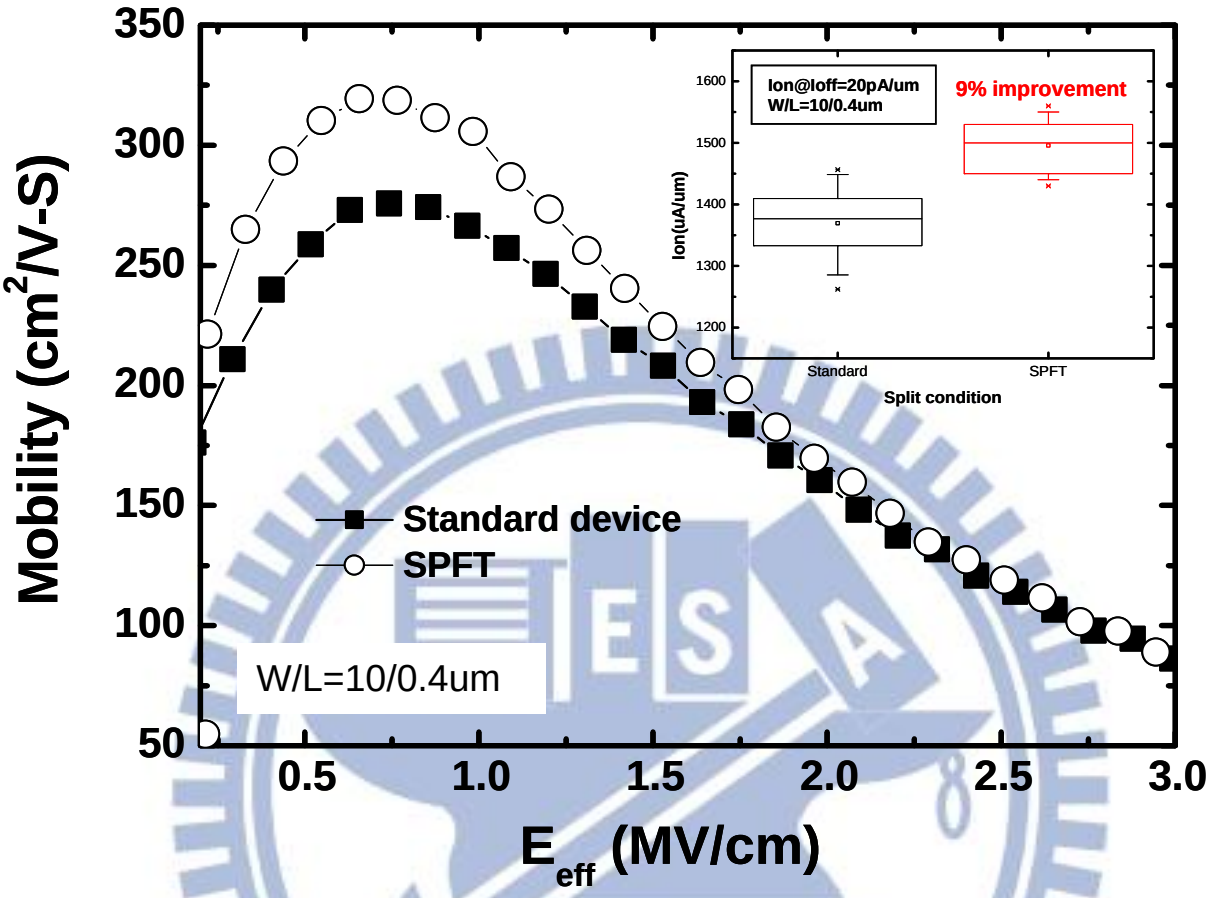


Fig. 2-3 Electron mobility and Ion@Isof=20pA/um for standard device and SPFT

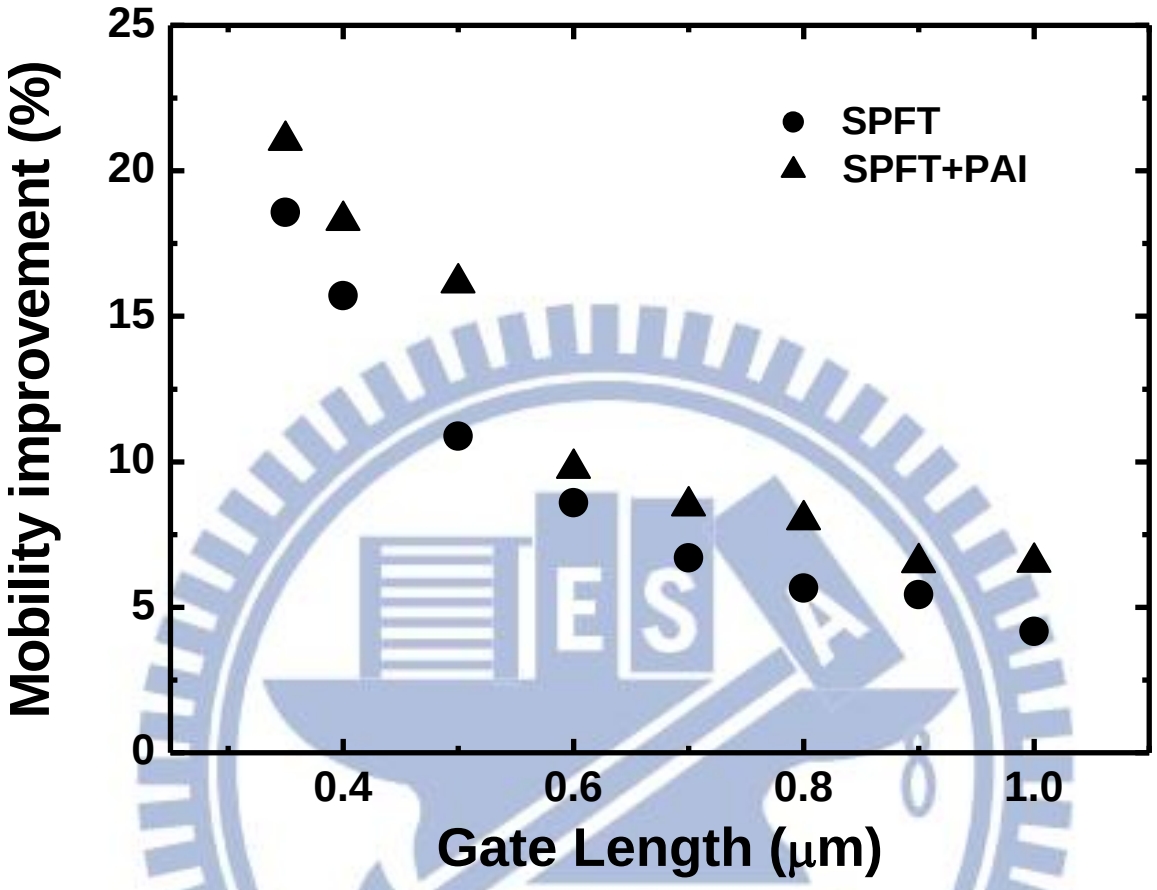


Fig. 2-4 Electron mobility improvement of SPFT and SPFT+PAI

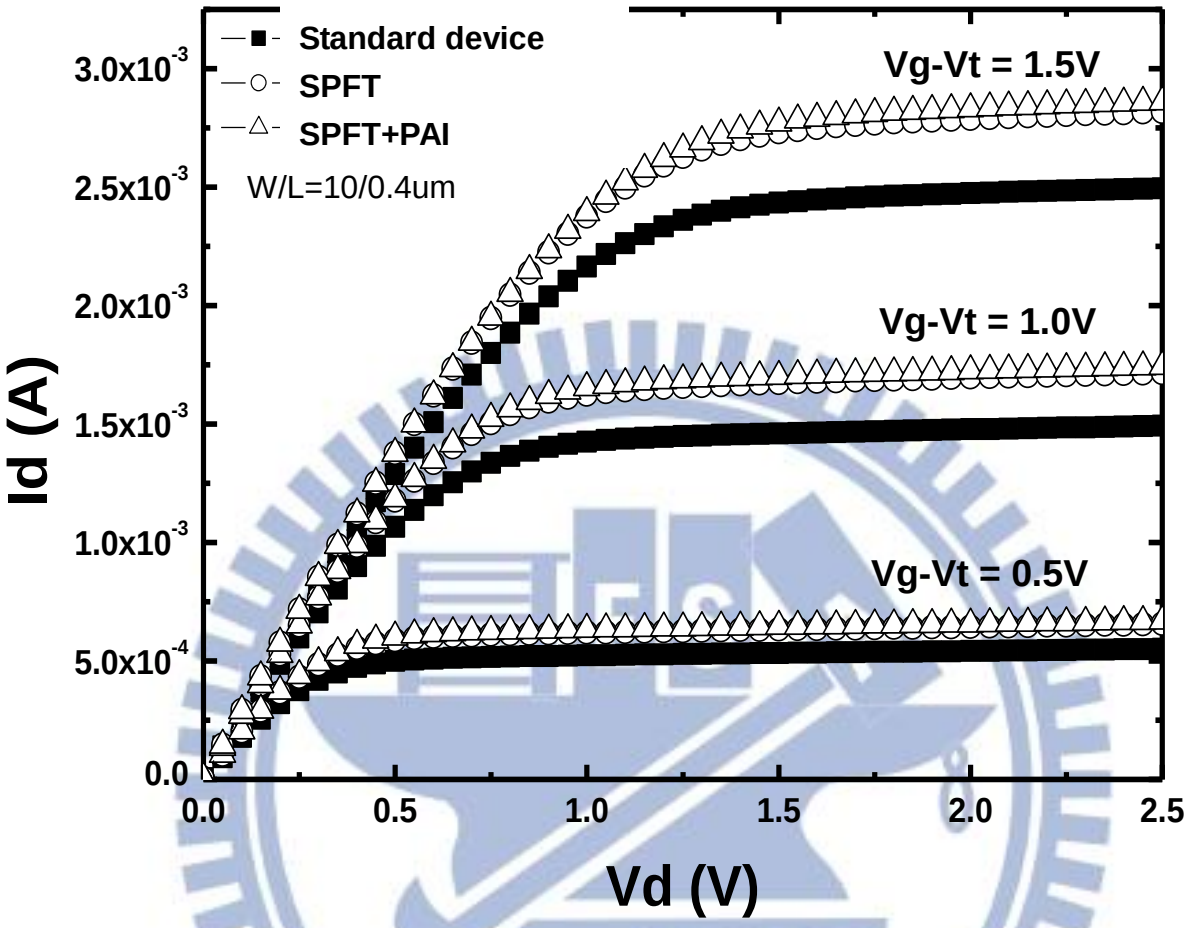
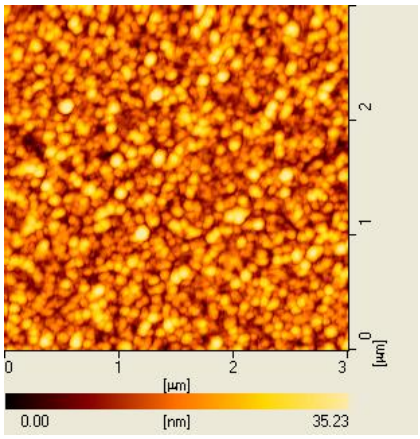
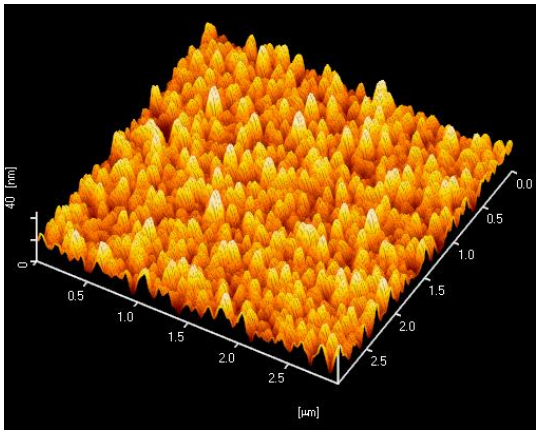
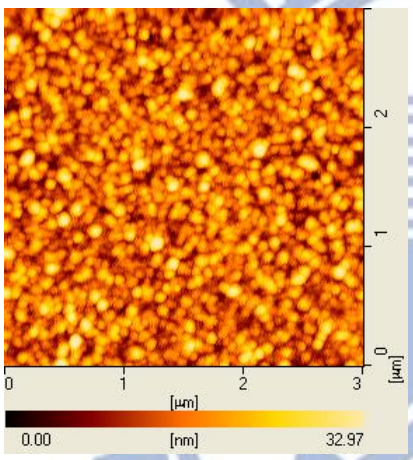


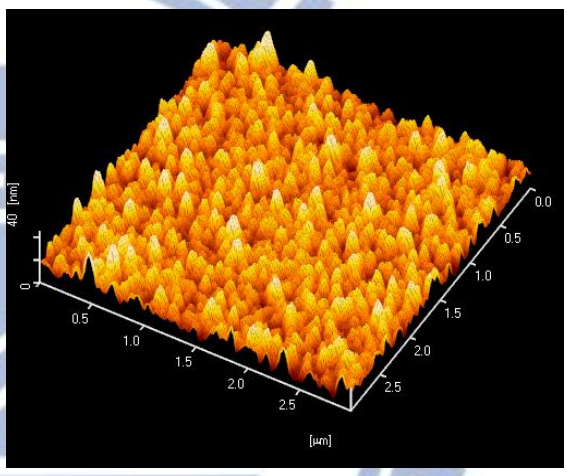
Fig. 2-5 Id-Vd charateristics for SPFT and SPFT+PAI





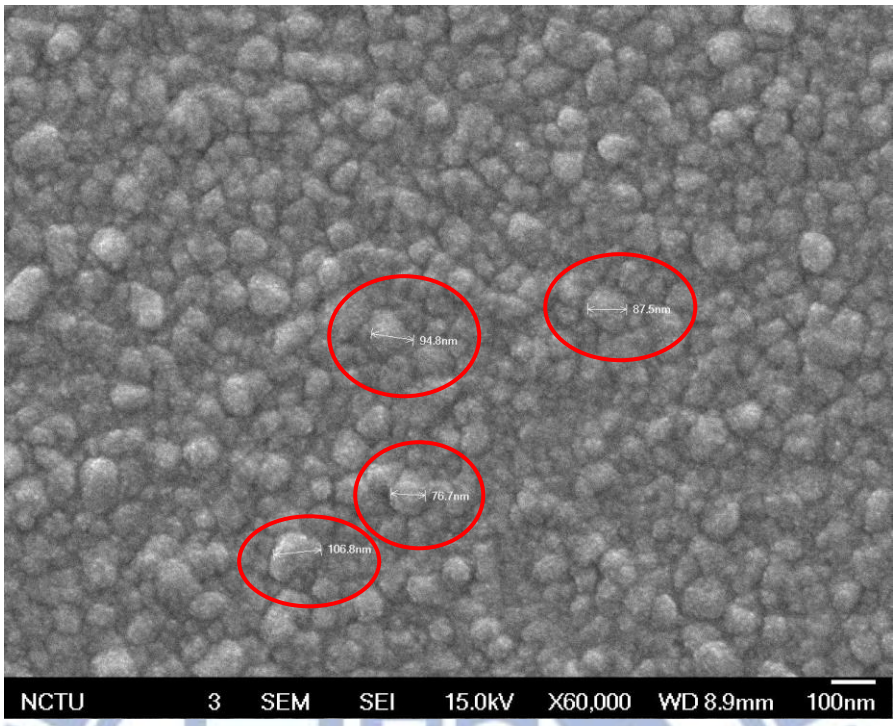
(a) AFM image for standard device (b) 3-D AFM image for standard device



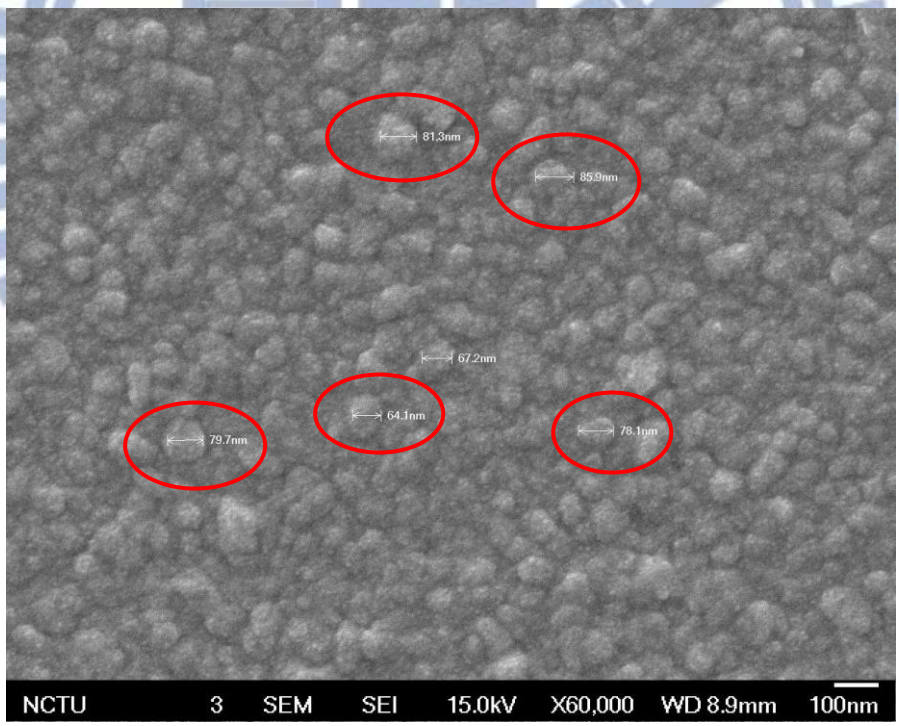


(c) AFM image for SPFT (d) 3-D AFM image for SPFT

Fig. 2-6 AFM images for standard device and SPFT. Poly mean grain size of standard device is 94 nm and 72 nm for SPFT.



(a) SEM image for standard device



(b) SEM image for SPFT.

Fig. 2-7 SEM images for standard device and SPFT. The poly grain size for standard device is 77 nm to 106 nm and for SPFT is 64 nm to 79 nm.

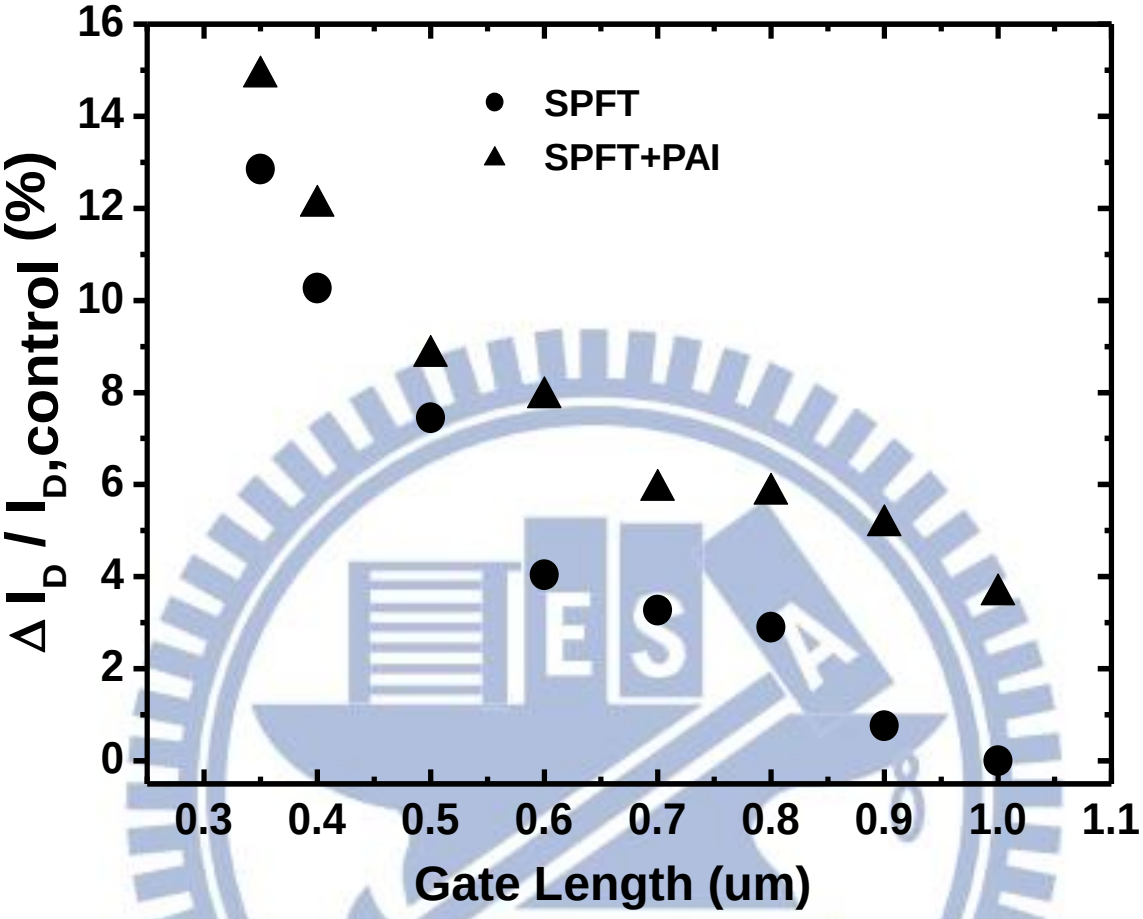


Fig. 2-8 Drain current Id improvement of SPFT and SPFT+PAI

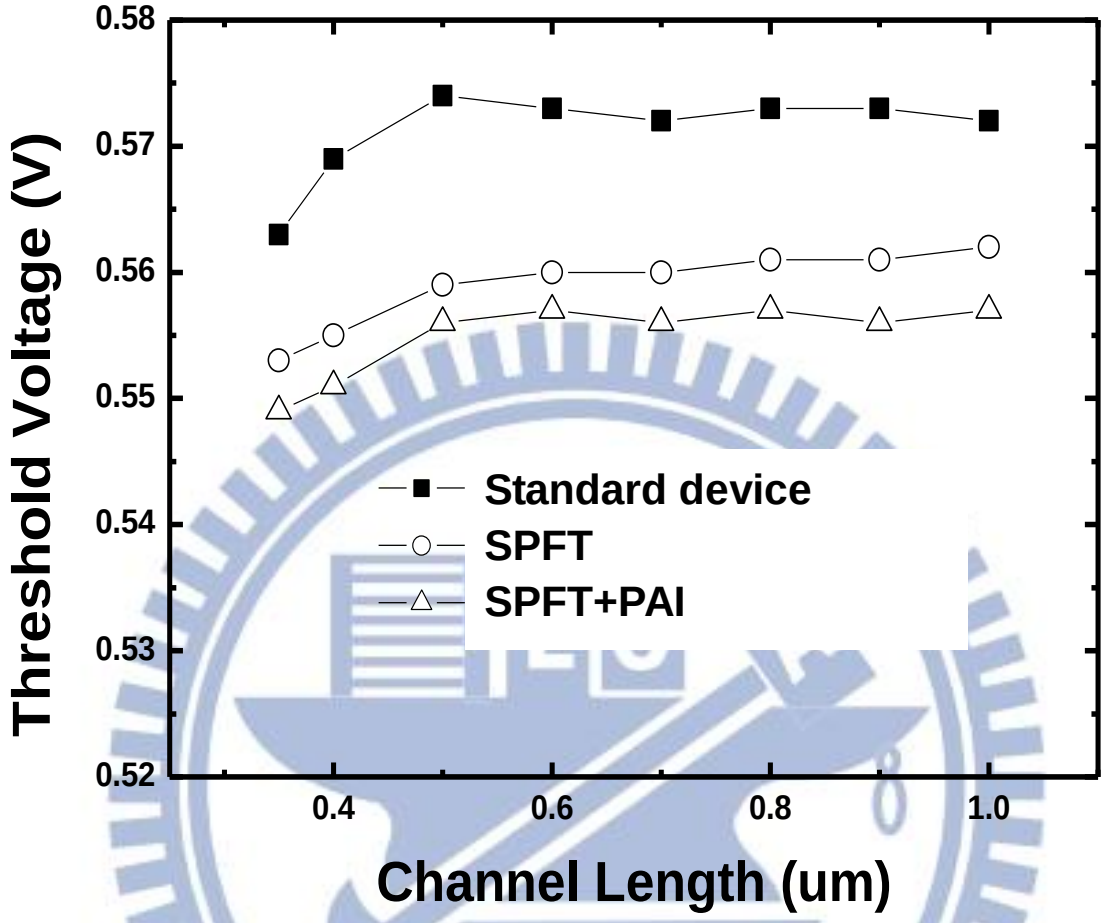


Fig. 2-9 Threshold voltage Vt_lin for SPFT and SPFT+PAI

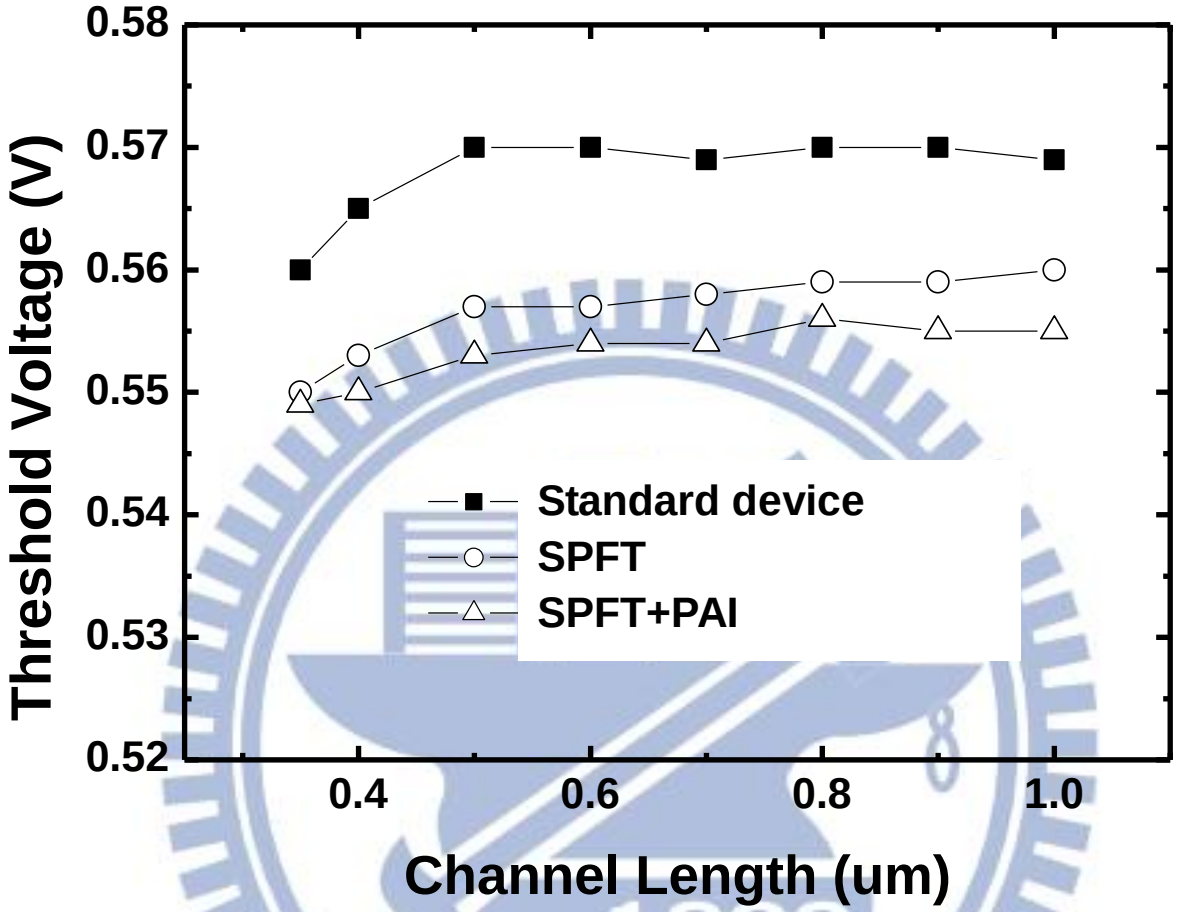
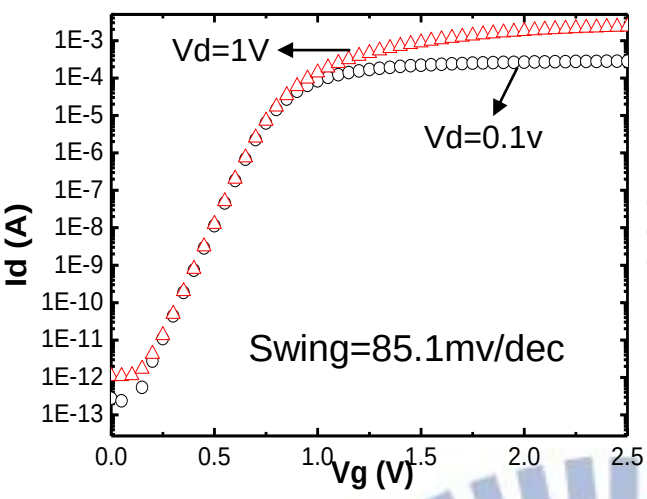
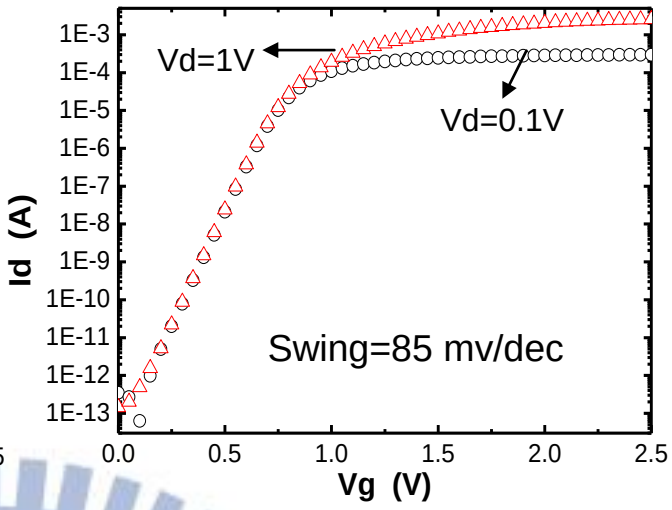


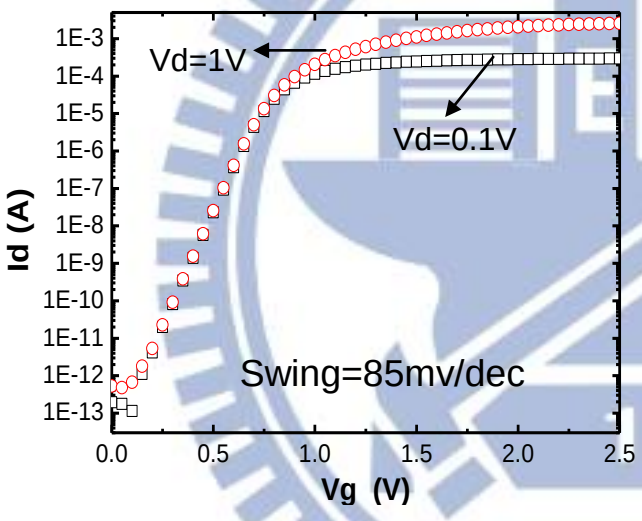
Fig. 2-10 Threshold voltage Vt_sat for SPFT and SPFT+PAI



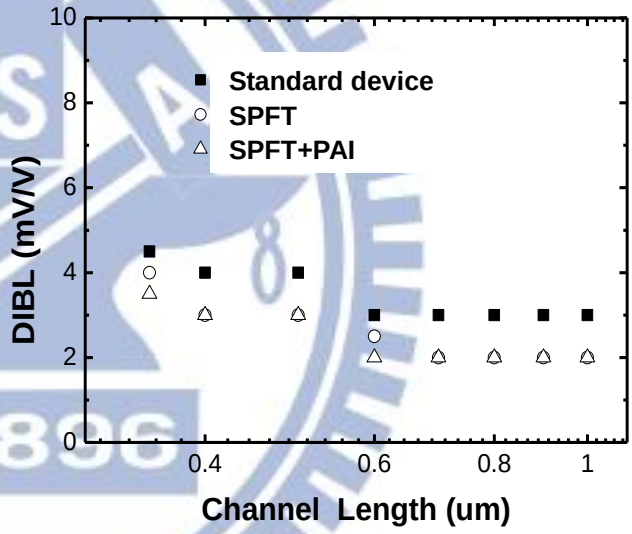
(a) Standard device



(b) SPFT



(c) SPFT+PAI



(d) DIBL for SPFT and SPFT+PAI

Fig. 2-11 Sub-threshold swing and DIBL for SPFT and SPFT+PAI

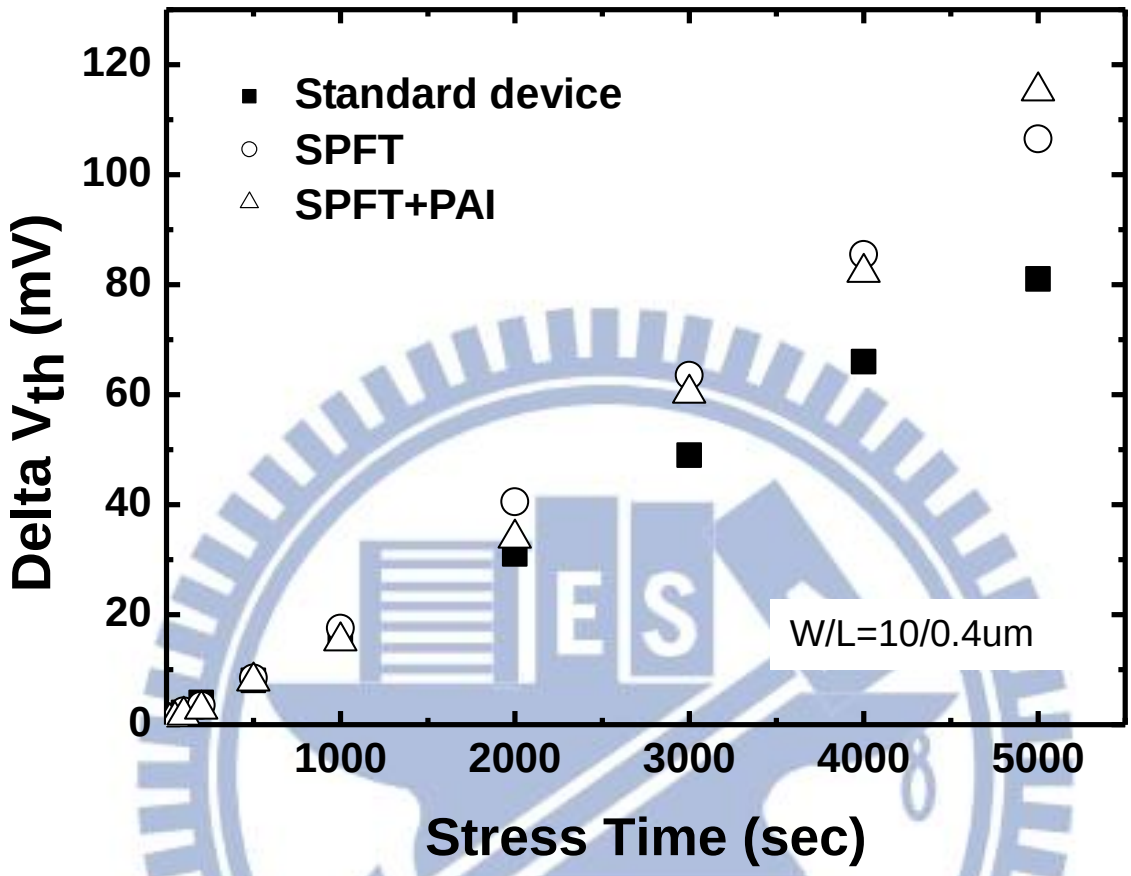


Fig. 2-12 Channel hot carrier reliability (Delta Vth) for SPFT and SPFT+PAI

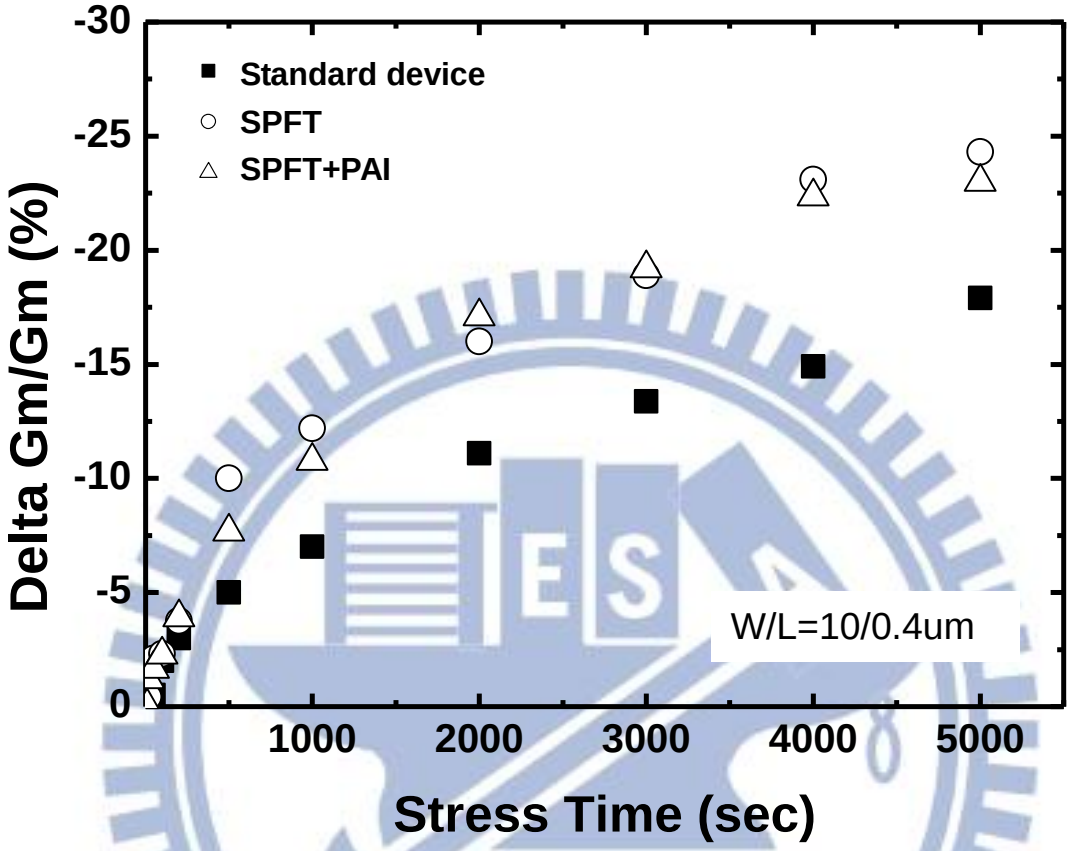


Fig. 2-13 Channel hot carrier reliability (Delta Gm) for SPFT and SPFT+PAI

Chapter 3. SPFT with Stacked Gate Structure

3.1 Introduction

As the scaling of design rules for sub-45nm CMOS technology, mobility improvement by strain engineering will be limited by the narrowing gate space environment. Stressor volume limitation and process integration issues are the big challenges for performance boost on low power and high speed circuits. Capping stressor CESL and stress memorization technique (SMT) have been reported to improve electron mobility on nMOSFETs and widely studied by different methods. However, most previous studies have demonstrated the performance boost without considering the scalability of the gate space in high density circuits. Introducing longitudinal tensile stress and vertical compressive stress into the channel region are the well known principles of electron mobility improvement. However, longitudinal tensile stress becomes limited as the stressor volume reaches its saturation point, causing performance degradation. Besides, process integration issues like poor salicide formation and abnormal contact resistance are induced by stressor residue in narrowing gate space circuits.

Strain-proximity-free technique (SPFT) has been demonstrated to offer performance improvement without the limitation of stressor volume in high density CMOS circuits [24]. Electron mobility and driving current of nMOSFETs are

improved by inserting a capping stressor and carrying out thermal annealing before gate patterning. In this study, we have demonstrated an improvement of electron mobility and Ion-Ioff performance on nMOSFET using SPFT in combination with stacked gate structure. It utilizes a stacked poly-Si structure with combining a different grain size of poly-Si by controlling the process conditions. Re-crystallization of the stacked poly-Si during thermal annealing processes is expected to introduce strain into the channel to improve electron mobility. Both mobility and current drivability are improved from single SPFT. Channel hot carrier reliability is also discussed for characterizing device reliability on the strain engineering.

3.2 Experiments

nMOSFETs were fabricated on 6-in wafers with resistivity of 15-25 Ω-cm. After the RCA cleaning process, 2.5 ± 0.1 nm gate-oxide was grown in a vertical furnace (800℃, O_2 ambient). Then, the stacked gate structure was built using poly-Si with optimization of bottom layer poly-Si grain size, thickness by controlling process temperature and deposited in the same ambient. The bottom layer thickness of the stacked gate is near 70nm. The final gate thickness was kept the same for all samples, 200-nm. The SPFT whose process flow of stacked gate structure with SPFT is illustrated in Fig. 3-1, is proposed in order to introduce stress into the channel region.

Before patterning on the poly-Si gate, the SPFT is introduced by high tensile stressor deposition, rapid thermal annealing (RTA) and stressor removed processes. The stressor of SPFT in this experiment is a high tensile thermal CVD SIN film of thickness 100nm. The stress level of this film is near 1.3GPa. 2-step dry and wet etching was used in the stressor removal process. After gate patterning, source/drain extension (SDE) implantation, side wall spacer and S/D formation are processed. A 100nm thermal CVD tensile SiN CESL is deposited on all transistors. After inter layer dielectric (ILD) film deposition and contact patterning, a four-level metallization (Ti-TiN-Al-TiN) was carried out in PVD system.

3.3 Results and Discussions

The performance improvement for the nMOSFET is illustrated in Fig. 3-2. The SPFT shows a 16% mobility improvement on device channel width/length = 10/0.4um. A significant improvement of mobility on SPFT with stacked gate structure is found, as shown in Fig. 3-2. It appears that SPFT with stacked gate structure can further increase mobility to 24% and Id improvement of 16% may be achieved when using both SPFT and stacked gate structure. The threshold voltage of SPFT and SPFT with stacked gate structure is illustrated in Fig. 3-3. The threshold voltage (Vth) of SPFT is 15~20mV lower than standard devices. Moreover, SPFT with stacked gate structure

shows Vth ~50mV lower than SPFT. The gate length (Lg) dependence of transconductance (Gm) and drain current (Id) improvement is shown in Fig. 3-4 and 3-5. Higher Gm and Id improvement are observed in short Lg region. Poly depletion effect is not show on stacked gate structure in this experiment. The gate oxide shows a comparable thickness for both stacked gate structure and single poly-Si gate structure. In the SPFT approach, the RTA has transferred the high tensile stress from the disposable stressor to the gate poly-Si, resulting in the inducing of a plastic strain in the poly-Si. To compensate this external stress from the disposable stressor, a very high vertical compressive strain is induced in the poly-Si. The deformation of the poly-Si is expanded in the longitudinal direction and compressed in the vertical direction. This further creates the longitudinal tensile stress and vertical compressive stress in the Si channel. After stressor removal, the high longitudinal tensile stress and vertical compressive stress may be memorized in the channel region. This mechanism appears to explain the increased stress resulting from use of SPFT to enhance electron mobility.

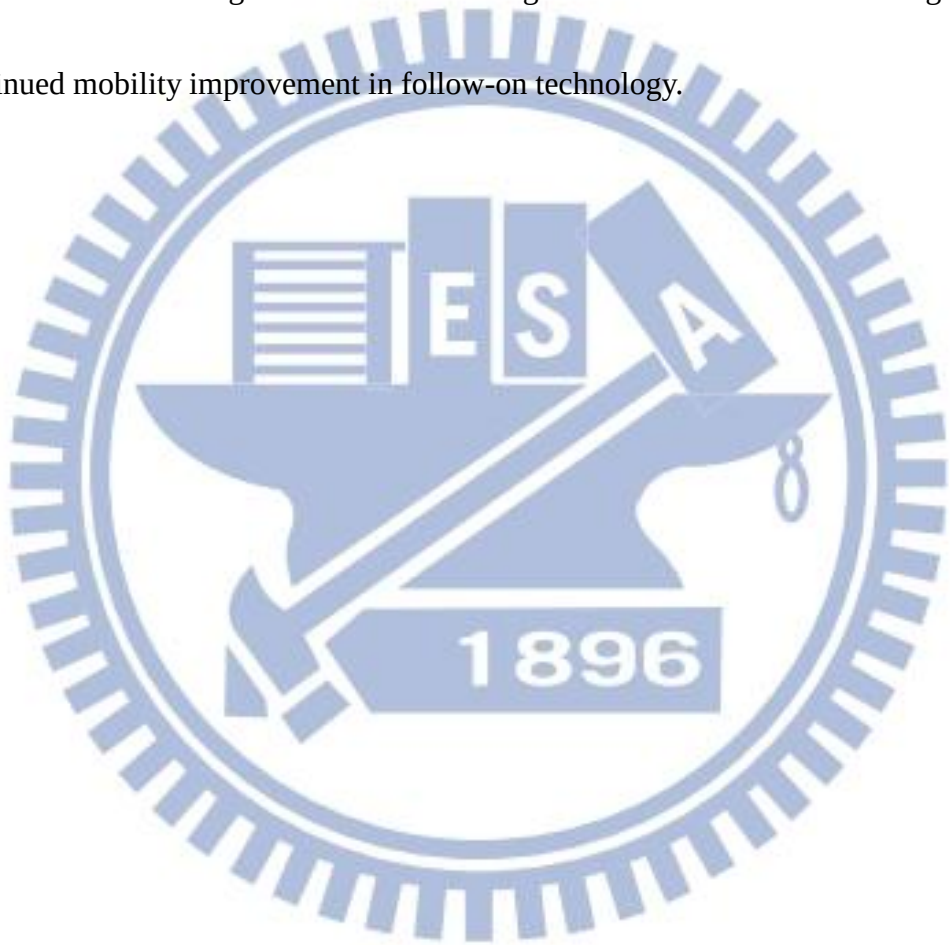
Moreover, the mechanism of the stress enhancement in stacked poly-Si gate may be as follows: the re-crystallization of the bottom poly-Si region during the SPFT process leads to shrinkage of the total thickness of the stacked gate and results in a residual compressive strain. The stacked gate structure with optimization of bottom layer

poly-Si grain size and thickness, provide more vertical compressive stress and longitudinal tensile stress to the channel region. The gate leakage of stacked random-poly-Si gate structure is comparable to single poly-Si gate which is near 0.7 pA/um for device of L/W = 10/0.4um. The substrate leakage current (Isub) of SPFT and SPFT with stacked gate structure is illustrated in Fig. 3-6. SPFT with stacked gate structure shows slightly higher Isub than single SPFT and standard devices. The dependence of the channel-hot-carrier reliability is shown in Fig. 3-7 and 3-8. We found that the shift of the threshold voltage (Δ Vth) and drain current (Δ Idsat) is slightly higher in SPFT as a function of the stress time. Moreover, SPFT with stacked gate structure shows higher Δ Vth and Δ Idsat than single SPFT. This result may be attributed to the improved drain current under the same bias conditions and induced higher substrate current in SPFT and SPFT with stacked gate structure. Since mobility enhancement is related to the stress induced energy bandgap narrowing, it may accompany modification of the impact ionization rate and channel hot carriers in the Si substrate.

3.4 Summary

We have proposed a scheme for electron mobility improvement that uses the SPFT with stacked gate structure. Both electron mobility and current drivability may be

improved by controlling the bottom layer poly-Si grain size and thickness. Poor channel hot carrier is shown in SPFT with stacked gate structure due to the improved drain current under the same bias conditions and induced higher substrate current. Without the limitation of stressor volume in high density CMOS circuits, we believe this scheme combining SPFT with stacked gate structure will serve as a guide for continued mobility improvement in follow-on technology.



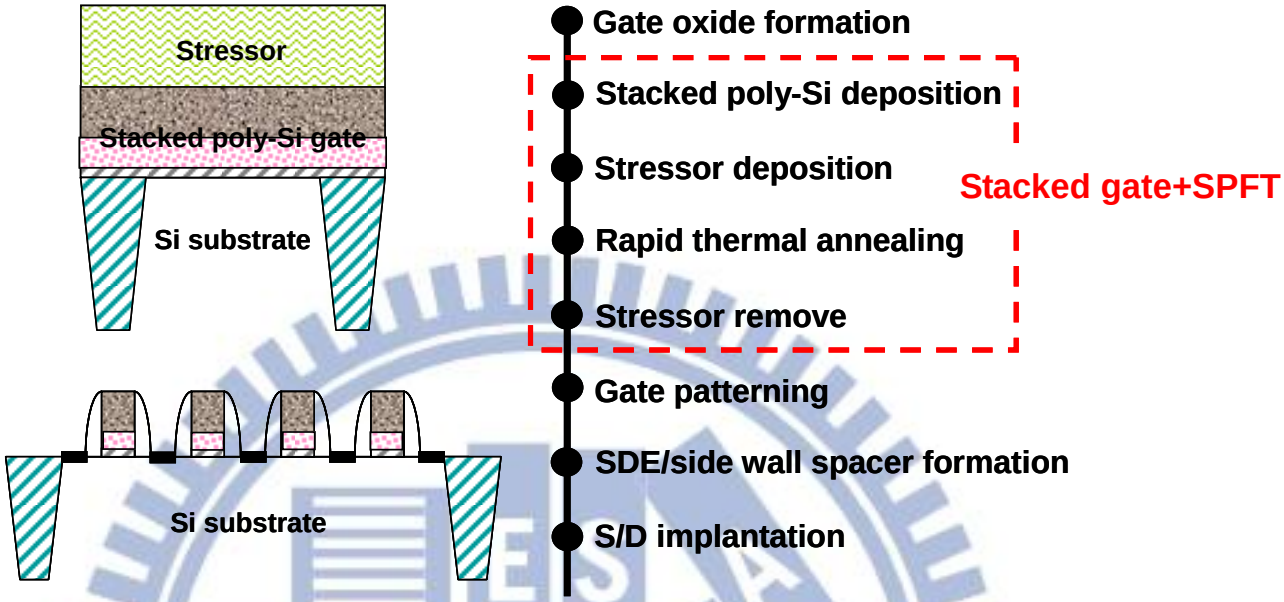


Fig. 3-1 Process flow for SPFT with stacked gate structure

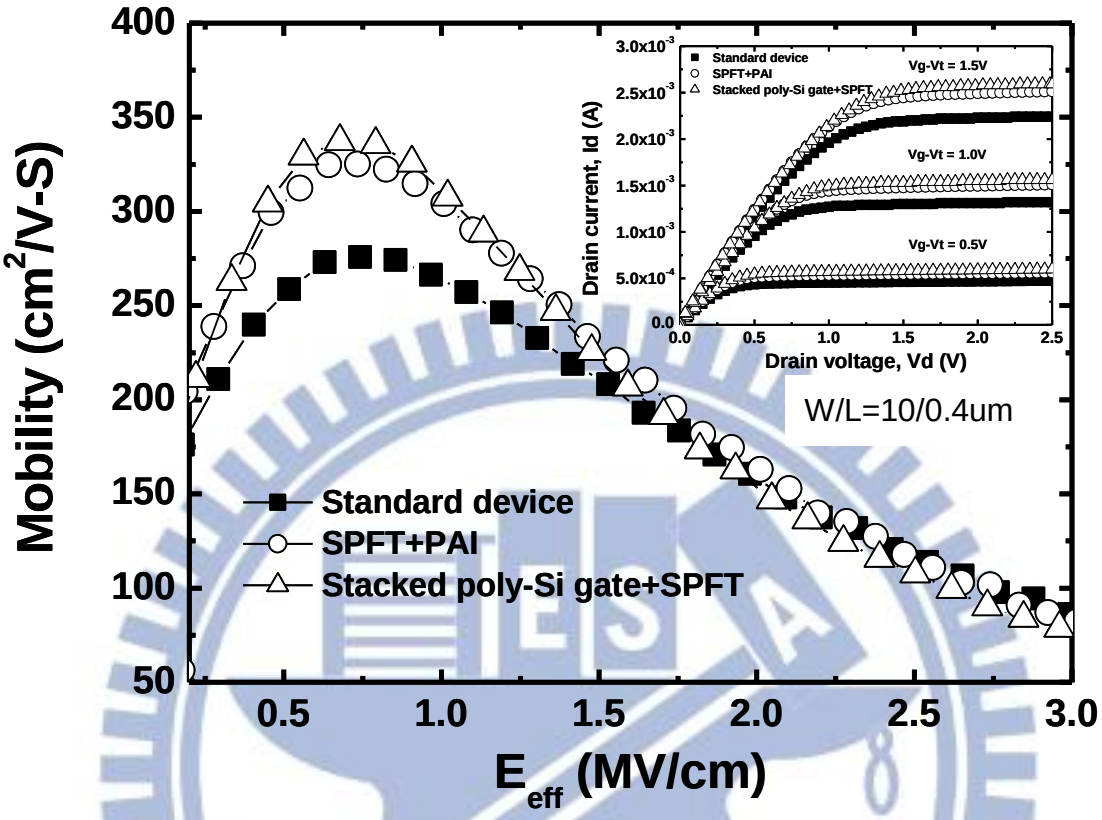


Fig. 3-2 nMOSFET electron mobility for SPFT on channel width/length = 10 um/0.4 um. Single Poly-Si gate 200nm is as a standard device. In the inset, the corresponding Ion characteristic is shown.

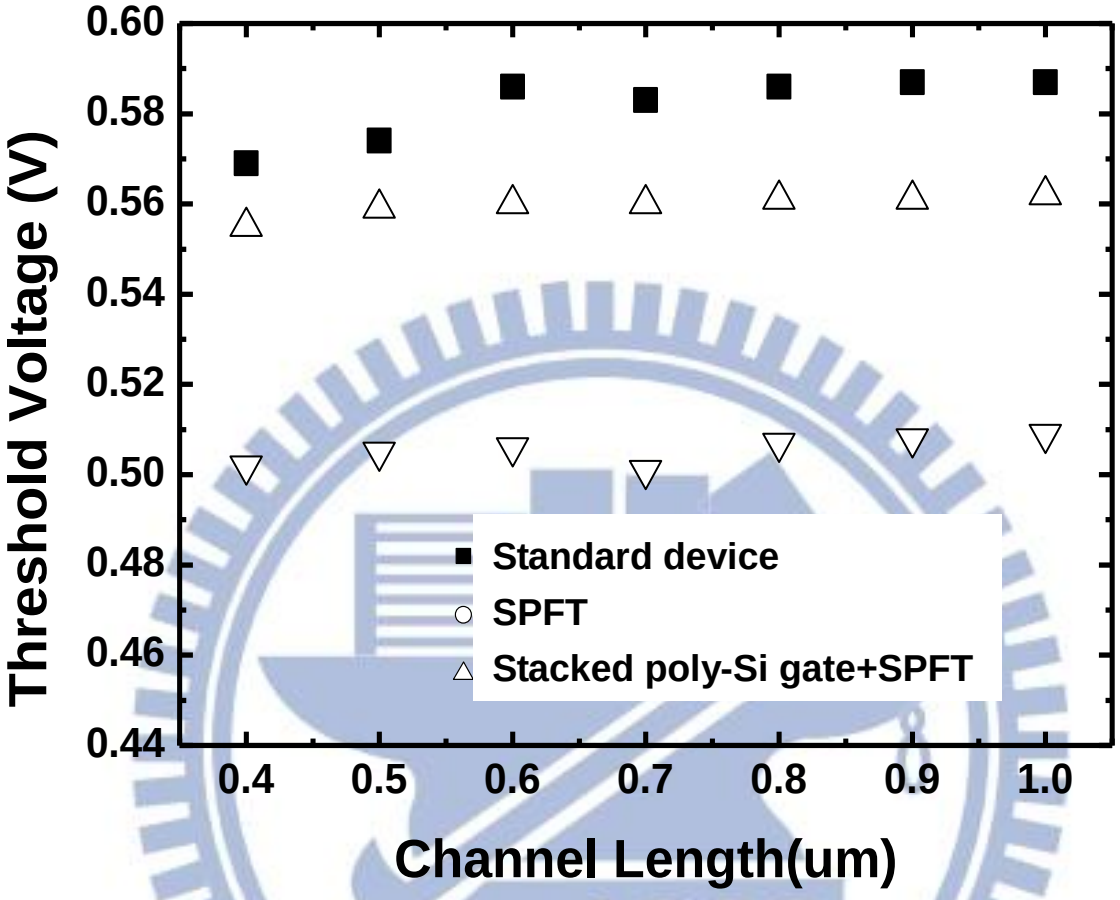


Fig. 3-3 Threshold voltage Vt_lin for stacked poly-Si gate+SPFT

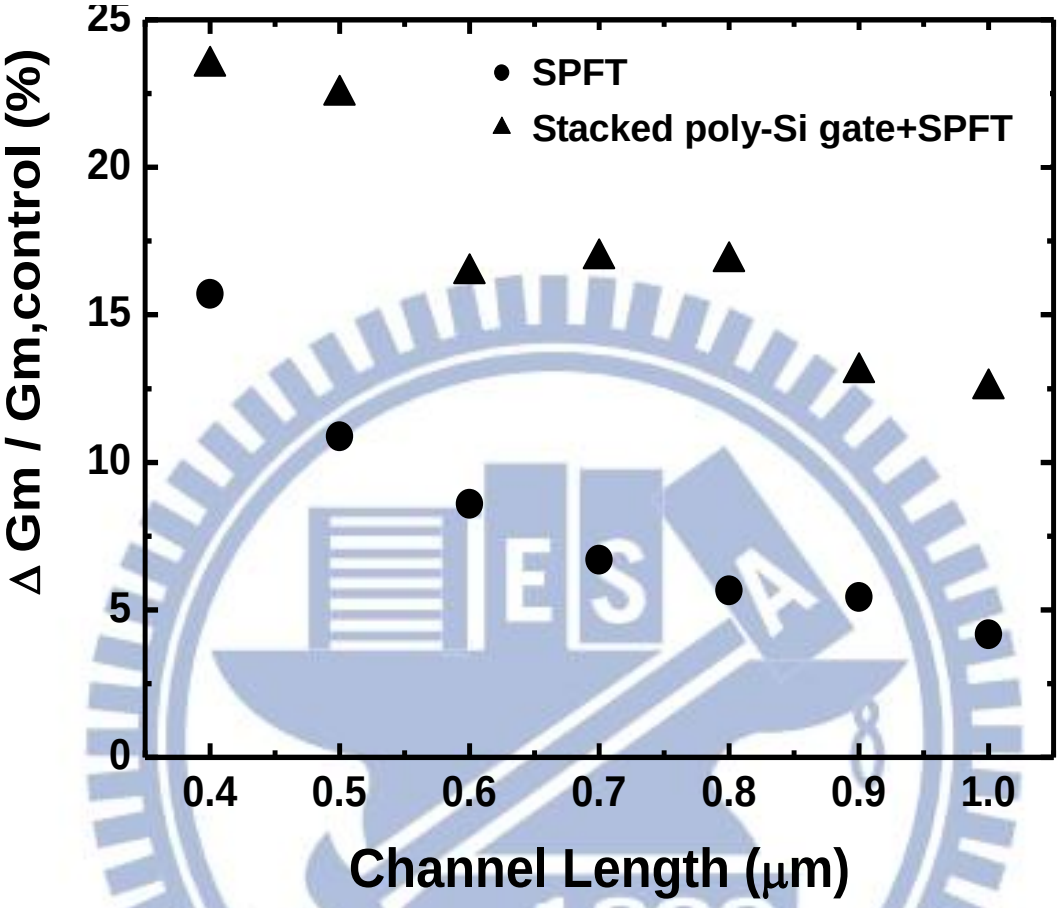


Fig. 3-4 Gm improvement of stacked poly-Si gate+SPFT

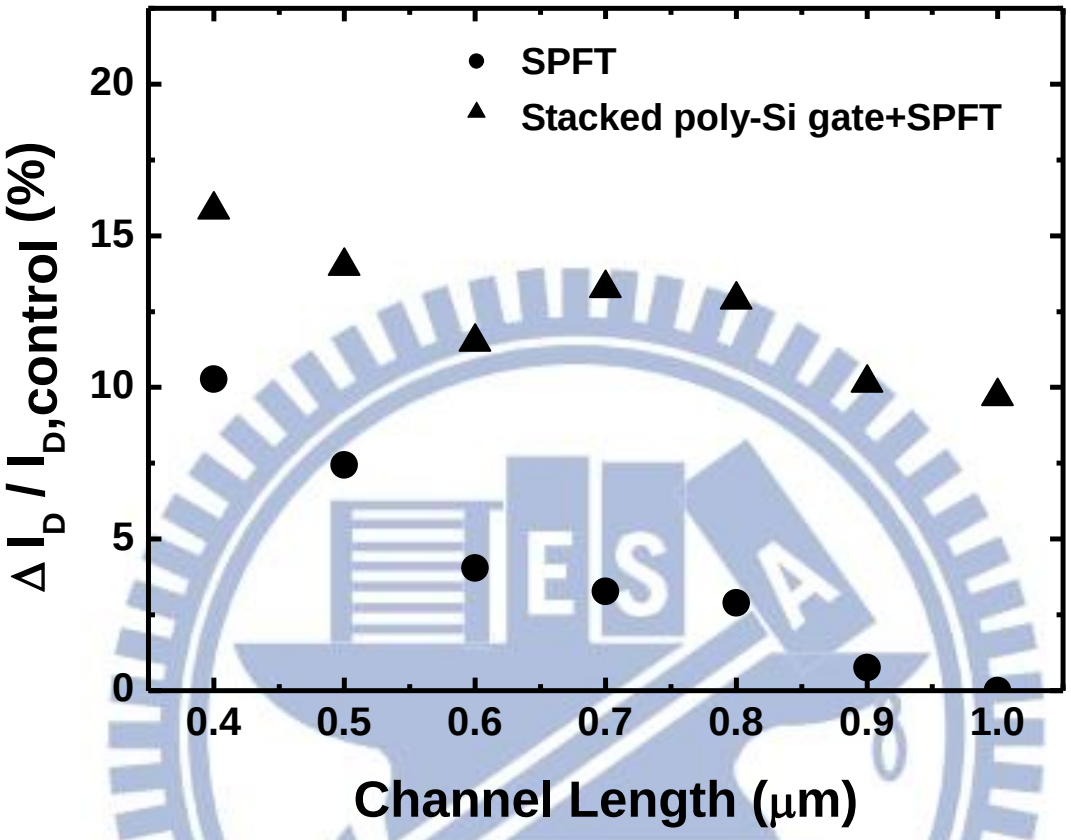


Fig. 3-5 Drain current Id improvement of stacked poly-Si gate+SPFT

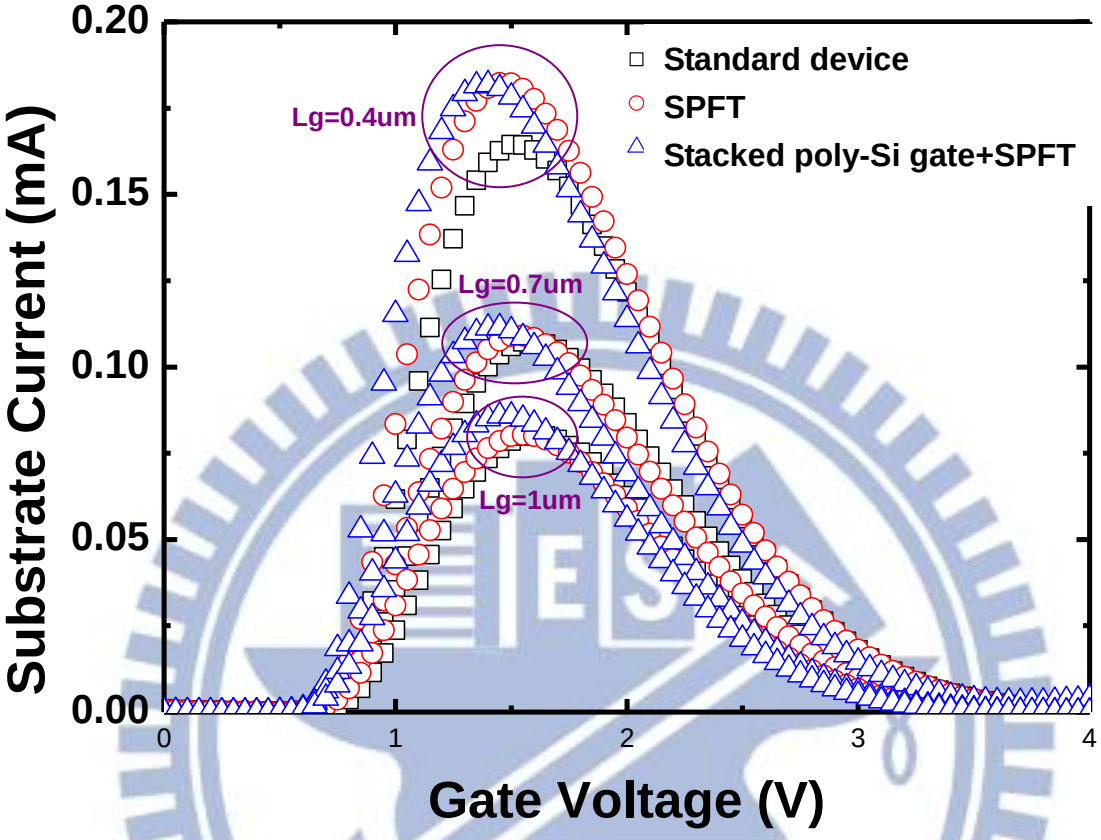
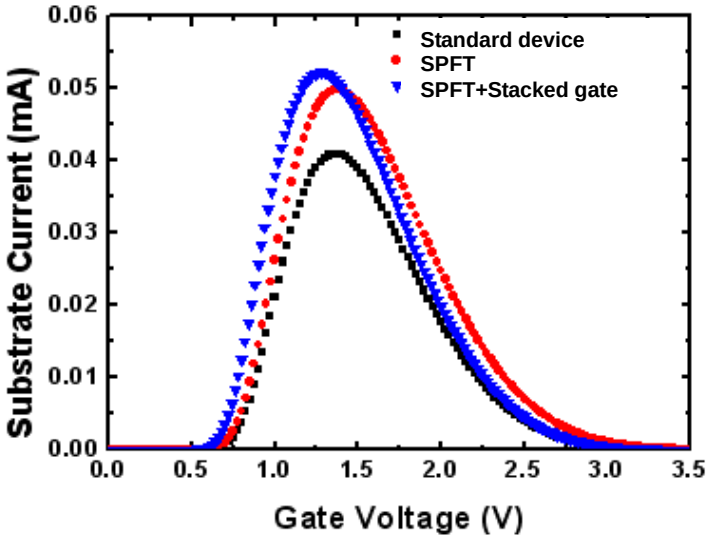
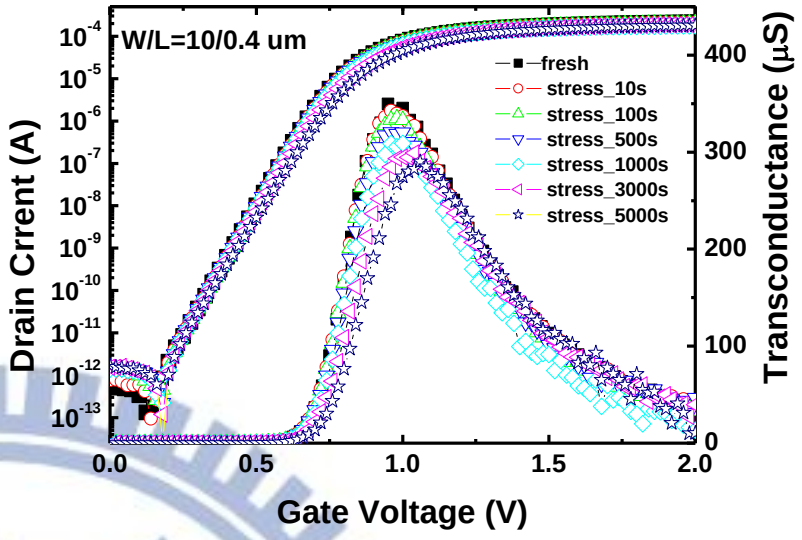


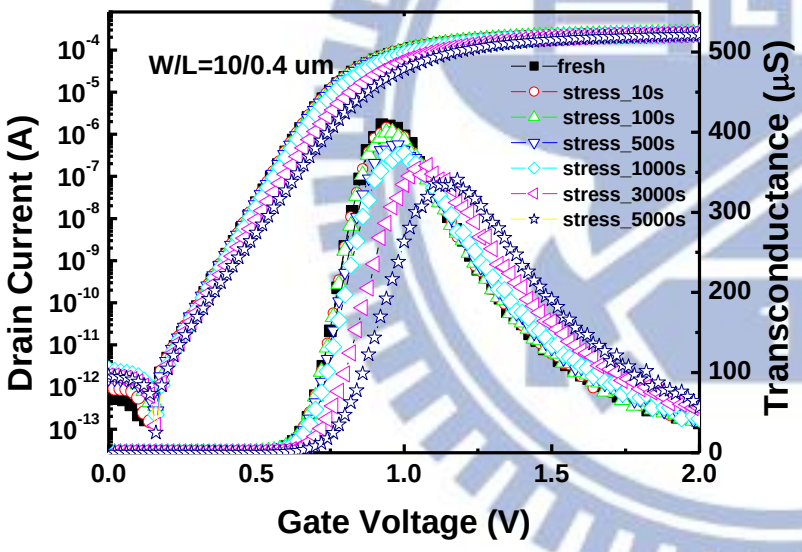
Fig. 3-6 Substrate current Isub for stacked poly-Si gate+SPFT



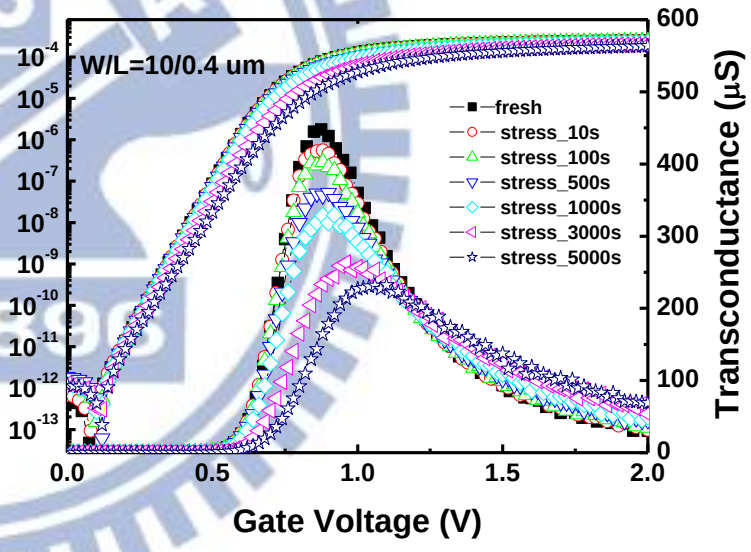
(a)



(b)



(c)



(d)

Fig. 3-7 Before and after hot carrier stress 5000 sec for the three splits at Vds=3.5v & Vg=Isub_max .(a) Substrate current Isub (b) Standard device (c) SPFT (d) Stacked poly-Si gate+SPFT

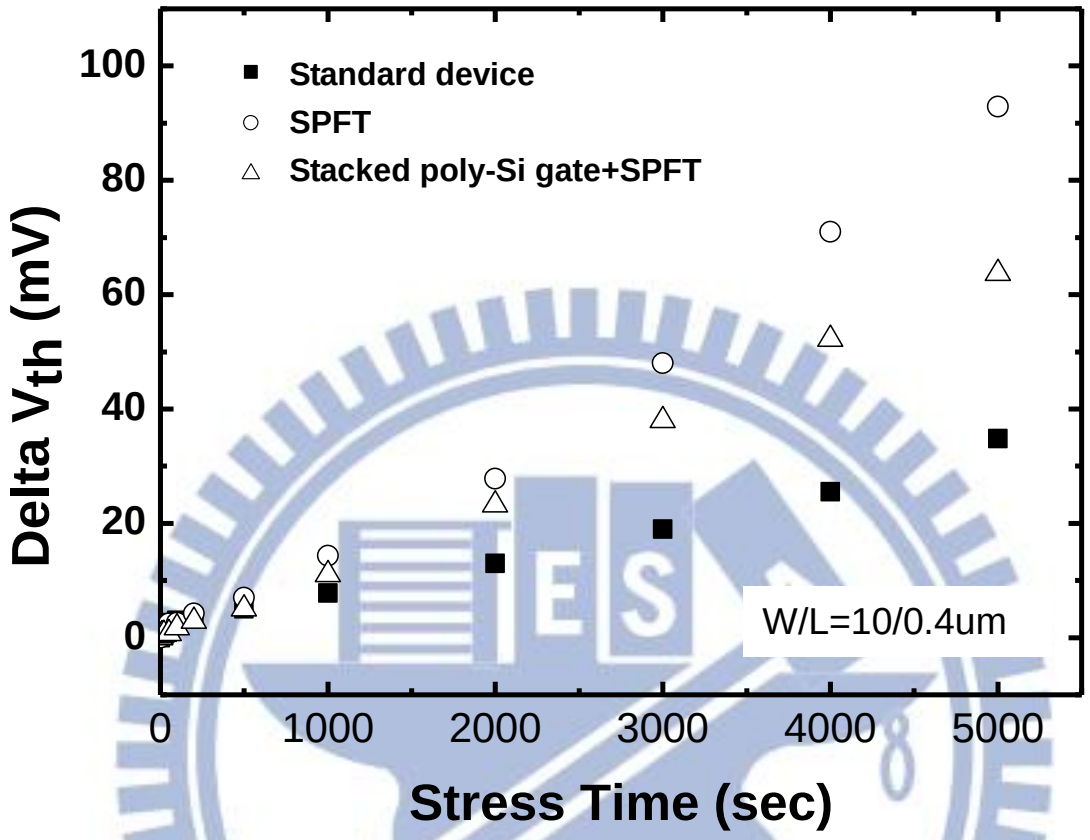


Fig. 3-8 Delta Vth after hot carrier stress for stacked poly-Si gate+SPFT on W/L=10/0.4um NMOS devices

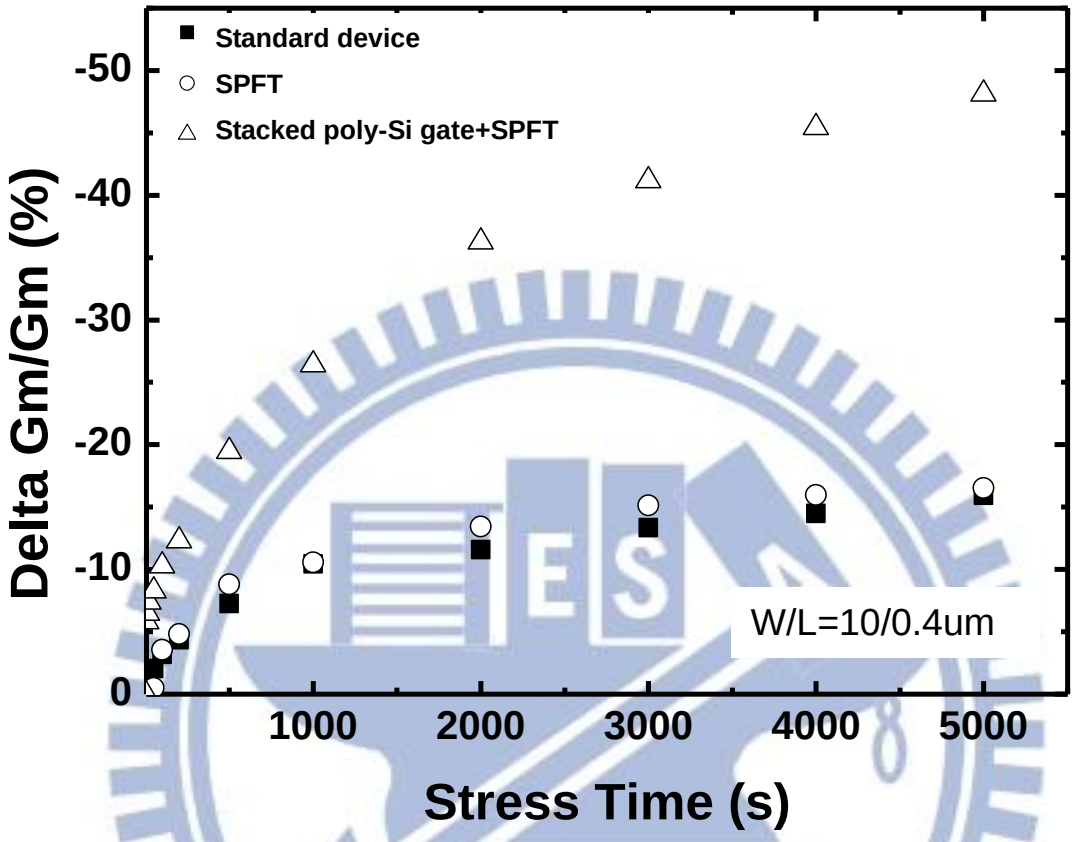


Fig. 3-9 Delta Gm after hot carrier stress for stacked poly-Si gate+SPFT on W/L=10/0.4um NMOS devices

Chapter 4. SPFT with Pre-Amorphous Layer (PAL) Gate Structure

4.1 Introduction

In pursue of high speed circuit applications, mobility enhancement by local stressor engineering in high performance CMOS transistors has been intensively studied, using techniques such as contact etch stop layer (CESL) and embedded SiGe (eSiGe) in the source/drain area. Recently, stress memorization technique (SMT) has been reported to enhance electron mobility on nMOSFETs and has been widely studied using a variety of approaches. However, most previous studies have demonstrated the performance boost without considering the scalability of the gate density. As the scaling of design rules such as poly pitch shrinks in high density SRAM circuits (as shown at the top of Fig. 4-1.), mobility enhancement will be limited by stressor volume and process integration issues. The introduction of longitudinal tensile stress and vertical compressive stress into the channel region are well known principles of mobility enhancement in nMOSFETs. However, longitudinal tensile stress will be limited as the stressor volume reaches its saturation point, causing performance degradation. Moreover, poor Ni-silicide formation and contact process integration issues will be induced by stressor residue in high density CMOS circuits.

In this work, we propose a strain proximity free technique (SPFT) to circumvent

the limitation of stressor volume for performance improvement in high density circuits. Two-step thermal annealing in SPFT is proposed to improve device performance. Moreover, a stacked gate structure has been reported to enhance channel stress and electron mobility by controlling bottom layer grain size and thickness of poly-Si deposition [24]. In this study, we have proposed a pre-amorphous layer (PAL) gate structure using implantation process to further improve performance on nMOSFETs.

Dynamic threshold voltage MOS (DTMOS), which lowers the threshold voltage of MOSFETs only in active operation, is proposed for high speed and low power applications [25-26]. DTMOS realizes a higher saturation current in active mode and a lower leakage current in standby mode. We have applied DTMOS and combined it with SPFT to demonstrate further performance improvement without increasing standby power consumption. Gate oxide and channel hot carrier reliability are also discussed for characterizing performance improvement and device reliability on the strain engineering.

4.2 Experiments

nMOSFETs were fabricated on 6-in wafers using a conventional MOSFET process flow including local oxidation of device isolation, gate oxide, S/D extension

implantation, sidewall spacer formation, deep S/D implantation, contact patterning and metallization processing, as listed in Fig. 4-1. All the nMOSFETs characterized in this work had 2.5 nm thick gate oxide and a 150 nm thick poly-Si layer as the gate electrode, grown in a vertical furnace. Pre-amorphous layer (PAL) gate structure was proposed by arsenic atom implantation. Two arsenic dosages were split in this work for achieving different thicknesses of the amorphous layer in the gate electrode. The arsenic energy and dosage split in the experiment were 40KeV $1x10^{15}cm^{-2}$ and 40KeV $5x10^{15}cm^{-2}$, respectively. Pre-amorphous layer is located between the gate oxide and the poly-Si layer. The SPFT process flow is inserted between poly-Si layer deposition and gate patterning. Before patterning on the poly-Si gate, the SPFT is introduced by high tensile stressor deposition, rapid thermal annealing (RTA), and stressor removal processes. The stressor of SPFT in this experiment is a high tensile Si_3N_4 film of 100nm thickness by low pressure chemical vapor deposition (LPCVD). The stress level of this film is near 1.3GPa. RTA was processed by spike annealing in 1050℃ ambient. RTA 1100℃ and two-step RTA in SPFT are proposed to enhance electron mobility, which inserted an extra RTA after the buffer oxide deposition, can bring greater stress into the channel. Two-step dry and wet etching was used in the stressor removal process. To protect the poly-Si from plasma damage under dry etch, 90% of the stressor thickness was removed by plasma etching and the remainder was stripped

by thermal H_3PO_4 acid. Photo patterning and plasma etching to define the gate electrode were then carried out. After gate patterning, source/drain extension (SDE) formation by arsenic implantation, sidewall spacer formation, and deep S/D implantation were processed. After S/D dopant activation by spike RTA, a 100nm LPCVD tensile Si_3N_4 CESL was deposited on all transistors. After inter layer dielectric film deposition and contact patterning, a four-level metallization (Ti-TiN-Al-TiN) was carried out in PVD system.

The device characteristics were measured by a semiconductor parameter analyzer, a Keithly-4200. The electron mobility is determined by field effective mobility extraction as $\mu_{EF} = \frac{G_m \times L}{W \times C_{ox} \times V_d}$, where G_m is the transconductance, C_{ox} is the gate-oxide capacitance, V_d is the drain voltage, and *W/L* are channel width and length, respectively. The threshold voltage was determined by the constant drain current method when the drain current was set to 40nA/um. The linear and saturation mode threshold voltages, Vt_lin and Vt_sat, were extracted at drain voltages of 0.1V and 1.5V, respectively.

4.2 Results and Discussions

The gate oxide reliability is confirmed by testing breakdown voltage (V_{BD}). The SPFT shows a V_{BD} (=5V) performance comparable to standard devices. The

performance improvement for the nMOSFET is illustrated in Fig. 4-2. The standard device here is an unstrained device without SPFT and PAL gate structure. SPFT without PAL gate structure shows a 14% mobility improvement on device channel width/length = 10/0.35 μm. The corresponding I_d-V_d characteristic of SPFT is also shown in Fig. 4-3. The SPFT shows a 8% I_d improvement, compared to that of the standard device.

Since the SPFT is applied to introduce stress into the channel region before gate patterning, it can prevent the problems of stressor volume and small gate pitch in high density circuits. A simple model is proposed to explain the mechanism of SPFT. It was reported that the vertical compressive stress is the major component of stress in SMT processes. In the SPFT approach, the RTA has transferred the high tensile stress from the disposable stressor to the gate poly-Si, resulting in the induction of a plastic strain in the poly-Si. To compensate for this external stress from the disposable stressor, a very high vertical compressive strain is induced in the poly-Si. The deformation of the poly-Si is expanded in the longitudinal direction and compressed in the vertical direction. This further creates longitudinal tensile stress and vertical compressive stress in the Si channel. After stressor removal, the high longitudinal tensile stress and vertical compressive stress will be memorized in the channel region. This mechanism appears to explain the increased stress resulting from use of SPFT to

enhance electron mobility. Moreover, previous studies have shown that the poly-Si got a smaller grain size after processing with SMT. Our SEM pictures show that the mean grain size of the typical poly-Si is 77~106nm, while the mean grain size for SPFT poly-Si is 64~86nm, as shown in Fig. 4-5. Grain size changed during SPFT may affects the interface between poly-Si and gate oxide, which modulates the energy barrier height in poly-Si.

A significant improvement of mobility on SPFT with a pre-amorphous layer (PAL) gate structure is found, as shown in Fig. 4-2. It appears that SPFT with PAL gate structure can further increase mobility to 24% for PAL1 and 31% for PAL2 dosing with 40KeV, $1x10^{15}$ cm^{-2} and $5x10^{15}$ cm^{-2} of arsenic implantation, respectively. Moreover, I_d increases of 21% and 28% (as shown in Fig. 4-3.) may be achieved when using both SPFT and PAL gate structure. The corresponding Ion-Ioff characteristics of SPFT with PAL1 and PAL2 are shown in Fig. 4-4. The SPFT with PAL1 shows a 35% Ion-Ioff improvement and SPFT with PAL2 shows ~120% improvement at Ioff = 4pA, compared to that of the standard SPFT device. The mechanism of the stress enhancement in the PAL gate structure may be as follows: the re-crystallization of the amorphous region during the SPFT process leads to shrinkage of the total thickness of the gate and results in a residual compressive strain. The PAL gate structure with optimization of the arsenic implantation of the pre-amorphous

layer, provides more vertical compressive stress and longitudinal tensile stress to the channel region. For recently High-K/Metal Gates structure, a thin metal layer below the poly-Si is plays a role of work function adjustment. Since the metal layer we usually use is thinner than 10nm, we believe the SPFT combine PAL gate structure can be efficient for improving electron mobility in the advanced technology [27-29]. Two-step RTA in combination with SPFT and PAL2 gate structure shows further mobility improvement. As shown in Fig. 4-6, gate length dependence of mobility improvement in SPFT+PAL2 with two-step RTA shows ~10% mobility improvement than SPFT+PAL2 with single RTA. This may attributes to an extra RTA that provides more gate deformation and higher stress into the channel region. Another sign to show that the mobility improvement by SPFT and combines it with PAL gate structure and two-step RTA. As shown in Fig. 4-7, the lower slope of R_{total} in SPFT, SPFT+PAL2 and SPFT+PAL2+Two-step RTA proves electron mobility improvement and without increasing source/drain resistance, R_{SD}(R_{total}=R_{SD}+$R_{channel}$). In short channel devices, mobility is affected by parasitic resistance in source/drain severely. However, in our experiment, 0.35um-long nMOSFETs are relative long gate length. Thus the mobility extraction is relatively accurate in our devices. As shown in Fig. 4-8, SPFT+PAL2+Two-step RTA shows ~100mV Vth lower than single RTA. Gate leakage current under SPFT combined with PAL gate structure is slightly higher than

in a conventional gate structure device, which is near 30 pA/um, as shown in Fig. 4-9. The higher gate leakage current in PAL2 gate structure may comes from the thicker pre-amorphous layer and induces interface roughness between gate oxide and Si substrate during SPFT.

Dynamic threshold voltage MOS (DTMOS) is applied for a further performance boost to the SPFT. This was proposed by connecting the poly-Si gate to the Si body (well region). We present the gate length dependence of the threshold voltage for a standard device and the DTMOS device in Fig. 4-10. The saturation threshold voltage Vth for DTMOS SPFT was nearly 100mV lower than the standard SPFT device. A better explanation for the reduction of threshold voltage is a forward Si body to the source junction bias. Further, an insignificant Vth difference is found when using SPFT to improve electron mobility. As shown in Fig. 4-11, electron mobility is improved by 32% and 46% using DTMOS standard device and DTMOS SPFT, compared to the simple standard device. Moreover, near 60% mobility enhancement can be achieved by combining a PAL2 gate structure with DTMOS SPFT, respectively. Furthermore, two-step RTA in DTMOS SPFT and combine it with PAL2 gate structure shows an extra 7% mobility improvement than single RTA, as shown in Fig. 4-12. The corresponding I_d-V_g characteristic of DTMOS SPFT is illustrated in Fig. 4-13. The drain current at $I_{on,\,(Vg=0.7V,\,Vd=0.1V)}$, $I_{off,\,(Vg=0V,\,Vd=0.1V)}$ state and I_{on}/I_{off} ratio are

also illustrated in the inset of this figure. It is shown that the I_{off} current of DTMOS SPFT and combines PAL gate structure with DTMOS SPFT is comparable to the simple standard device. Higher I_{on}/I_{off} ratio can be achieved by combining PAL gate structure with DTMOS SPFT. It enables realization of lower threshold voltage operation and higher electron mobility for high speed circuit application.

The interface state density is checked by measuring charge pumping current. As shown in Fig. 4-14, SPFT with PAL1 gate structure shows comparable interface state density with standard SPFT. However, combining SPFT with PAL2 shows higher interface state density than standard SPFT. It is suspected by higher dosage of pre-amorphous implantation in PAL2 gate structure which may degrades the gate dielectric to Si interface quality. The dependence of the channel-hot-carrier reliability is shown in Fig. 4-15. We found that the shift in the threshold voltage ($\triangle V_{th}$) and electron mobility degradation are slightly higher in SPFT as a function of the stress time. This result is suspected by the improved drain current under the same bias conditions and induced higher substrate current. Since mobility enhancement is related to the stress induced energy band gap narrowing, it will accompany modification of the impact ionization rate and channel hot carriers in the Si substrate. SPFT with PAL gate structure introduces more stress into the channel region. As shown in Fig. 4-16, the $\triangle V_{th}$ and mobility degradation are slightly higher than for the

single SPFT device. Moreover, as shown in Fig. 4-17, the shift of gate oxide interface state density is higher in SPFT with PAL1 and PAL2. The higher pre-amorphous implantation dosage will induce the higher shift of interface state density. The quality of gate oxide to Si interface will affect the channel-hot-carrier reliability. This study explored both performance improvement and device reliability on the SPFT device, finding that the higher strain provided higher electron mobility, but degraded the device reliability.

The electron mobility improvement of nMOSFET, with optimization of thermal RTA process on SPFT with PAL2 is illustrated in Fig. 4-18. The electron mobility is improved by 6% on higher RTA temperature 1100℃. Moreover, two-step RTA process in SPFT is demonstrated a 12% electron mobility improvement than single step RTA process. We have inserted an extra 1050℃ RTA between buffer oxide and stressor SiN capping layer deposition. The corresponding Ion-Ioff characteristics of RTA 1100℃ and two-step RTA are shown in Fig. 4-19. The higher RTA temperature 1100℃ shows a 49% Ion-Ioff improvement and two-step RTA shows ~70% improvement at Ioff = 4pA, compared to that of the standard SPFT+PAL2 device. The mechanisms of the stress enhancement on higher RTA temperature and two-step RTA process may be as follows: The higher RTA temperature during SPFT process leads to enhance the longitudinal tensile stress on SiN capping layer. It will enhance the

deformation of the poly-Si to expand in the longitudinal direction and compressed in the vertical direction. This further creates the longitudinal tensile stress and vertical compressive stress in the Si channel. Besides, two-step RTA in SPFT process is demonstrated the higher electron mobility. This approach is similar to apply an extra SMT in SPFT process. Since the extra RTA is inserted after buffer oxide deposition. It will provide more tensile stress into the channel region. The gate leakage current of SPFT+PAL2 with different RTA process is shown in Fig. 4-20. The higher RTA temperature revealed the lower gate leakage current. It's suspected by improving the gate oxide quality and proved on lower interface state density (as shown in Fig. 4-21). The higher RTA temperature leads to reduce hydrogen (H) in oxide/Si interface and improves interface state density. The channel-hot-carrier reliability for different RTA process in SPFT+PAL2 is shown in Fig. 4-22 and Fig. 4-23. The shift of threshold voltage ($\triangle$Vth) and transconductance ($\triangle$Gm) is improved by higher RTA temperature and two-step RTA process in SPFT+PAL2. It's suspected by lower gate oxide interface state density in high temperature RTA process. Moreover, the better channel-hot-carrier reliability is demonstrated by more gradient source/drain junction profile and lower electric field by using higher RTA temperature and two-step RTA process.

4.3 Summary

We have proposed a multiple strain-gate engineering that uses SPFT and PAL gate structure. The electron mobility and current drivability may be improved by controlling the SPFT process and the thickness of the PAL gate structure. Moreover, SPFT in combination with DTMOS can achieve a lower threshold voltage operation and a higher performance boost. Channel-hot-carrier reliability is slightly degraded as the channel stress is increased. Without the limitation of stressor volume in high density CMOS circuits, we believe this scheme that combines SPFT with PAL gate structure and DTMOS will serve as an important guide for continued improvement in future CMOS technology.

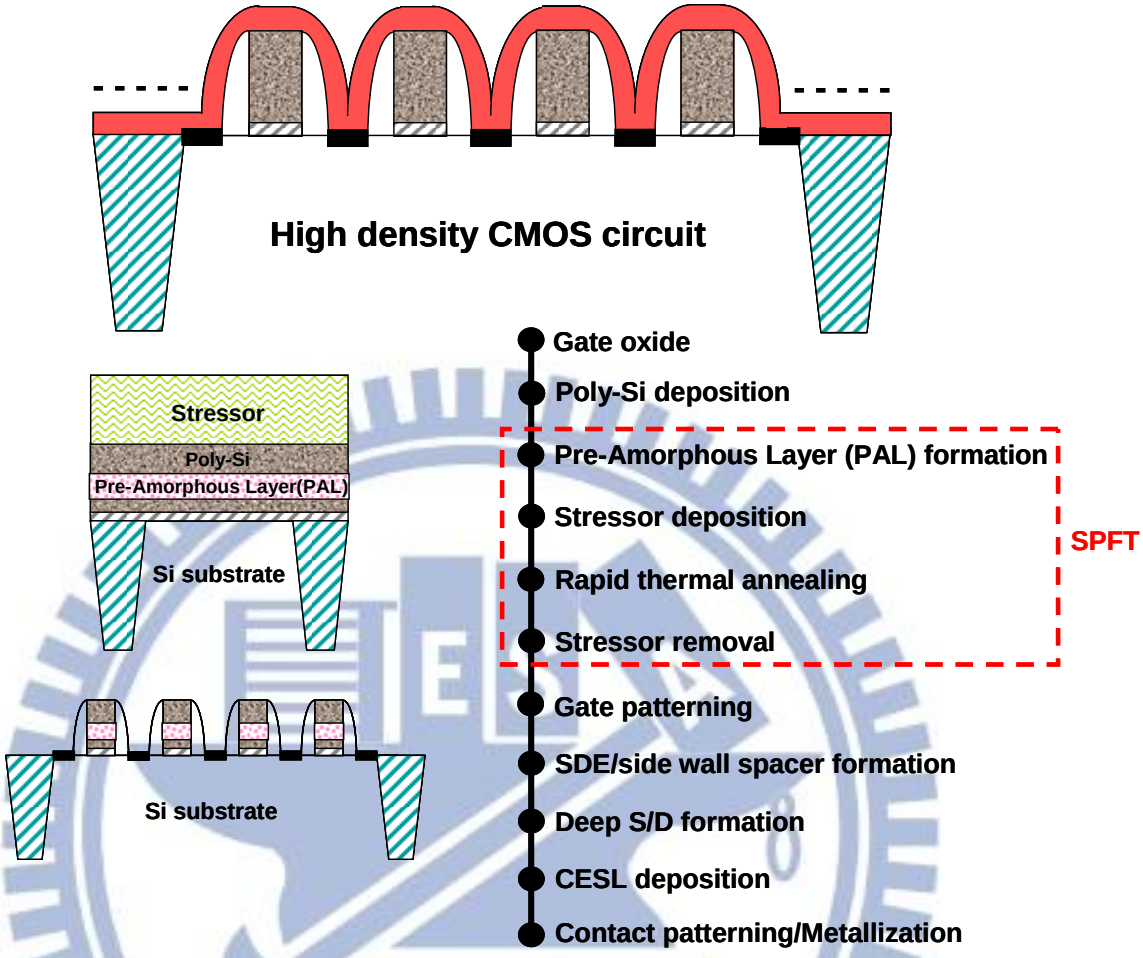


Fig. 4-1 High density CMOS circuit structure, process flow for the Strain Proximity Free Technique (SPFT)

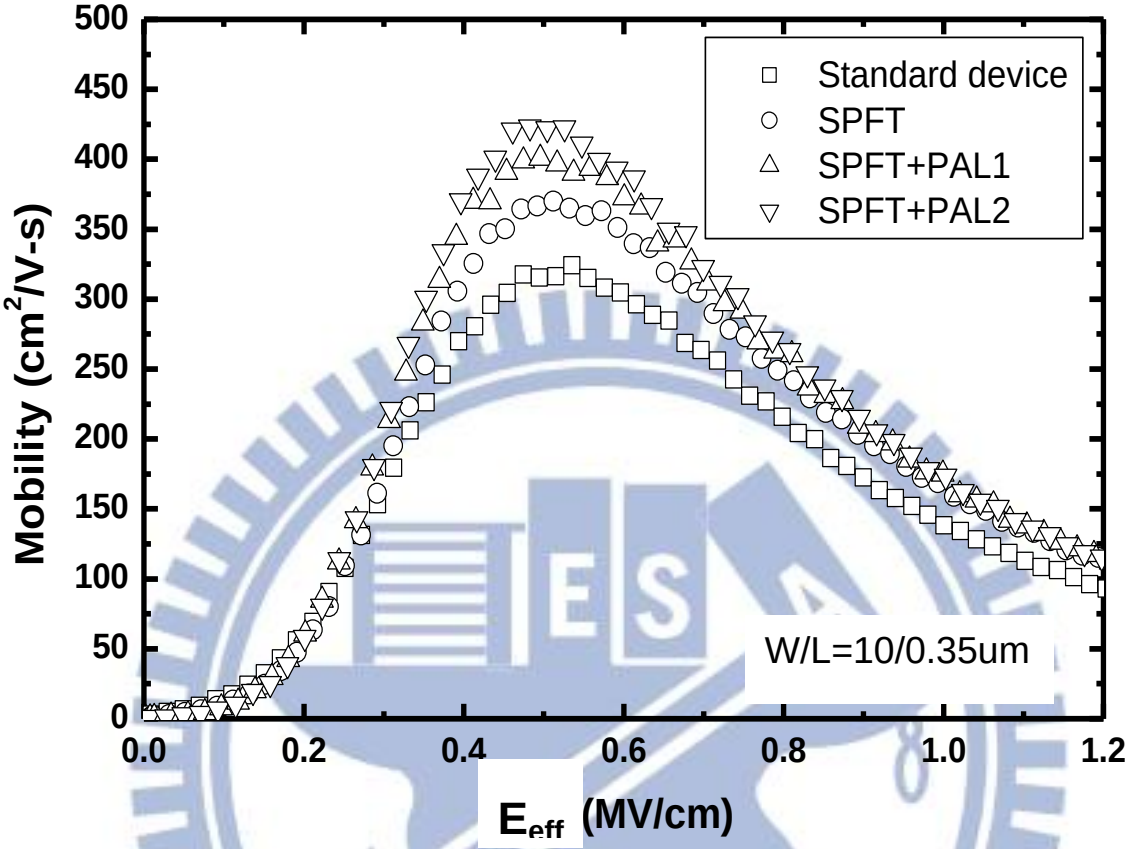


Fig. 4-2 nMOSFET electron mobility for SPFT and combing SPFT with PAL gate structure on channel width/length = 10 um/0.35 um

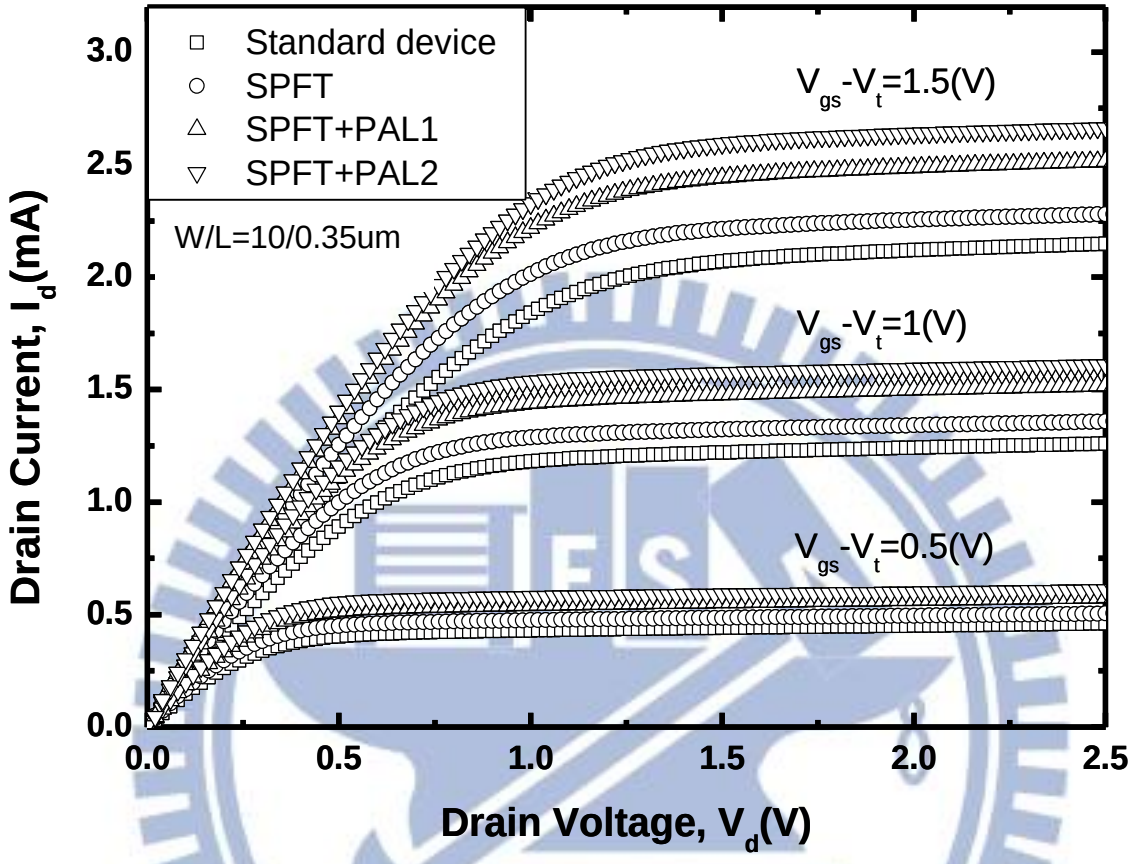


Fig. 4-3 The corresponding I_d-V_d characteristic of nMOSFET for SPFT and combing SPFT with PAL gate structure on channel width / length = 10 um/0.35 um

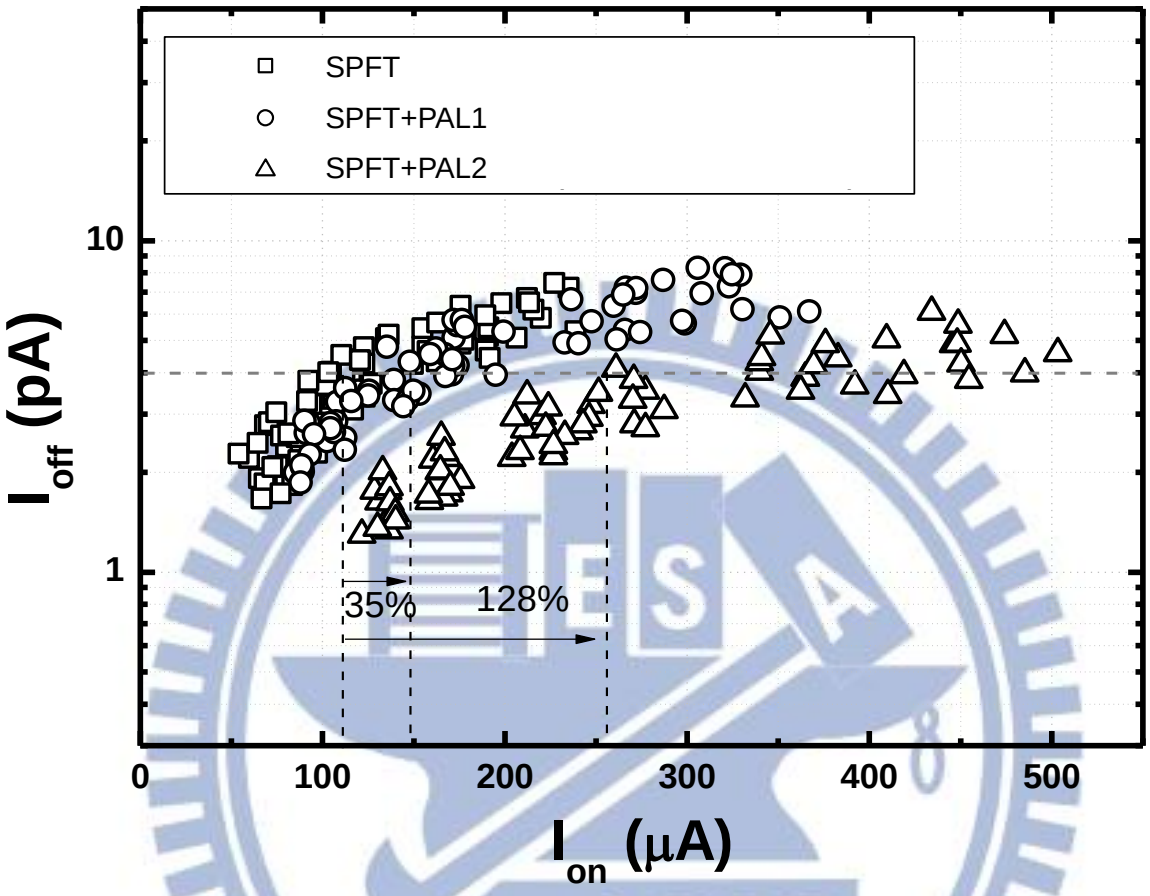


Fig. 4-4 The corresponding I_{on}-I_{off} characteristic of nMOSFET for SPFT and combing SPFT with PAL gate structure

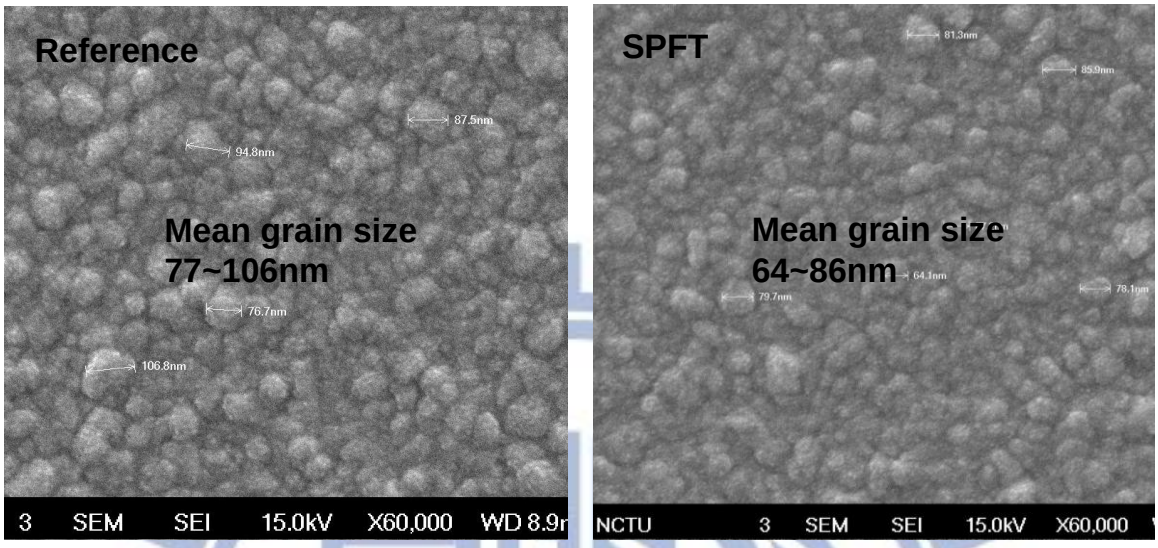


Fig. 4-5 SEM pictures with mean grain size of poly-Si for SPFT

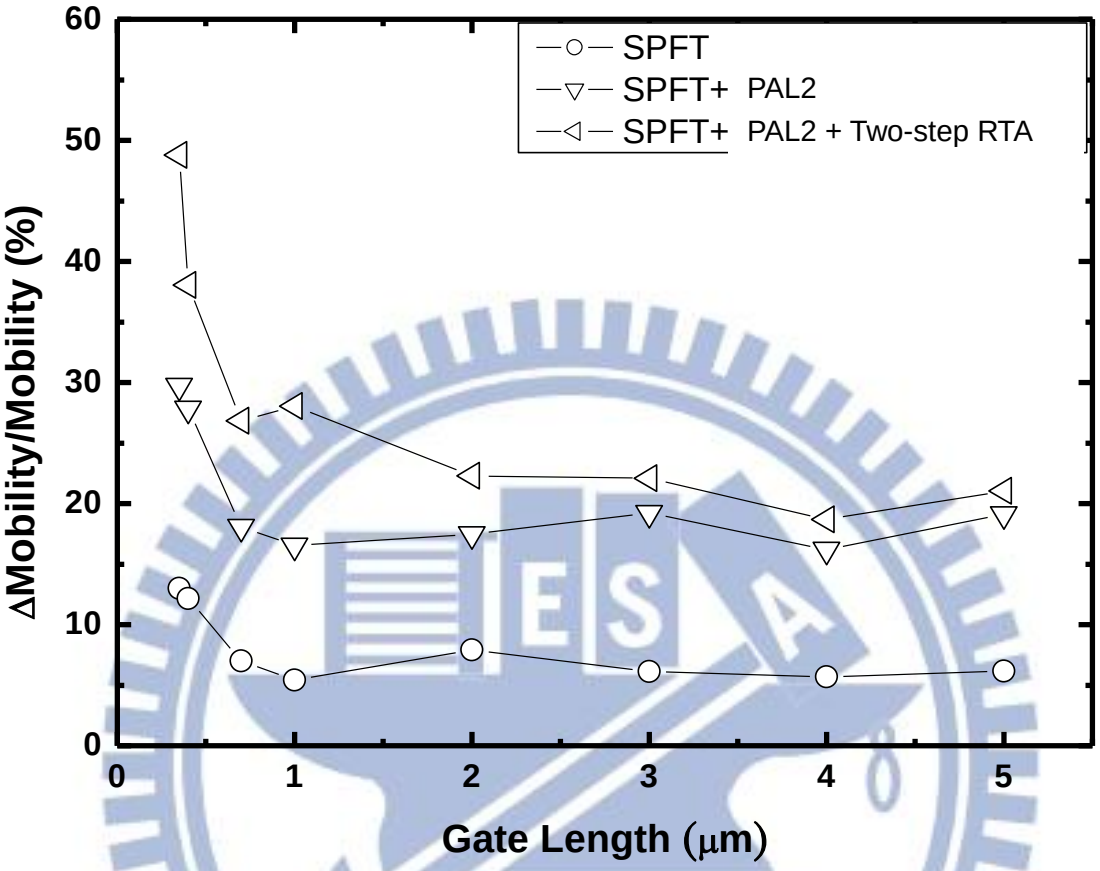


Fig. 4-6 Gate length dependence of mobility improvement in SPFT combines PAL gate structure and two-step RTA

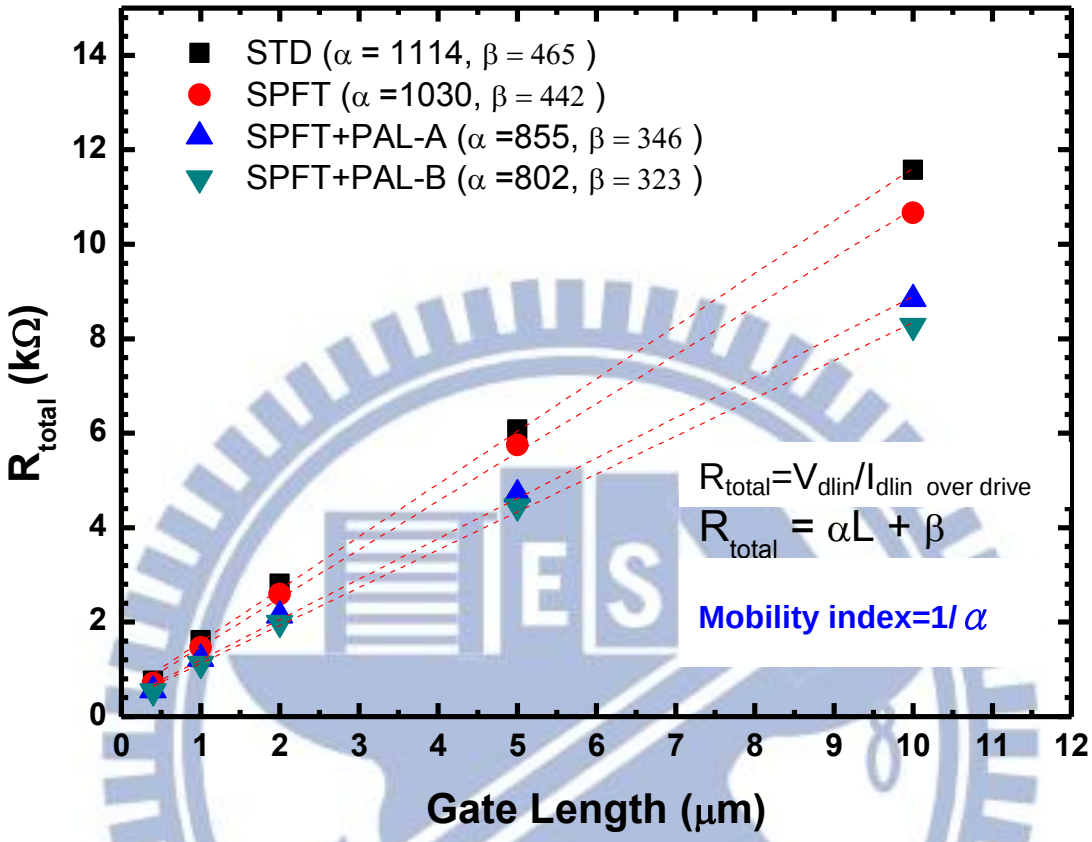


Fig. 4-7 Gate length dependence of Source/Drain resistance R_{total} for SPFT with PAL gate structure and two-step RTA

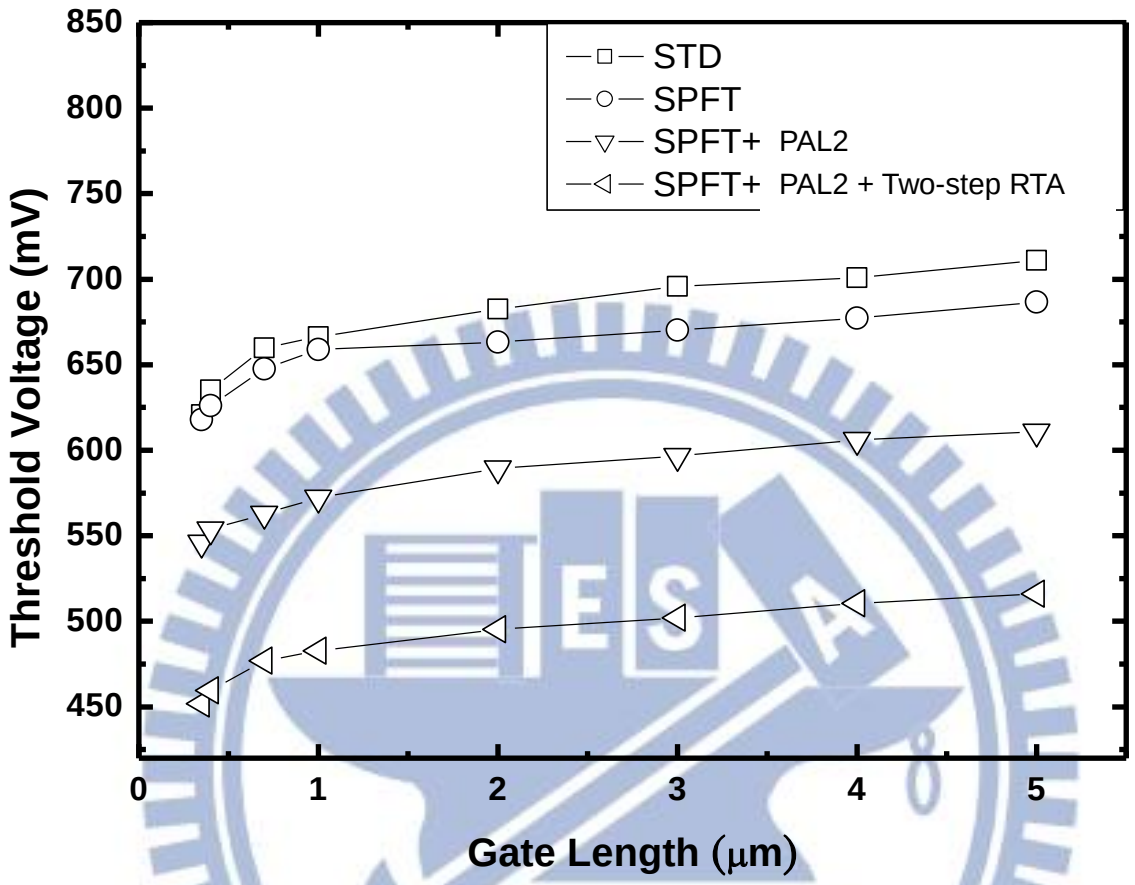


Fig. 4-8 Threshold voltage (Vth) for SPFT with PAL gate structure and two-step RTA

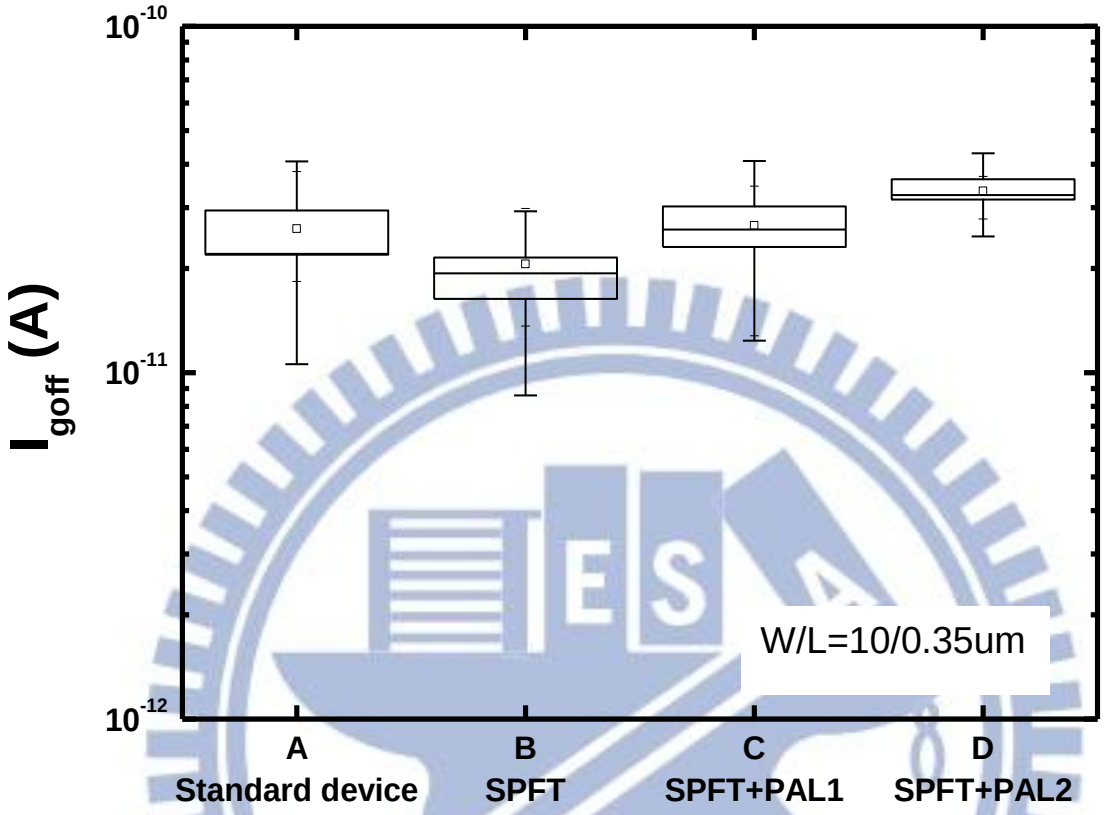


Fig. 4-9 Gate leakage current of nMOSFET for SPFT and combing SPFT with PAL gate structure on channel width/length = 10 um/0.35 um

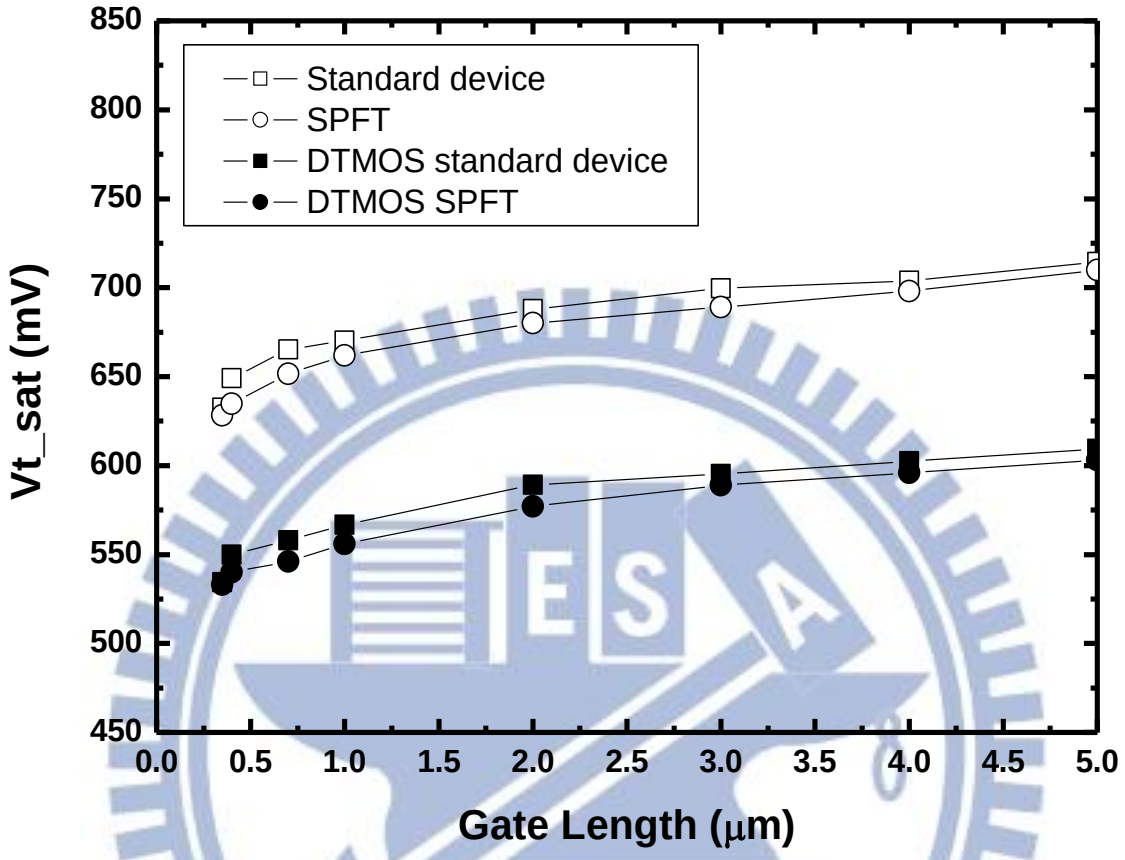


Fig. 4-10 nMOSFET saturation threshold voltage Vt_sat for SPFT and DTMOS SPFT

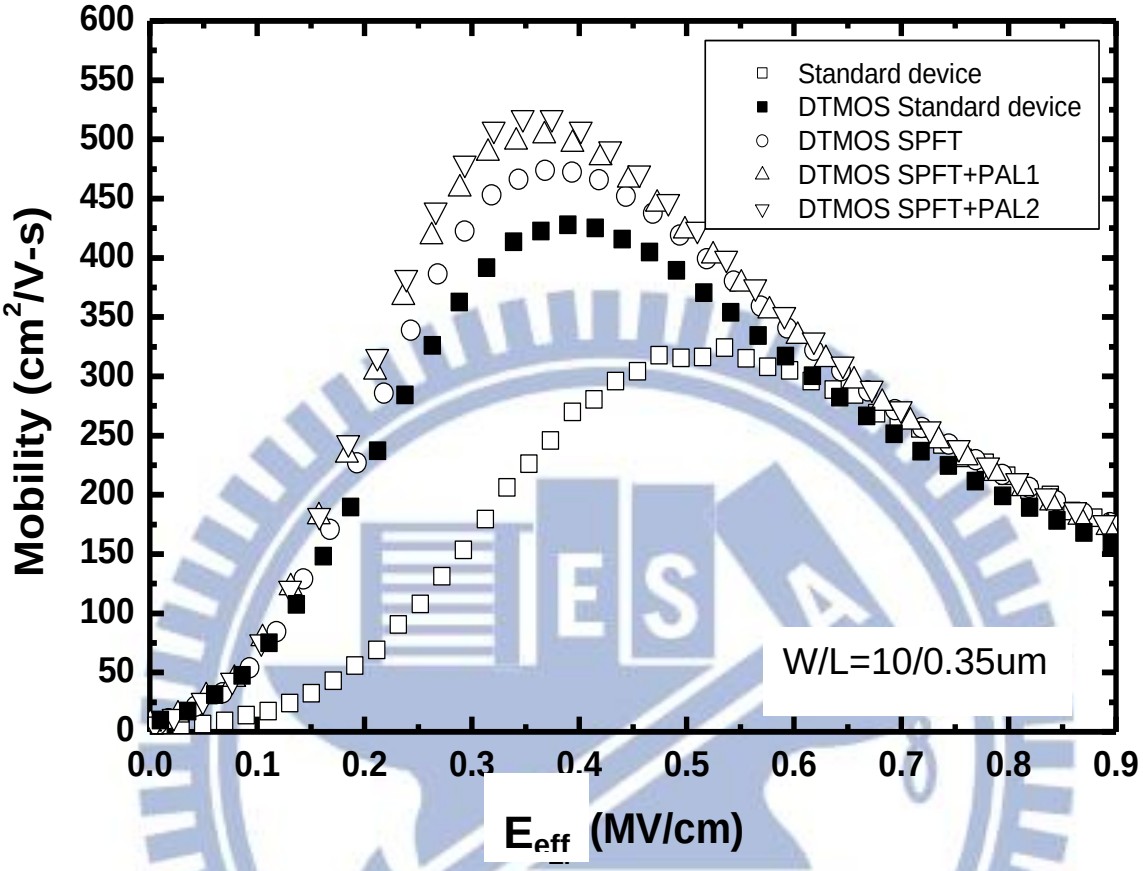


Fig. 4-11 nMOSFET electron mobility for DTMOS SPFT and combining SPFT with PAL gate structure on channel width/length = 10 um/0.35 um

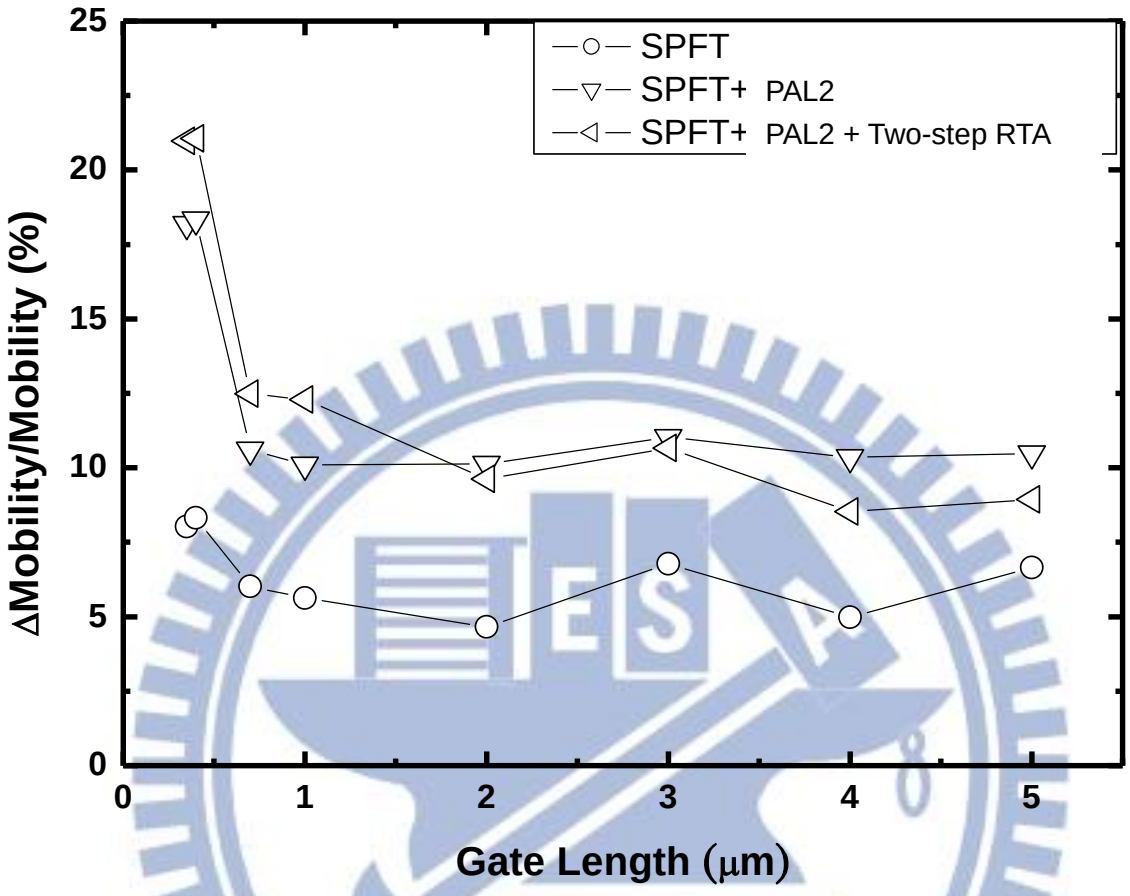


Fig. 4-12 Gate length dependence of mobility improvement in DTMOS SPFT with PAL gate structure and two-step RTA

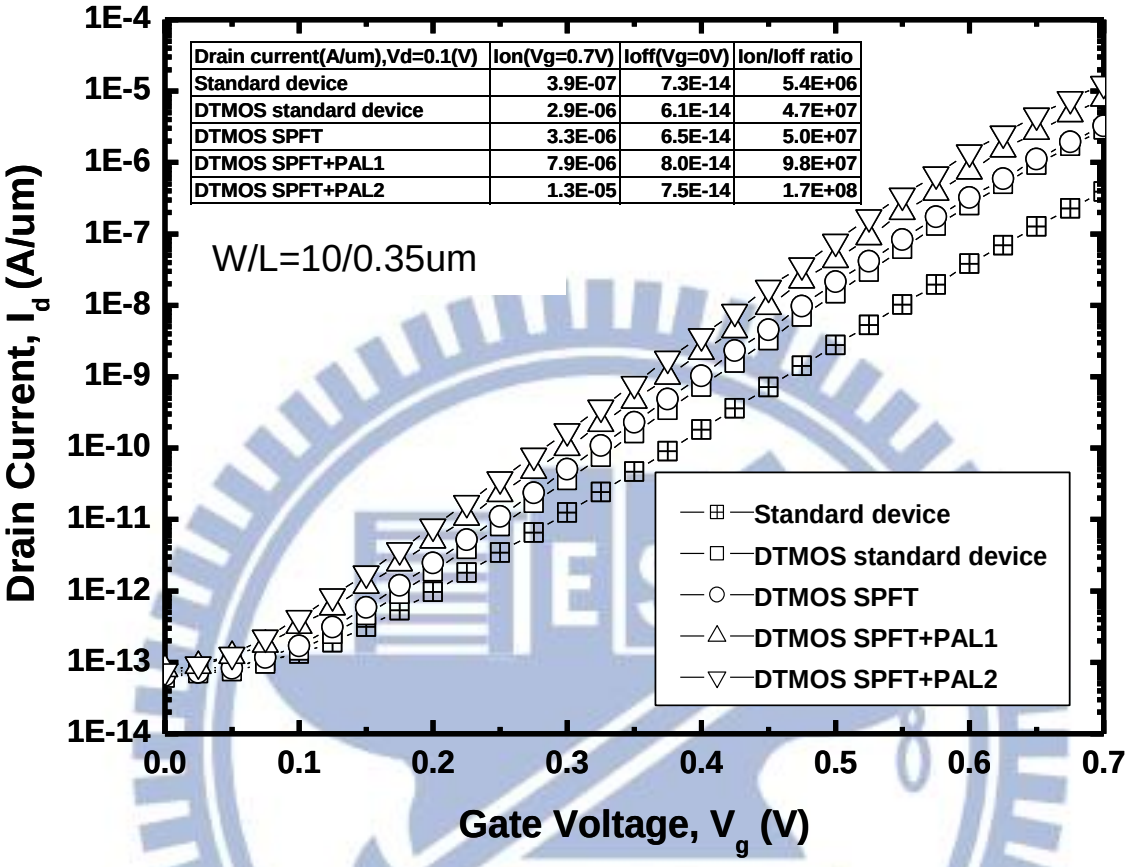


Fig. 4-13 The corresponding I_d-V_g characteristic of DTMOS SPFT and combining PAL gate structure with DTMOS SPFT on channel width / length = 10 um/0.35 um. The drain current at $I_{on, (Vg=0.7V, Vd=0.1V)}$, $I_{off, (Vg=0V, Vd=0.1V)}$ state and I_{on}/I_{off} ratio are also illustrated in the inset of this figure.

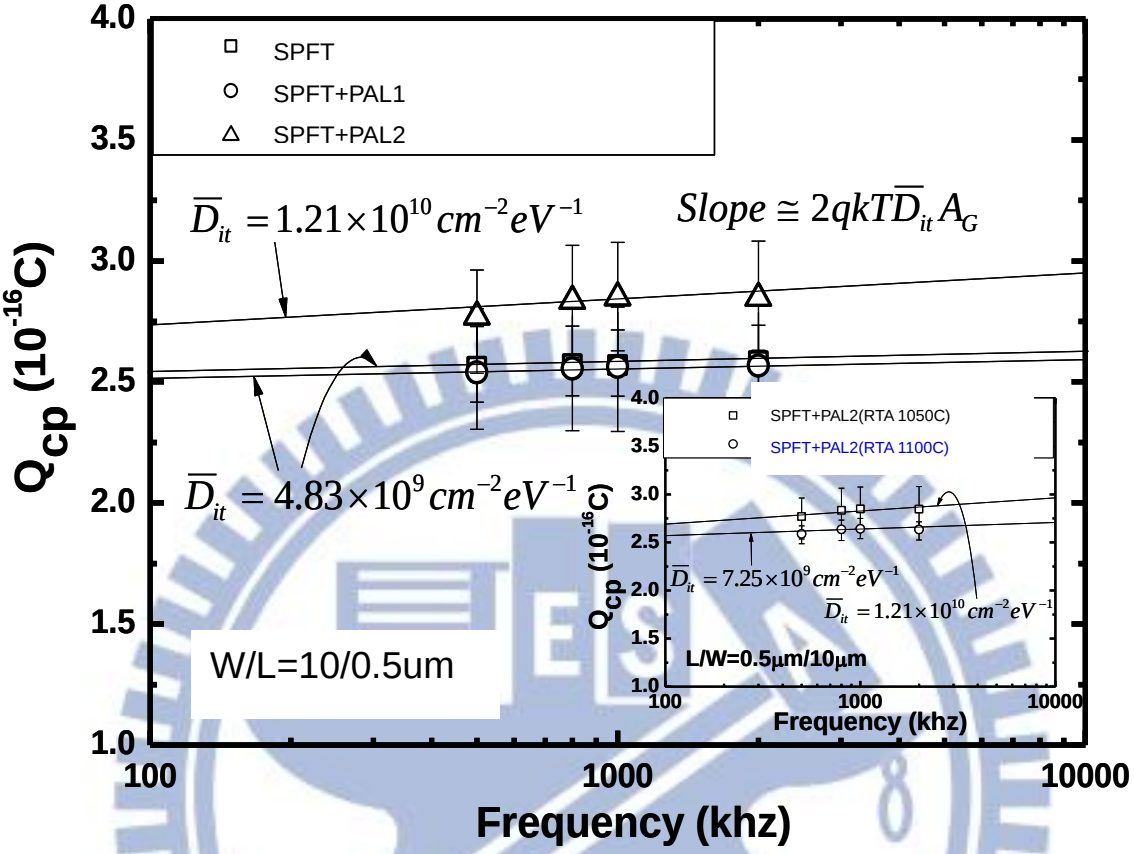


Fig. 4-14 Interface state density of SPFT with PAL gate structure

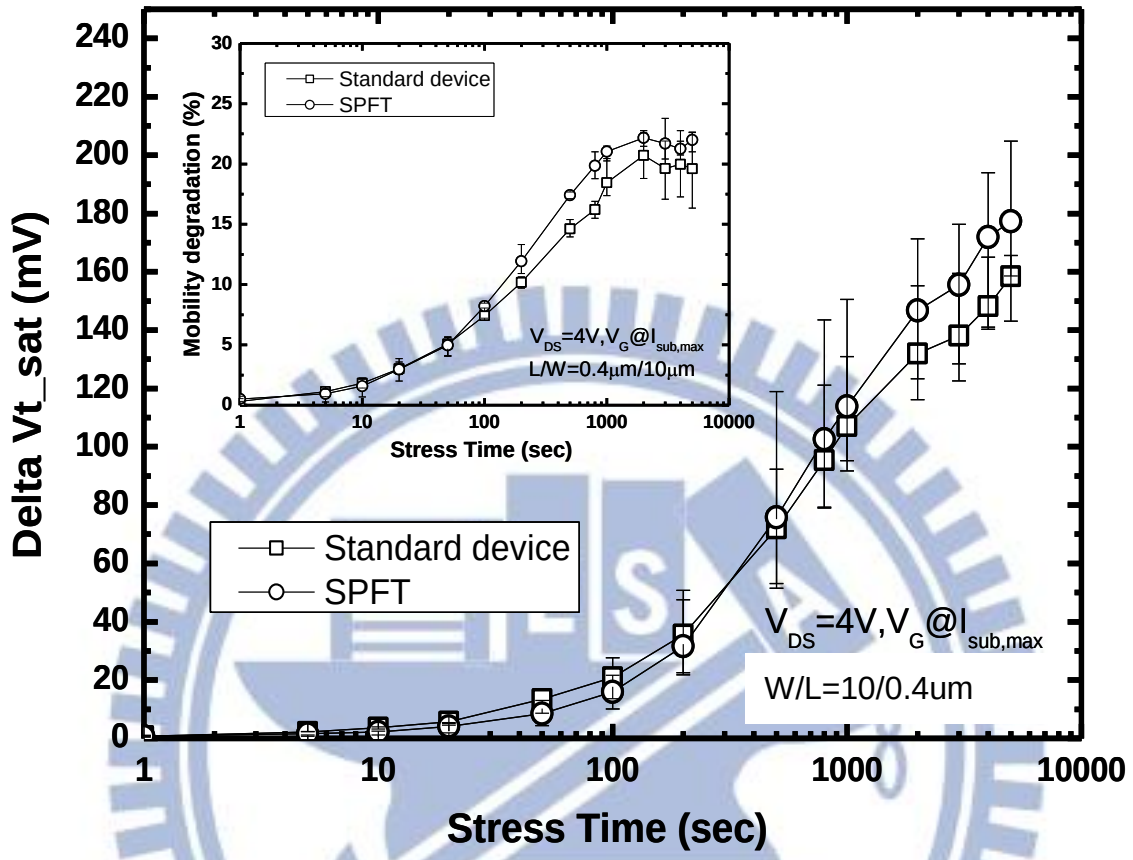


Fig. 4-15 Threshold voltage shift ($\triangle V_{th}$) for SPFT under hot carrier stressing at V_{DS} = 3.5V, $V_g = V_{g,\text{(maximum substrate current)}}$. Channel width/length = 10 um/0.4 um. In the inset, the mobility degradation under identical stress conditions is shown.

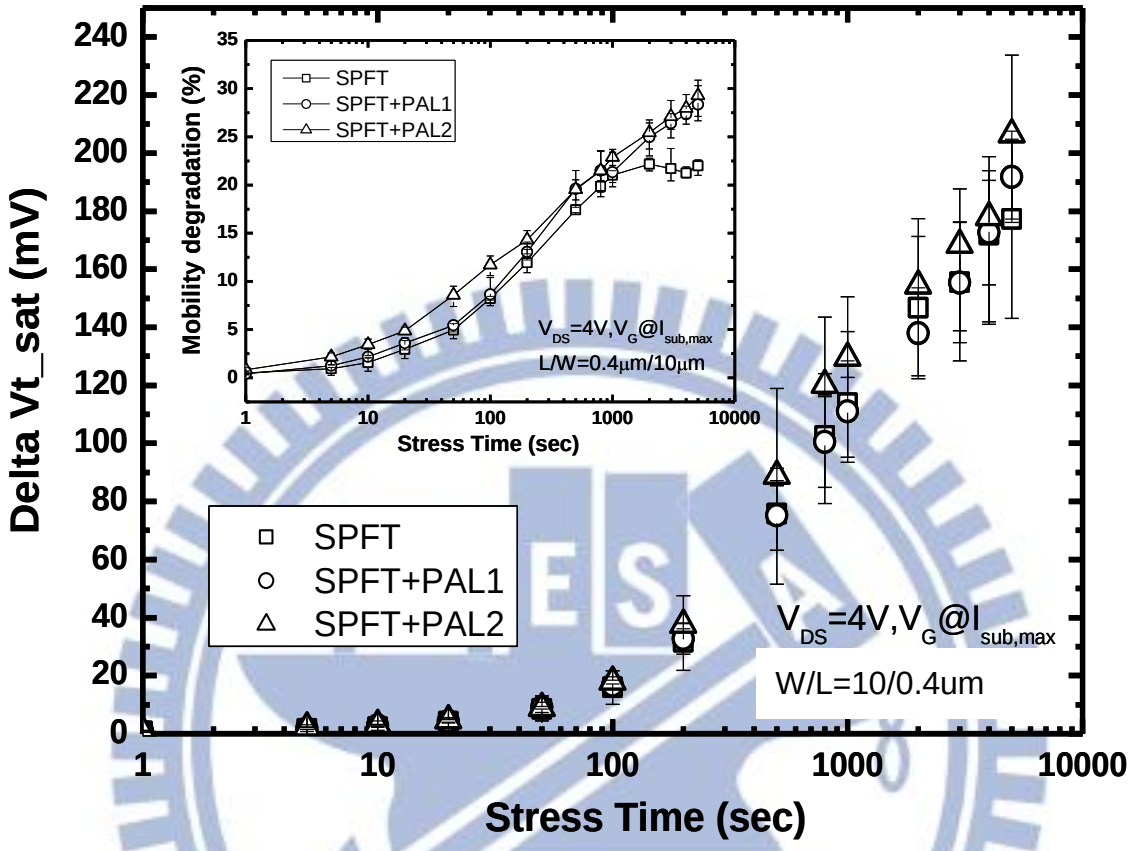


Fig. 4-16 Threshold voltage shift ($\triangle V_{th}$) for SPFT combing with PAL gate structure under hot carrier stressing at V_{DS} = 3.5V, V_g = $V_{g,\text{(maximum substrate current)}}$. Channel width/length = 10 um/0.4 um. In the inset, the mobility degradation under identical stress conditions is shown.

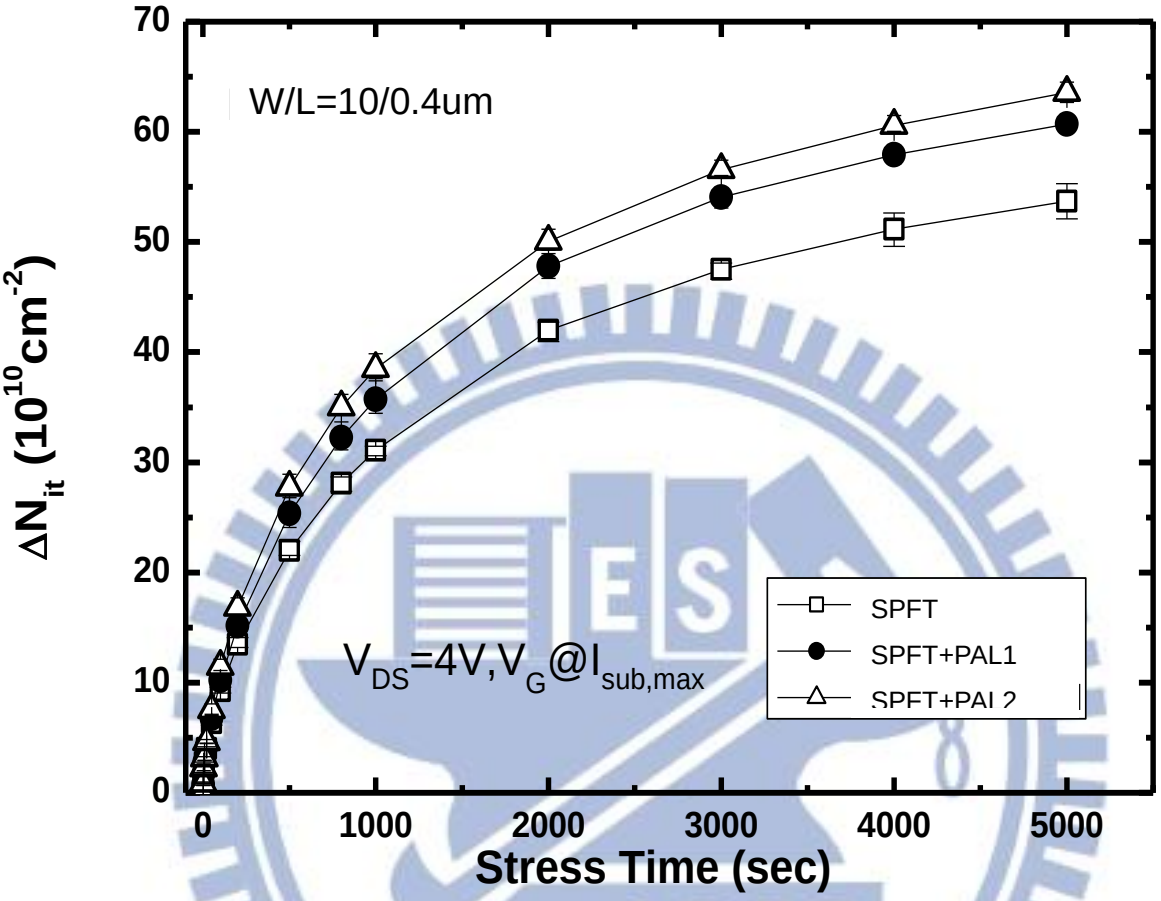


Fig. 4-17 Gate oxide interface state density shift ($\triangle N_{it}$) under hot carrier stressing. Channel width/length = 10 um/0.4 um

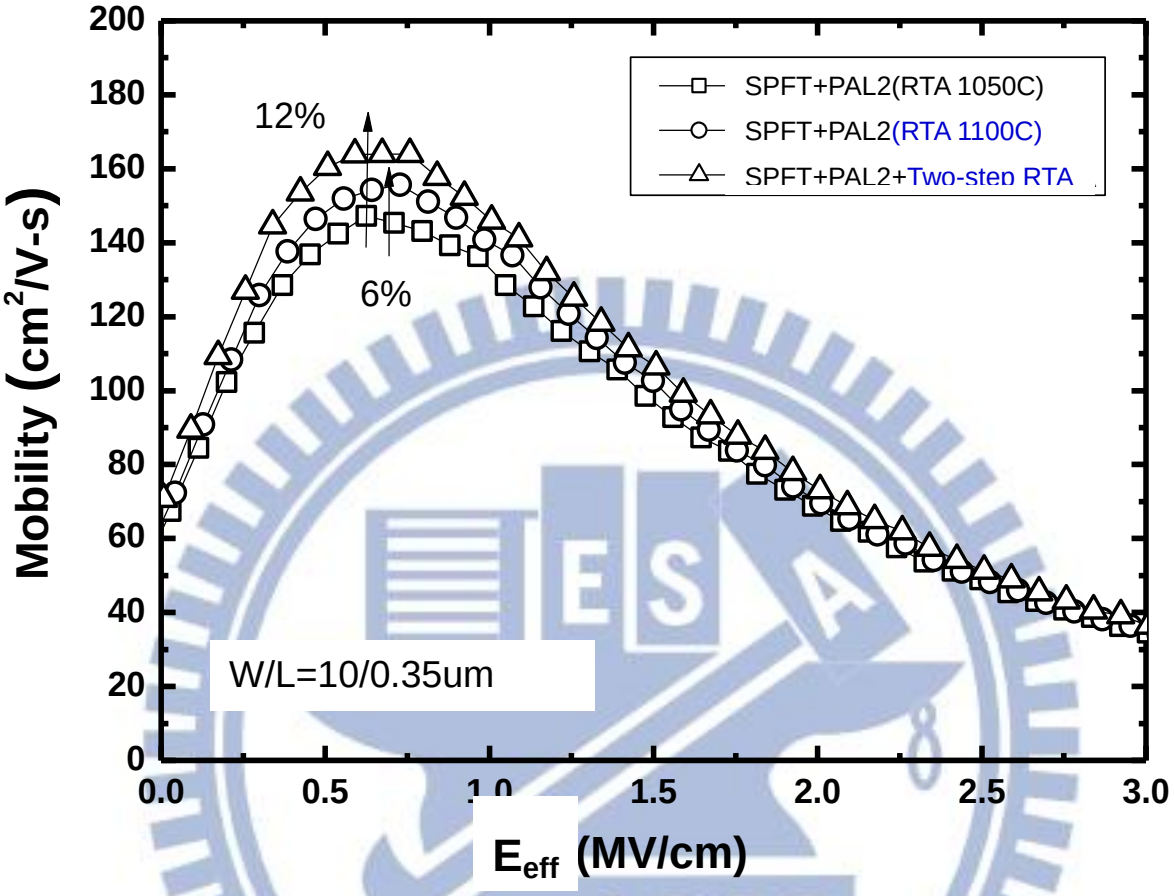


Fig. 4-18 nMOSFET electron mobility for SPFT with PAL2+RTA 1100℃ and two-step RTA process on channel width/length = 10 um/0.35 um

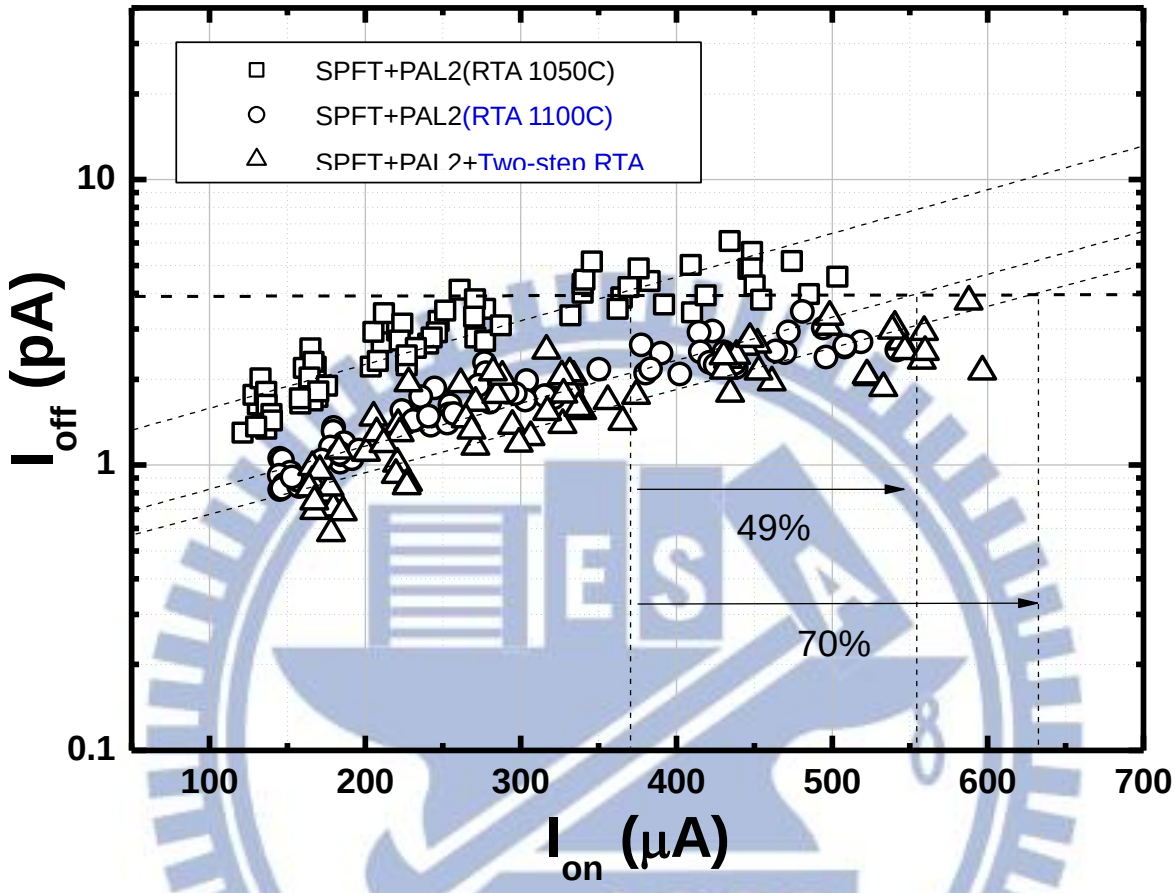


Fig. 4-19 Corresponding Ion-Ioff characteristics of SPFT with PAL2+ RTA 1100℃ and two-step RTA process

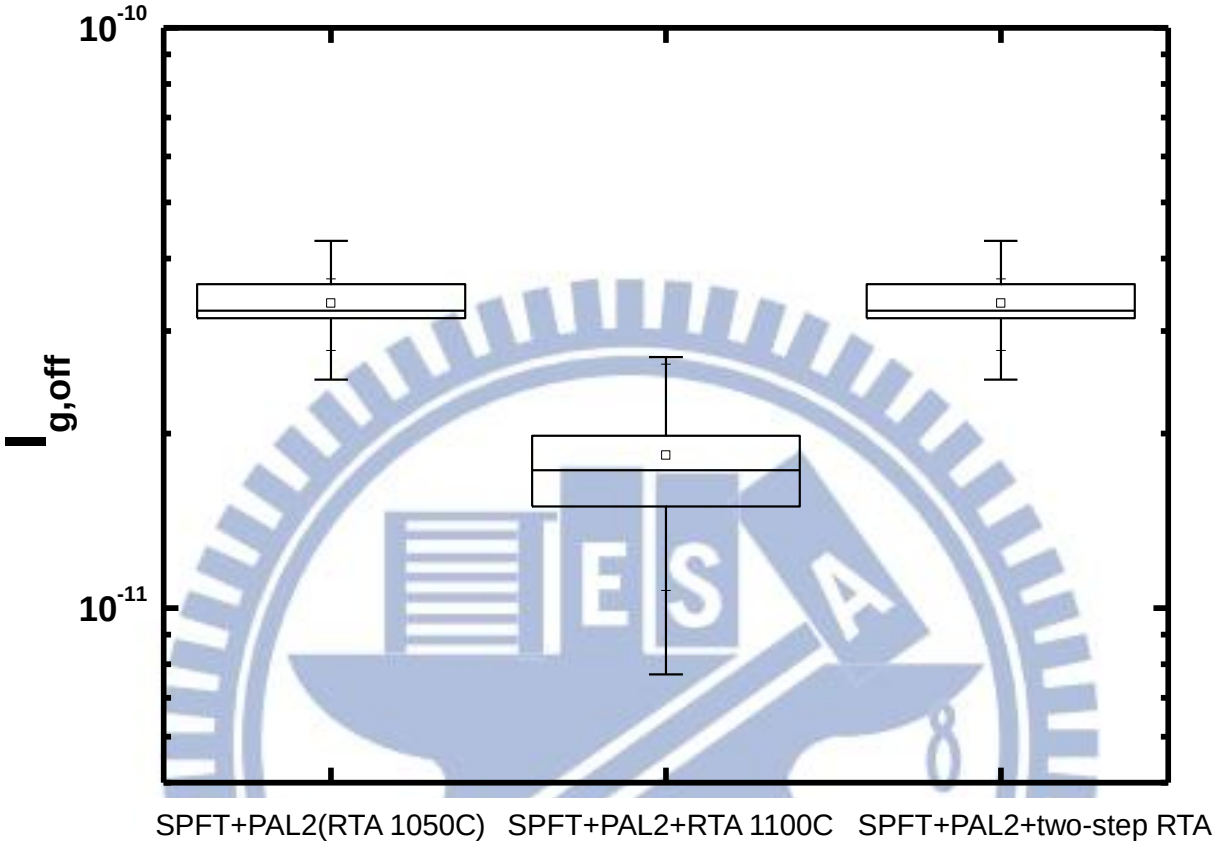


Fig. 4-20 Gate leakage current of SPFT with PAL2+ RTA 1100℃ and two-step RTA process

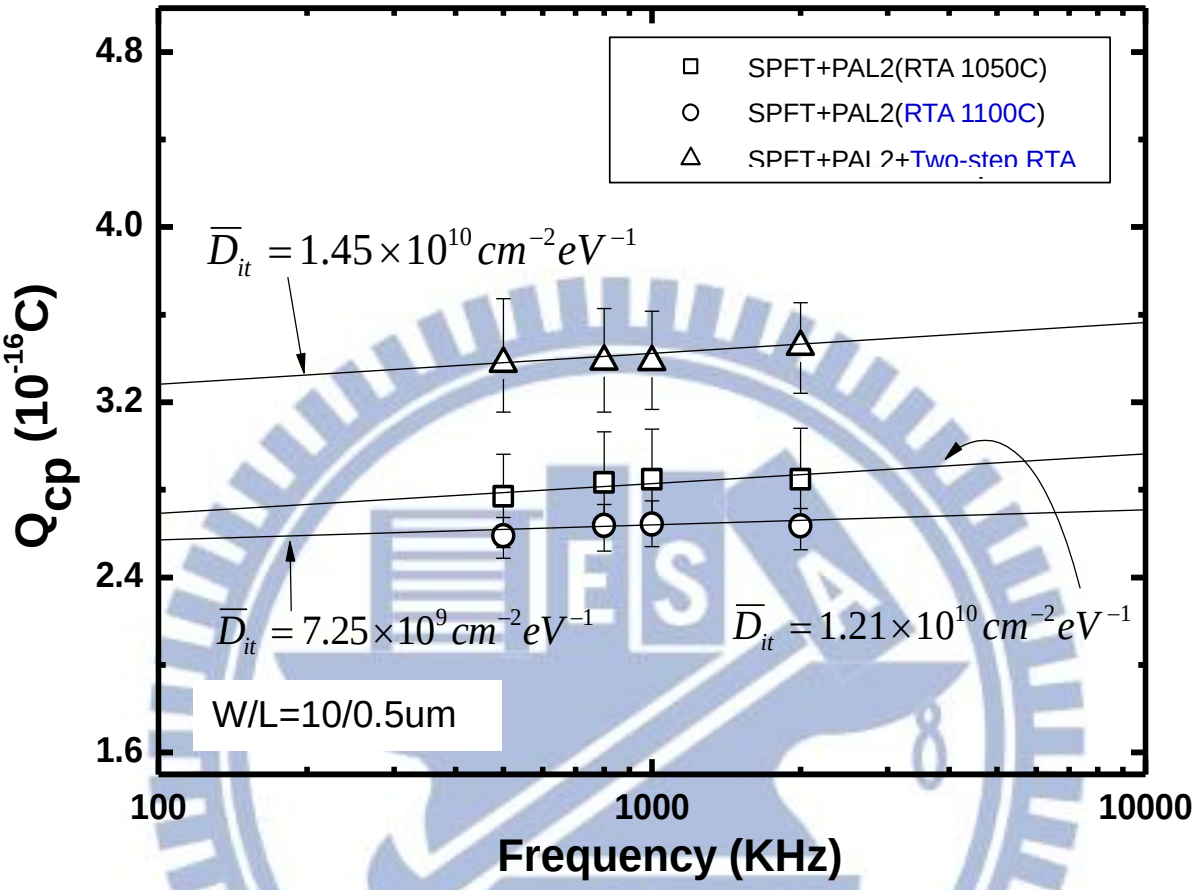


Fig. 4-21 Gate oxide interface state density of SPFT with PAL2 + RTA 1100℃ and two-step RTA process

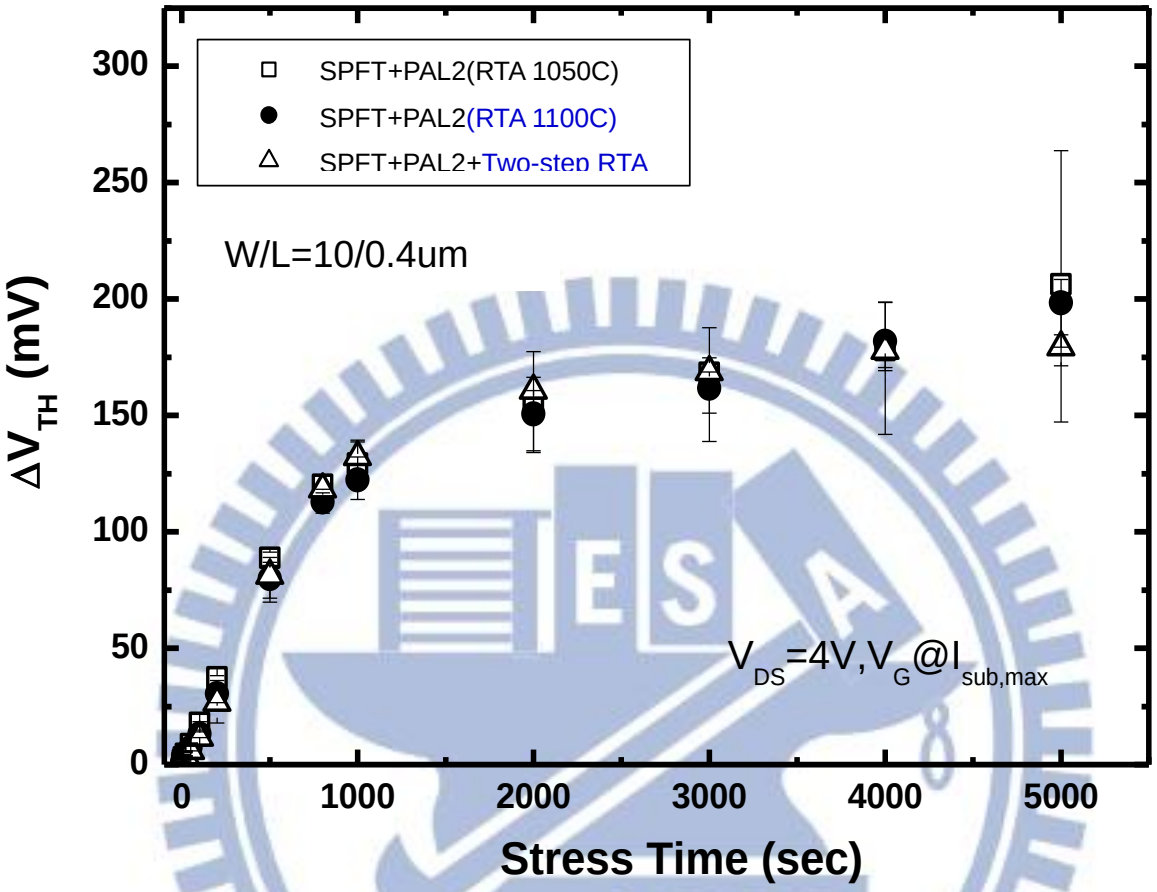


Fig. 4-22 Threshold voltage shift (△Vth) under hot carrier stressing at VDS = 4V, Vg = Vg, (maximum substrate current). Channel width/length = 10 um/0.4 um.

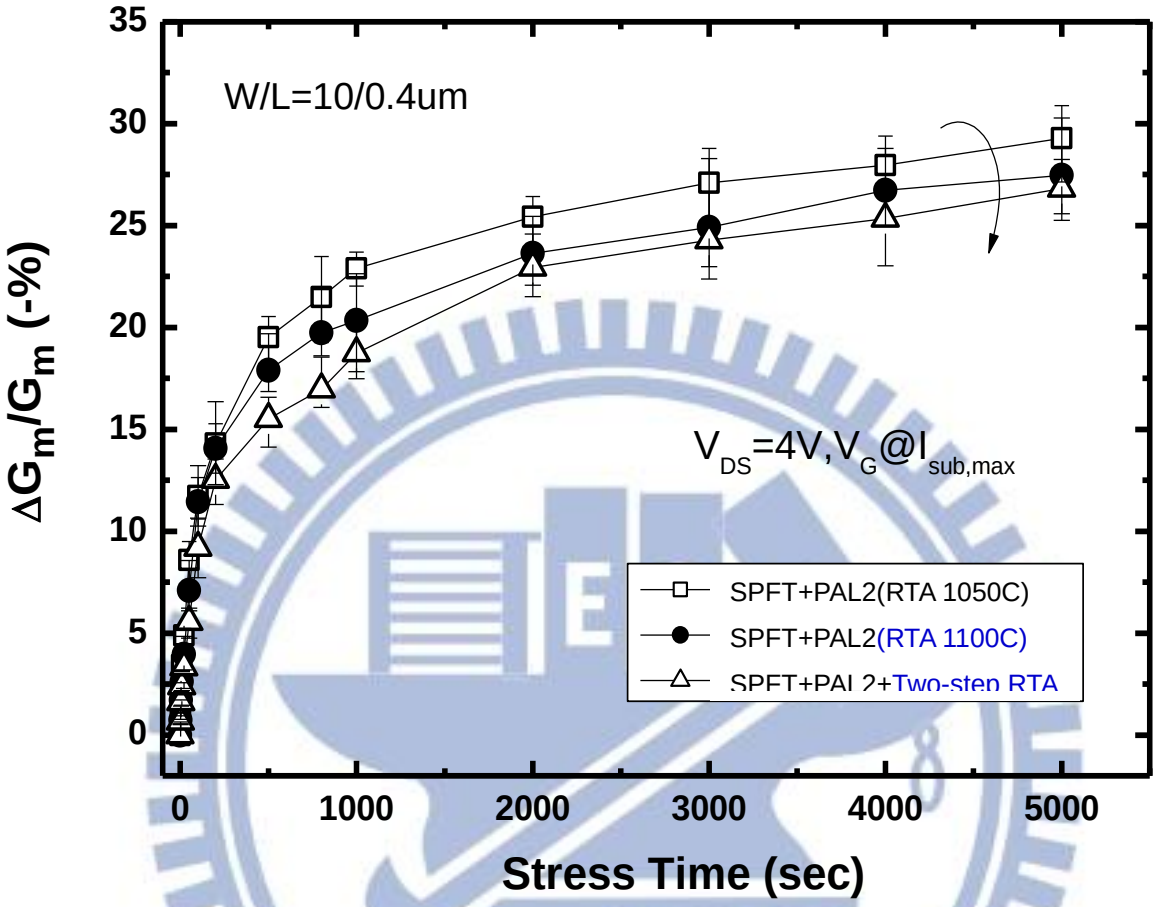


Fig. 4-23 Transconductance shift (△Gm) under hot carrier stressing at VDS = 4V, Vg = Vg, (maximum substrate current). Channel width/length = 10 um/0.4 um.

Chapter 5. Temperature Sensitivity for SPFT and SPFT with PAL Gate Structure

5.1 Introduction

For sub-65nm CMOS technology development, mobility improvement by strain engineering will be limited by the narrowing gate space. Stressor volume limitation and process integration issues are the key challenges for boosting performance in circuit applications. Stress memorization technique (SMT) has been reported to improve electron mobility in nMOSFETs and has been widely studied using different methods. However, most previous studies have demonstrated the performance boost without considering the scalability of the gate space in high density circuits. Longitudinal tensile stress along device channel becomes limited as the stressor volume reaches its saturation point, causing performance degradation.

Strain-proximity-free technique (SPFT) has been shown to offer performance improvement without the limitation of stressor volume in high density CMOS circuits. In this study, we demonstrate electron mobility and drain current improvement in nMOSFETs by using SPFT in combination with a PAL gate structure. The temperature dependence of electron mobility in the strain gate structure is also discussed. In order to extend the applications of devices operating across wide temperature ranges, analysis of the electrical properties at various temperatures is

required. Phonon scattering dominating electron mobility at high temperatures by lattice vibration is a well known mechanism in Si. We have found that the gain in electron mobility in SPFT in combination with PAL gate structure decreases at high temperatures. Gate dielectric and Si interface properties are investigated to explain this phenomenon. Furthermore, zero-temperature-coefficient (ZTC) point, which is an important parameter for CMOS circuits work over an operated temperature, is also discussed in order to check strain dependence of temperature effect on the SPFT and DTMOS SPFT in combination with PAL gate structures [30].

5.2 Experiments

nMOSFETs were fabricated on 6-in wafers with a resistivity of 15-25 Ω-cm. 2.0 ± 0.1 nm gate-oxide and 200nm poly-Si grown in a vertical furnace. The process flow of SPFT, proposed in order to introduce stress into the channel, is illustrated in Fig. 5-1. Before patterning of the poly-Si gate, the SPFT was processed by high tensile stressor deposition, Rapid-Thermal-annealing (RTA) using spike annealing at 1050℃, and stressor removal processes. The stressor used in the SPFT was a high tensile thermal CVD SiN film of 100nm thickness. The stress level of this film is close to 1.3 GPa. The PAL gate structure is proposed by pre-amorphous layer (PAL2) in gate using an implantation process, which was discussed in the chapter 4. It was inserted

into the SPFT process after poly deposition. The dosage split of the arsenic is [40 keV, 5E15 cm-2]. The pre-amorphous layer combines a two-step annealing processes with SPFT (PAL2+Two-step RTA), which, inserted after the stressor buffer oxide deposition, can bring greater stress into the channel. Dry and wet etching was used in the stressor removal process. After gate patterning, source/drain extension (SDE) implantation, side wall spacer and S/D formation were carried out. A 100nm thermal CVD tensile SiN CESL was deposited on all transistors. After interlayer dielectric (ILD) film deposition and contact patterning, a four-level metallization (Ti-TiN-Al-TiN) was carried out in the PVD system.

5.3 Results and Discussions

The electrical gate oxide inversion thickness is around 29.6+/-0.2Å for all split conditions. The performance improvement of nMOSFET in SPFT at various temperatures is illustrated in Fig. 5-2. At room temperature, electron mobility is improved by 15% using SPFT, compared to standard (STD) devices. Moreover, a significant improvement in mobility in SPFT with PAL2 and PAL2+Two-step RTA is found. It appears that SPFT with PAL2 and PAL2+Two-step RTA can further improve mobility, by 33% and 52%, respectively. Temperature sensitivity of electron mobility on SPFT with PAL gate structures are also shown in Fig. 5-2. It is found that

the mobility is decreased as temperature is increased. This may be attributed to phonon scattering and reveals mobility degradation [31]. However, the gain of mobility by SPFT in combination with PAL2 and PAL2+Two-step RTA is also decreased when temperature is increased. The slopes of the STD, SPFT, SPFT with PAL2 and PAL2+Two-step RTA are -0.78, -0.82, -1.29 and -1.53, respectively. Higher temperature leads to lower electron mobility gain in the SPFT with the PAL gate structure. The mobility degradation of SPFT with PAL gate structures is more serious than in STD device at high temperature region. It implies the strain dependence of mobility improvement becomes weaker at high temperatures, especially on the SPFT in combination with PAL gate structures.

Fig. 5-3. shows measured drain current at various temperatures. A significant improvement of drain current in SPFT and SPFT with PAL2 and PAL2+Two-step RTA accompanies the improvement of electron mobility. The drain current shows a similar trend with the mobility under various temperatures. It is also shown that the drain current is decreased at higher temperatures. Besides, the gain of drain current by SPFT in combination with PAL2 and PAL2+Two-step RTA is also decreased when temperature is increased. The slopes of the fitting curves on STD, SPFT, SPFT with PAL2 and PAL2+Two-step RTA are -0.27, -0.32, -0.63 and -0.96, respectively. The drain current degradation of SPFT with PAL gate structures is more serious than in

STD device at high temperatures. This result is consistent with the mobility trend and attributes to the weaker strain at high temperatures, especially on the SPFT with PAL gate structures. The mobility improvement of DTMOS SPFT at various temperatures is illustrated in Fig. 5-4. Higher mobility gain can be achieved in DTMOS SPFT with PAL gate structures and had discussed in chapter. 4. However, the mobility degradation of SPFT with PAL gate structures becomes serious in high temperature is still observed in DTMOS structures. This result implies the reduced gain of mobility at high temperatures is not attributed by higher substrate current or channel doping concentration.

The threshold voltage Vth of SPFT at various temperatures is illustrated in Fig. 5-5. It is found that the Vth is decreased when temperature is increased. Higher temperature leads to increase energy band bending φ_s at Si surface and results to reduce the threshold voltage. Not similar to the mobility and the drain current behavior at high temperatures, the Vth slope of SPFT with PAL gate structures is comparable to the standard device. It appears to show that the serious mobility and drain current degradation at high temperatures are not attributed by anomalous threshold voltage. Besides, the delta Vth of SPFT with PAL gate structures at high temperatures is also comparable to the single SPFT and the standard device, as illustrated in Fig. 5-6. Moreover, the threshold voltage of DTMOS SPFT with PAL

gate structures is illustrated in Fig. 5-7. It is also shown that the Vth is decreased as temperature is increased. The Vth slope of the DTMOS SPFT with PAL gate structures is comparable to the standard device at various temperatures. The delta Vth of DTMOS SPFT with PAL gate structures is shown in Fig. 5-8. Comparable delta Vth is found in both standard device and DTMOS SPFT with PAL gate structures at various temperatures.

Gate dielectric interface state density of SPFT with PAL gate structure is checked by measuring the charge pumping current (as shown in Fig. 5-9.). SPFT with PAL2 and PAL2+Two-step RTA obtained higher interface state density than the standard device. The gate dielectric interface charge and gate impurity play important roles in carrier scattering [32]. Electron mobility is dominated by Coulomb scattering at room temperature and low electric field region. Moreover, interface charge inducing Coulomb scattering is in proportion to temperature as $1/\mu_{int}(T) \propto T$ [33]. Simultaneously, more ionized impurities in the gate resulting from increasing temperature will enhance remote Coulomb scattering. Therefore we found the gain of electron mobility in the SPFT with PAL2 and PAL2+Two-step RTA is decreased at high temperatures. Moreover, it is possible that lighter effective mass shows stronger temperature dependence. In the original concept, we considered the effect of phonon scattering on all devices is the same. The temperature dependence of mobility gain

concerns the slope change in Fig. 5-2 and Fig. 5-3. Obviously, PAL2 and PAL2+Two-step RTA show different slopes than the STD device. The major difference between PAL2 and PAL2+Two-step RTA is an extra RTA for enhancing channel stress. Since the relaxation time in Δ2 valleys is shorter than Δ4 valleys, mobility degradation induced by interface charges is serious in strained-Si than in Si. Moreover, there are more impurities and interface charges in SPFT with PAL2 and PAL2+Two-step RTA. Therefore, we conjecture that the effects of interface charges and impurities scattering are enhanced by reducing screening effect under high temperature conditions.

The definition of Zero temperature coefficient Vg(ZTC) is the drain current independent of temperature at Vg=Vg(ZTC). For Vd>Vg(ZTC), Idsat is decreased when temperature is increased(Negative temperature coefficient). For Vd<Vg(ZTC), Idsat is increased when temperature is increased(Positive temperature coefficient). In general, lower Vg(ZTC) for lower Vd is expected for low power device. Vg(ZTC) of SPFT is shown in Fig. 5-10. We measured the Vg(ZTC) of all samples for operation at room temperature to military range 20℃ to 120℃. Vg(ZTC) of STD, SPFT, SPFT with PAL1, PAL2 and PAL2+Two-step RTA is 1.4V, 1.35V, 1.25V, 1.15V, 1V, respectively. It is found that the temperature independent Vg(ZTC) is decreased in the SPFT and SPFT with PAL gate structures. Another way to find the Vg(ZTC) by

comparing delta Isat at 60℃, 100℃ and 120℃ with Isat at 20℃, as illustrated in Fig. 5-11. Consistent Vg(ZTC) with previous result is obtained by this measurement. The mechanism of decreasing Vg(ZTC) on SPFT and combine it with PAL gate structures is try to figure out. As shown in Fig. 5-12, Vg(ZTC) shows a strong correlation with the threshold voltage (Vth). Since the strain dependence of mobility improvement in SPFT will lead the Vth to decrease. Strong correlation between Vg(ZTC) and device threshold voltage (Vth) for SPFT and SPFT+PAL gate structure are expected to explain this phenomenon. The decreased Vth of SPFT and SPFT with PAL gate structures may be a root cause of decreasing Vg(ZTC). The Vg(ZTC) point of DTMOS transistor is also discussed, as illustrated in Fig. 5-13. It is found that the Vg(ZTC) in DTMOS transistor is ~100mV lower than standard transistor for both SPFT with PAL2 and PAL2+Two-step RTA. According to previous findings, it is suspected by lower Vth in DTMOS transistor than in standard MOS device. As shown in Fig. 5-14, consistent Vg(ZTC) can be achieved by comparing delta Isat at 55℃, 85℃ and 115℃ with Isat at 25℃.

The device performance of SPFT and SPFT with PAL gate structures is also verified at wide temperatures. Mobility improvement in SPFT and SPFT with PAL gate structures at various temperatures is illustrated in Fig. 5-15. Mobility degradation in SPFT with PAL gate structures is become serious at higher temperatures, which is

consistent to the previous discussions. However, mobility improvement is become stronger in SPFT with PAL2 and PAL2+Two-step RTA at lower temperatures. It is possible that lighter effective mass of electrons by strain engineering shows stronger temperature dependence than un-strained devices. A similar trend of drain current at various temperatures is shown in Fig. 5-16. Serious drain current degradation in SPFT and SPFT with PAL gates structures is attributed by mobility degradation. Fig. 5-17 shows the Vth of SPFT and SPFT with PAL gate structures at various temperatures. Insignificant Vth deviation is found in SPFT and in combination with PAL gate structure at various temperatures. This result is appears to explain the decreased gain in electron mobility at higher temperatures and stronger drain current boost at lower temperatures are not attributed by Vth deviation. Channel strain decreases at high temperatures may be a root cause of decreasing gain in electron mobility from SPFT.

5.4 Summary

We have proposed a scheme for electron mobility improvement that uses the SPFT in combination with a PAL gate structure. The gain of mobility decreases as temperature increases, due to the gate dielectric interface charges and ionized impurities. Therefore, controlling gate impurities and improving interface quality are the keys to continued improvement in future CMOS technology.

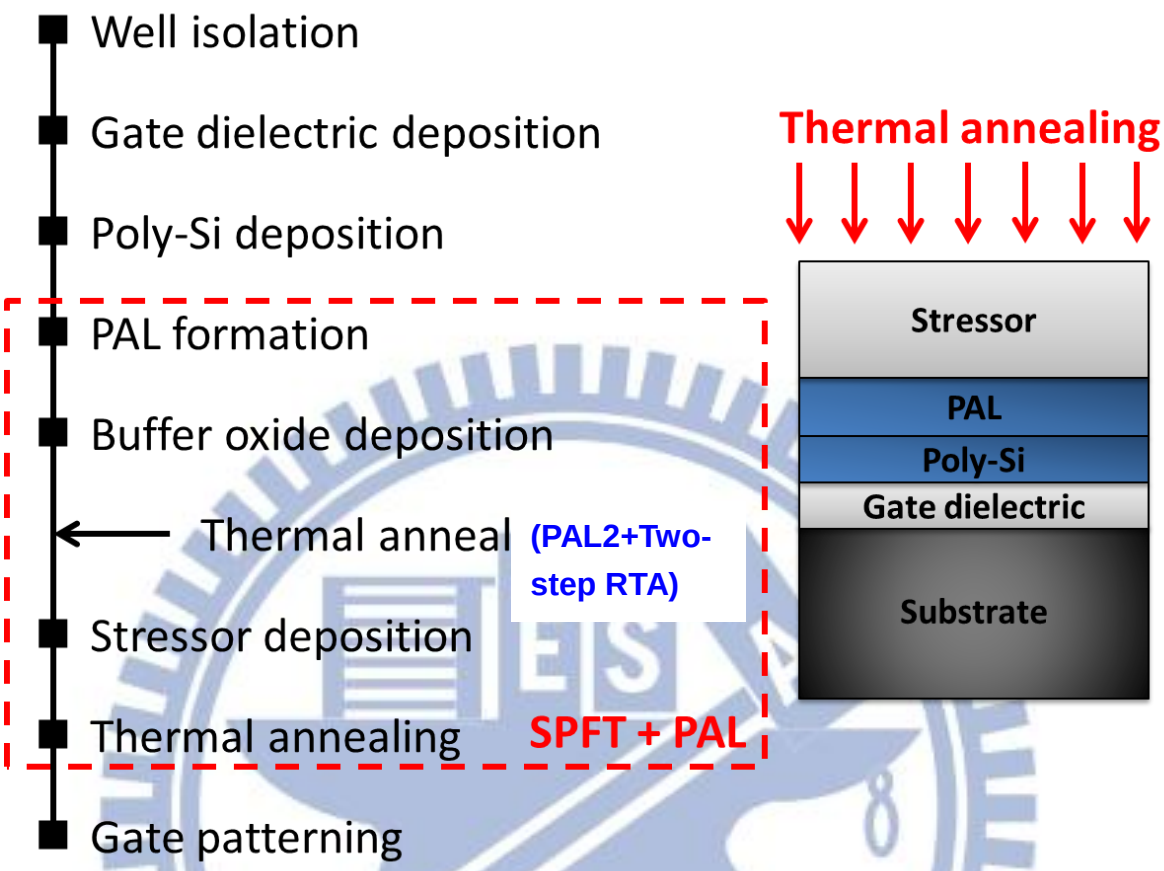


Fig. 5-1 Process flow of SPFT and SPFT with PAL gate structure

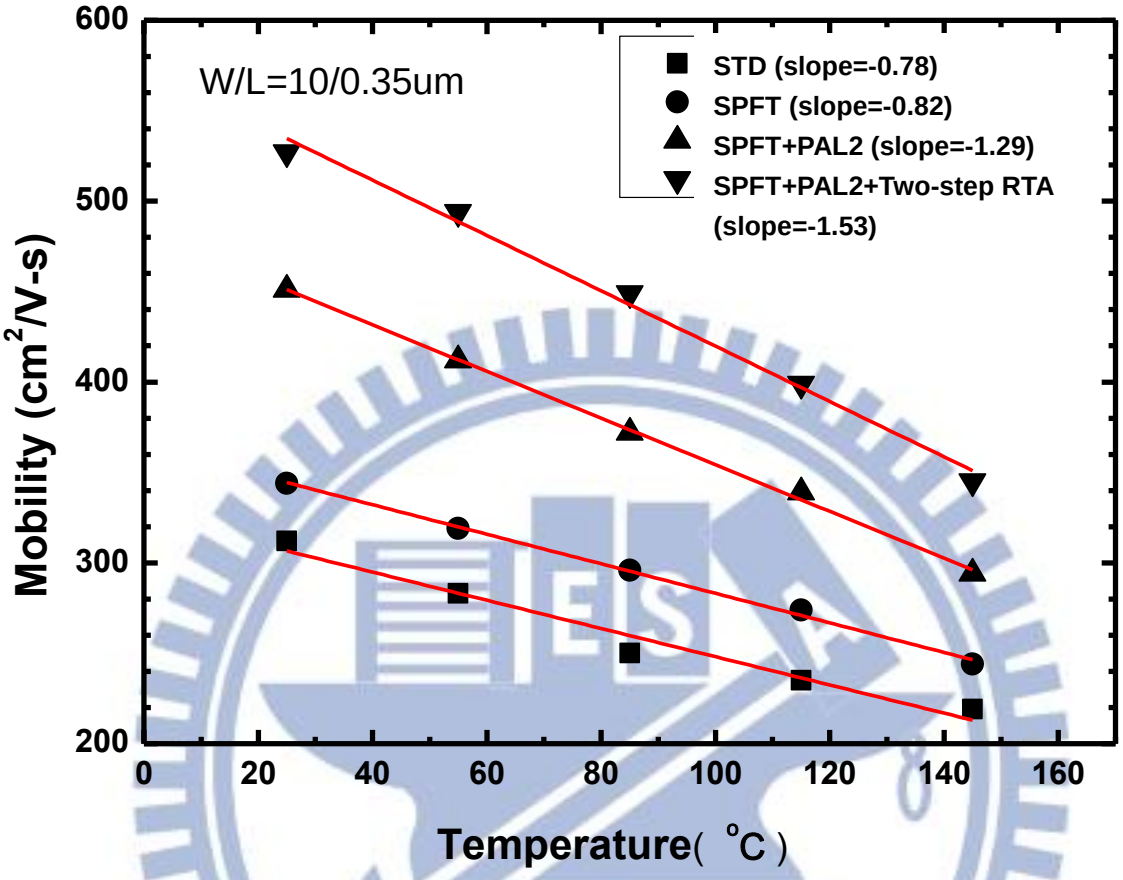


Fig. 5-2 Measured mobility for SPFT and SPFT with PAL gate structures at various temperatures

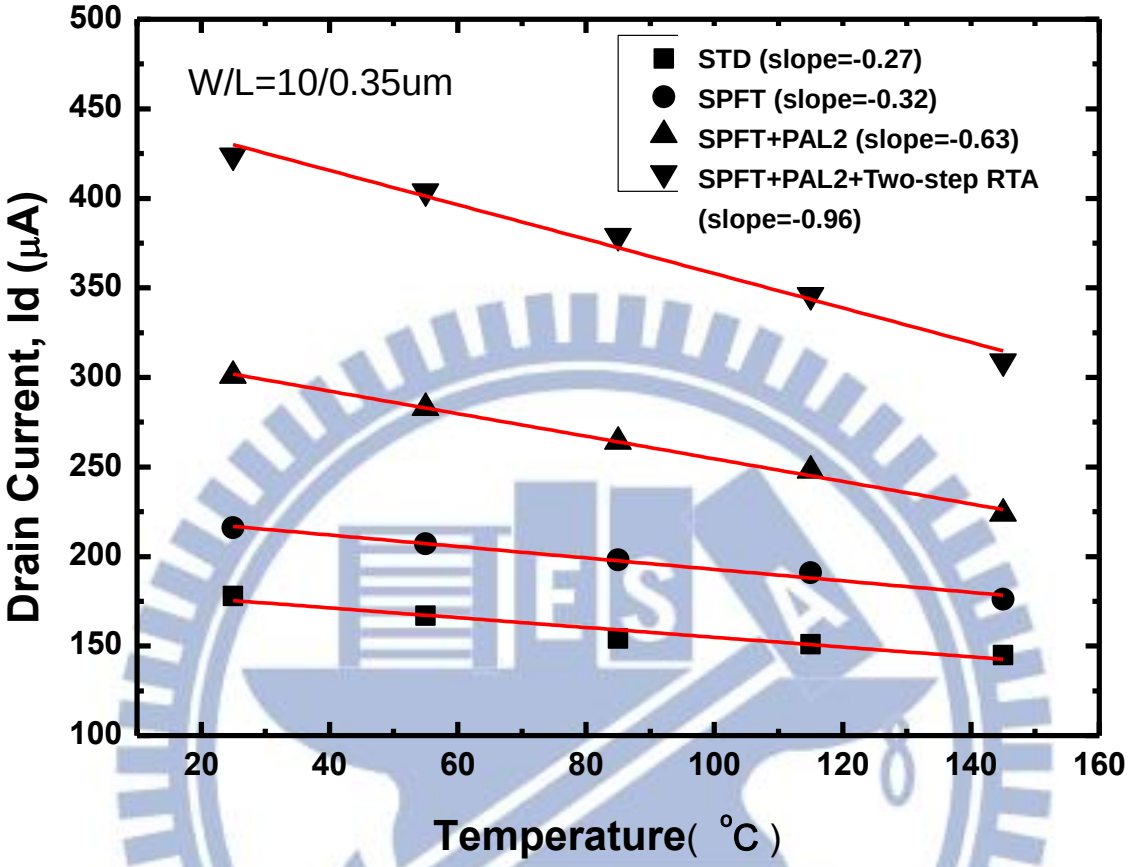


Fig. 5-3 Measured drain current for SPFT and SPFT with PAL gate structures at various temperatures

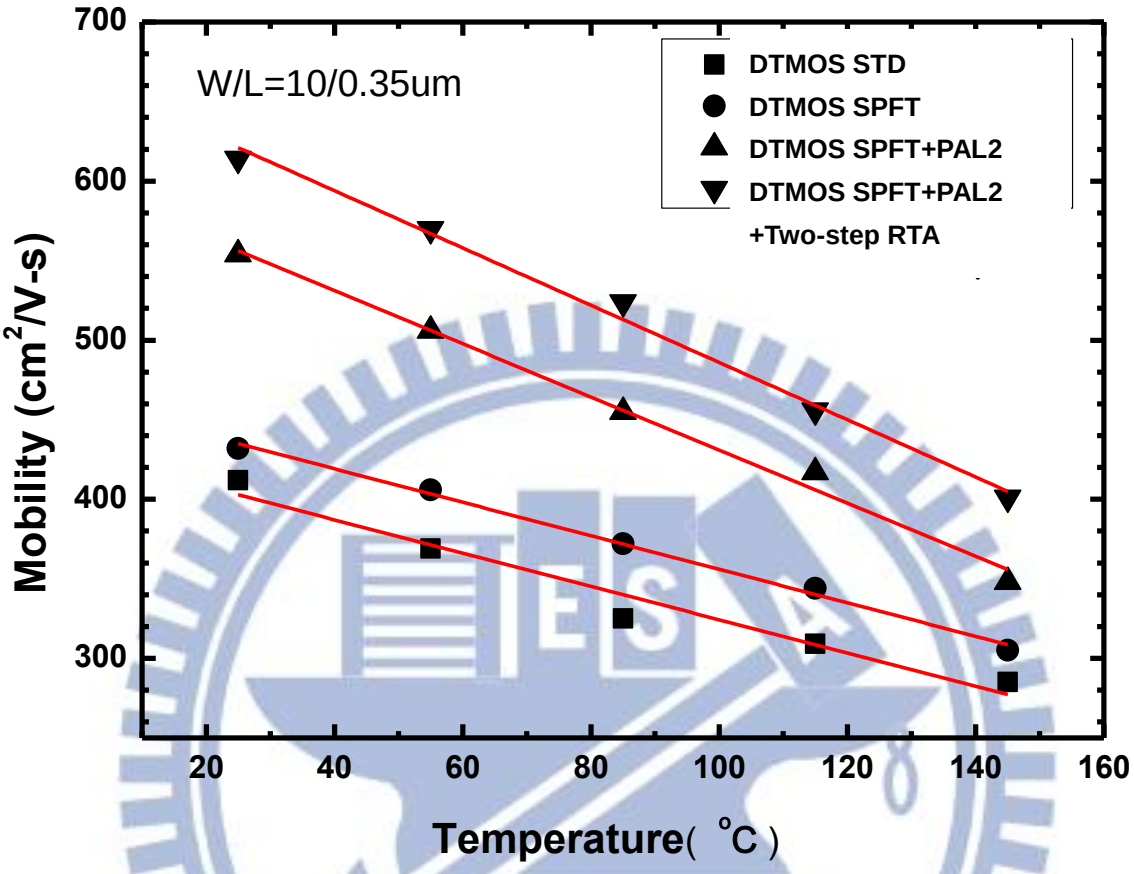


Fig. 5-4 Measured mobility for DTMOS SPFT and DTMOS SPFT with PAL gate structures at various temperatures

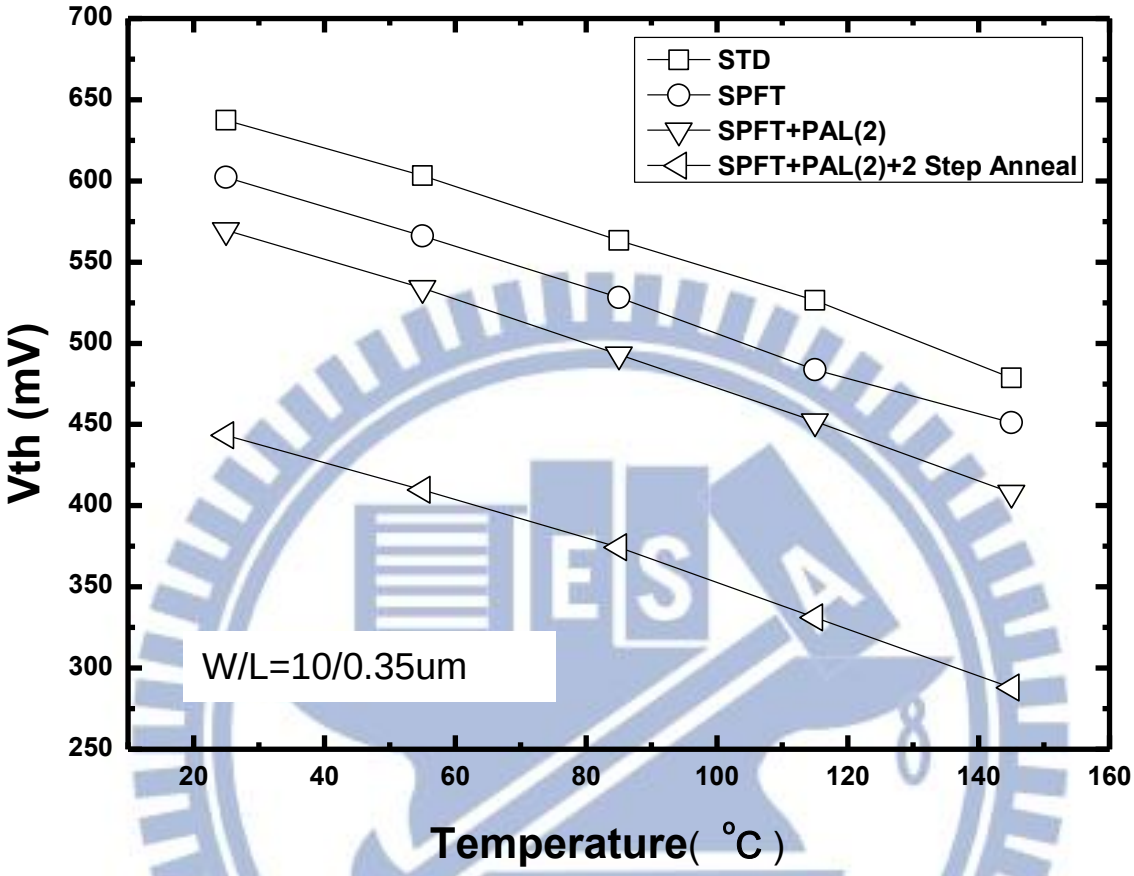


Fig. 5-5 Measured threshold voltage (Vth) for SPFT and SPFT with PAL gate structures at various temperatures

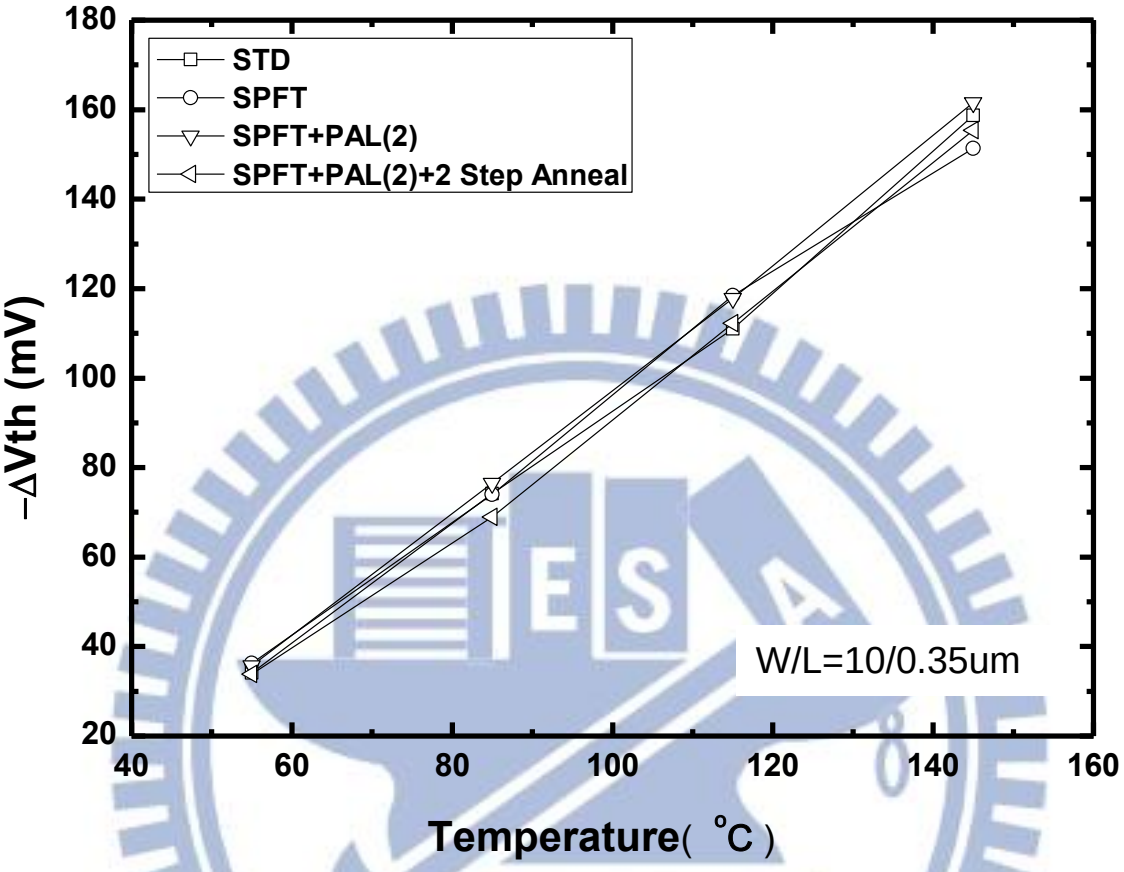


Fig. 5-6 Delta Vth of SPFT and SPFT with PAL gate structures at various temperatures

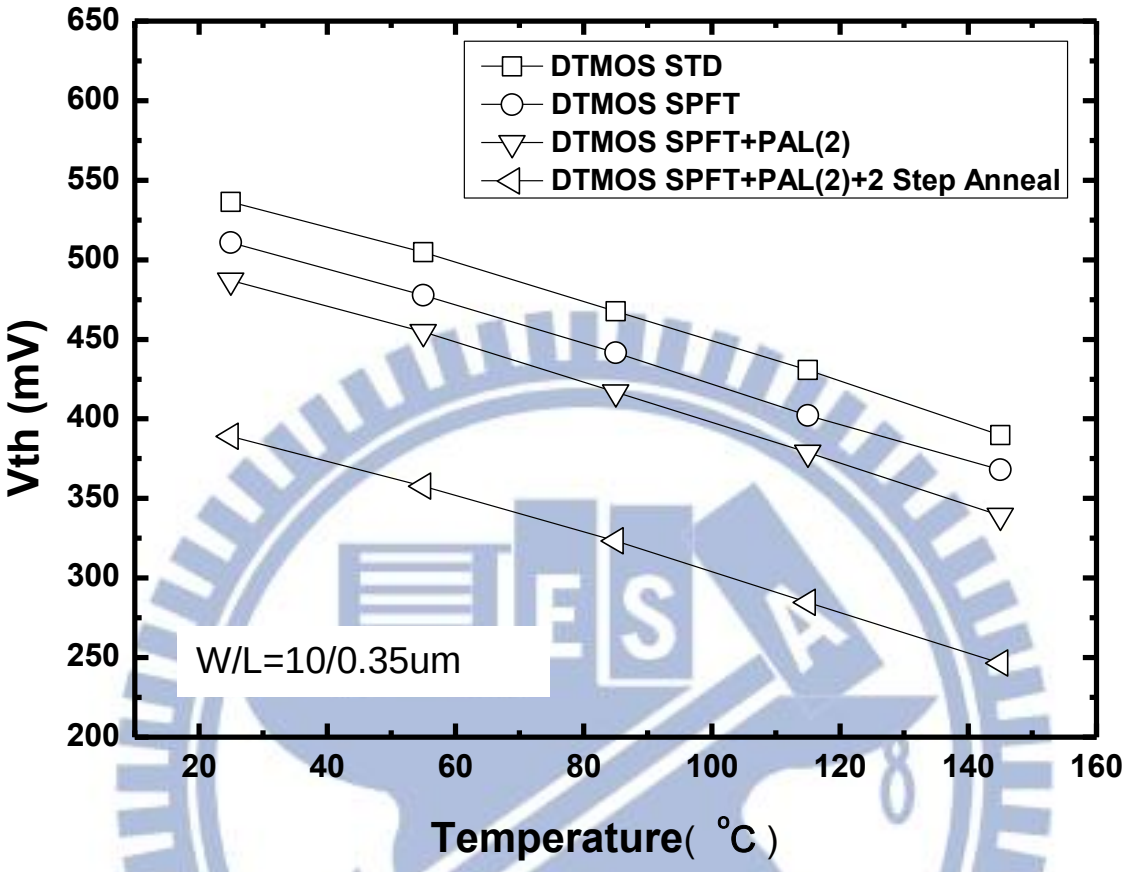


Fig. 5-7 Measured threshold voltage (Vth) for DTMOS SPFT and DTMOS SPFT with PAL gate structures at various temperatures

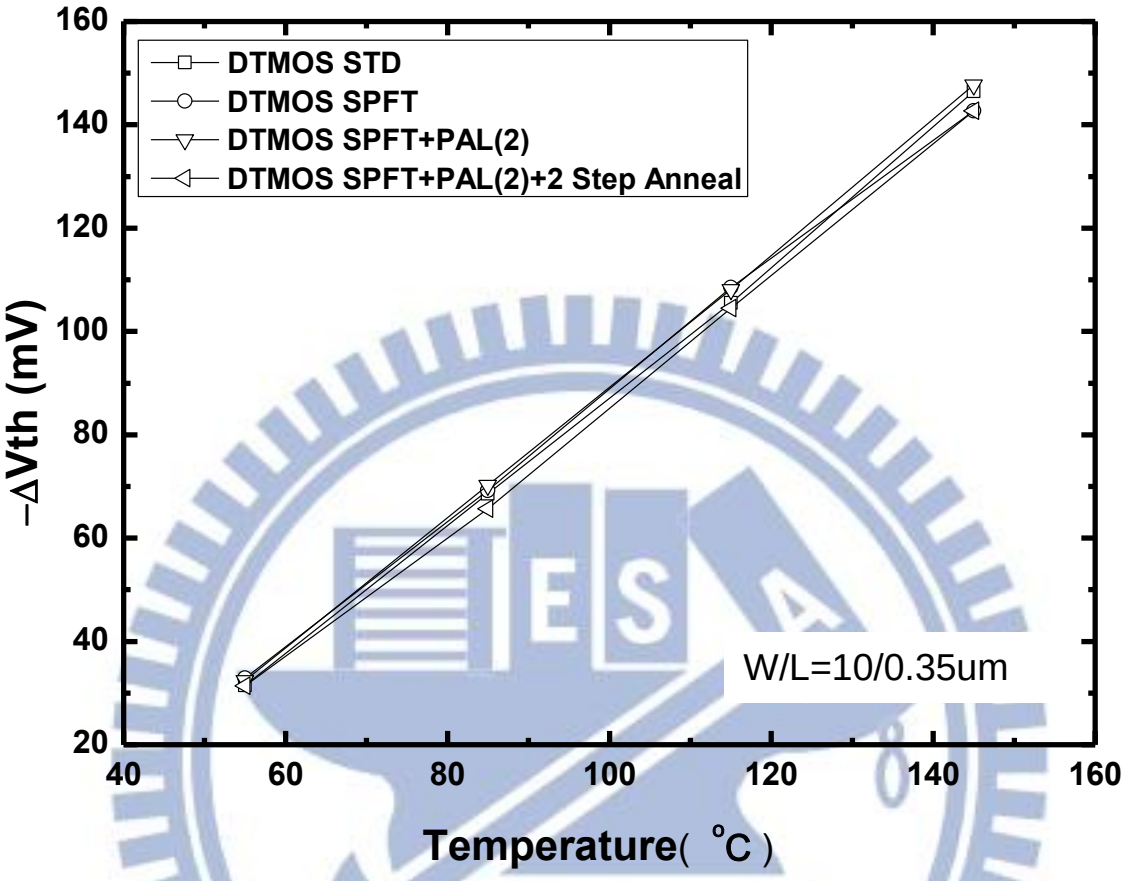


Fig. 5-8 Delta Vth of DTMOS SPFT and DTMOS SPFT with PAL gate structures at various temperatures

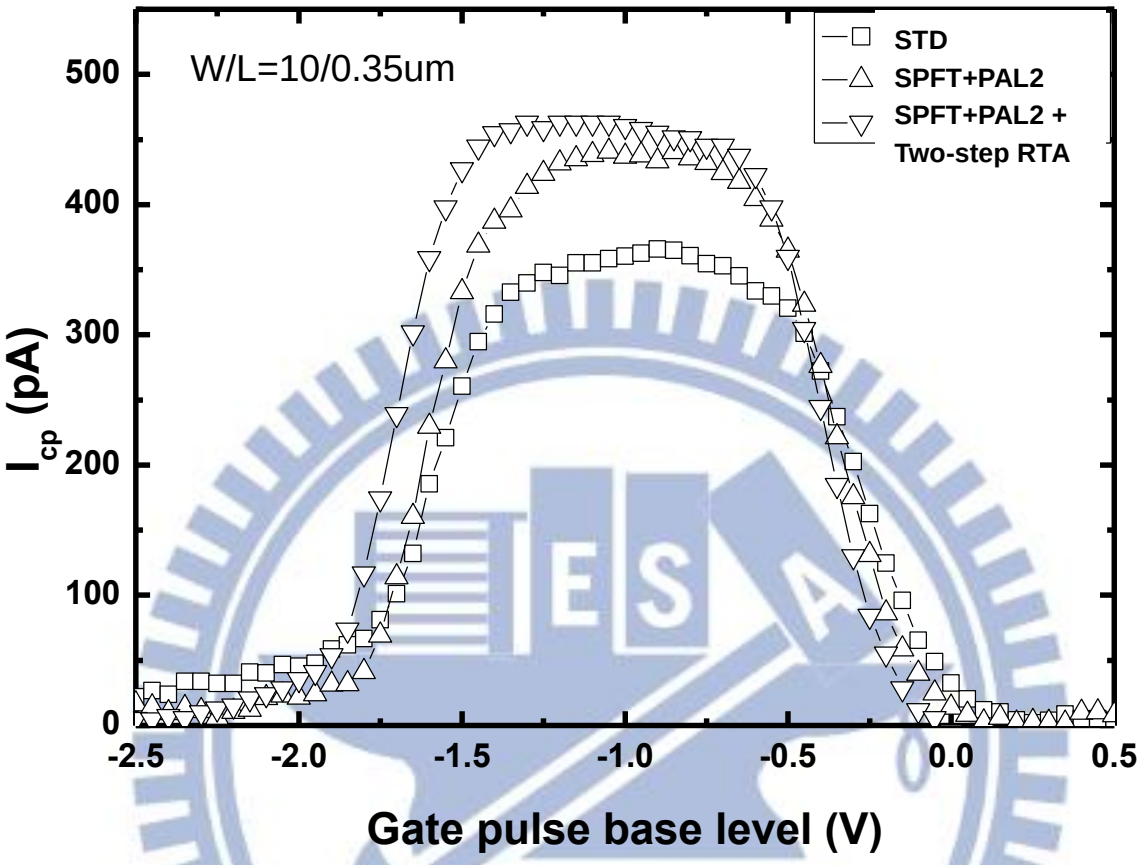


Fig. 5-9 Charge pumping current of SPFT and SPFT with PAL gate structures

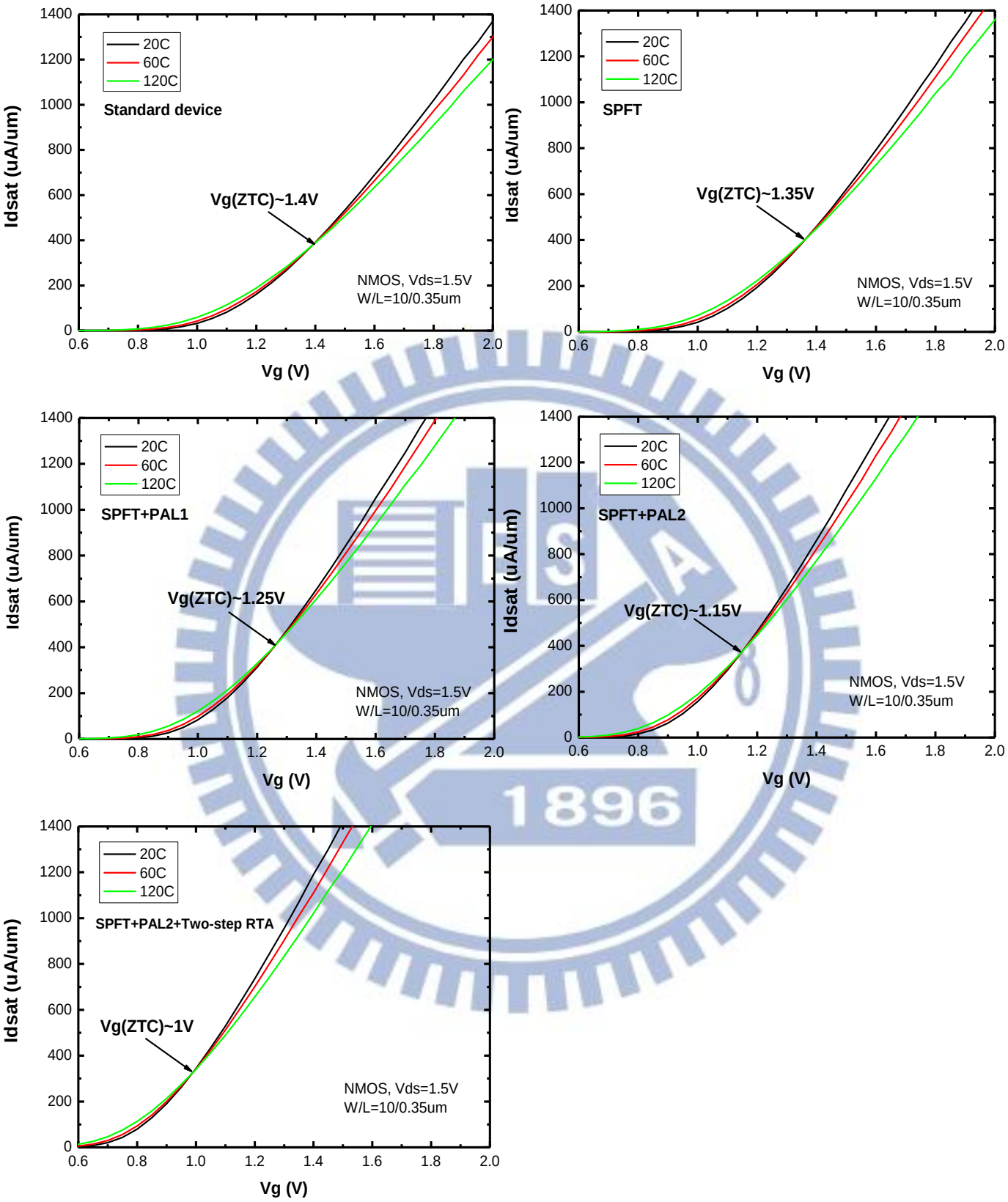


Fig. 5-10 Zero temperature coefficient Vg(ZTC) of SPFT and SPFT with PAL gate structures

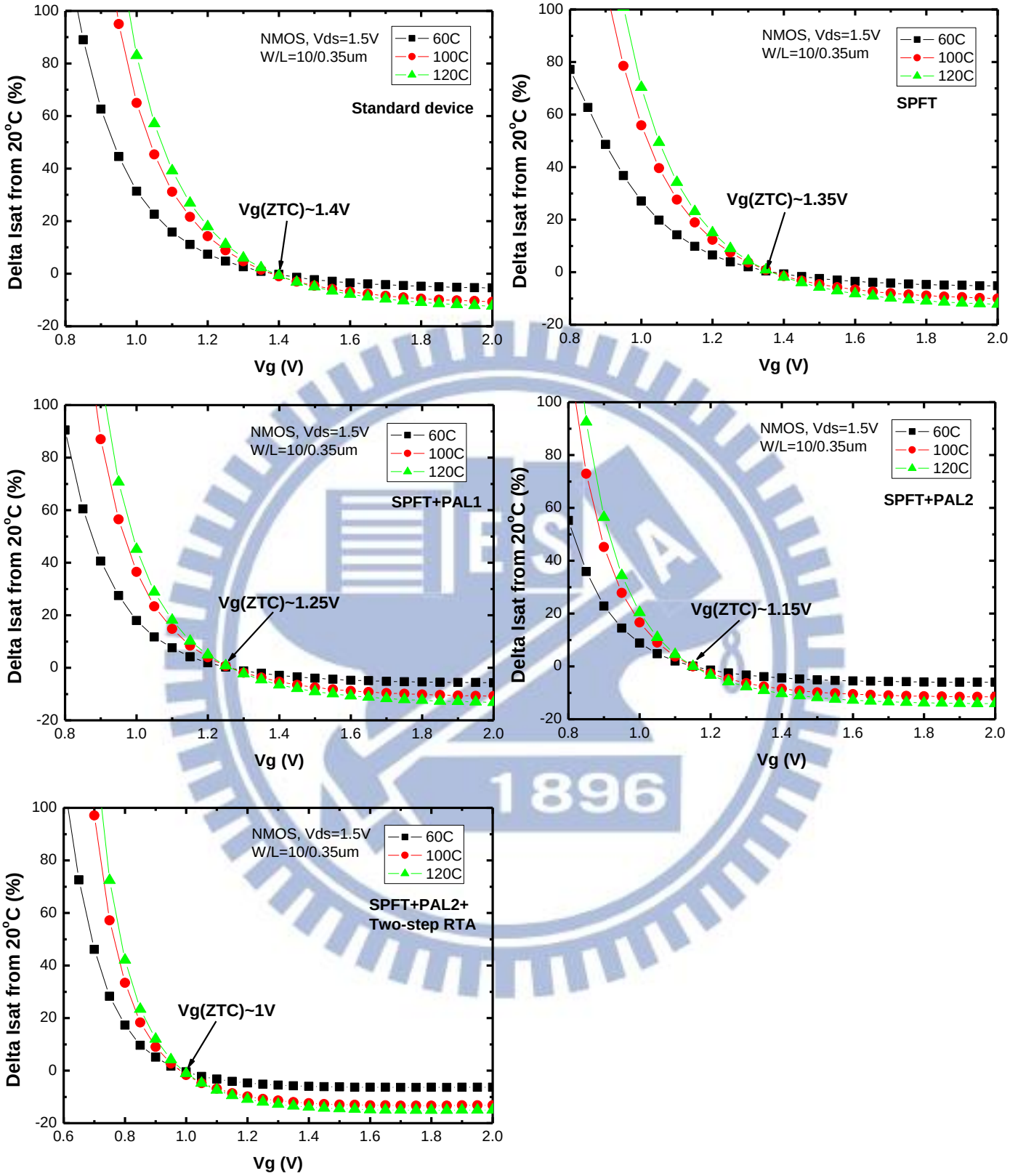


Fig. 5-11 Zero temperature coefficient Vg(ZTC) of SPFT and SPFT with PAL gate structures

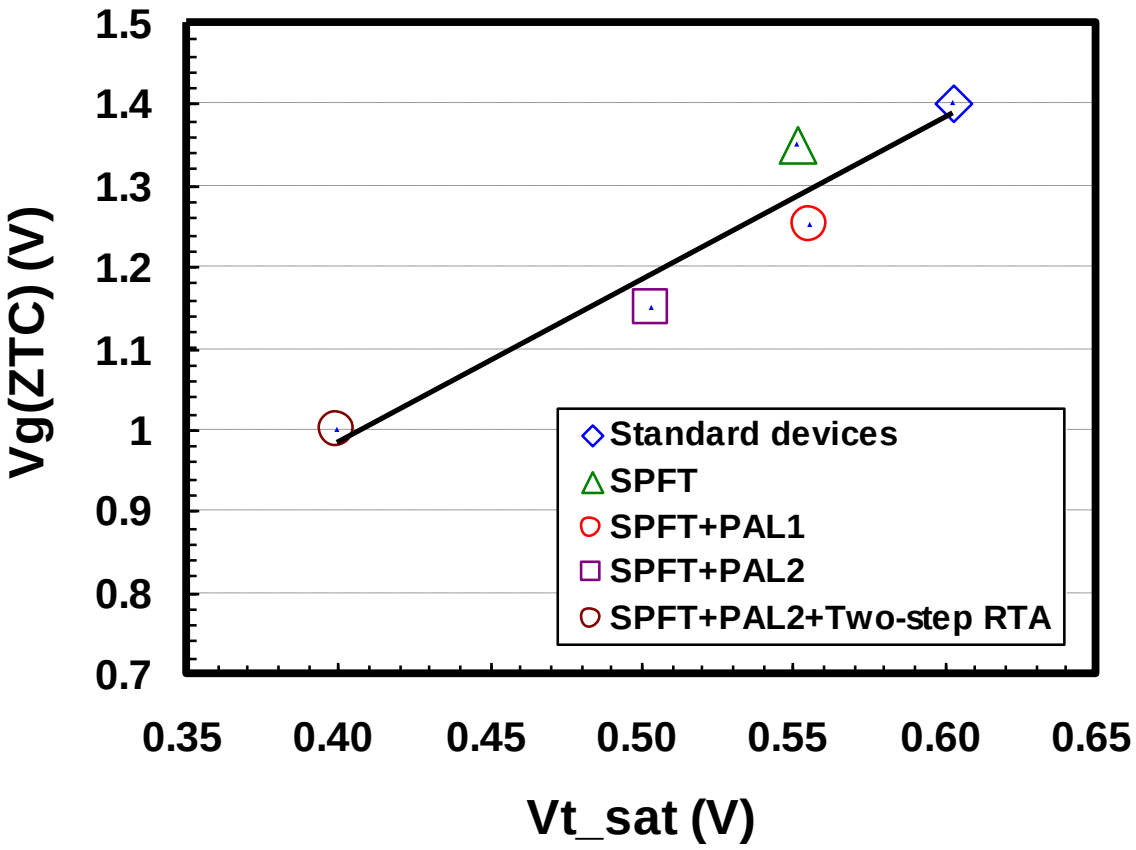


Fig. 5-12 Vg(ZTC) and threshold voltage correlation of SPFT and SPFT with PAL gate structures

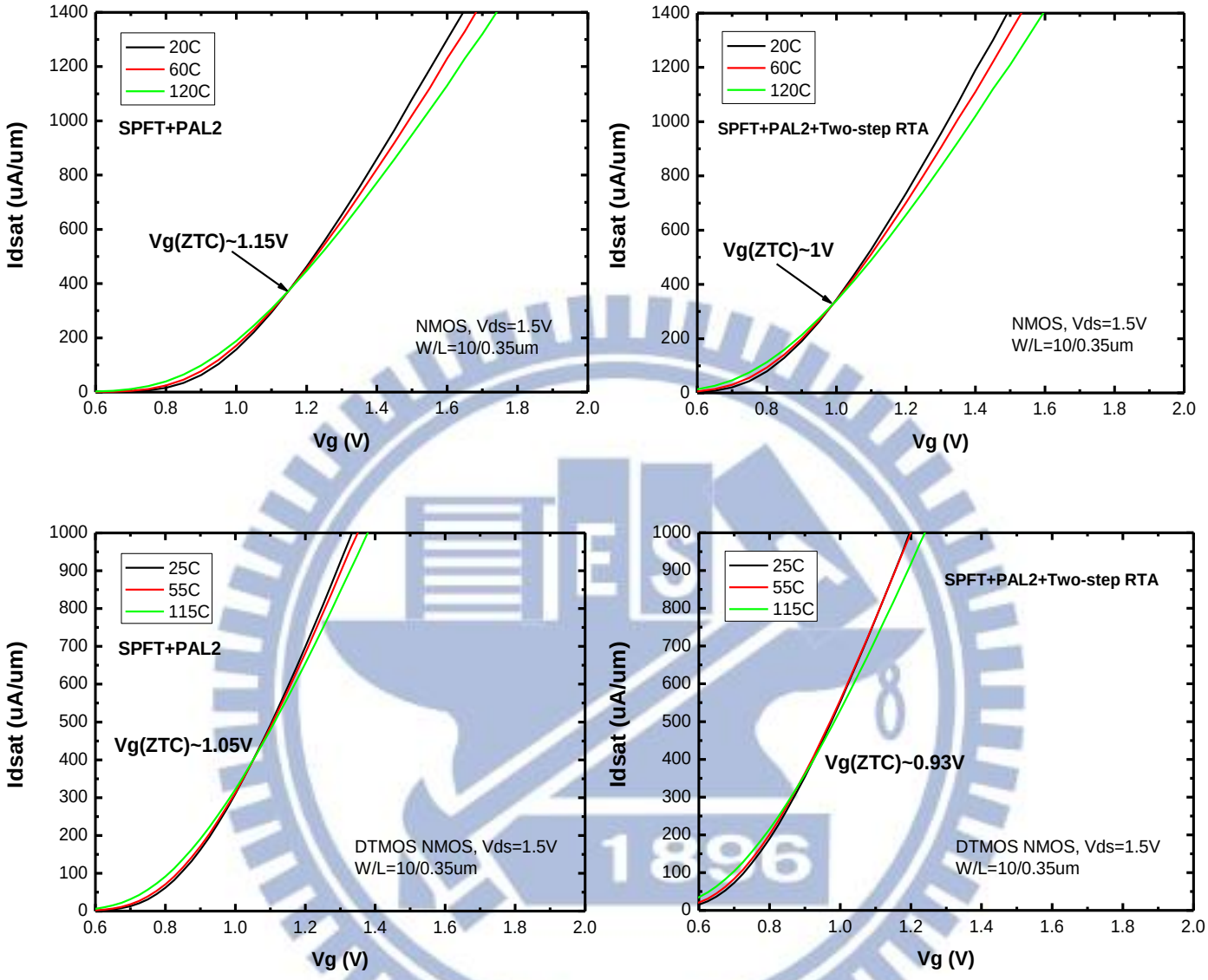


Fig. 5-13 Zero temperature coefficient Vg(ZTC) of DTMOS SPFT and DTMOS SPFT with PAL gate structures

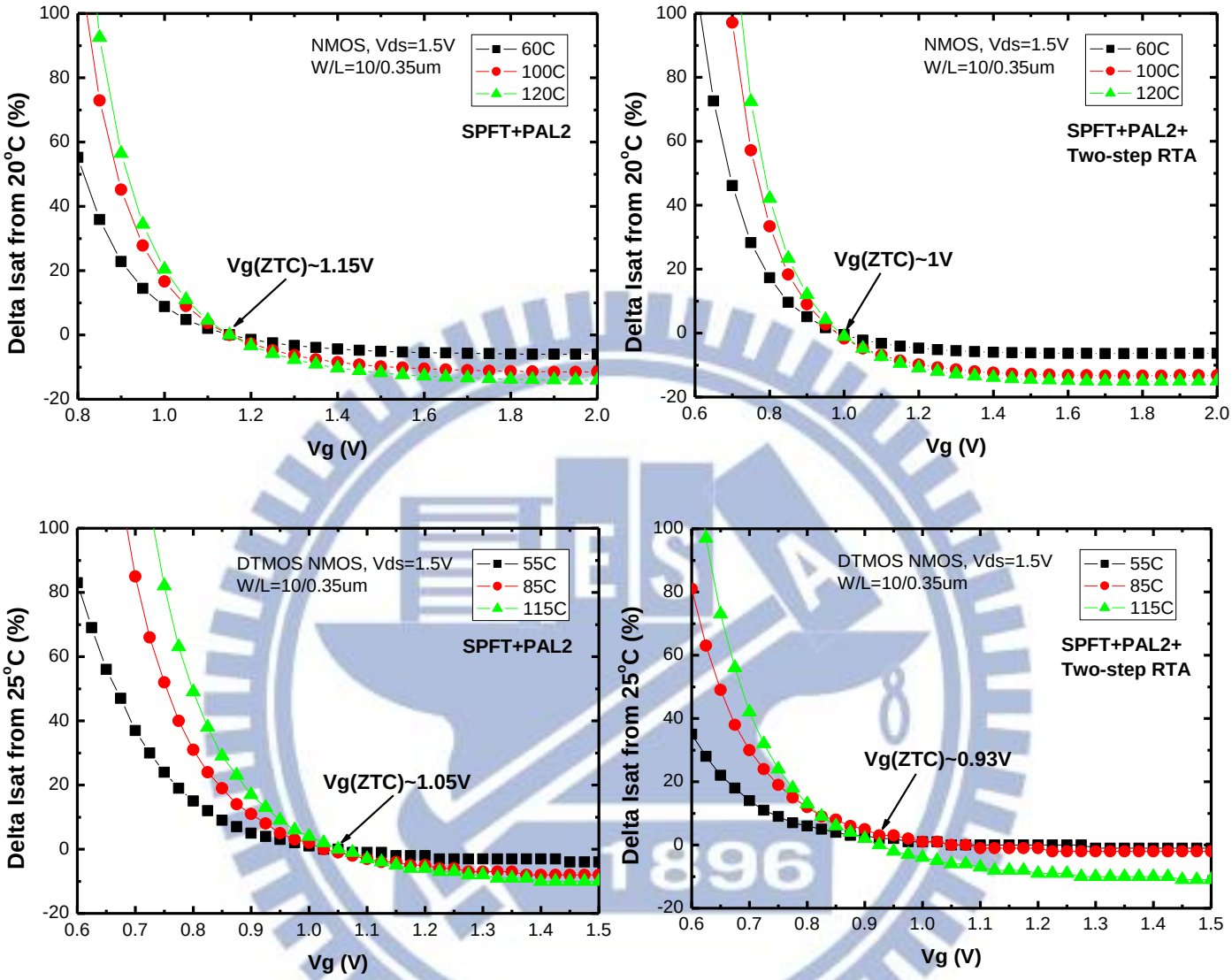


Fig. 5-14 Zero temperature coefficient Vg(ZTC) of DTMOS SPFT and DTMOS SPFT with PAL gate structures

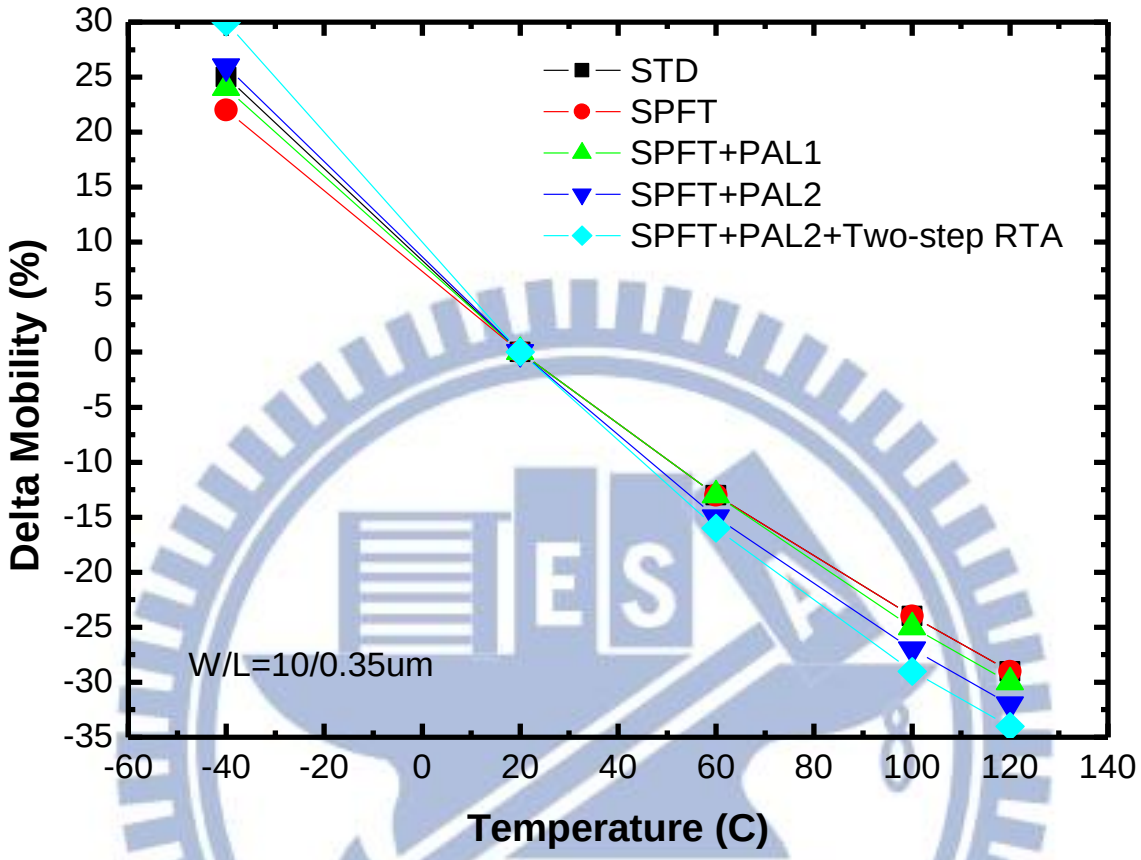


Fig. 5-15 Delta mobility for SPFT and SPFT with PAL gate structures at various temperatures

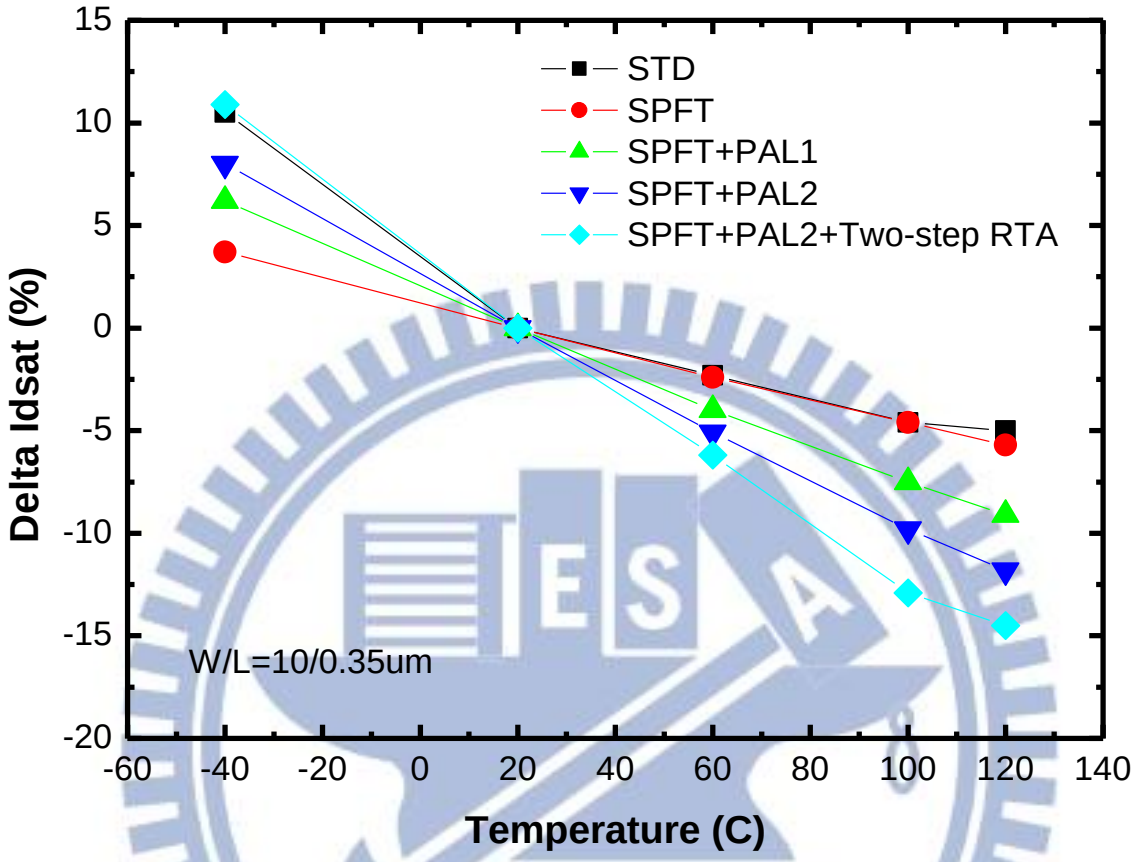


Fig. 5-16 Delta drain current (Idsat) for SPFT and SPFT with PAL gate structures at various temperatures

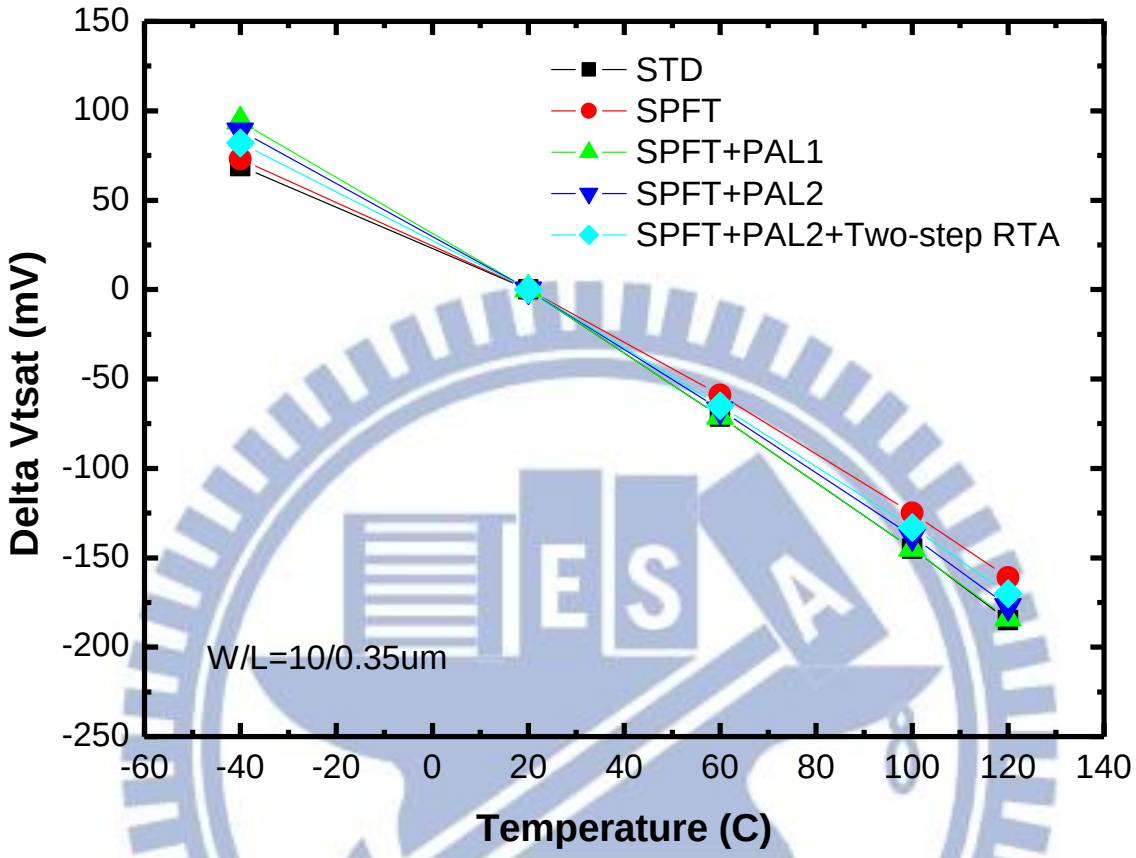


Fig. 5-17 Delta threshold voltage (Vtsat) for SPFT and SPFT with PAL gate structures at various temperatures

Chapter 6. Conclusion and Future Work

We have demonstrated a novel stress memorization technique (SMT) that uses strain proximity free technique (SPFT) to demonstrate mobility improvement through multiple strain-gate engineering. The electron mobility of nMOSFETs with SPFT exhibits a 15% increase over counterpart techniques. Compared with conventional SMT, SPFT avoids the limitation of stressor volume for performance improvement in high density CMOS circuits. We found that optimization of stacked gate structure in combination with SPFT can improve mobility further to 22% more than a single-poly-Si gate structure without SPFT. We also found that the pre-amorphous layer (PAL) gate structure in combination with SPFT can improve mobility further, to 31% greater than standard devices. Moreover, an additional 30% mobility enhancement can be achieved by using dynamic threshold voltage MOS (DTMOS) and combining PAL gate structure with SPFT, respectively. Gate oxide and channel-hot-carrier reliability are also analyzed. Our results show mobility improvement by SPFT, a slightly increased gate leakage current, and degraded channel-hot-carrier reliability. Gate leakage and gate dielectric interface states can be effectively improved by optimizing thermal annealing process in SPFT. Furthermore, we found that the gain in electron mobility in the SPFT in combination with PAL gate structure decreases at high temperatures. Gate dielectric interface states and ionized

gate impurities inducing carrier scattering will play important roles when operating devices under high temperature conditions. Zero temperature coefficient (ZTC) is also discussed for designing CMOS circuit work over an operated temperature. It is found that the Vg(ZTC) is decreased when using SPFT and in combination with PAL gate structure. Strong correlation between Vg(ZTC) and device threshold voltage (Vth) is appears to explain this phenomenon. Moreover, insignificant Vth deviation is found in SPFT and in combination with PAL gate structure at various temperatures. This result is expected to explain the decreased gain in electron mobility for SPFT with PAL gate structure at high temperatures and drain current boost at low temperatures are not attributed by anomalous Vth. Gate dielectric interface traps and channel strain degradation may be the root causes of decreasing gain in electron mobility for SPFT with PAL gate structure under high temperature conditions. Without the limitation of stressor volume in high density CMOS circuits, we believe this scheme that combines SPFT with PAL gate structure and DTMOS will serve as an important guide for continued improvement in future CMOS technology.

In the following work, we would like to go deep into the performance and reliability improvement of nMOSFET by using SPFT and SMT. PAL gate structure is demonstrated electron mobility improvement in SPFT. We will study on implant species and optimize the implant energy, dosage to further enhance stress in the

channel region. Since the strain dependence of mobility improvement often accompanies the gate dielectric and hot carrier reliability degradation. We will focus on thermal annealing process optimization to find out a sweet spot on device performance and reliability.

We would also like to study the novel strain technology on high-k gate dielectric and metal gate device. We believe a high performance nMOSFET with high-k and metal gate structure will be observed by using SPFT. Besides, discussion of high-k gate dielectric device reliability by using the novel strain technology is also an emphasis on my future work.

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