Guest Editorial

I. Background

INTERACTION and merging of the computer, communication, and entertainment industries gave birth to the multimedia era. Multimedia has the potential of becoming one of the most powerful forms of searching for information, communicating ideas, and experiencing new concepts of any form of communication or networking. Many business opportunities are connected through the incredible "Information Superhighway—the Internet." As the deep-submicron microelectronic technologies continue to advance, system algorithms and software tools become more sophisticated. Moreover, as the hardware becomes cheaper to construct, the potential for multimedia systems and machines to be commonly used is tremendous. Therefore, the computer, telecommunication, entertainment, cable, and other consumer electronics industries are racing to this emerging market. Knowledge and results achieved by researchers/engineers in the Circuits and Systems Society of IEEE have been making a significant impact on the development of multimedia machines.

Multimedia is now widespread in our lives. It has changed the way we live, work, entertain, and learn for good. With the connection of the Internet, kids could spend more time on computers using the information superhighway than on watching the TV. Once the power of image, video, and graphics through high-speed fiber optics transmission or wireless communication is enjoyed, no one is interested in returning to the plain text, old-fashioned approach anymore.

The biggest challenge we face is to make multimedia technologies compact, lightweight, cost-effective, and with advanced features for the general public. The price of sophisticated multimedia equipment is still too high for most people, and in many cases beyond the reach of many schools, particularly in rural areas where such equipment is needed the most. However, the future of multimedia looks very bright indeed, and it is expected that multimedia products will eventually become affordable with rapid advances in microelectronic and packaging technologies and with increased efforts in research and development. With the ability of the consumer electronics industry to mass-produce sophisticated electronic equipment, the price of multimedia systems will become cheaper for both schools and the home in the future.

Significant advances in hardware and software codesign technologies have occurred over the past ten years. The microprocessing power has been increased from 10 million to 1200 million instructions per second (MIPS). Continued progress toward more than 10 billion instructions per second can be available in early twenty-first century. With the new packaging technologies, tens of millions of transistors can be compactly integrated for very low-power operation in advanced multimedia applications. Recent advances in micromachining and nano-structure technologies will be integrated into fabrication technologies for multimedia products.

Video technology has made explosive progress during the past ten years. Various image and video coding standards for still image compression (JPEG), video conferencing (CCITT H.261 and H.263) and motion video for storage media applications (MPEG-1/2) have been established, and many more [such as MPEG-4 and digital high-definition television (HDTV)] are under intensive development. Significant progresses in use of wavelet transform to realize high compression ratios and fast search in digital library have been made. It is widely recognized that a new era of global visual communication has arrived. Standards will always play a major role in multimedia applications. According to a recent projection, multimedia will represent a new total market of $40 billion by the year 2000 and $65 billion by the year 2010. The National Science Foundation has recognized the importance of multimedia. In 1996, one of the four new Engineering Research Centers was devoted to this fast-growing field and awarded to the Integrated Media Systems Center (IMSC) at University of Southern California in Los Angeles.

II. About the Special Issue

The Tutorial Program of ISCAS-95 in Seattle, WA, was dedicated to multimedia. The companion tutorial book published by IEEE Press in May 1995 was entitled *Microsystems Technology for Multimedia Applications* co-edited by B. Sheu, M. Ismail, E. Sánchez-Sinencio, and T. Wu. In order to further promote multimedia research and applications activities within the Circuits and Systems Society, a three-step approach is taken. As the first step, the Multimedia Systems and Applications Technical Committee (MSATC) was established in 1996 with 20-plus founding members. Founding Chair and Secretary are B. Sheu and C.-S. Li, respectively. A special session and a tutorial session were organized for ISCAS-97 in Hong Kong in June 1997. In the ISCAS-98 to be held in Monterey, CA, multimedia has become an independent technical track for the Symposium.

Publication of this Special Issue marks the important second step of the effort. The third step will be to have a journal publication devoted to the multimedia field. A possible arrangement is to start a new IEEE Transactions on Multimedia Technology, or any other suitable title.

The purpose of this special issue is to report on some recent advances in circuits and systems development for multimedia systems and applications. Topics of interest for this special issue include, but are not limited to:

- new standards, system trends;
- speech/audio signal processing, synchronization of multimedia signals;
- source modeling, characterization;

Publisher Item Identifier S 1051-8215(97)05897-7.

- video processing, compression, high-definition TV's;
- wireless communication, ATM, multimedia networking, mobile computing;
- digital library, servers for data storage and information retrieval;
- low-power circuits, architectures, system operation;
- VLSI implementations, portable devices, and equipment;
- multimedia man–machine interface with recognition technology;
- software/hardware partitioning and CAD development tools;
- three-dimensional graphics, virtual and augmented reality;
- worldwide web-based applications;
- multimedia testbeds and multimedia systems and technology.

Over 36 manuscripts were submitted for consideration, and 17 full papers and four brief papers are included. Due to global planning consideration, papers for this Special Issue are to appear in the August and October issues. In the August issue, papers in the areas of CMOS technology, intelligent processing, communication and networking, and four brief papers are included. In the October publication, papers in the areas of efficient coding and multimedia systems are included. The full papers are arranged according to technical areas of CMOS technology, intelligent processing, communication and networking, efficient coding, and multimedia systems. Three papers belong to the *CMOS technology* area. Kemeny *et al.* describe architecture, design, and test results of the innovative active pixel sensor imager with multiresolution capability. This new CMOS imager sensor is superior to the charge-coupled device (CCD) sensors in terms of cost, power consumption, and integration level. Many semiconductor companies in the United States, Japan, Europe, and Taiwan are racing for CMOS imagers into camera products. Hung *et al.* describe architecture, design, and test results of a low-power CMOS elliptic GM-C filter for baseband wireless communication. An enhanced low-voltage rail-to-rail operational transconductance amplifier is used to perform voltage-to-current conversion. The filter operates at 3-V supply and consumes 2.48 mW. Hsieh *et al.* describe in detail various readout techniques for CMOS focal-plane-array devices. The properties of infrared detector structures are carefully presented. Circuits of working designs and packaging technologies are also addressed.

The next three papers focus on *intelligent processing* of image and video data. Kozek *et al.* describe new results in object-oriented dynamic images using the cellular neural network architecture. Measurement results from prototype chips are included. Comparison among TMS320C80 chip from Texas Instruments Inc., the multiprocessor chip from CNAPS Inc., and the proposed CNN universal chip is given. Wang and Chang describe a new method for face region recognition on MPEG video sequences. The inverse-quantized discrete cosine transform (DCT) coefficients are used as inputs, and the generated results are the locations of the detected face regions. The success rate is around 85–92% from three test sets. Izquierdo describes a stereo matching method for use in 3-D video communication. A modified block matching algorithm is used with careful selection of cost function. A confidence measure is introduced to ensure reliability of the results.

Four papers belong to the *networking area*. Rabiner and Chandrakasan describe an efficient motion estimation method for use in wireless video terminals. The method is based on prediction of object motion. The proposed approach reduces the number of operations by over two orders of magnitude. Chen *et al.* present the algorithm and architecture of a neural network-based code division multiple access (CDMA) detector that achieves high performance in near–far resistance. Mellaney *et al.* report results from the study of MPEG-2 video traffic over LAN/ATM network. Experimental video-on-demand testbeds are used for both unloaded and heavily-loaded conditions. Tsai *et al.* describe a multicasting solution for ATM video applications. The architecture and detailed operation of the proposed method are presented in detail. The hardware design is based on a 0.8-μm CMOS technology.

The next three papers, in the October issue, focus on *efficient coding* of video data. Wang *et al.* describe a scalable coding method for high-resolution video in HDTV or super-HDTV applications. The virtual zero-tree approach is used. Wavelet transform and hierarchical motion compensation help to achieve high-quality results. Idris *et al.* describe an indexing technique for compressed video. The vector quantization method is used to achieve the desired results. The operations are executed in the compressed domain. Cheng *et al.* describe results on mapping of block matching algorithms to systolic arrays. Three evaluation criteria are used: silicon area, input/output requirement, and image quality. A more interesting item will be comparison with execution of block matching algorithms on a new generation of microprocessors with multimedia extension. However, that is not emphasized.

Four papers, also in October, address issues of importance to *system-level design* of multimedia. Chang *et al.* address issues related to storage and real-time retrieval of video data. Both single-disk and multiple-disk approaches are considered. Detailed simulation results from a four-disk system are presented. Yeung and Yeo describe a video visualization method for analyzing video and the subsequent derivation of representative visual presentation. A video sequence is condensed into a few images! The proposed method is suitable for video browsing, query, search, and retrieval in digital libraries and over the Internet. Lavagetto describes a method for estimating lip movements from speech analysis. The results are very useful in audio–visual synchronization in title authoring. A time-delay neural network is use to perform the estimation. Ohm and Lavagetto describe an object-based system for stereoscopic viewpoint synthesis. The results can be used in teleconferencing. The proposed method identifies the foreground and background regions and then applies disparity estimation to the foreground objects.

Four brief papers highlight new results for *multimedia applications*. Akramullah *et al.* present a performance study of a software-based MPEG-2 video encoder on parallel and distributed computer systems. Significant simulation results are included. Cheng *et al.* describe a new rate control method for an embedded wavelet-based video coder. A bit allocation approach is used. Natarajan *et al.* describe the algorithm

and architecture for block-based motion estimation. The 1-bit transformation method is used. Tsai *et al.* present recent advances in efficient optical links to speed up interprocessor communication. Significant results are included.

ACKNOWLEDGMENT

The Guest Editors would like to thank the many people who made this Special Issue possible. Prof. R.-W. Liu, CAS President in 1995, and Prof. M. Liou, Chair of the T-CSVT Steering Committee, strongly encouraged the three-step promotion approach for multimedia activities in the Society. Prof. M.-T. Sun, the Editor-in-Chief, provided valuable support and advice on editorial matters. Prof. Y.-F. Huang, 1997 CAS VP-Publications, Prof. R. J. P. de Figuieredo, 1996 CAS VP-Publications, and Prof. J. Choma, 1997 CAS President, all provided strong support and encouragement for the completion of the Special Issue. Dr. Sheu is grateful for the assistance from graduate students: W. Young, C.-T. Chang, and A. Chu.

Further thanks are expressed for the many reviewers, the staff at the IEEE Headquarters, and the authors for their efforts and cooperation to make timely publication of this Special Issue possible. More multimedia-oriented papers are to be published in the regular issues of this Publication in the future.

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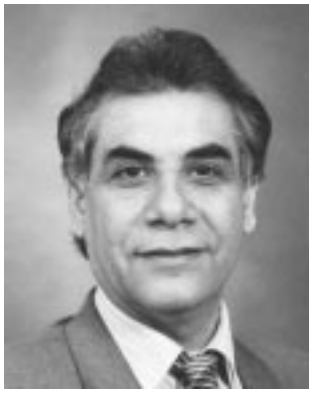
In 1985, he joined the faculty of the Electrical Engineering Department at the University of Southern California, Los Angeles, and is currently an Associate Professor with joint appointment in the Biomedical Engineering Department. He serves as Chair of Colloquium Series and Publications in IMSC, which is an NSF/Engineering Research Center. He serves as the Director of the VLSI and Signal Processing Laboratory. His research interests include VLSI chips and systems, massively paralleled neural networks and image processing, and high-speed computing and multimedia. He is an Honorary Consultant in National Taiwan University and National Chiao Tung University, in Taiwan.

At the National Taiwan University, Dr. Sheu was the recipient of the Distinguished Book-Coupon Award seven times. He was the recipient of the 1987 NSF Engineering Initiation Award, as well as the recipient of the Best Presenter Award at the IEEE International Conference on Computer Design in 1990 and 1991. He is a recipient of the Best Paper Award of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS in 1995; the Best Poster Paper Award of the World Congress on Neural Networks from the International Neural Network Society in 1995; the NASA Certificate of Recognition in 1995 and 1996; and a recipient of Guillemin Cauer Award from the IEEE Circuits and Systems Society in 1997. He served on the Technical Program Committees of IEEE ISCAS, ICASSP, IJCNN, ICCD, and CICC. He served as a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS for March 1992 and 1993 Special Issues; a Guest Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS for June 1993 Special Issue; an Associate Editor of IEEE TRANSACTIONS ON NEURAL NETWORKS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I (Express Letters) and Part II (VLSI DSP), and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS. At present, he serves as Editor-in-Chief of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS; and CAS Editor of the IEEE CIRCUITS AND DEVICES MAGAZINE. He served as the Tutorials Chair of the 1995 IEEE International Symposium on Circuits and Systems; the Technical Program Chair of the 1996 IEEE International Conference on Neural Networks, the 1997 IEEE International Conference on Computer Design, and the 1997 International Conference on Next Decades of High Technologies. He was among the key contributors of the widely used BSIM model in the SPICE circuit simulator. He is a member of International Neural Networks Society, Eta Kappa Nu, and Phi Tau Phi. He also serves as Editor of the Multimedia Book Series by IMSC Press of Prentice-Hall Inc.



Mohammed Ghanbari (M'78–SM'97) received the B.Sc. degree in electrical engineering from Aryamehr University of Technology, Tehran, Iran, in 1970, the M.Sc. degree in telecommunications, and the Ph.D. degree in electronics engineering, both from the University of Essex, England, in 1976 and 1979, respectively.

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Dr. Ghanbari is the co-recipient of the 1995 A. H. Reeves Premium Prize for the year's best paper published in the *IEE Proceedings* on the theme of digital coding. He has been a member of the organizing committee of several international workshops and conferences. He is the current Chairman of the Steering Committee of the 1997 International Workshop on Audio Visual Services over Packet Networks, AVSPN'97.

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He was a technical officer responsible for communication electronics R&D from 1984 to 1986 in Taiwan. Between 1989 and 1990, he researched signal processing ASIC and optical networking at IBM Almaden Research Center and IBM T. J. Watson Research Center. He worked at Teknekron Communications Systems, Inc., Berkeley, CA, as the principle architect of a JPEG chip from 1990 to 1991. He then joined the AT&T Bell Labs in 1991 and transformed his BLSI system research successfully into various video codec and network IC products. In 1996, he joined NEC America Inc., San Jose, CA, led LAN switching VLSI development, and defined network storage products which helped to create the spin-off HolonTech Corp., where he was a Co-Founder and Director of LAN IC Engineering. In 1997, he joined NeoParadigm Labs Inc., San Jose, CA, heading application-specific standard IC product development for both multimedia and networking communications. He has published extensively and holds patents in the area of image/video coding, channel coding, ATM, application-specific memory, and low-voltage IC.

Dr. Lin was elected a member of the Phi Tau Phi scholastic honor society in 1984. He is an Associate Editor for the IEEE CIRCUITS AND DEVICES MAGAZINE and a founding member of the multimedia systems and applications technical committee of the IEEE Circuits and Systems Society.

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Dr. Wu was awarded the Outstanding Research Awards by the National Science Council in 1989 and 1995 and the Outstanding Engineering Professor by the Chinese Engineer Association in 1996. He is a member of Eta Kappa Nu and Phi Tau Phi.