利用双節制技術之功率意識乘法器設計

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摘　　要

功率意識(Power awareness)是近幾年來新興的研究領域,它可以衡量能量與品質之間交換。舉例來說，我們考慮數位相機的使用。在某個時候使用者可能想要較好的影像品質，如此就需要降低電池的壽命。在另一個時候，使用者可能想要降低影像品質以便延長電池的壽命。當系統設計成功率意識時便可以將這樣的交換最佳化。在本篇論文中，我們設計一個用於數位訊號處理(DSP)應用，功率意識管線(pipelined)正負號(signed)乘法器。這個乘法器有 16 bit 被乘數、16 bit 乘數、以及 16 bit 乘積。我們使用 Dadda 方法與 Brent-Kung 進位-向前看加法器，並且插入 6-stage 管線暫存器來產生快速乘法器。在功率意識方面，我們提出一個双節制(double truncated)技術：即同時節制乘積與輸入(包括被乘數及乘數)。本論文是用 VHDL 設計，以 Synopsys 公司的 Design Analyzer 作合成,Prime Power 做為估計 power 的工具，我們以訊號-雜音比(Signal-Noise Ratio, SNR)來代表品質，並且使用 Battery Design Player 模擬 battery lifetime。根據損失品質的功率意識指標做法，我們選擇輸入設為零與乘積保留前值(IZ-PD)的双節制方法及其 4 種操作模式，來產生功率意識最佳化的乘法器。功率意識乘法器比未做功率意識乘法器增加了 37%的 battery lifetime，衰減 14 dB 的 SNR，並且只需增加 3%的面積。另外，其 clock 頻率為 156.25 MHz，可達到高速乘法器的要求。

Design on Power-aware Pipelined Multiplier Using Double Truncating Technique

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ABSTRACT

“Power awareness” is a new research in recent years. It is able to scale power and quality tradeoff. For example, consider the user of a digital camera. At times, the users might want high image quality at the cost of reduced battery lifetime. At other times, the user might want low image quality in return for extending battery lifetime. Such tradeoffs can only be optimal if the system was designed in power-aware manner. In this paper, we design a power-aware pipelined signed multiplier for DSP application. This multiplier has 16 bits multiplicand , 16 bits multiplier , and 16 bits product . We use the Dadda scheme and Brent-Kung carry look-ahead adder to present a fast multiplier implemented as a 6-stage pipeline register. We make double truncating technique to truncate both product and input (including multiplicand and multiplier) for power awareness. The design is written by VHDL and synthesized by Synopsys Design Analyzer. Power is estimated using Prime Power. We use Signal-Noise Ratio (SNR) to represent quality, and estimate battery lifetime by Battery Design Player. By the definition of lossy power awareness , we choose truncating way of Inputs remained Zero and Products remained Data(IZ-PD) and select 4 operation mode to propose optimal power-aware multiplier. The power-aware multiplier increased 37% battery lifetime to unpower-aware multiplier while lost 14 dB SNR and increased 3% area. Besides, the clock frequency achieved 156.25 MHz to be high speed multiplier.