國 立 交 通 大 學

電子工程學系　電子研究所

博 士 論 文

對於利用氮化矽局部電荷儲存之快閃記憶元件可靠度問題的探討

Investigation of Reliability Issues in a Nitride-Based Localized Charge Storage Flash Memory Cell

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摘要

在本論文中，我們針對以氮化矽(Si_3N_4)局部電荷儲存(localized charge storage)原理為快閃記憶元件之可靠度問題作了深入的研究。雖然此元件利用介電層缺陷(trap)為電荷儲存媒介以及以一較厚的穿隧氧化層(tunnel oxide)來提昇其電荷保存能力，我們仍觀察到該能力在元件經過重複的資料寫入／抹除(program/erase)操作後大為衰退。研究後發現在寫入／抹除過程中，於穿隧氧化層所產生的缺陷扮演了關鍵的角色。對一處於寫入狀態(program state)的記憶細胞而言，其臨界電壓(threshold voltage)的下降肇因於其儲存於氮化矽缺陷中的電子經由Frenkel-Poole放射機制到達氮化矽導帶，並藉由穿隧氧化層缺陷而逃逸。此外，部分的介面缺陷(interface state)在高溫烘烤測試後會逸失，此效應亦為臨界電壓下降的原因。對一處於抹除狀態(erase state)的記憶細胞而言，其臨界電壓卻隨著時間而漸增。這是由於穿隧氧化層中存有正電荷。這些正電荷隨時間逐漸脫離穿隧氧化層而導致所儲存的淨負電荷增加，並形成臨界電壓的正漂移。此外，當讀取儲存資料時，記憶細胞的閘極及汲極將被施予高偏壓。這些正電荷能增強通道電子或通道熱電子穿隧進入氮化矽層的機率而引發讀取擾動(read disturb)。我們亦發現，寫入及抹除操作後所引發的介面缺陷以及暫態基底電流(transient substrate current)的增量是該元件資料保存能力的良好指標。上述現象皆與電荷沿垂直於閘極介電層方向運動有關。但對於一過度抹除之記憶細胞而言，儲存的過剩正電荷易沿著氮化矽層橫向移動。此機制將導致通道短縮效應而使該記憶細胞之臨界電壓隨時間而下降。最後我們亦探討抹除速度退化的原因。我們發現在一近乎穿擊導通(punch-through)的記憶細胞中，鄰接接面的偏壓會調變熱電洞注入效率，抹除速度因而改變。此外當儲存電子愈靠近通道中央時愈難抹除。這些遠端電子較易產生於一個鄰接位元已為寫入狀態的記憶細胞中，特別是一個經過多次寫入／抹除操作後的記憶細胞。

Investigation of Reliability Issues in a Nitride-Based Localized Charge Storage Flash Memory Cell

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Abstract

Reliability issues in a trapping nitride, localized charge storage flash memory cell are comprehensively investigated in this dissertation. Though the use of a thick bottom oxide and trapping storage concept provides excellent intrinsic charge retention, data loss is found after program/erase (P/E) cycling. Our study shows that trap generation in the bottom oxide during P/E cycling plays a central role. V_t loss in a program-state cell is due to the escape of trapped electrons in the nitride via Frenkel-Poole emission and subsequent oxide trap-assisted tunneling. Interface state annihilation during high-temperature baking would be another source of the observed V_t loss. V_t drift-up in an erase-state cell is the outcome of the tunnel detrapping of cycling-induced positive oxide charges. Furthermore, these positive oxide charges could enhance channel electron tunnel injection and channel-hot-electron injection into the nitride during read operation and thus cause read disturb. Stress-induced interface state growth and transient substrate current are good indicators of cellís retentivity. All the above regard the charge transport along the vertical direction. On the other hand, lateral migration of excess holes in the trapping nitride dominates the V_t loss in an over-erased cell. Finally, erase speed degradation is studied. It is found that neighboring junction bias would suppress the hot-hole injection efficiency in a nearly punch-through cell. Besides, a cell is hard-to-erase if more electrons reside in the central channel region. Those far electrons are prone to be injected as its neighboring bit is programmed or after P/E cycling.

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在論文的研究上必須感謝許多曾經一起參與研究的同仁。尤其是鄒年凱及葉致鍇在實驗執行上的大力協助和研究建議，以及陳旻政、古紹泓及詹前泰在交大實驗室內的相關工作所提供的數據、經驗及意見。感謝張耀文在我修課期間對我工作上的大力協助。我也要對旺宏電子的盧志遠副總、古延輝協理以及現任職於台積電的潘正聖前協理表達最深的謝意，沒有他們的支持與鼓勵我將難以兼顧工作與課業。而郭治群及王明宗在我職涯初期的信任與提攜更是我能追求更高學術成就的重要推手。

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僅將此論文致予我的太太敏秀。她伴隨著我經歷這一段青春歲月，由朋友而情人而伴侶，讓我們除了此論文外也有了個可愛的女兒，孟伶。

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First of all, I would like to express my deepest gratitude to my advisor Prof. Tahui Wang. He guided me as early as I was pursuing my Master degree. His solid theoretical background, brilliant insight into the research topic, focused and conscientious attitudes on his work affect me a lot. Those help to develop my independent researching capability and to approach each issue in an innovative way. His continual contribution in the frontier territory, growing and open mind mold the scholarly model for we young researchers. His patience and encouragement help me to finish this dissertation in such a beautiful manner.

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At last, I would like to present this work to my wife, Michelle. She went through all the youthhood by my side, as a friend, a love and my mate. In addition to this dissertation, she also helped to deliver a lovely little girl, our daughter, Morning.

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Chapter 1

Introduction

1.1 An Overview

In the past decade, Flash memory market has been driven by cellular phone and other types of electronic portable equipment (MP3 audio player, digital camera, and so on). It would further explosively grow in mass storage applications such as memory card and removable storage (e.g. USB Flash driver). It reached a worldwide revenue of 12.4 billions in 2003 and is predicted to be 17.3 billions in 2004 [1.1].

Flash memory cell was firstly invented in 1984 [1.2]. It was realized by a 2μm triple poly-silicon technology with a cell size of 64μm^2 to compose of a 256Kb chip [1.3]. It is based on the same concept of a floating-gate EPROM [1.4]. However, the erase is performed on a block of cells (or a whole chip) at the same time via electrical method. Such ìflash eraseî much increases the erase speed and thus earn the name after that. Excellent data retention is the most extinguishing feature of the ìnonvolatileî memory (NVM) (e.g. Mask ROM, PROM, EPROM, EEPROM) against the ìvolatileî one (e.g. SRAM, DRAM). It means that, for example, the stored data can be retained more than 10 years even the ambient temperature is as high as 85C and the power supply is removed [1.5].

From the device structure point of view, floating-gate based [1.4] and SONOS-type cells [1.6] (evolved from the MNOS cells [1.7]) are the most matured which use floating poly-silicon and trapping nitride, respectively, as the charge storage media above the conduction channel of a MOSFET to modulate the memory cellís V_t. One of the advantages of the charge trapping-storage cells over the floating-gate cells is their better resistance to charge loss via defects (oxide traps, pin holes) in the surrounding oxide [1.8]. Regarding the operating principles, hot-carrier injections [1.9-1.17] and Fowler-Nordheim (FN) tunnel injection [1.18-1.19] are used for both program and erase. Program to high-V_t state [1.2] and to low-V_t state [1.20] are also proposed.

There are two major categories of Flash memory product. For ìcodeî application, it is mostly composed of NOR-type arrays to have high random access speed. It advances from a 256Kb chip based on 1.5μm technology (cell size of 36μm^2) in 1988

[1.21] to a cell size of 0.049μm^2 based on 70nm technology in 2004 [1.22]. For ìdata storageî application, it uses NAND-type arrays to have higher program/erase throughput and the smallest cell size. It advances from a cell size of 6.43μm^2 based on 1μm technology in 1987 [1.23] to a 8Gb chip based on 63nm multi-level-cell technology (cell size of 0.0164μm^2) in 2004 [1.24]. In all cases, low voltage/power operation, small cell size, high program/erase/read speed, good endurance and retention are the dream targets for any kinds of Flash memory.

Floating-gate based cell is the mainstream technology till now. To meet the needs of high density and low cost, Flash product doubles its density as the technology node evolves to next generation [1.25]. The other density-increasing approach is by multi-level-cell (MLC) concept [1.26]. It means that, for example, 2 bits can be stored in a single memory cell. In this way, ìelectricalî memory density can be doubled based on exactly the same ìphysicalî cell and process technology. Still another way to increase the memory density is by storing bit information at physically different sites in a ìsingleî memory cell. This concept has been applied to both floating-gate based [1.27] and trapping-storage based cells [1.28]. It can also have electrical multi-level in each sites to obtain 4-bit (or more) per cell [1.29].

1.2 Brief of the Trapping-Nitride Localized-Charge Storage Cell

Except for the higher packing density, localized charge trapping-storage cells (NROM [1.28], NBit [1.30], PHINES [1.31], *micro*Flash [1.32], MirrorBit [1.28], TwinFlash [1.34]), which use hot-carrier injections for both programming and erasing, are more immune to charge loss since they have a sufficiently thick bottom oxide (>5nm) to avoid charge direct back tunneling [1.35], as comparing to conventional SONOS cells using uniform charge storage and FN-/modified-FN-tunnel injection/ejection of charge carriers through a much thinner tunnel oxide (~2nm) during programming/erasing. Furthermore, less process complex and absence of floating-gate coupling issue are also the advantages over the floating-gate cells [1.36]. In this way, trapping-nitride based, localized charge-storage Flash memory cell rivals recently and is considered to be a promising candidate of the high density Flash products [1.37-1.38].

Letís take a closer look at such a cell now. Fig.1.1 shows a typical NBit cell [1.30] (From now on, the memory cell discussed in this dissertation is named as the NBit

cell). It is made of an n-channel MOSFET with an oxide-nitride-oxide (ONO) gate structure. The charges are stored locally in the nitride layer above the channel region nearby the n^+ source/drain junctions. Since the nitride is a dielectric film, the charge is immobile inside it. Long-term localized charge storage is thus workable.

Once charges are stored locally in it, a reverse-read scheme is applied to sense the bit state [1.28]. It means that to read out the information stored in Bit-S (Bit-D), V_d (V_s) is biased at 1.8V and V_s (V_d) is grounded (Fig.1.2). The applied V_d must be large enough to ìscreenî out the injected charge effect at the drain side (Bit-D). The read current (or threshold voltage) is then controlled by the stored charges at the source side (Bit-S), almost regardless of the charges at Bit-D. Fig.1.3 show the junction bias effect on the sensed V_t. Assuming Bit-S and Bit-D store a low-V_t state and a high-V_t state, respectively (as shown in Fig.1.2). If the applied V_d is small (e.g. V_d=0.1V), Bit-S would be incorrectly read as a high-V_t bit. However, if V_d is high enough (e.g. V_d=1.5V), Bit-S can be correctly sensed as a low-V_t bit. Even so, the operating-V_t window, which means the V_t difference between the high-V_t state and the low-V_t state, is limited in such read scheme. Assuming there is no charges stored at Bit-S, and there are electrons stored at Bit-D (Fig.1.4 (a)). The sensed V_t of Bit-S, which is equal to the applied V_g that conducts a channel current of 1μA, is defined to be $V_{t\text{-}REV}$ and $V_{t\text{-}FWD}$ by applied 1.8V at drain side and at source side, respectively. Fig.1.4 (b) shows the $\Delta V_{t\text{-}FWD}$ v.s. $\Delta V_{t\text{-}REV}$ plot in which each point represents various amounts of electrons stored at Bit-D. If there are only few electrons distributed within the drain depletion region, the sensed $\Delta V_{t\text{-}REV}$ is close to 0V as expected while the $\Delta V_{t\text{-}FWD}$ is proportional to the stored electron density at Bit-D. If there are more and more electrons stored at Bit-D, electron distribution would be wider and is beyond the drain depletion region at V_d=1.8V. $\Delta V_{t\text{-}REV}$ would increase with $\Delta V_{t\text{-}FWD}$, which is proportional to the stored electron density, with a slope of 1 on the $\Delta V_{t\text{-}REV}$ v.s. $\Delta V_{t\text{-}FWD}$ plot. This is known as the 2^{nd}-bit effect (Bit-D here) in the NBit technology [1.39]. The operating-V_t window which is equal to $|\Delta V_{t\text{-}REV}-\Delta V_{t\text{-}FWD}|$ is then saturated at 2V.

The last subject to realize 2-bit-per-cell is how to inject the charges locally into the trapping nitride. Channel-hot-electron (CHE) injection and band-to-band-tunneling (BTBT) induced hot-hole (HH) injection [1.28] are utilized for programming and erasing, respectively (Table 1.1). Carriers are heated by local electric field and then inject toward the gate nearby the junction and then are trapped

in the nitride. Since they are based on hot-carrier injection processes, the bottom oxide of this cell can be thicker to avoid charge direct back tunneling. Its intrinsic data retention is thus better than a conventional SONOS cell which using FN (or modified-FN) injection through a much thinner tunnel oxide. Fig.1.5 and Fig.1.6 show the program and erase characteristics, respectively, of this NBit cell. Two bits can be programmed independently and erase ìsimultaneouslyî (since they belong to the same ìsectorî).

Finally, the cell shows good intrinsic data retention before program/erase (P/E) cycles (Fig.1.7), and it is also demonstrated to be endurable more than 100K cycles (Fig.1.8). However, we find that data retention degrades as the cells undergo extensive P/E cycles. Fig.1.9 show the V_t evolution with the storage time of a 10K P/E cycled cell. The ambient temperature is only at 25C. It is found that the program-state V_t drops down and the erase-state V_t drifts up with retention time. As these two states approaches to each other, it may result in a wrong data sensing. We use Fig.1.10 to illustrate the reliability issues we have observed in this cell. They are cycling-induced high-state V_t loss, low-state V_t drift-up and drop-down, read disturb, and erase speed degradation.

1.3 Organization of This Dissertation

We will address each issue in this dissertation, which is thus organized in the following manner. An overview of the Flash memory cell technologies and the concepts of a trapping-nitride localized-charge storage cell (the NBit cell here) and its reliability issues have been presented here. We will discuss the mechanisms that dominate the charge loss in chapter 2. In chapter 3, the charge gain behavior is addressed. V_t drop-down in an over-erased cell is characterized in chapter 4. Various read disturb modes are modeled in chapter 5. We will disclose the causes of erase speed degradation in chapter 6. Conclusions follow in chapter 7.

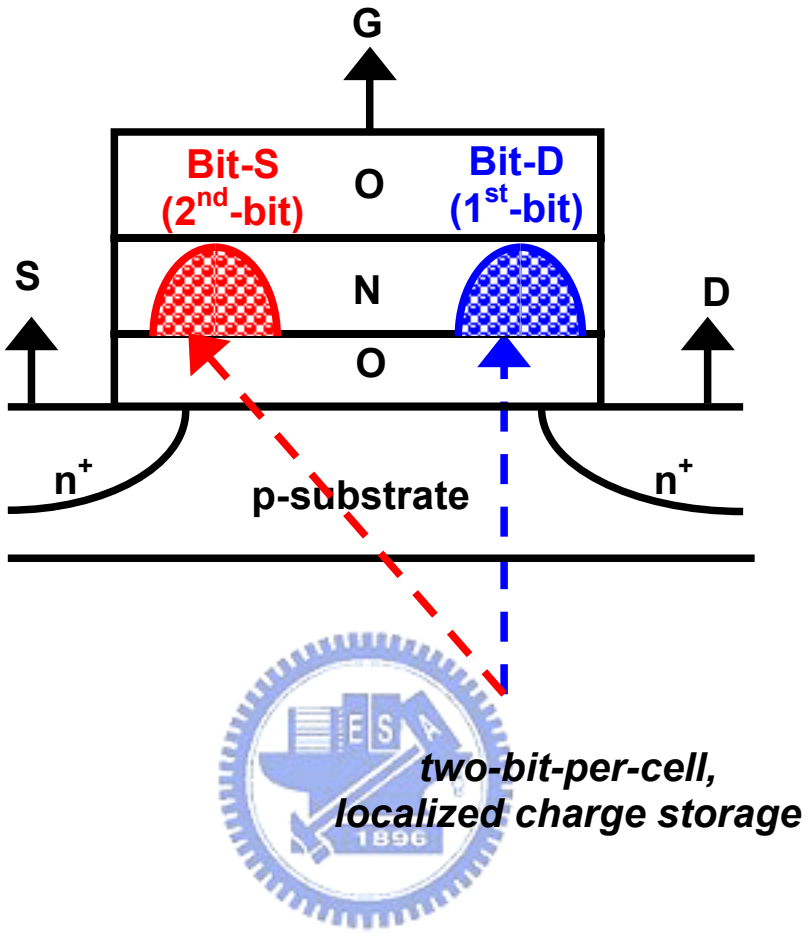


Fig.1.1 Schematic representation of an NBit cell.

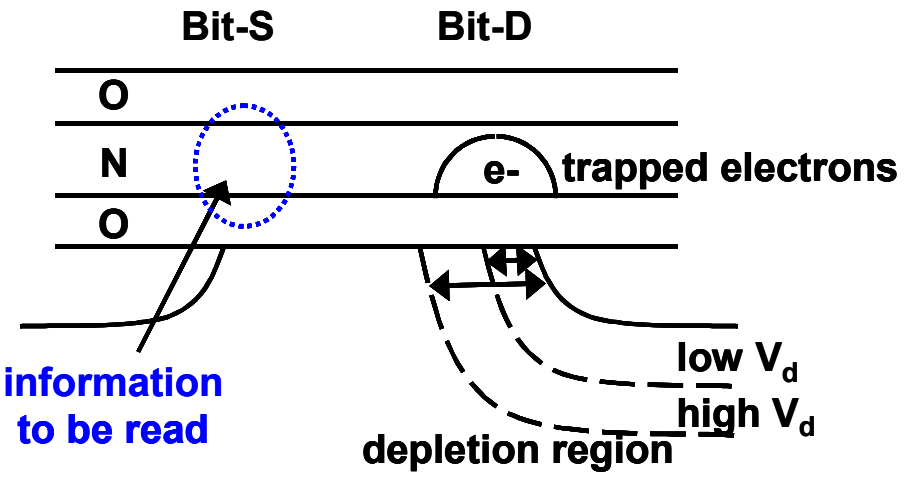


Fig.1.2 Concept of reverse read is depicted by the drain depletion region in which the effect of injected charges is screened out.

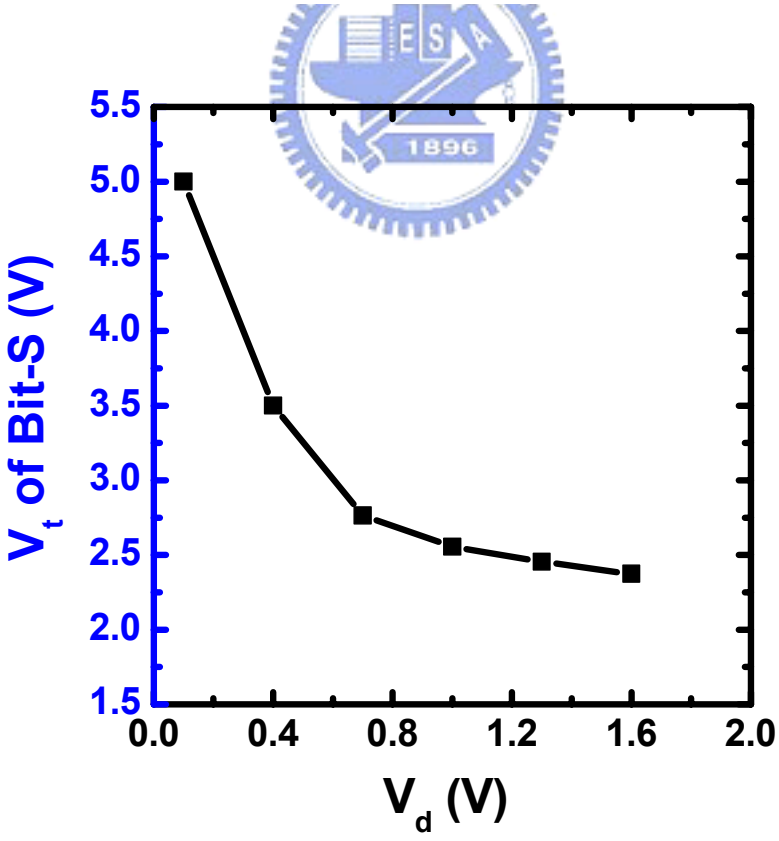
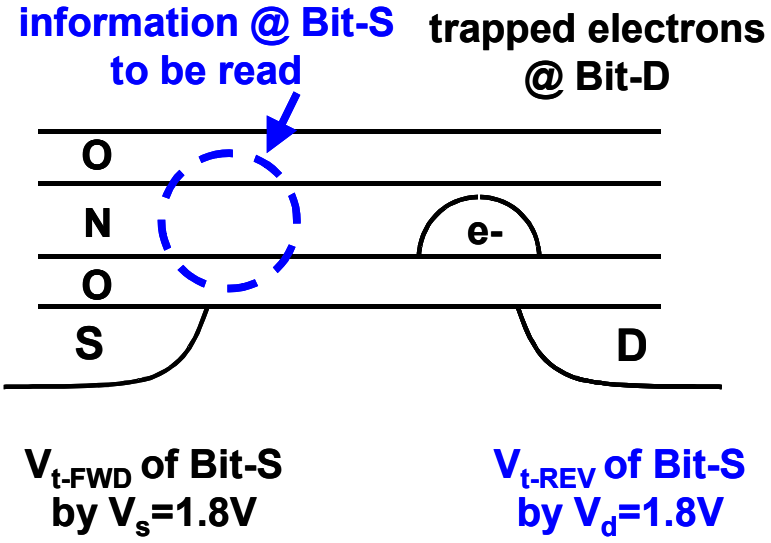
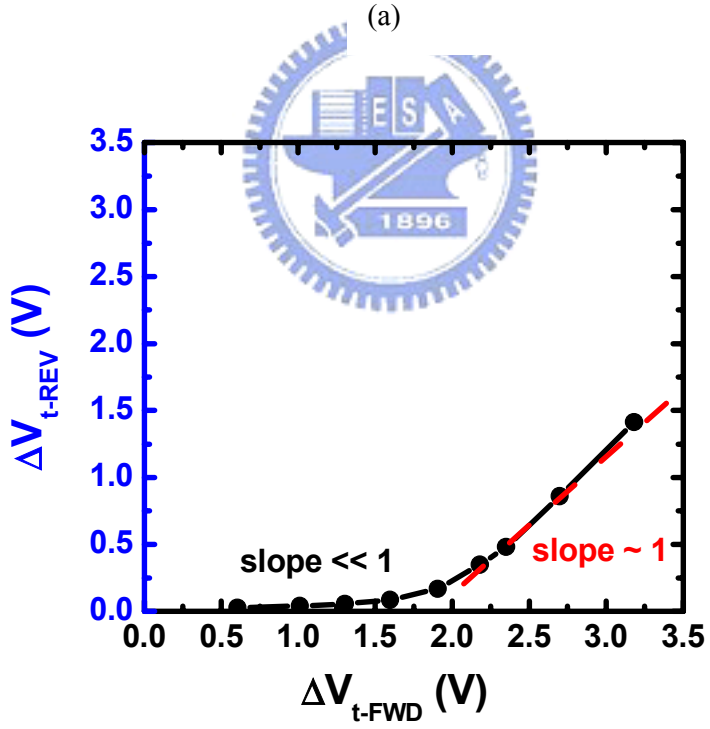


Fig.1.3 Junction bias effect on the reverse read scheme.



(a)



(b)

Fig.1.4 (a) Definition of the forward- and the reverse-read V_t of Bit-S. (b) $\Delta V_{t\text{-}REV}$ versus $\Delta V_{t\text{-}FWD}$ plot of the Bit-S in (a). Operating-V_t window is saturated due to the so-called 2nd-bit effect.

	Bit-D			Bit-S		
	V_g	V_d	V_s	V_g	V_d	V_s
Program (CHE)	11V	5V	0V	11V	0V	5V
Erase (BTBT HH)	-3V	8V	0V	-3V	0V	8V
Read (Reverse)	2.5V	0V	1.5V	2.5V	1.5V	0V

Table 1.1 Operating principles and bias conditions of an NBit cell.

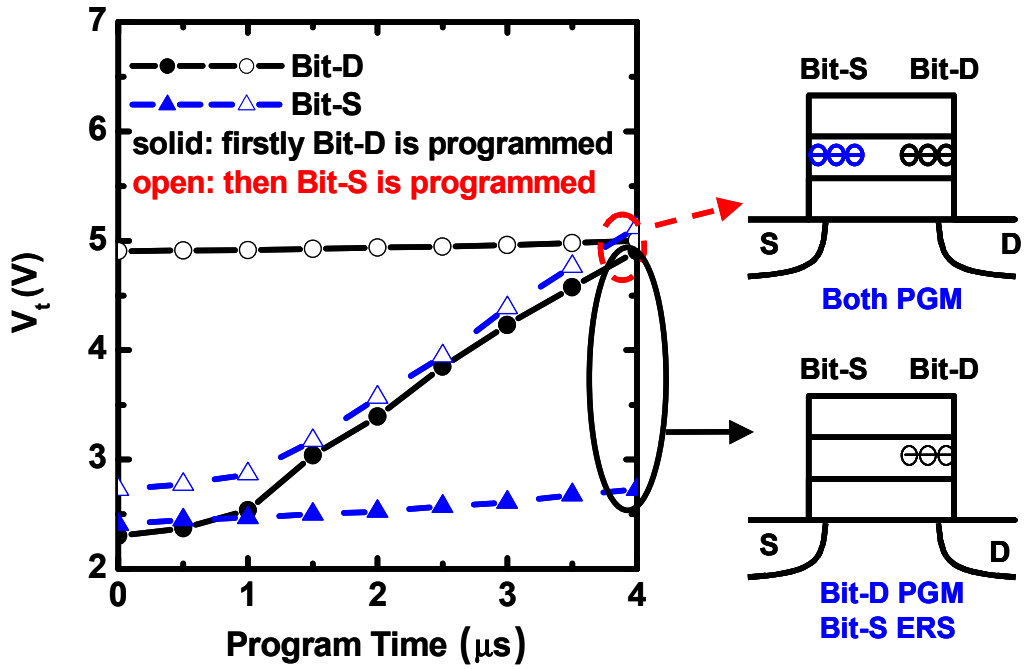


Fig.1.5 Two-bit programming characteristics of an NBit cell. Firstly, Bit-D is programmed while Bit-S is at erase state. Then Bit-S is programmed while Bit-D has been at program state.

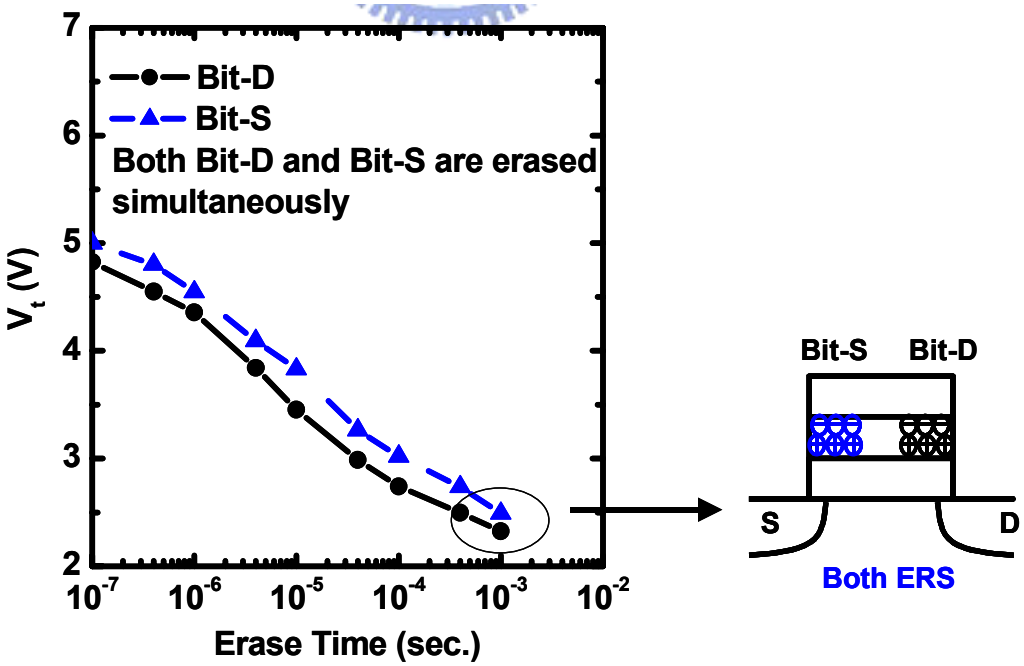


Fig.1.6 Two-bits erasing characteristics of an NBit cell.

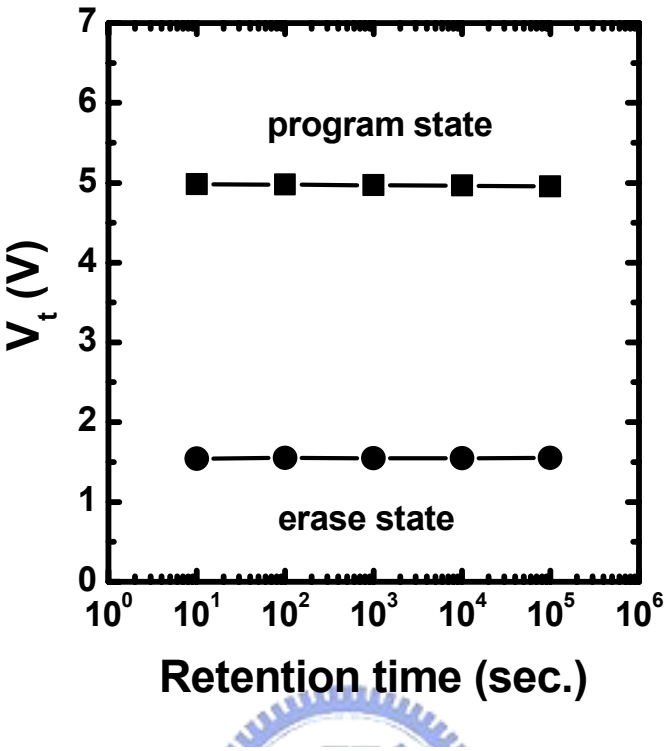


Fig.1.7 V_t versus retention time of a fresh NBit cell. The bake temperature is 150C.

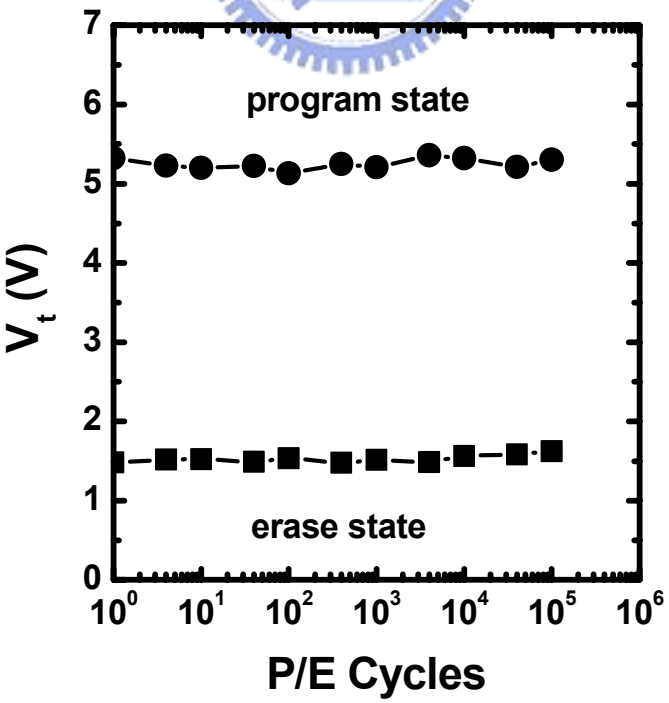


Fig.1.8 Endurance characteristics of an NBit cell.

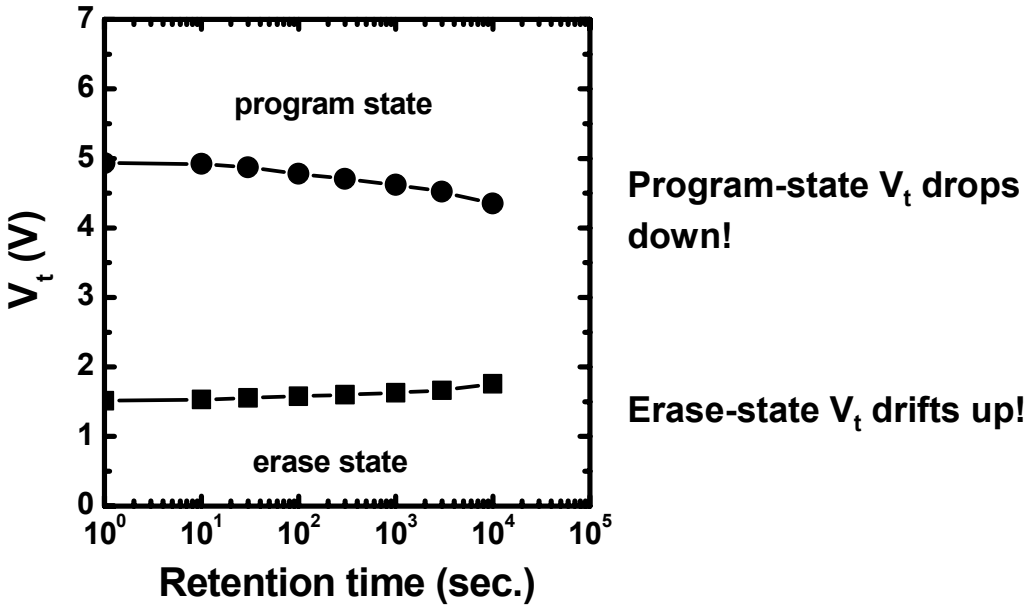


Fig.1.9 V_t versus retention time of a 10K P/E cycled NBit cell. The storage temperature is 25C.

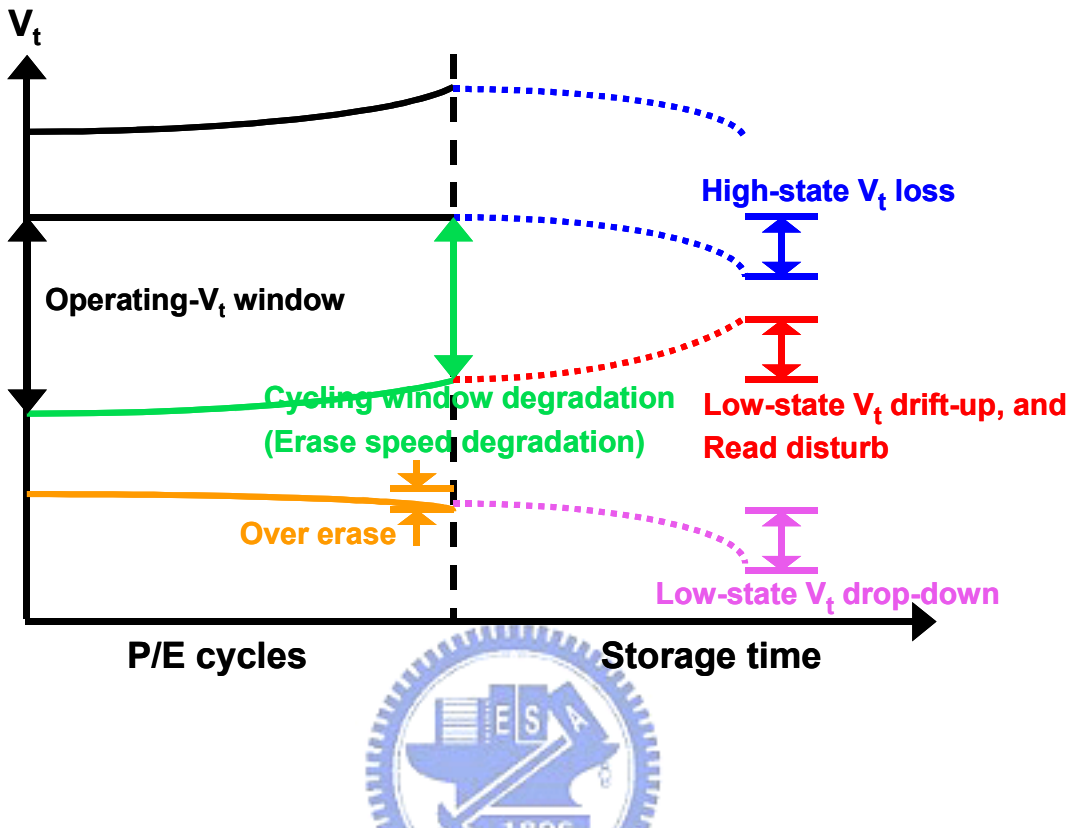


Fig.1.10 Representation of the reliability issues we have observed in an NBit cell.

Chapter 2

Charge Loss in a High-V_t Cell

2.1 Motivation

In previous chapter, we have showed that a fresh cell has good charge retentivity (Fig.1.7). However, charge retention in a P/E cycled cell degrades (Fig.1.9). Fig.2.1 shows that charge loss increases with cycle numbers. In addition, this charge loss exhibits strong temperature dependence (Fig.2.2).

It is still controversial about the mechanisms to explain the observed charge loss in the localized trapping-storage cells. Saifunís group has proposed that thermionic emission and then re-distribution or leak-out of the stored electrons are the cause of V_t loss in an un-cycled cell [2.1]. They also claimed that lateral re-distributions of the trapped charges, especially some residual holes, account for the V_t loss in a cycled one [2.2-2.3]. However, we do not find any direct evidence of ìnetî residual holes in a cycled cell which is at program state. Meanwhile, we find that the V_t loss is strongly dependent on the applied V_g bias during retention test. Charge loss along the vertical direction is suspected. In the following sections, we would develop the models in detail.

2.2 Experimental

2.2.1 Device Samples

The cell used in this work (and in the dissertation) is made of an n-channel MOSFET with an oxide-nitride-oxide (ONO) gate dielectric structure (Fig.1.1). Typically, the thickness of each ONO layer is 9nm (top oxide), 6nm and 6nm, and W_g/L_g is 0.38μm/0.48μm. An ONO capacitor (2.5×10^5 μm^2) with uniform stress and charge storage is also used. The effect of lateral charge migration can be excluded in this device. The evolution of the flatband voltage (V_{fb}) of the ONO capacitor with time is monitored to study the charge retention behavior. Finally, a 64Mb chip with a sector size of 512Kb which is composed of such cells is also characterized. It is used to demonstrate that the observed phenomena in a single cell and the utilized methods to characterize it are consistently applicable to a real product.

2.2.2 Characterization Techniques

Two specific methods are utilized to study the lateral spreading of the injected carriers. Assuming that electrons are trapped in the nitride layer above the channel nearby the junction, a V_t versus V_j measurement is used to investigate the lateral extent of the trapped electrons (Fig.2.3 (a)). Here, V_t is defined as the applied gate voltage that induces a drain current of 1μA. These trapped electrons will raise the potential barrier nearby the injection junction. An increased V_t, which is proportional to the trapped electron density, will be measured at a low junction bias (V_{j1} in Fig.2.3). As a sufficiently high junction bias (V_{j2} in Fig.2.3) is applied, the junction depletion region will extend toward the channel. The trapped electrons will have little effect on the measured I-V characteristics when they are located within the junction depletion region [2.4]. The trapped electron density and its lateral extent can be estimated by this measurement (Fig.2.3 (b)).

A charge-pumping (CP) method [2.5], which is also able to probe the lateral distribution of trapped charges, is also used. Letís see Fig.2.4 (a). A trapezoidal pulse train (Gate pulse P) with a fixed high level (V_{gh}) and successively decreasing low levels (V_{gl}) is applied to the gate of the device. The substrate and the drain are grounded and the source is floating. The charge-pumping current I_{cpP} ($=I_d=I_b$) versus V_{gl} is measured. The fixed V_{gh} is sufficiently high to ensure that the entire channel is inverted. By varying V_{gl}, only the part of channel that undergoes inversion-accumulation-inversion over a pulse cycle contributes to I_{cpP}. Since the trapped electrons (near the drain side) cause an increase of the local flatband voltage, an I_{cpP} shift along the V_{gl} axis will be observed in a programmed cell. Based on the measured I_{cpP} versus V_{gl} curves of an un-programmed and a programmed cells (Fig.2.4 (b)), the trapped electron density can be extracted [2.5]. The trapped hole density can be profiled in a similar manner by a pulse train with a fixed low level and successively increasing high levels (Gate pulse E in Fig.2.4 (a)) applied to the gate. The lateral migration of trapped charges in both the program and the erase states can also be estimated by this technique.

2.2.3 Characterization Results

We use the V_t versus V_d characteristics to give an indication of the density and the lateral extent of the trapped electrons in a programmed cell. Fig.2.5 shows the V_t-V_d characteristics of a 100K P/E cycled cell in the program state before and after 24 hours storage. The storage temperature is 85C. It can be seen that the V_t has dropped due to charge loss, however, the shape of V_t versus V_d curves is essentially unchanged and there is no crossover in the V_t versus V_d characteristics before and after 85C, 24 hours storage. This indicates that lateral migration of electrons does not occur. We have also applied the charge-pumping technique to probe the lateral electron extent (Fig.2.6). If the trapped electrons spread laterally during the storage period, an increased I_{cp} will be observed due to the extension of the trapped electron area. As indicated in Fig.2.6, the leftward shift of the I_{cp} implies a decrease of the trapped electron density. However, no clear evidence of lateral electron movement is shown in the charge-pumping characteristics. On the other hand, we find the charge loss is strongly dependent on the applied vertical field during the retention test (Fig.2.7). It gives us a hint that the stored charges may leak out along the vertical direction: from the trapping nitride through the bottom oxide to the substrate.

In order to correlate the V_t loss to charge escape through the bottom oxide, the temporal evolution of the flatband voltage of an ONO capacitor was measured (Fig.2.8). The ONO capacitor has undergone a negative gate stress (-100nA for 1000 seconds, to emulate the P/E cycling effect) and then was programmed to a high-V_t state by +FN injection. Since the structure has uniform charge storage, lateral re-distribution effect of the stored charges can be excluded. Charge loss through the bottom oxide should be the only cause for the flatband voltage shift. The gate bias in the measurement is from V_g=0V to V_g=-6V. The measured results are shown in Fig.2.9. The flatband voltage shift indeed exhibits vertical field dependence, which is similar to the V_t loss behavior we observed in a single cell (Fig.2.7).

2.3 Charge Loss Model

We thus propose the physical mechanism to explain the charge loss behavior in a P/E cycled cell, as shown in Fig.2.10. The field- and temperature-accelerating effects and the cycling-enhanced effect on the charge loss suggest that the nitride charge escape is through thermionic-field emission and subsequent oxide trap-assisted tunneling. Frenkel-Poole model has been recognized to be the dominant charge carrier transport mechanism in nitride [2.6]. According to the model, the emission time

constant τ_{en} of an electron in a nitride trap of energy depth of ϕ_{en} below the nitride conduction band edge can be expressed as:

$$\tau_{en}(\phi_{en}) = \tau_{en0} \exp(\frac{\phi_{en} - q\sqrt{\frac{qE_n}{\pi\varepsilon_n}}}{kT}) \quad (2.1),$$

where E_n is the nitride field and ε_n is the nitride dielectric constant. If the trapped electron density (corresponding to the trap level of ϕ_{en}) is N_{en0} right after programming, it will evolve with time as:

$$N_{en}(\phi_{en}, t) = N_{en}(\phi_{en}, 0) \exp(-\frac{t}{\tau_{en}(\phi_{en})}) = N_{en0} \exp(-\frac{t}{\tau_{en}(\phi_{en})}) \quad (2.2).$$

In a Frenkel-Poole emission limited condition (*i.e*, τ_{ox} in Fig.2.10 sufficiently fast), the nitride charge escape current can be derived as:

$$I_{en}(t) \propto \int \frac{dN_{en}(t)}{dt} d\phi_{en} \propto N_{en0} \int \exp(-\frac{t}{\tau_{en}(\phi_{en})}) \cdot \frac{d\phi_{en}}{\tau_{en}(\phi_{en})} \propto \frac{N_{en0} kT}{t} \quad (2.3),$$

assuming that the trapped electron distribution (right after programming) is continuous in the energy spectrum and is with a constant trapping density (N_{en0}) in the nitride. The corresponding V_t loss would be:

$$\Delta V_t(t) \propto \Delta Q_{en}(t) \propto \int I_{en}(t) dt \propto N_{en0} [q\sqrt{\frac{qE_n}{\pi\varepsilon_n}} + kT \ln(\frac{t}{\tau_{en0}})] \quad (2.4).$$

According to Eq. (2.4), V_t and V_{fb} evolution is linearly dependent on log(t), which is as shown in Fig.2.7 and Fig.2.9 for a single cell and a capacitor, respectively. Besides, the charge loss is proportional to the square root of the nitride field, which is proportional to (V_0-V_g). This is shown in Fig.2.11. Here, V_0 is the built-in potential, including the flatband voltage and trapped charge effects, at program state. From a 2D device simulation [2.7], V_0 is around 2V in the single cell and 5V in the capacitor.

Learning from Fig.2.7, it is apparent that V_g is an effective accelerating factor for retention lifetime measurement. If we assume that during the discharge time t all the nitride traps with time constants less than t will be completely emptied and all other traps will be unaffected, the memory retention time will be equal to the nitride charge detrapping time (we assume oxide trap assisted tunneling is sufficiently fast.). According to Eq. (2.1), we would further expect that:

$$\frac{d\log(Lifetime)}{d\sqrt{V_0 - V_g}} \propto \beta \qquad (2.5),$$

where

$$\beta = \log(e)\frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_N T_{ono}}} \qquad (2.6),$$

by $E_n=(V_0-V_g)/T_{ono}$. Here, T_{ono} is the equivalent thickness of the ONO stack. β is calculated to be 2.6 decade/$V^{0.5}$ in our sample.

In Fig.2.12, we plot the retention lifetime versus $(V_0-V_g)^{0.5}$. The symbols represent the measured result. The extracted slope in Fig.2.12 is about 2.75 decade/$V^{0.5}$ which is close to the theoretical value of 2.6 decade/$V^{0.5}$. The extrapolated memory retention time at V_g=0V is about 10^7 sec. for ΔV_t=1.5V and is above 10 years for ΔV_t=2.0V. We have also plotted the retention lifetime versus $(V_0-V_g)^{0.5}$ of an ONO capacitor as shown in Fig.2.13. The slope is 2.49 dec/$V^{0.5}$ which is quite close to the theoretical value (2.6 decade/$V^{0.5}$) and the slope of a memory cell (2.75 decade/$V^{0.5}$). It implies that the vertical charge loss occurs in an ONO capacitor with uniform charge storage and also in a memory cell with localized charge storage.

In this model, cycling-induced oxide defect is considered to be the stepping stone of the charge loss. Fig.2.14 shows the increase of the charge-pumping current (right axis) of the cell versus cycle numbers. The charge-pumping current is a direct measurement of the density of the interface states (N_{it}). It can be found that $I_{cp,max}$ (Fig.2.4(b)) increases with cycle numbers. The growth rate follows a power law with the power factor of 0.5. It is quite consistent with the generation of interface states in a stressed NMOSFET [2.8], which implies that the bottom oxide is damaged during

P/E cycling. It is also suggested that bulk oxide defects (Q_{ox}) are also created meanwhile [2.9]. However, itís hard to measure the bulk oxide trap density directly. We plot the charge loss versus cycle numbers on a log-log plot (Fig.2.14, left axis). A power law dependence with the power factor of 0.24, which is quite close to the generation rate of bulk oxide traps in a stressed NMOSFET [2.8], is obtained. It provides an indirect evidence of the role of oxide trap and its generation during P/E cycling.

2.4 Product Demonstration

The model is successful verified by a single cell and a capacitor. We would like to apply the same field accelerating method to a memory array under real product operation. A 64Mb chip used in this study is fabricated by 0.25μm process with a sector size of 512Kb. The cycling is performed on a MOSAID tester [2.10] and all bits are programmed and erased within one cycle. During retention test, checker-board pattern is used. In other words, each cell has one programmed bit and one erased bit at the same time.

In Fig.2.15, the V_t evolution with retention time at V_g=-3V is measured for a chip before and after 10K cycles. Charge loss is observed for the cycled high-V_t cells. To simplify the notation, the $<V_t>$ is used to represent the mean value of the high-V_t distribution. In Fig.2.16, the field-accelerating effect on the $\Delta<V_t>$ is observed and the dependence is quite similar to the single cellís results (Fig.2.7). At both cases, charge loss increases with increasing vertical field. In Fig.2.17, the cycle number dependence of the $\Delta<V_t>$ is measured at V_g=-7V. The charge loss increases with the cycle number and a power law dependence with the power factor of 0.223 is observed. Once again, it is close to the power factor of 0.29 obtained in a single cell (Fig.2.14). From Fig.2.15 to Fig.2.17, we know that the single cell and the product are well-correlated, and the validity of field acceleration is confirmed at product level as well as in a single cell.

2.5 Temperature Effect

The temperature-accelerating method is widely used in the retention test of a floating-gate cell [2.11]. We also investigate such application. Fig.2.18 shows the charge loss versus time at T=25C, 85C and 150C, respectively. In addition to the

strong dependence on the bake temperature, the retention loss at 150C shows a saturation behavior. Further study by using a charge-pumping technique reveals that amounts of the interface traps are annealed (Fig.2.18 (b)). We would suspect that trap annealing effect plays a role during the high-temperature bake period.

Letís also apply the high-temperature baking test to a chip. The chip firstly undergoes 10K P/E cycles. Two kinds of retention test procedure are compared. One is purely to bake the chip at 150C for 50 hours, and the other is to apply an extra field acceleration (by V_g=-3V, 18.5 hours) to the chip before baking.

In Fig.2.19, the $\Delta<V_t>$ís of sectors with and without a preceding field acceleration are compared after baking. $\Delta<V_t(\text{field})>$ and $\Delta<V_t(\text{bake})>$ represent V_t loss due to field acceleration and bake, respectively. Fig.2.20 shows similar results of different accelerating vertical field. Some interesting phenomena are observed. Firstly, regardless of cycle numbers, $\Delta<V_t(\text{bake})>$ is reduced if a preceding field acceleration has been applied. Secondly, the overall retention loss is similar for both cases at low cycle numbers, however, it is larger for the field-acceleration-and-then-bake one after 10K cycles. Thirdly, charge loss by field acceleration ($\Delta<V_t(\text{field})>$ by Vg=-5V, 18.5 hours) could be larger than that by high-temperature bake only ($\Delta<V_t(\text{bake})>$ at T=150C, 50 hours without a preceding field acceleration) as shown in Fig.2.20. And finally, the same $\Delta<V_t(\text{bake})>$ (~0.2V) is found in 10K cycled sectors after strong field acceleration, though the accelerating field and $\Delta<V_t(\text{field})>$ are quite different (Fig.2.20).

To investigate the relationship between these two accelerating methods, emulated single cells are firstly cycled up to 10K times. Retention loss is measured firstly by a negative-V_g acceleration with various time, and then by another high-temperature bake at T=150C for 50 hours, as illustrated in Fig.2.21. The $\Delta I_{cp,max}$ís before and after baking are also described. The overall V_t loss ($\Delta V_t(\text{field})+\Delta V_t(\text{bake})$) is a constant value (~0.5V) as $\Delta V_t(\text{field})$ is less than 0.3V, and it drops further (about additional 0.2V) when $\Delta V_t(\text{field})$ exceeds 0.5V. If the two accelerating factors, temperature and field, are interchangeable, $\Delta V_t(\text{bake})$ will increase with decreasing $\Delta V_t(\text{field})$. In Fig.2.22, $\Delta V_t(\text{bake})$ following various field-accelerating conditions is collected and is plotted along with its preceding $\Delta V_t(\text{field})$. $\Delta V_t(\text{bake})$ shows a negative linearly correlation with $\Delta V_t(\text{field})$ as $\Delta V_t(\text{field})$ is less than 0.5V. It implies that both methods are interchangeable if the overall retention loss is within 0.5V. However, if $\Delta V_t(\text{field})$

is more than 0.5V, the following bake would result in an additional, constant V_t loss (~0.2V).

Trap annealing is proposed to explain these phenomena. During high-temperature bake, traps are annealed [2.12-2.14]. As shown in Fig.2.23, the annealing effect would re-fresh the cell [2.14] and the charge leaky paths through the bottom oxide are reduced. V_t loss is thus saturated at 0.5V. However, larger V_t loss may be found by field acceleration since traps are not annealed in this approach. Once the field-accelerated V_t loss exceeds the saturated value (as seen by temperature acceleration), the additional, constant V_t loss in the following bake period is due to the interface state annealing effect.

2.6 A Simple Monitor of Charge Retentivity

In Fig.2.14 and Fig.2.17, we suggest that the bottom oxide damage may be responsible for the retention loss induced by field acceleration, since the power factor (0.223 or 0.29) is quite consistent with the published oxide trap generation rate [2.8]. Since the generation of interface traps is an indicator of the bottom oxide damage, $\Delta I_{cp,max}$ ($\propto \Delta N_{it}$) is expected to be related to charge loss. In Fig.2.24, a positive correlation is found between a field-induced ΔV_t and the $\Delta I_{cp,max}$. Meanwhile, it has been demonstrated that the bake-induced ΔV_t are also positively correlated with the I_{cp} [2.14-2.15].These results strongly support that the charge loss by both kinds of accelerating method are related to bottom oxide damage. Furthermore, the cycling number dependence of $\Delta I_{cp,max}$ of cells of four process conditions is characterized (Fig.2.25). Though the magnitude is difference, the power law dependence still stands and the power factors are similar. After baking at 150C for 50 hours, the corresponding ΔV_tís of these 10K cycled cells are measured (Fig.2.26). A positive correlation between ΔV_t and $\Delta I_{cp,max}$ is also identified. It implies that $\Delta I_{cp,max}$ after P/E cycling would be a good monitor of the charge retentivity of the NBit cell.

2.7 Summary

Charge loss of the NBit cell at program-state is investigated. It is found that the charge loss is negligible in a fresh cell. Charge loss increases with cycle numbers and shows strong dependence on temperature and the applied vertical field during retention test.

Our study find that lateral re-distribution of trapped charges has little effect in a highly cycled cell. V_t loss is attributed mostly to nitride charges escape by Frenkel-Poole emission and subsequent oxide trap-assisted tunneling. These oxide traps are created during P/E cycling. A linear dependence of the nitride charge loss on the square-root of the electric field is obtained. This model is well confirmed by both the single cell and the product characterization. According to these concepts, a V_g-accelerating technique and a temperature-accelerating method are therefore developed. No matter which accelerating factors are used, evidences have been provided to demonstrate that the retention loss of NBit cells is related to the bottom oxide damage, i.e. the charge loss path is the same. The field and temperature accelerations are found to be interchangeable. Stress-induced interface state density is a good monitor of cellís retention. In addition, the annealing of interface states would be another source of the observed V_t loss in a highly cycled cell, and the annealing of oxide traps would cause the saturation of V_t loss when baking at high temperature.

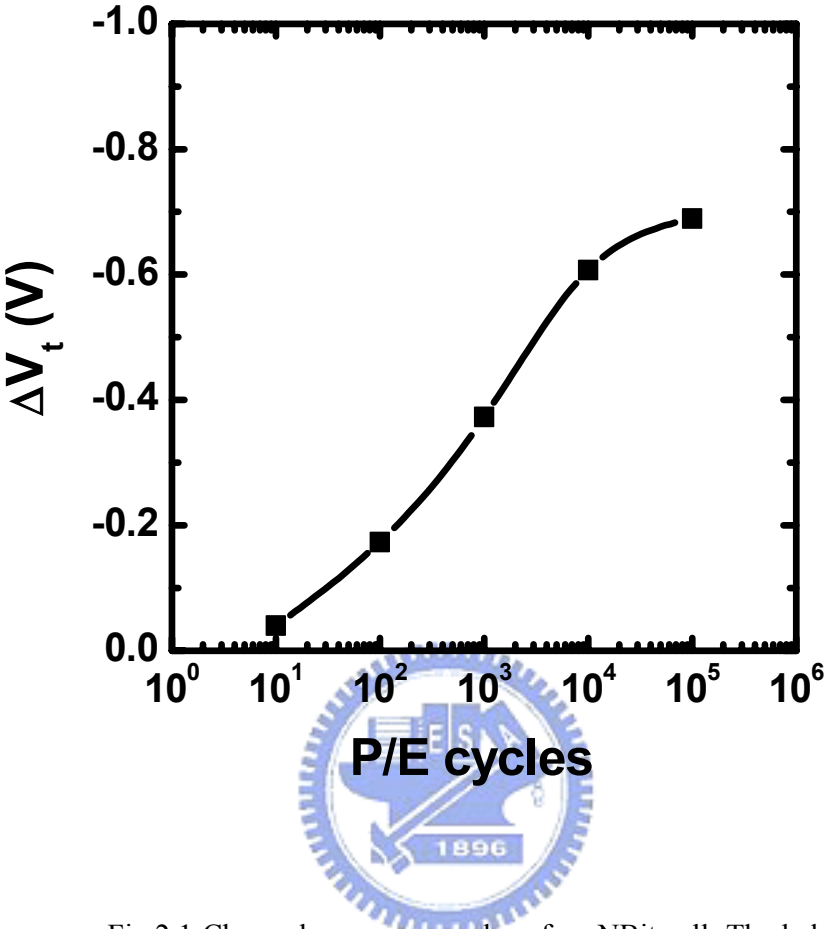


Fig.2.1 Charge loss versus cycles of an NBit cell. The bake is at 150C for 24 hours.

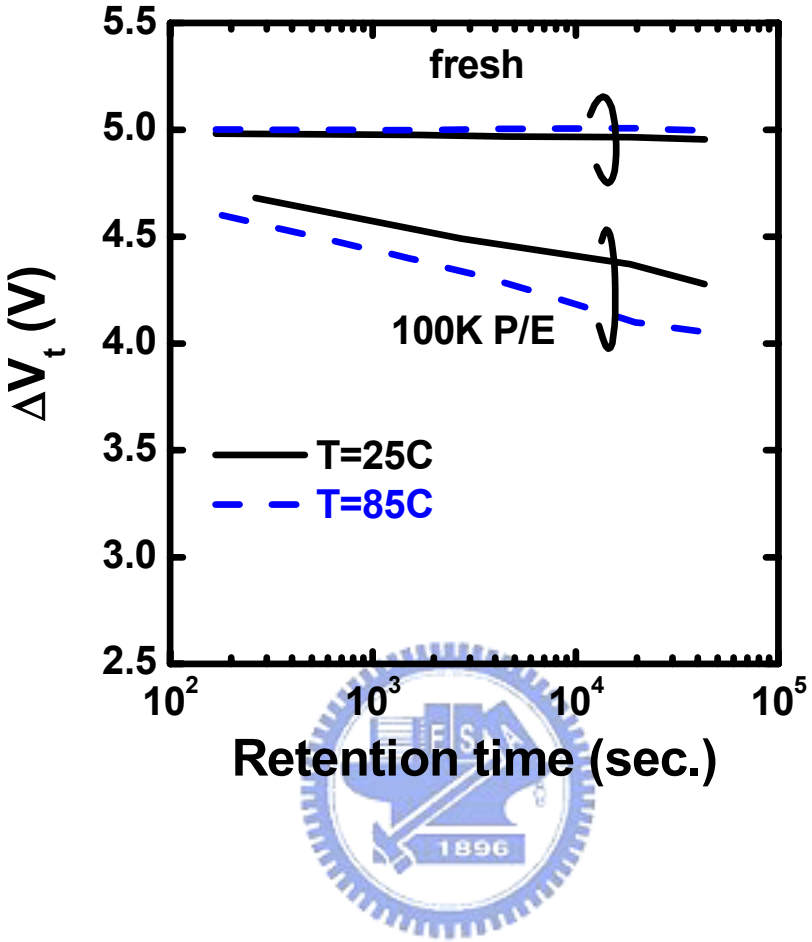
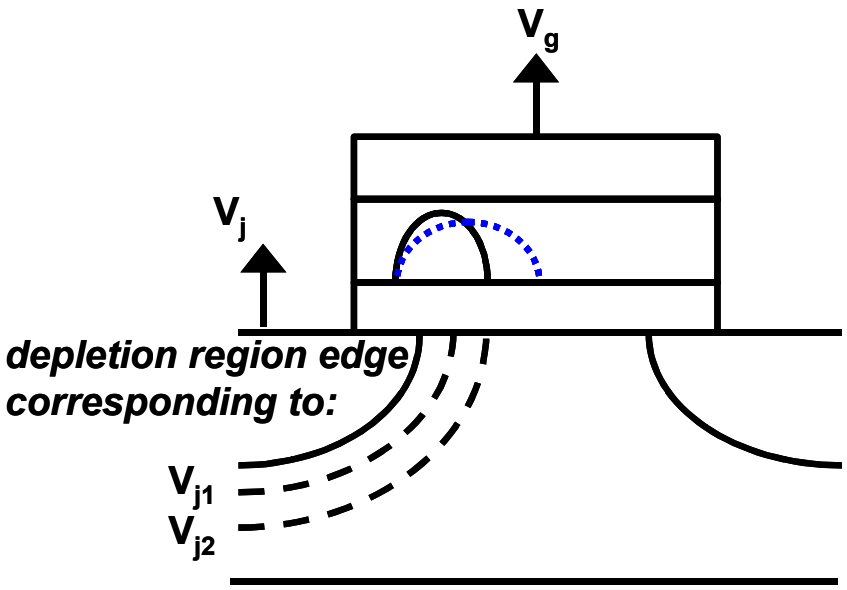
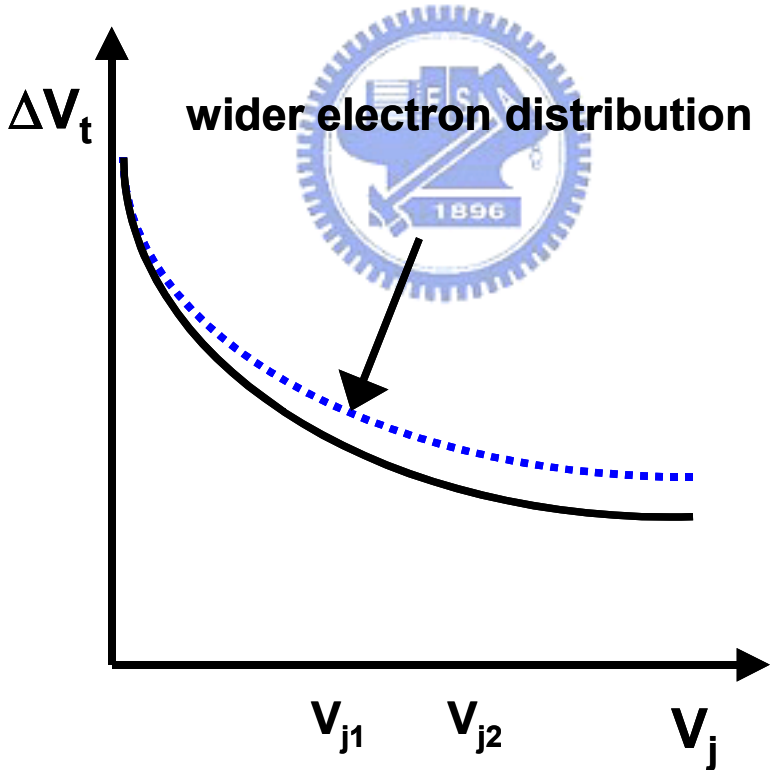


Fig.2.2 Program-state charge loss versus retention time in a fresh and a 100K P/E cycled NBit cells. T=25C and 85C.

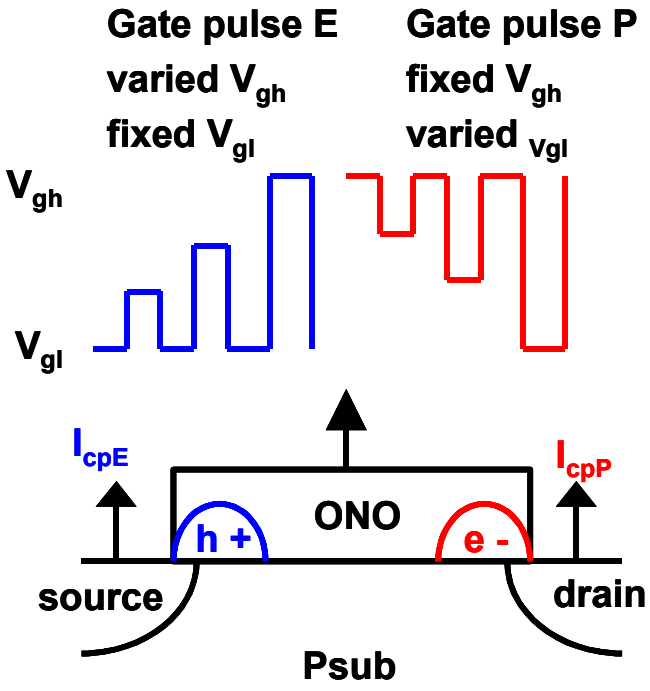


(a)

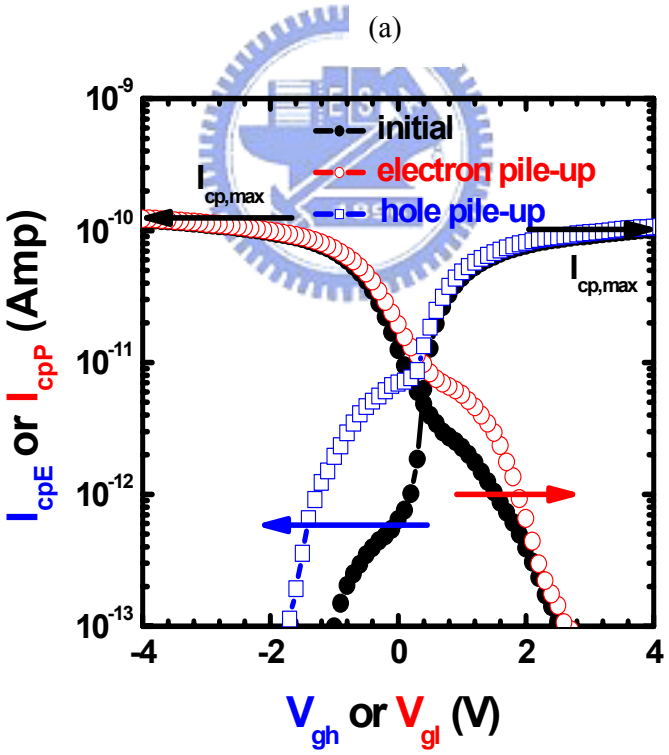


(b)

Fig.2.3 (a) Concept of V_t-V_j measurement to explore the trapped electron extent in an NBit cell. (b) Illustration of V_t-V_j characteristics by which charge lateral extent can be estimated. The dashed one has a wider electron distribution as shown in (a).



(a)



(b)

Fig.2.4 (a) Charge-pumping current (I_{cp}) measurement to characterize the localized trapped charges nearby the injection junction. (b) Trapped-hole (I_{cpE}, open square) and trapped-electron (I_{cpP}, open circle) effect on the measured I_{cp} characteristics.

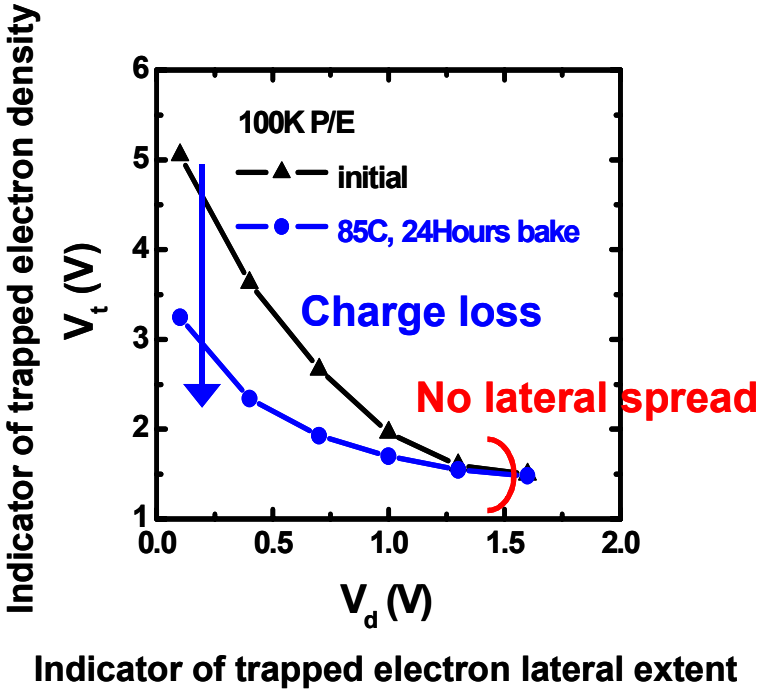


Fig.2.5 The measured V_t versus V_d characteristics of a 100K P/E cycled cell before and after 24 hours, 85C storage. The cell is at program state.

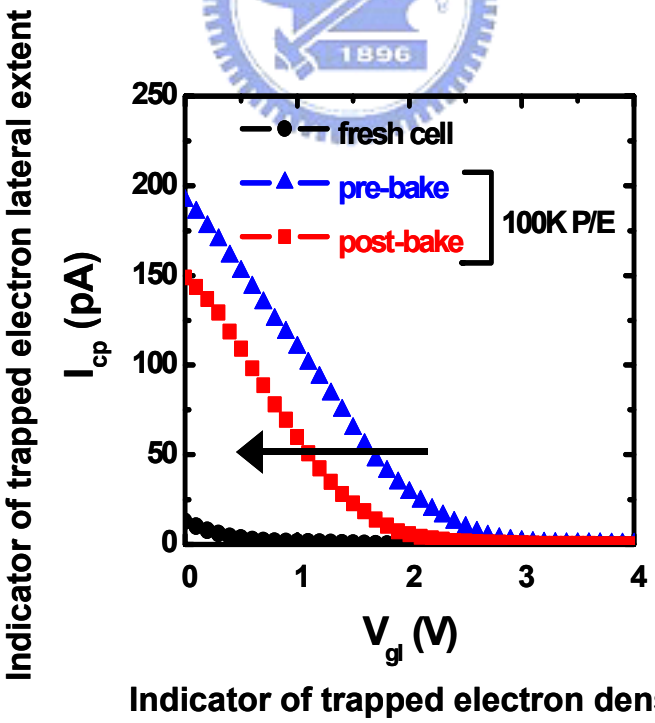


Fig.2.6 The measured charge-pumping current (I_{cp}) versus the low level of gate pulse (V_{gl}) in the CP measurement. The 100K cycled cell is at program state. The bake time is 24 hours and the bake temperature is 85C.

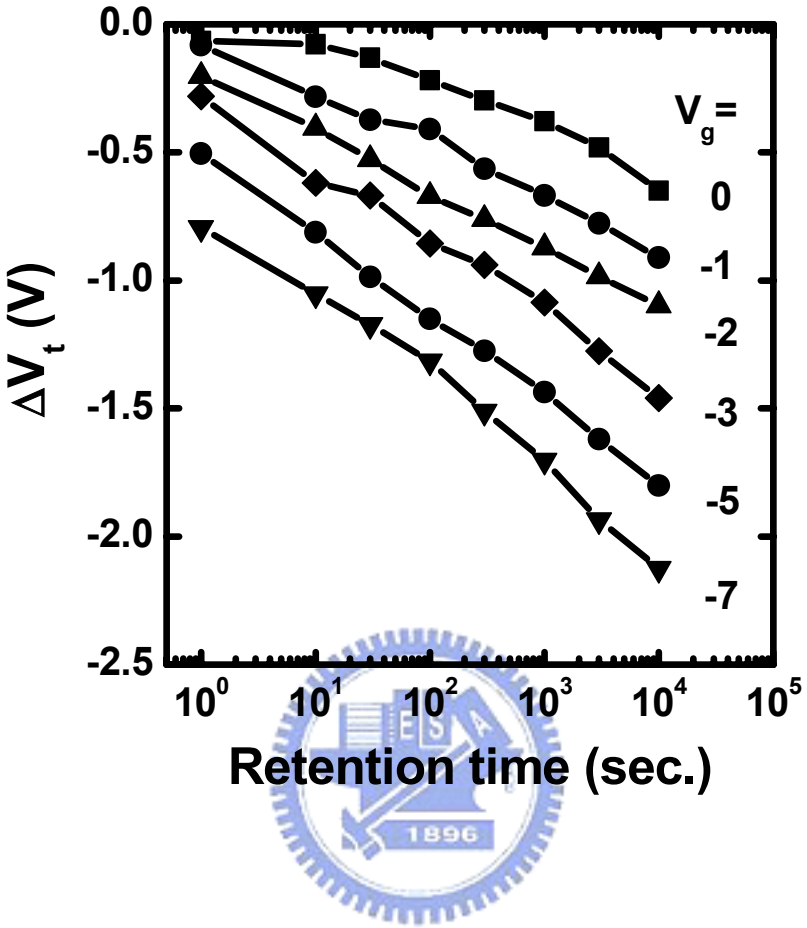


Fig.2.7 Program-state charge loss at different applied gate biases. T=25C.

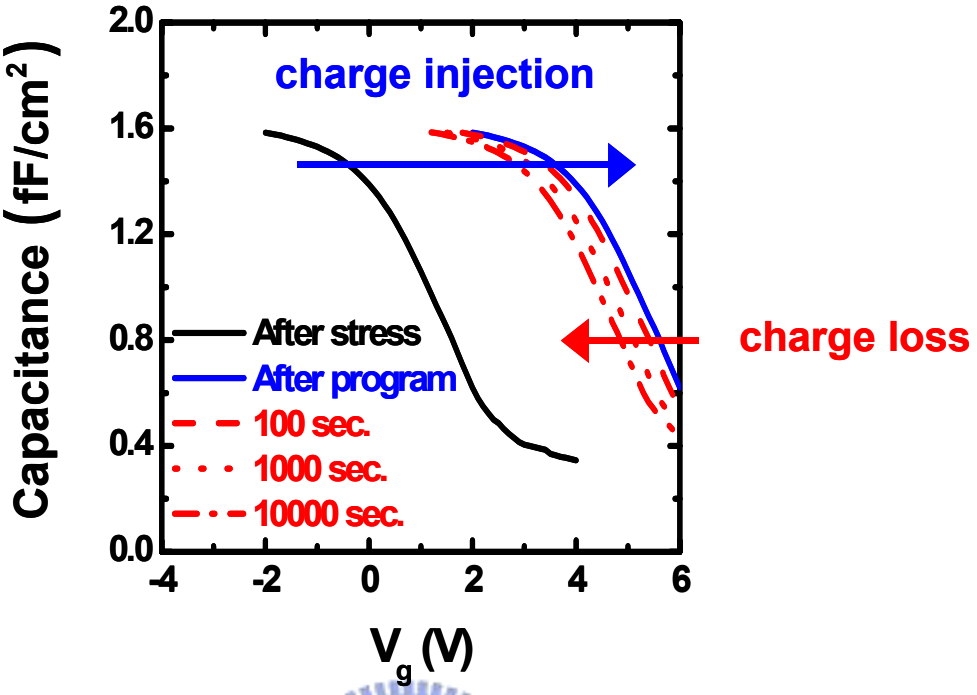


Fig.2.8 The CV temporal evolution of an ONO capacitor.

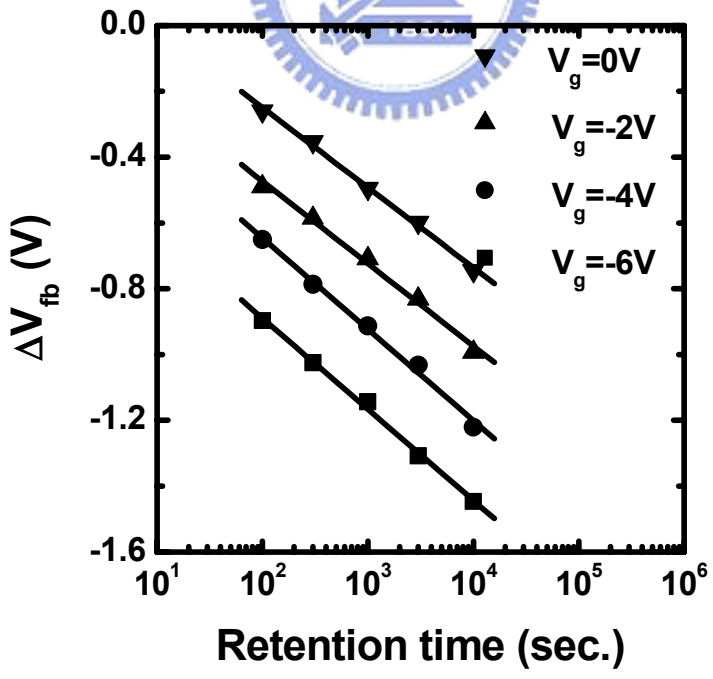


Fig.2.9 Evolution of the flatband voltage shift with the retention time in an ONO capacitor. The gate biases in measurement are 0, -2V, -4V, and -6V.

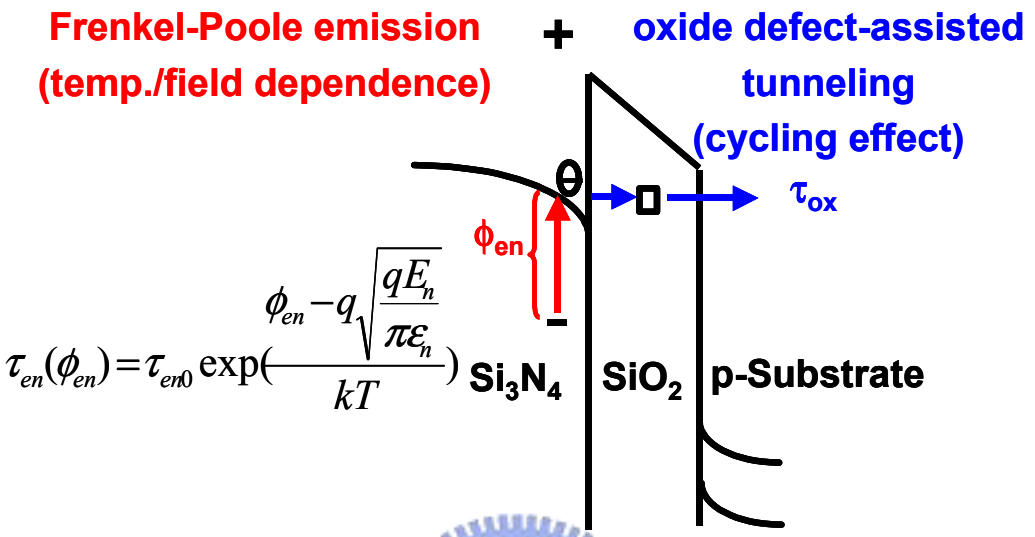


Fig.2.10 Illustration of nitride trapped charges escape via Frenkel-Poole emission and subsequent oxide defect-assisted tunneling.

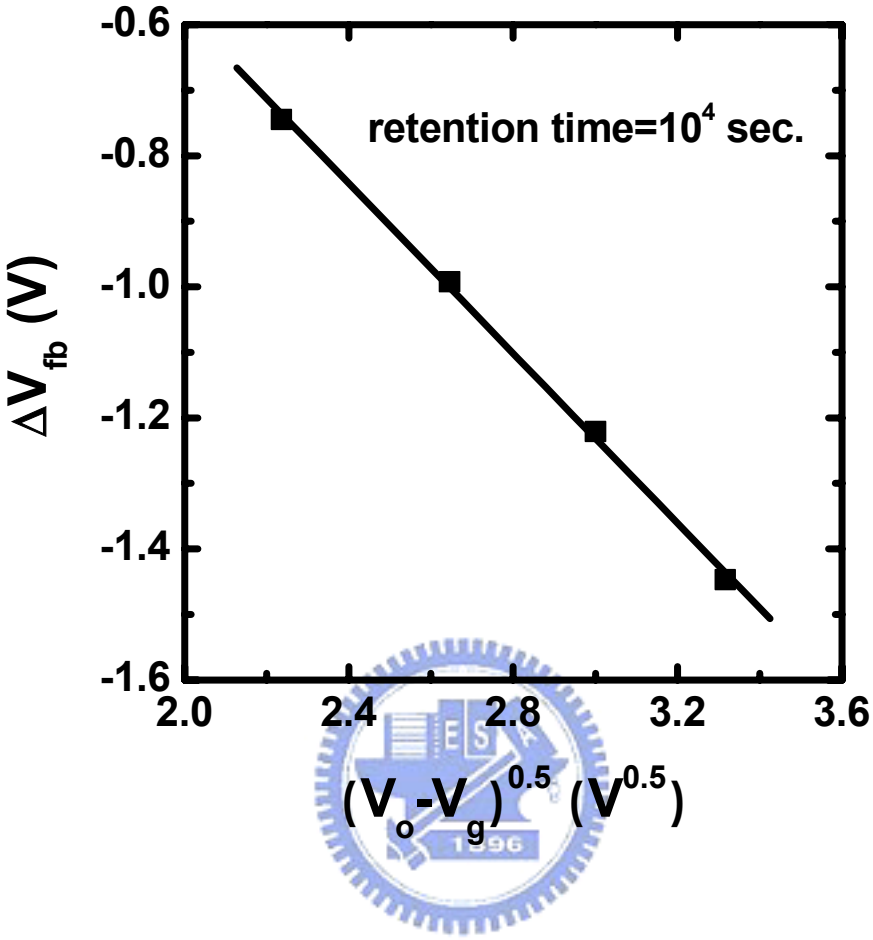


Fig.2.11 The measured flatband voltage shift versus the square root of the nitride electric field which is proportional to (V_0-V_g). V_0 represents the internal built-in field including the flatband voltage and the trapped charge effects. It is 5V in our example. The storage time is 10000 sec..

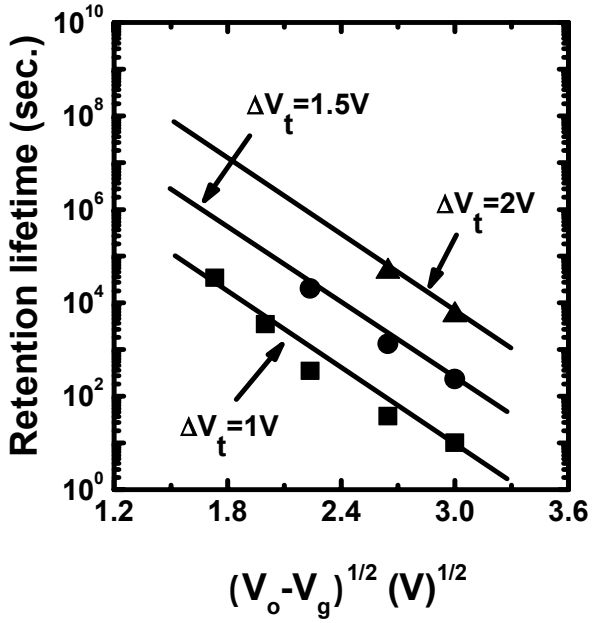


Fig.2.12 The charge retention lifetime versus $(V_0-V_g)^{1/2}$. Retention lifetime is defined as the storage time sustained for ΔV_t=1V, 1.5V, and 2V, respectively.

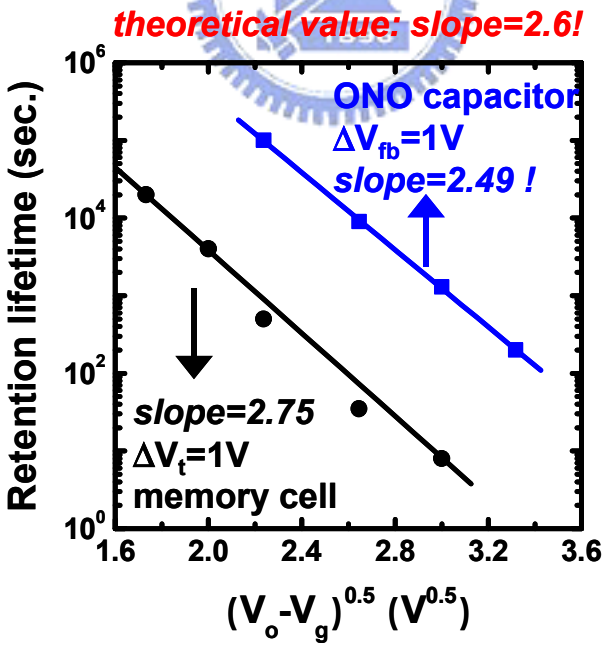


Fig.2.13 The retention lifetime versus $(V_0-V_g)^{1/2}$. V_0 is 2V and 5V for the cell and the capacitor, respectively. The retention lifetime is defined as the storage time sustained for a 1V shift of the V_{fb} of the capacitor or a 1V shift of the V_t of the memory cell.

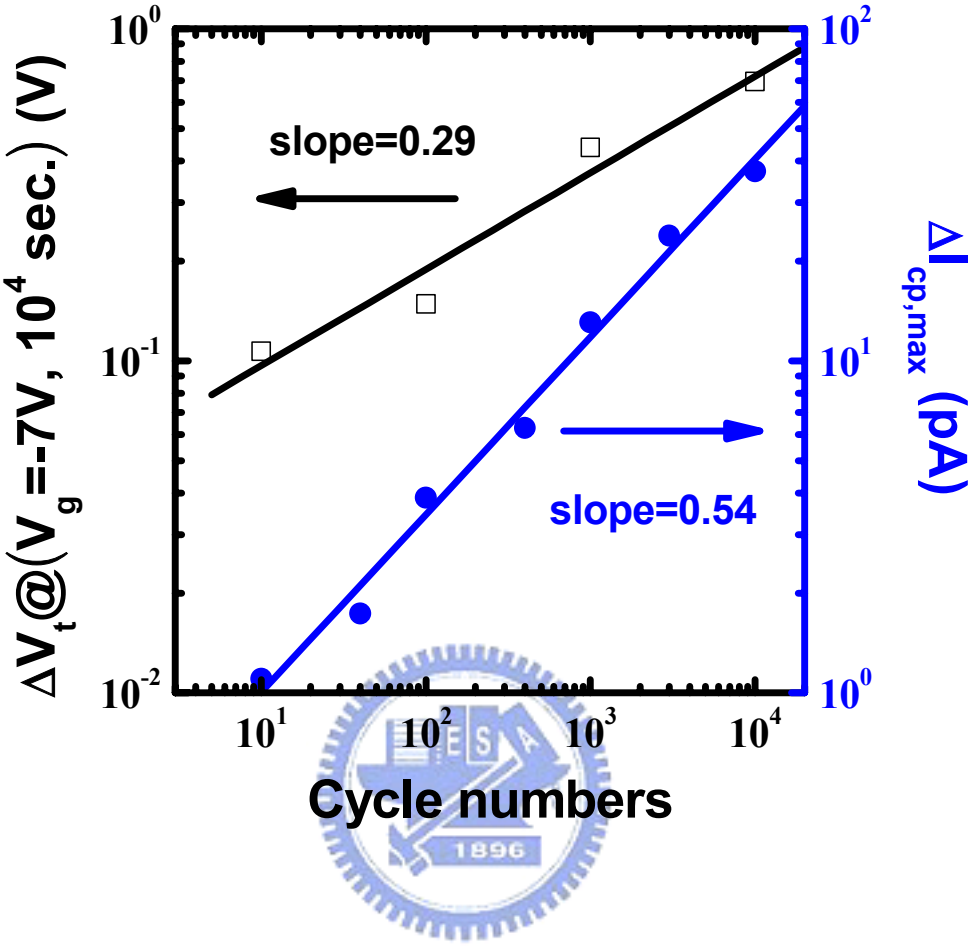


Fig.2.14 ΔV_t (by field acceleration) and $\Delta I_{cp,max}$ versus cycle numbers of an NBit cell.

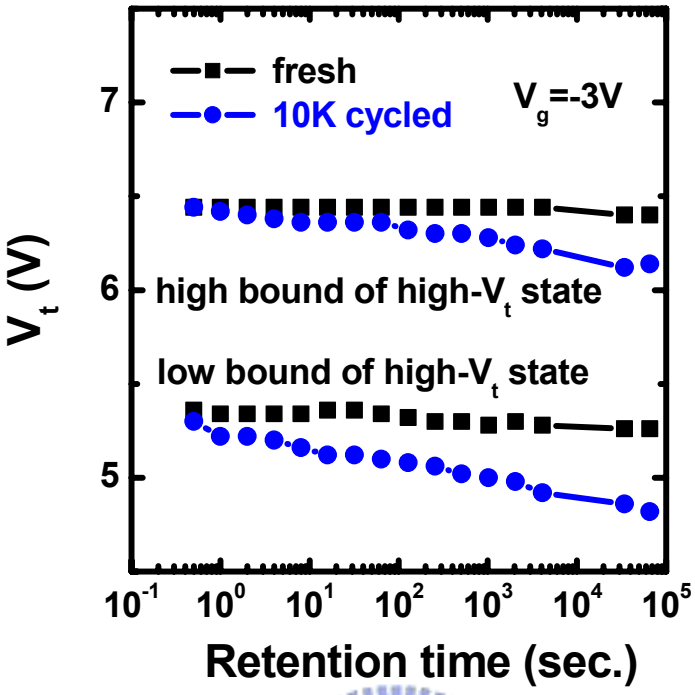


Fig.2.15 V_t evolution with V_g-accelerating time of a fresh and a 10K cycled sectors. V_g=-3V.

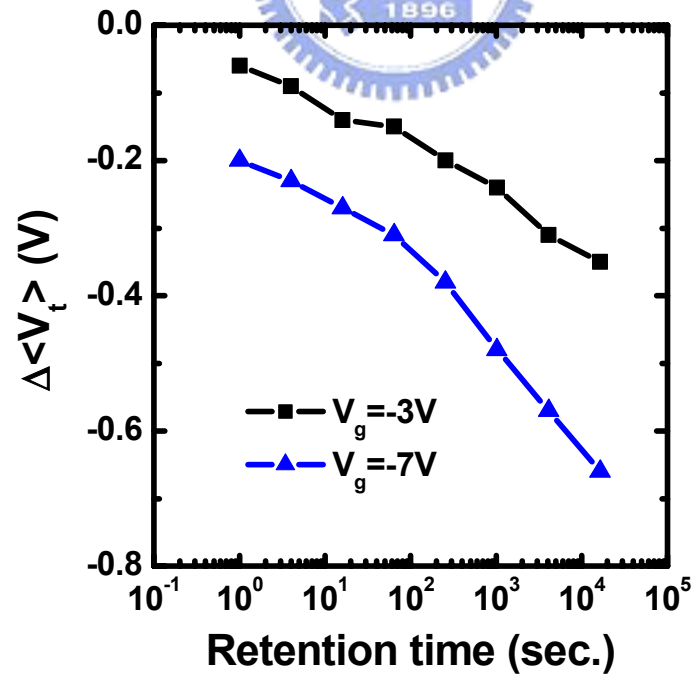


Fig.2.16 $\Delta<V_t>$ evolution with V_g-accelerating time of a 10K cycled sector. V_g= ñ3V and ñ7V.

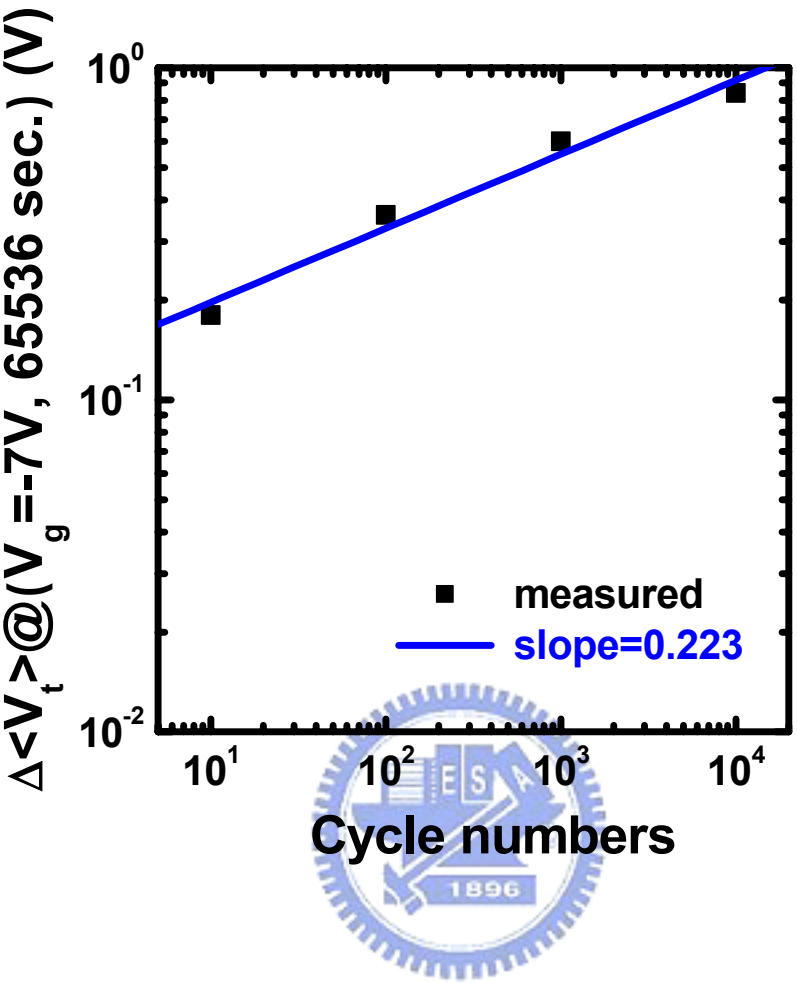
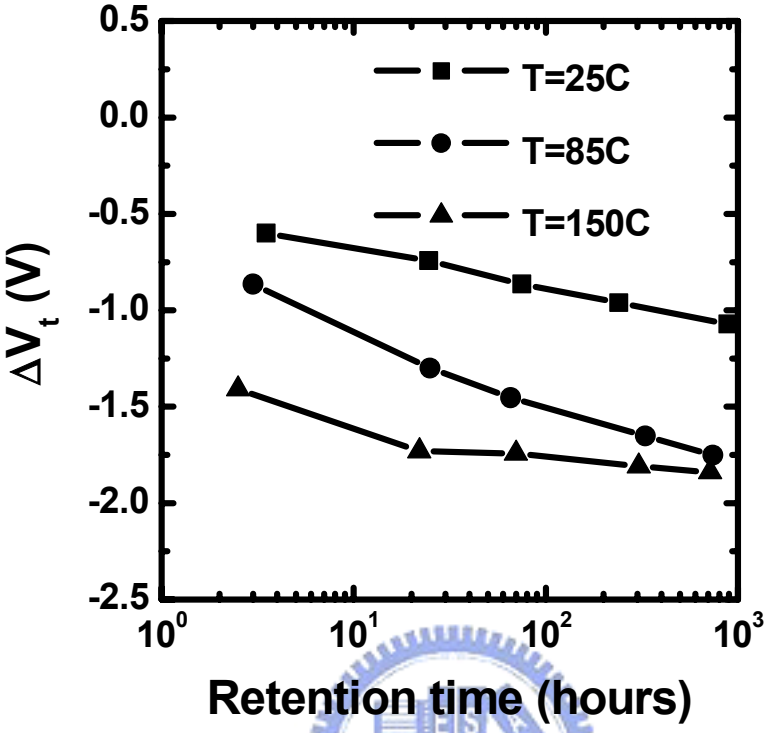


Fig.2.17 $\Delta<V_t>$ by field acceleration versus cycle numbers in a product.



(a)

	fresh	100K P/E	After 20 hours 150C bake
$I_{cp,max}$(pA)	63	425	195

(b)

Fig.2.18 (a) Program-state retention loss versus time at different temperatures. (b) Charge-pumping current in a fresh and a 100K P/E cycled cells. The bake temperature is 150C.

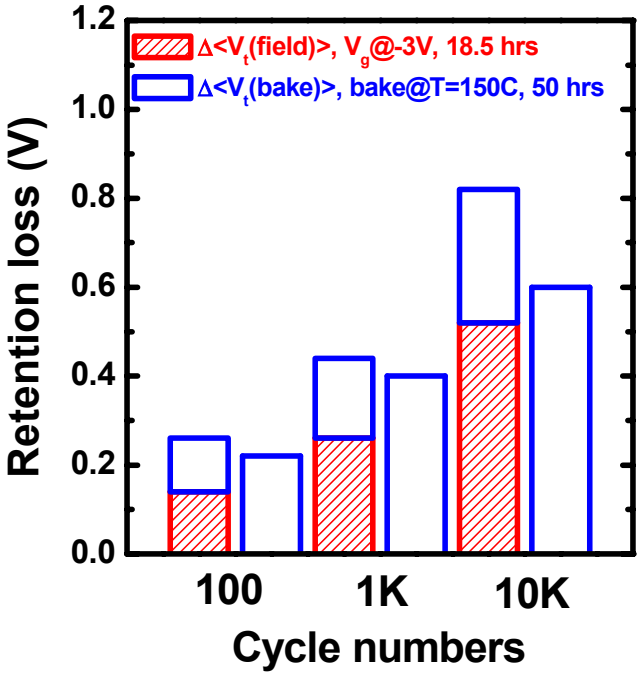


Fig.2.19 Overall retention loss of various cycled sectors by 150C, 50 hours bake ($\Delta<V_t(bake)>$) with and without a preceding field acceleration of V_g=-3V, 18.5 hours ($\Delta<V_t(field)>$).

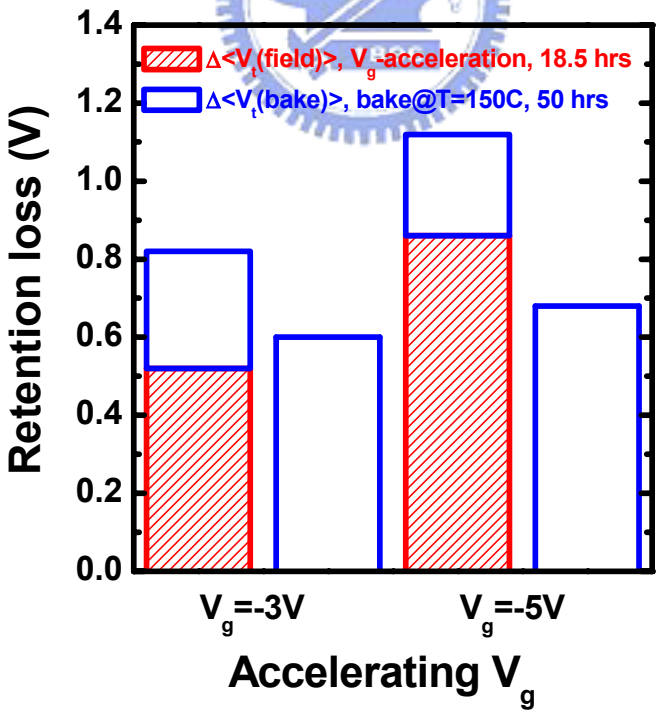


Fig.2.20 Overall retention loss of 10K cycled sectors by 150C, 50 hours bake ($\Delta<V_T(bake)>$) with and without a preceding 18.5 hours field acceleration of V_g=-3V and ñ5V ($\Delta<V_t(field)>$).

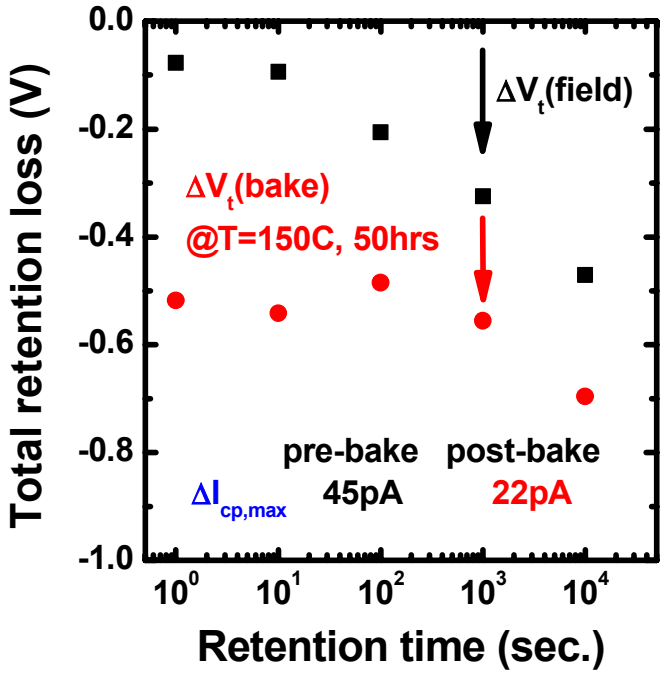


Fig.2.21 The retention loss of a 10K cycled cell, which is firstly accelerated by V_g=-3V for various time and then baked at T=150C for 50 hours, is recorded. The variation of $\Delta I_{cp,max}$ is also denoted.

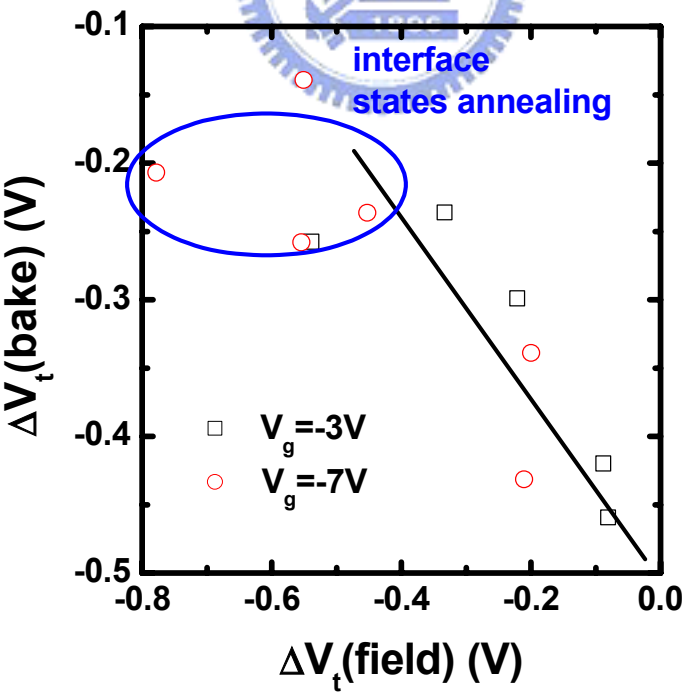


Fig.2.22 (Following) ΔV_t(bake) versus (preceding) ΔV_t(field) of 10K cycled cells. Bake is at 150C, 50 hours, and field acceleration is done by V_g=-3V and ñ7V with various retention time.

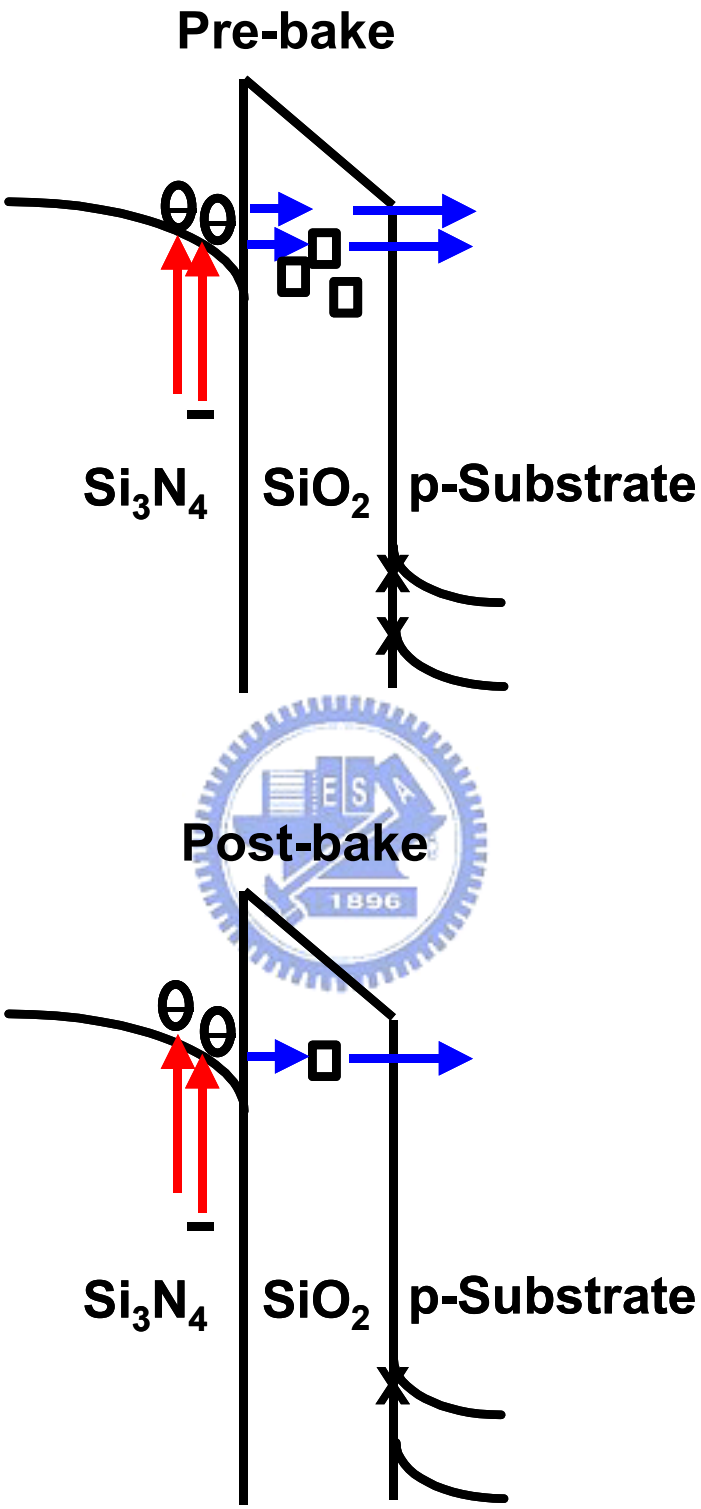


Fig.2.23 Roles of oxide trap and interface state in the retention loss of an NBit cell.

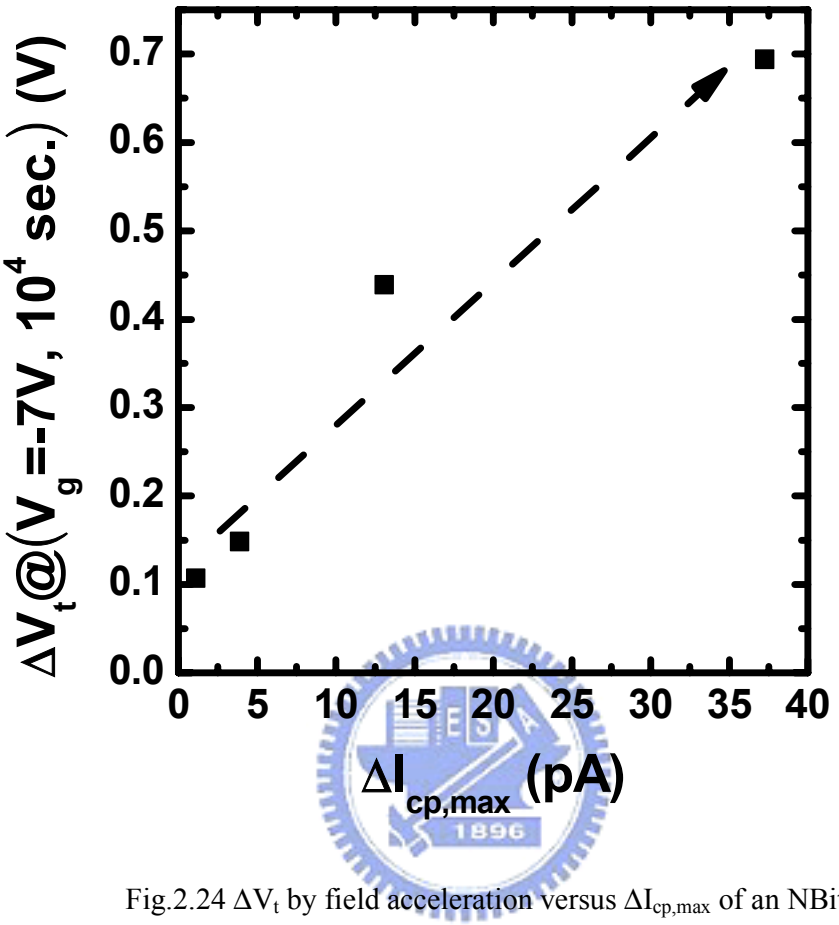


Fig.2.24 ΔV_t by field acceleration versus $\Delta I_{cp,max}$ of an NBit cell.

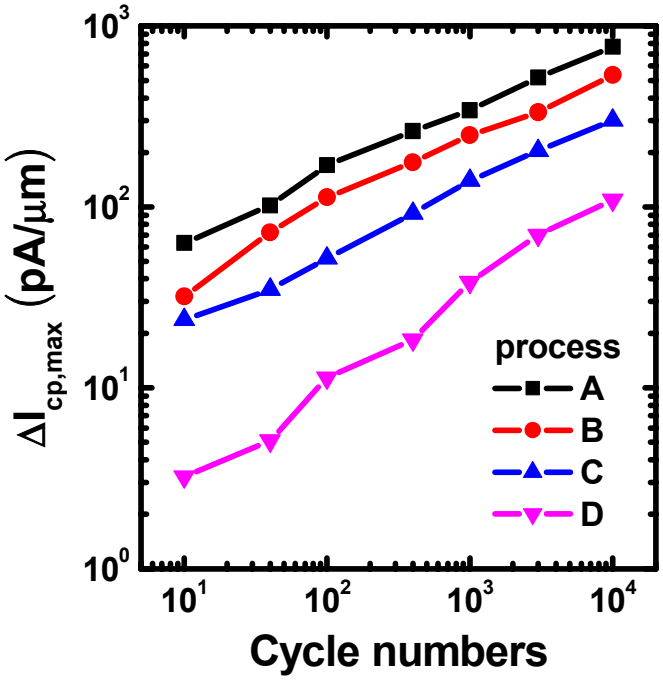


Fig.2.25 Normalized $\Delta I_{cp,max}$ versus cycle numbers of NBit cells fabricated by various process conditions.

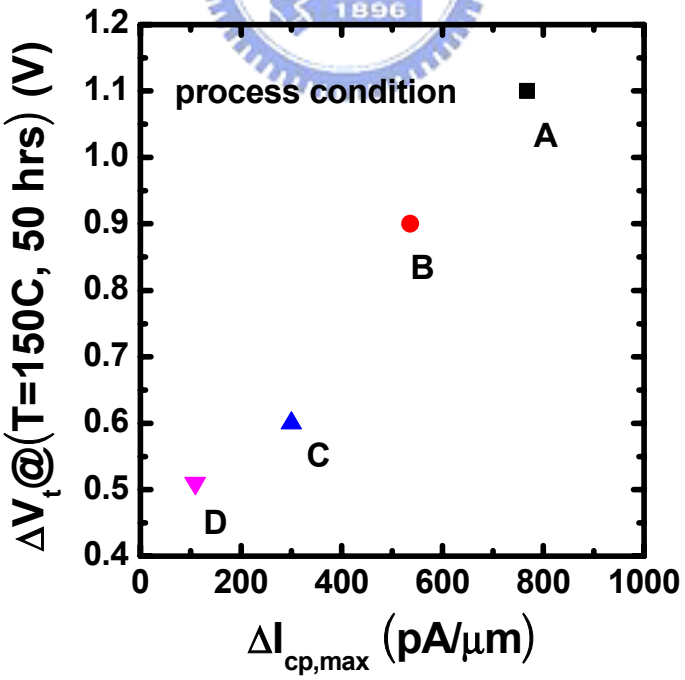


Fig.2.26 ΔV_t by high-temperature bake versus $\Delta I_{cp,max}$ of 10K cycled cells of various processes.

Chapter 3

Charge Gain in a Low-V_t Cell

3.1 Motivation

Charge loss of a program-state cell has been discussed in previous chapter, the next interest is: how about the V_t stability of an erase-state cell.

Firstly, letís look what happens in an erase-state cell after a period of ìdumbî storage. Fig.3.1 shows the V_t evolution of a fresh and a 1K P/E cycled NBit cells. It can be clearly found that V_t is kept unchanged in a fresh cell, however, a ìpositiveî V_t drift with logarithmic time dependence is observed in a cycled one.

Saifunís group has suggested that holes move laterally and the reversal of a ìdipole fieldî to explain such phenomena [3.1]. It is said that the injected holes (during erase operation) may mis-align the electron-storage location. Amounts of holes may accumulate inside the channel region. In the following retention time, these holes move laterally via trap-to-trap tunneling along the nitride toward the n^+ junction and cause the V_t drift-up.

We have studied the temperature effect on such V_t shift. It is found to be very insensitive to the bake temperature (Fig.3.2). It means that the physical mechanism is not dominated by a thermally enhanced process. Hole migration in the trapping nitride, which should be strongly dependent on the temperature [3.2], is not supported accordingly. We also applied the charge-pumping technique to explore the lateral extent of the stored charges before and after baking. The principle of this characterization is clearly explain in chapter 2. As shown in Fig.3.3, we do not observe any obvious distortion of the I_{cp} characteristic after an 85C, 4 hours baking, except for a little interface state annealing effect. From above, we donít think that lateral migration and re-distribution of the stored charges in the nitride layer is likely. The next question is: what is the dominant physical mechanism?

3.2 Experimental

In addition to the enhanced V_t drift-up after P/E cycling, the amount of V_t shift shows a unique P/E cycling dependence (Fig.3.4). V_t drift-up does not increase with cycle numbers monotonically, it shows a maximum value as the cell undergoes 1K~10K P/E cycles. This turn-around feature is similar to the build-up of positive

oxide charges during gate oxide stress experiment in a conventional MOSFET [3.3]. It is also reported that the positive oxide charge creation is dominant during the initial period of P/E stress in a floating-gate Flash memory cell [3.4-3.5]. The appearance of the peak strongly implies that the V_t drift-up is related to positive charge generation in the bottom oxide.

We further study the local charge polarity of an erase-state cell after P/E cycling. The gate-induced drain leakage (GIDL) current [3.6] and the V_t of a fresh cell and of a P/E stressed cell are measured (Fig.3.5 (a)). From the changes of GIDL current and V_t, it can be deduced that after P/E stress the ONO layer above the n^+ drain region should possess net positive charges while the ONO layer above the channel has net negative charges in our P/E operation. It means that holes and electrons co-exist in the ONO stack. Fig.3.5 (b) gives a schematic representation of the residual charge configuration of an erased NBit cell after P/E cycling corresponding to Fig.3.5 (a).

3.3 Charge Gain Model

The charges involved in the process include the residual electrons in the trapping nitride that do not recombine with the injected holes, and the hole traps in the bottom oxide which are created by P/E stress and are charged positively via erase operation. During the storage period, these positive trapped charges can escape from the bottom oxide to the substrate via tunneling. It introduces a substrate current I_h (Fig.3.6). The total ONO charges in the channel region therefore becomes more negative as time goes by. It results in the observed V_t drift-up. The reason that we propose the tunneling process is due to its insignificant dependence on the bake temperature. And the involved positive charges do not reside in the nitride is due to the thick bottom oxide (6nm) prevent the nitride hole back tunneling occurring in a conventional SONOS cell [1.35] and since the V_t may start to drift within 10us in our case [3.1].

Based on the tunnel front model [3.7] and assuming that the stress-induced oxide trap density has a uniform distribution along the bottom oxide, the hole detrapping current can be derived as [3.8]:

$$I_h \propto \frac{N_{ox}}{t} \qquad (3.1),$$

and the V_t drift due to I_h would be:

$$\Delta V_t(t) \propto \Delta Q_{ox} \propto \int I_h dt \propto N_{ox} \log(t) \qquad (3.2).$$

N_{ox} represents the positive oxide trap volumtric density and is assumed to be a constant value. The logarithmic dependence of V_t evlution is deduced and is consistent with the experiment results. Insensitive temperature effect is also expected by this model.

3.4 Results and Discussions

We use a charge separation technique (Fig.3.7) to monitor the I_h [3.9]. An ONO capactor is used to emulate the cell characteristics.The measured $I_g(=I_{sd}+I_b)$ and $I_b(=I_h)$ are plotted in Fig.3.8. Note that the positive oxide charge detrapping current ($I_h=I_b$) follows 1/t time dependence as predicted by our model (Eq. (3.1)). This finding provides a direct evidence that the erase-state V_t drift is related to positive oxide charge tunnel detrapping.

As shown in the model (Eq. (3.2)), V_t drift is also proportional to N_{ox}. Large area devices fabricated with two different ONO processes (A and B) are compared. Process B is known to have better oxide endurance. The substrate current (I_b) before and after an FN stress was measured in these two samples. Fig.3.9 shows that the post-stress substrate current follows 1/t time dependence. Note that process B exhibits a smaller post-stress substrate current because of less positive oxide charge creation. The corresponding V_t drift in a 10K P/E cycled NBit cell is shown in Fig.3.10. Process B has indeed a smaller V_t drift than that of process A. A well correlation between the V_t drift and I_b is obtained. It means that we can use I_b as a good indicator of the quality of the bottom oxide and the amount of the Vt drift-up.

3.5 Summary

In erase state, a V_t drift-up with storage time is observed after P/E cycling. Tunnel detrapping of the positive oxide charges created in the bottom oxide during P/E stress is the cause. ONO process condition is critical to improve the cell reliability. By charge separation technique, I_b is a direct indicator of the quality of the bottom oxide and the amount of the V_t drift-up.

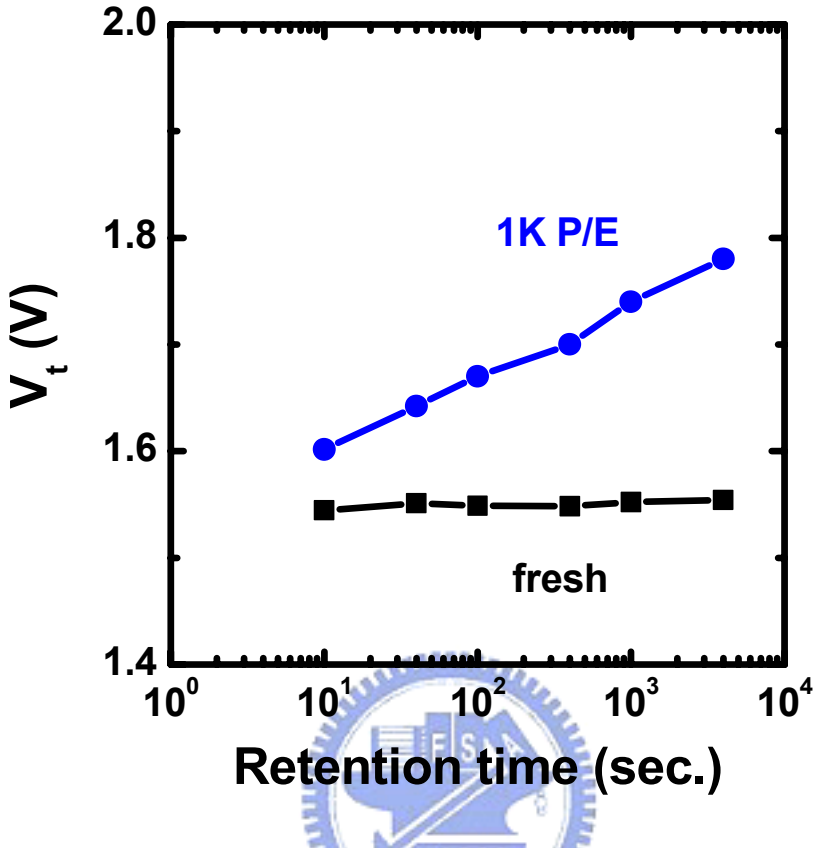


Fig.3.1 Erase-state V_t drift versus retention time of a fresh and a 1K P/E cycled NBit cells.

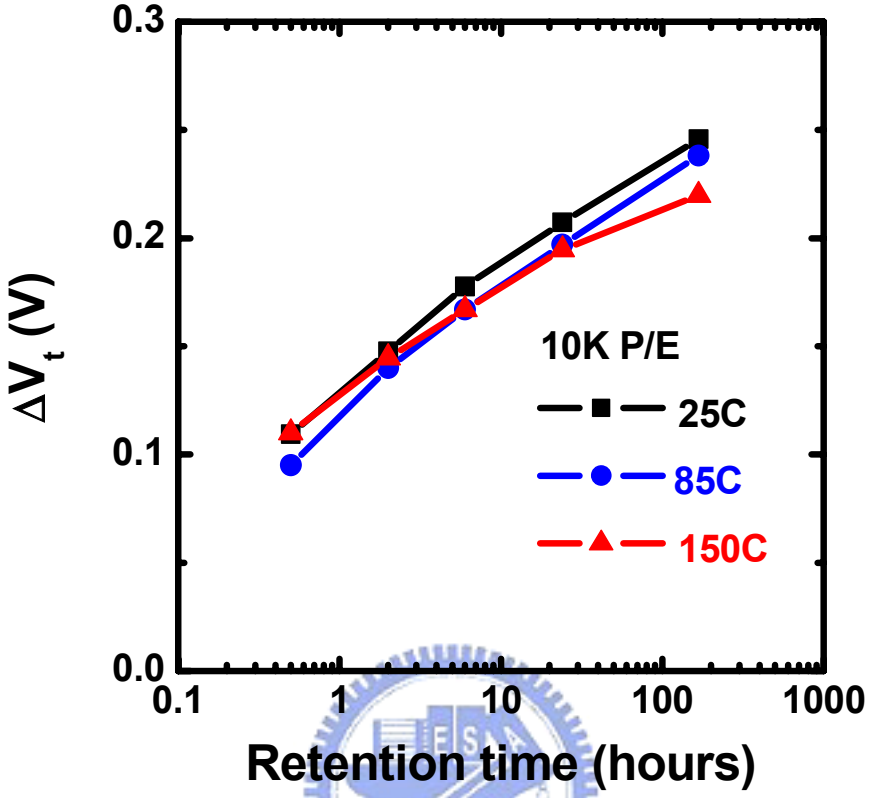


Fig.3.2 The V_t shift versus the retention time of 10K P/E cycles cells in erase state. The bake temperatures are 25C, 85C, and 150C.

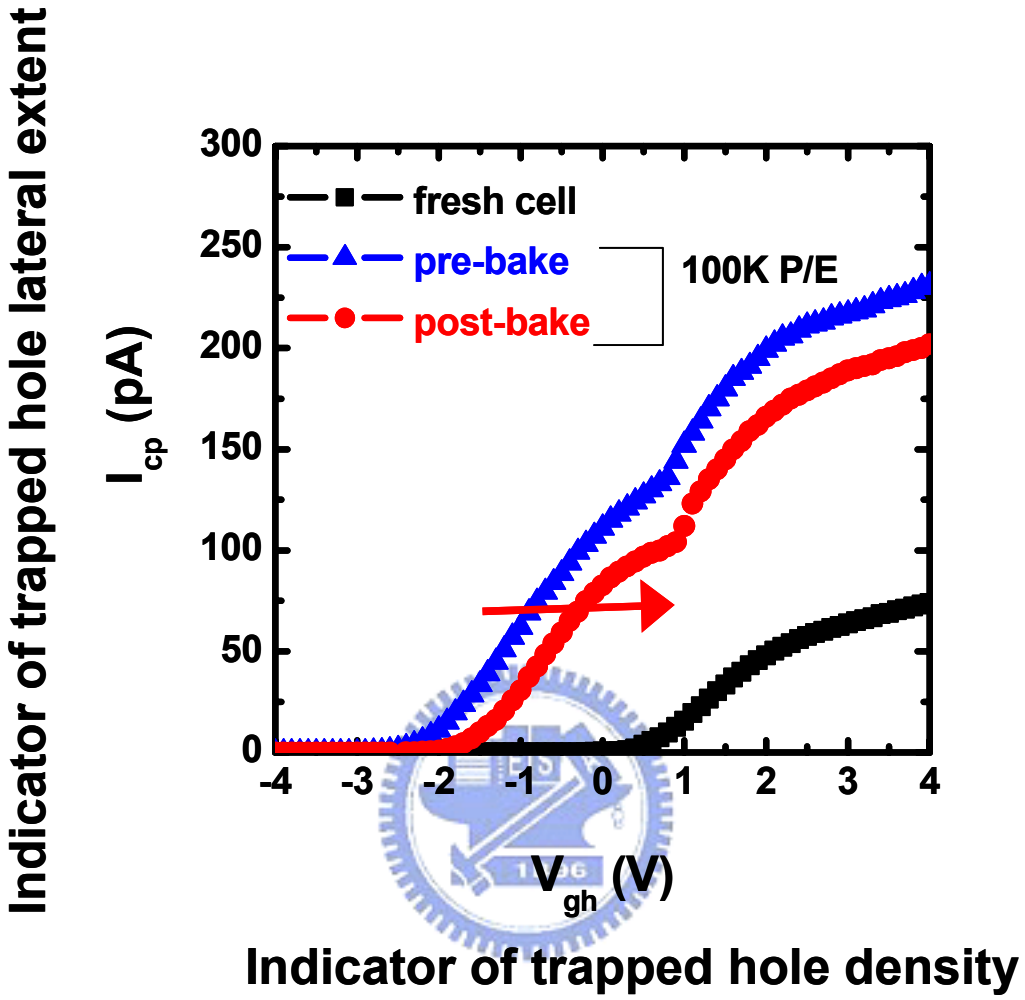


Fig.3.3 The measured I_{cp} versus V_{gh} of a 100K P/E cycles cell in erase state. The bake time is 4 hours and the bake temperature is 85C.

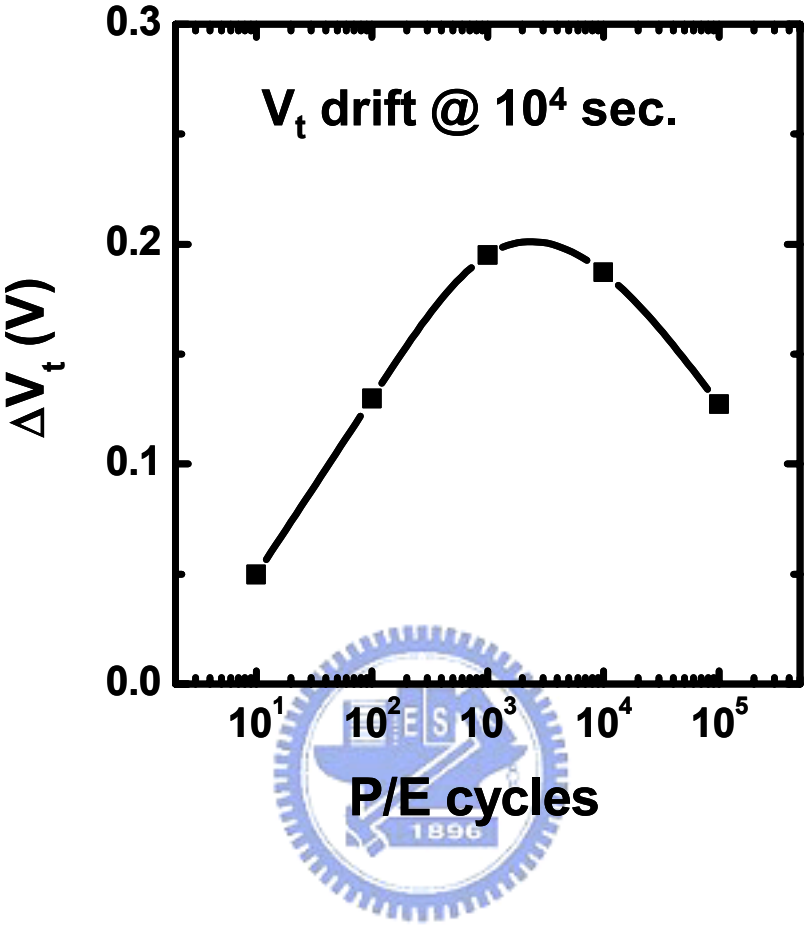
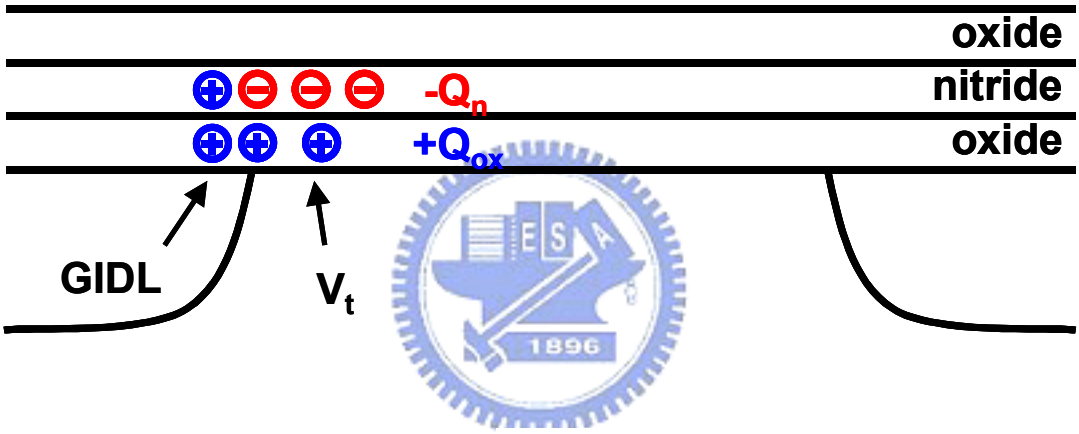


Fig.3.4 P/E cycling dependence of erase-state V_t drift after 10^4 sec. storage.

	Fresh	1K P/E	Net charge
V_t (V)	1.195	1.354	negative
GIDL (pA)	27.91	23.45	positive

(a)



(b)

Fig.3.5 (a) The measured V_t and GIDL current of a fresh and a 1K P/E cycled NBit cells. (b) Proposed charge configuration according to the results in (a).

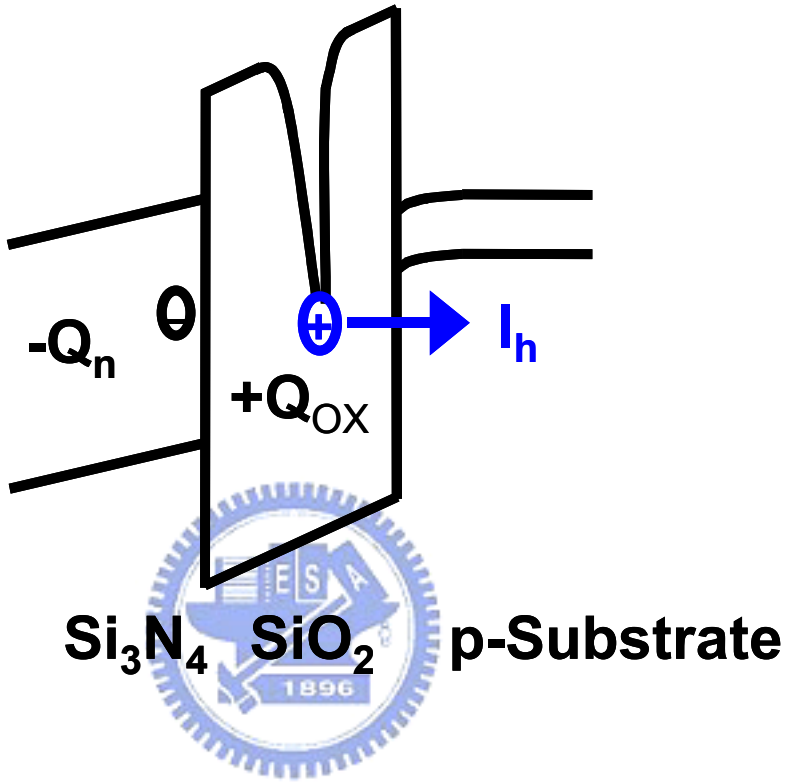


Fig.3.6 Schematic band diagram illustrating the positive oxide charge detrapping current (I_h) in an NBit cell.

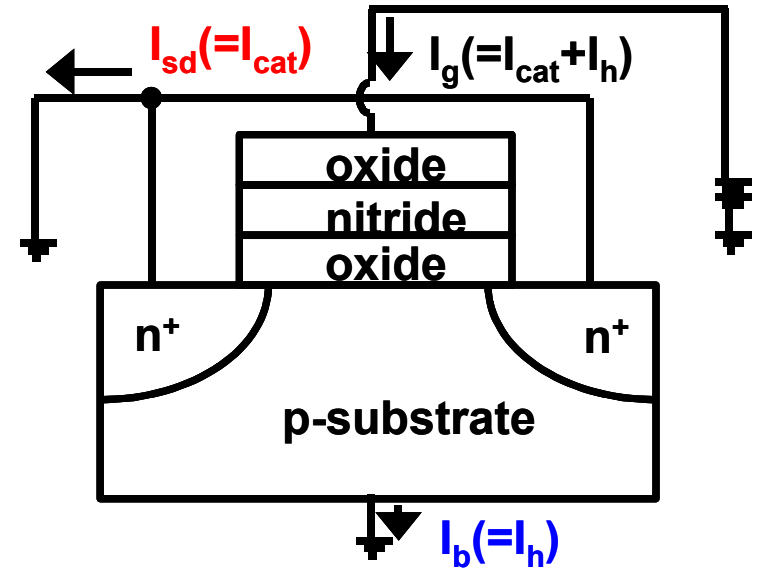


Fig.3.7 Illustration of a charge separation technique. I_{sd} is an electron leakage current and I_b is a hole leakage current.

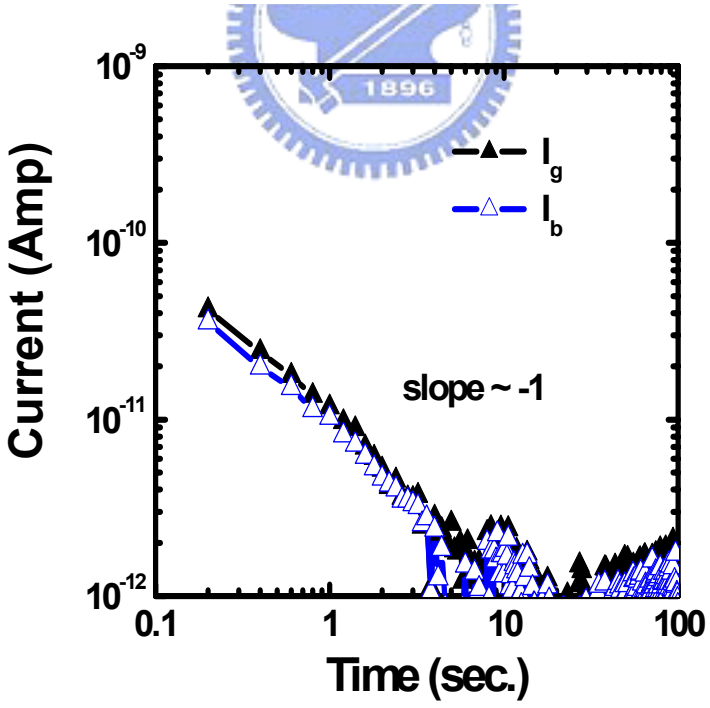


Fig.3.8 The measured I_g and I_b transients in an ìerase-stateî capacitor. The capacitor has a large gate area (2.5×10^5 μm^2). $V_g=V_{fb}$ in the measurement.

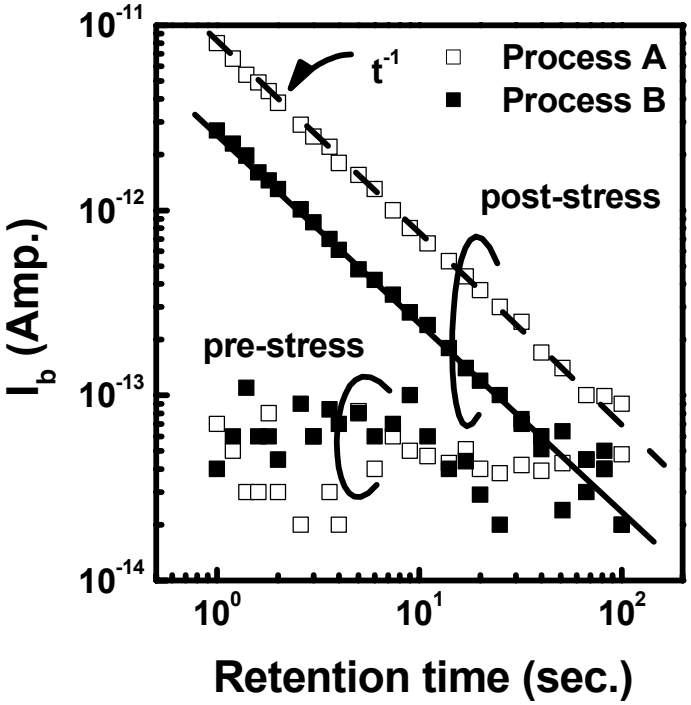


Fig.3.9 Pre-stress and post-stress substrate currents in two large area devices (500μm ㄨ 500μm). The FN stress condition is V_g = -18V for 3000s. Substrate current was measured at V_g=V_{fb}.

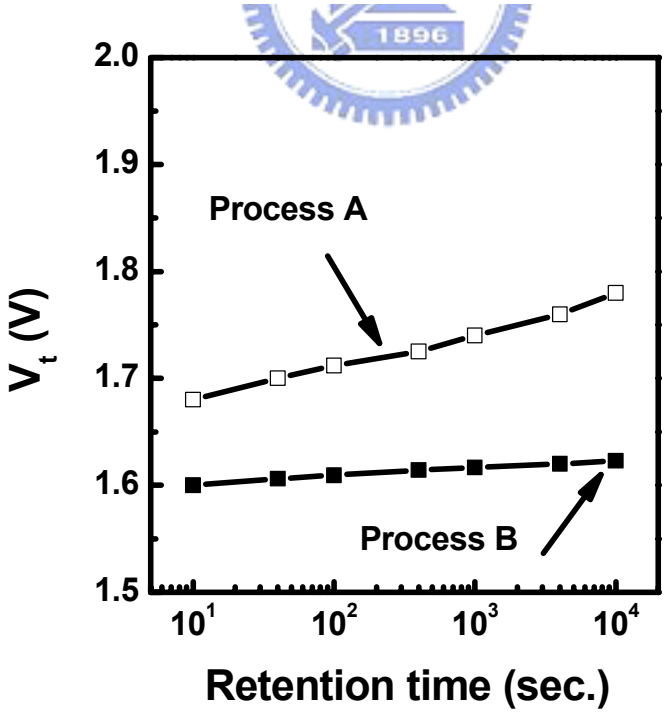


Fig.3.10 Room-temperature V_t drift versus time in two 10K P/E cycled cells fabricated with different ONO processes. The cell size is L_g=0.5μm and W_g=0.35μm.

Chapter 4

Excess-Hole Effect in an Over-Erased Cell

4.1 Motivation

In the previous chapter, we have clarified the cause of the V_t drift-up of an erase-state cell. We also observe that the V_t of an erase-state cell may goes more and more lower during the storage period. In Fig.4.1, the lowest bound of the erase-state V_t distribution versus the cycle numbers is shown before and after baking at 150C for 168 hours. The sample size of the distribution is a ì sectorî which has 512K cells. It is found that the V_t shifts toward a lower value after baking, and it is more severe after P/E cycling. It may induce an increasing bit-line leakage current and would cause malfunction of read operation, especially for scaled cells. In the following sections, we would address this issue.

4.2 Experimental

4.2.1 Device Samples and Characterization Techniques

An NBit cell with L_g=0.46μm and W_g=0.38μm, which is the same as the unit cell in the 512K array, is also used in the study. Two characterization methods are utilized here (Fig.4.2). The first one is the charge-pumping technique [2.5], which has been clearly explained in chapter 2. As shown in Fig.4.2 (b), we define a parameter V_{cp} to be the gate voltage (V_{gh}) that results in a collected charge-pumping current of 1pA. It is the indicator of the trapped charge density and polarity above the channel region. Another parameter, V_{btbt}, is defined as the negative gate voltage that induces a GIDL current of 100pA at V_d=2.5V (Fig.4.2 (c)). It indicates the GIDL current modulation by the trapped charges above the n^+ junction region. In other word, trapped charge density above the channel region and above the n^+ junction region are monitored by V_{cp} and V_{btbt}, respectively (Fig.4.2(a)). Their evolutions also mirror the charge density variation with storage time.

4.2.2 Characterization Results

Moreover, we plot the required erase time, corresponding to Fig.4.1, at each specified cycle number in Fig.4.3. The erase time increase with increasing P/E cycle numbers.

We use a single cell trying to emulate such effect. Fig.4.4 shows the V_t shift by each erase shot of a fresh cell and a P/E cycled cell. Erase speed indeed gets slower after P/E cycling. We also extract the corresponding V_{btbt} after each erase shot (Fig.4.5). V_{btbt}ís of the fresh and the cycled cells almost coincide with each other between shot-4 and shot-7. It means that the hot-hole injection efficiency does not degrade after P/E cycling. The initial discrepancy (before shot-3) indicates fewer electrons are stored above the n^+ junction of a program-state cell after P/E cycling. The degraded erase speed is due to the enhanced mis-alignment between the programmed electrons and the injected holes. More ì farî electrons, which are harder to be ì erasedî, are prone to be injected after P/E cycling. In order to compensate the residual electrons near the central channel region, more holes are injected. It results in the increasing erase shots (9 shots v.s. 7 shots for a fresh cell) and the more negative V_{btbt} (-6.6V for a P/E cycled cell v.s. ñ5.7V for a fresh cell) after cycling. Erase speed degradation will be discussed more comprehensively in chapter 6.

We also study the temperature effect on the V_t drop-down. As shown in Fig.4.6, V_t drops more seriously at higher temperature. Here, we use a cell with intentionally extra erase shots to emulate the excess-hole pile-up at the n^+ junction (Fig.4.5). It is thus dominated by a thermally enhanced mechanism, which is quite different from the V_t drift-up phenomena discussed in chapter 3.

A charge-pumping measurement is applied to compare the charge density and lateral extent variations before and after baking. Once again, to emulate the increasing erase time and excess hole injection over the n^+ junction and to avoid the interface state generation after P/E cycling and their annealing during baking, a fresh cell is intentionally over erased by 30 erase-shots. Its charge-pumping characteristics are shown in Fig.4.7. The pulse frequency is 2.5MHz. As indicated in the figure, a considerable amount of holes is trapped in the nitride layer above the channel after erase. It causes a leftward shift of the low V_{gh} portion (for $V_{gh}<0V$) of the I_{cp} characteristic [2.5]. The cell is then baked at 150C for different time. A crossover of the I_{cp} characteristics before and after baking is observed. We can see that the low V_{gh} portion ($V_{gh}<-1V$) of the I_{cp} curve shifts rightward along with bake time. It indicates that the trapped hole density near the edge side decreases. In addition, I_{cp} increases

between V_{gh}=-1.5V and V_{gh}=-0.5V. We believe that this increment of I_{cp} is caused by the lateral spread of the trapped holes and thus the enlarged ì locally low-V_tî area.

To further verify this idea, another indictor, the corresponding V_{btbt} (Fig.4.2 (c)), is used to explore the variation of the trapped charge density. In Fig.4.8, a positive linear correlation is found between V_{cp} and V_{btbt}. This provides another evidence that the trapped hole density was decreasing with increasing bake time. It also means that both V_{cp} and V_{btbt} can be monitors of the evolution of trapped hole density in the nitride.

We summarize the experimental results related to the V_t drop-down in an erase-state cell. The V_t drop-down is more obvious after P/E cycling, especially for a cell belonging to the low bound of the low-V_t distribution. Such a cell is stored with excess holes. And the V_t drops more seriously at higher baking temperature.

4.3 V_t Drop-Down Model

We thus propose the model to explain the V_t drop-down. Excess holes are injected in a cycled cell during the enlarged erase period. While storage, trapped holes firstly emit from the traps and then are laterally driven by an internal field and are re-captured by other traps. The hole emission is a thermally enhanced process which explains the temperature effect. These holes eventually move along the nitride toward the central channel region. It causes the channel shortening effect and the observed V_t drop-down (Fig.4.9).

Since the V_t loss is due to the channel shortening effect, which is a complicated 2-D effect, it cannot be directly correlated to the change of the locally trapped hole density. For example, with the same degree of hole lateral migration, the cellís V_t is not affected in a long-channel device while it is significantly reduced in a short-channel one. Therefore, the V_{btbt} and the V_{cp}, which are more sensitive to a local charge variation, are suggested to be the indictors of the temporal evolution of these holes. Fig.4.8 have shown the consistency between V_{cp} and V_{btbt}. We would choose V_{btbt} as the monitor in the following discussion since it is more easier to be measured.

According to the thermionic emission model, the emission time constant τ_{hn} of a hole in a nitride trap of energy depth of ϕ_{hn} above the nitride valence band edge can be described as [4.2-4.3],

$$\tau_{hn}(\phi_{hn}) = \frac{1}{AT^2}\exp(\frac{\phi_{hn}}{kT}) \quad (4.1),$$

where

$$A = 2\sigma_{hn}(\frac{3k}{m^*})^{1/2}(\frac{2\pi m^* k}{h^2})^{3/2} \quad (4.2).$$

Here σ_{hn} is the capture cross-section of traps and m* is the effective hole mass in the nitride. If we assume the trap energy is continuous in the energy spectrum and the trapped hole density is uniformly distributed within the nitride with a volumetric density of N_{hn0}, the emitted holes could be derived as:

$$\Delta Q_{hn} \propto \int J_{hn}dt \propto \iint \frac{N_{hn0}\exp(-t/\tau_{hn})}{\tau_{hn}} d\phi_{hn}dt \propto N_{hn0}kT\log(t) \quad (4.3).$$

Eq. (4.3) indicates that the amount of holes that involved in the re-distribution is linearly dependent on log(t) with a slope proportional to the temperature. V_{cp} and V_{btbt}, which is proportional to ΔQ_{hn}, would follow the same dependence accordingly.

4.4 Results and Discussions

In Fig. 4, the ΔV_{btbt} versus bake time at various temperatures is plotted. All curves are straight lines on a semi-log plot. By utilizing Eq. (4.2) and Eq. (4.3) and using the results at T=150C to calibrate the parameters, the measurement data under T=120C and T=85C can be successfully matched. The extracted capture cross-section of holes is about 1×10^{-17} cm^2. In calculation, $m^*=0.5m_0$ is used. Based on this result, we may reach an accelerating test condition for such V_t drop-down phenomena. The required time for a hole emitting from a nitride trap of depth of ϕ_{hn} at different bake temperatures can be related by utilizing Eq. (4.1), by which

$$\phi_{hn} = \ln[AT_1^2 t(T_1)]^{kT_1} = \ln[AT_2^2 t(T_2)]^{kT_2} \quad (4.4),$$

and then

$$t(T_1) = \frac{1}{AT_1^2}[AT_2^2 t(T_2)]^{kT_2/kT_1} \quad (4.5).$$

Accordingly, the accelerating time that performs at T=150C needs to be at least 114 hours to meet the 10 years guarantee at T=85C.

4.5 Summary

A negative V_t shift is found to increase with storage time in a cycled cell at erase state. Lateral spreading of excess-trapped holes is the root cause. It will result in the channel shortening effect that induces the observed negative V_t shift. It may be a potential issue for future device scaling. According to thermionic emission model, the amount of holes involved in the re-distribution is linearly dependent on log(t) with a slope proportional to the temperature. The extracted hole capture cross section is about 1×10^{-17} cm^2. Therefore, to guarantee a 10-year reliability at T=85C, accelerating test at T=150C for 114 hours is the minimum requirement.

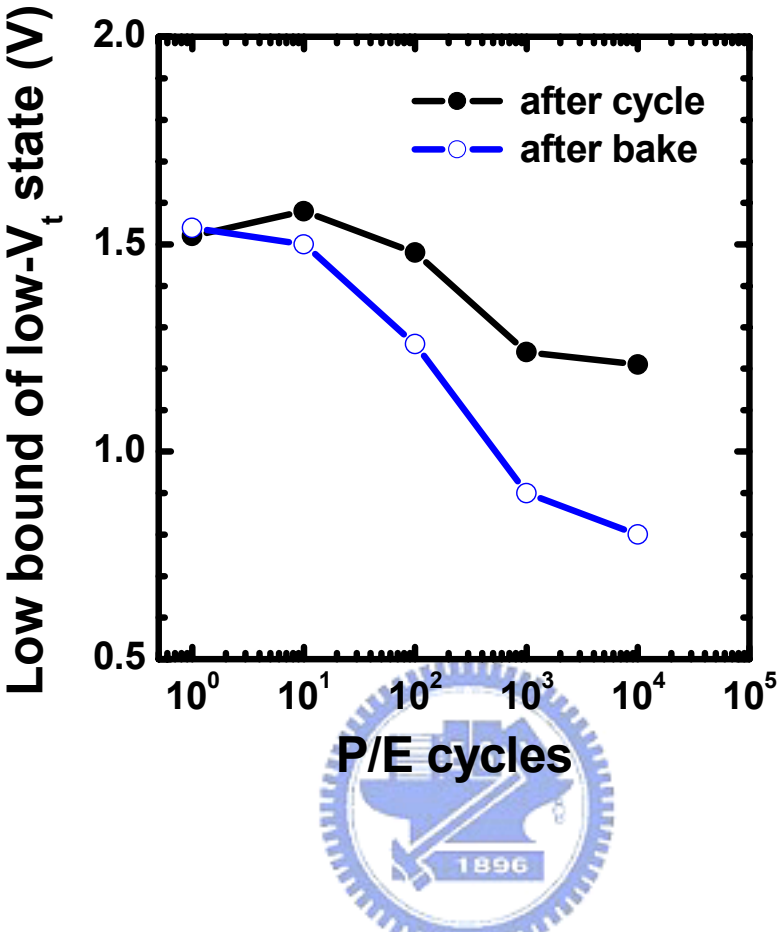
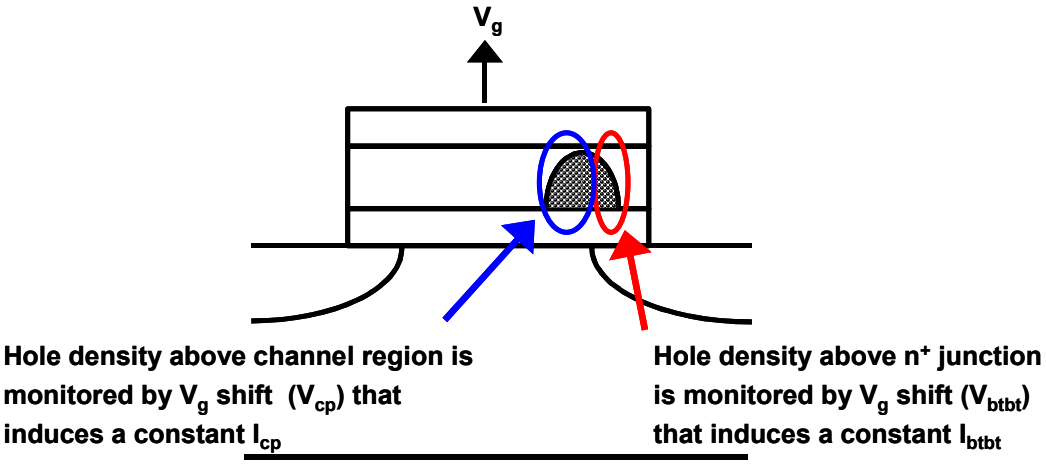
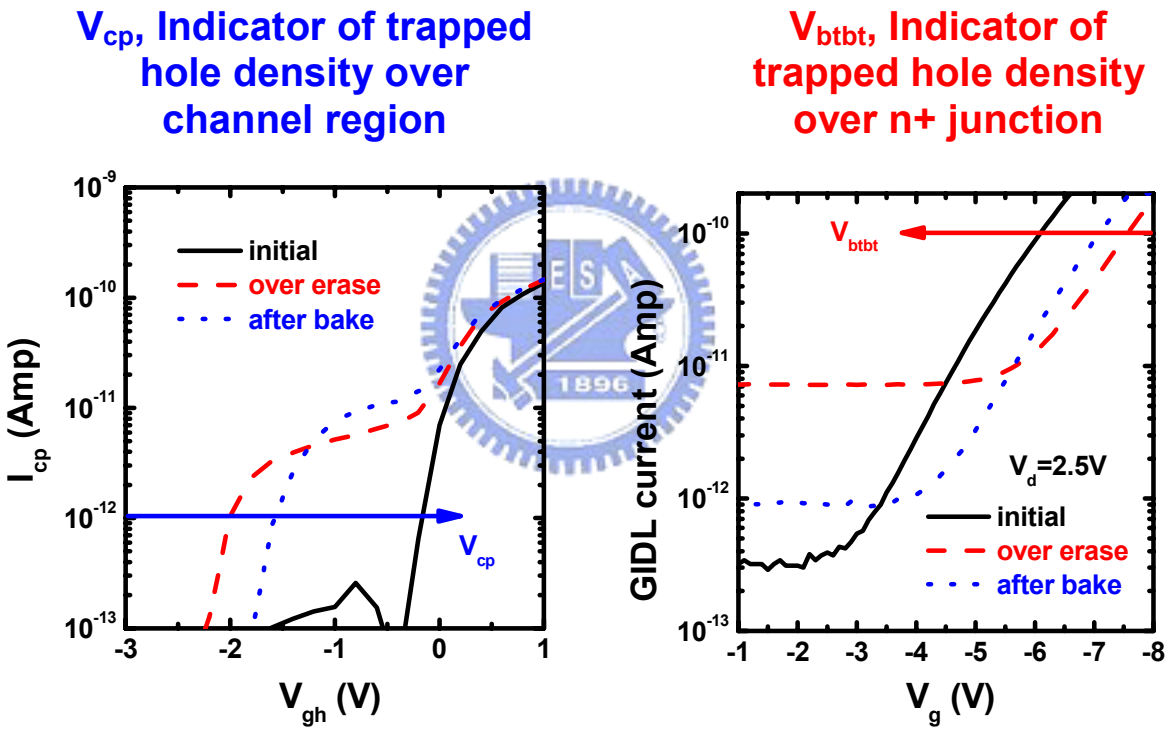


Fig.4.1 The low bound of erase-state V_t distribution versus cycle numbers before and after baking at 150C for 168 hours.



(a)



(b) (c)

Fig.4.2 (a) Concept of V_{cp} and V_{btbt} to estimate the stored charges above the channel and the n^+ junction, respectively. Charge-pumping characteristics (b) and GIDL current (c) are measured for a fresh NBit cell which is then over-erased and then baked at high temperature.

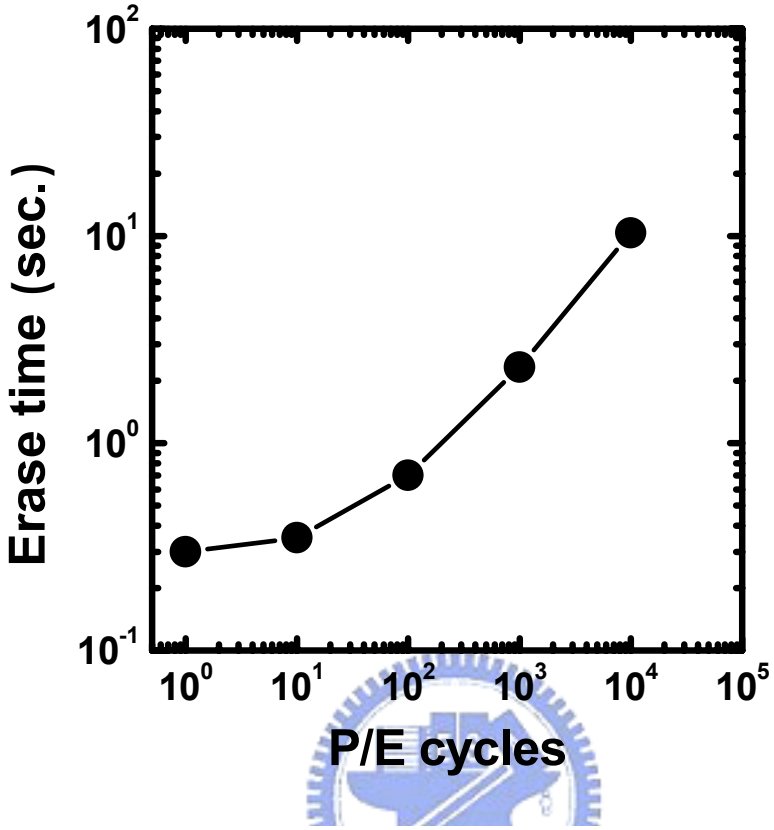


Fig.4.3 The required erase time versus cycle numbers corresponding to Fig.4.1.

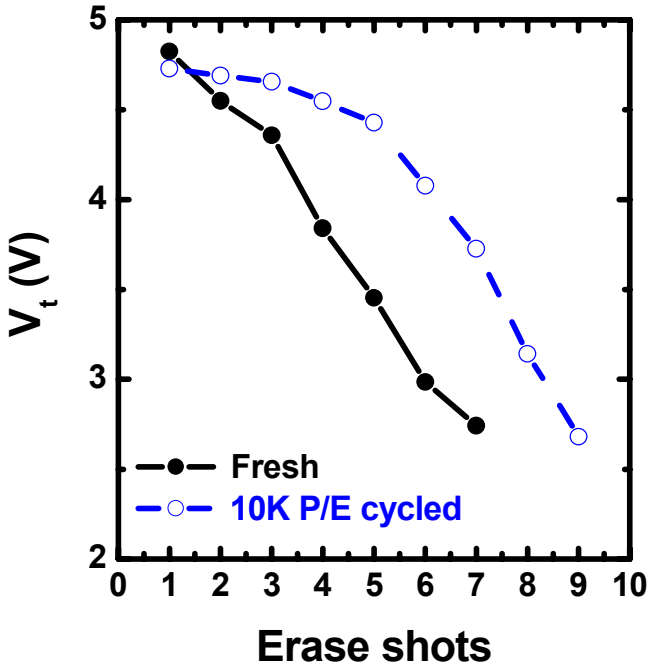


Fig.4.4 The required erase time versus cycle numbers of an emulating single cell.

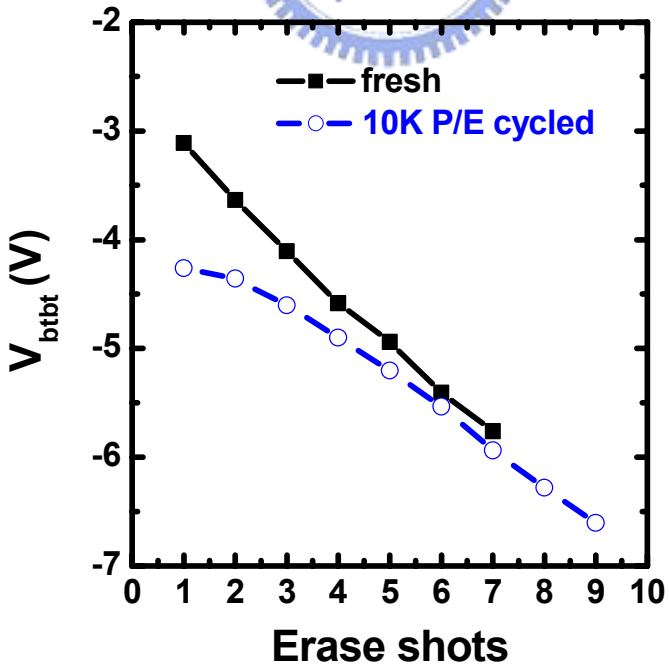


Fig.4.5 The extracted V_{btbt} versus cycle numbers corresponding to Fig.4.4.

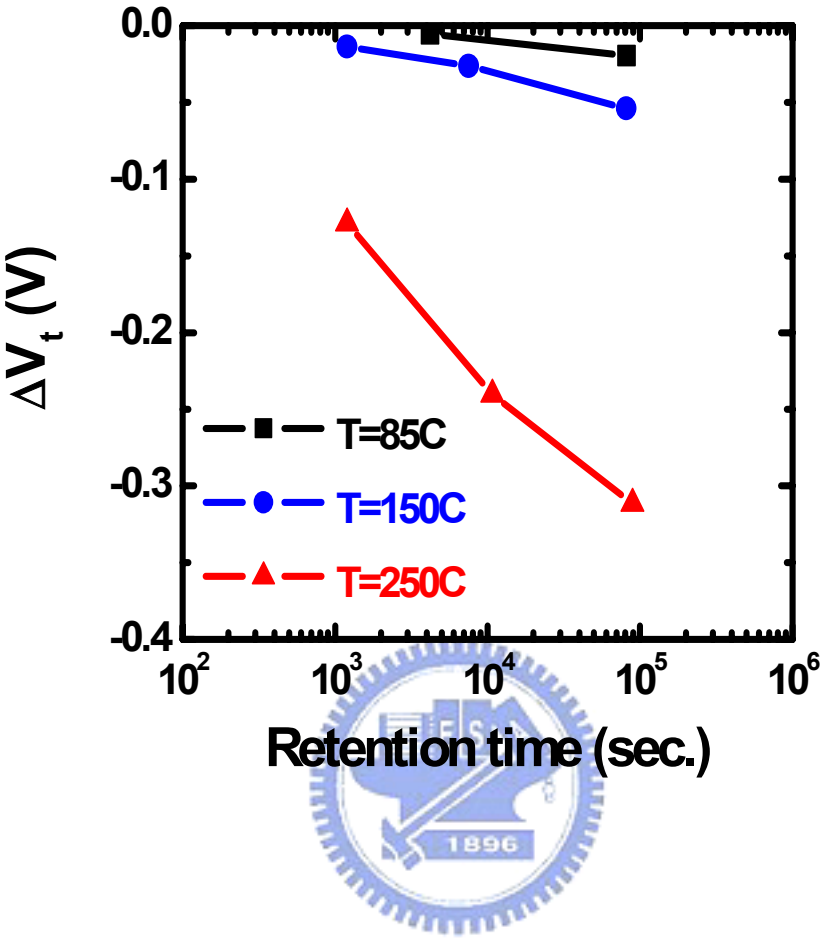


Fig.4.6 The evolution of V_t with the storage time in a strongly erased cell. The bake temperature are 85C, 150C, and 250C. A negative V_t shift is observed.

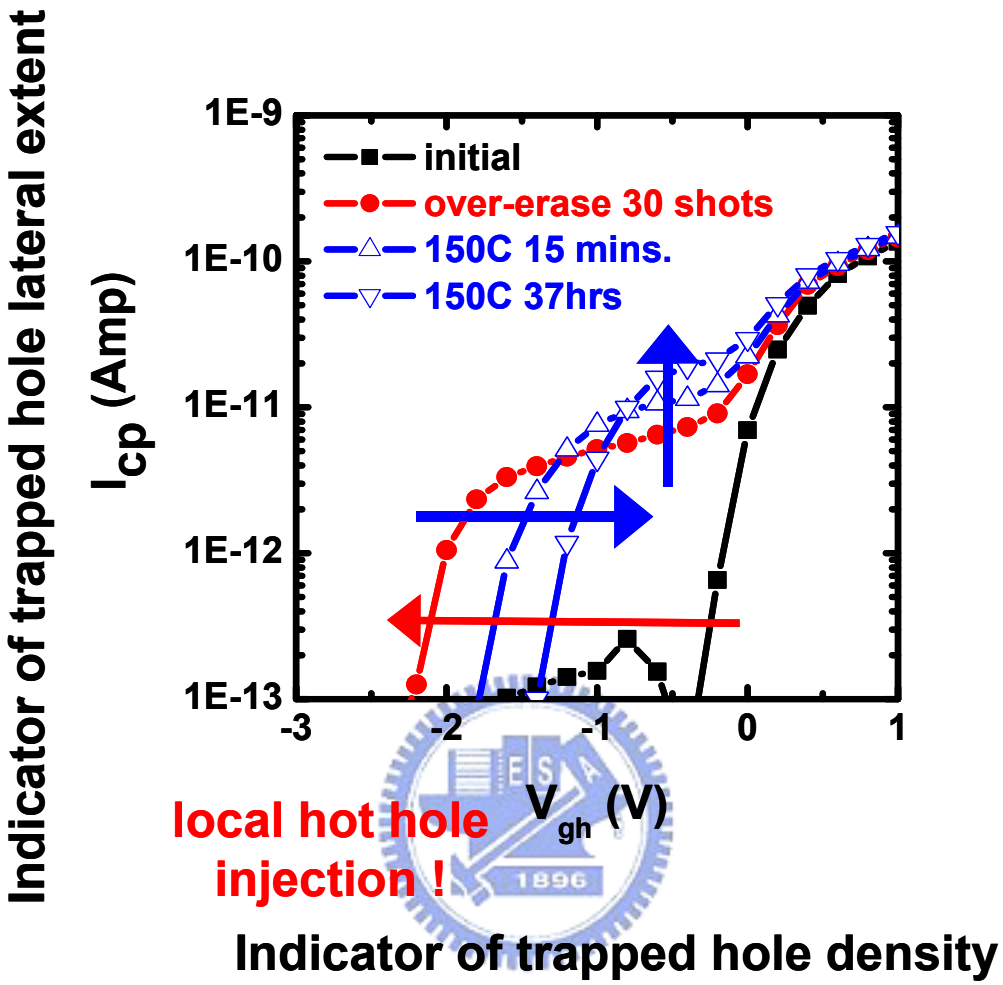


Fig.4.7 Charge pumping characteristics of an NBit cell which is erased by 30 shots and then is baked at 150C for 15 minutes, 3 hours, and 37 hours, respectively.

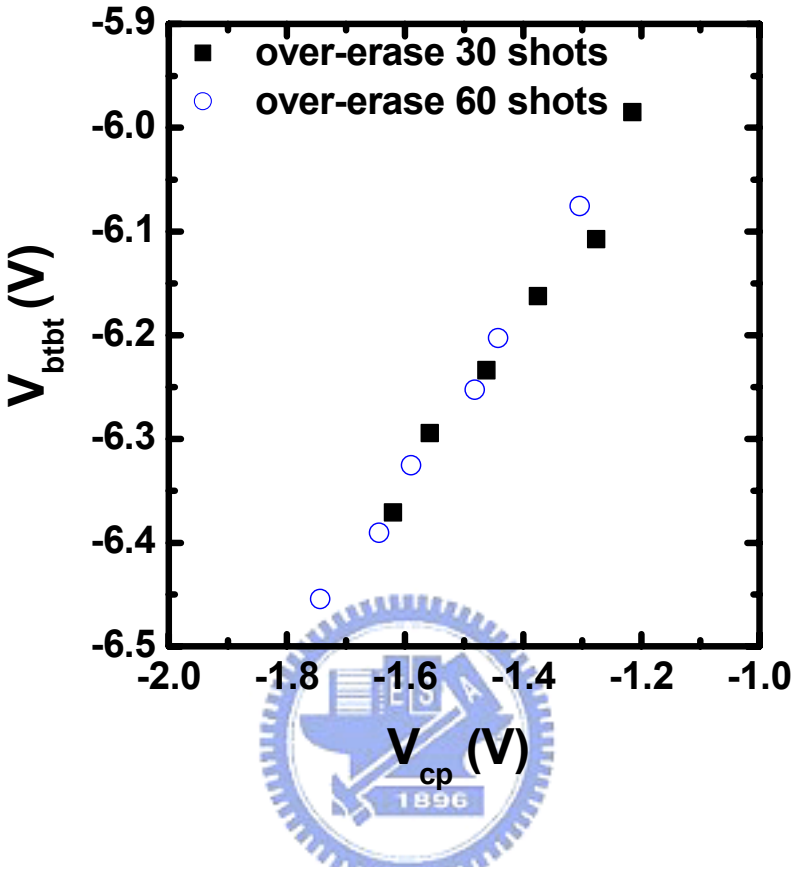


Fig.4.8 V_{btbt} is plotted against V_{cp}. A positive correlation is found between them.

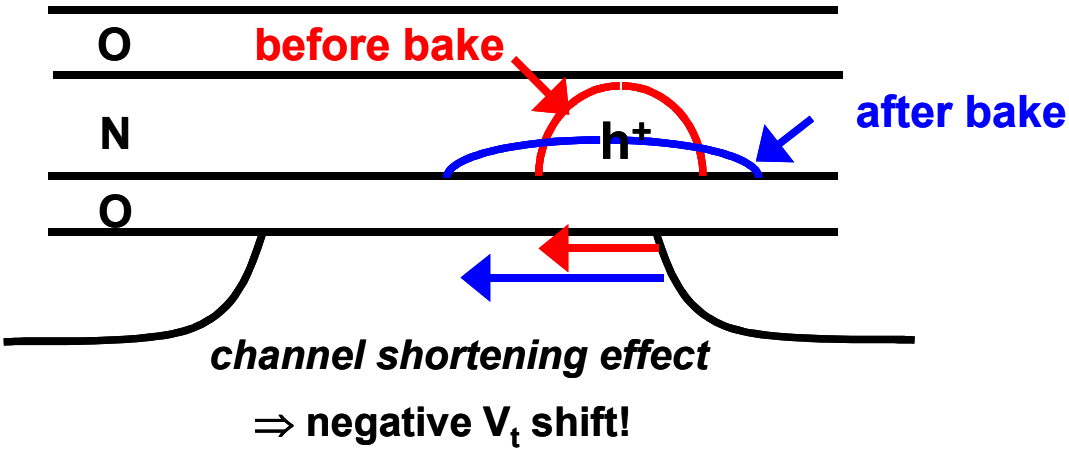


Fig.4.9 Schematic representation of the lateral spread of trapped holes and the resulting channel shortening effect that cause the negative V_t drift in an NBit cell.

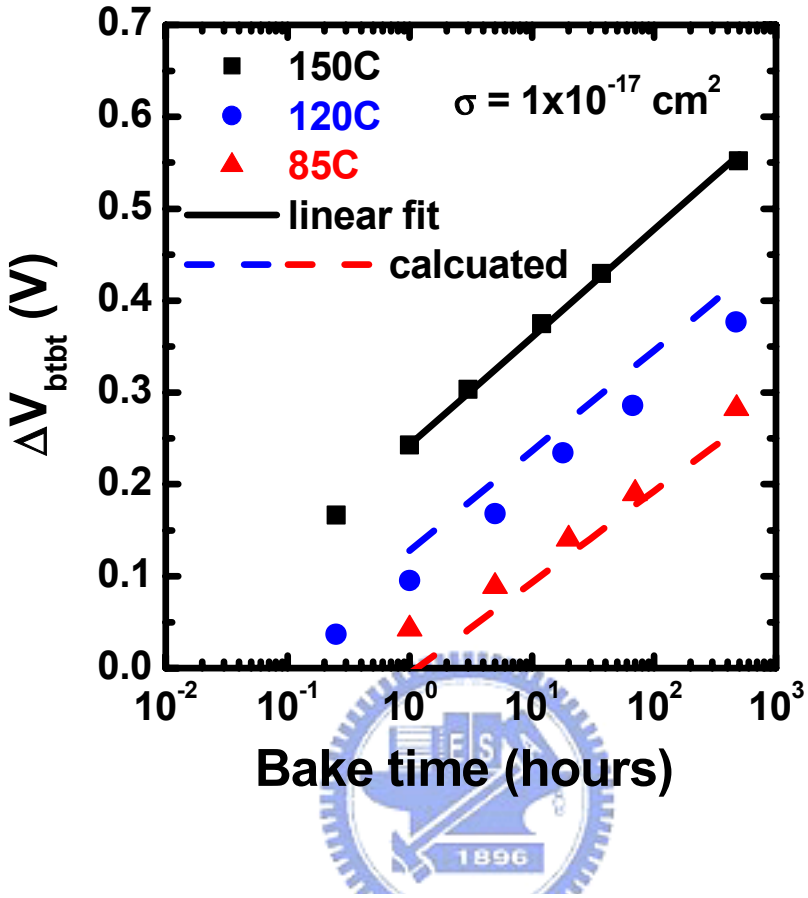


Fig.4.10 ΔV_{btbt} versus bake time at various temperatures. All curves follow a straight line on a semi-log scale. The lines represent the calculated results.

Chapter 5

Read Disturb

5.1 Motivation

We have discussed the data retention issues of the NBit cell in both program and erase states. Mechanisms responsible for the V_t instability after long-term storage are addressed in detail. Another source of V_t instability is due to read-induced disturb. It is a little different from what has been discussed in previous chapters. In previous retention tests, the cell is in ìpureî storage mode without any applied bias on the cell. However, data stored in a NVM cell is sensed over and over again for system applications. In other words, read biases are applied to the cell to induce signal corresponding to its bit state. In addition to the localized charge injection and the non-conducting property of the trapping storage material, the unique feature to realize two-bit-per-cell storage is a reverse-read scheme [5.1]. As depicted in Fig.1.2, a drain bias (V_d) is applied to read out the information stored at Bit-S. The applied V_d must be large enough to ìscreenî out the injected charges at Bit-D. The read current (or V_t) is then controlled by the charge state nearby the source side (Bit-S), almost regardless of the charges at Bit-D. Typically, the applied bit-line voltage during read is around 1.6V, which is higher than that in a floating-gate Flash memory cell (typically around 1V). Fig.5.1 shows the V_t shift of a 10K P/E cycled cell during read operation, whereas the V_t drift is not observed in a non-cycled cell. In the figure, the applied V_g and V_d are 2.5V and 1.6V, respectively. This V_t shift will degrade the operating-V_t window and result in the failure of read operation. In this chapter, we would like to find out the dominant mechanisms that cause such erase-state V_t instability during read operation.

5.2 Experimental

The cell used here is the same as that introduced in previous chapters. Devices with gate length from 0.5µm to 0.3µm and with initial-threshold voltage (V_{ti}, without any trapping charge) from 1.2V to 3V are characterized. The gate width is around 0.35µm. Temperature effect from ñ20C to 85C is studied.

Three read-related disturb modes are investigated for P/E cycled cells at erase state. In the first one, gate and drain biases are applied and the source is grounded. It

is the conventional read disturb (RD) mode. The second one has an applied gate bias and the source and drain are grounded. It is referred to as the gate disturb (GD) mode, which is to emulate the gate bias effect on cells sharing the same word-line with the cells to be read and on the in-series cells acting as pass gates in a NAND-type array. Finally, the ì room-temperatureî drift (RT) mode, in which the V_t drift is insensitive to temperature as discussed in chapter 3, is the special case where the cell is in ì un-biasedî storage (without any applied bias).

5.3 Modeling of Positive Oxide Charge Effect on Read Disturb

Fig.5.2 shows the V_t shift of a 10K P/E cycled cell in a two-phase measurement, e.g. RT and RD are measured in sequence, or vice versa. It is found that after RT (or RD), the following RD (or RT) is reduced. This gives us a hint that RT and RD may have the same cause since they influence each other. It also means that the V_t shift due to RD is dependent on the sampled time. Since positive oxide charge detrapping (with the co-existence of residual negative charges in nitride) has been clarified to be the major cause of RT (chapter 3), these positive oxide charges created during P/E cycling are considered to affect RD as well. It also explains the cycling effect on the observed erased-state V_t instability. Following the model proposed in chapter 3, we summarize the V_t drift models at various bias conditions and the corresponding time evolutions in Fig.5.3. In each case, the cycling-induced positive oxide charge plays a major role.

As the cell is stored without applied V_g and V_d (RT mode), tunnel detrapping of the cycling-generated positive oxide charges (J_h in Fig.5.3) is the dominant mechanism. According to the tunnel front model [3.7], this detrapping current follows t^{-1} time dependence. Its V_t evolution would have logarithmic time dependence ($\Delta Vt \propto \log(t)$). This phenomena has been clearly discussed in chapter 3.

If a sufficiently high V_g is applied, (e.g. for cells belonging to the same word-line of a selected-reading cell, GD mode), an inversion layer is induced beneath the gate. The positive oxide charges will cause the inversion electrons to tunnel into the trapping nitride at such high vertical field. According to the positive charge-assisted tunneling (PCAT) model [3.8], this injection current (J_{cat} in Fig.5.3) will follow a t^{-p} law where t is the elapsed time and p is around 0.7. The V_t shift thus has power-law time dependence t^n with $n=1-p\approx0.3$ via integrating J_{cat} ($\propto t^{-p}$) over the storage period.

For a read cell, to which the read V_g and V_d are applied (RD mode), channel electrons will be accelerated by the lateral field near the drain junction. Both the high drain field and the positive oxide charges will enhance electron injection into nitride. This positive oxide charge-enhanced hot-electron injection will cause a positive V_t drift with the same time dependence as GD, i.e. $\Delta Vt \propto t^n$ with n=0.3.

5.4 Results and Discussions

5.4.1 Bias Dependence of Read Disturb

Fig.5.4 shows the gate-disturb characteristics of a 10K P/E cycled cell. The applied gate bias is from V_g=0V (RT mode) to V_g=4V. It is found that V_t shift shows linear dependence on log(t) at V_g=0V. This has been well modeled by hole tunnel detrapping [3.8].

However, accelerated V_t drift, which exhibits power-law time dependence t^n, is observed at V_g=4V. It would be clear if we show the ΔV_t versus disturb time on a log-log plot, as indicated by the open square and the right-axis in Fig.5.4. Since the time evolution of the V_t drift would show power-law time dependence t^n if PCAT dominates, the accelerated V_t drift with its unique time dependence confirms that positive charge-assisted electron tunneling into the trapping nitride takes place at high vertical field, in addition to hole tunnel detrapping. A charge separation technique (Fig.3.7) is applied again to measure the I-t characteristics of a stress ONO capacitor (the principle and results have ever been discussed in chapter 3). The results are shown in Fig.5.5 (a) and (b). The measured I_b, which shows very weak dependence on the applied field and follows 1/t time dependence, provide the direct evidence of hole tunnel detrapping. I_{cat}, which represents positive oxide charge-assisted electron tunneling current [3.9] from the substrate to the nitride conduction band, occurs as V_g increases. It shows $t^{-0.7}$ time dependence. Both are consistent with the proposed models. The V_g dependence of ΔV_t is shown in Fig.5.6. Gate disturb may impose the limitation of the applied V_g on the read cell and on the cells acting as pass gates in a NAND-type array.

Fig.5.7 shows the RD characteristics of a 10K P/E cycled cell with L_g=0.5μm. The drain bias is from 1.7V to 2.3V and the gate bias is 3V. V_t shift versus drain bias is shown in Fig.5.8. Since the nitride conduction band edge is 2.1eV above the silicon

conduction band edge, sufficient lateral-field heating is necessary to make the channel electrons ìhot enoughî to inject into the trapping nitride, if the vertical field is low. The drastically enhanced RD found at high drain bias (V_d=2.3V) can be explained by the channel hot-electron injection into the trapping nitride. In addition, the t^n time dependence of V_t drift also indicates that PCAT process is involved. As V_d decreases, hot-carrier effect is too weak to make the electrons inject into the trapping nitride. The V_t shift is then dominated by hole tunnel detrapping, which is the same as RT (Fig.5.4, Vg≈0V). It shows that for V_d<2V, V_t shift due to read disturb is almost the same (Fig.5.8), and ΔV_t is proportional to log(t) (Fig.5.7). Furthermore, a smaller V_t shift at V_g/V_d=3V/1.7V than that at 3V/0V can be explained by the reduced vertical field in the former case [3.9].

Finally, we would like to highlight that V_d acceleration is widely used for hot-carrier lifetime projection. As shown in Fig.5.9, V_d-accelerating effect is observed at high V_d. However, gate enhanced read disturb, instead, dominates at low drain bias where hot-carrier effect is insignificant. V_t shift is almost independent of V_d in this regime (e.g. V_d<2V with L_g=0.5μm). The extrapolated read lifetime based on the results at high-V_d regime will be overestimated if we use a low drain voltage during read operation, where the hot-carrier effect is very weak.

5.4.2 Channel Length Scaling Effect

It is known that hot-carrier effect will become more serious in a short-channel device. Fig.5.10 shows the RD results of three cells with gate length (L_g) of 0.5μm, 0.4μm, and 0.3μm, respectively. Increased RD is observed in a shorter gate-length cell. In addition, the temporal evolution of the V_t shift follows a log(t) time dependence for L_g=0.5μm, and exhibits t^n time dependence for L_g=0.3μm. It implies that strong hot-carrier enhanced RD dominates the V_t shift as the channel length is scaled down.

5.4.3 Temperature Effect

We also investigate the temperature effect on RD. It was reported that hot-carrier induced gate current injection increases with decreasing temperature, even with a low drain bias (e.g. V_d<2V) [5.2]. Fig.5.11 shows that RD is almost independent of temperature in a long channel device (L_g=0.5μm), in which hole tunnel detrapping

dominates (so it is termed as room-temperature drift, RT). On the other hand, enhanced RD is observed at low temperature in a shorter device (L_g=0.3μm), where hot-carrier enhanced degradation dominates.

5.4.4 Channel Doping Effect

Channel doping is usually used to control short-channel effect and to improve hot-electron injection efficiency. It was reported that gate disturb is worse in a high-V_{ti} cell [5.3]. RT, GD and RD are characterized for cells with V_{ti} of 1.2V, 2V, and 3V, respectively, in our study. During GD and RD measurements, we use (V_g-V_{ti})=1.5V which is the same gate over-drive that conducts the same read current for each cell. The read drain bias is 1.6V. The results are plotted in Fig.5.12.

As shown in Fig.5.12, two major features are observed. First, RT is almost the same for these three cells, while GD and RD increase with increased V_{ti} (channel doping concentration). Second, V_t shift is strongly enhanced by V_g/V_d in high-V_{ti} cells, however, it is less affected by V_g/V_d in a low-V_{ti} cell. More severe RD in a high-V_{ti} cell (solid triangles) is due to a stronger hot-carrier effect since the channel doping concentration is higher. As the tunneling detrapping of positive oxide charges is responsible for the V_t drift at low vertical/lateral field, RT is expected to be almost the same in these three cells (solid squares). Since the same gate over-drive implies the same inversion charge density in these cells, we need to find out the cause that results in the enhanced GD in a high-V_{ti} cell (solid circles).

The oxide (vertical) field at strong inversion can be formulated as (without trapped charges):

$$E_{ox} = \frac{V_g - V_{ti}}{T_{ox}} + \frac{\sqrt{2\varepsilon_{si}(2\phi_f)qN_A}}{\varepsilon_{ox}} \qquad (5.1),$$

where E_{ox} is the oxide field, T_{ox} is the equivalent oxide thickness of the ONO stack, N_A is the effective channel doping concentration, and ϕ_f is the potential difference between the Fermi level (with acceptor concentration of N_A in the deviceís channel) and the intrinsic Fermi level. ε_{ox} and ε_{Si} are the dielectric constants of oxide and silicon, respectively. Obviously, even with the same gate over-drive (V_g-V_{ti}), the vertical field is stronger in a cell with higher channel doping N_A. The higher vertical

field will enhance the charge tunneling rate [3.9]. This explains the larger GD in a high-V_{ti} cell.

5.5 Summary

Read disturb induced V_t instability is investigated here. It is found that at low vertical/lateral field, tunneling detrapping of cycling-induced positive oxide charges dominates the V_t shift, which is insensitive to temperature. Hot-carrier effect (drain field heating) dominates the V_t shift in a short-channel device, especially at low temperature. Gate voltage-enhanced V_t drift occurs even in a long-channel device, and it is much worse in a high-V_{ti} cell. All of the results are attributed to positive oxide charges, which are created during P/E stress, that can enhance electron injection into the trapping nitride. Process improvements and operating-scheme optimizations have been shown to be effective in suppressing these disturbs [1.38, 5.4-5.5].

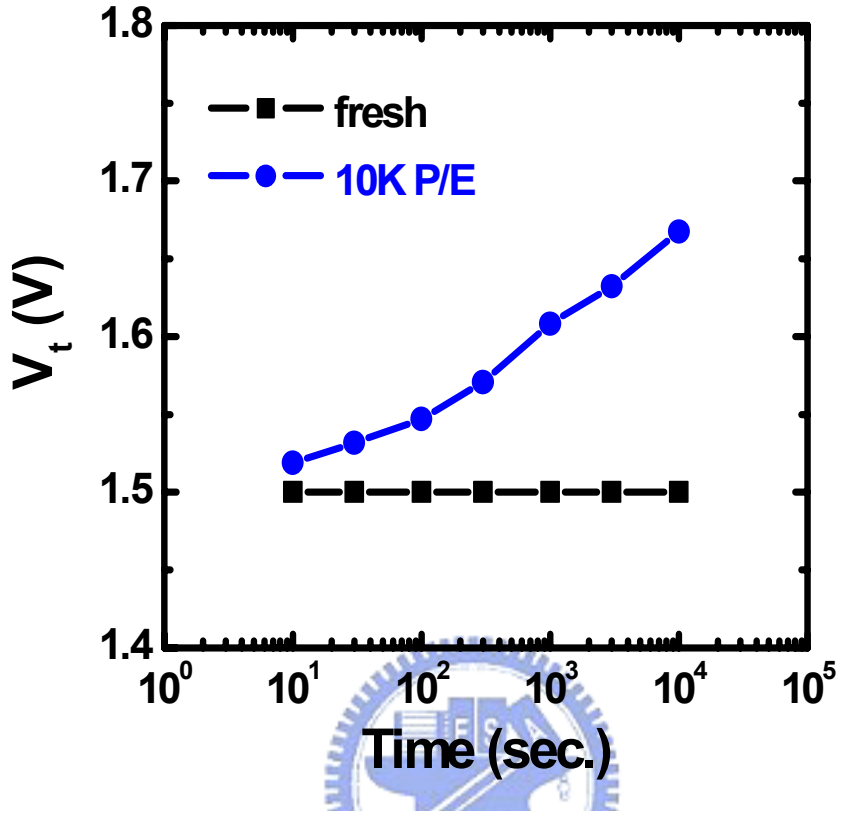


Fig.5.1 Read disturb characteristics of a fresh cell and a 10K P/E cycled cells. L_g=0.5μm and $V_g/V_d/V_s$=2.5V/1.6V/0V.

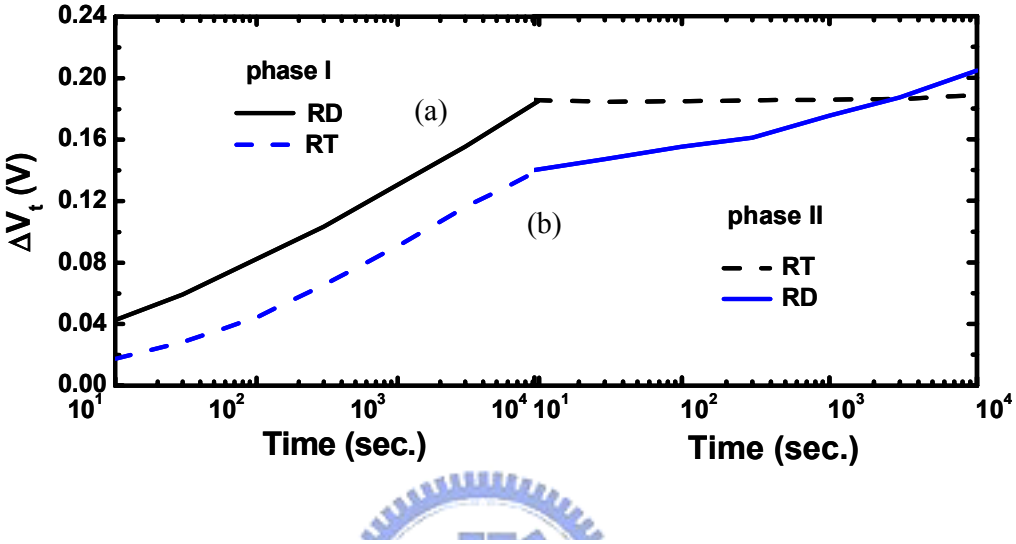
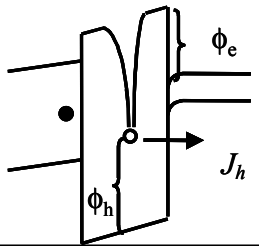
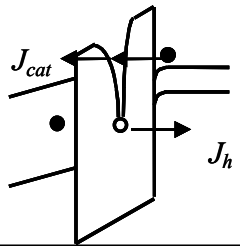
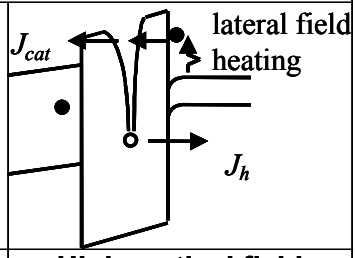


Fig.5.2 Two-phase measurement of the V_t shift temporal evolution of a 10K P/E cycled cell. In curve (a), the cell is at RT mode in the first 10^4 sec. and is at RD mode in the following 10^4 sec. The sequence is reversed in curve (b). Bias conditions of RT and RD are $V_g/V_d/V_s$=0V/0V/0V and $V_g/V_d/V_s$=3V/1.6V/0V, respectively. L_g=0.5μm.

Hole tunnel detrapping	Positive charge-assisted electron tunneling (PCAT)	
		
Low vertical field Low lateral field	**High vertical field Low lateral field**	**High vertical field High lateral field**
Room temp. drift V_g/V_d=0V/0V	**Gate disturb in read V_g/V_d=3V/0V**	**Read disturb V_g/V_d=3V/2V**
$J_h \propto \frac{N_{ox}}{\sqrt{m_h \phi_h}} t^{-1}$	$J_{cat} \propto N_{ox} t^{-p}$	$p = \sqrt{\frac{m_e \phi_e}{m_h \phi_h}} \sim 0.7$
$\Delta V_{t,h}(t) \propto \frac{N_{ox}}{\sqrt{m_h \phi_h}} \log(t)$	$\Delta V_{t,cat}(t) \propto N_{ox} t^{n}$	$n = 1\text{-}p \sim 0.3$

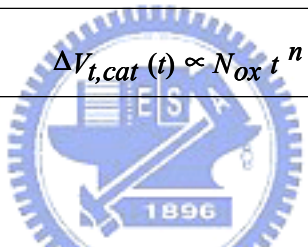


Fig.5.3 Schematics of band diagrams and carrier transport mechanisms at various bias conditions. Solid circles represent the residual electrons in trapping nitride or channel electrons in silicon, and open circles represent the positive trapped charges in bottom oxide. ϕ_h and ϕ_e represent the hole and electron tunneling barrier heights, respectively. m_h and m_e represent the hole and electron tunneling effective masses, respectively. N_{ox} is the effective positive oxide charge volumtric density. Three carrier transport paths are illustrated: (a) Positive oxide charge tunnel detrapping at low oxide field (J_h). (b) Positive oxide charge-assisted electron injection into nitride (J_{cat}), in addition to J_h, at high oxide field. (c) Positive oxide charge-assisted hot-electron injection into nitride (J_{cat}), in addition to J_h, at high lateral field. Hot electrons are generated via lateral field heating. Time evolutions of these injection currents and V_t shifts are also formulated.

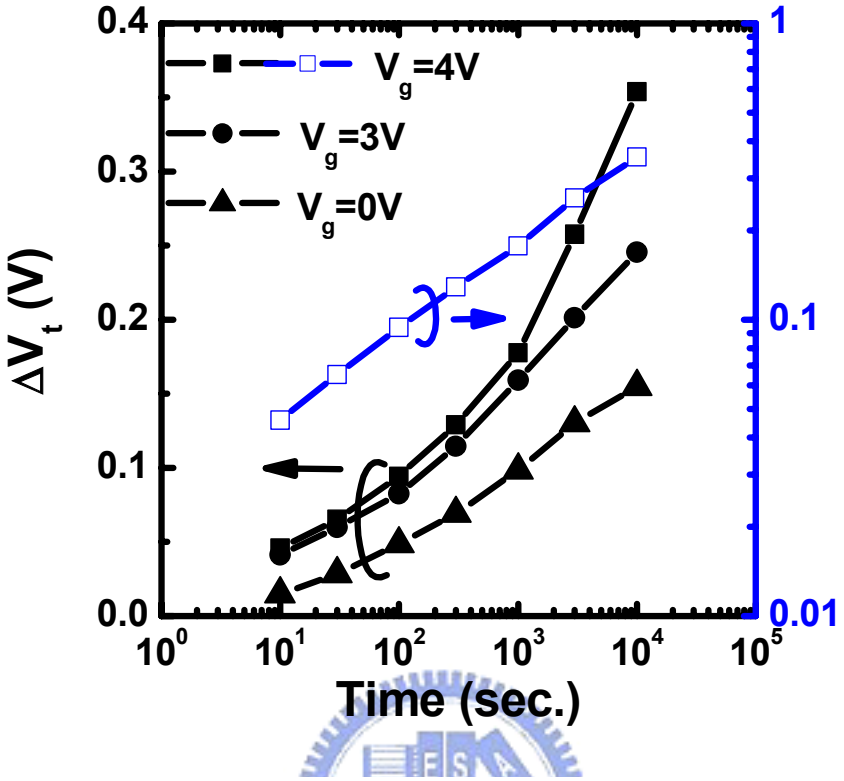
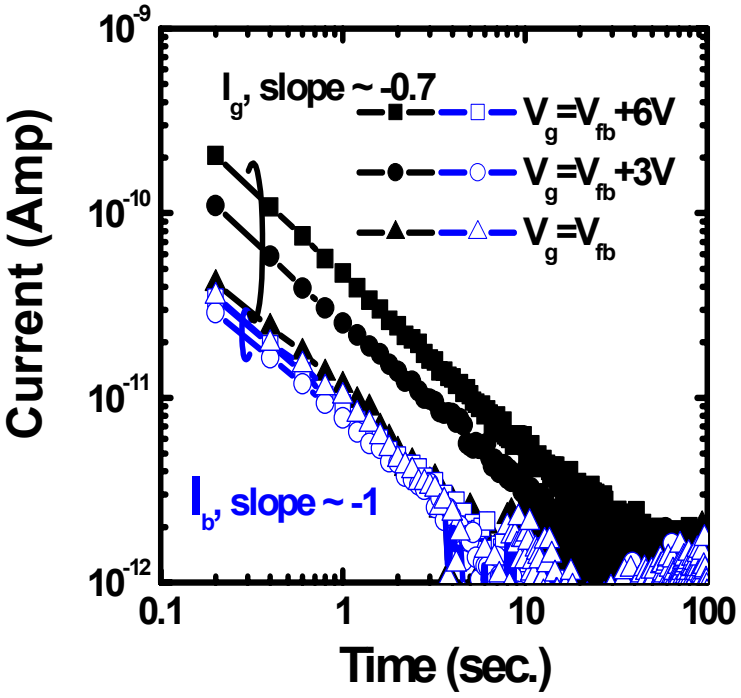
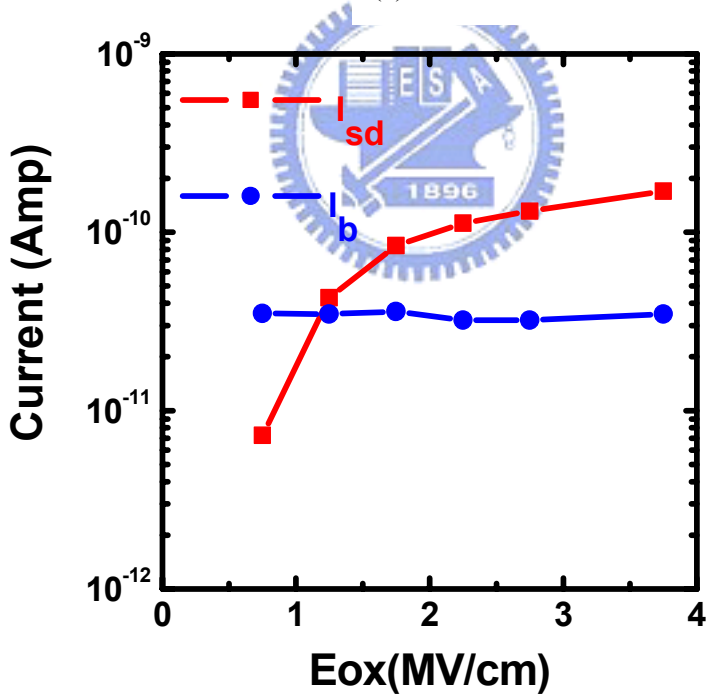


Fig.5.4 V_t shift versus applied gate bias of a 10K P/E cycled cell. The drain and the source are grounded, and the disturb time is 10^4 sec. L_g=0.5μm.



(a)



(b)

Fig.5.5 (a) The measured I_g and I_b transients at erase state. The cell has a large gate area (2.5×10^5 μm^2). V_g is equal to V_{fb}, V_{fb}+3V, V_{fb}+6V, respectively. (b) Field dependence of positive oxide charge detrapping current (I_b) and electron tunneling current (I_{sd}) at t=0.2 sec. in (a).

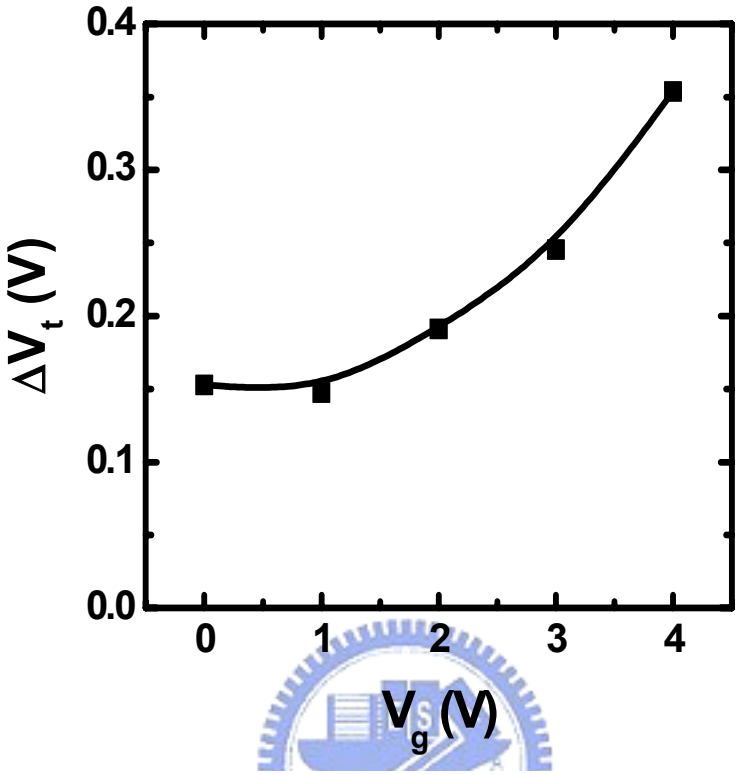


Fig.5.6 V_t shift versus applied gate bias of a 10K P/E cycled cell. The drain and the source are grounded, and the disturb time is 10^4 sec. L_g=0.5μm.

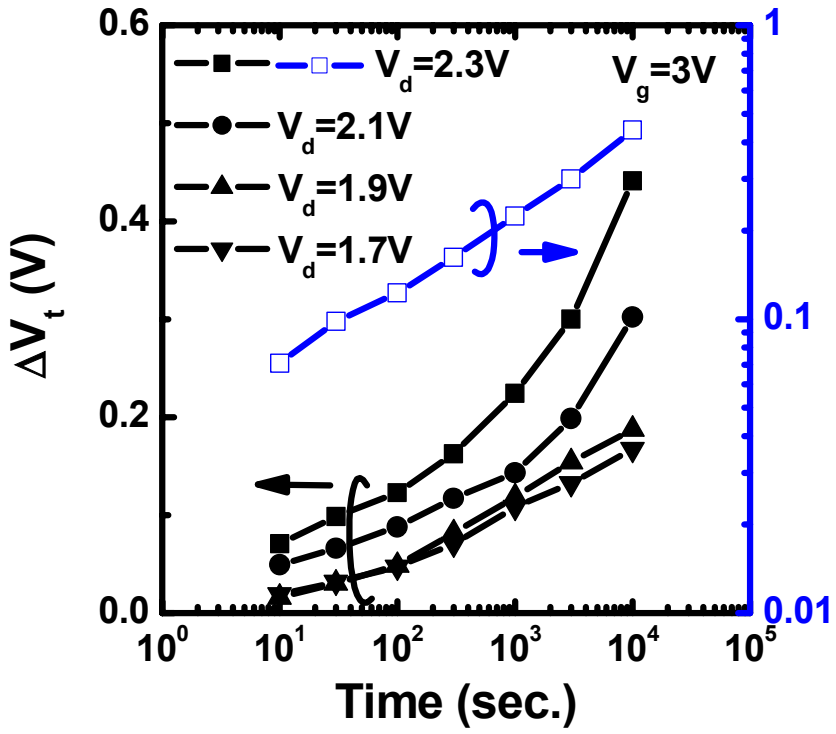


Fig.5.7 V_t shift versus disturb time of a 10K P/E cycled cell at various drain biases. V_g/V_s=3V/0V and L_g=0.5μm.

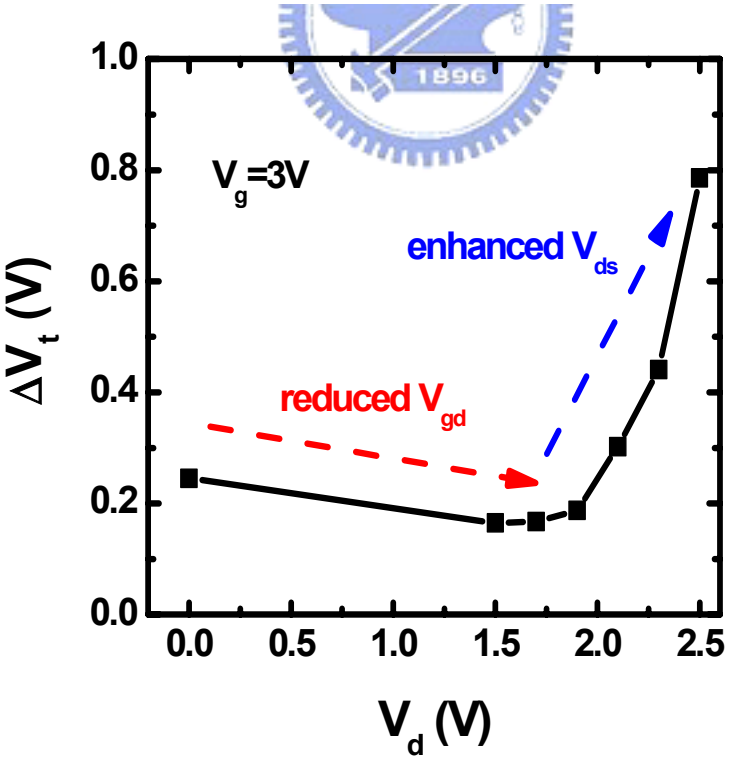


Fig.5.8 Read disturb induced V_t shift versus applied drain bias of a 10K P/E cycled cell. The disturb time is 10^4 sec. V_g/V_s=3V/0V and L_g=0.5μm.

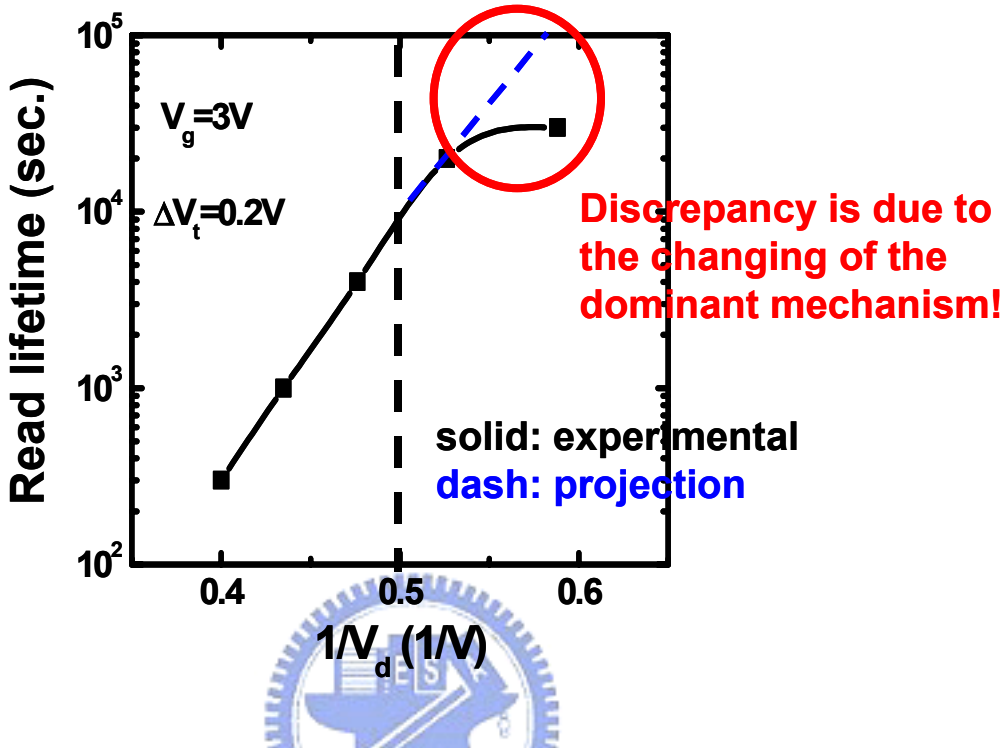


Fig.5.9 Read lifetime projection by V_d-accelerating approach. Lifetime is defined as the disturb time resulting in a V_t shift of 0.2V. V_g/V_s=3V/0V and L_g=0.5μm. As shown in the figure, lifetime is overestimated in the low-V_d regime where gate-enhanced disturb dominates.

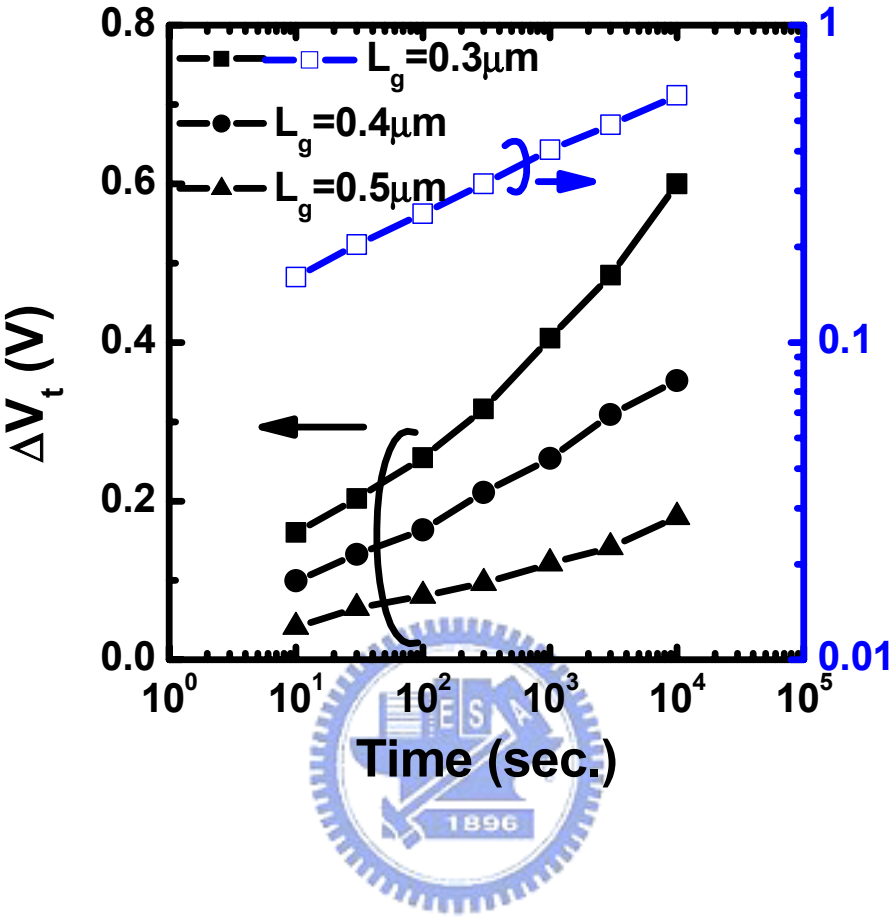


Fig.5.10 V_t shift versus disturb time of 1K P/E cycled cells with different channel lengths. $V_g/V_d/V_s$=3V/1.6V/0V.

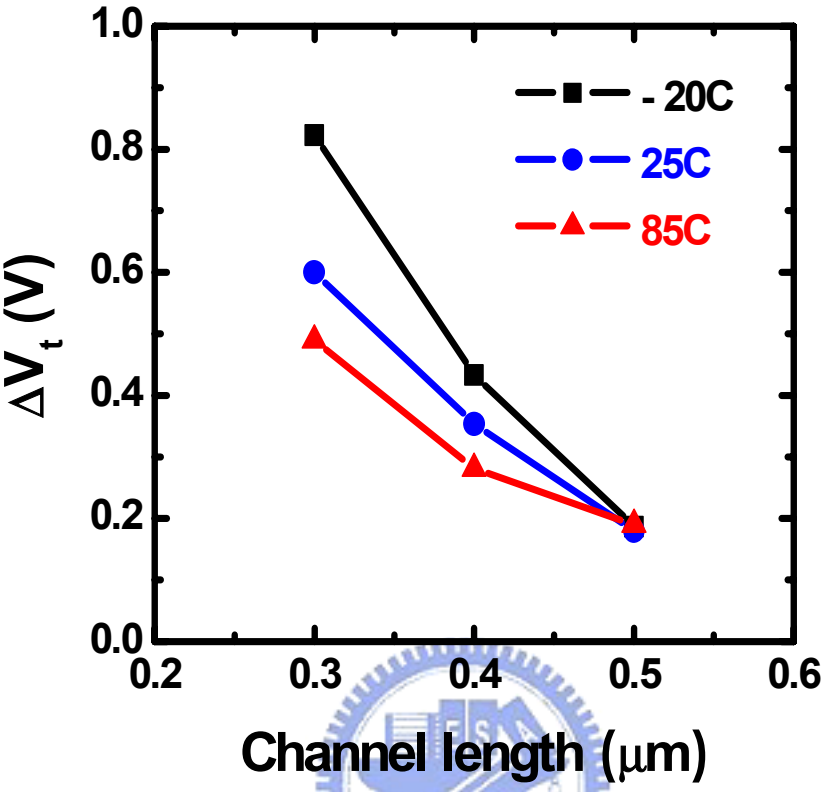


Fig.5.11 Temperature effect on read disturb of 1K P/E cycled cells. Devices with gate lengths of 0.5μm, 0.4μm and 0.3μm are characterized. The applied gate and drain biases are 3V and 1.6V, respectively, and the disturb time is 10^4 sec..

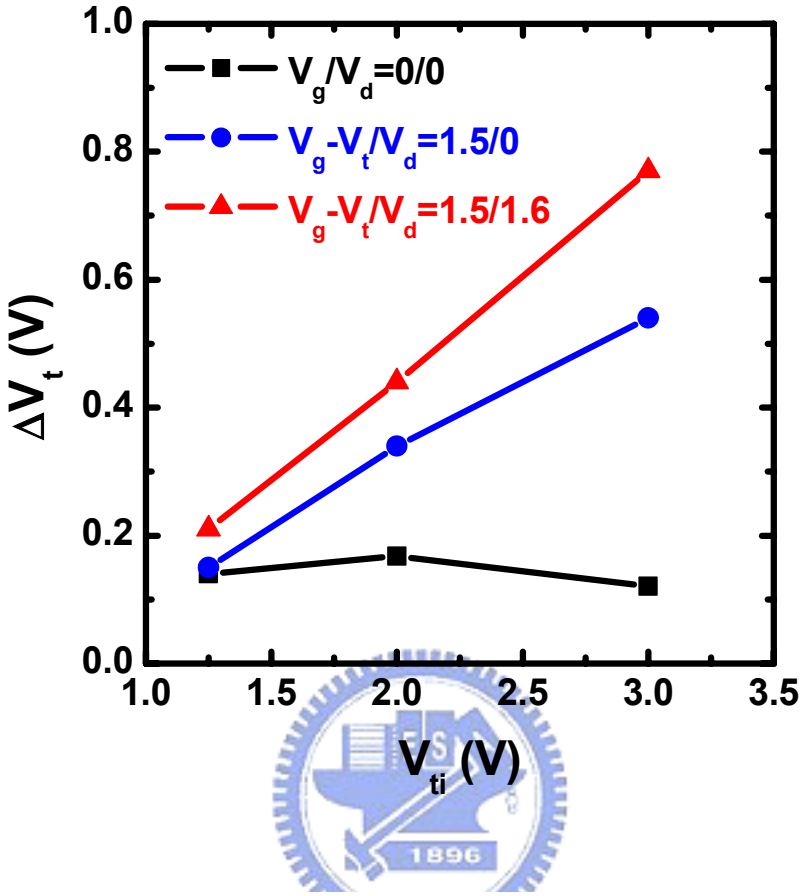


Fig.5.12 Initial threshold voltage versus room-temperature drift, gate disturb and read disturb. The cells undergo 10K P/E cycles. The bias conditions for GD, and RD are V_g-$V_{ti}/V_d/V_s$=1.5V/0V/0V and 1.5V/1.6V/0V, respevtively, and $V_g=V_d=V_s$=0V for RT. The disturb time is 10^4 sec. and L_g=0.5μm.

Chapter 6

Erase Speed Degradation

6.1 Motivation

Till now, we have discussed the V_t instability, which in general is considered to be data retention issues. Another reliability concern that is also important for NVM products is its endurance, which means the allowed cycles it could undergo before it fails to be programmed and erased any more. Cycle-induced traps in the tunnel oxide is considered to be the major cause of endurance failure in a floating-gate flash memory cell [2.9, 6.1-6.4]. These traps would affect the program and the erase efficiency. More seriously, the tunnel dielectric may even goes breakdown [3.4].

Endurance characteristics of the NBit cell have been reported [6.5]. Operating-V_t window degradation has also been mentioned. It is said that the substrate-hot-electron injection may occur. These electrons are accumulated at the central channel region and are hard to be erased. This phenomena is getting worse after P/E cycling. It is also claimed that doping profiles are closely related to this effect. Novel Bias schemes [5.6, 6.6-6.7] and device structure [6.8] have been proposed to improve the endurance as well.

We have interesting findings regarding the endurance characteristics of the NBit cell. Letís look at Fig.1.8 again. V_t window can indeed be kept unchanged up to 100K P/E cycles. However, the required erase time may increase. Fig.6.1 shows the EV-pass shots v.s. cycles of a 2Mb test chip. Here, the EV-pass shots mean the total erase shots necessary to pass erase-verify (EV). Slower erase speed of the 2^{nd} bit is observed from the beginning and it degrades more significantly after cycling. On the other hand, erase speed of the 1^{st} bit in 2b/c operation and in 1b/c operation is relatively stable. In this paper, causes of such erase speed degradation are clarified. In addition, scaling impacts on the erase characteristics are also discussed.

6.2 Experimental

The devices used in this study are listed in Table 6.1. Cell-B is the same as the unit cell in the 2Mb test chip. Two-bit-per-cell P/E cycling sequence in our characterization is described in the following. Please refer to Fig.6.2. Firstly, Bit-D is programmed until it passes program-verify (PV, and this bit is named as the 1^{st} bit),

then programming of Bit-S follows (this bit is named as the 2nd bit). During erasing, erase pulses are applied to these two bits successively (firstly the 1st bit, and then the 2nd bit) until both of them pass erase-verify (EV) simultaneously. V_t is defined as the gate voltage that induces a channel current of 1μA. The program and erase operating conditions are summarized in Table 6.2.

Two techniques are utilized to investigate the injected charge distributions. The V_t-V_j measurement, which has been clearly explained in chapter 2 (Fig.2.3), is applied to probe the lateral extent of the trapped electrons [6.9]. Besides, ΔV_t and ΔV_{btbt} is used to monitor the amount as well as the polarity of injected charges above the channel region and above the n^+ junction region, respectively [6.10-6.11]. Pleases refer to Bit-D side of Fig.6.3 (a). Here, ΔV_{btbt} is the V_g shift of a programmed (or an erased) cell, as compared to its virgin state, that induces a constant GIDL current at V_d=2V. Since the GIDL current is modulated by the vertical electrical field above the n^+ junction, ΔV_{btbt} is a good indicator to estimate the stored charges in that region. A negative ΔV_{btbt} means that net positive charges reside, and vice versa. On the other hand, charges stored above the channel region (outside n^+ junction) affect deviceís V_t most. A positive $\Delta V_{t\text{-}REV}$ means that net negative charges stored above the channel region. Fig.6.3 (b) gives a graphic description of the polarity of the (net) stored charges above the channel and above the n^+ junction in a $\Delta V_{t\text{-}REV}$-ΔV_{btbt} plot (simplified to be ΔV_t-ΔV_{btbt} plot in the following). In addition, the amount of the stored charges is proportional to the shifts.

6.3 Results and Discussions

6.3.1 Wider Trapped-Electron Area of the 2nd-Programmed Bit

As shown in Fig.6.1, erase speed is slower for the 2nd bit. Fig.6.4 shows the EV-pass shots versus cycle numbers of a single NBit cell, which is used to emulate the test-chip-like operation. As being consistent with the test-chip results, the ì2nd bitî bit is always erased more slowly, and its EV-pass shots increase with cycles. We use the V_t-V_j measurement to probe the lateral extent of the trapped-electron regions of the 1st and the 2nd bits. In Fig.6.5, ΔV_t (the y-axis) is equal to ($V_t(V_j)$-$V_t(V_j$=0.1V)), which is an indicator of the trapped electrons that are screened out by the junction depletion region. Higher junction bias is necessary for the 2nd bit, as compared to the 1st bit, to

suppress the trapped-electron effect, though both bits have the same ΔV_t after programming. It implies that more ìfarî electrons are injected and are stored above the central channel region (neighboring to the 2nd bit side) as the 2nd bit is programmed, if the 1st bit has been programmed at first. Fig.6.6 shows the ΔV_t-ΔV_{btbt} plot of the 1st bit and the 2nd bit as they are programmed (each point in this figure indicates the ìcharging statusî above the channel region and above the n^+ region after each program shot). It can be found that for the same ΔV_t, which indicates the comparable peak electron density stored above the channel region after programming, the 2nd bit is always with a smaller ΔV_{btbt} (positive). It means that the stored electrons above the n^+ region are less for the 2nd bit. Fig.6.5 and Fig.6.6 give us a picture that the injected electrons of the 2nd bit is more away from the n^+ junction (Fig.6.2), if its neighboring 1st bit has been programmed.

Two-dimensional device simulator [2.7] is used to explore the physical cause. Fig.6.7 (a) and Fig.6.7 (b) show the normalized profiles of the electron temperature and of the electron density whose energy is higher than 3.2eV, respectively. Here, the x-axes are the normalized position along the conduction channel. Solid lines and dash lines represent the simulated results during the programming of Bit-D as its neighboring Bit-S is not programmed and is programmed, respectively. It is found that if the Bit-S is programmed, a locally high electric field would be built there during the programming of Bit-D. Channel electrons would be heated by this locally enhanced field before they enter into the depletion region at drain side where the programming junction bias is applied (Fig.6.7 (a)). The injected electron distribution of the 2nd-programmed bit would thus shift toward the central channel region (Fig.6.7 (b)).

6.3.2 Degraded Erase Speed of the 2nd-Programmed Bit After Cycling

Fig.6.8 shows the ΔV_t versus. ΔV_{btbt} plot of the 1st and the 2nd bits as they are erasing. The circled region in Fig.6.8 indicates that though amounts of holes are injected (ΔV_{btbt} is more and more negative, >1.5V), ΔV_t is less affected (<0.3V). Let us look back to Fig.6.6 where the post-cycling ΔV_t-ΔV_{btbt} plot of the 1st and the 2nd bits during programming is also shown. We can find that for the same ΔV_t (e.g., 2V), ΔV_{btbt} of the 2nd bit is reduced after cycling. By a V_t-V_j measurement, we also find that the stored electron distribution extends toward the central channel region after

P/E cycling (Fig.6.9). These results suggest that more ì farî electrons, which are hard to access, are more easily to be injected in a highly cycled cell, especially for the 2nd bit (Fig.6.10). It is consistent with the cycling effect on EV-pass shots as shown in Fig.6.4.

6.3.3 Erase Speed Modulation by Adjacent Junction Bias

Fig.6.11 shows the erase characteristics of four cells (Table 6.1). Erase speed is normal in high-V_{ti} cells (cell-A and cell-Aí), except that over-erasure is found in the short-channel one (cell-Aí). However, slower erase speed is found in a short-channel and low-V_{ti} cell (cell-Bí). Since cell-A and cell-B have comparable erase speed, channel doping effect cannot explain the slow erase found in cell-Bí. We also observed that the erase speed (as erasing Bit-D) is varied with source biases in cell-Bí (Fig.6.12). However, source bias effect is not observed in cell-A. It implies that the erase speed could be affected by adjacent junction bias [6.2, 1.31]. Fig.6.13 shows the simulated surface potentials of cell-Aí and cell-Bí, in which V_s is equal to 0V and 2V [2.7]. Surface potential nearby the drain side (the erasing side) is modulated by V_s in cell-Bí. On the other hand, it is not affected by V_s in cell-Aí. It explains the slower erase speed of cell-Bí. During erasing (of Bit-D), the floating source junction of cell-Bí would be charged positively via the punch-through-induced coupling of the drain bias. This coupling effect reduces the lateral field and suppresses the BTBT HH injection. However, the drain and source sides are well isolated in cell-A and cell-Aí since the channel doping is higher, and in cell-B since it has a longer channel. Accordingly, a higher channel doping and an appropriate management of adjacent junction bias would solve such kind of slow erase observed in a short-channel, nearly punch-through cell (cell-Bí). These arguments are summarized in Table 6.3.

6.4 Summary

Erase speed degradation in an NBit cell is investigated. Our study shows that the trapped-electron area of the second-programmed bit would extend more toward the central channel region if its neighboring bit (of the same cell) has been programmed. The second bit would then be erased more slowly. This effect gets more obvious after P/E cycling. In addition, the erase speed would be modulated by adjacent junction bias in a short-channel, nearly punch-through cell.

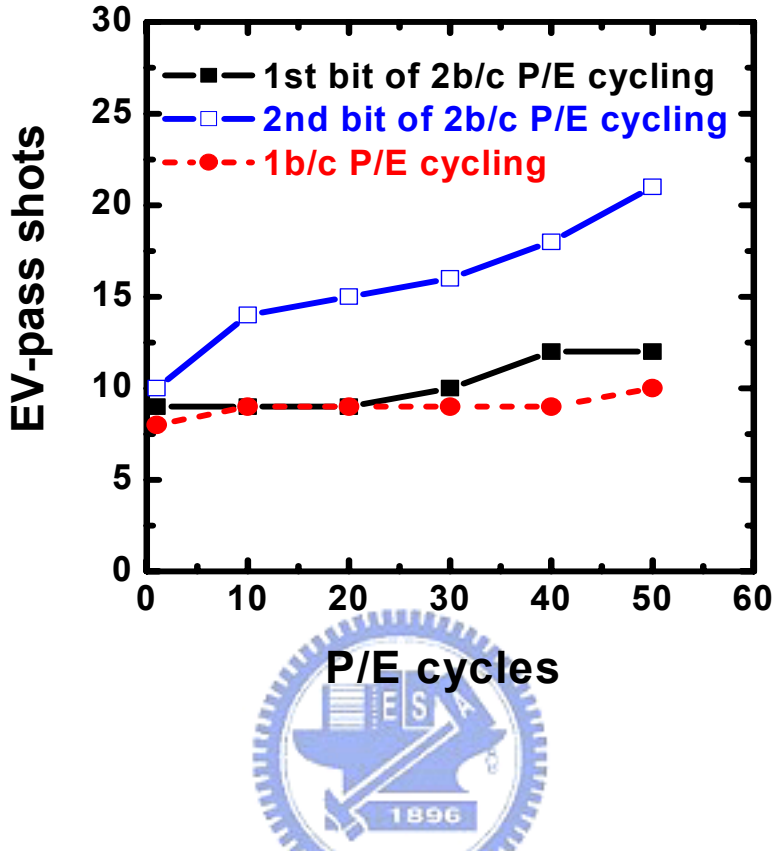


Fig.6.1 EV-pass shot v.s. cycles of a 2Mb test chip. Here, the EV-pass shots mean the accumulated erase shots necessary for all the ì1stî or the ì2ndî bits of the chip to pass erase-verify (EV).

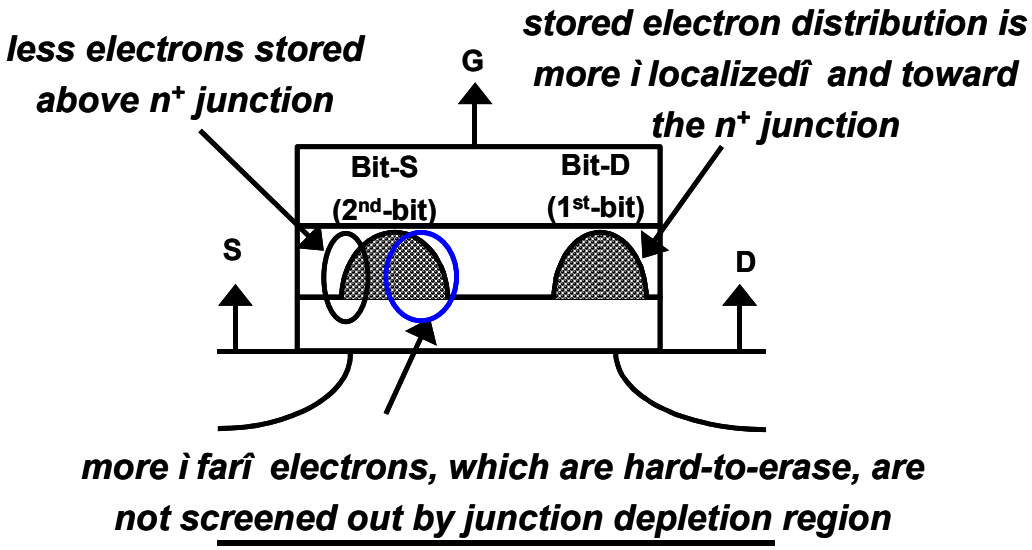


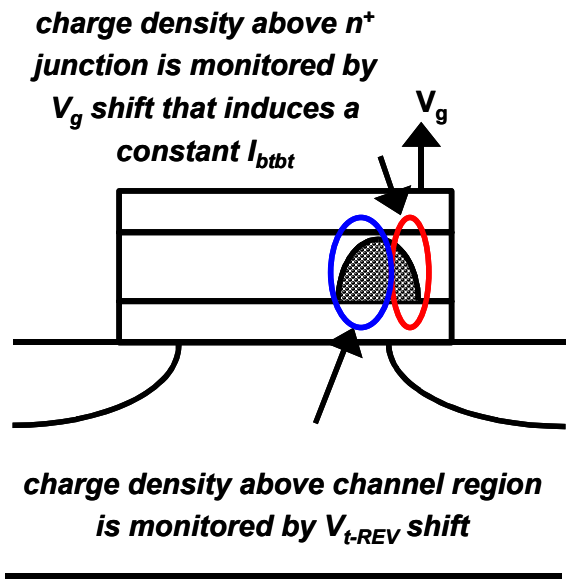
Fig.6.2 Schematic representation of an NBit cell structure and localized charges storage. The charge distributions are depicted for the case in which Bit-D is the 1st bit and Bit-S is the 2nd bit.

Table 6.1 Devices used in the study. V_{ti} means the initial-V_t of the cell. The channel width is 0.18μm.

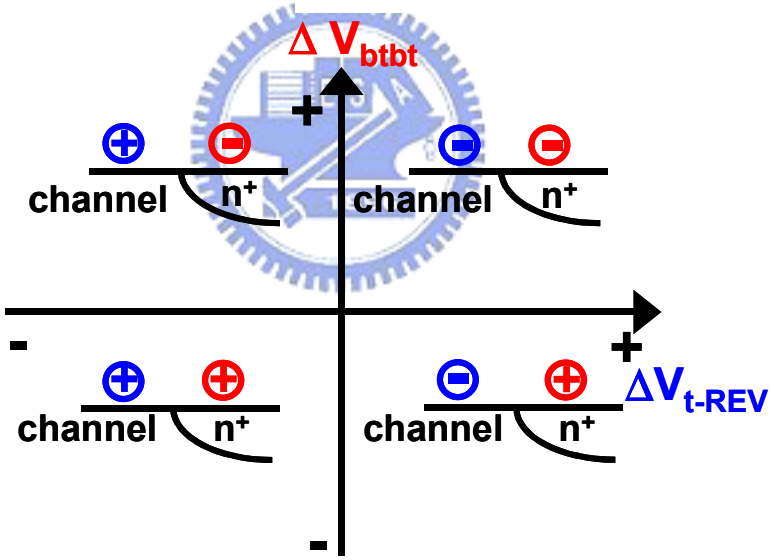
L_g / V_{ti}	0.32μm	0.24μm
High V_{ti}	A	Aí
Low V_{ti}	B	Bí

Table 6.2 Operating principles and conditions in this study.

Operation	Principle	Details
Program	CHE	V_g: 10V, V_d: 3.6V, V_s:0V, V_b: 0V, ΔT=1μs, when programming Bit-D. PV passes until (V_{tp}-V_{ti})>2V
Erase	BTBT HH	V_g: -6V, V_s: floating, V_b: 0V, ΔT=0.2ms, when erasing Bit-D; V_d: stepping from 3V to 5.4V with ΔV_d=0.3V in the first 9 shots, and then 5.4V thereafter; EV passes until (V_{te}-V_{ti})<0.1V.
Read	Backward Read	V_s: 1.6V, V_d: 0V, V_b: 0V, V_t is defined to be the V_g that induces I_s=1μA, when reading Bit-D.



(a)



(b)

Fig.6.3 (a) Techniques to monitor the stored charge distribution in the trapping nitride. Charges stored above the channel region are estimated by $V_{t\text{-}REV}$ shift that induced a constant read current. Charges stored above the n^+ junction are estimated by V_g shift that induced a constant GIDL current at V_d=2V. (b) Schematic representation of the net stored charge polarity above the channel and above the n^+ region in a $\Delta V_{t\text{-}REV}$-ΔV_{btbt} plot. Reverse-read V_t ($V_{t\text{-}REV}$) is used here to measure the stored charged effect above the conduction channel.

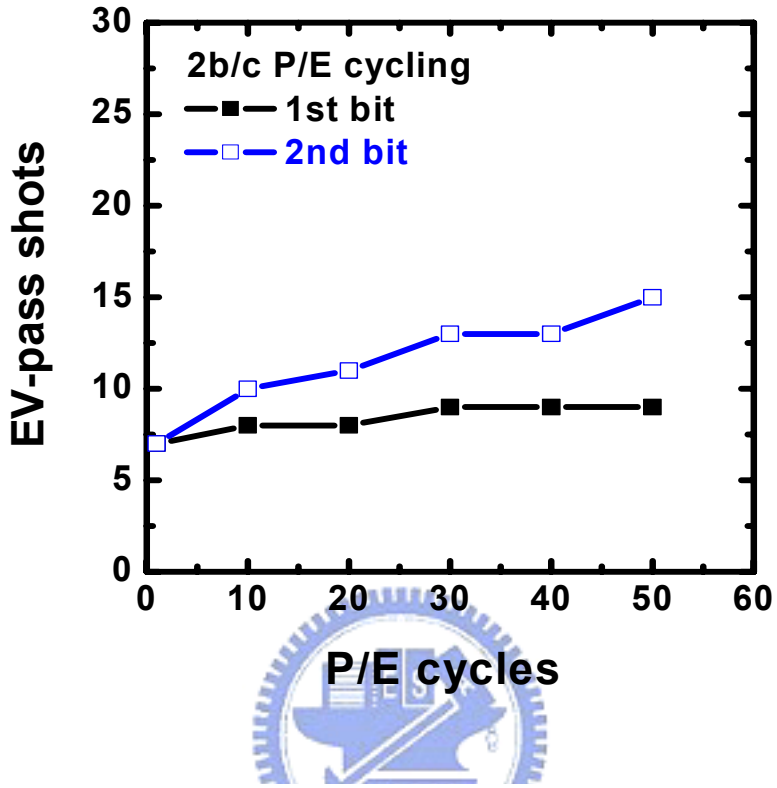


Fig.6.4 EV-pass shots v.s. P/E cycles of an NBit cell.

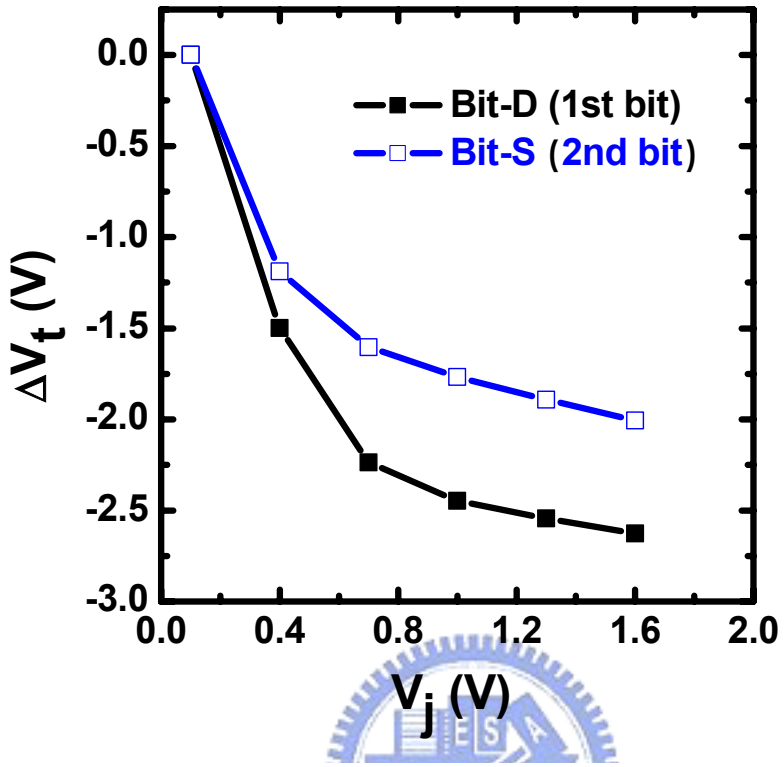


Fig.6.5 ΔV_t-V_j measurement of the Bit-D and the Bit-S of an NBit cell. V_j is equal to V_d for Bit-D, and is equal to V_s for Bit-S. This result is at the 50^{th} cycle.

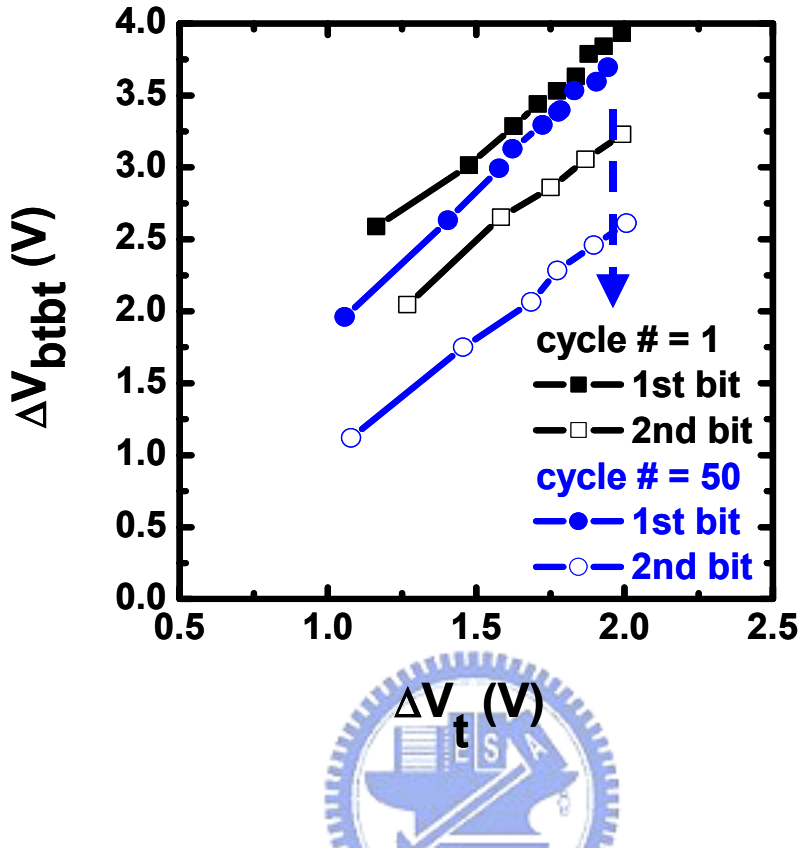
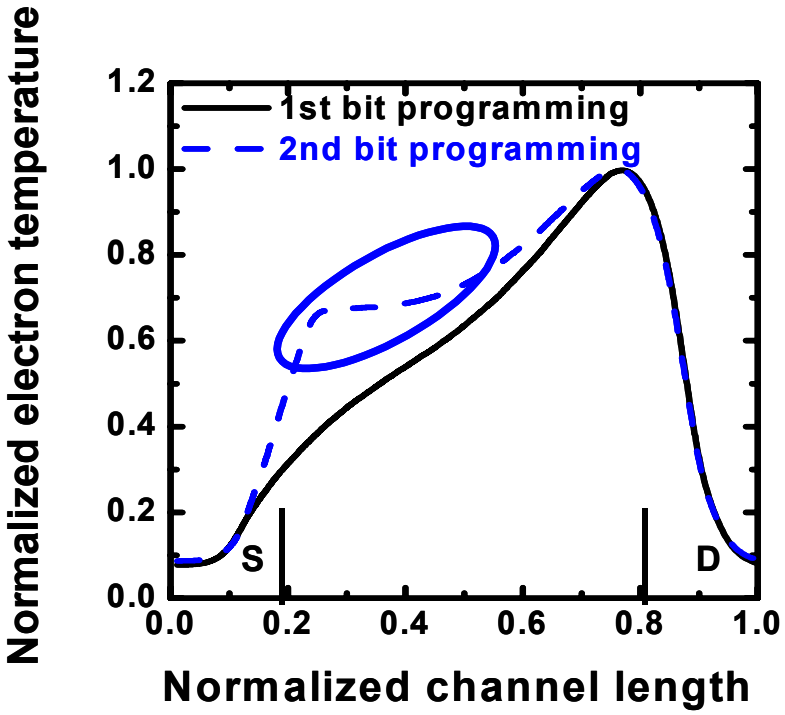
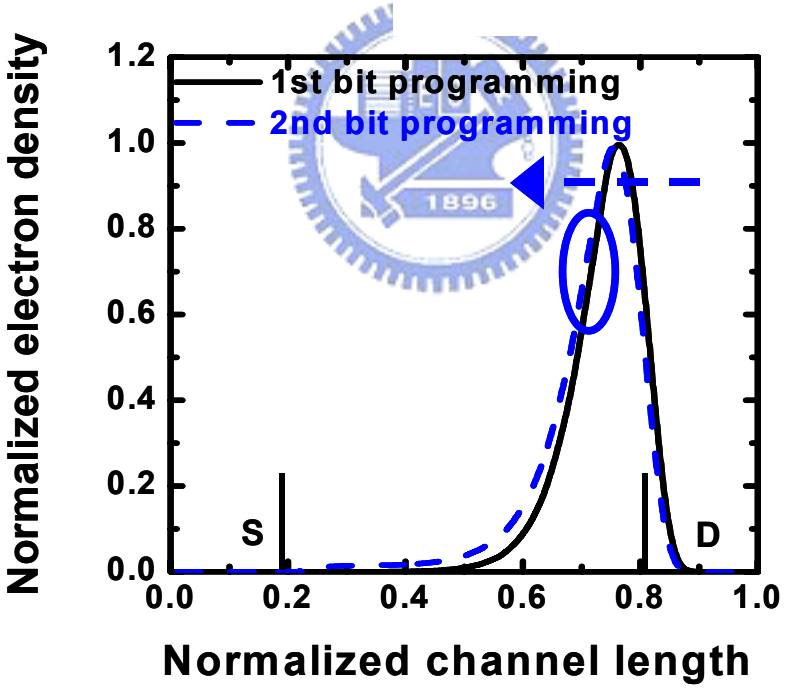


Fig.6.6 ΔV_t-ΔV_{btbt} plot during programming of a fresh and a 50 P/E cycled NBit cells.



(a)



(b)

Fig.6.7 Normalized electron temperature profiles (a), and electron density (electron energy > 3.2eV) distributions (b) along the conduction channel calculated by 2D device simulations. V_g/V_d=10/3.6V. For the 2nd bit, the neighboring 1st bit has been programmed to ΔV_t=2V.

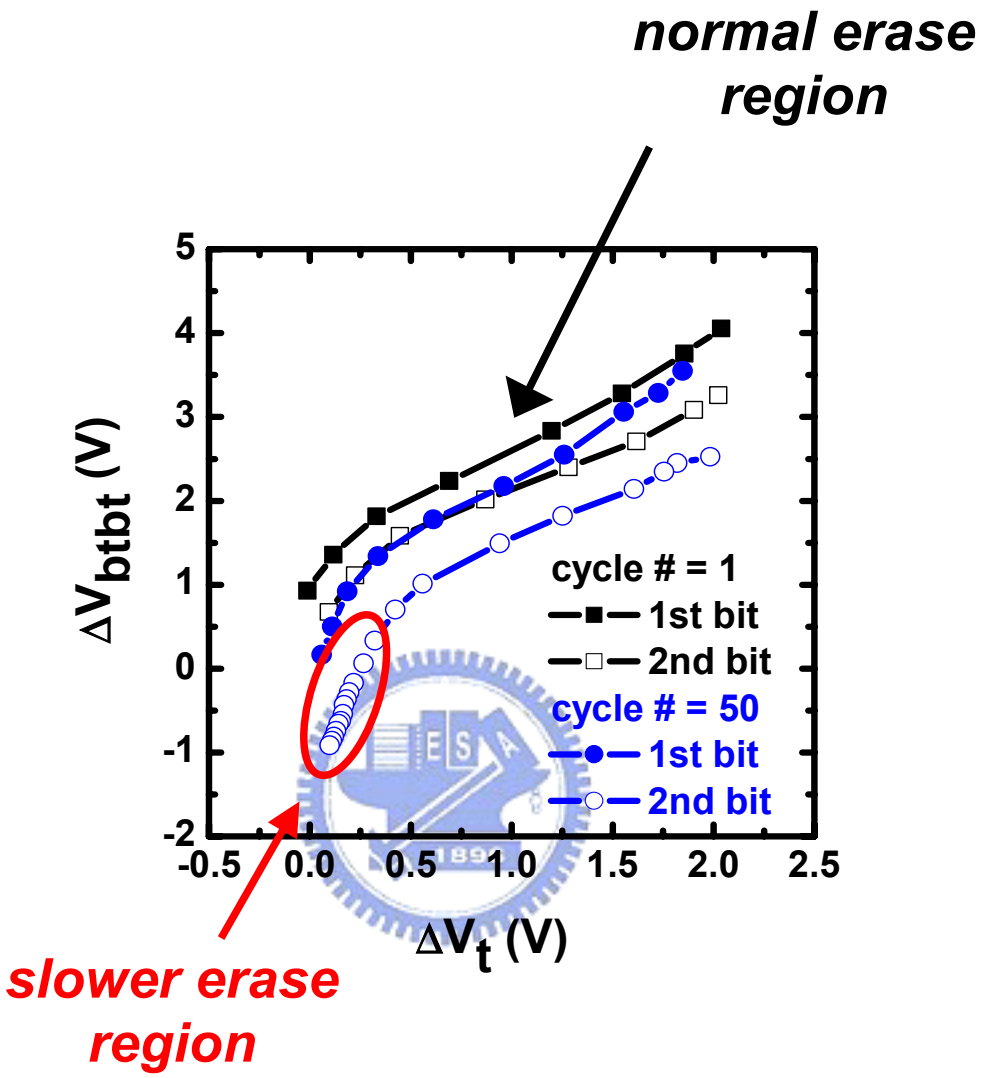


Fig.6.8 ΔV_t-ΔV_{btbt} plot during erasing of a fresh and a 50 P/E cycled NBit cells.

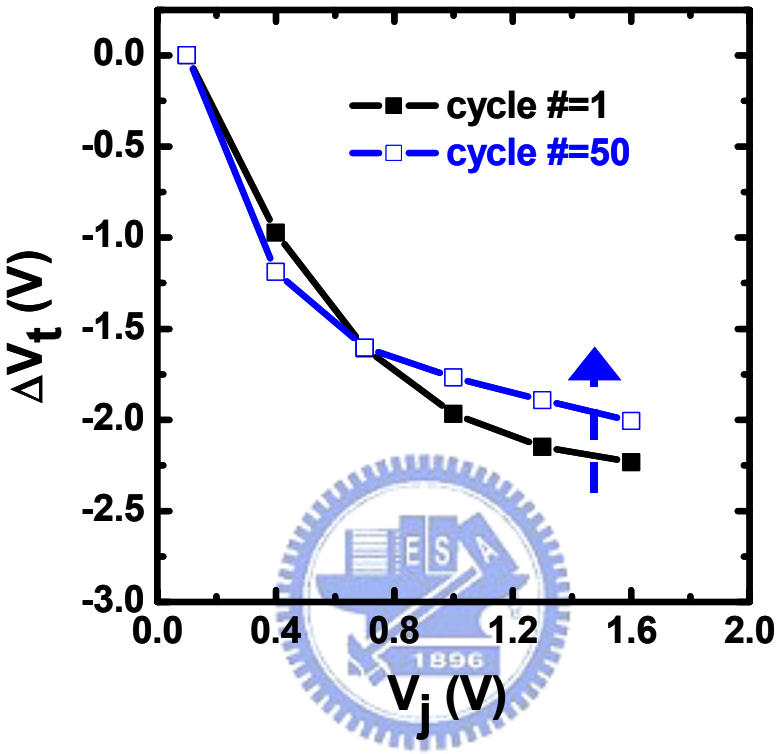


Fig.6.9 Comparison of the ΔV_t-ΔV_j characteristics of a fresh and a 50 P/E cycled NBit cells.

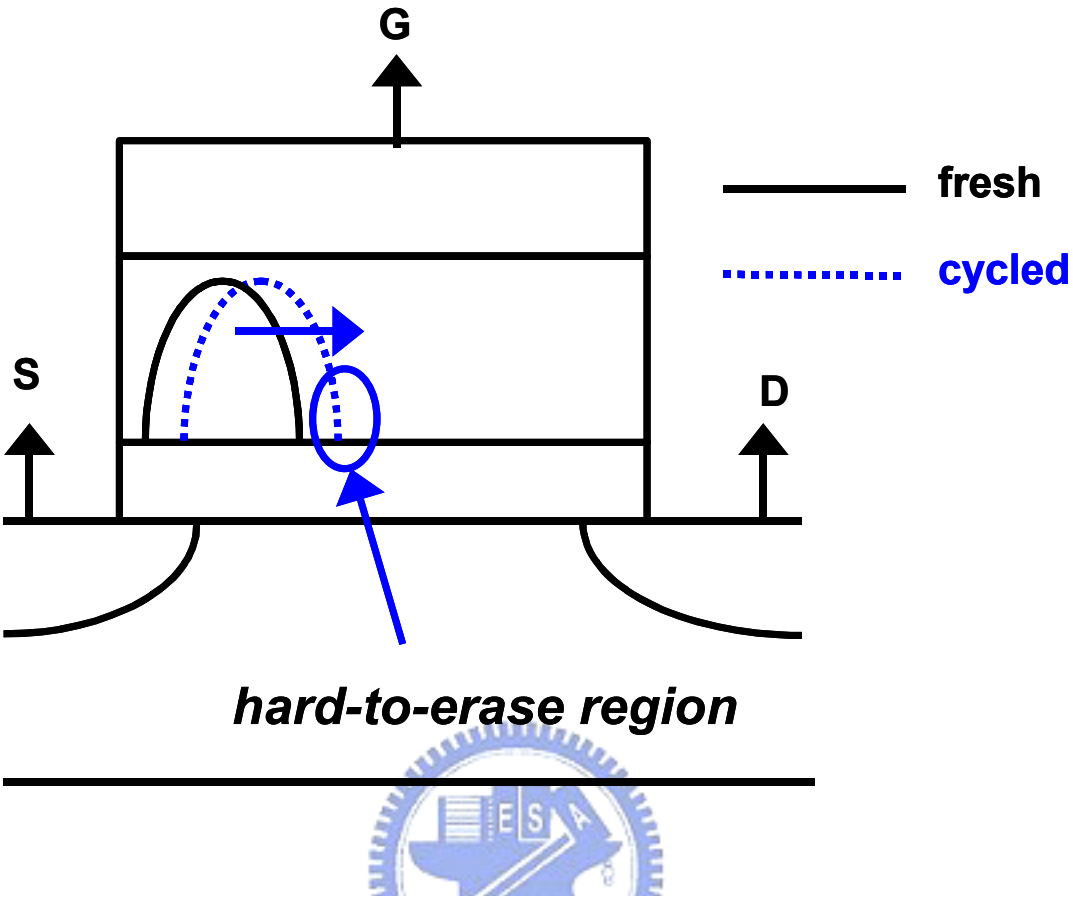


Fig.6.10 Schematic representation of the injected electron distribution after programming of a fresh and a 50 P/E cycled NBit cells.

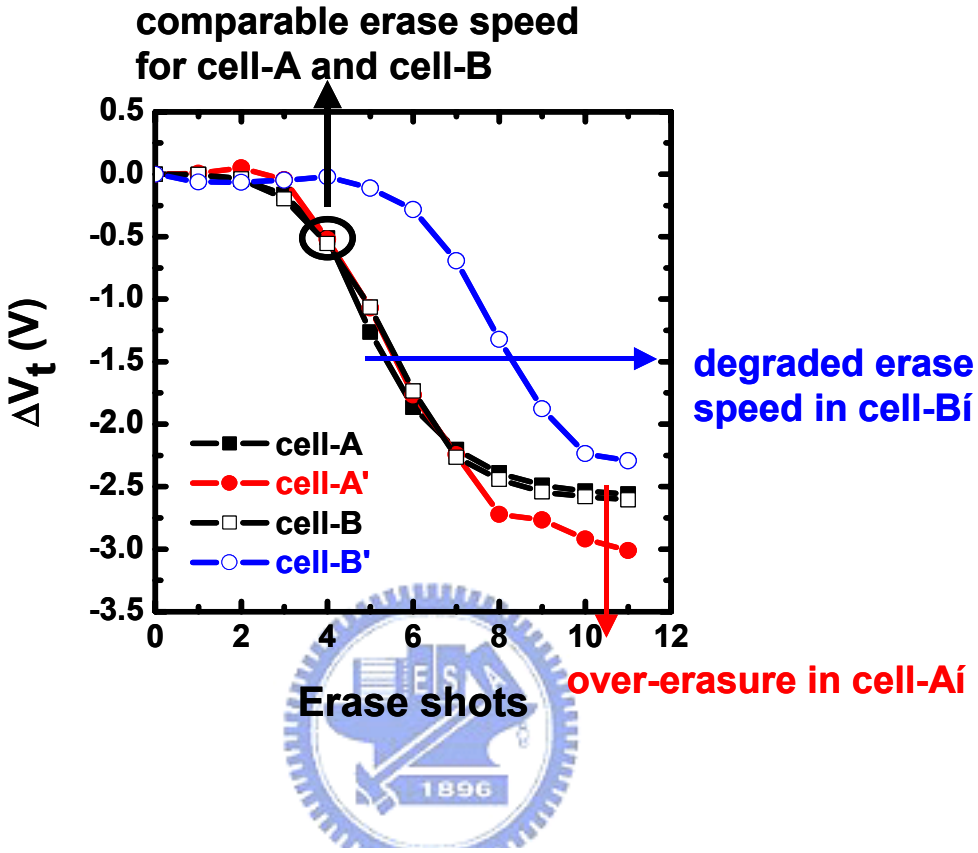


Fig.6.11 Erase characteristics of cells of various L_g and V_{ti} (Table 6.1). ΔV_t representation the V_t shift from its programmed-stateís V_t after each erase shot.

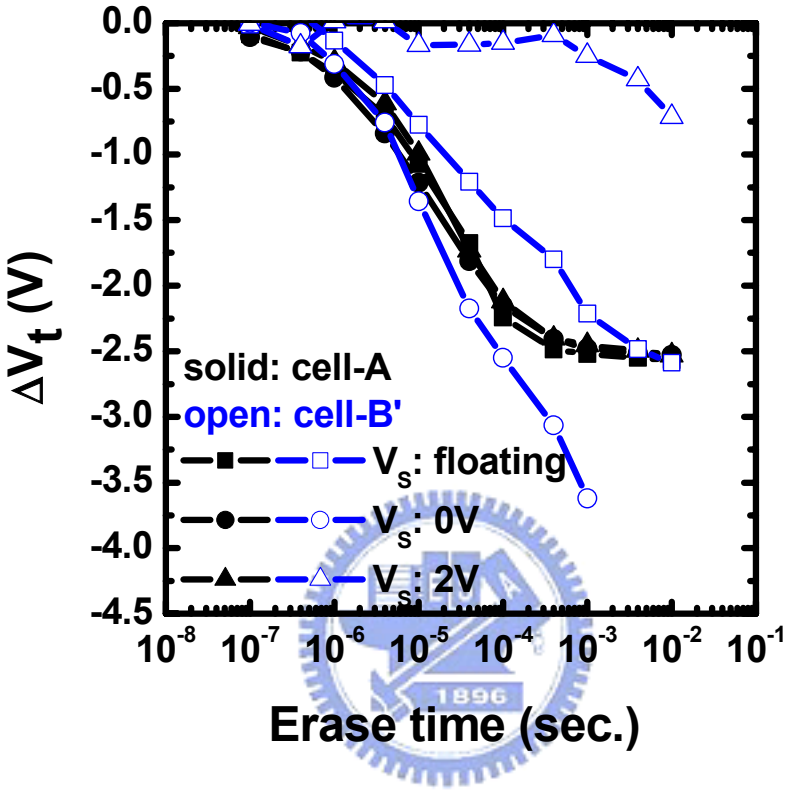


Fig.6.12 Erase speed comparison among various source junction biases during erasing the Bit-D of cell-A and cell-Bí. V_g/V_d=-6V/5V.

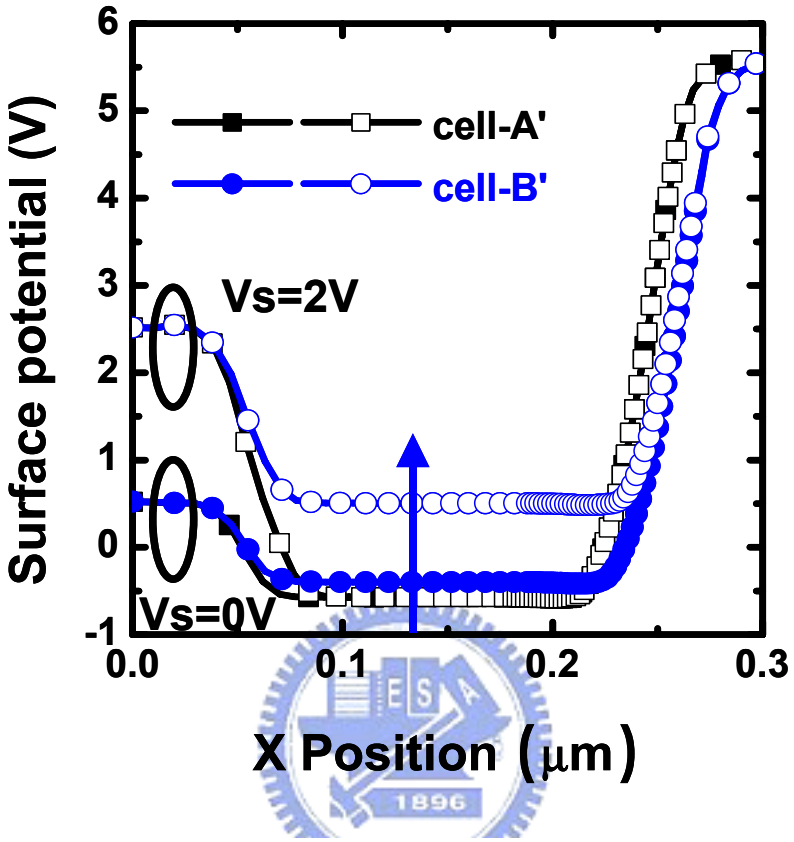


Fig.6.13 Surface potentials of cell-Aí and cell-Bí. V_g/V_d=-6V/5V.

Table 6.3 Comparison of neighboring junction bias effect among cells of various channel length and channel doping concentration.

channel length / channel doping	long	short
high	Not affected, **junctions are well-isolated by long channel length and high channel doping.**	Not affected, **junctions are well-isolated by high channel doping, though may be** over erased**.**
low	Not affected, **junctions are well-isolated by long channel length.**	Affected, since **it is nearly punch-through.**

Chapter 7

Conclusions

We have investigated the reliability issues in a trapping nitride, localized charge storage Flash memory cell. The subjects that have been comprehensively discussed in previous chapters include charge loss in a high-V_t cell, charge gain in a low-V_t cell, excess-hole effect in an over-erased cell, read disturb modes, and erase speed degradation. We would like to summarize the important conclusions here.

Intrinsic charge rententivity is excellent in an un-cycled NBit cell. However, charge loss increases with cycle numbers and shows strong dependence on bake temperature and the applied vertical field during retention test. Our study finds that lateral re-distribution of trapped charges has little effect in a highly cycled cell. V_t loss is attributed mostly to nitride charges escape by Frenkel-Poole emission and subsequent oxide trap-assisted tunneling. These oxide traps are created during P/E cycling. Increase of stress-induced interface state density, which can be monitored by a charge-pumping current measurement, is a good indicator of cellís retention. This model is well confirmed by both the single cell and the product characterizations. Furthermore, dependence of the nitride charge loss on the square root of the nitride electric field has been obtained by this model. Accordingly, a V_g-accelerating technique and a temperature-accelerating method are developed. The field and temperature accelerations are found to be interchangeable. However, traps would be annealed during high-temperature baking. The annealing of interface states would be another source of the observed V_t loss and the annealing of oxide traps would cause the saturation of V_t loss.

In erase state, a V_t drift-up with storage time is observed after P/E cycling. It shows a turn-around feature with the cycles numbers, and is found to be insensitive to the bake temperature. Tunnel detrapping of the positive oxide charges created in the bottom oxide during P/E stress is the cause. ONO process condition is critical to improve the reliability. By a charge separation technique, the measured transient substrate current is a direct indicator of the quality of the bottom oxide and the amount of the V_t drift-up.

A negative V_t shift, on the other hand, is found to increase with storage time in an over-erased cell. Such V_t drop-down gets more pronounced at higher temperature.

Lateral spreading of the excess-trapped holes is the root cause. It will result in channel shortening effect that induces the observed negative V_t shift. It may be a potential issue for future device scaling. Deriving from the thermionic emission model, the amounts of holes involved in the spreading should follow a straight line on a semi-log plot against the bake time with a slope proportional to the bake temperature. Accordingly, temperature-accelerating method is applicable in its qualification test.

Various read-disturb modes are clarified. It is found that at low vertical/lateral field, tunneling detrapping of cycling-induced positive oxide charges dominates the V_t shift, which is insensitive to temperature. Hot-carrier effect (drain field heating) dominates the V_t shift in a short-channel device, especially at low temperature. Gate voltage-enhanced V_t drift occurs even in a long-channel device, and it is much worse in a high-V_{ti} cell. The last two modes are attributed to positive oxide charges, which are created during P/E stress, that enhance electron injection into the trapping nitride. Process improvements and operating-method optimizations have been shown to be effective in suppressing these disturbs.

Regarding the cycling endurance, erase speed degradation in an NBit cell is finally investigated. Our study shows that the trapped-electron area of the second-programmed bit would extend more toward the central channel region if its neighboring bit (of the same cell) has been programmed. The second bit would then be erased more slowly. This effect gets more obviously after P/E cycling. In addition, the erase speed would be modulated by adjacent junction bias in a short-channel, nearly punch-through cell.

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Investigation of Reliability Issues in a Nitride-Based Localized Charge Storage Flash Memory Cell

Vita

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Publication List

(A) Journal Papers:

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