國立交通大學

光電工程研究所

博士論文

高介電係數介電質於五苯有機薄膜電晶體及金氧半場效電晶體之研究

The Researches of High-κ Dielectrics on Pentacene Based OTFTs and MOSFETs

研 究 生：張明峯
指導教授：李柏璁 博士
荊鳳德 博士

中華民國九十九年六月

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荊鳳德　博士　　Dr. Albert Chin

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光電工程研究所博士班

摘要

由於以五苯(pentacene)為主動層之有機薄膜電晶體可廣泛的應用於無線射頻身分識別標籤、邏輯電路、顯示器驅動元件、感測元件，因此五苯有機薄膜電晶體成為世界上各研發單位的重要研究課題之一，且在元件性能上屢有重大的突破與進展。在本研究論文中，我們將探討高介電系數介電層在有機薄膜電晶體的應用，並研究分析高介電系數介電層對於元件特性的改善。

首先我們製作與整合高介電系數氧化鉿鑭(HfLaO)介電層與氮化鉭(TaN)金屬閘極於五苯有機薄膜電晶體，此元件量測到低的操作電壓、小的次臨界擺幅、低的臨限電壓、良好的場效遷移率。此良好的元件特性可以說明氧化鉿鑭介電層適合應用於有機薄膜電晶體。

為了達到未來可撓式電子的需求，我們降低製程溫度在可撓的聚亞醯胺基板

上製作氧化鉿鑭/五苯有機薄膜電晶體。此元件也展現良好的元件特性，在低的 2.5 伏操作電壓下，量測到 0.13 V/decade 的次臨界擺幅、-1.24 伏的臨限電壓、0.13 cm^2/V·s 的場效遷移率。

根據製作高介電系數氧化鉿鑭為介電層之五苯有機薄膜電晶體所得到的良好電性，我們進一步發展使用高介電系數氮氧化鉿(HfON)為電荷捕捉層，在可撓的聚亞醯胺基板上製作非揮發性五苯有機薄膜電晶體記憶體元件。利用高介電系數介電材料氮氧化鉿為電荷捕捉層、氧化鉿鑭為電荷阻擋層和二氧化鉿(HfO_2)為電荷穿隧層，五苯有機薄膜電晶體記憶體元件可以得到低的寫入與抹除電壓。

最後我們探討在氮氧化矽(SiON)上，以高介電系數氧化鉿鋁(HfAlO)介電層為覆蓋層去調變臨界電壓，使其適用於 p 型金氧半場效電晶體，我們也分析調變臨界電壓的物理機制。在最佳 1.5 奈米厚的氮氧化矽，氮化鉬(MoN)/氧化鉿鋁/氮氧化矽 p 型金氧半場效電晶體可得到 0.85 奈米的等效氧化層厚度、低的臨界電壓、良好的次臨界擺幅、高的場效遷移率。平帶電壓朝正電壓方向改變被證明是由於氧化鋁(Al_2O_3)與氮氧化矽的交互擴散與反應，形成氧化矽鋁(AlSiO)矽化物並造成帶電的氧空缺。

The Researches of High-κ Dielectrics on Pentacene Based OTFTs and MOSFETs

Student: Ming-Feng Chang **Advisors: Dr. Po-Tsung Lee**
Dr. Albert Chin

Department of Photonics & Institute of Electro-Optical Engineering

National Chiao Tung University

ABSTRACT

Due to the widespread applications such as radio frequency identification tags, logic circuits, display driver and sensors, the pentacene-based organic thin film transistors (OTFTs) are widely investigated and have many remarkable breakthroughs in performance. In this dissertation, we investigate the application of high dielectric constant (κ) dielectric to improve the performance and function of OTFTs.

First of all, we demonstrate the integration of HfLaO high-κ dielectric and TaN metal gate into pentacene OTFTs to get low operation voltage, small sub-threshold swing (SS), low threshold voltage (V_T) and good field effect mobility (μ). Theses results indicate HfLaO is a good dielectric for OTFTs.

In order to meet the requirements of future flexible electronics, we decrease the process temperature to develop HfLaO/pentacene OTFT on flexible polyimide substrates. This device also shows good device integrity of a small *SS* of 0.13 V/decade and a V_T of −1.25 V and a good μ of 0.13 cm^2/V·s at a low operating voltage of 2.5 V.

Based on the good electrical characteristics of pentacene OTFT incorporated with high-κ HfLaO dielectrics, we further use high-κ HfON as a charge trapping layer to develop organic pentacene non-volatile OTFT memory fabricated on flexible polyimide substrate. By using high-κ HfON as a charge trapping layer, HfLaO as a blocking layers and HfO_2 as a tunneling layer, the pentacene OTFT memory shows record low program/erase voltage.

Finally, we study the High-κ HfAlO as a capping layer on SiON to modulate V_T for *p*-MOSFET application. The mechanisms of V_T modulation also have been investigated. Under the optimized 1.5 nm SiON, good device integrity of small 0.85 nm equivalent-oxide-thickness, low V_t, good *SS* and high mobility are obtained in the MoN/HfAlO/SiON *p*-MOSFETs. The large positive flatband voltage shift is explained due to the forming charged oxygen vacancies in AlSiO silicate, which is originated from diffusion and interaction of Al_2O_3 and SiON.

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Contents

Chapter 1 Introduction

Chapter 2 Low Sub-threshold Swing HfLaO/Pentacene Organic Thin Film Transistors

Chapter 3 Small Sub-threshold-Swing and Low-Voltage, Flexible Organic Thin Film Transistors which use HfLaO as the Gate Dielectric

Chapter 4 A Flexible Organic Pentacene Nonvolatile Memory Base on High-κ Dielectric Layers

Chapter 5 Interfacial SiON Thickness Dependence on Device Performance of High-κ MoN/HfAlO/SiON *p*-MOSFETs

Table Captions

Chapter 1 Introduction

Chapter 2 Low Sub-threshold Swing HfLaO/Pentacene Organic Thin Film Transistors

Chapter 3 Small Sub-threshold-Swing and Low-Voltage, Flexible Organic Thin Film Transistors which use HfLaO as the Gate Dielectric

Figure Captions:

Chapter 1 Introduction

Chapter 2 Low Sub-threshold Swing HfLaO/Pentacene Organic Thin Film Transistors

Chapter 3 Small Sub-threshold-Swing and Low-Voltage, Flexible Organic Thin Film Transistors which use HfLaO as the Gate Dielectric

Chapter 4 A Flexible Organic Pentacene Nonvolatile Memory Base on High-κ Dielectric Layers

Chapter 5 Interfacial SiON Thickness Dependence on Device Performance of

High-κ MoN/HfAlO/SiON *p*-MOSFETs

Chapter 1

Introduction

1.1 Overview of High-κ Gate Dielectrics

As the physical thickness of Silicon dioxide (SiO_2) based gate dielectric is small than 1.5 nm, a number of fundamental problems arise in metal-oxide-semiconductor field-effect transistor (MOSFET). Below the physical thickness of 1.5 nm, the gate leakage current exceeds the 1 A/cm^2 due to tunneling mechanism as shown in Figure 1-1 [1.1]. To continue scaling down of SiO_2 and to reduce gate leakage current, hafnium-based high dielectric constant (high-κ) materials have been used to replace SiO_2 as gate dielectric at 45 nm node and beyond [1.2, 1.3].

From an electrical point of view, an MOSFET is a capacitance-operated device, where the source–drain current of the MOSFET depends on the gate capacitance.

$$C = \frac{\varepsilon_o \kappa A}{t} \tag{1}$$

where ε_o is the permittivity of free space, κ is the dielectric constant (also referred to relative permittivity), A is the area of capacitor, and t is the oxide thickness. Since the tunneling probability reduces exponentially with the gate dielectric thickness, the tunneling problem can be solved by replacing SiO_2 with a physically thicker layer of high-κ material. This will keep the same capacitance but decrease the tunneling current.

Many high-κ materials have been studied as potential alternative gate dielectrics, such as Ta_2O_5, TiO_2, HfO_2, ZrO_2, Al_2O_3, La_2O_3, Si_3N_4 or mixtures of them or metal-oxide-silicates of the mentioned compounds which have the κ values ranging from 7 to 80. For the aforementioned requirements, the κ value of high-κ material should be over 12, preferably 25-30. Unfortunately, each of these materials is found to have its drawbacks. There is a trade off with the band offset condition, which requires a reasonably large band gap to obtain acceptable gate leakage current [1.4, 1.5]. Table 1 and Figure 1-2 show that the κ value of candidate oxides tends to vary inversely with the band gap. Al_2O_3 and Si_3N_4 were found to have small κ value <10, which can not meet our future requirements. TiO_2 has high-κ value of 80, but it is found to have a low crystallization temperature of about 400 ^{o}C and low conduction band offset.

The κ value of all transition metal oxides is higher than SiO_2. However, not every high-κ oxide can be used as a gate dielectric material. The thermal SiO_2, having been used and studied intensively for more than 40 years, has excellent interface properties with the Si substrate. Instead, the high-κ materials are far less familiar to us and most of their properties are still unclear. For gate dielectric application, the high-κ materials must have several advanced features in addition to the high-κ value. They should be chemically stable with substrate and the gate electrode and thermally stable at required process temperatures. Moreover, they should have good interface properties with the channel materials so that the structure can have low interface trap density, high channel mobility, low oxide trap density, large band gap, and large band offset.

1.2 Organic Thin Film Transistors

Organic semiconductors have been studied since the late 1940s [1.6]. However, the first description of field effect in organic semiconductor was in 1970 [1.7, 1.8]. Figure 1-3 shows the molecular structures of several common p-type organic semiconductors. Organic thin film transistors (OTFTs) have been identified as potential elements of electronic devices since the report by Koezuka and coworkers using electrochemically polymerized polythiophene in 1986 [1.9]. The performance of OTFTs has undergone great progress, especially in the last several years. OTFTs have many advantages over conventional silicon technology: they can be fabricated at low cost, large area coverage and on flexible substrates. They have attracted considerable attention for use in a wide range of cost effective, high volume applications such as radio frequency identification tags, logic circuits, display driver and sensors [1.10-1.16]. Compared to the performance of field-effect transistors based on single-crystalline inorganic semiconductors, such as Si and Ge, the charge carrier mobility is about several orders of magnitude lower. However, recently, the mobility of OTFTs based on rubrene single crystals was found to be 15.4 cm^2 /Vs [1.17], which exceeds that of amorphous silicon (a-Si : H) devices.

1.2.1 Charge Transport in Organic Semiconductors

The primary difference between organic semiconductors and inorganic semiconductors is the nature of charge transport. In inorganic semiconductors, such as Si or Ge, the atoms are held together by strong covalent bonds. The strong covalent bonds between atoms lead to the existence of large conduction and valance band widths. The nature of charge transport in inorganic semiconductors is band-like as the system has definite order. The charge carrier mobility of inorganic semiconductors such as single-crystalline Si is very high, of the order of 10^3 cm^2/Vs. The carrier mobility in inorganic semiconductors reduces with increasing temperature because the lattice vibrations (phonons) cause scattering.

However, the bonding between organic molecules is weak van der Waals forces. Band-like transport model is invalid in amorphous or organic semiconductors. The charge carrier mobility of organic semiconductors is several orders of magnitude lower than inorganic materials. The nature of charge transport in organic semiconductors is more of the hopping kind. Crystalline organic semiconductors can have band-like transport at low temperatures. In disordered materials, a variety of trap states further lower the mobility. Energy states are localized in disordered organic materials and charge transfer takes place by hopping. Due to the charge carrier scattering at every step, the carrier mobility is significantly lower. In most organic semiconductors, the mobility increases with increasing temperature as hopping transport is assisted by phonons [1.18, 1.19].

The Multiple Trapping and Release (MTR) model is employed to explain charge transport in organic semiconductors [1.20]. The model suggests a narrow delocalized band be associated with a high concentration of localized levels that act as traps. At low gate voltages, a majority of charge carriers injected in the semiconductor get trapped in these localized states with the deep traps filling up first. As the gate voltage is increased, more traps get successively filled and the Fermi level approaches the valence band edge. In some cases, when a sufficiently high gate voltage is achieved, all trap states are filled and the subsequently injected carriers move with the mobility associated with carriers in the valence band [1.21, 1.22]. However, the temperature-independent mobility reported in some cases (Pentacene and oligothiophenes) is not accounted for by the MTR model [1.23-1.25]. Thus, the mechanisms for charge transport between molecules could be band-like transport, hopping, or tunneling [1.26-1.29]. At room temperature, the boundary between the band and hopping transport is usually taken at a mobility between 0.1 and 1 $cm^2/V.s$ [1.23, 1.30]. The mobility in highly ordered molecular crystals or single crystal molecular is exceeding to that limit, so that there is still controversy as to whether the conductivity in these materials should be described by localized or delocalized transport.

1.2.2 The Operation Mode and Principles of OTFTs

The general operation mode and structure of OTFTs are developed from insulated gate field-effect transistors fabricated from crystalline or amorphous inorganic semiconductors [1.30]. Figure 1-4 shows the common device configurations used in OTFTs. It is composed of three main components: source, drain, and gate electrodes; a gate dielectric; and an organic semiconductor as a channel layer. The p-type organic semiconductors such as pentacene or P3HT use Au, Pt, or Ni metals with high work function as source and drain electrode to form ohmic-like contact. Although the device structures of OTFTs and inorganic TFTs are similar, there are some differences in the operation mode.

The organic semiconductors are difficult to dope to another type. There are no P-N junctions in source and drain to reduce the off-state leakage current. The low off-state leakage current of OTFTs is due to low conductivity of organic semiconductors. The most OTFTs operate in accumulation or depletion modes that are different compare with inversion mode operation of poly-Si TFT or MOSFET.

The current-voltage characteristics of OTFTs can be divided in two regimes, linear and saturation regimes as following:

At low drain voltage (V_D), drain current (I_D) increases linearly with V_D (linear regime) and is approximately determined from the following equation:

$$I_D = \frac{W}{L}\mu C_i (V_G - V_T - \frac{V_D}{2}), \quad V_D < V_G - V_T \tag{2}$$

where L is the channel length, W is the channel width, C_i is the capacitance per unit area, V_T is the threshold voltage, V_G is the gate voltage and μ is the field effect mobility.

For higher V_D, exceed V_T, I_D tends to saturate (saturation regime) due to the pinch-off of the accumulation layer, and is modeled by the equation

$$I_D = \frac{W}{2L}\mu C_i (V_G - V_T)^2, \quad V_D > V_G - V_T \tag{3}$$

1.2.3 Parameter Extraction of OTFTs

There are actually four important parameters to be determine the quality of OTFTs: mobility, threshold voltage, sub-threshold swing and on-off-state drive current ratio.

(1) Mobility

In the linear regime, the field effect mobility can be calculated from the transconductance (g_m), which follows from the first derivative of Equation (2) with respect to the V_G.

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L}\mu C_i V_D \tag{4}$$

In the saturation regime, the mobility can be calculated by rewriting Equation (3) as:

$$\sqrt{I_D} = \sqrt{\frac{W}{2L}\mu C_i}(V_G - V_T) \tag{5}$$

Equation (5) predicts that plotting the square root of the saturation current against V_G would result a straight line. The mobility is obtained from the slope of the line.

(2) Threshold voltage

Threshold voltage is defined as the onset voltage for the channel formation. The magnitude of threshold voltage corresponds to power consumption. It can be extracted from Equation (5) by the x-intercept of $|I_D|^{1/2} - V_G$ plot.

(3) sub-threshold swing

Sub-threshold swing (*SS*) controls the on-to-off voltage swing, and should be as low as possible. The *SS* also represents the interface quality and is defined as

$$SS \equiv \left.\frac{\partial V_G}{\partial \log I_D}\right|_{V_D=\text{constant}} = \frac{KT}{q} \times \ln 10 \times \left(1 + \frac{C_{dep} + C_{it}}{C_i}\right) \tag{6}$$

where C_{dep} is the depletion capacitance density of semiconductor channel layer and C_{it} is the capacitance density from charged interface traps.

(4) on-off-state drive current ratio

The major potential application of TFTs is to control the switching of every pixel in active-mattress liquid crystal display (AMLCD). The high on-off-state current ratio

(I_{on}/I_{off}) can be helpful to define the logic level of digital signal. The I_{on}/I_{off} represents the ratio of the current when the device is turned on and when the device is in the off state. It is another important OTFTs characteristic and is given as

$$I_{on}/I_{off} = \frac{\mu C_i V_G}{2\mu_r q N_A t} \tag{7}$$

where μ_r and N_A are the semiconductor mobility and carrier concentration (in the off-state), respectively, t is the semiconductor film thickness, and q is the electron charge. Therefore, the high I_{on}/I_{off} can be obtained by large carrier mobility and a very low off-conductivity value for the organic semiconductor. Note that Equations (7) are valid only when a number of conditions are satisfied [1.30, 1.31].

1.3 Motivation

Although the mobility of OTFTs is higher than 1 $cm^2/V.s$, there are still several electrical characteristics need to be improved such as threshold voltage, sub-threshold swing and operation voltage for commercial application. Therefore, how to enhance these characteristics is important.

The goal of our study is to improve the device performance by integrating high-κ dielectric into pentacene-based OTFTs. In addition to the logic function of OTFTs, the nonvolatile memory function is required for system-on-panel (SOP) application. We also investigate organic pentacene nonvolatile memory based on high-κ dielectric layers.

On the other hand, the threshold voltage control is a critical issue of metal-gate high-κ MOSFETs. The flatband voltage is affected by the interface of High-κ dielectric and SiO_2. For this reason, we use high-κ HfAlO as a capping layer on SiON to study the flatband voltage shift and device performance of MoN/HfAlO/SiON *p*-MOSFETs.

1.4 Dissertation Organization

This dissertation is organized as follow:

In Chapter 2, we discuss the device performance of OTFTs that incorporates high-κ HfLaO as the gate dielectric. The effects of surface treatment on TaN gate electrode are discussed along with the electric characteristics of OTFTs. The focus of this research is the integration of pentance based OTFT with high-κ HfLaO to reach good electrical characteristics such as a low SS and small V_T.

In Chapter 3, we study the integration of pentacene OTFTs with a high-κ HfLaO dielectric onto flexible substrates.

In order to further extend the function of OTFTs, we develop a pentacene OTFT nonvolatile memory fabricated on a flexible polyimide substrate in Chapter 4. This memory function has been achieved by using a high-κ dielectric as charge trapping, blocking, and tunneling gate insulator layers.

A comprehensive study of flatband voltage shift and device performance with

HfAlO capping SiON p-MOSFETs is mentioned in Chapter 5. The mechanisms of flatband voltage shift are discussed. By optimizing thickness of SiON, the good device performance of MoN/HAlO/SiON p-MOSFET can be reached.

A summary of the research work carried out is given in Chapter 6.

Table 1-1 Comparison of relevant properties for high-k candidates [1.4].

Material	**Dielectric constant (κ)**	**Band gap (ev)**	**ΔEc (ev) to Si**	**Crystal Structure**
SiO_2	**3.9**	**9**	**3.2**	**Amorphous**
Si_3N_4	**7**	**5.3**	**2.4**	**Amorphous**
Al_2O_3	**9**	**8.8**	**2.8**	**Amorphous**
Y_2O_3	**15**	**6**	**2.3**	**Cubic**
La_2O_3	**30**	**6**	**2.3**	**Hexagonal, cubic**
Ta_2O_5	**22**	**4.4**	**0.35**	**Orthorhombic**
TiO_2	**80**	**3.5**	**0**	**Tetragonal (rutile, anatase)**
HfO_2	**25**	**5.8**	**1.4**	**Monoclinic, Tetragonal, Cubic**
ZrO_2	**25**	**5.8**	**1.5**	**Monoclinic, Tetragonal, Cubic**

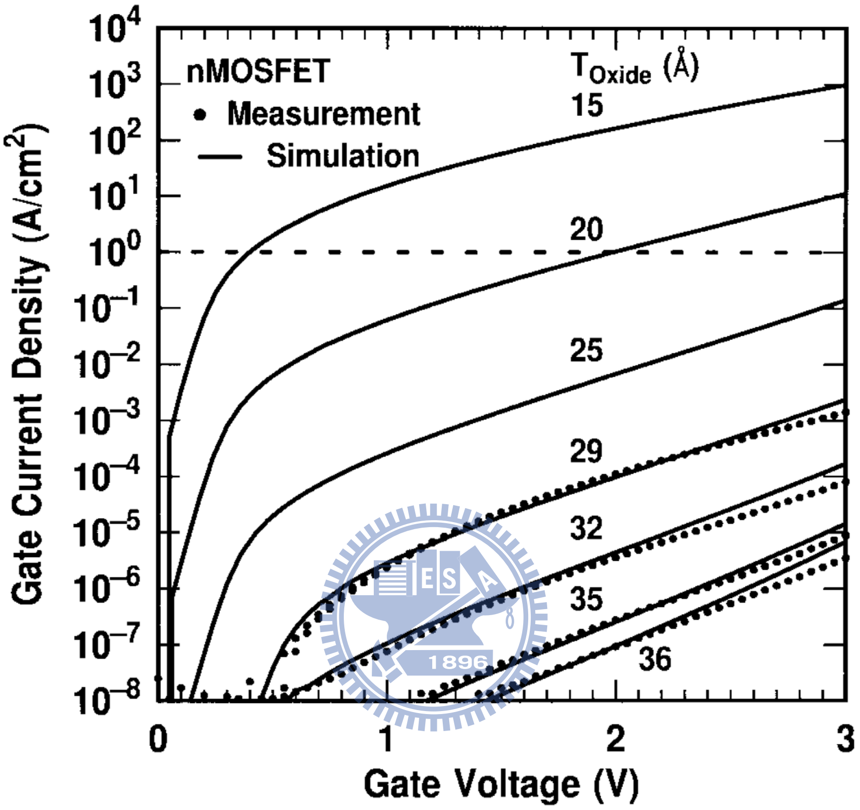


Fig. 1-1. Leakage current versus voltage for various thickness of SiO_2 layers [1.1].

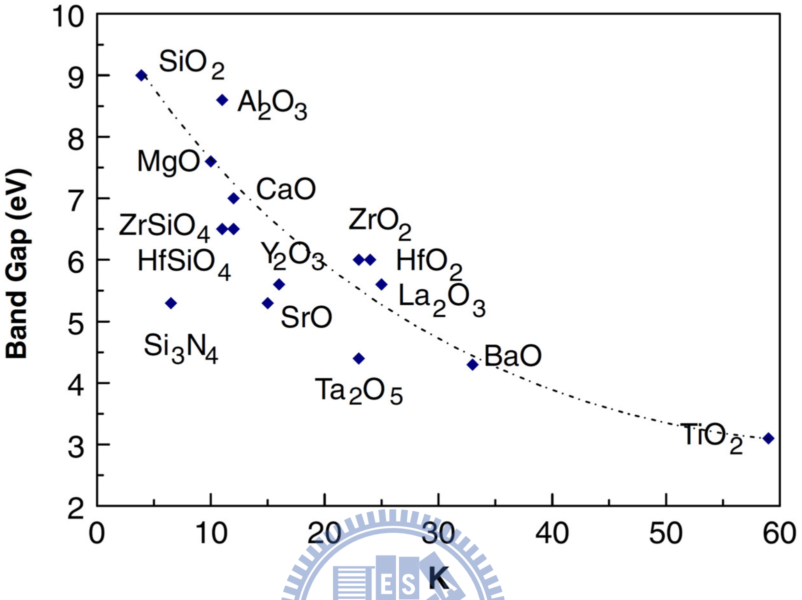


Fig. 1-2. Static dielectric constant versus band gap for candidate gate oxides [1.5].

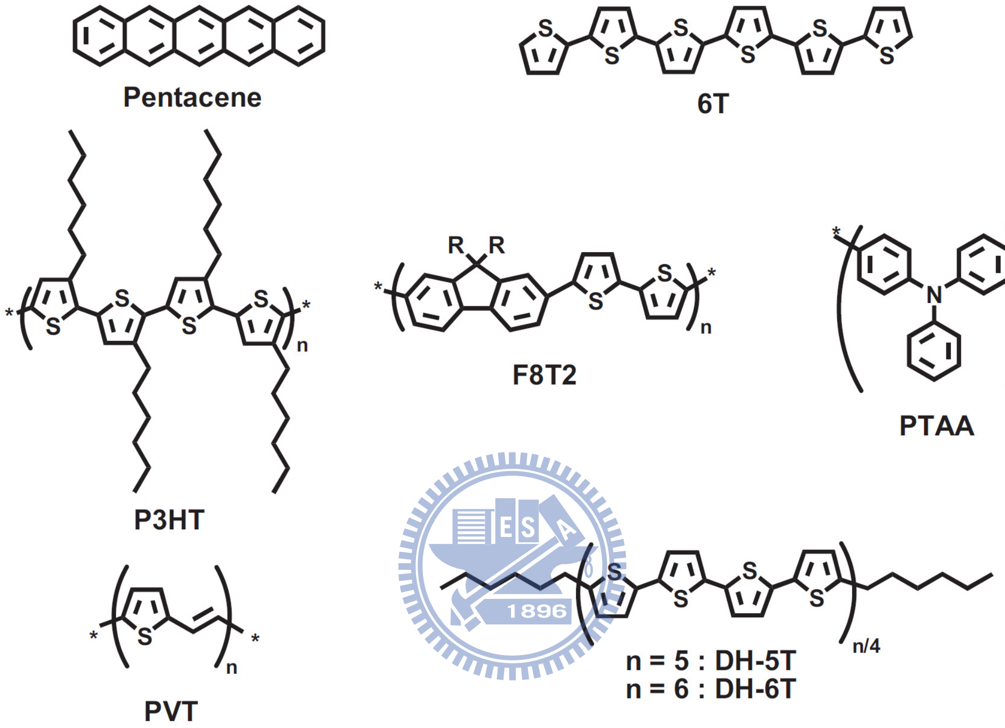


Fig. 1-3. Molcular structure of common p-type organic semiconductors: Pentacene, 6T (sexthiophene), P3HT (regioregular poly(3-hexylthiophene)), F8T2 (poly(9,9'dioctylfluorene-co-bithiophene)), PTAA (polytriarylamine), PVT (poly(2,5-thienylene vinylene)), DH-5T (α,ω-dihexylquinquethiophene), DH-6T (α,ω-dihexylsexithophene) [1.31].

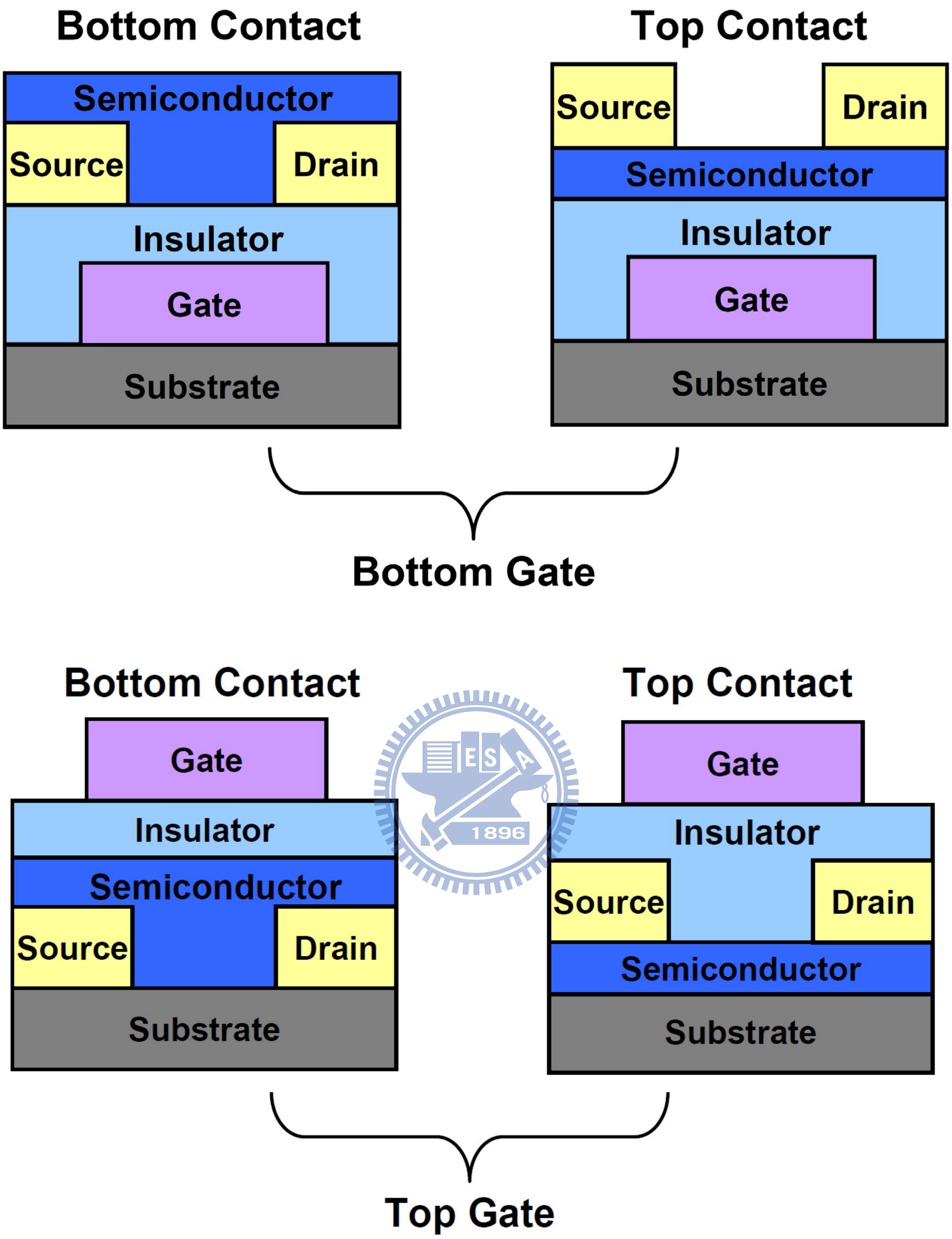


Fig. 1-4. Various device structures of OTFTs.

Chapter 2

Low Sub-threshold Swing HfLaO/Pentacene Organic Thin Film Transistors

2.1 Introduction

Poly-Si thin-film transistors (TFTs) [2.1]-[2.6] are currently used for active matrix liquid crystal displays (AMLCDs) on glass substrates. These poly-Si TFTs are operated in inversion mode, and the ion-implantation for the n^+ source-drain requires activation using furnace annealing at 600°C, typically for ~12 hours. This extended annealing slows down the process sequence and the large thermal budget is unfavorable for environment energy conservation. In contrast, organic TFTs (OTFTs) [2.7]-[2.9] can be processed with a significantly lower thermal budget, and without requiring ion implantation or an extended dopant activation period. This is because the OTFTs can be operated in the accumulation mode, where ohmic-like source-drain contacts are used rather than ion-implanted n^+ source-drain regions. Unfortunately, for OTFTs their low hole mobility and poor sub-threshold swing (*SS*) limit the drive current when operated at low voltage [2.7]-[2.9]. The poor *SS* leads to inverters being slow when used in logic circuits. In this chapter we study using high-κ HfLaO [2.10]-[2.12] as the gate dielectric for OTFTs, with the aim of addressing the above issues. Besides displaying a high-κ value of up to 24, HfLaO permits low-temperature processing due to the strong metal-oxide bond enthalpy of both Hf-O and La-O [2.13]. The adding La_2O_3 into HfO_2 is especially important to decrease the leakage current at low temperature process due to the larger conduction band offset of La_2O_3 (2.3 eV to Si) than that of HfO_2 (1.5 eV to Si) [2.14]. The HfLaO MOSFET also shows less Fermi-level pinning than using HfO_2 [2.10]-[2.12].

2.2 Experimental Details

The devices were fabricated on a thick SiO_2 layer grown on Si wafers to mimic poly-Si TFTs fabricated on glass substrates [2.2]. A 50 nm thick TaN gate electrode was then deposited on the SiO_2/Si, through a shadow mask, using reactive sputtering. The surface of the TaN gate was subsequently treated with an NH_3 plasma to improve the gate leakage current [2.14]-[2.16]. Such nitrogen plasma treatment is the key factor to achieve low leakage current and small EOT in previous DRAM capacitors [2.14]-[2.16]. The 20 nm thick HfLaO gate dielectric was then deposited by electron beam evaporation and annealed in O_2 at $350^{\circ}C$ for 10 min. Next, pentacene (Aldrich Chemical Co.) was evaporated through a shadow mask onto the sample to form an active layer 70 nm thick. This evaporation was performed at a deposition rate of 0.5 Å/s at $70^{\circ}C$, under a pressure of 3×10^{-6} torr. Finally, Au source/drain electrodes, 50 nm thick, were deposited onto the pentacene. The devices had a channel length of 80 μm and width of 2000 μm. We also deposited Au directly onto HfLaO/TaN to make 200×200 μm^2 capacitors to analyze the dielectric properties. The devices were characterized using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter, under dark and air ambient conditions.

2.3 Results and Discussion

In Figure 2-1 we show the schematic diagram of OTFT. The *J-V* characteristics of Au/HfLaO/TaN capacitors are shown in Figure 2-2. The NH_3 plasma treatment improves the leakage current of both electron injection from top Au/HfLaO and bottom HfLaO/TaN with close capacitance density shown in Figure 2-3. It is important to notice that the leakage current is much worse as electron injected from bottom interface, which is consistent with previous Analog/RF and DRAM MIM capacitors [2.14]-[2.16]. However, such bottom electron injection is needed for the negative V_G used in p-channel OTFTs. The data with NH_3 plasma treatment indicate a leakage current of 5.1×10^{-7} A/cm^2 at 2 V, at a capacitance density as high as 950 nF/cm^2. This gives an equivalent-oxide-thickness (EOT) of only 3.6 nm and a high-κ value of 21.7. Such a low leakage current at 2 V is better than previous high-κ $LaAlO_3$ poly-Si TFTs, which had a lower capacitance density of 390 nF/cm^2 (8.7 nm EOT) and involved annealing at higher 400°C for 30 min [2.6]. These observations point to the merit of using HfLaO as the gate dielectric.

The output characteristics (I_D-V_D) of a high-κ HfLaO/pentacene OTFT are displayed in Figure 2-4. The I_D-V_D characteristics with NH_3 plasma treatment are well-behaved, and suggest possible operation at 2 V, which has the advantage of reducing the power consumption ($I_D \times V_D$) in circuit operations. The I_D-V_D curves without NH_3 plasma treatment show poor characteristics that are due to high gate leakage current induced I_D lowering. The transfer characteristics (I_D-V_G), as shown in Figure 2-5, enable the extraction of the mobility (μ) and threshold voltage (V_T) from the $-I_D^{1/2}$ vs. V_G plot. The device with NH_3 treatment improves on current (I_{on}), *SS* and off current (I_{off}). The I_{on} improvement is not due to the pentacene, since the surface roughness and grain sizes are similar shown in Figure 2-6. The performance improvements are due to NH_3 plasma treatment to reduce gate leakage current. The device with NH_3 plasma treatment shows a record small *SS* of only 78 mV/decade, a V_T of -1.3 V, and a good μ of 0.71 cm^2/V.s, along with an on-off-state drive current ratio (I_{on}/I_{off}) as high as 1.0×10^5. To analyze the low *SS*, we used the relationship:

$$SS = \frac{KT}{q} \times \ln 10 \times (1 + \frac{C_{dep} + C_{it}}{C_i}) \qquad (1)$$

where C_{dep} is the depletion capacitance density of pentacene, C_{it} is the capacitance density from charged interface traps and C_i is the gate capacitance density. Here the *SS* controls the on-to-off voltage swing, which should be as low as possible for high-speed and low-voltage operation. The *SS* of only 0.078 V/decade is better than that for poly-Si TFTs [2.1]-[2.6] and OTFTs [2.7]-[2.9] and is close to theoretical minimum value of 0.06 V/decade at room temperature. We attribute these results to the high C_i of 950 nF/cm^2 and small EOT of 3.6 nm, resulting from the use of advanced high-κ HfLaO dielectric even processed at low temperature.

The important device parameters are detailed in Table I, where the data from conventional n-channel poly-Si TFTs using solid phase crystallization (SPC) and LPCVD or PECVD oxides [2.3]-[2.5] are included for comparison. Note that the μC_i term is directly related to $I_D\,(W/2L \times \mu C_{\mathrm{i}}(V_G\text{-}V_T)^2)$, normalized to the channel length L, channel width W, and over-drive voltage of V_G-V_T. The performance of our HfLaO OTFTs is comparable with that of poly-Si TFTs, which incorporate LPCVD and PECVD TEOS oxides [2.3]-[2.5], but with the additional merits of a better *SS*, lower V_T, faster process sequence and lower thermal budget process.

2.4 Summary

We have fabricated and characterized low voltage OTFTs that incorporate high-κ HfLaO as the gate dielectric. These devices exhibit good electrical characteristics such as a low *SS* of only 0.078 V/decade, a high gate capacitance density of 950 nF/cm^2, a low V_T of -1.3 V, a good μ of 0.71 cm^2/Vs and a large I_{on}/I_{off} of 1.0×10^5. This superior performance permits the devices to be operated at 2 V, which could be useful for display applications.

Table 2-1 Comparison of p-channel HfLaO/pentacene OTFTs with n-channel poly-Si TFTs.

	HfLaO	LPCVD SiO_2	PECVD TEOS oxide	PECVD TEOS oxide
Gate dielectric	20 nm	80 nm [2.3]	60 nm [2.4]	40 nm [2.5]
Conduction channel	thermally evaporated pentacene	poly-Si by SPC	poly-Si by SPC	poly-Si by SPC
C_i (nF/cm^2)	950	43.1	57.5	86.3
V_T (V)	-1.3	5.6	8.14	Not extracted
μ (cm^2/Vs)	0.71	20	12.44	3
SS (V/decade)	0.078	1.4	1.97	2.67
μC_i (nF/Vs)	674.5	862.8	715.7	258.8
I_{on}/I_{off}	1.0×10^5	3.5×10^5	2.97×10^5	Not extracted

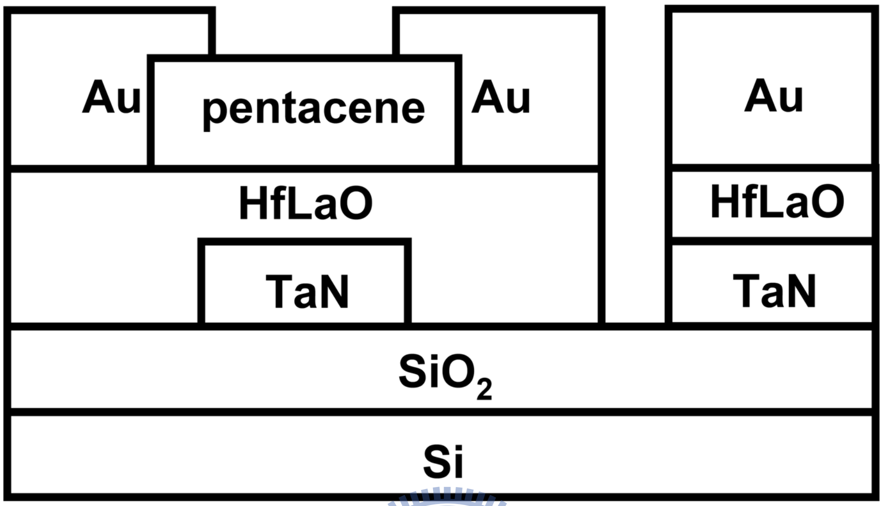


Fig. 2-1. Schematic diagram of HfLaO/pentacene OTFTs and Au/HfLaO/TaN MIM devices.

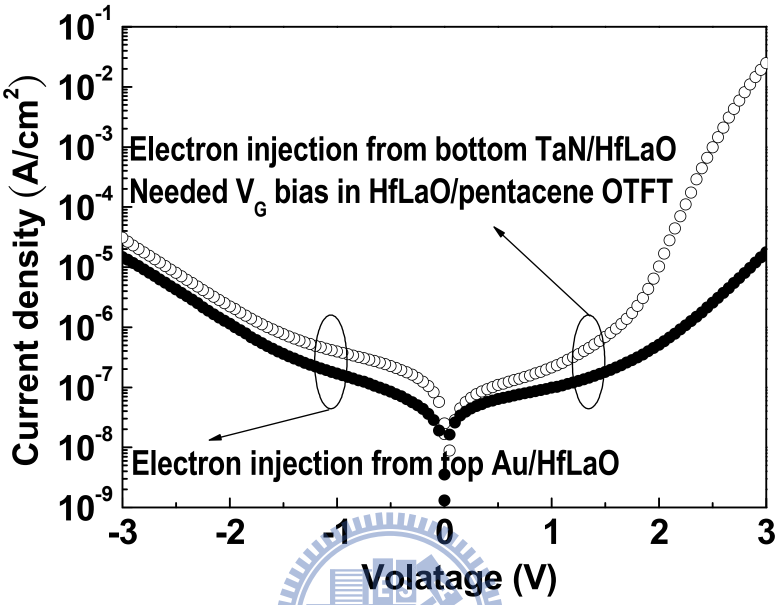


Fig. 2-2. Leakage current comparison of Au/HfLaO/TaN capacitors with and without NH_3 plasma treatment

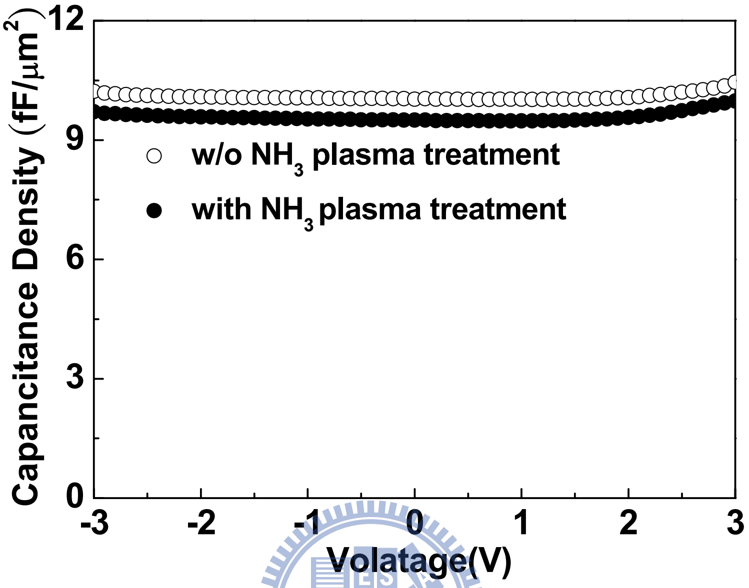
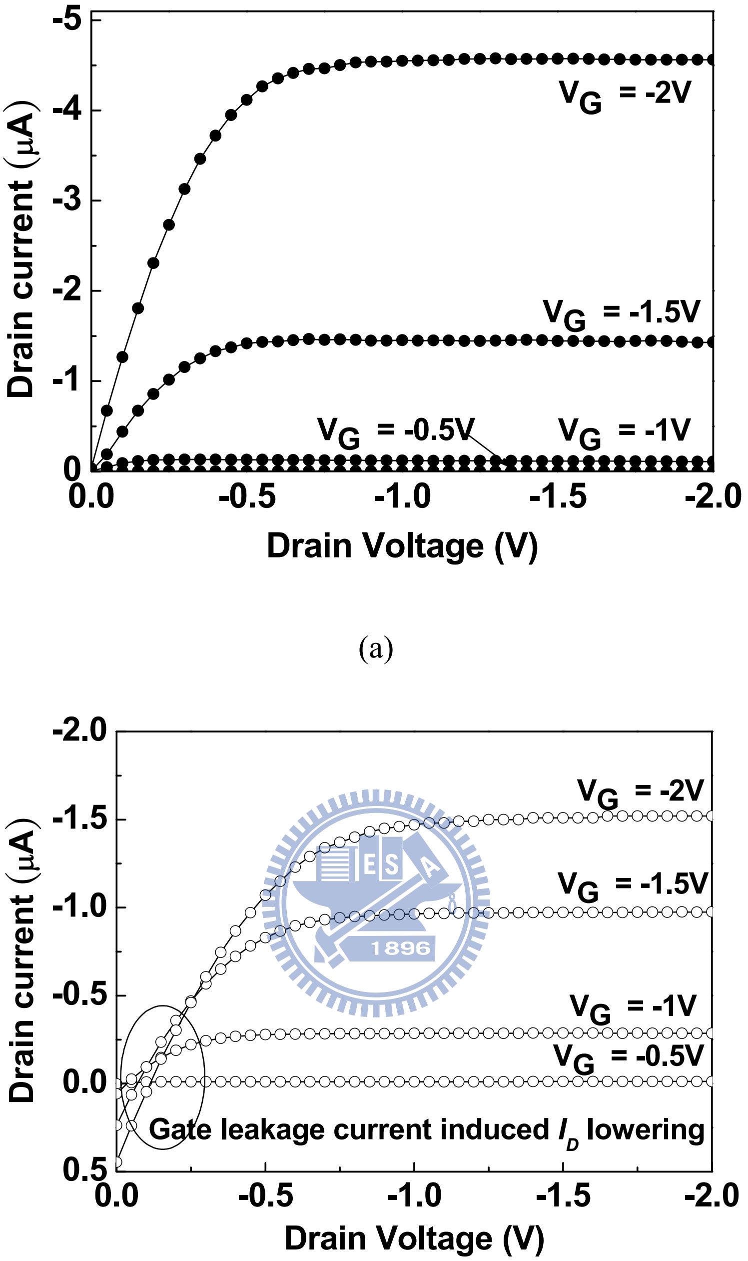


Fig. 2-3. *C-V* characteristics of Au/HfLaO/TaN capacitors with and without NH_3 plasma treatment.



(a)

(b)

Fig. 2-4. I_D-V_D characteristics of HfLaO gate dielectric OTFTs with (a) and without (b) NH_3 plasma treatment.

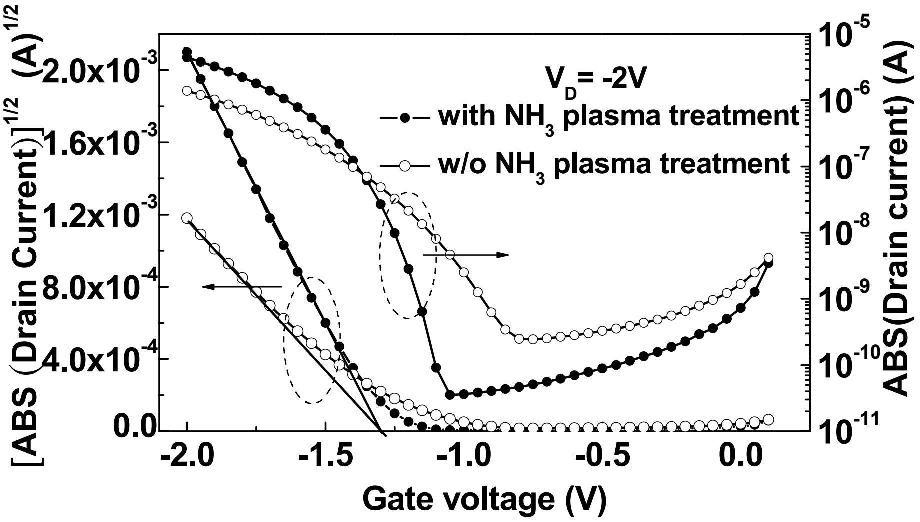


Fig. 2-5. $I_D^{1/2}$-V_G and I_D-V_G characteristics of HfLaO gate dielectric OTFTs with and without NH_3 plasma treatment.

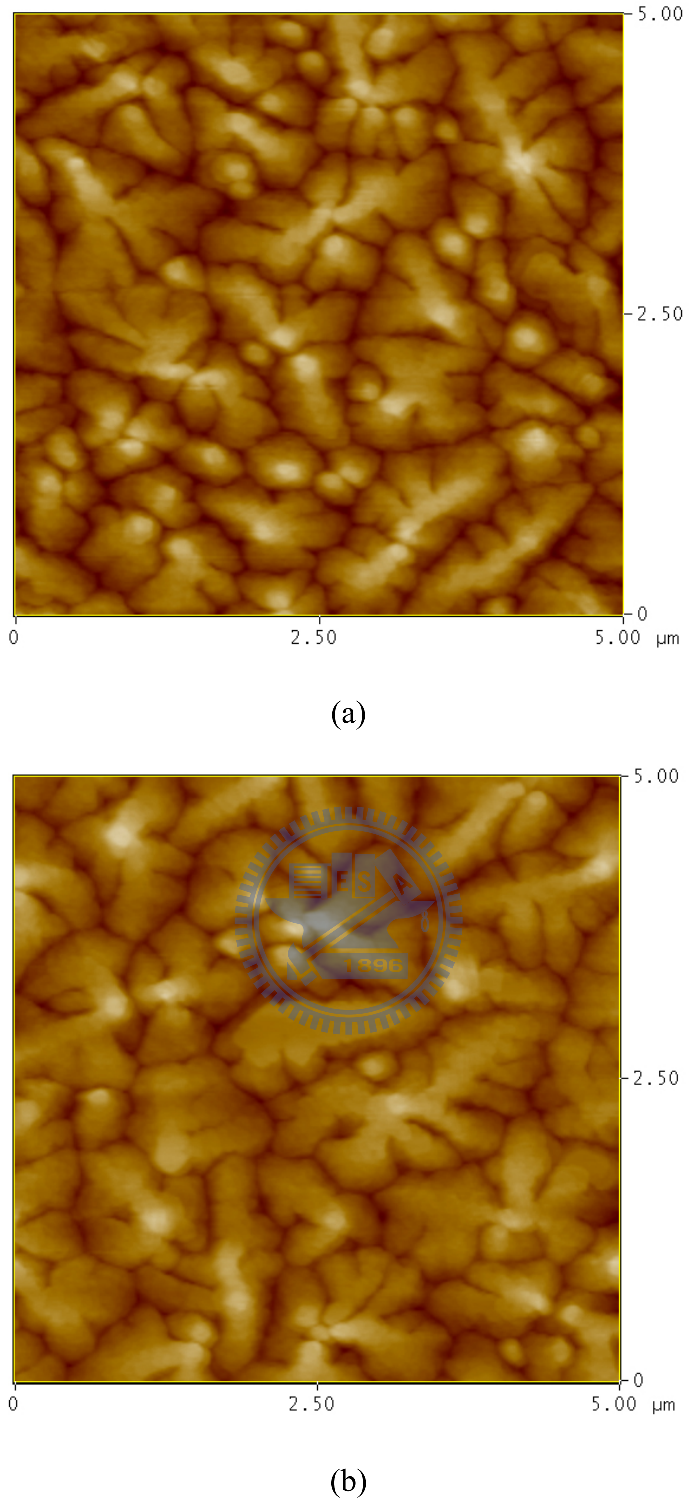


Fig. 2-6. AFM surface images of pentacene (5μm×5μm) on HfLaO/TaN with (a) and without (b) NH_3 plasma treatment.

Chapter 3

Small Sub-threshold-Swing and Low-Voltage, Flexible Organic Thin Film Transistors which use HfLaO as the Gate Dielectric

3.1 Introduction

Pentacene-based organic thin-film transistors (OTFT$_{S}$) have been intensely investigated due to their low cost and light weight, for potential use in applications such as flexible displays and low-cost flexible integrated circuits (IC) [3.1]-[3.3]. The low thermal budget and rapid processing have strong merits of energy saving and environment friendly, which in sharp contrast to the extended 600°C annealing times in conventional solid-phase crystallized (SPC) poly-Si TFTs. Although low thermal budget poly-Si TFTs can also be formed on plastic substrate using excimer laser annealing [3.4]-[3.5], the uniformity is a concern. Alternatively, poly-Si TFTs [3.6] or even single crystal sub-μm MOSFETs [3.7] can be realized on plastic substrate by fabrication first, separation and transfer, but these methods still require high thermal budget for device fabrication. However, conventional OTFTs require a high operating voltage and show a poor sub-threshold swing (*SS*), which detracts from their suitability in integrated circuit operations [3.8]-[3.10]. To address these issues, high-κ gate dielectrics have been applied in OTFTs for low–voltage operation [3.1], [3.3], [3.11]-[3.14]. In chapter 2 we have studied pentacene OTFTs, on SiO_2/Si substrates using high-κ HfLaO as the gate dielectric. Although the performance is comparable with SPC poly-Si TFTs, the process temperature of 350°C is still not suitable for flexible electronics. In this work we further decrease the process temperature to 200°C and demonstrate HfLaO/pentacene OTFTs, fabricated on low-cost flexible polyimide (PI) (Kapton HPP-ST, Dupont) substrates. These substrates are much more economical than other PI (Kapton E-type, Dupont) substrates [3.1], [3.11] and those which use polyethylene naphthalate (Teonex Q65 PEN, Dupont) [3.2].

3.2 Experimental Details

All the devices were fabricated on 125 μm thick PI substrates (Kapton HPP-ST, Dupont). Prior to the device fabrication process, the PI substrates were annealed in vacuum environment (3×10^{-6} torr) at 200°C [3.2]. A 100 nm SiO_2 thin film was deposited on the PI substrate by electron beam evaporation to ensure a low internal stress [3.3]. Then a 50 nm TaN gate electrode was deposited by reactive sputtering, through a shadow mask. The surface of the TaN gate was treated in an NH_3 plasma to reduce the gate leakage current [3.15]-[3.17]. A 30 nm thick HfLaO gate dielectric [3.18]-[3.21] was then deposited. A 200°C, 30 minute furnace O_2 treatment was then used to improve the gate oxide quality. Next, the pentacene active layer (Aldrich

Chemical Co.), 70 nm in thickness, was deposited through the shadow mask. A deposition rate of 0.5 Å/s, at a pressure of 3×10^{-6} torr was used, with a temperature of the substrate at 70°C. Finally, 50 nm of Au was deposited for the source/drain electrodes. The channel width and channel length were 2000 and 100 μm, respectively. Metal-insulator-metal (MIM) Au/HfLaO/TaN capacitors, 200×200 μm^2 in size, were also fabricated to analyze the leakage current and the dielectric properties. All electrical characteristics were measured using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter in the dark and an air ambient.

3.3 Results and Discussion

We show a schematic diagram and image of the OTFTs in Figs. 1(a) and (b). The *C-V* and *J-V* characteristics of the Au/HfLaO/TaN capacitors are detailed in Fig. 2 (a) and (b) respectively. A low leakage current of 3.5×10^{-6} A/cm^2 at 2.5 V was measured, along with a capacitance density of 450 nF/cm^2. This density yields an equivalent-oxide-thickness (EOT) of 7.7 nm and a high-κ value of 15.3.

The output characteristics (I_D-V_D) of a high-κ HfLaO OTFT are shown in Fig. 3. Good drain saturation behaviors were observed and suggest possible operation at 2.5 V. Fig. 4 shows the I_D-V_G characteristics of a representative OTFT, and mobility (μ) and threshold voltage (V_T) were determined from the $-I_D^{1/2}$ vs. V_G plot. The resulting values are: -1.25 V for V_T, 0.13 cm^2/Vs for μ, and an *SS* of 0.13 V/decade. The on-off-state drive current ratio (I_{on}/I_{off}) was 1.2×10^4. These values make the device suitable for high-switching-speed, low-power ICs. The *SS* controls the on/off voltage swing, and should be small. The *SS* of our device is better than values observed for other flexible pentacene OTFTs [3.1]-[3.3], [3.11], [3.12]. The low *SS* value arises from the high gate capacitance density and small EOT. The relatively smaller mobility and I_{on}/I_{off} were due to both lower operation voltage and poor surface roughness. A rms surface roughness of 4.3 nm was measured by Atomic Force Microscopy (AFM) on HfLaO and worse than the 2.0 nm value of BZN [3.3], which is originated from the poor 9.0 nm roughness of very low cost PI substrate (Kapton HPP-ST, Dupont).

In Table 3-1 we summarize some important device parameters, including other data of low-voltage flexible pentacene OTFTs using $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN), polyvinylphenol (PVP), Ta_2O_5, $TiSiO_2$ and Mn-doped $Ba_{0.6}Sr_{0.4}TiO_3$ (Mn-doped BST) as gate dielectrics, and fabricated on high quality PI (Kapton E-type) and PEN substrates [3.1]-[3.3], [3.11], [3.12]. The low-voltage OTFTs using (2-anthryl)undecoxycarbonyldecylphosphonic acid (π-σ-PA1)/AlO_x, octadecylphosphonic acid (OPDA)/AlO_x and HfLaO as gate dielectrics, fabricated on Si, glass and SiO_2/Si substrate are also list in Table 3-1 for comparison [3.13]-[3.14]. The value of the μC_i term is directly proportional to I_D ($W/2L\times\mu C_i(V_G-V_T)^2$), normalized to the channel length *L*, channel width *W*, and over-drive voltage of V_G-V_T.

The performance of our HfLaO OTFTs is comparable with other low-voltage flexible pentacene OTFTs for low-power applications, but with the additional merit of a good SS and the use of economical PI substrates.

3.4 Summary

A high-κ HfLaO dielectric was successfully integrated into pentacene OTFTs fabricated on low-cost flexible substrates. The electric characteristics of these HfLaO/pentacene OTFTs showed a low SS of only 0.13 V/decade, a high gate-capacitance-density of 450 nF/cm^2, a low V_T of -1.25 V, a good μ of 0.13 cm^2/Vs and a I_{on}/I_{off} of 1.2×10^4. This superior performance permits the devices to be operated at 2.5 V, which could be useful in flexible electronics.

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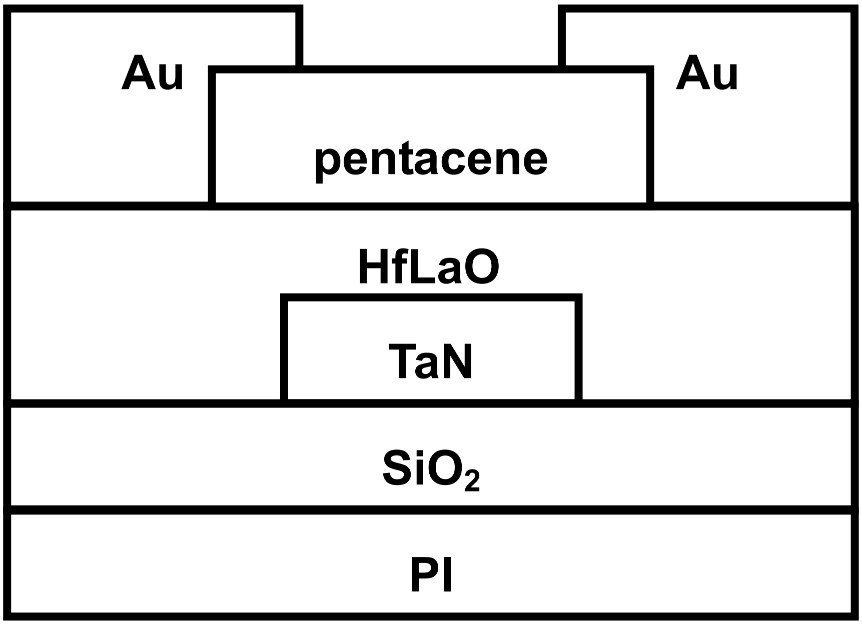
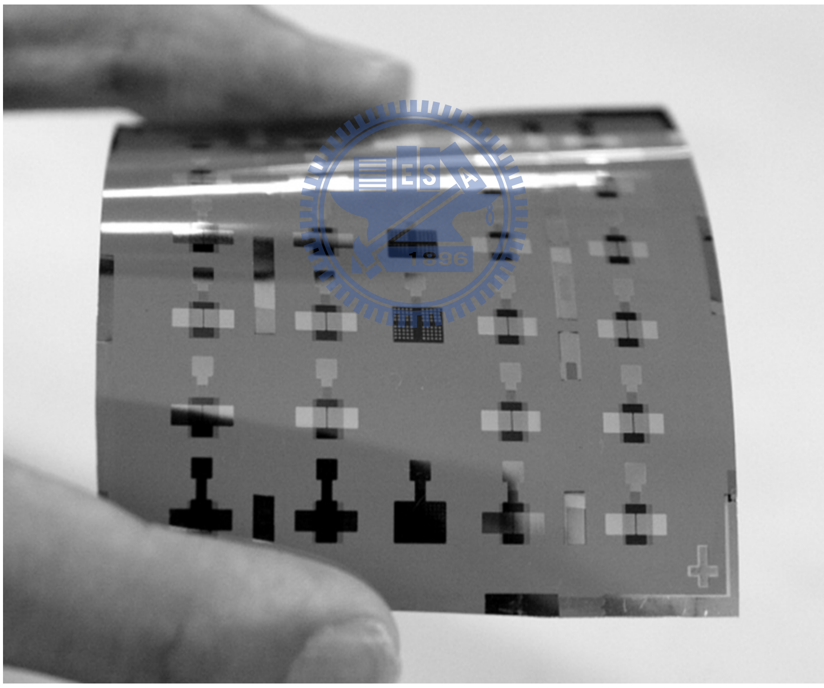
Table 3-1 Comparison of low voltage OTFTs with various gate dielectrics.

OTFTs with various gate dielectrics	**HfLaO [This work]**	**BZN [1]**	**PVP [2]**	**Ta_2O_5 [3]**	**Mn-doped BST [11]**	**$TiSiO_2$ [12]**	**π-σ-PA1 /AlOx [13]**	**OPDA/ AlO_x [14]**	**HfLaO**
substrate	**PI Kapton HPP-ST**	**PI Kapton E-type**	**PEN**	**PEN**	**PI Kapton E-type**	**PEN**	**Si**	**glass**	**SiO_2/Si**
Dielectric thickness (nm)	**30**	**200**	**50**	**150**	**200**	**136.4**	**-**	**-**	**20**
Operating voltage (V)	**2.5**	**2**	**8**	**12**	**10**	**5**	**3**	**2**	**2**
C_i (nF/cm^2)	**450**	**221**	**63.7**	**141.6**	**110**	**142.1**	**760**	**600~800**	**950**
V_T (V)	**-1.25**	**0.1**	**-**	**0.8**	**-1**	**-0.88**	**-1.3**	**0.35**	**-1.3**
μ (cm^2/Vs)	**0.13**	**0.5**	**0.1**	**0.25**	**0.32**	**0.67**	**0.18**	**0.04**	**0.71**
SS (V/decade)	**0.13**	**0.3**	**0.6**	**-**	**-**	**0.315**	**0.085**	**0.11**	**0.078**
μC_i (nF/Vs)	**58.5**	**110.5**	**6.37**	**35.4**	**35.2**	**95.21**	**136.8**	**24~32**	**674.5**
I_{on}/I_{off}	**1.2×10^4**	**3.5×10^5**	**1×10^4**	**-**	**$<1\times10^3$**	**1×10^4**	**1×10^5**	**1×10^4**	**1×10^5**

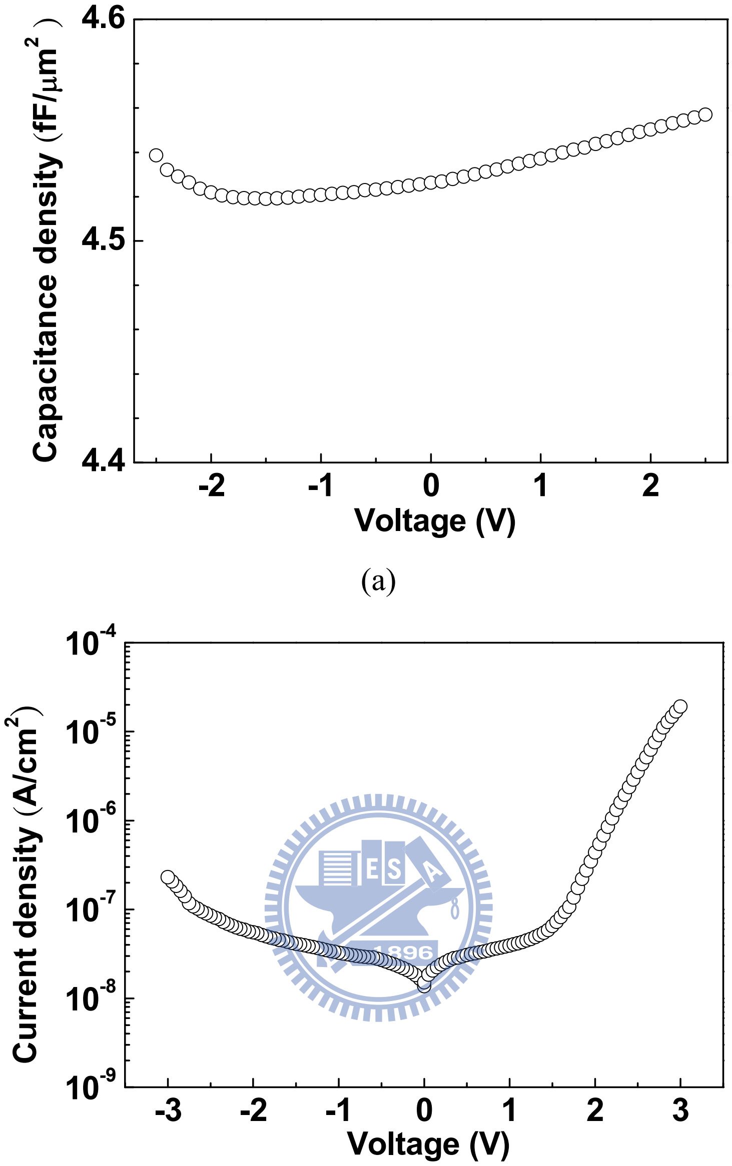


(a)



(b)

Fig. 3-1. A schematic diagram and image of the high-κ flexible HfLaO/pentacene OTFTs.



(a)

(b)

Fig. 3-2. (a) *C–V* and (b) *J–V* characteristics of Au/HfLaO/TaN capacitors.

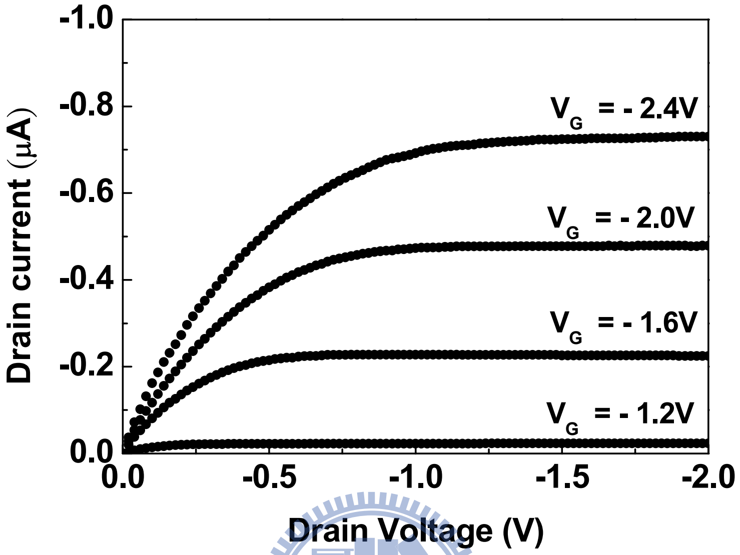


Fig. 3-3. I_D-V_D curve for an HfLaO gate dielectric OTFT.

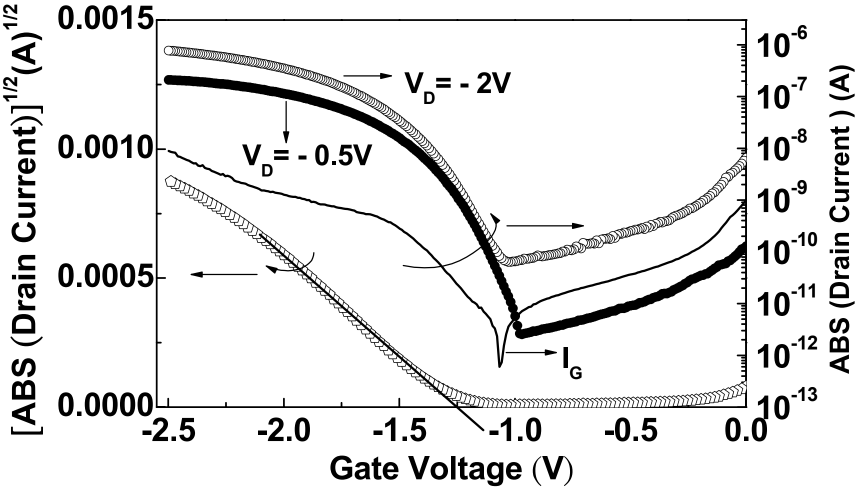


Fig. 3-4. I_D-V_G and -$I_D^{1/2}$-V_G of an HfLaO gate dielectric OTFT.

Chapter 4

A Flexible Organic Pentacene Nonvolatile Memory Base on High-κ Dielectric Layers

4.1 Introduction

Organic non-volatile memory devices have potential applications in flexible display drive logic, radio frequency identification tags and smart cards [4.1, 4.2]. These non-volatile memory devices supply an essential function for integrated circuits (ICs) based on organic thin-film transistors (OTFTs). The advantages of using organic memory devices, over their inorganic counterparts, are in their low cost, light weight, simple structure, mechanical flexibility, and low-temperature processing. The OTFT-based non-volatile organic memory devices display high drive current, low off-state leakage current and reasonably-fast switching speeds. The memory properties of these OTFT-based devices arise from the electric field modulation in the gate insulator, through the spontaneous polarization of ferro-electrics [4.2-4.4] or because of charge trapping [4.5, 4.6] in a chargeable layer. The charge-trapping type of OTFT memory device employs the well-known device physics of such structures and can build on the manufacturing experience of the Si industry. Digital data can be programmed into the device by injecting charges into the gate insulator, or erased by removing the stored charges. This charge transfer in the gate dielectric is readable by measuring the threshold voltage (V_T) of the transistor. This program or erase function can be obtained by having a large electric field across the gate insulator. Previous charge-trapping OTFTs have used a polymer as the insulator [4.5] or a floating gate [4.6] – necessitating a high gate voltage (V_G) to write the data. Such high voltages are incompatible with low-power IC designs and challenge existing battery technology. A solution to lowering the program and erase voltages is to use a high-κ dielectric. This has been done by incorporating a high-κ dielectric as the gate insulator in the OTFTs, leading to lower voltage operation [4.7-4.9].

Here we demonstrate a pentacene OTFT non-volatile memory, fabricated on a flexible polyimide (PI) substrate, which shows a program/erase voltage of 12 V, speed of 1 ms/100 ms, initial memory window of 2.4 V and a 0.78 V memory window after 48 hours. This has been achieved by using a high-κ dielectric as charge trapping-, blocking- and tunneling gate insulator layers. This yields to similar program/erase voltages as in charge trapping non-volatile memory devices in Si technology [4.10-4.14]. The magnitude of the V_T writing voltage can be decreased to 6 V by applying voltages of different polarity to the gate-electrode and the pentacene. We suggest that such an OTFT memory device could be useful in non-volatile data-storage and low-cost flexible electronics.

4.2 Experimental Details

The OTFT memory devices were fabricated on 125 μm thick PI substrates (Kapton HPP-ST, Dupont). Prior to device fabrication, the substrates were cleaned in de-ionized water and annealed in a vacuum (3×10^{-6} torr) at 200°C - to improve the dimension stability. A 100 nm SiO_2 thin film was deposited on the substrate by electron beam evaporation to create a layer with low internal stress. A 50 nm TaN gate electrode was then deposited by reactive sputtering, through a shadow mask. This was given a NH_3 plasma treatment to improve the metal-electrode/high-κ interface [4.9]. The 20 nm HfLaO, 20 nm HfON and 6 nm HfO_2 were then deposited by physical vapor deposition and given a 200°C, 30 minute furnace treatment in O_2, to improve the gate oxide quality. This was followed by deposition, through a shadow mask, of the pentacene active layer (Aldrich Chemical Co.), 70 nm in thickness. (The deposition conditions were: - a deposition rate of 0.5 Å/s, at a pressure of 3×10^{-6} torr, with the substrate being held at 70°C.) Finally, 50 nm of gold was deposited, at rate of 1 Å/s, for the source/drain electrodes. The channel width and channel length were 1500 and 150 μm, respectively. All electrical characteristics were made using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter at 1 kHz, in the dark and an air ambient.

4.3 Results and Discussion

A schematic diagram of the OTFT non-volatile memory is shown in Figure 4-1(a) and a corresponding image in Figure 4-1(b). The structure comprises a TaN gate electrode, HfLaO charge blocking dielectric, HfON charge trapping layer, HfO_2 charge tunneling dielectric, pentacene semiconductor layer and gold electrodes for the source-drain contacts. Output and transfer characteristics for such a device are displayed in Figures 4-2(a) and 4-2(b). From the transfer characteristics, the mobility, V_T, sub-threshold swing (*SS)* and on/off current ratio (I_{on}/I_{off}) were 0.1 $cm^2V^{-1}s^{-1}$, -1.4 V, 160 $mVdec^{-1}$ and 1×10^4 in the saturation region at a drain voltage (V_D) of -3 V. The low V_T and good *SS* are due to the use of a high-κ material as gate the dielectric [4.7-4.9].

The energy band diagram our OTFT memory device [4.15, 4.16] is shown in Figure 4-3. The HfLaO gate dielectric has a high dielectric constant, large bandgap and high electron injection barrier with respect to the TaN gate electrode during the erase process [4.9]. The small band-gap HfON, [4.10-4.12] with its deep trapping energy, was chosen as the charge-trapping layer to achieve good charge trapping characteristics. The thin HfO_2 dielectric serves as a charge-tunneling layer. The gold electrode forms an ohmic-like contact for the injection of holes. When a proper gate bias is applied, the charges in the pentacene active layer tunnel through the HfO_2 and are trapped in the HfON layer.

A Metal-Insulator-Semiconductor (MIS) structure is useful for charge injection studies [4.17]. Figure 4-4 shows the quasi-static capacitance-voltage (C-V) characteristics, as a function of V_G, for a TaN-HfLaO-HfON-HfO_2-pentacene-Au MIS structure. The maximum capacitance density was found to be 2.7 fFμm^{-2}. The decrease of the capacitance value at positive V_G , and increase for negative V_G , reflects the depletion and accumulation of holes stored in the MIS capacitor, respectively. No bipolar behavior [4.17] was observed in our OTFT devices. These results suggest that the pentacene is a p-type semiconductor and that no electron accumulation occurs at the dielectric/pentacene interface. It is important to notice the large C-V hysteresis, with the shifts being as large as 4 V. Since the area under the C-V curves reflects the trapped charges, the large hysteresis indicates good charge storage capacity, potentially useful for memory devices. The charges are mainly stored in the HfON layer of our device - this conclusion follows from the observation that, for a similar MIS structure without an HfON layer, no significant C-V hysteresis was found for the same biasing conditions.

In Figure 4-5 we show the shift of the transfer characteristics at $V_D = -1$ V, under a gate bias of -12 V at 1 ms for the program, and +12 V at 100 ms for the erase process . The drain current-gate voltage (I_D-V_G) curve shifted in a the negative direction when a V_G of -12 V was applied for 1 ms, and in the positive direction after application of a reverse V_g of 12 V for 100 ms. Thus the V_T value can be shifted, reversibly, by applying an appropriate gate bias. We investigated the program and erase characteristics further, and observed different V_T shifts as a function of V_G, for program or erase functions (Figure 4-6(a) and 4-6(b)). A 2.6 V V_T shift was shown after a -12 V program voltage pulse applied for 1 ms. The could be erased, with a large 2.5 V V_T shift, after a +12 V voltage pulse for 100 ms. Since a negative voltage was applied across the HfLaO/HfON/HfO_2 gate dielectric stack during the programming process, hole accumulation occurred at the dielectric/pentacene interface. The increase of the V_T shift with the increase in negative V_G indicates that the accumulated holes were injected over the HfO_2 gate dielectric and stored in the lower energy HfON dielectric. The erase was performed by applying a positive V_G to the TaN gate electrode, where the applied electric field over the HfLaO/HfON/HfO_2 gate dielectric stack causes hole depletion in the pentacene. The stored holes in the HfON may tunnel out, over the HfO_2 gate dielectric, into the pentacene; alternatively, the minority carriers (electrons), generated in the depletion region of the pentacene, can also tunnel through the HfO_2 and into the HfON – all of which gives rise to the erase function. Similar mechanisms have also been suggested by us to explain the program and erase functions in Si-based non-volatile memory [4.10-4.14]. The shift in capacitance-voltage characteristics for a TaN–HfLaO–HfON–HfO_2-pentacene-Au

MIS capacitor is shown in Figure 4-5 (b)

For non-volatile memory applications good retention characteristics are essential. To investigate the retention we applied a V_G of -12 V at 1 ms to program the device, and 12 V at 100 ms for the erase function. In Figures 4-7(a) and 4-7(b) we show the retention data. The V_T was extracted in the linear region of the I_D-V_G characteristics at V_D = -1V. The initial memory window was 2.4 V, which decreased to 0.78 V after 48 hours. The significant charge loss of 50% at 10^3 s is possibly related to the increase in the leakage current due to the surface roughness of the PI substrates, as well as defects in the low-temperature-formed HfO_2. Atomic force microscopy showed that the rms surface-roughness was approximately 5 nm. Improvements in the leakage current can be expected from smoother substrates and replacing the HfO_2 with a higher-quality gate dielectric. Finally in figure 8 we display the endurance characteristics of the memory device. A large memory window of 2.3 V, with a degradation of less than 5 %, was obtained after 10^2 cycles.

4.4 Summary

We have fabricated organic pentacene non-volatile OTFT memory devices on flexible PI substrates. These devices used a high-κ HfON dielectric as the charge trapping layer, HfLaO as blocking layers and HfO_2 as the tunneling layer. We found program/erase voltages of -12/12 V, at a speed of 1 ms/100 ms, along with an initial memory window of 2.4 V.

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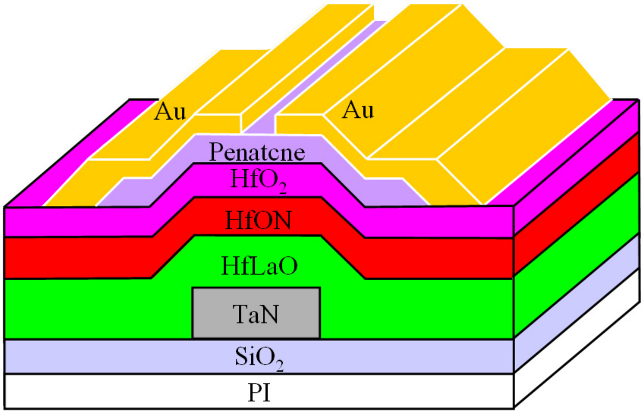

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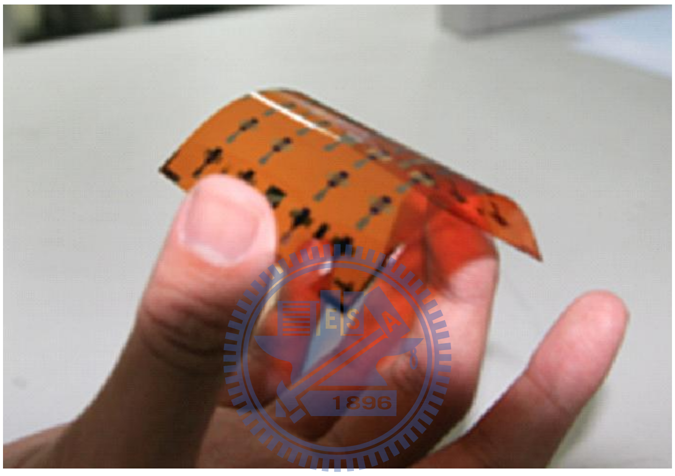

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Fig. 4-1. (a) Schematic cross-sectional diagram and (b) Image of the flexible pentacene OTFT memory devices.

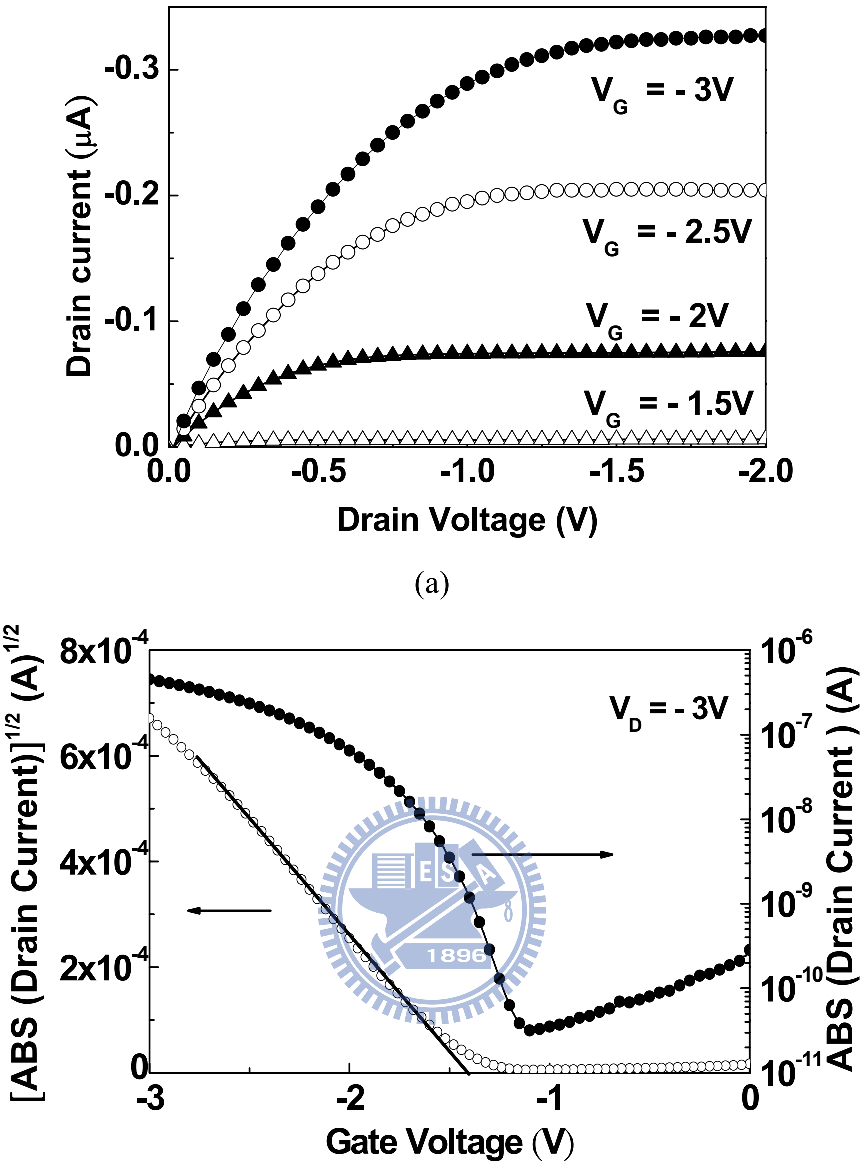

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Fig. 4-2. (a) Output and (b) transfer characteristics of pentacene OTFT memory devices.

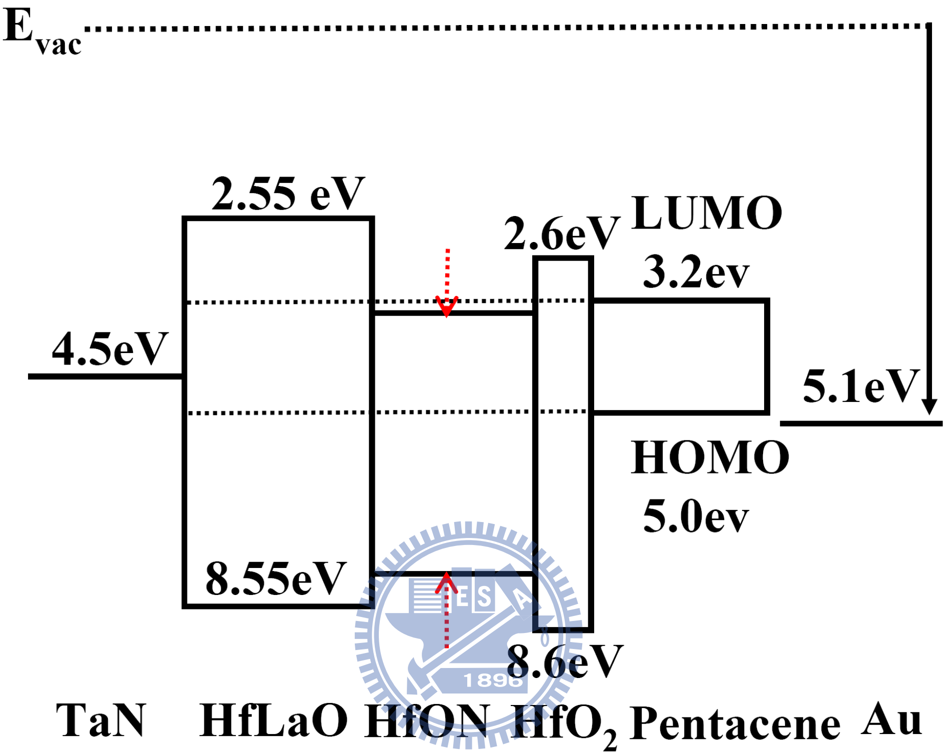


Fig. 4-3. Band diagram of the TaN-HfLaO-HfON-HfO_2-pentacene-Au OTFTs.

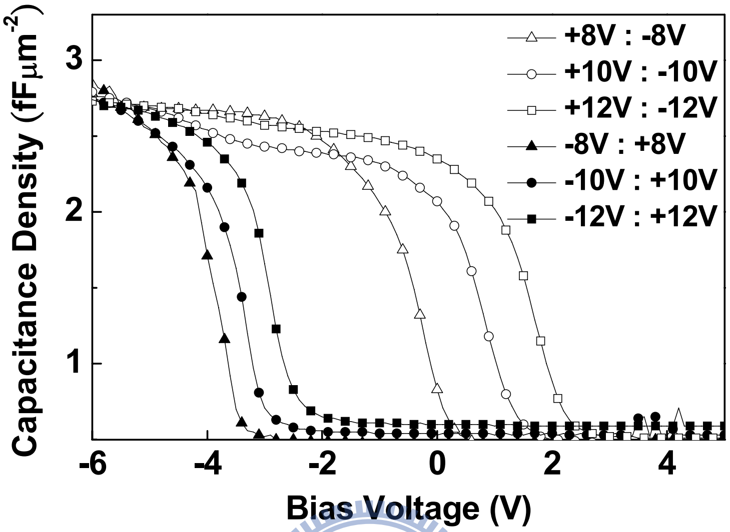
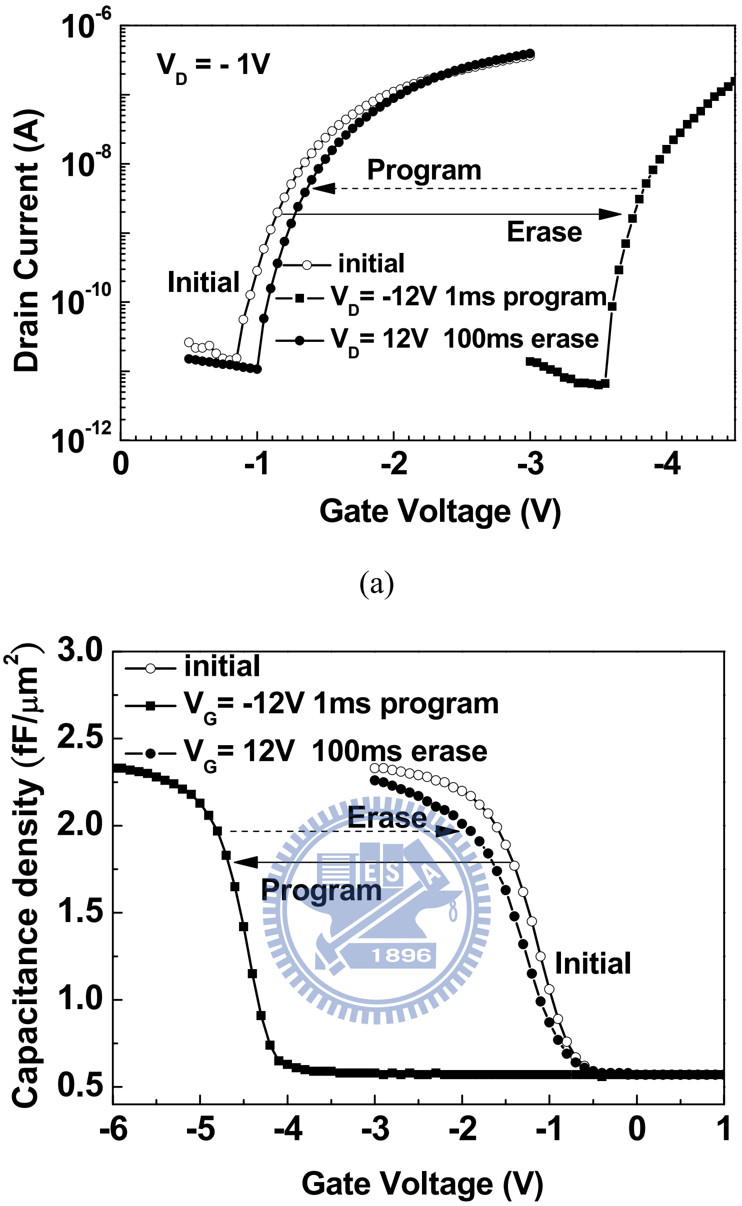


Fig. 4-4. Capacitance-voltage hysteresis for the MIS structure, showing 3-4V hysteresis. The curves are for different sets of program and erase voltages, as indicated.



(a)

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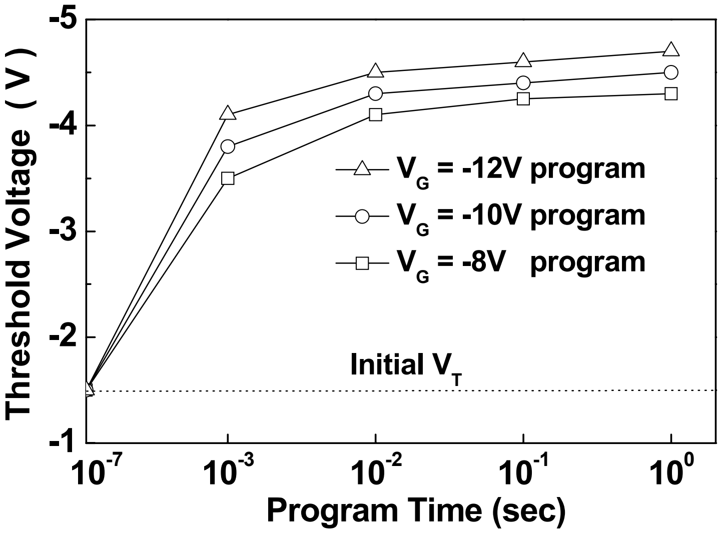
Fig. 4-5. (a) Drain current-Gate Voltage (I_D-V_G) hysteresis curves for a pentacene OTFT memory device under V_G = -12V, 1 ms program and V_G = -12V, 100 ms erase conditions. The I_D-V_G curves were measured at V_D = -1V. (b) Capacitance-voltage hysteresis curves for a TaN-HfLaO-HfON-HfO_2-Pentacene-Au metal-insulator-semiconductor.



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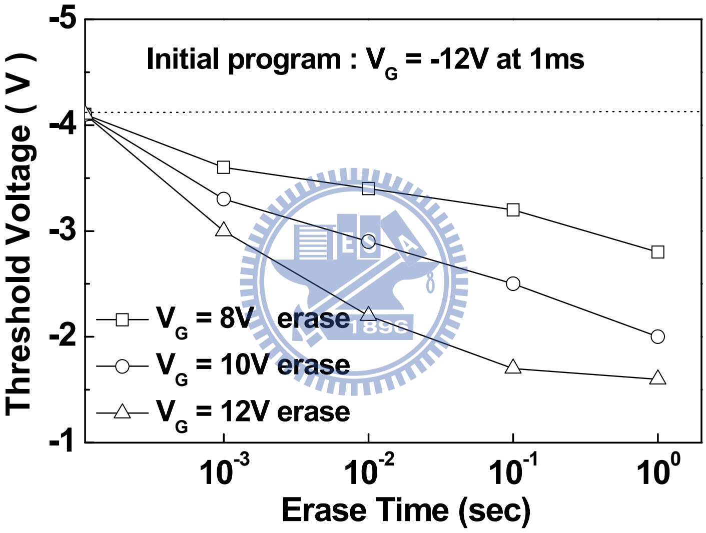
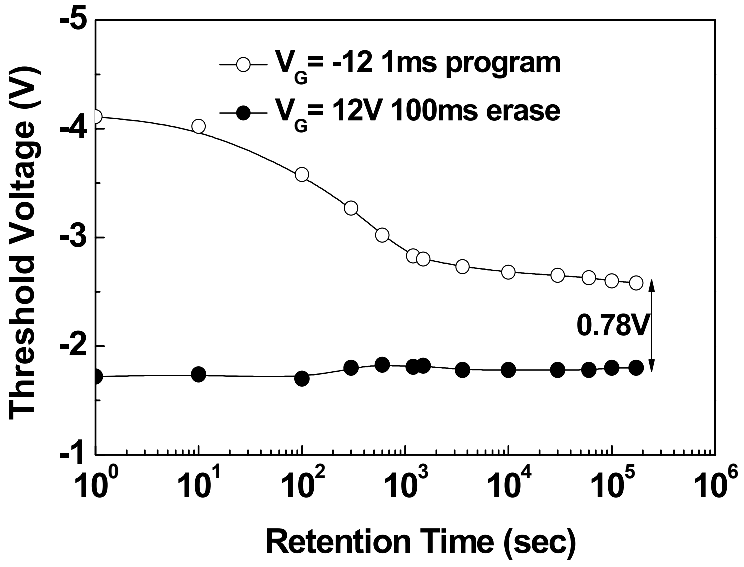


(b)

Fig. 4-6. (a) Program characteristics and (b) erase characteristics of OTFT memory devices for different voltages and times. The erase characteristics were initially programmed at V_g = -12V for 1ms. The V_{th} was extracted from the I_d-V_g curve at V_d = -1 V in the linear region.



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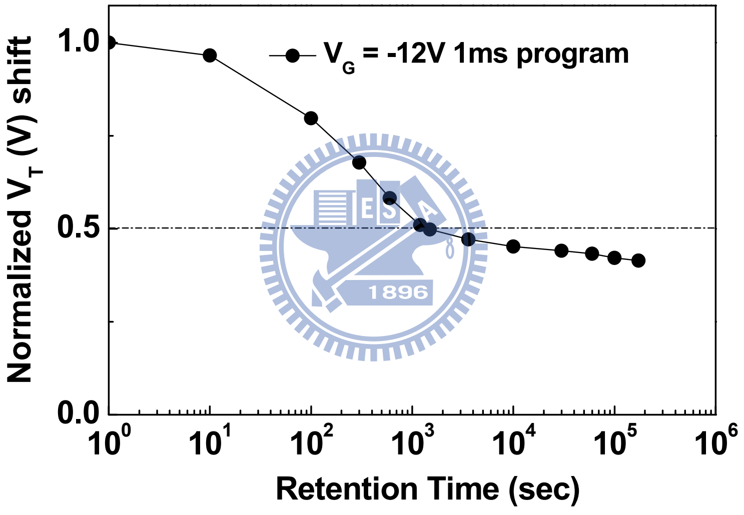


(b)

Fig. 4-7. (a) Retention characteristics in terms of the threshold voltage, *Vth*, for the memory device, for V_g = -12V 1ms program and V_g = 12V 100ms erase conditions. b) Normalized retention characteristics of the devices after V_g = -12V 1ms programming. The charge loss is approximately 50% after 10^3 s

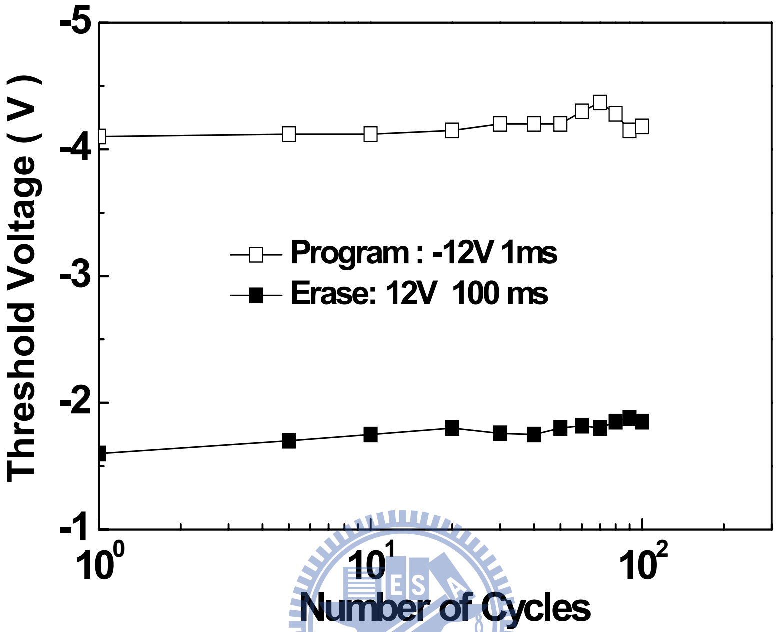


Fig. 4-8. Endurance characteristics of a pentacene OTFT memory device.

Chapter 5

Interfacial SiON Thickness Dependence on Device Performance of High-κ MoN/HfAlO/SiON *p*-MOSFETs

5.1 Introduction

Although the high-κ gate oxide and metal gate have been successfully implemented into 45 nm node CMOSFETs and below, the undesired high threshold voltage (V_T) is still a difficult challenge [5.1]-[5.14]. This challenge is even worse at small equivalent-oxide thickness (EOT) by the flat-band voltage (V_{fb}) roll-off effect [5.4]-[5.6]. The unwanted high V_t issue is particularly harder for *p*-MOSFET than *n*-MOSFET due to very limited elements of metal-gate in the Periodic Table that have the needed high effective work-function ($\phi_{m\text{-}eff}$) >5.2 eV [5.1]. One effective method to reduce the V_T is to use the unique negative or positive V_{fb} property of high-κ La_2O_3 [5.8]-[5.10] or Al_2O_3 [5.11]-[5.14] to mix or cape with the Hafnium (Hf) based high-κ dielectric for *n*- or *p*-MOSFET, respectively. Besides, it was reported that Fluorine ion (F^+) implantation into Si can also increase the V_{fb} [5.15]-[5.19] but did not degrade on hole mobility [5.18]-[5.19]. The F^+ implantation may be potentially useful for metal-gate/high-κ *p*-MOSFET.

In this chapter we have investigated the devices performance and mechanisms of HfAlO capping on different thickness SiON. The F^+ implantation is also performed to study the V_{fb} shift on MoN/HfAlO/SiON *p*-MOS capacitors. Under the optimized condition, small EOT, low V_T, good sub-threshold swing (*SS*) and high mobility are simultaneously reached in the gate-first MoN/HfAlO/SiON *p*-MOSFETs.

5.2 Experimental Details

The gate-first MoN/HfAlO/SiON *p*-MOSFET was fabricated on 12-in N-type Si wafer. After standard cleaning, different 0.83, 1.5 or 2.1 nm thick SiON (8% N) was grown by using *in-situ* steam-generated (ISSG) oxide. Next, a 1 nm HfAlO [5.1] dielectric was deposited by physical vapor deposition (PVD), followed by a 500°C O_2 post-deposition anneal. The composition ratio of Hf and Al in HfAlO is 1:1. Then 50-nm MoN and 200-nm TaN were deposited *ex-situ* by PVD. The nitrogen content in TaN and MoN is 50%. After gate definition, self-aligned BF_2^+ was implanted at 35 KeV and 5×10^{15} cm^{-2} for p^+ source-drain regions and activated at 1000°C by rapid thermal annealing (RTA) for 1 sec. For comparison, MoN/SiON *p*-MOSFETs were also formed. We also studied the effect of F^+ implantation on *p*-MOS devices, performed before gate oxide stack at 10 KeV and $1x10^{14}$ cm^{-2} dosage. The formed gate stack was examined by X-ray Photoelectron Spectroscopy (XPS) and Secondary Ion Mass Spectroscopy (SIMS) analysis. The XPS spectra was excited by Al K_α

radiation and detected at a take-off angle of 60^{o}. The fabricated devices were characterized by capacitance-voltage (C-V) and gate current density-voltage (J-V) measurements using the HP4284A precision LCR meter and HP4156C semiconductor parameter analyzer, respectively. The V_{fb} and EOT values were extracted from measured C-V curves using a CVC simulator [5.20] that accounts for the quantum-mechanical effects. The mobility of MOSFET was extracted directly from the measured I_d-V_g characteristics.

5.3 Results and Discussion

A. *Positive* V_{fb} *shift of MoN/HfAlO/SiON gate capacitors*

Figures 5-1(a) and 5-1(b) show the C-V and J-V characteristics of MoN/HfAlO/SiON gate capacitors with various SiON thicknesses and control MoN/2.1nm SiON. The C-V measurements were performed at a frequency of 100 kHz. The positive V_{fb} value of as-deposited MoN/HfAlO/SiON capacitor is nearly identical to the control MoN/2.1nm SiON device, which is consistent with the previous report [5.21]. In sharp contrast, large positive V_{fb} shift of more than 500 mV and a higher capacitance density were obtained for MoN/HfAlO/1.5-nm-SiON devices after 1000^{o}C RTA. The $\phi_{m\text{-}eff}$ of 5.1 eV and oxide charge density of 4.5x10^{12} cm^{-2} were obtained from the V_{fb}–EOT plot in Figure 5-2. Similar large V_{fb} values were obtained for MoN/HfAlO/SiON p-MOS capacitors with different 2.1 and 0.83 nm thick SiON after 1000°C RTA. The capacitor with the thinnest 0.83 nm SiON shows the largest V_{fb} that may be due to Al diffusion through SiON and react with Si channel layer. The EOT is improved with decreasing SiON thickness from 2.1 to 1.5 nm, but degrades at the thinnest 0.83 nm. The leakage current is higher at thinner EOT, where the MoN/HfAlO/1.5-nm-SiON *p*-MOS capacitor has the highest leakage current of 5×10^{-3} A/cm^2 at 1 V. The achieved large V_{fb} and low gate leakage current were due to the using high-work function MoN gate and HfAlO. In addition, the high temperature RTA is also crucial to reach further positive V_{fb} shift of HfAlO/SiON gate dielectric. At optimized 1.5 nm interfacial SiON, a small EOT of 0.85 nm was obtained using quantum-mechanical *C-V* calculation.

B. *The mechanism*

To investigate the needed positive V_{fb} shift after 1000°C RTA, we have performed the XPS measurements on HfAlO/SiON gate dielectric. Figure 5-3 exhibits the Si 2*p* photoemission spectra of MoN/HfAlO/SiON gate stack, where the top MoN was etched back for XPS measurements by using reactive ion etching (RIE) with BCl_3/Cl_2 plasma. The XPS spectrum of MoN/SiON was also added for comparison. There are two major peaks in the XPS data after Gaussian function de-convolution. The peak at 99.3 eV binding energy is assigned to Si-Si bonds. The peak at 102~104 eV corresponds to Si-O bonds of silicate or SiO_x from control MoN/SiON sample [5.22].

The Si-O bonding energy of as-deposited MoN/HfAlO/SiON is 102.6 eV that lowers to 102.1 eV after 1000°C RTA. This 102.1 eV value is very close to the reported data [5.23]-[5.24] that is attributed to AlSiO silicate formation. This is originated from the Al_2O_3 reacting with Si substrate [5.23] or Si_3N_4 dielectric [5.24]. During the silicate formation with a lower 0.5 eV Si-O binding energy, the charged oxygen vacancies in Al_2O_3 may also be formed after 1000°C RTA:

$$Al_2O_3 + SiO_{1.92}N_{0.08} \rightarrow Al_2O_{3-x} + SiO_{1.92+x}N_{0.08} \tag{1}$$

The formation is thermo-dynamically favorable due to the lower bond enthalpy of Al_2O_3 (511 kJ/mol) and SiN (470 kJ/mol) in SiON than that of SiO_2 (800 kJ/mol) [5.1]. Similar formation of charged oxygen vacancies was also reported in HfLaO/Si MOS capacitor after high temperature RTA [5.6] and responsible to the V_{fb} roll-off at smaller EOT [5.5]-[5.6], [5.25]. This charged oxygen vacancies can lead to the unique positive V_{fb} of Al_2O_3 from theoretical calculation [5.26], which explains well the measured >0.5 V positive V_{fb} shift of HfAlO/SiON gate stack after 1000°C RTA.

We have used the F^+ implantation to further study the effect of V_{fb} shift. Figure 5-4 shows the *C-V* characteristics of MoN/HfAlO/SiON *p*-MOS gate capacitors with F^+ implantation. The control MoN/2.1-nm-SiON device shows a slightly higher V_{fb} with F^+ implantation, but the V_{fb} shift and EOT of the same MoN/HfAlO/1.5-nm-SiON device are deteriorated with F^+ implantation compared these without (Fig. 5-1(a)).

The SIMS depth profiles were measured to study the degradation in MoN/HfAlO/SiON device. Figures 5-5(a) and 5-5(b) show the SIMS profiles for MoN/HfAlO/1.5-nm-SiON gate stack without and with F^+ implantation, respectively. After 1000°C RTA, the Al and Mo are diffused closer to SiON/Si that explains the achieved higher capacitance density or smaller EOT than as-deposited case. The poor EOT for MoN/HfAlO/0.83-nm-SiON device may also be related to the diffusion of Al_2O_3 through the very thin SiON and reaction with bottom Si. In F^+-implanted sample, the F-atoms were diffused strongly and accumulated into high-κ gate dielectric after 1000°C RTA. This phenomenon is related to the F-atoms bonding with the charged oxygen vacancies in high-κ gate dielectric because of the largest electro-negativity, but no such bonding can be formed in defect-free single crystal Si substrate. This bonding further blocks the V_{fb} shift by decreasing oxygen vacancies in Al_2O_3. This mechanism can also explain the degraded EOT with F^+ implantation, since the formed SiOF [5.16] in gate stack is a well known low κ dielectric ($\kappa<3.9$) for backend isolation. The above results strongly suggest the positive V_{fb} shift of MoN/HfAlO/SiON gate capacitor after 1000°C RTA is related to the oxygen vacancy that is also consistent with the theoretically calculation [5.26].

C. *Transistor Characteristics*

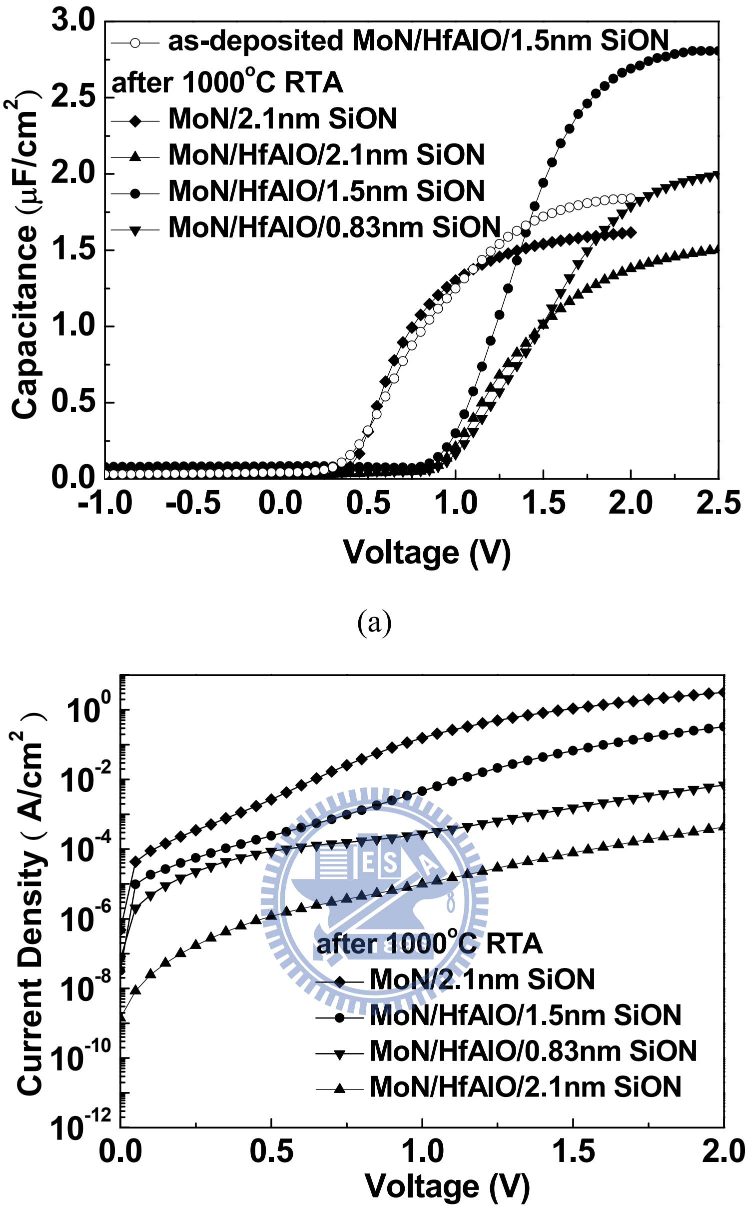
Figure 5-6 shows the transistor I_D-V_G characteristics of MoN/HfAlO/SiON *p*-MOSFETs. Low V_t values of -0.01, -0.10 and -0.08 V are obtained from the linear I_D-V_G plot of transistors with SiON thickness of 0.83, 1.5 and 2.1 nm, respectively. These low V_T values are due to the large V_{fb} values in *C-V* characteristics shown in Fig. 1(a). The metal-gate/high-κ *p*-MOSFET with the thinnest 0.83-nm SiON interfacial layer also shows the poorest *SS* of 90 mV/dec, while *SS* of 68 mV/dec are obtained for transistors with 1.5-nm and 2.1-nm interfacial SiON.

Figure 5-7 shows the mobility as a function of effective electric field of MoN/HfAlO/SiON *p*-MOSFETs with different SiON thickness. Peak hole mobility of 91, 80 and 60 cm^2/Vs are obtained for MoN/HfAlO/SiON *p*-MOSFETs with SiON thickness of 2.1, 1.5 and 0.83 nm, respectively. The thinnest 0.83-nm SiON shows the lowest hole mobility that is attributed to the increased remote Coulomb scattering of Al_2O_3 [5.27] or interaction of diffused Al_2O_3 with Si channel. This result further suggests that the optimized thickness of interfacial SiON is important to obtain not only small EOT but also good hole mobility.

5.4 Summary

The V_T shift of MoN/HfAlO/SiON *p*-MOSFETs have been studied. Under the optimized 1.5 nm SiON, excellent device integrity of small 0.85 nm EOT, low -0.10 V V_T, good 68 mV/dec *SS* and high 80 cm^2/Vs mobility are obtained in the

MoN/HfAlO/SiON *p*-MOSFETs. The large positive V_{fb} shift after 1000°C RTA is explained due to the forming charged oxygen vacancies in AlSiO silicate, which is originated from diffusion and interaction of Al_2O_3 and SiON by XPS and SIMS analysis. The mechanism is further supported by the poorer V_{fb} shift with F^+ implantation, where the oxygen vacancies can be lowered by bonding with F-atoms. Our gate-first metal-gate/high-κ *p*-MOSFET has extra merit of full process compatibility with current VLSI line.



(a)

(b)

Fig. 5-1. (a) *C-V* and (b) *J-V* characteristics of the MoN/HfAlO/SiON and control MoN/SiON MOS capacitors before or after 1000°C RTA. The device area is 100μm×100μm.

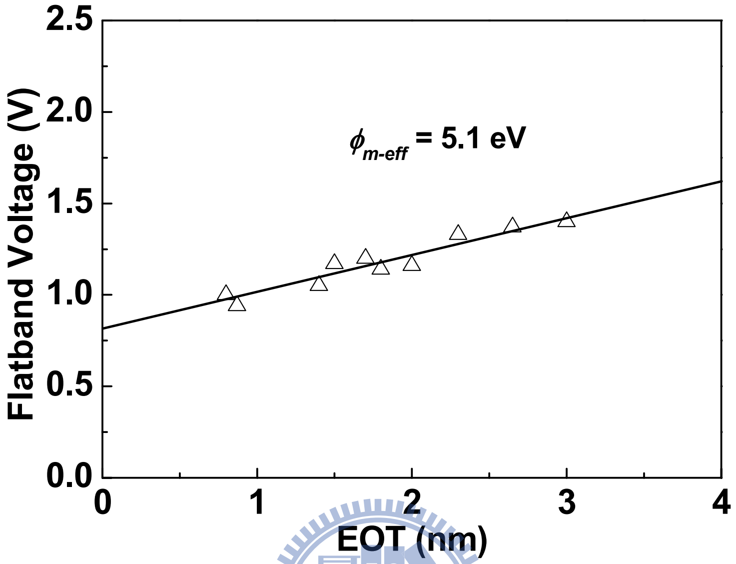


Fig. 5-2. V_{fb}-EOT plot with different HfAlO thickness on constant 1.5 nm SiON.

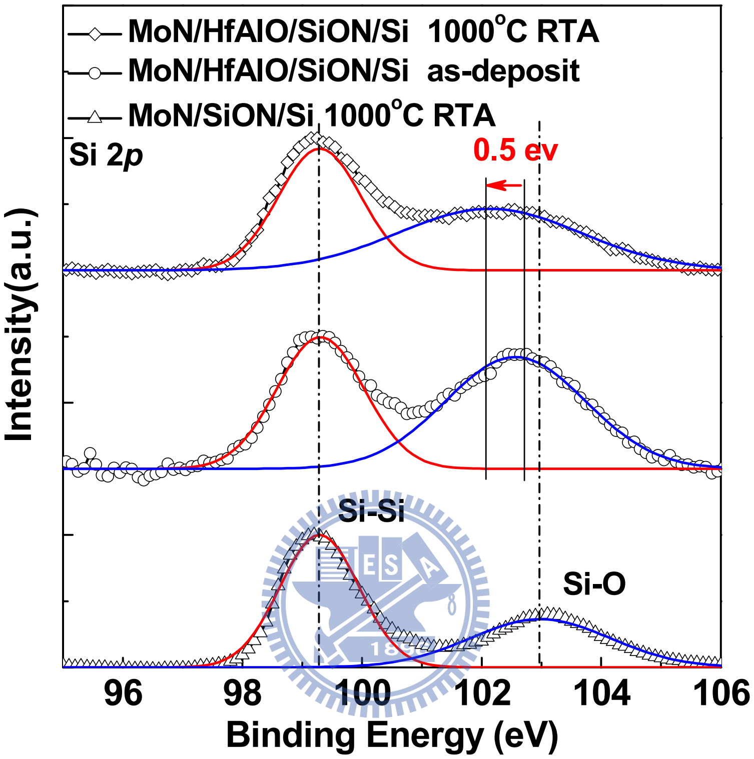


Fig. 5-3. Si 2*p* XPS spectra of MoN/HfAlO/SiON/Si and control MoN/SiON/Si gate stacks with MoN layer etched back. Lowered peak energy was found after 1000°C RTA

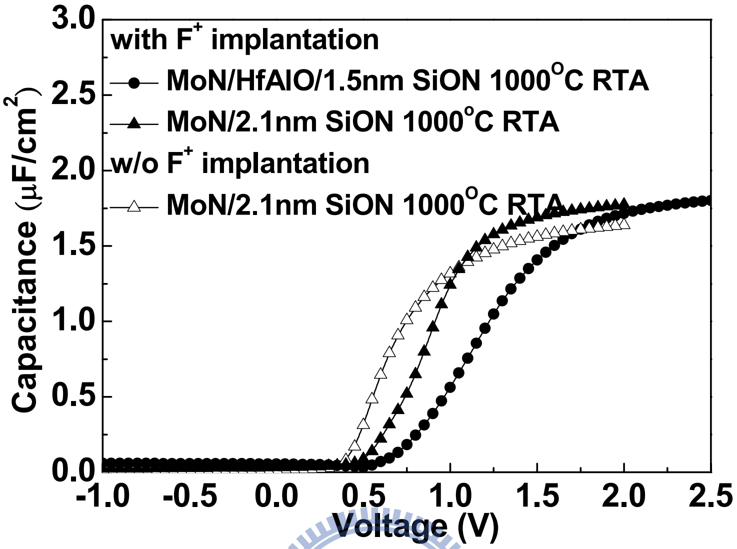
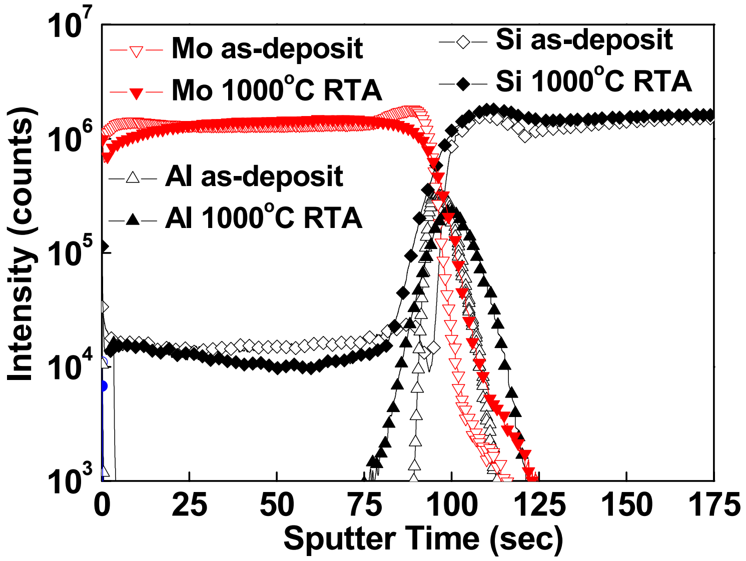


Fig. 5-4. *C-V* characteristics of MoN/HfAlO/SiON and control MoN/SiON MOS capacitors with F$^+$ implantation.



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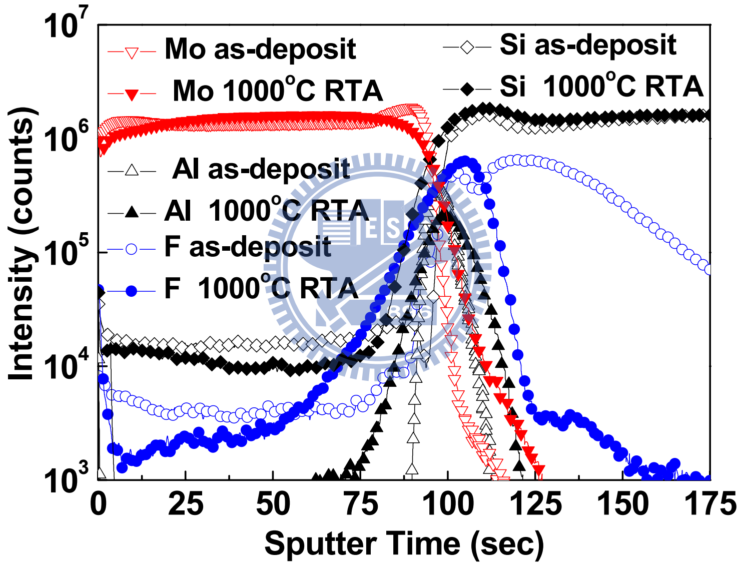

(b)

Fig. 5-5. SIMS profiles of MoN/HfAlO/SiON gate stack (a) without and (b) with F^+ implantation. The SiON thickness is 1.5 nm.

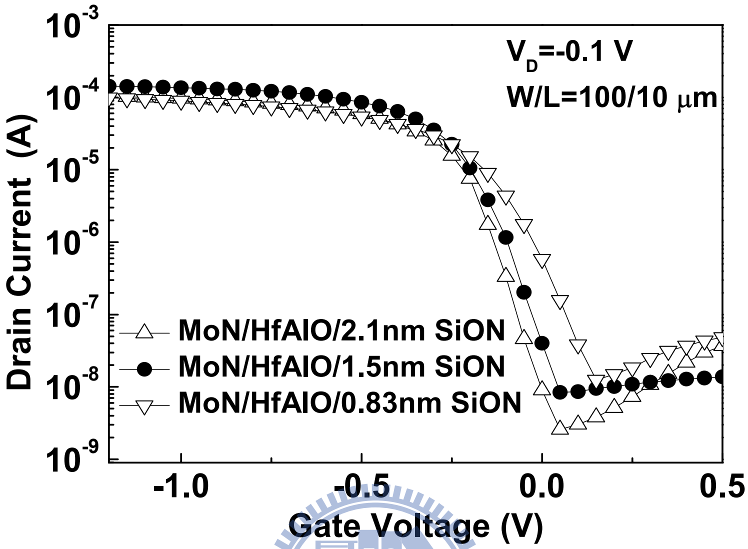

Fig. 5-6. I_D-V_G characteristics of MoN/HfAlO/SiON *p*-MOSFETs.

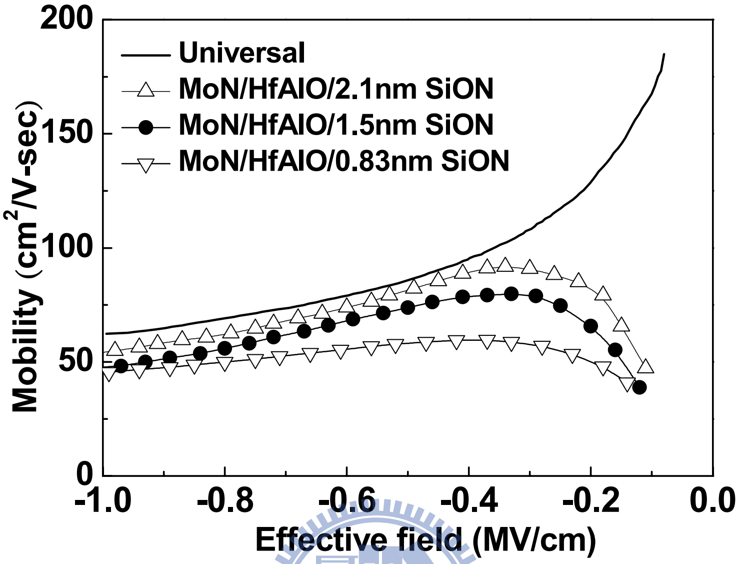

Fig. 5-7. Hole mobility versus effective electric field of MoN/HfAlO/SiON and MoN/SiON *p*-MOSFETs

Chapter 6

Conclusion

The high transistor current of OTFTs is the important factor to drive high operation current organic light emitting diode and high resolution display. The high drive current can be achieved by increasing the channel mobility of OTFTs, ratio of *W/L* or gate-capacitance density by the use of high-κ dielectric. In this dissertation, we first integrate a high-κ HfLaO dielectric into pentacene-based OTFTs on SiO_2/Si substrate. This device shows good device performance, such as a low *SS* of 0.078 V/dec, a V_T of −1.3 V, and a μ of 0.71 cm^2/Vs. The good performance is due to the high gate-capacitance density that is given by the HfLaO dielectric, which is achieved at an EOT of only 3.6 nm with a low leakage current.

For flexible electronics and system-on-panel application, the low temperature process and the nonvolatile memory function are required. We further decrease the process temperature to 200^{o}C and demonstrate HfLaO/pentacene OTFT fabricated on low-cost flexible polyimide substrates. The flexible pentacene OTFT exhibits a low *SS* of 0.13 V/decade and a V_T of −1.25 V. The μ is 0.13 cm^2/V·s at an operating voltage as low as only 2.5 V. These characteristics are attractive for flexible electronics applications. Based on the good OTFT device performance, we have developed a pentacene thin film transistor nonvolatile memory fabricated on a flexible polyimide substrate. This device shows a low program/erase voltage of 12 V, a speed of 1/100 ms, an initial memory window of 2.4 V, and a 0.78 V memory window after 48 h. This has been achieved by using a high-κ dielectric as charge trapping, blocking, and tunneling gate insulator layers.

Moreover, we study the dependence of interfacial SiON thickness on device performance of high-κ MoN/HfAlO/SiON *p*-MOSFETs. Under the optimized SiON thickness, low V_T of -0.1 V is achieved at EOT of only 0.85 nm after standard 1000°C RTA. From the SIMS and XPS analysis, the small EOT and low V_T are attributed to the diffusion of Al_2O_3 and MoN into SiON and the formation of silicate and oxygen vacancies.

References

Chapter 1 Introduction

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