CHAPTER 3

Theory and Design of Active Balanced Switching Mixer

3.1 Active drain-drive mixer

In this chapter a HJFET nonlinear model (Figure 3.1) is used for the nonlinear analysis of mixer. Here the drain port acts as a gate controlled current source. The DC condition of HJFET could be obtained by setting Vgs fixed and sweeping Vds, therefore a characteristic curve of current versus voltage (I-V curve) could be calculated and measured in this way. The measured I-V curve of NEC HJFET device (Figure 3.2) shows that when setting the bias voltage fixed at the gate of FET, the FET device would acted as a Vds controlled amplifier, as shown in Figure 3.3.

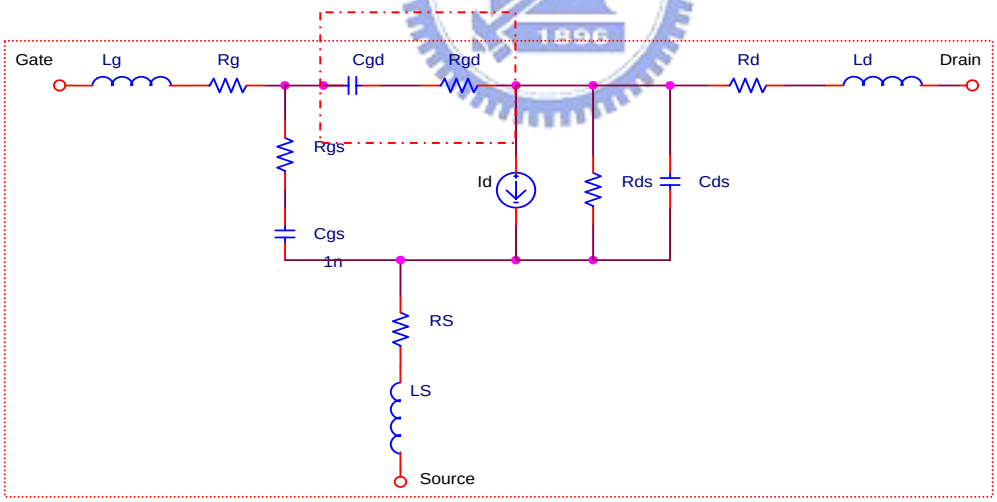


Figure 3.1 NEC HJFET nonlinear model.

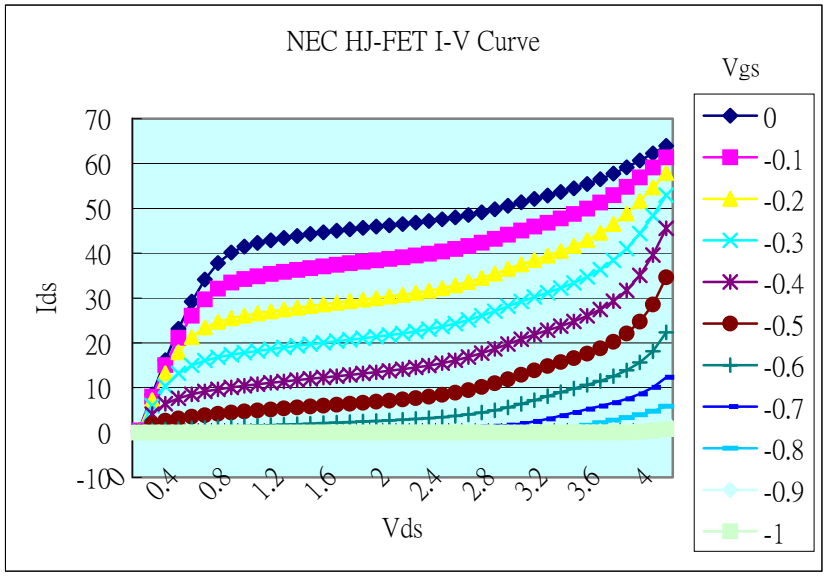


Figure 3.2 NEC HJ-FET I-V Curve measured result

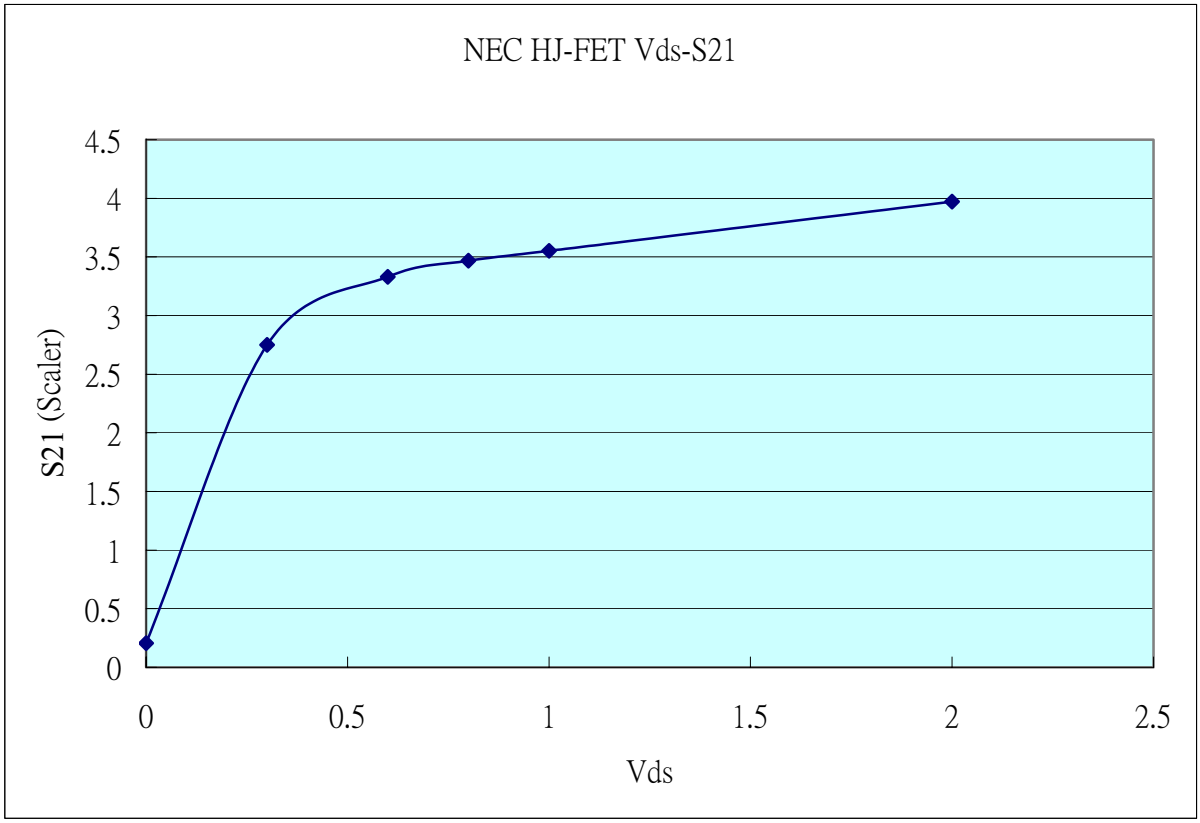


Figure 3.3 NEC HJ-FET Vds-S21 Curve at fixed Vgs

We refer to [12] to provide a typical example of active drain-driven mixer (Figure 3.4) operating at X-band. The local and RF frequency of the mixer are 10GHz and 11GHz respectively, then generating the IF frequency at 1GHz as a result. In Figure 3.4, this circuit was implemented on a plastic substrate using microstrip technology and the mixer device should be biased with Vgs =-0.3V, Vds =0.7V for the purpose to attain maximum conversion gain, thus the local oscillator power could be 10.5dBm. To obtain optimum conversion gain, the input network must provide conjugate matching at RF and a short circuit at IF [12]; also the output network must conjugate match the device at IF and provide a short circuit at LO frequencies (f0, 2f0) while providing filtering and LO-to-IF isolation. The influence on conversion gain of the network impedance at image frequency has been proved negligible and, in accordance, a short circuit was assumed.

The IF short circuit at the input is implemented by using, as gate biasing circuit, a quarter-wavelength stub at RF frequency. The image frequency rejection is achieved by means of an open stub with a quarter wavelength at this frequency. The simulation of this network, assuming Zin to be constant, is presented in Figure 3.5 and compared with the measured input reflection coefficient of the mixer [12].

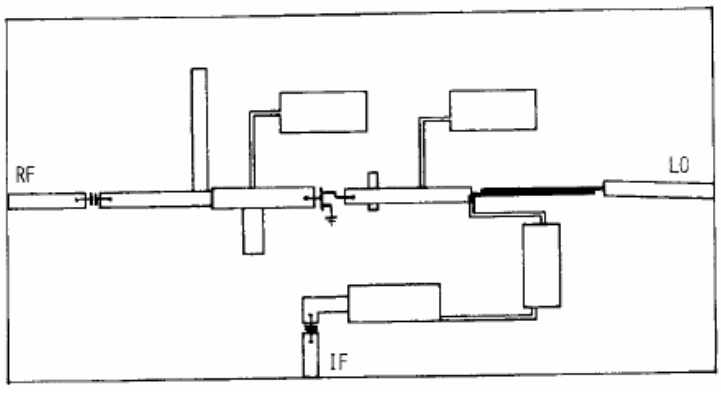


Figure 3.4 Active Drain Mixer, Microstrip Prototype

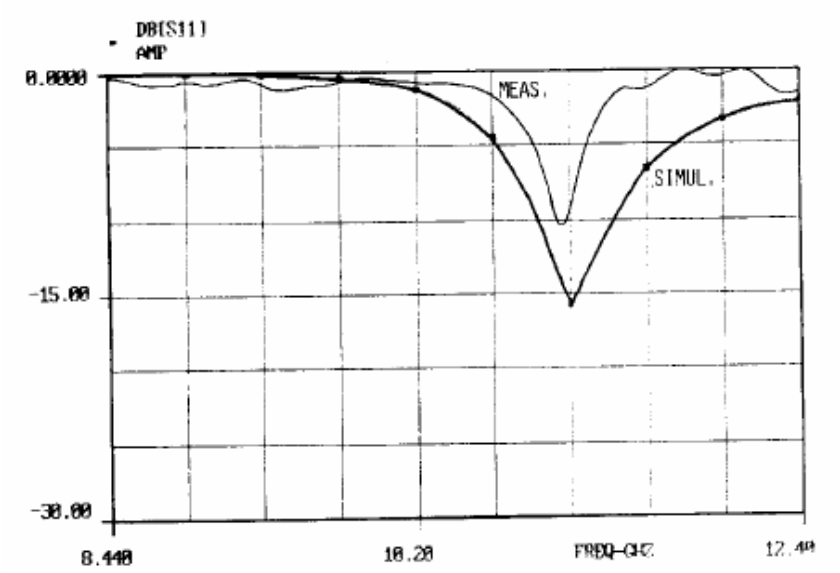


Figure 3.5 Active Drain Mixer; measured and simulated RF input reflection coefficients versus frequency

The main feature an active drain mixers possessed [12][5] lies in its capability to attain low noise figure with a moderate conversion gain, however the poor impedance matching at input port would become an issue in design consideration.

For analyzing mixer the local signal could be categorized as a large signal model if the local power is large enough to turn the FET “on” on the positive cycle then turn the FET “off” on the negative cycle. The LO signal drives FET to change its state between “on” and “off” states, then causes a impedance change at the Zin because of the components Cgd and Rgd [6] are connected to FET output and input port. Therefore Zin will be changed in the states of ”on” and “off” by FET, hence lead to an issue of poor return loss at the RF input port.

For active mixers the FET acts like an amplifier at the “on” state as the conversion gain A is determined by the amplitude of LO signal, while in “off” state the mixer acts like a high-impedance resistance, so the mixer input impedance Zin is different in “on” and “off” states.

To analyze the active drain mixer, we can divide the circuit into several equivalent parts such as amplifier block Amp, input impedance block Zi, output impedance block Zo and feedback impedance block Zf as shown in Figure 3.4. Base on the Miller Theorem, we can reduce the impedance Zf to Zif and Zof as shown in Figure 3.7. The value of Zif and Zof could be expressed in accordance to Zf and A, as shown in eqn (1) and eqn (2).

$$\text{Zif} = \frac{Zf}{(1 - A(V_{LO}))} \qquad \cdots\cdots\cdots\cdots\cdots\cdots \quad \text{eqn (1)}$$

$$\text{Zof} = \frac{Zf}{(1 - \frac{1}{A(V_{LO})})} \qquad \cdots\cdots\cdots\cdots\cdots\cdots \quad \text{eqn (2)}$$

In the “on” state, the mixer acts like an amplifier as the conversion gain with a amplitude of A1, which is determined by the amplitude of LO signal. Based on eqn (1), the mixer input impedanc**e Zi1** is equivalent to Zi ***//*** (Zf /(1-A1)). In the “off” state, the mixer acts like an high-impedance resistance with a amplitude of A2, so the input impedance **Zi2** is equivalent to Zi ***//*** Zf/((1-A2)). Because that the “on” state amplitude A1 is much larger than “off” state amplitude A2, the input impedance Zi1 of ”on” state would be much smaller than “off” state impedance Zi2. The change of LO input impedance could affect the RF input impedance at large signal input to drain port.

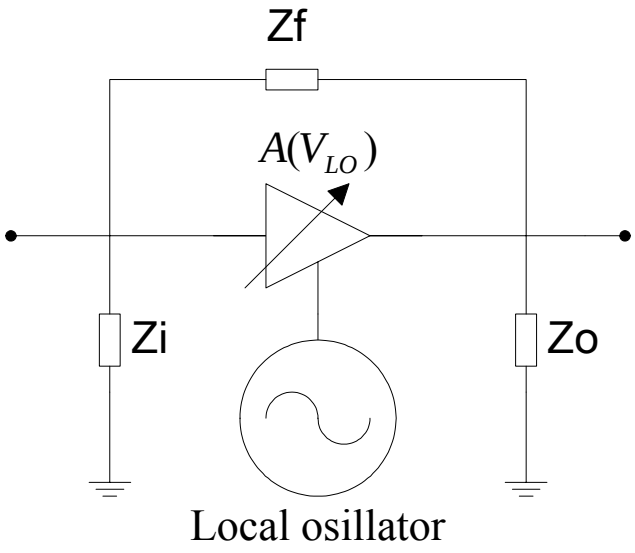


Figure 3.6 Simplest the equivalent circuit of the transistor to component Zi, Zo, Zf, and Amp

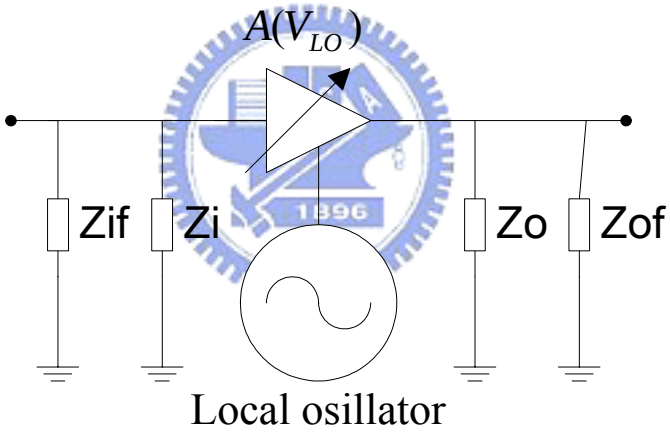


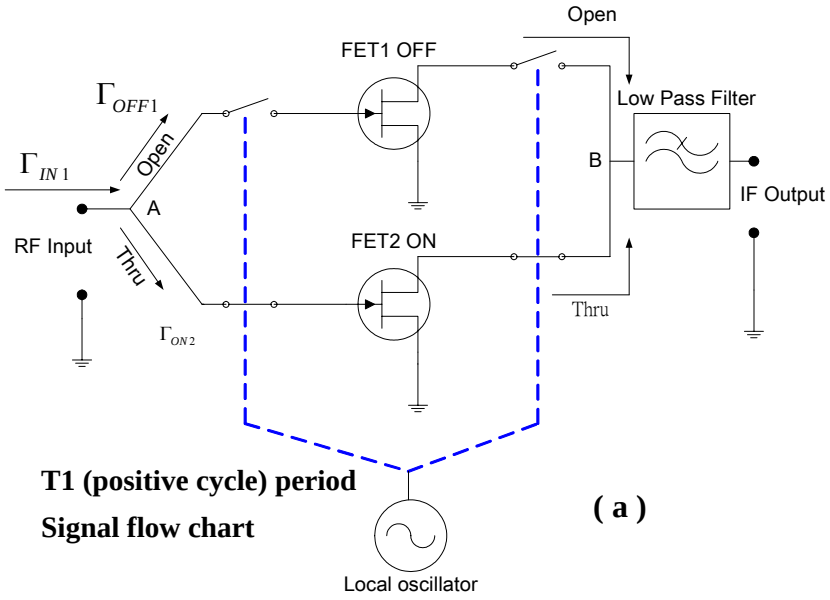
Figure 3.7 Reduce the impedance between gate and drain to Zif and Zof

3.2 Concept of Active Balanced Switching Mixer

The most important issue of active drain mixer is that its input return loss was not very good, hence we should suggest using a balance structure to improve the impedance mismatch. In publish papers the common methods to improve input return loss are as follow:

1. Add the hybrid before FET gate port to reduce the RF port reflection coefficient [7], but this method will increase the noise figure and conversion loss by more than 3dB.
2. Add the component "isolator" before RF port, but that component is very expensive.
3. Used the switching mixer, as shown in the figure 2.11, but the performance of conversion gain and noise figure would be only decent, but not good.

We combined the switching mixer and drain mixer to form a new design that provides a better performance than the methods described above. We called this structure "Active balanced switching mixer". The design concept and block diagram of the mixer is as shown in the figure 3.8.



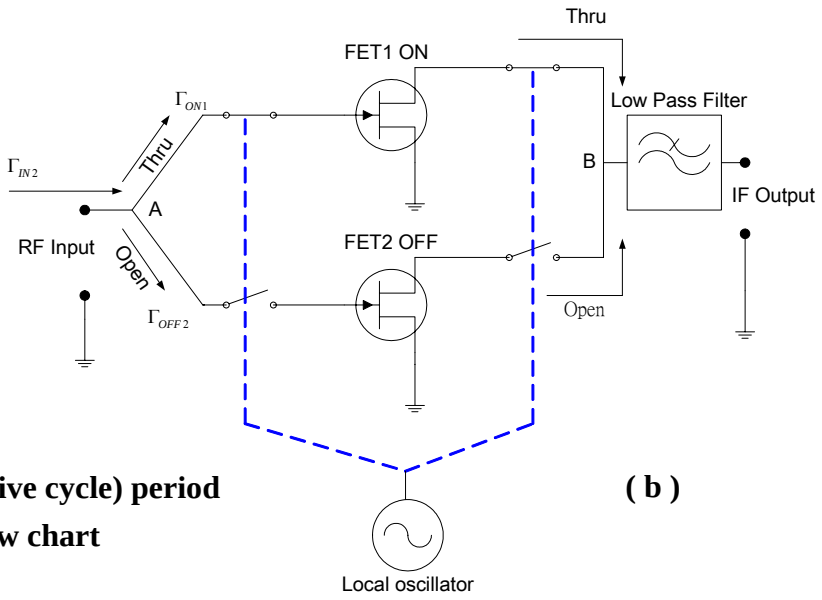


Figure 3.8 Concept of non-hybrid active balance switching mixer
(a) Positive cycle signal flow (b) Negative cycle signal flow

At T1 period, the LO signal will drive FET2 to turn on and FET1 to turn off, thus the RF signal will pass through FET2. At node A, the reflection coefficient Γ_{IN1} will be determined by two coefficients Γ_{ON2} and Γ_{OFF1} in parallel path. If the impedance of $Z_{OFF1} >> Z_{ON2}$, then the RF signal will flow through FET2, thus $\Gamma_{IN1} \approx \Gamma_{ON2}$. At T2 period, the LO signal will control the RF signal input to FET1, and FET2 will be turn off. At node A, the reflection coefficient Γ_{IN2} will be determined by two coefficients Γ_{ON1} and Γ_{OFF2} in parallel path. If the impedance of $Z_{OFF2} >> Z_{ON1}$, then the RF signal will flow through FET1, thus $\Gamma_{IN1} \approx \Gamma_{ON2}$. In designing input matching circuit of the mixer, if we can make Γ_{IN1} similar to Γ_{IN2}, then we can get a constant value of Γ_{IN}, therefore reduce the difficulty of input impedance matching.

As stated before that when the FET gate bias was fixed, the device can be driven at drain port in the positive period, and been a high-impedance in the negative period. We add the LO

frequency 180° balun to each FET drain port to control FET “On” and “off” states.

3.3 Microwave FET small signal S-parameter measurement and TRL calibration

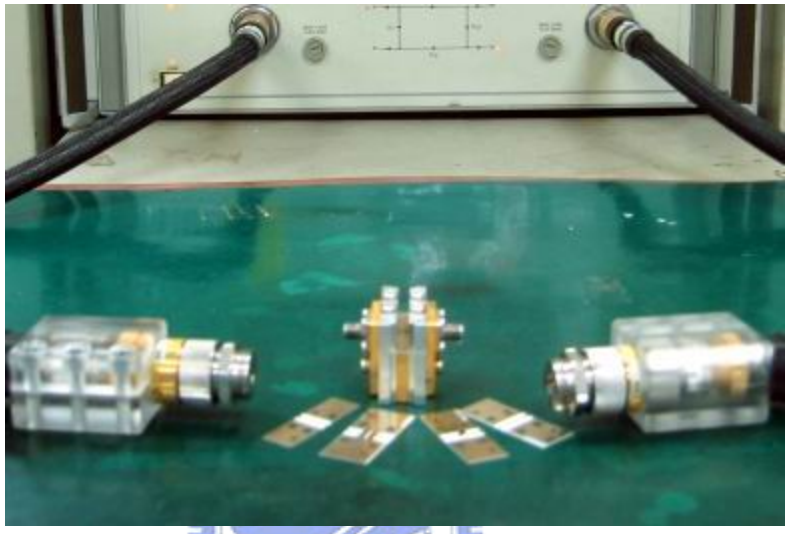


Figure 3.9 The photo of the TRL calibration kit

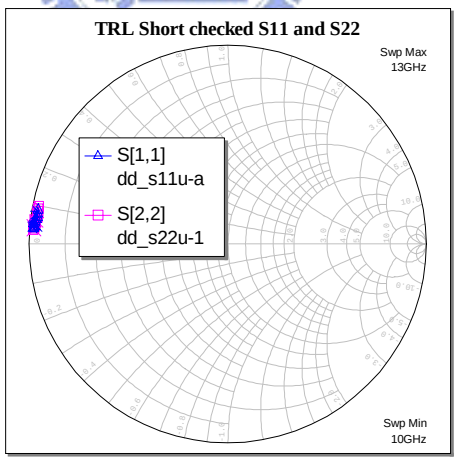


Figure 3.10 TRL calibration result S11 and S22 short curve

We need to measure the small signal S parameter of device at FET “on” and “off” states. A TRL calibration kit as shown in Figure 3.9 was designed to improve the calibration. In that kit we used Rogers 4003 PCB as the substrate material with parameters such as 20mil

thickness, 1/2 once Au coating. The gap between gate and drain is 2.0 mm, and the grounding via hole is placed as close as possible.

Figure 3.10 shows the calibrated result using our calibration kit, we can use the short circuit to check out if the calibration is correct or not. As shown in figure 3.10, the short curve is very closed to the ideal short in the smith chart, so we can make sure that the calibrated result is very reliable. The measured results of NEC HJ-FET S-parameters were as shown in Figure 3.11 and Figure 3.12.

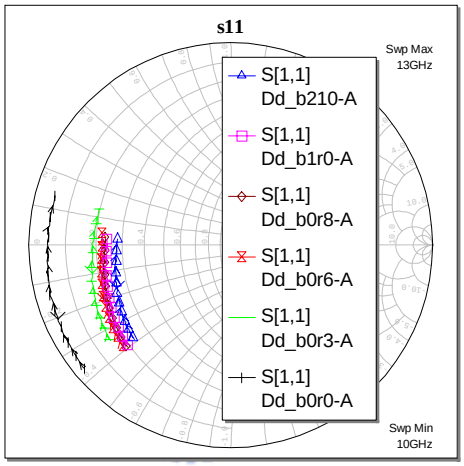


Figure 3.11 HJ-FET S11 measured curve at variable drain bias condition and Vgs is fixed

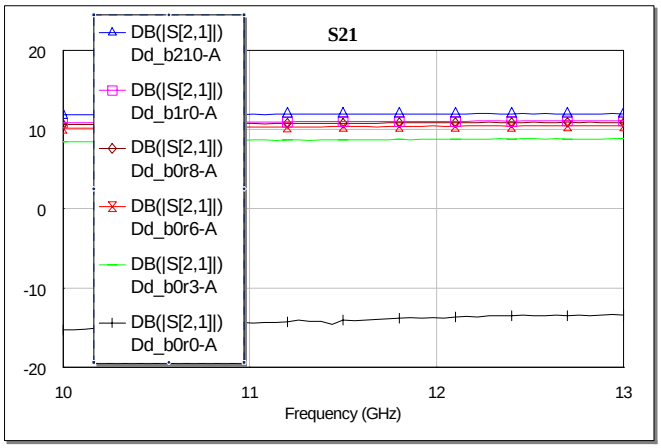


Figure 3.12 HJ-FET S21 measured curve at variable drain bias condition and Vgs is fixed

3.4 Design Procedure of the Active Balanced Switching Mixer

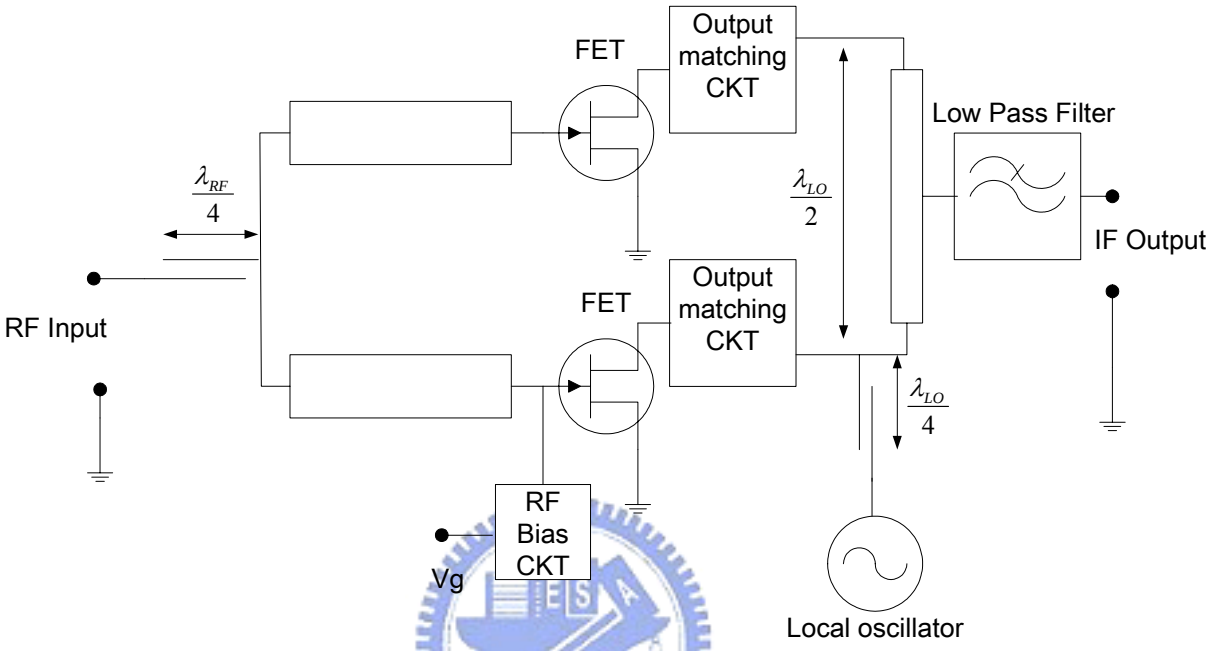


Figure 3.13 The block diagram of the active balanced switching mixer

We had design the RF couple and microstrip phase shift lines as shown in Figure 3.13. The phase shift lines were used to transform the impedance Z_{OFF} from low impedance to high impedance as shown in the Figure 3.14. The simulation result of RF port input return loss of the mixer is as shown in Figure 3.15.

In this circuit we also added devices such as balun, IF low pass filter and LO couple line at the output port as shown in Figure 3.16. Figure 3.17 and Figure 3.18 show the mixer layout and an actual fabricated circuit photo.

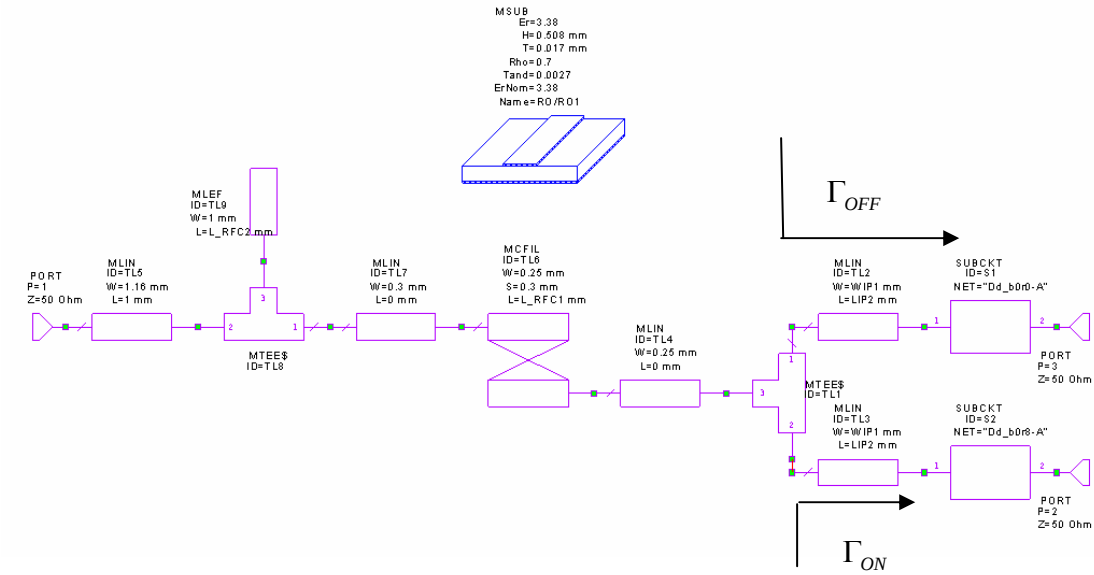


Figure 3.14 The mixer input port simulation circuit

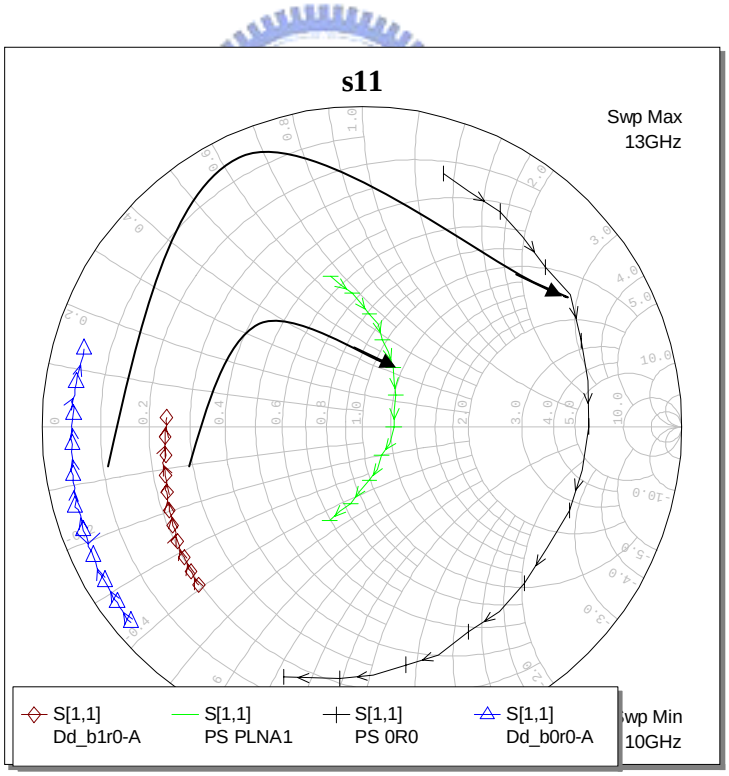


Figure 3.15 Impedance transformation illustrated by smith chart

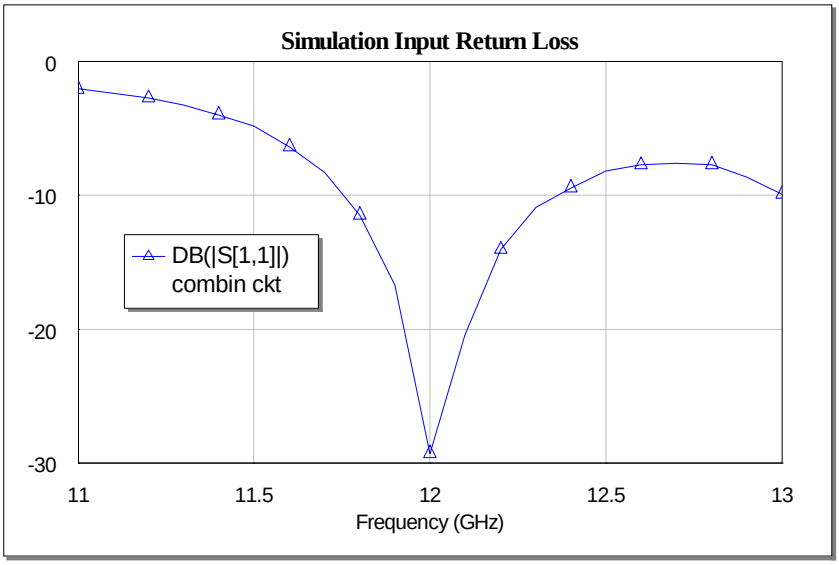


Figure 3.16 simulation result of input return loss

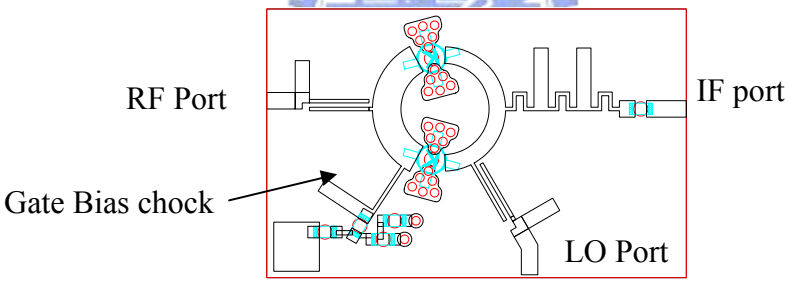


Figure 3.17 Layout of the mixer

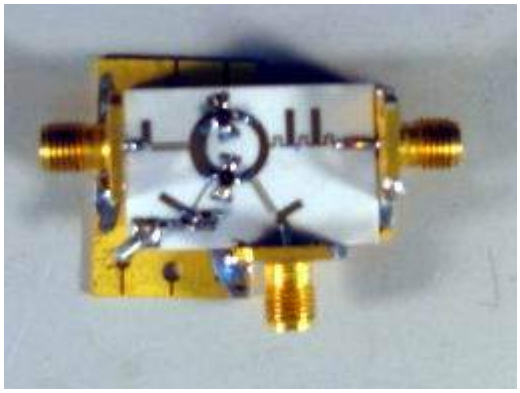


Figure 3.18 Photo of the mixer