國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

元件可靠度的改善及類比電路應用時之影響

Reliability investigation for process improvement and on
analog circuit application

研 究 生：林榮俊

指導教授：雷添福 教授

中 華 民 國 九 十 六 年 七 月

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摘要

　　隨著半導體工業科技的日新月異,製程技術的快速進步,使各種功能能夠同時置入於一顆晶片之中的可行性就不斷的在提升,也就是希望利用先進半導體製程來整合數位和類比功能於單一晶片中,此時對於半導體元件的可靠度除了傳統數位電路的考量,在類比電路使用時的可靠性的研究也隨之而來,.

　　本篇論文首先提出在深次微米元件的製程之中的回火條件控制上,時間的控制比溫度的控制更能有效改善元件熱載子的可靠性問題.當半導體深次微米製程中,源極工程用到銦(Indium)元素時,可以利用較低的溫度但較長時間的回火條件,使其均勻擴散來達到源極濃度較低, 源極電場較小進而使其有較佳熱載子的可靠性與元件特性,與此同時,當考慮系統單晶片對元件有不同功能的要求時,利用製程與元件模擬軟體的幫助及實際製程的驗證結果,適當的利用源極工程,當元件尺寸越來越小的時候,大角度的植入可以調整元件通道中二維濃度的變化,從而改變元件的各項特性,使其具有數位電路需要的大的開啟電流以及較小的靜態電流,並且同時具備類比電路的高輸出電阻和電壓增益,除此之外透過高電壓加速測試方法,來比較元件在類比電路的操作特性和傳統數位電子元件操作特性的差異之處,發現在類比電路時元件操作特性更容易有劣化的現象.進一步比較類比電路中之重要的參數不匹配特性的變化, 發現 NMOS 的電流在遭遇高電壓後與PMOS 相比, 不匹配特性會有明顯劣化或變大的結果. 這個現象值得提供給類比電路設計時電路設計者考慮元件劣化對參數不匹配特性的改變,因電路隨使用時間之增加而元件劣化對參數不匹配特性的改變,使得數位電路仍正常工作時,但類比電路因不匹配特性的改變而導致整個電路不能正常工作,也就造成單晶片的失效的現象.

Reliability investigation on process improvement and for analog circuit application

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Abstract

The dissertation addresses the issues related to reliability improvement of CMOS device and reliability of CMOS device on the analog circuit application especially the mismatch degradation of devices on the analog circuit.

In the beginning, the effect of post-thermal annealing after indium-halo and As-halo implantation on the reliability of sub-0.1um MOSFETs was investigated. We found that the control of annealing time is more efficient than that of annealing temperature with respect to improving the hot carrier-induced device degradation. The best results of device performance were obtained with post-annealing treatment performed at medium temperatures (e.g., 900) for a longer time.

Secondary, MOSFETs having 20 Å and 32 Å gate oxide thickness of 0.13 μ m technology are used to investigate DC hot carrier reliability at elevated temperatures up to 125 . The research also focused on the degradation of analog properties after hot carrier injection. Based on the results of experiments, the hot carrier degradation

of Id,op (defined based on analog application) is found to be the worst case from room temperature to 125 . This result should be a valuable message for analog circuit designers. As to the reverse temperature effect, the substrate current (Ib) commonly accepted as the statues for monitoring the drain avalanche hot carrier (DAHC) effect should be modified since the drain current (Id) degradation and Ib variations versus temperature have different trends. For the devices having gate oxide thinner than 20 Å, we suggest that the worst condition in considering hot carrier reliability should be placed at elevated temperature.

Finally, hot carrier stress impact on mismatch properties of n and p MOS transistors with different sizes produced using 0.13 μ m CMOS technology is presented for the first time. The research reveals that HCI does degrade matching of nMOSFETs' properties, but, for pMOSFETs, the changes are minor. Due to matching variation after HCI stress, for analog circuits' parameters, it is found that the after stress lines of n and pMOSFETs exhibit cross points for both σ (ΔVt,op) and σ (ΔIds,op/Ids,op) drawings. It is suggested that the cross points can be used to indicate the minimal size for n and p pairs to have the same degree of mismatch in designing analog circuits. In addition, the interpretations for the differences in n to pMOSFETs and Ids,op to Ids,sat mismatches are provided with experimental verifications.

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Contents

Chapter 1 Introduction

Chapter 2 Efficient improvement of Hot Carrier-Induced Device's Degradation for Sub-0.1μm CMOS Technology

Chapter 3 Influence of Pocket Implant on Digital and Analog Performances of Nano-MOSFET

Chapter 4 An Investigation on Hot Carrier Effect at Elevated Temperatures for nMOSFETs of 0.13 um Technology

Chapter 5 An Investigation on Hot Carrier Effect at Elevated Temperatures for pMOSFETs of 0.13 um Technology

Chapter 6 Mismatches after Hot-Carrier Injection in Advanced Complementary Metal-Oxide-Semiconductor Technology Particularly for Analog Applications

Chapter 7 Conclusion and Future Work

Table Captions

Chapter 4

Chapter 5

Chapter 6

Figure Captions:

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Chapter 1

Introduction

1.1 Research Background and Motivation

The integrated circuit (IC) industry has followed a steady path of shrinking device geometries for more than 40 years. It is widely believed that this process will continue for at least another ten years. According to the International Technology Roadmap for Semiconductor (ITRS), by extending this device scaling and increased functionality scenario to the year 2014, minimum feature sizes are projected to be 32 nm and chips with $>10^{11}$ components are expected to be available. However, there are increasingly difficult materials and technology problems to be solved over the next decade if this is to actually occur and, beyond ten years, there is great uncertainty about the ability to continue scaling metal-oxide-semiconductor field-effect transistor (MOSFET) structures. The industry is also growing from major digital logic circuit to System on a Chip (SoC) era. The major issues need to be handled on the difference operation requirements for devices used between digital and analog circuit in the same time.

In the development of 0.1um technology, the drain engineering is important to match the device universal curve (Ion-Ioff) and Vt roll-off. The major approach will

be used the indium implant to achieve this purpose with less lateral diffusion due to it more heavy ion mass or less diffusivity.

The Indium implant will also cause large silicon interstitial so it will need the post thermal anneal to eliminate the interstitial due to the implant. But the thermal budget is sensitive with respect to anneal time and temperature condition. In this chapter it will be show the combination of anneal temperature and anneal time with the device performance and HCI reliability to find the best condition will be the time to anneal the interstitial.

Secondly, we investigate the degradation of parameter for analog circuit application used. The hot-carrier degradation of N/P MOSFET's is investigated from the viewpoint of analog operation. Applying sensitive measurement methods was taken to determine (The parameters are investigated to) drain current, drain conductance, and transconductance in the saturation regime besides the commonly investigated parameters in the linear regime of operation.

On the basis of previous research activities, lifetime criteria for hot-carrier-stressed MOSFET's have undergone changes. They generally aim for a closer relation to operation conditions, while covering the worst case of operation and still assuring easy applicability. This effort has concentrated primarily on the digital case and has reached a status so that today, stressing conditions, the electrical

parameters to characterize the damage, and the extrapolation to duty cycles and voltages of operation can be defined in an appropriate way. The important case of analog applications has not yet reached the dame status of knowledge, since analog CMOS applications differ from digital ones in a number of points, as listed below.

1) Operation point: Analog devices usually operate in the saturation region with a quasistatic low gate voltage. Thus neither a relaxation of reliability criteria due to field-assisted detrapping during off-state periods can be considered nor a duty-cycle-factor applied. Moreover, we like to point out that the analog operation region includes the gate voltage range with maximum degradation.
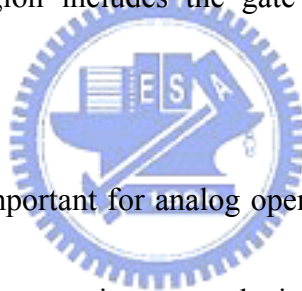
2) Device parameters important for analog operation: Besides the current drive capability, which is the most important device parameter for digital operation, the small signal parameters are of similar or even greater significance in the analog case. Of prime importance are the differential drain output conductance $Gds = \Delta Id/\Delta Vd$ and the transconductance $gm = \Delta Id/\Delta Vg$, which determine important parameters in analog circuits such as gain, frequency response, linearity and harmonic distortion. Moreover, good matching is an essential demand, since in analog circuits this property is responsible for the accuracy of differential stages and current mirrors. As a consequence the

maximum allowable parameter changes in analog circuits due to hot-carrier

degradation are often much smaller than in digital applications, where

dot-carrier induced parameter changes of 5 or 10% are frequently used

lifetime criteria.

3) Channel length: In order to improve the matching behavior, channel lengths

   used in analog circuits are usually a few times greater than the minimum

   channel length allowed by the process technology. For those greater lengths

   also the small signal parameters are improved.

Then, it was also investigated the mismatch degradation after HCI stress for

analog circuit application. It is the first time that the mismatch behaviors are

investigated after the HCI stress. From this work, it could provide an important design

guideline to reduce the circuit failure coming from mismatch value increased after the

product used for a certain time.

Device mismatch is too often treated as part of the black art of analog design.

However, extensive studies into the matching behavior of devices have yielded a good

understanding of the underlying physical phenomena and offer designers quantitative

models for the prediction of device variations.

Random device mismatch plays an important role in the design of accurate

analog circuits. Models for the matching of MOS and bipolar devices from open

literature show that matching improves with increasing device area. As a result, accuracy requirements impose a minimal device area and this paper explores the impact of this constraint on the mismatch performance of general analog circuits after stress.

1.2 Organization of This Thesis

This thesis is organized into seven chapters.

Following the introduction, the effect of post-thermal annealing after indium-halo implantation on the reliability of sub-0.1-um nMOSFETs was investigated. We found that the control of annealing time is more efficient than that of annealing temperature with respect to improving the hot carrier-induced device degradation. The best results of device performance were obtained with post-annealing treatment performed at medium temperatures (e.g.,900 C) for a longer time.

Chapter 3 presents analog device design in deep submicron regime is particularly challenging due to conflicting digital performance requirements and the circuit requirements in analog applications. To optimum digital and analog performance for SoC is important. Pocket or halo designs used in high performance digital CMOS design can improve short channel effect (Vt roll-off) but degrade analog device

performance. It is shown that the device transconductance (gm), output resistance (Rout) and Early voltage have a crossover phenomenon to gate length variations with different pocket. The Early voltage is divided in two parts, VA of fore cross due to CLM[1] and VA of back cross due to DIBL[2][3][4]. This paper presents non-uniform channel doping have distinct design concept with gate length variations to optimize the Early voltage by diverse pocket implantation experiments.

Chapter 4 describes n-channel metal–oxide–semiconductor field-effect transistors (nMOSFETs) having 20 and 32A˚ gate oxide thicknesses of 0.13 um technology were used to investigate DC hot-carrier reliability at elevated temperatures up to 125 C. The research also focused on the degradation of analog properties after hot-carrier injection. On the basis of the results of experiments, the hot-carrier degradation of Id,op (drain current defined on the basis of analog applications) is found to be the worst case among those of three types of drain current from room temperature to 125 C. This result should provide valuable insight to analog circuit designers. As to the reverse temperature effect, the substrate current (Ib) commonly accepted as the parameter for monitoring the drain-avalanche-hot-carrier (DAHC) effect should be modified since the drain current (Id) degradation and Ib variations versus temperature have different trends. For the devices having a gate oxide thinner than 20A˚ , we suggest that the worst condition in considering hot-carrier reliability

should be placed at elevated temperatures.

. Chapter 5 presents DUT under stress conditions were set at temperature 25 ℃, 75 ℃ and 125 ℃, and Vg biased at peak substrate current and maximum gate voltage as drain voltage. It is found that the pMOSFET's hot carrier mechanism is no longer dominated by negative oxide charges. Comparing different stress modes, the stress with the maximum gate voltage and the higher temperature cause the most severe current degradation. As a result, peak substrate current may not directly indicate hot carrier effect anymore, which is inconsistent with the conventional concept. After comparing all the drain currents, it is found for first time that Id,op is the worst among three kinds of currents. Such message should be valuable for analog circuit designers to have their circuits exhibiting satisfactory reliability.

Chapter 6, hot carrier stress impact on mismatch properties of n and p MOS transistors with different sizes produced using 0.15 μm CMOS technology is presented for the first time. The research reveals that HCI does degrade matching of nMOSFETs' properties, but, for pMOSFETs, the changes are minor. Due to matching variation after HCI stress, for analog circuits' parameters, it is found that the after stress lines of n and pMOSFETs exhibit cross points for both σ (ΔVt,op) and σ (ΔIds,op/Ids,op) drawings. It is suggested that the cross points can be used to indicate the minimal size for n and p pairs to have the same degree of mismatch in designing

analog circuits. In addition, the interpretations for the differences in n to pMOSFETs

and Ids,op to Ids,sat mismatches are provided with experimental verifications.

Conclusions are finally made in Chapter 7

Chapter 2

Efficient improvement of Hot Carrier-Induced Device's

Degradation for Sub-0.1μm CMOS Technology

2.1 Introduction

The reduction in threshold voltage with decreasing channel length is widely used as an indicator of the short-channel effect (SCE) in evaluating complementary-metal oxide-semiconductor (CMOS) technologies.[1] Since metal-oxide-semiconductor field-effect-transistors (MOSFETs) are being scaled down to 0.1 umm and below, this adverse Vth roll-off effect may be a major limitation on deep-submicron-device performance. Thus, finding ways to suppress the SCE while maintaining sufficiently low Vth is a key to working with sub-0.1 um MOSFETs because it is essential to manufacturability and reducing system power needs.[2] In order to control the SCE in the sub-0.1 um regime, it is necessary to reduce gate oxide thicknesses and source/drain extension-junction depths. However, the possibility of direct tunneling limits the extent to which gate oxide thicknesses can be reduced,[3] and reducing source/drain extension junction depths through lowering thermal budgets gives rise to the dopant activation problem, which refers to degradation of device driving

capabilities. In this context, lateral channel engineering gives an extra degree of

freedom in efforts to limit adverse SCE effects.[4] Recently, locally high doping

concentrations in channels near source/drain junctions have been employed via lateral

channel engineering, e.g., halo,[5] pocket,[6] tilted-channel implantation (TCI).[2]

and tilted implantation punchthrough stopper (TIPS).[7] These implantations

introduce the same types of impurity used in channel regions following gate-etching,

which can be symmetrical[6][7] or asymmetrical[8] with respect to the deep source

and drain implants. Engineering channel dopant profiles for localized halo implants

have been used extensively in deep-submicron CMOS work and has become

indispensable for achieving sub-0.1 um CMOSFETs.[9] Indium (In) has been

successfully used in fabricating abrupt nMOSFET profiles because of its low

diffusion constant,[10] which leads to shallower deep-submicron-nMOSFET

source-drain extension/halo profiles. Unfortunately, interstitial Si is introduced during

In implantation resulting in an increase in leakage current and degradation of device

performance.[11] Besides, the hot-carrier-induced device's degradation was also

enhanced; thus, a post-thermal annealing (PA) treatment after In-halo implantation is

proposed to solve these problems. However, pMOSFET device characteristics are

easily degraded by post thermal treatment because of the rediffusion of channel

doping. In this work, we inspect device characteristics and the hot-carrier effect of

B-halo nMOSFETs, In-halo nMOSFETs, and As-halo pMOSFETs. The effect of PA on hot-carrier-induced device's degradation was also investigated for these CMOSFETs. We propose an appropriate PA for In-halo nMOSFETs and As-halo pMOSFETs to obtain high performance as well as good reliability for sub-0.1 um CMOSFETs.

2.2 Experiment

Devices with channel lengths as small as the sub-0.1um range were fabricated on 8-in wafers (resistivity: 15–25 Ωs/cm) using the conventional CMOSFET twin-well process. After shallow-trench isolation techniques, n/p-wells were formed using MeV-implanted phosphorus (P) and boron (B) ions. Dual-gate CMOSFETs were fabricated using nitrided gate oxide (electrical oxide thickness ~ 25 A), grown by rapid thermal oxidation in NO ambient followed by poly-Si layer deposition. After gate patterning, n/p source/drain extensions were formed using, respectively, arsenic (As) and B-implantations. Then, tilted-angle halo-implantation was applied at 20–30 deg using B (at 10–30 keV, 2-5 x 10^{13} cm^{-2}) and In (at 120–180 keV, 1-3 x 10^{13} cm^{-2}) to produce nMOSFETs, and As (at 110–130 keV, 2-4 x 10^{13} cm^{-2}) to produce pMOSFETs. After halo implantation, various annealing schemes were employed using rapid thermal processing (RTP) at 900 to 1050 C for various

11

annealing times. A thin liner oxide was deposited at 500 to 900 C, followed by

SiN-spacer deposition at 400 to 800 C. After formation of a 0.1 um-thick composite

liner-oxide/SiN spacer, n+/p+ deep source/drain junctions were formed using As (at

40–60 keV) and B (at 6–10 keV) ion implantation. Finally, the wafers were annealed

using RTP at 1000 C followed by $CoSi_2$ salicidation processing, and then completed

using standard backend flow processing. To investigate the hot-carrier effect, device

stressing and measurements were carried out on a probe station at various drain

voltages ($|V| = 1.2\text{-}2.0V$) and gate voltages ($|V| = 0\text{-}1.8V$) with a stressing time

ranging from 0 to 100 min.

2.3 Results and discussion

2.3.1 Indium-halo vs boron-halo for nMOSFETs

Threshold voltages, obtained using the G_{mmax} method, are shown plotted

against effective channel lengths (L_{eff}) in Fig. 1(a). Compared to B-halo-structure

devices, the In-halo samples formed localized high-dose halo structures because

of their low diffusion constants, improving the punchthrough margins of the

devices. The In-halo samples were free of apparent reverse short-channel effects

(RSCEs), while the conventional B-halo samples exhibited such effects.

Transient enhanced diffusion (TED), which is believed to be the cause of RSCEs,

12

was effectively suppressed in the In-halo samples [12][13] due to indium deactivation. [14] Thus, In-halos allow Vth reductions while increasing device resistance to SCEs. Large amounts of interstitial Si are generated by As-extension implantation and enhanced by In-halo implantation. These Si interstitials can react with the In dopant more efficiently, resulting in a more pronounced deactivation, and causing accelerated Vth roll-offs in short channel devices.[15] Thus, PA is proposed to remove these Si interstitials and suppress the TED phenomenon. Although high-temperature (>1000 ℃) annealing is conventionally used for sub-100 nm device fabrication, junction depths will be increased after 1000 C RTP annealing, resulting in higher device Vth roll-offs. In this study, we found device SCEs can be improved by annealing at 900 ℃ for longer periods of time (>1 min.). It is believed that Si interstitials can be removed by medium-temperature annealing for appropriately longer times without degrading device SCEs. In this work, higher saturation Vths and RSCEs apparently occurred in In-halo nMOSFETs annealed at 900 C for longer periods of time. Medium-temperature annealing can improve In-halo device SCEs, even in the sub-0.1 μm-channel-length range, thus reducing the device's off-state drain current (I_{Dos}). Figure 1(b) illustrates that the I_{Do} of devices can be reduced with the 900 ℃ long time annealing. Notably, higher saturated Vth and

apparent RSCE occurred in In-halo nMOSFETs at 900 C with longer time annealing, improving the In-halo device's SCE. We believed that the Si interstitial can be removed by medium-temperature annealing for an appropriately longer time without degrading the device's SCE. Previous work15) had shown that the mobility of In halo nMOSFETs was better than that of the B-halo device particularly at L_{eff} less than 0.1um. Although the localized In-halo dopant was located only around the extension junction without degrading the device's driving capacity, the hot-carrier effect of the In-halo device was still a problem and became more serious as the device dimensions decreased. In comparison with B-halo nMOSFETs, the hot carrier-induced Gm degradation of In-halo nMOSFETs becomes more serious after hot-carrier stress particularly at higher gate voltages, as shown in Fig. 2. By the way, the In halo device shows worse subthreshold characteristic and degradation after hot-carrier stressing particularly at higher gate voltages, as shown in Fig. 3(a). After hot-carrier stressing, the device's subthreshold slope was degraded by 20mV/dec (100 -> 120mV/dec) for In-halo nMOSFETs and 7mV/dec (97 -> 104mV/dec) for B-halo nMOSFETs. The swing degradation indicates the creation of interface traps resulting in a threshold voltage shift.[16] Gate-induced drain leakage (GIDL) in both nMOSFETs at a negative gate bias of V_G = -0.5V was also increased. It has

been reported [16] that GIDL is a direct result of the generation of interface states; thus, the largest degradation in I_{Dsat} coincides with the largest increase in interface state density. Thus for In-halo nMOSFETs, worse subthreshold characteristics with larger Ido and GIDL are found. Furthermore, the gate leakage of the In-halo device was also larger than that of the B-halo device, and increased after hot-carrier stress particularly at a higher gate voltage, as shown in Fig. 3(b). It is presumably because a larger interface state was found for the In-halo nMOSFET, thus the In-halo device characteristics and reliability were degraded and then aggravated after hot-carrier stress. In this work, the In-halo device's subthreshold swing and I_{do} can be improved with PA particularly at 900 C with longer time annealing, as shown in Fig. 4. Figure 5 reveals that the hot-carrier-induced saturated drain current (Idsat) degradation of In-implanted nMOSFETs was more serious than that of B-implanted nMOSFETs. With an appropriate PA, the Idsat degradation of all In-implanted devices can be improved to be lower than that of B-implanted devices. For In-halo nMOSFETs, very low drain degradation (<3%) was obtained by PA at medium temperature with sufficient annealing time. For sub-0.1 um nMOSFETs, the interstitial defect caused by In-halo implantation and the channel impact ionization caused by electrons can be suppressed with PA; thus, In-halo nMOSFETs with PA have a

longer lifetime with a lower substrate current (I_{SUB}) than B-halo nMOSFETs

particularly at stress voltages larger than 1.5 V, as shown in Fig. 6.

2.3.2 Optimum As-halo structure for pMOSFETS

As-halos can be used to fabricate effective pMOSFETs drain structures

which can block B-extension efficiently. For pMOSFETs, Si interstitials still

occur after As-halo implantation. These Si interstitials degrade device

performance and enhance the hot-carrier effect. Thus, an appropriate PA is

necessary to alleviate these problems. However, B-extension/As-halo structures

are easily degraded by post-thermal treatment owing to the rediffusion channel

boron-doping profile, apparently causing the pMOSFET's threshold voltage (Vt)

shift particularly at a PA using 1000 C annealing, as shown in Fig. 7. It is

apparent that the hot-carrier-induced Gm degradation can be improved

particularly with PA at 900 C with a longer annealing time without degradating

the device characteristics after hot-carrier stress. Furthermore, the pMOSFET

subthreshold characteristics can also be improved with this appropriate annealing,

as shown in Fig. 8. In order to investigate the hot-carrier effect on pMOSFET

performance, the gate leakage of As-halo pMOSFETs with various PAs was

inspected before and after hot-carrier stress, as shown in Fig. 9. Apparently, the

gate leakage can be improved apparently particularly at 900 C with longer time annealing; thus, lower interface defects can be removed using this appropriate post-treatment, suppressing the hot-carrier-induced device degradation. Figure 10 shows the hot-carrier-induced Idsat degradation of As-halo pMOSFETs after 100 min stressing with and without post-annealing. It is noted that the hot-carrier-induced Idsat degradation of As-halo pMOSFETs can be improved using an appropriate PA particularly at 900 C with longer annealing time. Thus, very low drain degradation (<1%) can be obtained by PA at medium temperatures with sufficient annealing time.

2.4 Summary

In this brief, the post-thermal annealing effect impact on devices characteristic as well as hot-carrier-induced reliability of 0.1 um CMOSFETs was inspected. The Si interstitial caused by In-halo and As-halo implantation can be removed by PA with enough annealing time. For In-halo nMOSFETs as well as As-halo pMOSFETs, device characteristics and hot-carrier-induced device degradation can be improved by post-annealing particularly at medium temperatures with long time annealing without degrading the device performance.
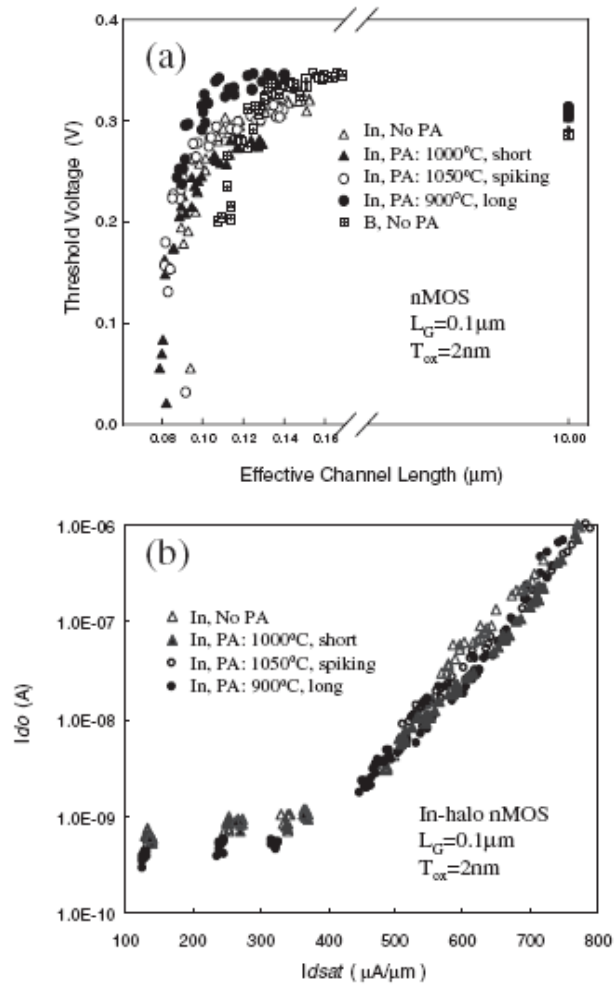
Fig. 1 (a) Threshold voltage roll-off as a function of effective channel length, and (b) Ion vs Ioff for B-implanted and In-implanted halo nMOSFETs with various PA.
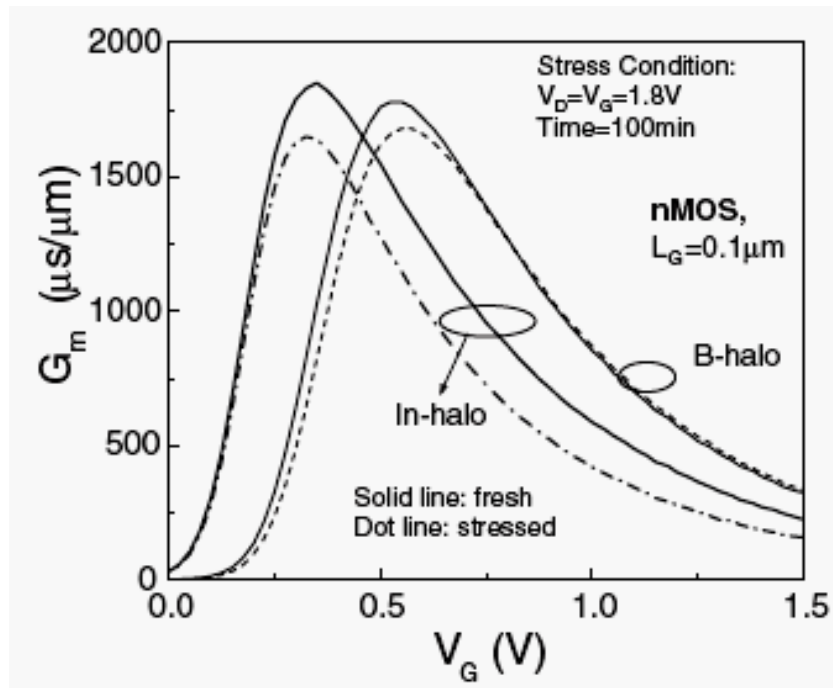
Fig. 2 Transconductance (G_m) as a function of gate voltage (V_G) for B-implanted halo and

In-implanted halo nMOSFETs before and after hot-carrier stress.
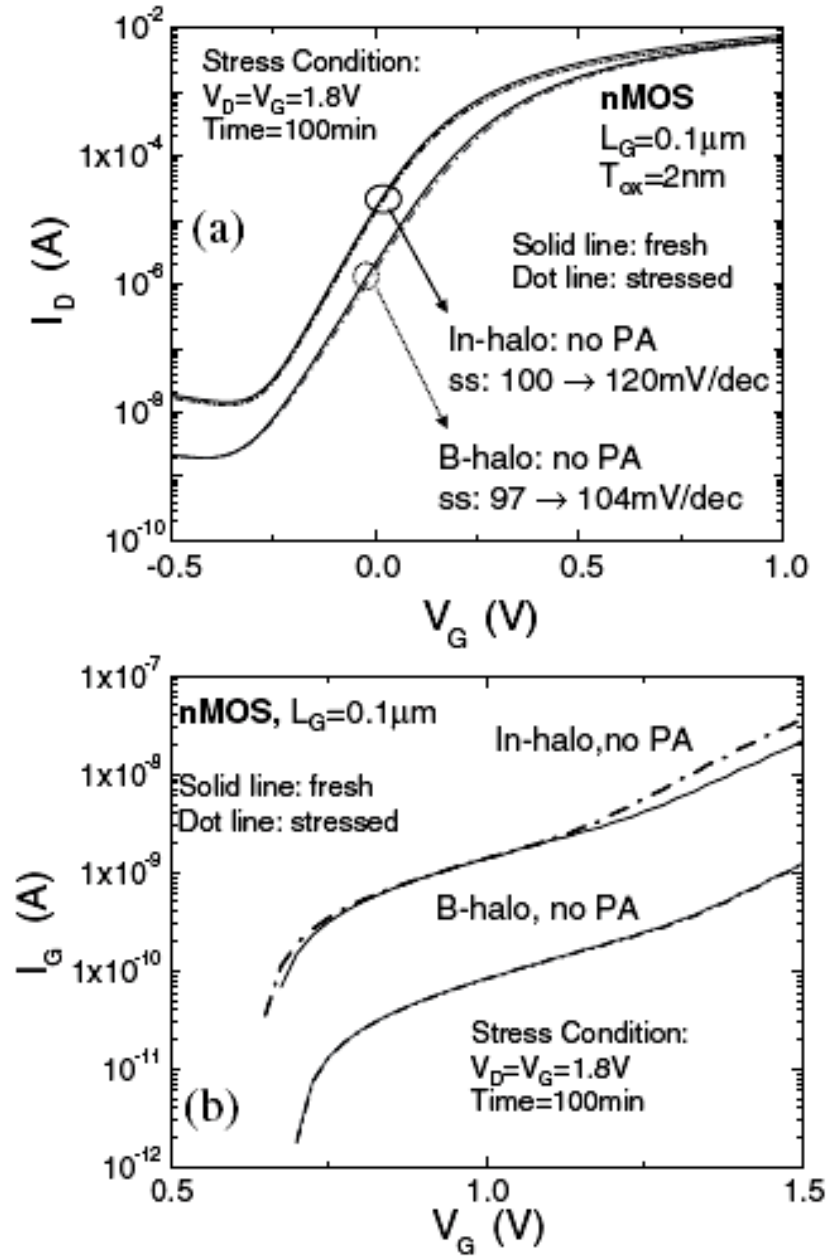
Fig. 3 (a) Subthreshold characteristics and (b) gate leakage (I_G) as a function of gate voltage (V_G) for nMOSFET with B-implanted and In-implanted halo structures before and after hot-carrier stress.
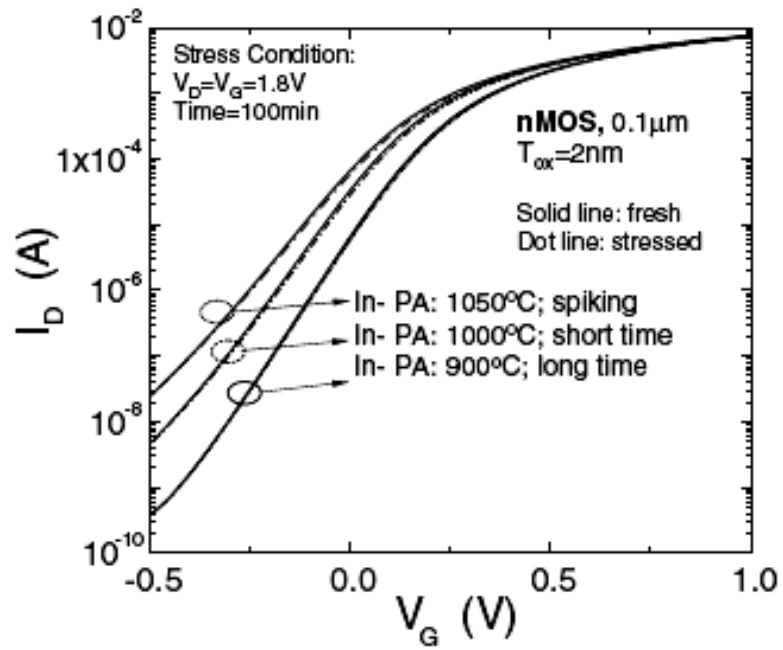
Fig. 4 Drain current (I_D) as a function of gate voltage (V_G) for nMOSFETs with various post annealing conditions before and after hot-carrier stress.
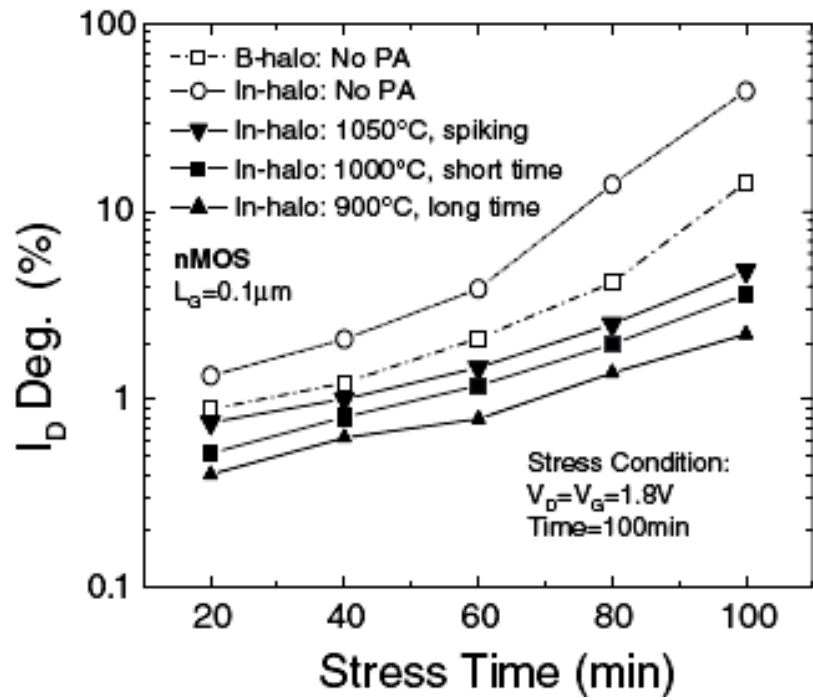
Fig. 5. Hot-carrier-induced saturated drain current (I_{DSAT}) degradation versus stress time for nMOSFETs with B-implanted and In-implanted halo structures under various post annealing conditions.
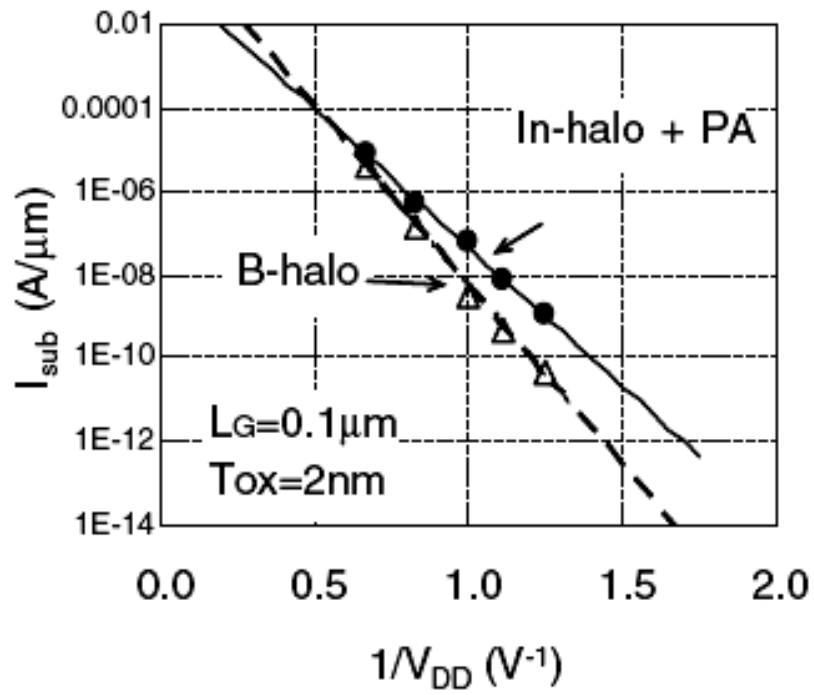
Fig. 6 Substrate current as a function of drain voltage (V_D) for B-halo nMOSFETs and

In-halo nMOSFETs with post annealing.
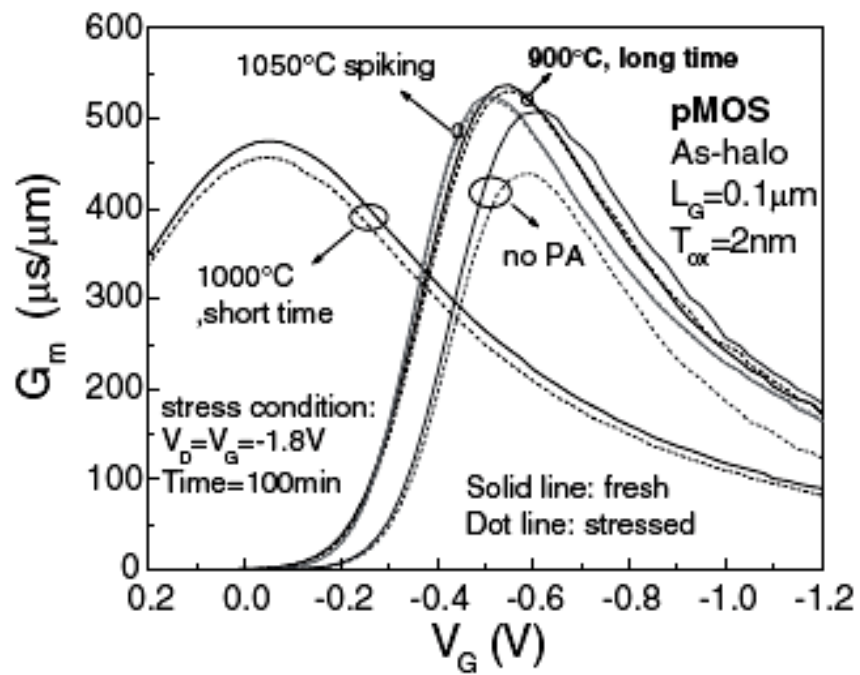
Fig. 7 Transconductance (G_m) as a function of gate voltage (V_G) As-implanted halo pMOSFETs with various post annealing conditions before and after hot-carrier stress.
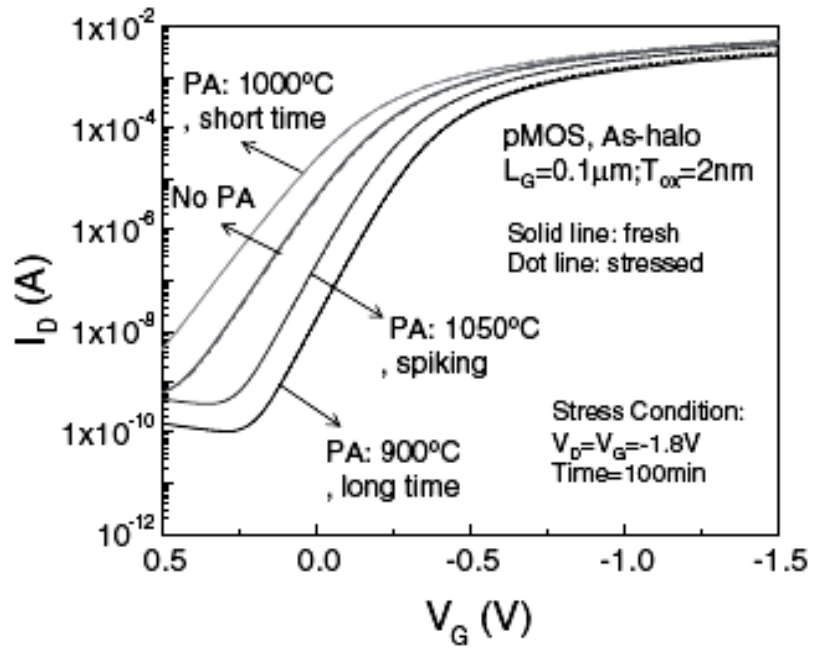
Fig. 8 Subthreshold characteristic for As-implanted halo pMOSFETs with various post annealing conditions before and after hot-carrier stress.
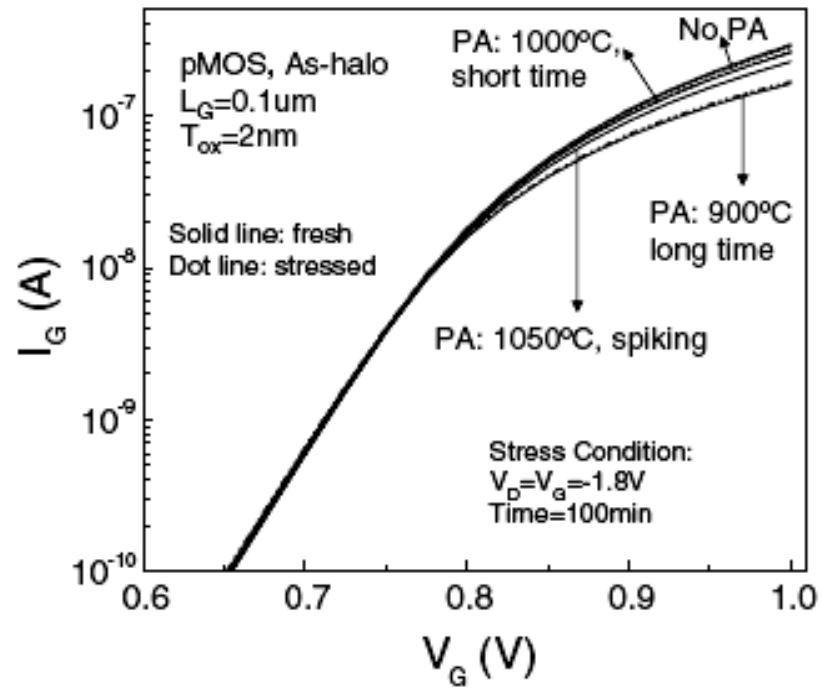
Fig. 9 Gate leakage (I_G) as a function of gate voltage (V_G) for As-implanted halo pMOSFETs before and after hot-carrier stress under various post annealing conditions.
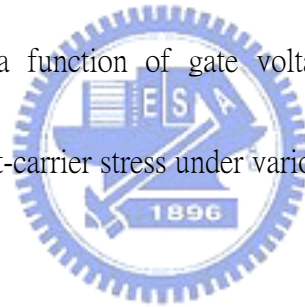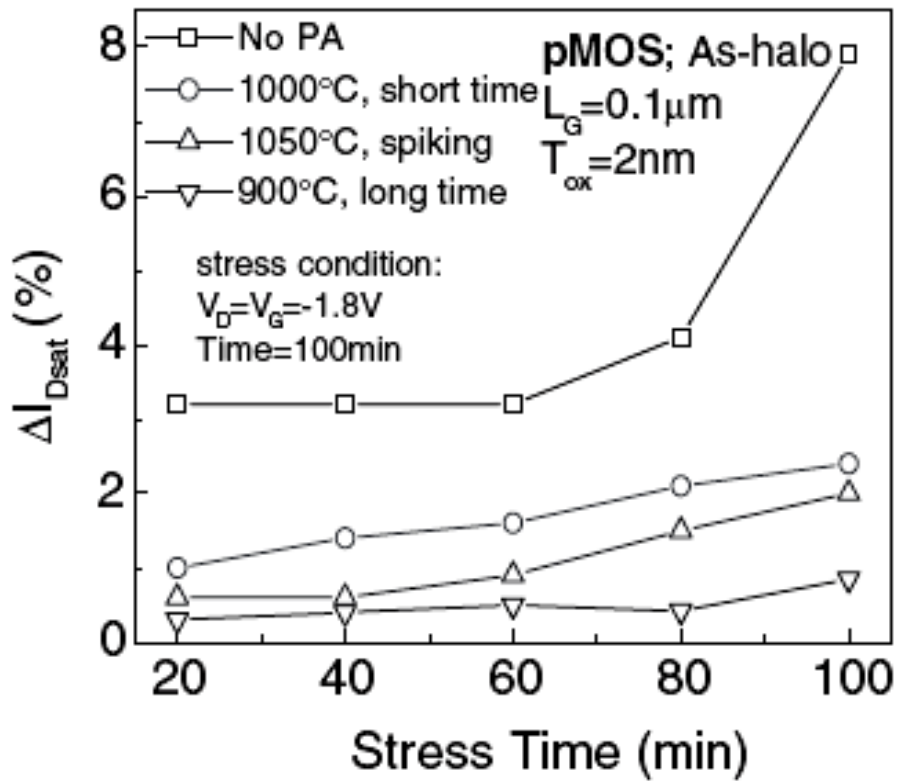
Fig. 10 Hot-carrier-induced saturated drain current (I_{DSAT}) degradation versus stress time for

pMOSFETs with As-implanted halo structures under various post annealing conditions.

Chapter 3

Drain Engineering Optimization for Nanometer nMOSFETs

on Mixed Signal Application

3.1 Introduction

The scaling of CMOS technology in nanometer regime has enabled to integrate the RF/analog and digital CMOS function together. Most of the analog applications rely on the pure digital CMOS technology [1]. The scaling of CMOS devices also reveals some difficult challenges, particularly for mixed signal system-on-chip (SoC) applications due to the tradeoff in design requirements for analog and digital applications. The key requirements for analog circuits are the signal swing, linearity, power dissipation, dynamic range (DR), bandwidth (allowed operating frequency), signal-noise-ratio (SNR), linearity, and reliability. Unfortunately, inherent tradeoff among the device parameters like threshold voltage (Vth), short channel effect (SCE), drain-induced barrier lowering (DIBL), transconductance (gm), output resistance ($Rout$), early voltage (V_A), voltage gain ($gm{\times}Rout$), and output conductance (G_{DS}) generally leads to compromise in the requirements and limits the continuous scaling.

To achieve the good analog performance, more specifically high voltage gain, or

high *gm*, and high *gm*/*Id* ratio are required. They can be achieved through strict control of SCE in deep submicron regime. On the other hand, performance of analog circuits critically depends on achieving a high V_A. High digital performance like good current drive-to-off state leakage tradeoff and SCE control are required, but often result in poor analog performance in terms of low output resistance, voltage gain, transconductance-to-drive current ratio, and matching properties [2].

Many solutions were suggested either with multiple threshold voltage designs that employed low doped substrates or with multiple gate-oxide thicknesses to accommodate higher power supplies for analog applications in SoC technology [3], [4]. However, these solutions are not sufficient for the long term due to their obvious impact on SCE and processing difficulties leading to degraded device performance. Thus, the asymmetric channel structures or single pocket (SP) were suggested for mixed signal applications [6]. They have shown good SCE control and *Vth* roll-off compared to the double pocket or super halo devices as well as super steep retrograde (SSR) devices [5], due to their laterally asymmetric channel doping profile that suppresses SCE and exploiting velocity overshoot to improve current drive. They also have shown better analog performance with increased output resistance and voltage gain over the SSR devices. Although the SP device does not need to compromise the requirements for analog and digital applications, it needs more masks than double

pocket device and result in cost increasing.

In order to optimize analog and digital performance of conventional device structure with double pocket implant devices, different pocket structures have been investigated. How to optimize those analog and digital requirements using ISE TCAD [5] will be presented later.

3.2 Device fabrication

MOSFETs fabricated using high performance 0.13um logic process is used to compare diverse pocket process optimized for high Idrive and good analog performances voltage gain. There are two pocket implant BF2 and In were carried out after the gate stack formation at the same device.
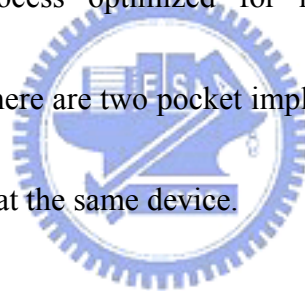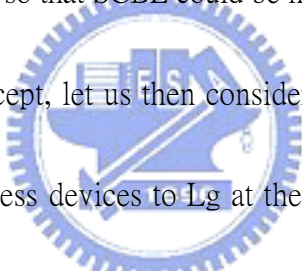
3.3 Experimental result and discussion

The threshold voltage independence on Lg is excellent Vth characteristics. Fig1 and Fig2 show Vth vs. drawn gate length (Lg) and Ion vs. Ioff respectively for diverse pocket implant doping concentration. The heavy pocket doping could lead to high RSCE as well as decrease Idrive at the same Vg bias conditions namely Vgs=Vt+0.1V (Vds=0.7). However, in the case of pocket implant devices which have good SCE control and Vth roll-off characteristics. Fig2 also shows that heavier pocket implant

could compress off current while keeping Ion current fixed

In analog circuit applications, the voltage gain is directly proportional to Rout .In [8], it's shown existing analytical models for MOSFET Rout are not adequate, because only channel length modulation effect is included. Here, we notice, The Rout curve can be clearly divided into four regions with each region dominated by a mechanism in Fig3 be shown .It is worth noting that the second region is the near-saturation region dominated by CLM. The third region is dominated by DIBL and the fourth is the high field region in which Rout is greatly reduced by the substrate current induced body effect (SCBE).[8] In this case, Rout is continual raise so that SCBE could be neglected.

In view of foregoing concept, let us then consider that the variation of Rout with different pocket and LDD process devices to Lg at the same Vgst (Vgs-Vt=0.1 V) and Vd bias which Vd=0.7 V for IO and Vd=0.6v for Core. It is shown in Fig4 and Fig5. It clearly shows that cross phenomenon. The different devices structure and process could move the cross points to gate length. Hence, the Rout at least should be differentiated into two physic effect. We believe that different channel length could lead to change of physic mechanism boundary of Fig3. The fore and back cross due to CLM and DIBL respectively. The concept of Rout to variable Lg should be changed as well. The most important characteristics of Rout in analog circuit designs are the maximum Rout which determines the maximum available gain from the device. Fig6

shows the gain of wide part dependence on the Rout. To obtain the high gain devices

have different notions in distinct Lg. The lighter pocket implant concentration could

induce high Rout and gain at after of cross. Adversely, that could induce poorer Rout

and gain at before of cross.

V_A has three components, i.e., V_{ACLM}, V_{ADIBL} and V_{ASCBE} corresponding to CLM, DIBL

and SCBE, respectively. Each component can be evaluated separately.[8]

$$\frac{1}{V_A} = \frac{1}{I_{dsat}}[(\frac{\partial I_{ds}}{\partial V_{ds}}) \mid CLM + (\frac{\partial I_{ds}}{\partial V_{ds}}) \mid DIBL + (\frac{\partial I_{ds}}{\partial V_{ds}}) \mid SCBE]$$

$$= \frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}} + \frac{1}{V_{ASCBE}} \tag{1}$$
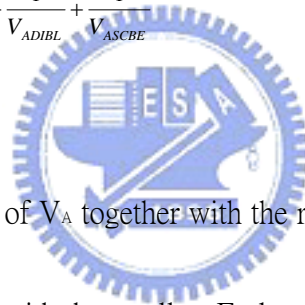
The individual component of V_A together with the resultant V_A is shown in Fig7. The

dominant mechanism is the one with the smallest Early voltage in each region.

In this case of V_A which obtaining by intersection of X axis with tangent of Vd

bias at 0.7V and 0.6V for IO and Core could exclude V_{ASCBE} because of this Vd bias is

not enough to induce substrate current. For experimental data in Fig8 and Fig9 these

are similar to the Rout that V_A appears cross points around 3 time technology node to

gate length for IO and core. Therefore, the V_A is at least dominated by two physical

effects − channel length modulation (CLM) and drain induce barrier lower (DIBL)

measured as $Vt,lin - Vt,sat$ [8].

The concept of V_A of fore cross due to CLM dominated. The length ΔL of the pinch-off region increases by an expansion in the direction of the source end with lighter pocket doping concentration and effective channel length has been reduced by ΔL at the same bias condition. In other word, the ΔL increase with decreasing pocket dose concentration could reduce V_A. CLM is not a special short-channel phenomenon, but its relative importance becomes distinctly more pronounced at short gate lengths. This is traditional notion for design V_A, but the concept of back cross is in conflict with pocket implant concentration. For long channel devices of back cross, despite CLM and DIBL should slowly be negligible. However, large residual DIBL exists at back cross for the pocket devices in Fig8, dominating the V_A values which function (1). In these dimension, higher pocket doping concentration lead to Vt,sat shift even more. The conventional explanation of channel length modulation is not entirely valid in pocket devices. Hence, these new observations have a significant impact on design of V_A by cross phenomenon of the pocket device. Anyway, the experimental results from pocket device are shown in Fig8 and Fig9. It can be seen that these devices have lower DIBL leading to higher V_A at back cross. Adversely, leading to poorer V_A at fore cross.

3.4 Summary

We have presented experimental data showing that certain pocket implant

concentration for digital CMOS technology and then found out the interesting cross

points, which imply pocket implants affect at least have two physic mechanisms CLM

and DIBL. The conventional explanation of channel length modulation is not entirely

valid in pocket devices. Hence, these new observations have a significant impact on

design of VA and Rout. The concept of back cross differs from CLM so that the

analog device design for pocket implant must be notice. The lighter pocket implant

concentration could induce higher Rout, gain and VA at back of cross. On the other

hand, the heavier pocket implant concentration could induce higher Rout, gain and

VA at fore of cross.
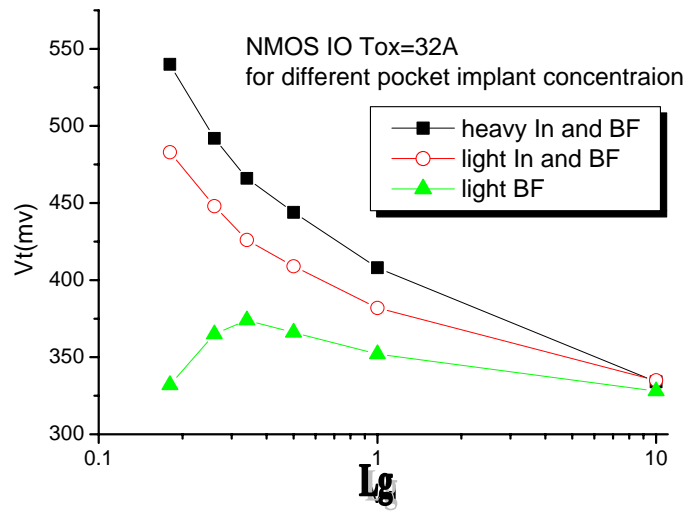
Fig1. Vt vs. Lg for different pocket implant concentration
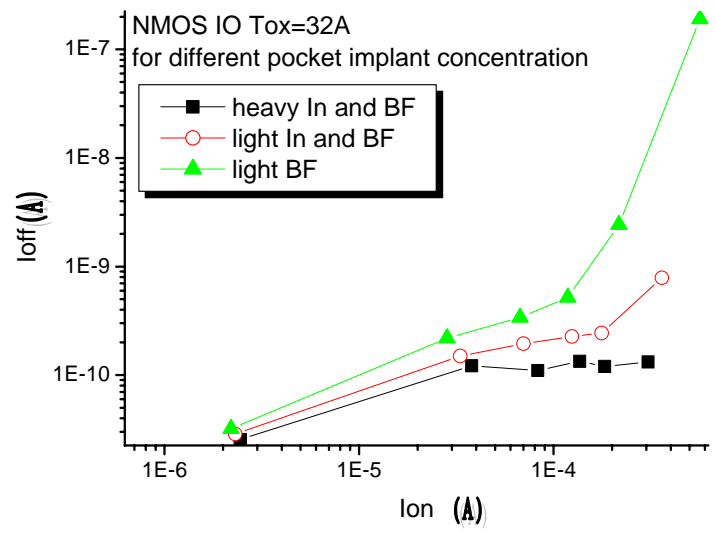
Fig. 2 Ion vs. Ioff for different pocket implant concentration
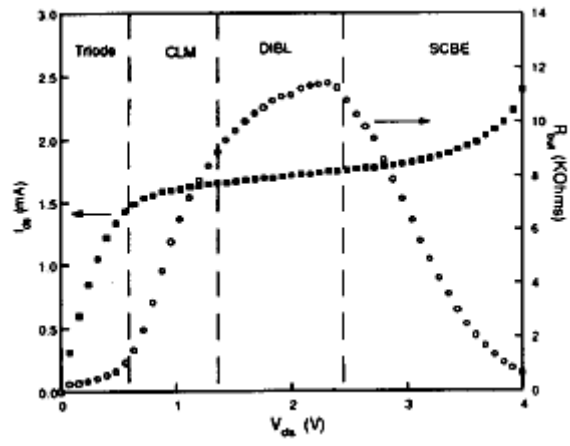
Fig. 3 Typical drain current and output resistance.
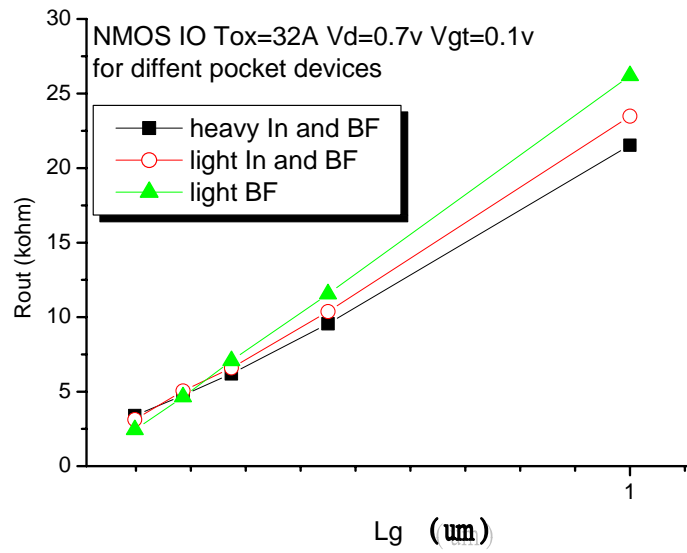
Fig4. Rout vs. Lg for NMOS IO
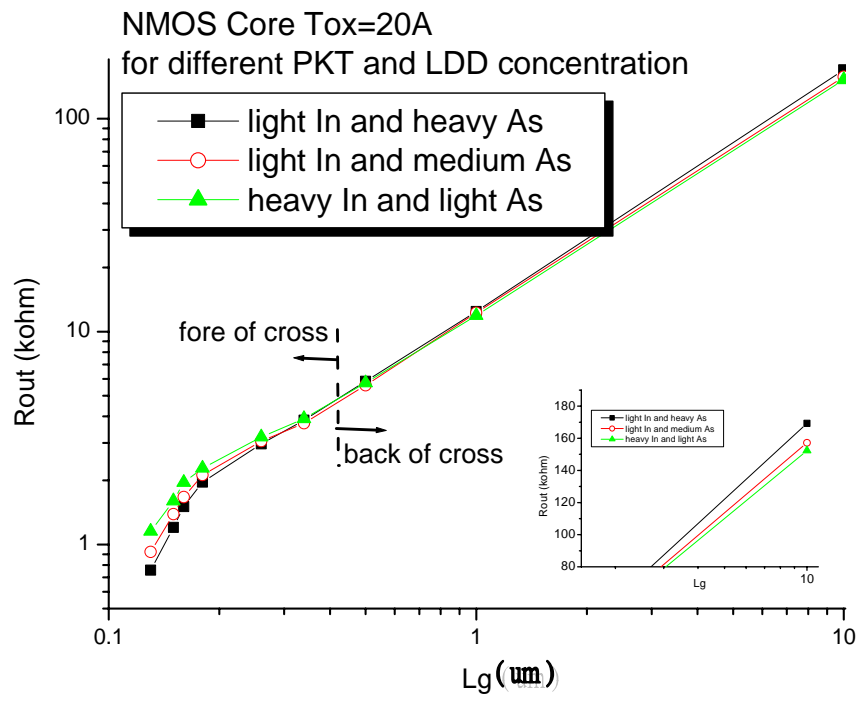
Fig5.Rout vs. Lg for NMOS Core
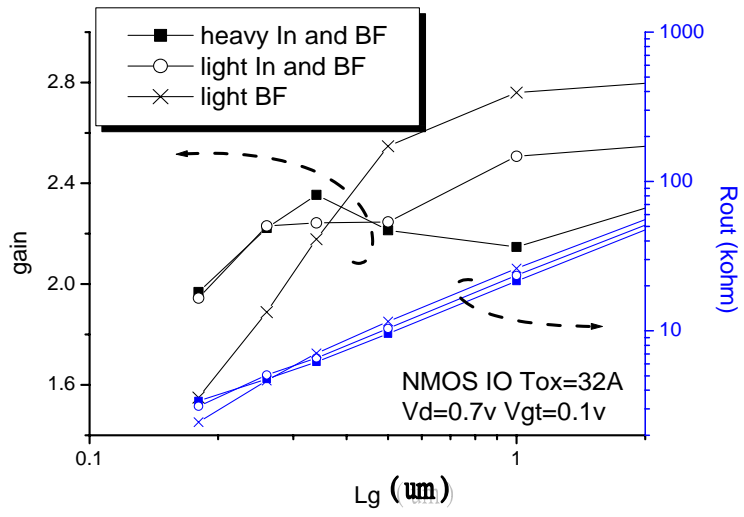
Fig6. Gain and Rout vs. Lg for different pocket implant devices.
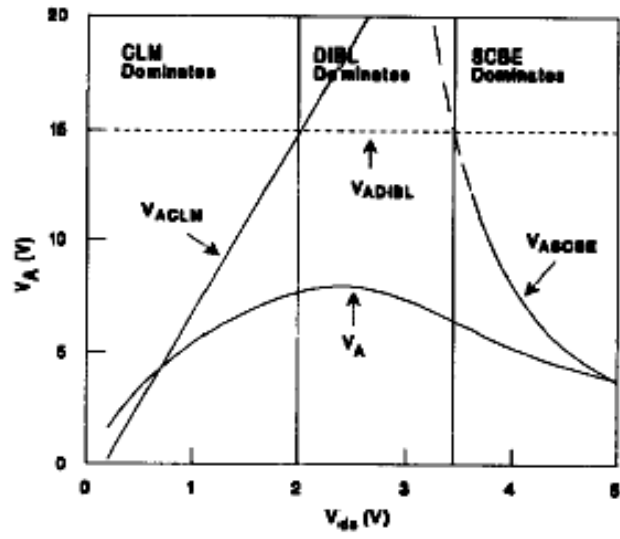
Fig7 Early voltage and its components versus Vds
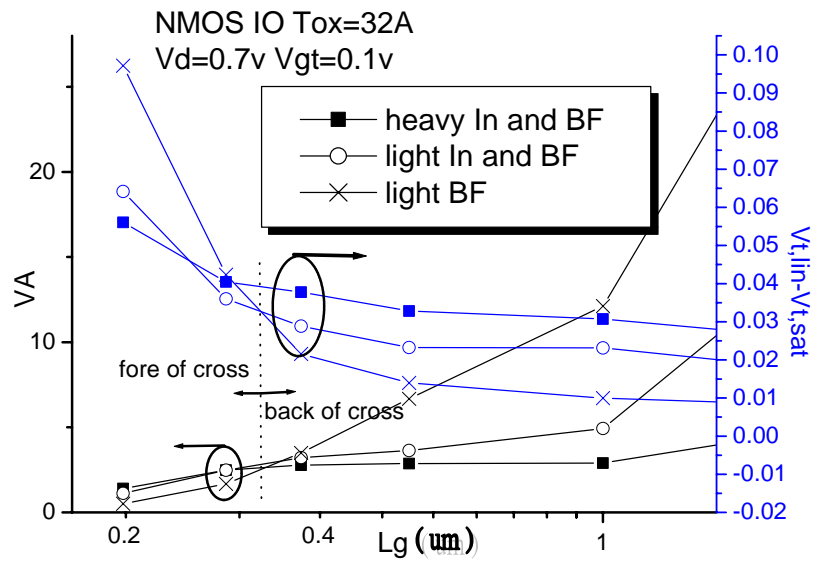
Fig. 8 V_A and DIBL vs. Lg for NMOS IO
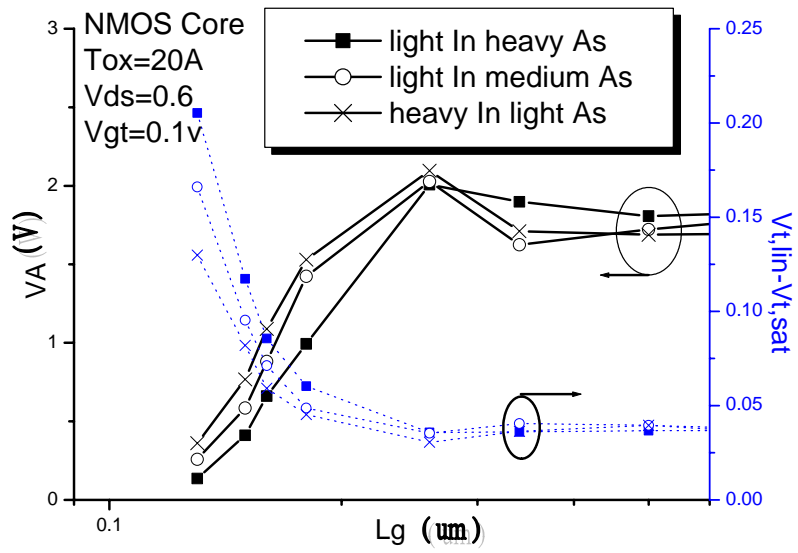
Fig. 9 V_A and DIBL vs. Lg for NMOS Core

Chapter 4

An Investigation on Hot Carrier Effect at Elevated Temperatures for nMOSFETs of 0.13 um Technology

4.1 Introduction

It is well known that, under certain bias conditions, hot-carriers in a metal-oxide-semiconductor (MOS) transistor will result in property degradation due to damage in the gate oxide and its interface. Owing to the increasing phonon scattering during the carrier' movement, the substrate current (I_b) and hot-carrier degradation of metal-oxide-semiconductor field-effect transistors (MOSFETs) are prevalently believed to be smaller at elevated temperatures [1][2]. However, the degradation of saturation drain current ($I_{d,sat}$) at high temperatures was reported to be larger due to the reduction of velocity saturation length, whereas the degradation of linear drain current ($I_{d,lin}$) was still smaller with increasing stress temperatures [3][4]. Other related studies showed that the hot-carrier effect had a transition point (voltage), which reversed the dependence of a MOSFET's I_b on temperature [5][6]. This finding was proved with the result in which the peak I_b would reverse its temperature dependence when the drain voltage (V_d) was biased across the transition voltage, which implied that a larger I_b at elevated temperature occurred only at a lower V_d. In addition, the peak I_b was found to be still

correlated with the degradation and lifetime [5][6]. These seemingly consistent findings now face new challenges as we examine the results of DC hot-carrier stress on nMOSFETs of nanometer technology.

In this study, we found that the drain current degradation at room temperature for 32 A gate oxide devices is still the worst condition by comparing to devices stressed at high temperatures, regardless of whether the stressed drain voltage is lower or higher than the transition point. Furthermore, for the first time, we show that the hot-carrier degradation of $I_{d.op}$ is the worst case among those of $I_{d,sat}$, $I_{d.lin}$, and $I_{d.op}$ from room temperature to as high as $125^{o}C$. This result should provide valuable insight to analog circuit designers.

4.2 Experimental

Tested devices were based on logic technology. The nMOSFETs used in our experiments have an effective channel length of L_{eff} = 120nm with a gate oxide thickness of 32A (I/O devices) and L_{eff} = 90nm with a gate oxide thickness of 20A (core devices), all with a width of W = 10 um. Stress conditions were (1) 25, (2) 75, and (3) $125^{o}C$, with all V_g is biased at the peak I_b. The measurement conditions are summarized in Table I. The $I_{d.op}$ in the table is defined to simulate the bias condition often used in analog circuits such as small-signal amplifiers and class-A

45

power amplifiers. Here, V_g is biased at the threshold voltage (V_t) plus 0.2V of

driving voltage

4.2.1 I/O devices

For 32A, 120nm input/output (I/O) devices, Figs. 1-3 show the experimental

substrate currents versus Vg at room and elevated temperatures for three different

drain voltages. When V_d = 2.2 V, a higher temperature causes a higher I_b. However,

when V_d = 3.0 V, a higher temperature causes a lower I_b. At V_d = 2.6 V, substrate

currents are almost independent of temperature. This voltage can be thus defined as

the transition point. The behavior of I_b versus V_g at different temperatures is

consistent with the findings of the previous studies [5][6].

As for the drain current degradation, Fig. 4 shows an example of the stress

bias set higher than the transition voltage (2.6 V). It is clear that Fig. 4 shows no

reverse temperature effect. The degradation of drain current at room temperature is

still more serious than the degradations of higher temperatures. The velocity

saturation length effect is not shown here [3][4]. In fact, not only on $I_{d,sat}$, Fig. 5

shows the degradation ratios of three drain currents, $I_{d,sat}$, $I_{d,lin}$, and $I_{d,op}$, after

5000s of stress for different temperatures. Comparing the three lines, the

degradation of $I_{d,op}$ is the largest in the entire temperature range while $I_{d,lin}$ exhibits

the worst case for digital circuit considerations. Also note that the trends in Fig. 5 clearly indicate that the room temperature situation is the most aggravated condition.

In the case of the drain bias set lower than the transition voltage, Fig. 6 still shows no reverse temperature effect at $V_d = 2.2$ V, in contradiction to a higher temperature possessing a higher I_b. In addition, room temperature still reveals the largest degradation among different temperatures for three types of drain current as revealed in Fig. 7. Again, $I_{d.op}$ is still the worst case among the three currents and $I_{d.lin}$ is worse than $I_{d,sat}$.

Actually, in the case of the drain bias set at the transition voltage, i.e., $V_d =$ 2.6 V, the results are the same as above.
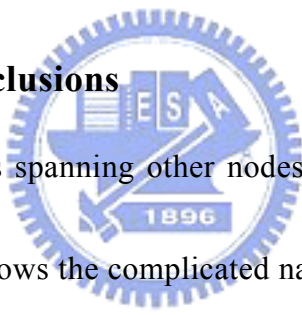
4.2.2 Core devices

For 20Aˆ, 90 nm core devices, Fig. 8 shows the experimental substrate currents versus V_g at room and elevated temperatures for $V_d = 2.2$ V. Here, a higher temperature causes a higher I_b. In fact, for $V_d = 1.8$ and 2.0V experiments, a higher temperature also causes a higher I_b, and the waveforms of I_b are very similar. No further higher V_d was tested in order to avoid inducing oxide breakdown. Therefore, it is presumable that there exits a transition point above V_d

= 2.2 V, and the reverse temperature effect is consistent with previous findings of

Aminzadeh and Wang [5][6].

Figure 9 shows the experimental $I_{d,sat}$ degradation versus stress time at

different temperatures stressed at V_d = 2.2 V. As expected, the degradations

increased as temperature rose from 25 to 125°C due to the reverse temperature

effect. Figure 10 shows the degradation ratios of drain currents at different

temperatures. Among them, the degradation of $I_{d.op}$ at 125°C is the worst case. For

digital circuits, $I_{d.lin}$ is worse than $I_{d,sat}$.

4.3 Discussion and Conclusions

Although further studies spanning other nodes of technologies and sizes are

required, the study at least shows the complicated nature of hot-carrier effects. The

significant facts revealed here are (1) I_b commonly accepted as the parameter for

monitoring the drain avalanche hot carrier (DAHC) effect [7][8] needs to be

modified since I_d degradation and I_b variations versus temperature have different

trends as shown for I/O devices here. This may be attributed to some holes flowing

to the gate oxide through the velocity saturation region, as was suggested by Koike

that the recombination of holes and electrons is the main mechanism of generating

interface traps, which then results in DAHC degradation. [9] Therefore, the I_b

formulation considering all holes of impact ionization flowing to the substrate [10] may not reflect all the facts. However, if this problem is intended to be completely solved, the question that needs to be dealt with is how the impact ionization and two-dimensional electric field in the velocity saturation region are affected by temperature and drain voltage variations. (2) In this paper, we show that, using 32A˚ I/O devices of 0.13um technology as an example, the hot-carrier degradation of $I_{d.op}$ at room temperature is the worst case for temperature varying from 25°C to an elevated value of 125°C and among $I_{d.op}$, $I_{d,sat}$ and $I_{d.lin}$, regardless of the existence of the reverse temperature effect. (3) For the devices having a gate oxide thinner than 20A˚ , the transition points are high above the operational voltages and approach the edges of breakdown. Hence, the worst condition in considering hot-carrier reliability should be placed at elevated temperatures.

		$L_{eff} = 90$ nm		$L_{eff} = 120$ nm	
		V_g	V_d	V_g	V_d
Digital	$I_{d,lin}$	1.2	0.05	1.8	0.05
	$I_{d,sat}$	1.2	1.2	1.8	1.8
Analog	$I_{d,op}$	0.53	0.6	0.68	0.9

Table I The measurement conditions   unit: V
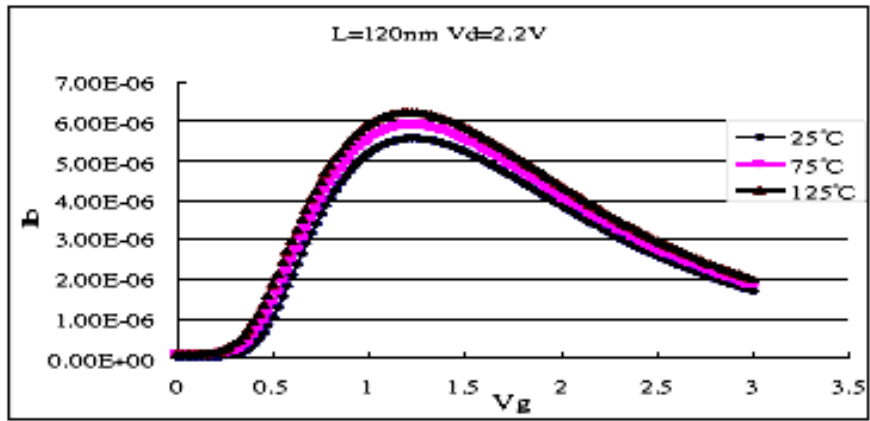
Fig. 1: Substrate current vs. gate voltage for *Vd* = 2.2V.
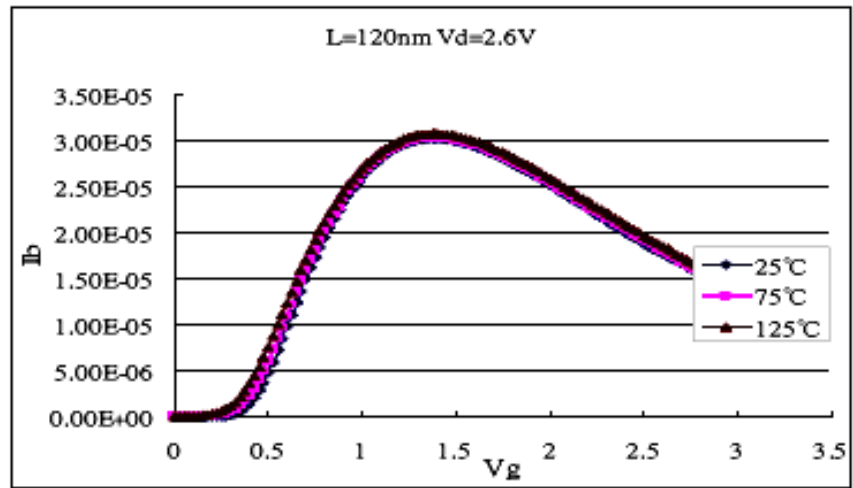
Fig. 2: Substrate current vs. gate voltage for *Vd* = 2.6V.
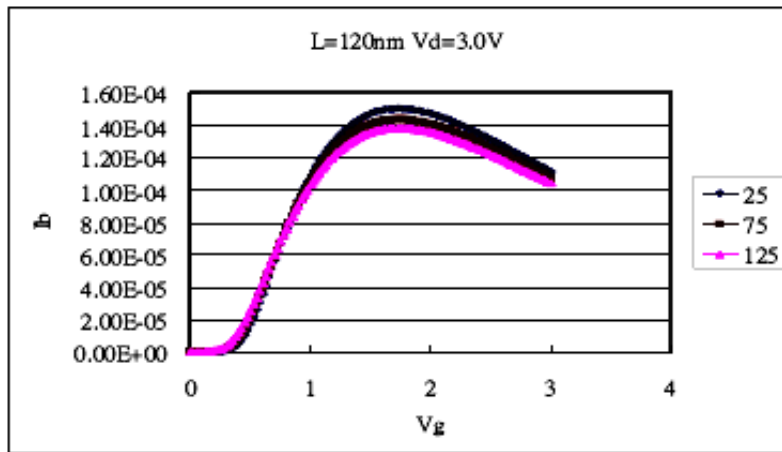
Fig. 3: Substrate current vs. gate voltage for $Vd = 3.0$V.
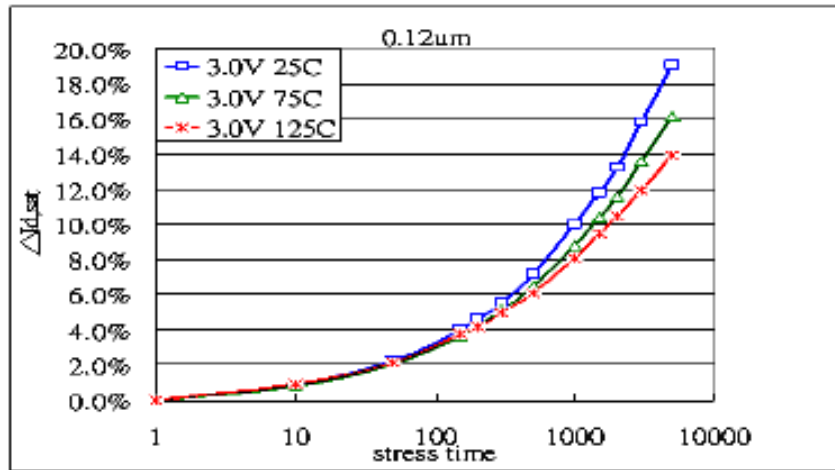
Fig. 4:   *Id,sat* versus stress time at *Vd* = 3.0 V with different

temperatures.
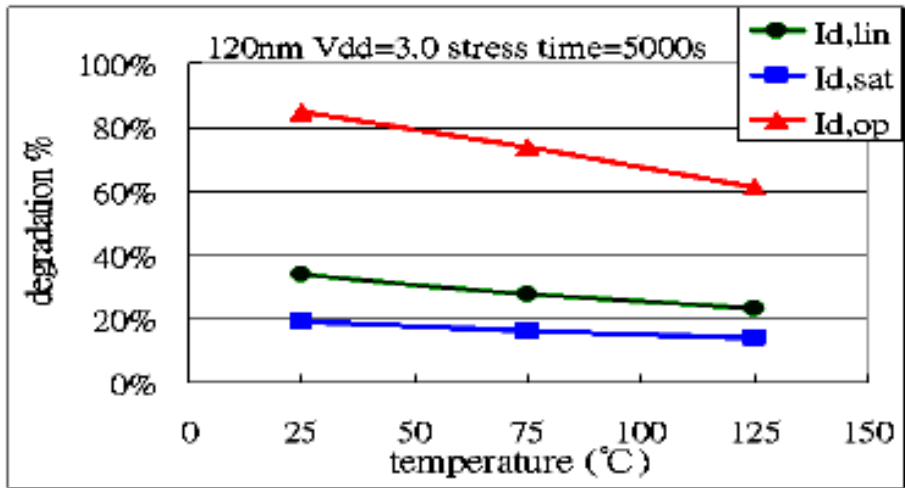
Fig. 5: Drain current versus temperature at *Vd* = 3.0 V after stress

5000 seconds.
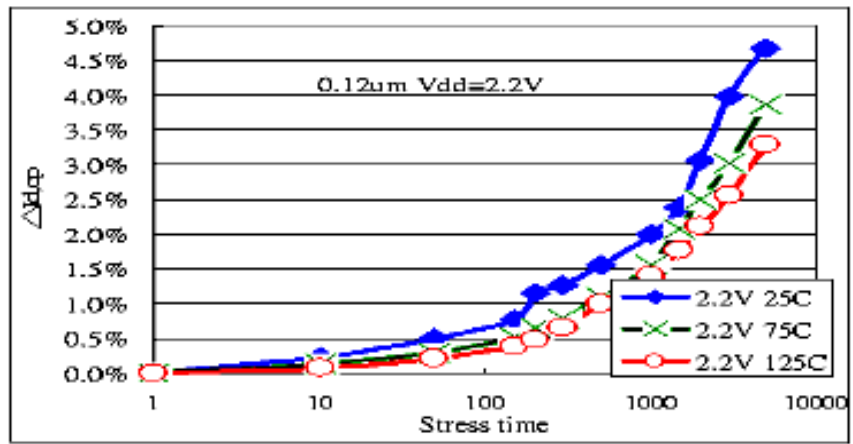
Fig. 6:   *Id,op* versus stress time at *Vd* = 2.2 V with different
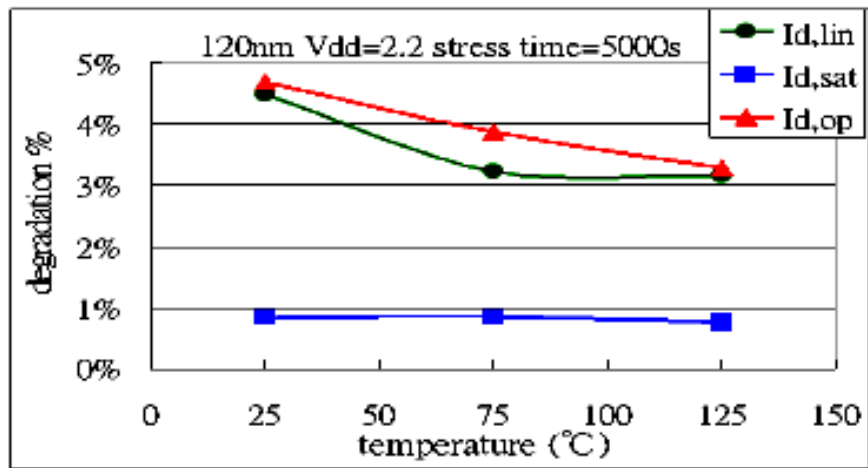
temperature.

Fig. 7: Drain current degradation versus temperature at *Vd* = 2.2 V

after stress 5000 seconds.
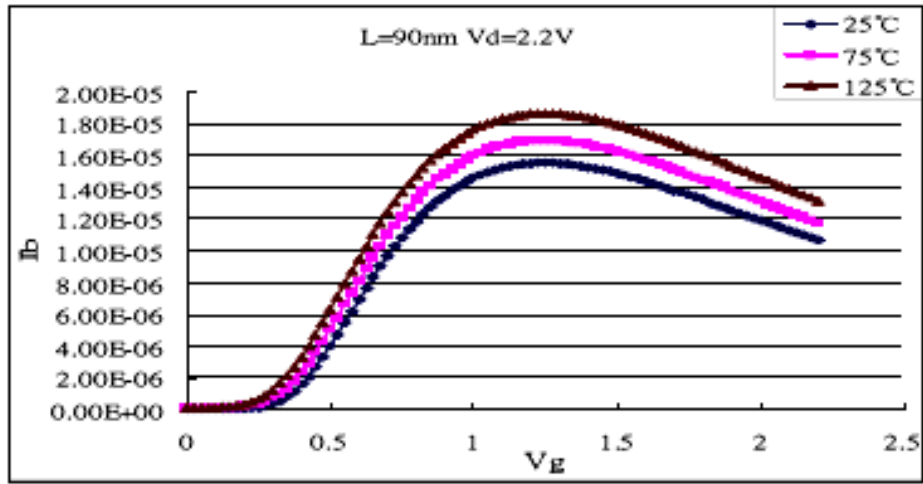
Fig. 8: Substrate current vs. gate voltage for *Vd* = 2.2 V.
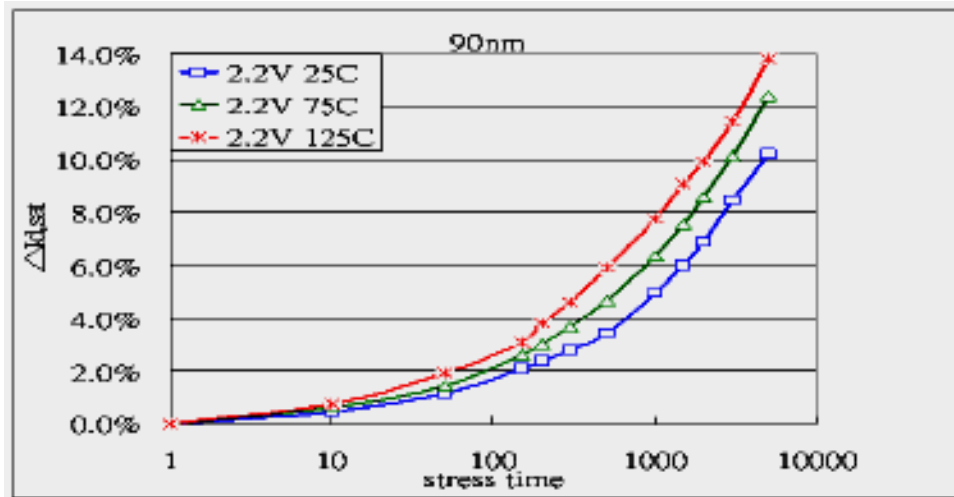
Fig. 9:   *Id,sat* versus stress time at *Vd* = 2.2 V with different
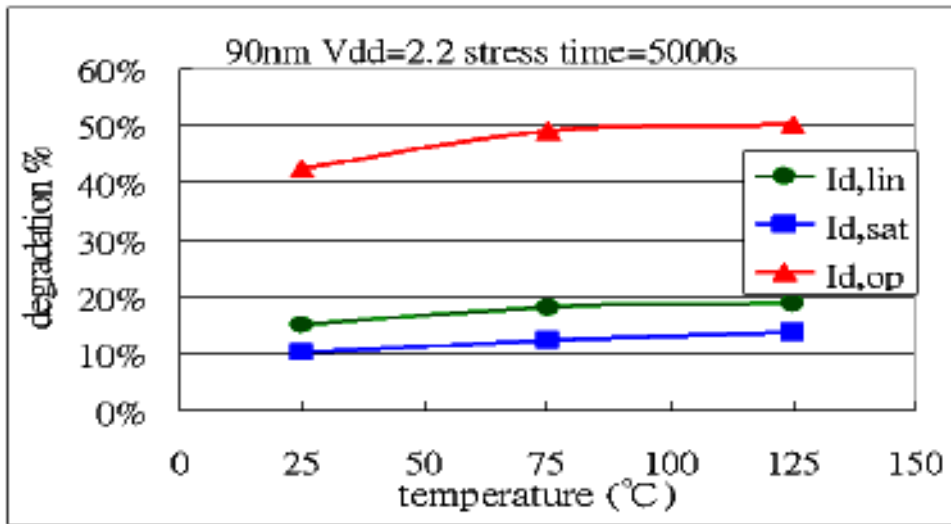
temperatures.

Fig. 10: Drain current degradation versus temperature at Vd = 2.2 V

after stress 5000 seconds.

Chapter 5

An Investigation on Hot Carrier Effect at Elevated Temperatures for pMOSFETs of 0.13 um Technology

5.1 Introduction

In the past few decades, the mechanism responsible for the hot carrier degradation in nMOSFET is believed to be the interface-state generation and the damage of gate oxide [1]. However, the situation for pMOSFET is less clear and had been long believed that hot carrier degradation of pMOSFETs is not so serious as nMOSFETs' for the following reason. The mean free path of holes in silicon is about one half that of the electron [2]; therefore, holes scatter more frequently and fewer of them can reach enough high energy (about 4 eV) to create interface states [3]. But recent studies showed that even the transistor channel length has been scaled down into the deep-submicron regime (and supply voltages have been reduced) hot carrier induced degradation of pMOSFET has surprisingly become larger and approaching that of nMOSFET [4].

As to the temperature effects, in hot carrier conventional degradation concepts, operation at low temperature is more severe than at high temperature. However, recently study reveals that, operation at high temperature, the degradation is more severe than at room temperature [5], and the mechanism is

relative to NBTI (Negative Bias Temperature Instability) effect [6].

In this research, we studied two devices with different biases and temperatures to verify the mechanism and temperature effect on pMOSFETs. We found that the hot carrier degradation of $I_{d,op}$ (defined based on analog application) is the worst in comparison with $I_{d,lin}$ and $I_{d,sat}$. This message should be important for designing analog circuits with satisfactory reliability. In addition, we found that the worst stress condition of 0.13μm technology and smaller is switched to the maximal gate voltage at high temperature.

5.2 Hot carrier of PMOSFETs and relative issues

5.2.1 PMOS Consideration

The carrier mobility of holes in silicon is about 470 cm^2/V-s, and the mean free path is about one halt that of the electrons, hence, holes scatter more frequently and fewer of them reach high enough energies to create interface states. However, as the channel length has been scaled down into nano regime, hot carrier induced degradation of pMOSFETs has been approaching of nMOSFETs. For this reason, the hot carrier reliability of pMOSFETs has been studied in more detail. Three hot carrier degradation mechanisms in pMOSFETs have been identified

[12][13]. The details will discuss in following section.

5.2.2 Mechanisms

There have been lots of studies [5][14-17] on electron traps mainly utilizing an avalanche injection method. Electron trapping near the drain region leads to a reduction in threshold voltage and to the effective channel shortening. As a result, pMOSFETs drive current, transconductance and $\triangle V_t$ increase. However, this mechanism is most important in longer channel pMOSFETs, and gate current I_G has been used as a predictor of the device lifetime [1]. As compared with electrons, holes are much less likely to be injected into an oxide, mainly due to the larger interfacial barrier height, however, once injected, they have much more influence on the MOSFET characteristics. It's commonly believed that hole trapping centers originate from excess silicon and strained Si-O bonds near the Si-SiO$_2$ interface [7]. According to the experimental result [18] that hole traps are more difficult to be recovered than electron traps.

Another mechanism is interface state generation; it's commonly believed to originate from silicon dangling bonds and oxygen dangling bonds, which are created by breaking originally inactive bonds. There are two kinds of mechanisms for interface state generation [7].

(1) The hydrogen model [14] suggests that a hydrogen-related center at the Si-SiO$_2$ interface captures an incident carrier. This breaks the $\equiv$Si-H or $\equiv$Si-O-H bond, allowing the hydrogen-containing species to escape [7].

The broken-bond model suggests that a strained Si-O or Si-Si bond is broken by capturing an incident carrier, especially a hole, leading to structural modifications.

5.3 Experimental Results and Discussion

For 90 nm devices, Fig. 1, 2 and 3 show the experimental results of $I_{d,lin}$, $I_{d,sat}$ and $I_{d,op}$ degradation versus stress time at different temperatures for stressed at $V_d =$ -2.0V. As expected in [5], the degradations are increased as temperature rise from 25 ℃ to 125 ℃.

Fig. 4 shows the degradation ratios of drain currents with different temperatures. Among three temperatures, 125 ℃ is the worst case for core devices. The degradation of $I_{d,op}$ at 125 ℃ is worse than $I_{d,lin}$ and $I_{d,sat}$, and for digital circuits, $I_{d,sat}$ is worse than $I_{d,lin}$.

For 120 nm devices, the stress bias is set at peak substrate current when $V_d =$ -3.2V. It is clear that Fig. 5, 6 and 7 show the $I_{d,lin}$, $I_{d,sat}$ and $I_{d,op}$ degradation versus stress time at different temperatures. It's showed that at room temperature reveal

64

more severe degradation than higher temperatures, which obey the historical theory.

Fig. 8 shows the degradation ratios of drain currents versus different temperatures. Comparing those results, the degradation of $I_{d,op}$ is still the largest among all temperature range. $I_{d,sat}$ is the worst case for digital circuit considerations. This result follows the conventional concept that high temperature results in phonon scattering, which then reduces the drain current and impact ionization.

For CHC stress method, the stress bias V_g is set at -3.2V, and obviously, in Fig. 9, 10 and 11 show the results of d $I_{d,lin}$, $I_{d,sat}$ and $I_{d,op}$ at 75℃ reveals more degradation than other temperatures. And the stress method of $V_g=V_d$, which causes more severe degradation rate more than $V_g=I_{b,max}$.

Fig. 12 shows the degradation ratios of drain currents versus different temperatures. Comparing those data, the degradation of $I_{d,op}$ is still the largest among all temperature range. And for digital circuit considerations, $I_{d,sat}$ is the worst case.

In order to find out the inside mechanism, $V_{t,lin}$ shift is plotted in log-log scale as in Fig. 13. All curves in the Fig. 13 exhibit rather parallel trend and obey the power law as

$$\Delta V_{t,lin} = At^{n} \qquad (4\text{-}1)$$

with $n \approx 0.26$ and A is a constant to be determine. We have examined the power law behaviors of $\triangle V_{\text{t,lin}}$ on DAHC and CHC stress modes for I/O devices and obtained exponent $n \approx 0.6$ and 0.4 in Fig. 14, 15 respectively. Because $n \approx 0.25$ is the typical trend of NBTI effect, we are then safe to say NBTI plus CHC would make the worst stress mode for small scale pMOSFET.

In addition, it is known that $\Delta V_{\text{t,lin}}$ only concerns with generated interface states' charges $q\Delta N_{it}$ and generated oxide trapped charges, $q\Delta N_{ot}$. But, if ΔN_{ot}' effect is negligible, we will have [7]

$$\Delta N_{it} \propto \Delta V_{t,lin} \propto I_{d,lin} \deg radation \tag{4-2}$$

Hence, as shown in Fig. 16, $I_{d,lin}$ degradation of core devices in log-log scale exhibits almost the same power law dependent and exponent $n \approx 0.26$. We can thus infer that generated oxide trapped charges must be minor in quantity and are negligible. The generated interface states are the dominant mechanism for all the degradation.

5.4 Conclusions

Through the measurement results and discussions in previous chapters, we have come to the conclusion summarized in the following sentences:

(1) For core devices, it's found that the stress method with $V_g = V_d$ is the worst case, and the hot carrier degradation of $I_{d,op}$, which based on analog operation condition, is the worst case at high temperature. For digital

consideration, $I_{d,sat}$ is worse than $I_{d,lin}$. We find temperature now has dominant effect on deciding the worst stress condition as the voltage did.

(2) For I/O devices, we also found that the stress method with $V_g = V_d$ is the worst case. On the contrary, the hot carrier degradation of $I_{d,op}$ is the worst case at room temperature.

(3) For the hot carrier mechanism, it is found that the worst case of HC induced degradation on pMOSFETs has switched from low temperature to high temperature and from DAHC stress mode to CHC mode. Additionally, the severity of degradation on pMOSFETs has become comparable to their nMOSFET counterparts. By analysis the measured I-V data and power law behaviors, the switching can be presumed by the integration of HC and negative bias temperature instability (NBTI) effects, in which the generation of interface states plays the major role in damaging the pMOSFETs devices.
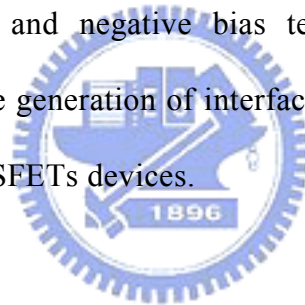
		L_{eff} = 90 nm		L_{eff} = 120 nm	
		V_g	V_d	V_g	V_d
Digital	$I_{d,lin}$	-1.2	-0.05	-1.8	-0.05
	$I_{d,sa}$	-1.2	-1.2	-1.8	-1.8
Analog	$I_{d,op}$	-0.53	-0.6	-0.68	-0.9

Table 1 The measurement conditions (unit: V)
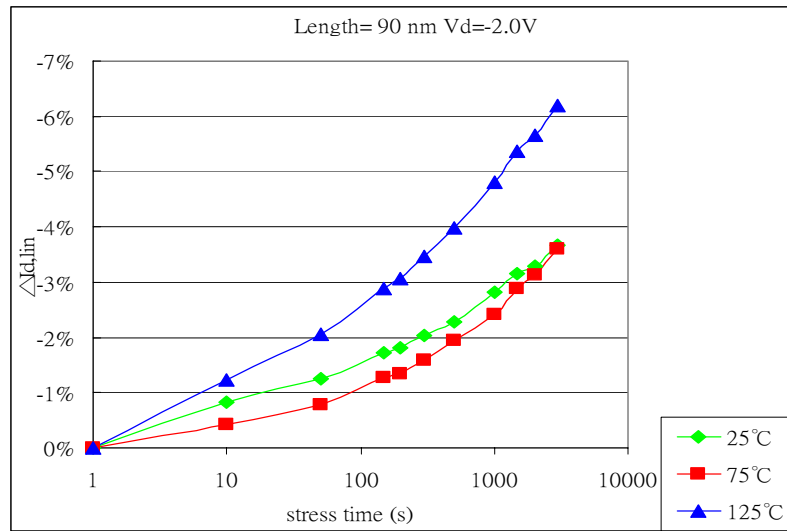
Fig 1. $I_{d,lin}$ versus stress time at V_d = -2.0 V at different temperatures.
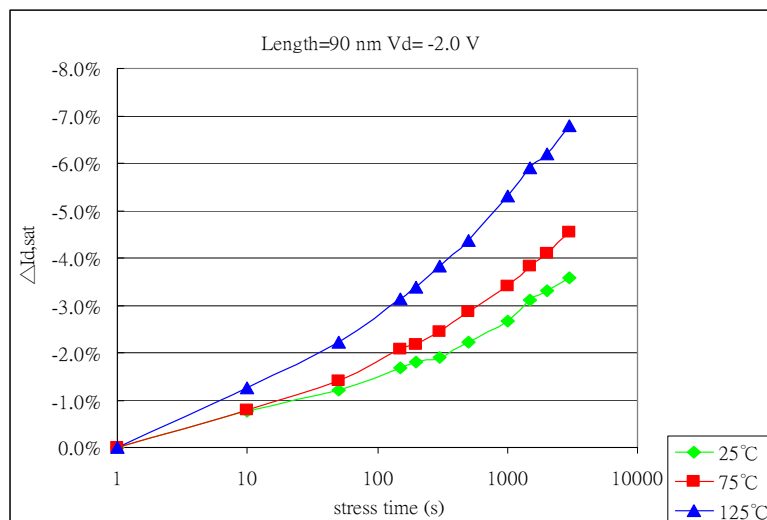
Fig. 2. $I_{d,sat}$ versus stress time at V_d = -2.0 V at different temperatures.
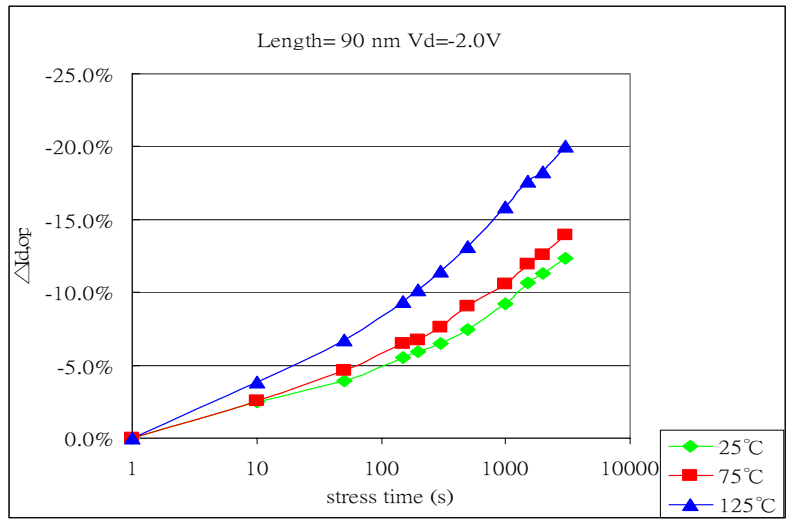
Fig. 3. $I_{d,op}$ versus stress time at V_d = -2.0 V at different temperatures.
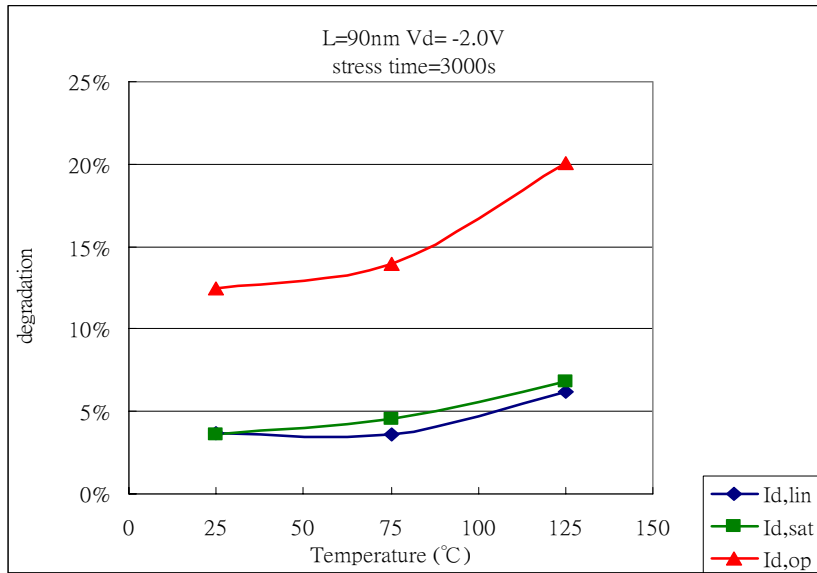
Fig. 4. Drain current degradation versus temperature at V_d = -2.0 V after stress 3000
seconds.
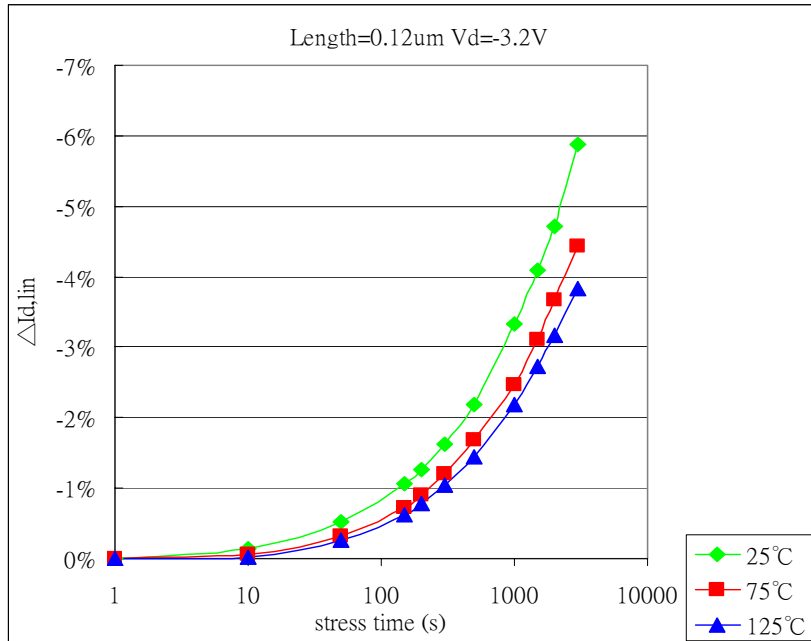
Fig. 5. $I_{d,lin}$ versus stress time at V_d = -3.2 V at different temperatures.
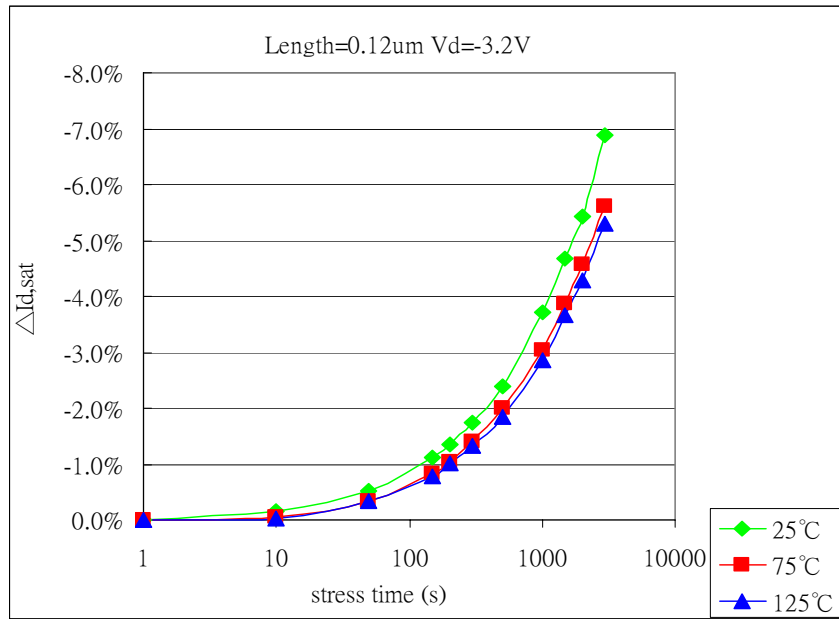
Fig. 6. $I_{d,sat}$ versus stress time at V_d = -3.2 V at different temperatures.
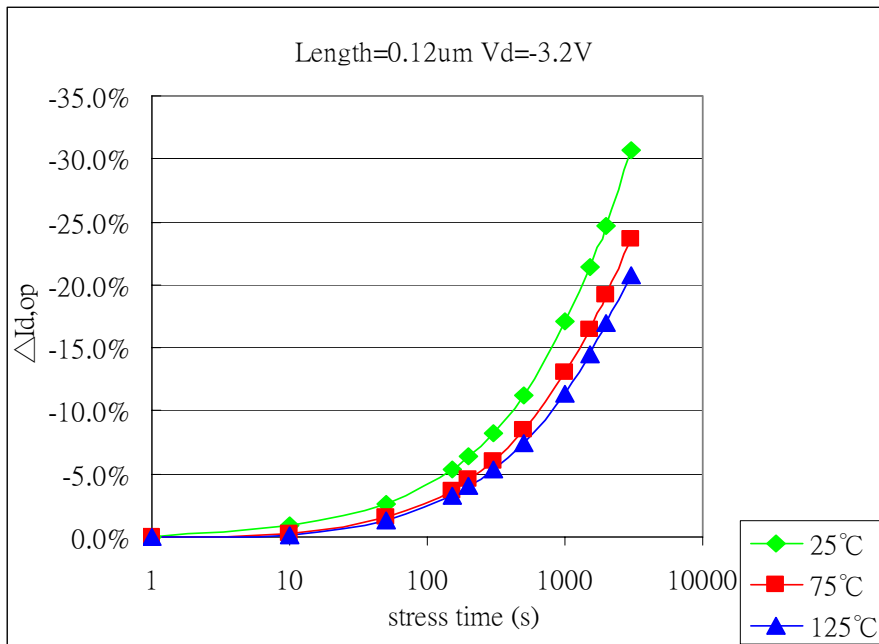
Fig. 7. $I_{d,op}$ versus stress time at V_d = -3.2V at different temperatures.
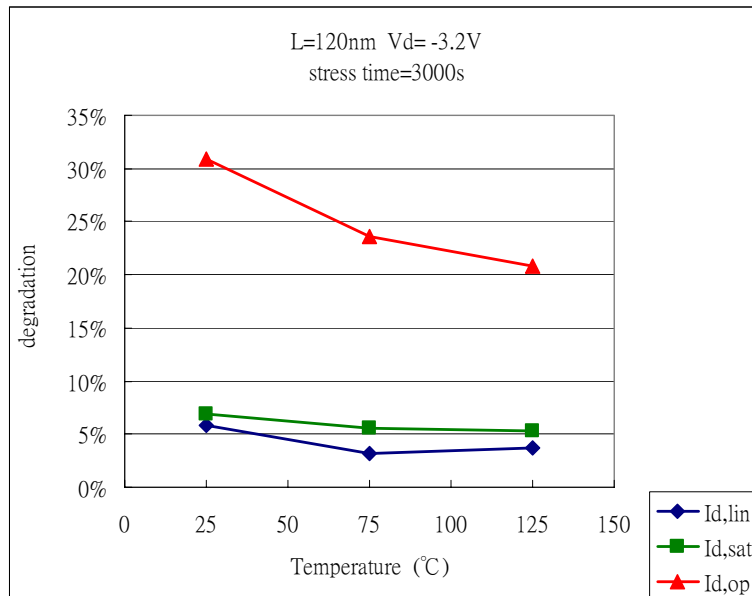
Fig. 8. Drain current degradation versus temperature at V_d = -3.2 V after stress 3000 seconds.
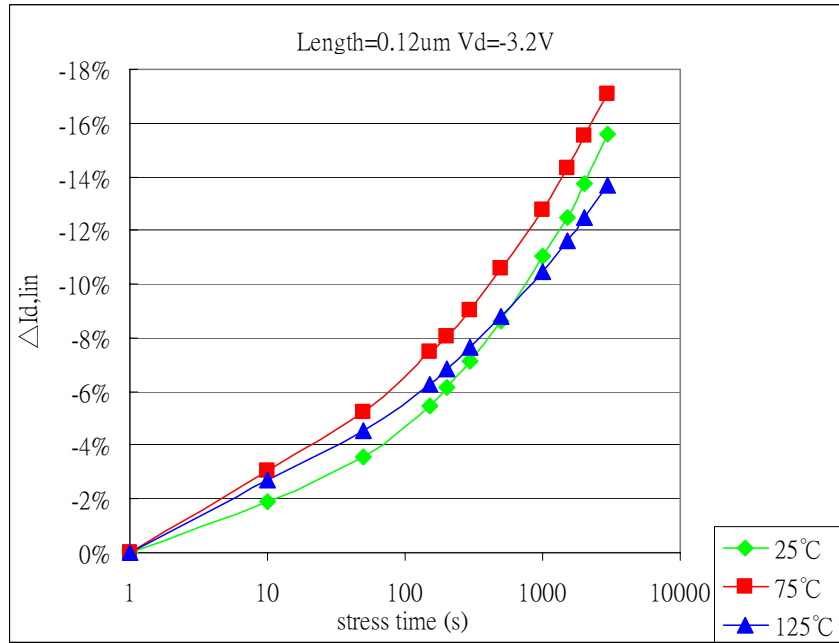
Fig. 9. $I_{d,lin}$ versus stress time at V_d = -3.2 V at different temperatures.
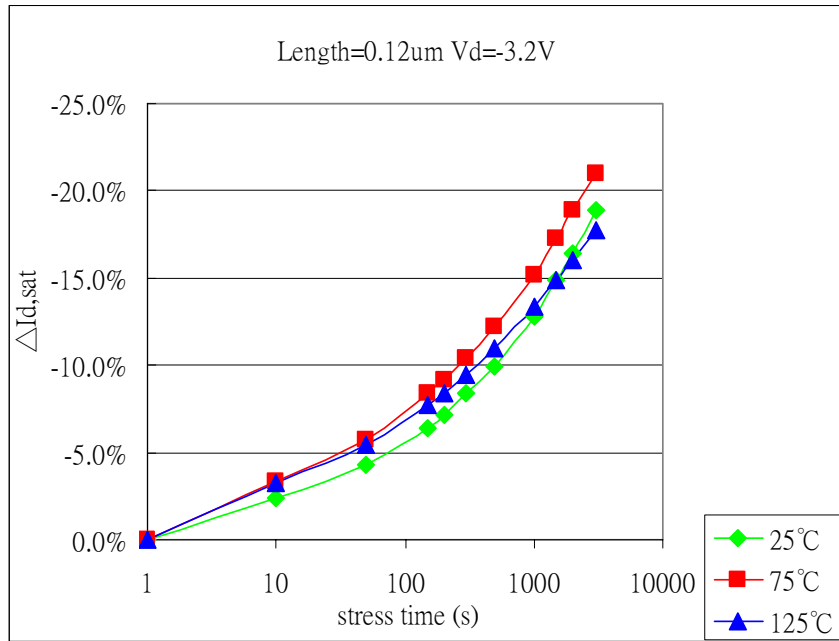
Fig. 10. $I_{d,sat}$ versus stress time at V_d = -3.2 V at different temperatures.
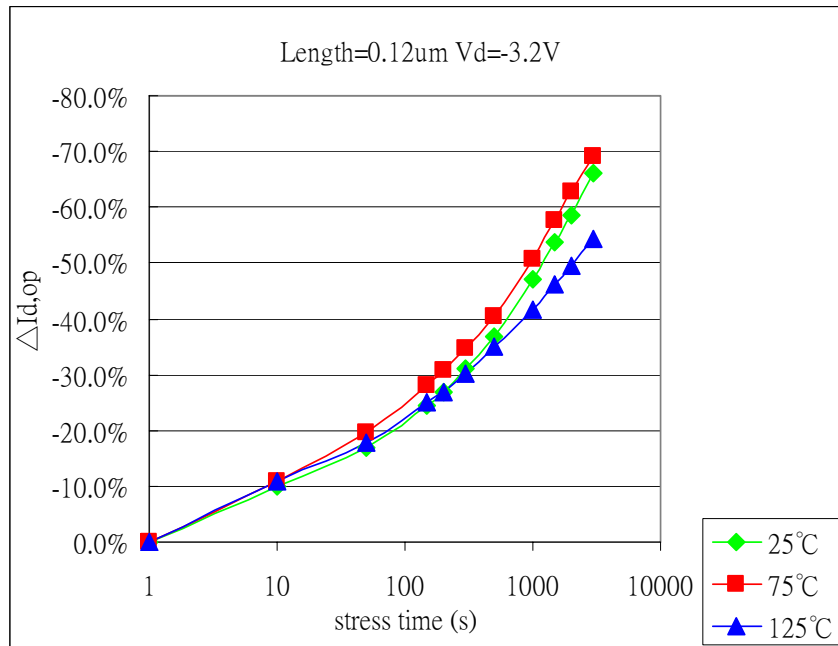
Fig. 11. $I_{d,op}$ versus stress time at V_d = -3.2 V at different temperatures.
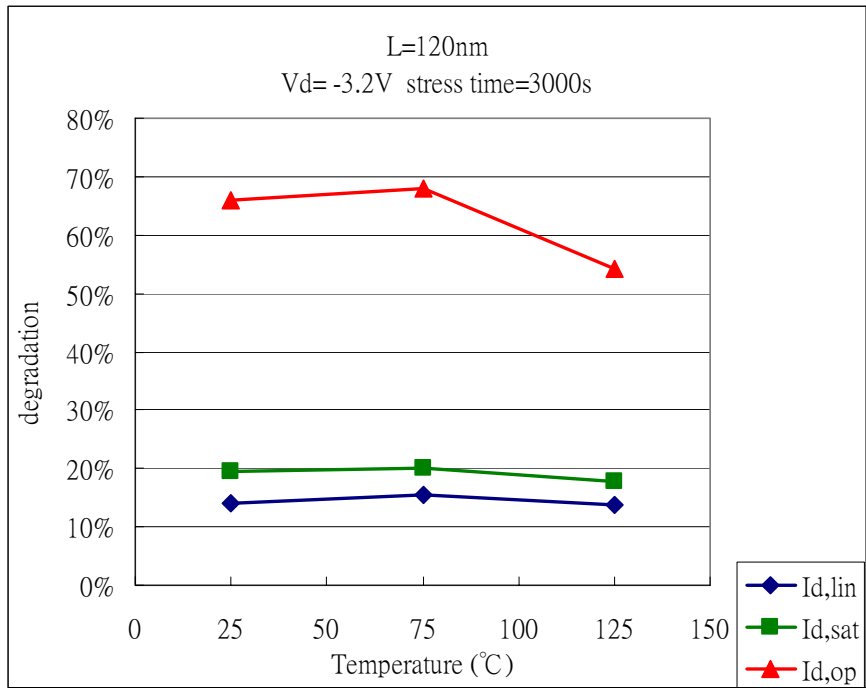
Fig. 12. Drain current versus temperature at V_d = -3.2V after stress 3000 seconds.
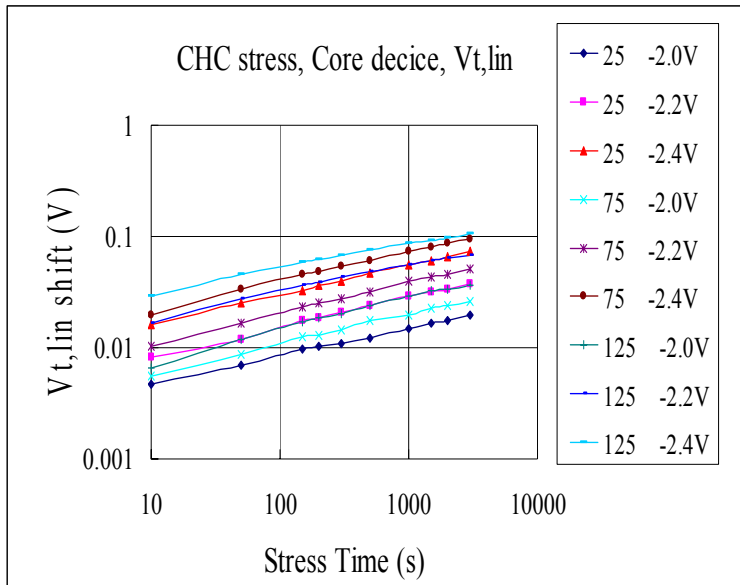
Fig. 13. $V_{t,lin}$ **shift of core devices versus stress time.**
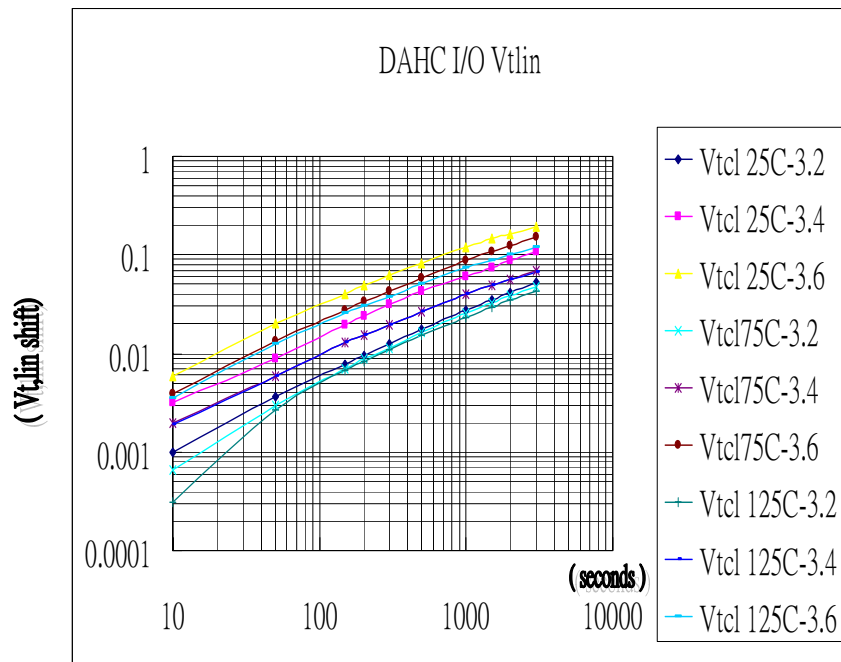
Fig. 14. $V_{t,lin}$ **shift of I/O devices (DAHC) versus stress time.**
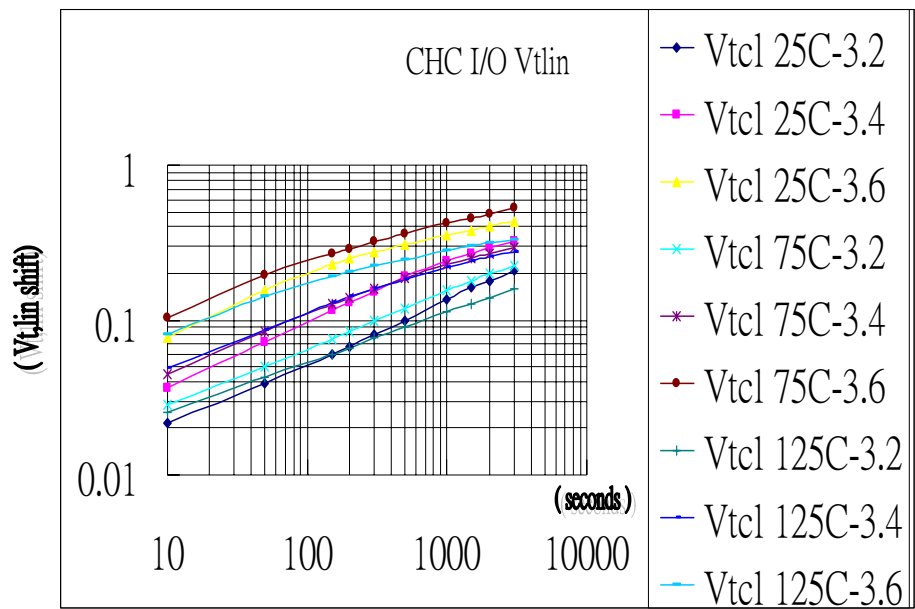
Fig. 15. $V_{t,lin}$ shift of I/O devices (CHC) versus stress time
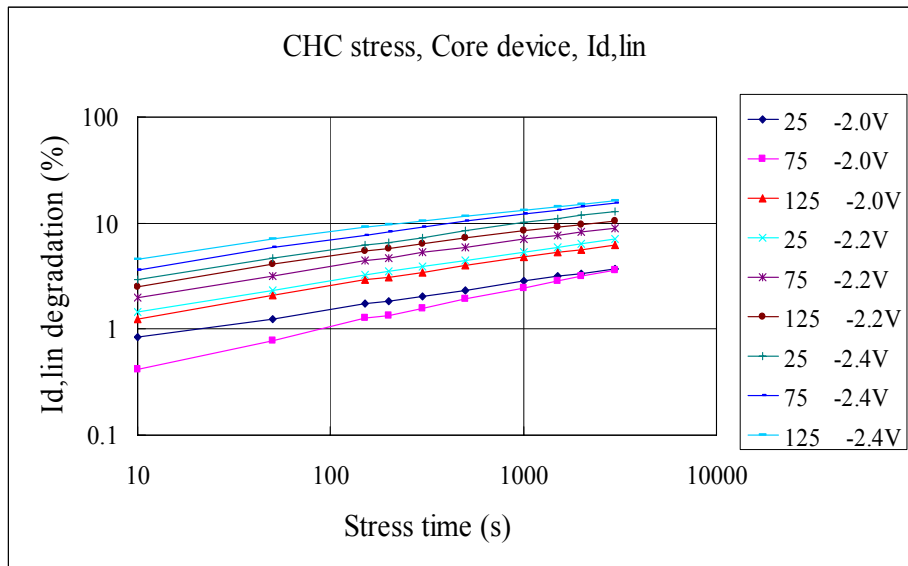
Fig. 16. I_d degradation of core devices versus stress time.

Chapter 6

Mismatches after Hot-Carrier Injection in Advanced Complementary Metal-Oxide-Semiconductor Technology Particularly for Analog Applications

6.1 Introduction

The mismatch properties of metal–oxide–semiconductor field-effect transistors (MOSFETs) on the same wafer are great concerns for both manufacturers and designers, particularly when the wafer is carrying analog circuits. The mismatches due to process variations are most commonly known [1][2][3]. Another popular factor being considered is the effects of size on parameters such as channel length, width, gate area, and layout type [2][3][4][5][6]. However, it is known that hot-carrier injection (HCI) in normal operation will degrade MOSFET performance, but the mismatches due to this effect have not been fully explored. In perhaps the sole example of a related study, the mismatches of the parameters β (current gain factor) and Vt (threshold voltage) due to HCI in nMOSFETs of one size were reported to monotonously increase with stress time [7]. It was concluded that the HC-induced transistor mismatches have a great impact on the reliability of analog circuits, such as those having mirrored transistors [7].

In this paper, we present the impact of hot carrier stress on the mismatch properties of n and p MOS transistors with different sizes produced using 0.15 u complementary MOS (CMOS) technology. The considerations particularly focus on the concerns of analog applications.

6.2 Experiments

Test devices, nMOSFET and pMOSFET pairs, were fabricated using a 0.15 um CMOS process. Source/drain and extension structures were formed by arsenic implantation for nMOSFETs and boron implantation for pMOSFETs. Devices in each pair are adjacent to each other with a gate oxide thickness of 2.6 nm and a minimum feature size of 0.15 um. In totally, 40 pairs of transistors having identical layout structures with W/L =1/0.15, 1/0.5, 5/0.15, and 5/0.5 um, half n and half p, on the same wafer were stressed to investigate the impact of HC on mismatch properties. HCI stressed at 25 ^{o}C and up to 5000 s was performed using the gate voltage Vg at maximal substrate current I$_{submax}$ while the drain was biased at 2.4 V, and the source and substrate were grounded. [Often this kind of stress condition is called drain avalanche hot carrier (DAHC).] After each stress period, analog threshold voltage Vt,op was measured at a drain-to-source voltage of Vds = 0.75V by the constant current method, and analog drain-to-source current Ids,op

was measured at Vg = Vt,op + 0.3V with Vds = 0.75V for all nMOSFETs; both

Vt,op and Ids,op were designed to simulate the operating conditions of analog

circuits, such as MOSFETs in small-signal amplifiers and class-A power

amplifiers. For pMOSFETs, the stress and measurement conditions were the same

except that Vds and Vg were negatively biased.

6.3 Results and Discussion

After some statistical arrangement of the tested data, the results are shown in

the following graphs and tables. Figures 1 and 2 show the standard deviations

of Vt,op and Ids,op/Ids,op for all the related pairs. Although it is a common

practice to express the mismatches in terms of 1= (gate area)^0.5 here the

distributions of the standard deviations are obviously not so uniform, to some

degree implicating the irregularity of the mismatch itself for deep submicron and

beyond devices. However, on the basis of their channel length and DAHC effect,

these can be interpreted as the following. For L = 0.15 um devices, 0.15 um is the

critical minimal length of this technology, so they should reveal larger standard

deviations than L = 0.5 um devices. This should also be the reason why, even for

the before-stress case, the shorter-channel-length devices exhibit higher levels of

standard deviation than their counterparts. In addition, because the DAHC effect is

proportional to the substrate current, which means that it is also proportional to drain current and to the reciprocal of channel length [8], the longer-channel-length devices showing much less variations in standard deviation after stressing seem reasonable. Even so, the slopes of these lines, called area factors (or area proportionality constants) [3][4] of corresponding properties as defined in eq. (1), mostly have the same trends in spite of their differences in channel length or differences before/after applying stress.

$$A_{\text{property}} = \frac{\sigma(\Delta_{\text{property}})}{1/\sqrt{WL}} \qquad (1)$$

As stated in the above interpretation, since the shorter-channel devices are more critical and more degraded due to DAHC, we shall focus our attention on the L = 0.15 um devices from now on. From Figs. 1 and 2, one can observe that, for nMOSFETs, the standard deviations of Vt,op and ΔIds,op/Ids,op are enlarged after stress, which means that the mismatches of all transistor pairs are worse after HCI. However, in the case of pMOSFETs, the changes are much smaller, although they possess higher degrees of mismatch initially. The reason for initial mismatches should be the contributions of irregular boron penetration, and the reason for small changes after stressing should result from the small hot carrier effect due to the holes in the p channel being hard to accelerate to generate

massive impact ionization. The latter is consistent with test data because we recorded Isubmax values of pMOSFETs that were almost two orders of magnitude smaller than those of nMOSFETs, and the ratios of Isubmax/Ids are about 20 times smaller for the same DAHC biases and sizes.

A hint that may be valuable to an analog circuit designer is the after-stress lines of n and pMOSFETs exhibit a cross point in the $V_{t,op}$ figure, which means that the $V_{t,op}$ mismatches are the same for the same gate area. It is suggested that the cross point can be used to indicate the minimal size at which n and p pairs will have the same or smaller degree of $V_{t,op}$ mismatch in designing analog circuits such as when a push–pull amplifier is involved. For the present case, the minimal gate area should be 0.18 um^2 (implying that the minimal width should be 1.22 um at this critical short channel length) at about $\sigma(\Delta V_{t,opT}) = 10$ mV. For $\Delta I_{ds,op}/I_{ds,op}$, it is difficult to find a cross point in Fig. 2, but the methodology can still apply for other processes if $I_{ds,op}$ mismatch is to be considered first.

The mismatch characteristics of the area factors of n and pMOS transistors at L = 0.15 um are summarized in Table I. All the positive area factors in Table I reveal that the smaller the gate area WL is, the larger the mismatch will be. One would also observe again that the mismatches of nMOSFETs are obviously degraded after HCI, whereas the mismatch changes are minor and even better for

pMOSFETs. The table provides conveniences for designer to forecast the mismatches of different sizes and can be used to compare with other factors also causing mismatches. More details will be given in the following paragraphs.

For nMOSFETs, Figs. 3 and 4 can help explain the fact that the difference in local damage is increased with stress time due to random variations in the number and spatial distribution of electron traps formed near the drain region. Because of this, the mismatch parameters are inclined toward becoming worse. The means of the threshold voltage shifts and drain current degradation ratios of stressed transistors at each size increase with stress time due to increasing electron trap density. Another observation is that the σ and means of the after-stress Ids,op of nMOSFETs become significantly higher than the values before stress. The σ enlargement of Ids,op also outweighs the changes in Vt,op. This is because the Ids variance is dominated by two factors, the variance in ΔVt and the variance of Δβ (change in current gain factor). However, Δβ is directly dependent on Δμ [3][9][10] (change in mobility). Hence, we can conclude that the mobility mismatch of nMOSFETs is greatly degraded after HCI.

For pMOSFETs, from Figs. 5 and 6, the means of threshold voltage shifts and drain current degradation ratios over stress time are random and more than an order of magnitude smaller than those of nMOSFETs. The means of Vt,op switch

back and forth across the zero line particularly before the stress time reaches about

500 s. This indicates that not only holes but also electrons surmount the oxide

barrier to become trapped at the silicon–oxide interface and maybe into the oxide

near the drain region, and the holes and electrons compensate or compete with

each other on their influences on the change in $V_{t,op}$. Specifically, it is

presumable that the electrons are trapped inside the oxide, but the holes are

trapped at the $Si–SiO_2$ interface to damage the channel mobility. Thus, even

though $V_{t,op}$ zigzags around the zero line, $I_{ds,op}$ does not reveal any enhancement

but only continues its degradation. For the stress time after 500 s, it is also

presumable that the holes trapped at the interface become dominant and both $V_{t,op}$

and $I_{ds,op}$ degrade rapidly. Actually, the above findings and inferences agree well

with the pMOSFET HC mechanisms proposed by Woltjer[11] and later proved by

Polishchuk.[12]

An exception about the mismatches of drain saturated current $I_{ds,sat}$ is

worthy to disclose. Whereas the $I_{ds,op}$ of nMOSFETs exhibits a clear mismatch

degradation, the $I_{ds,sat}$ portion is small and random as shown in Fig. 7. At the

same time, the means of $I_{ds,sat}$ degradation ratios are apparently lower than the

means of $I_{ds,op}$ degradation ratios in Fig. 4. Figure 8 shows the same situation of

pMOSFETs as that in nMOSFETs. The above phenomena may be due to the

velocity saturation length of MOSFETs covering parts of the HC-damaged region. This kind of mechanism has been used to interpret the anomalous HC degradation of nMOSFETs at elevated temperatures.[13] Figure 9 shows a schematic drawing depicting such a concept. Since velocity saturation length L increases as long as the MOSFETs are operated at Vd > Vd,sat and the saturated velocity is not liable to be influenced by the interface states and oxide-trapped charges, the Ids,sat mismatches after HC stress being considerably less degraded than the Ids,op of n and pMOSFETs seems reasonable.

6.4 Conclusions

For the first time, we thoroughly present the impact of hot carrier stress on the mismatches of the analog properties of n and p MOS transistors with different sizes produced using 0.15 um CMOS technology. Comparing the mismatched standard deviations with the means of the HC effect in each of Figs. 3–8, one would not find it difficult to conclude that the HCI does degrade the matching properties of MOSFETs. The degrees of degradation closely depend on the strength of the HC effect. Therefore, under the stress condition of DAHC, the mismatch degradation in nMOSFETs is more serious than in pMOSFETs.

It is also suggested that plotting the mismatches of stressed n and pMOSFETs

together may reveal cross points such as in Fig. 1. The cross points can be used to indicate the minimal size at which n and p pairs will have the same degree of mismatches in the design phase, such that circuit performance can be more reliable.

Finally, the mismatch changes in $V_{t,op}$ are believed to be due to the random variations in the number and spatial distribution of trapped charges at the silicon–oxide interface and inside the oxide. In addition to the threshold voltage shift factor, the reasons of mismatch changes in $I_{ds,op}$ need to add the effect of charges at the interface, which induce the degradation of mobility through the scattering effect and aggravate the $I_{ds,op}$ mismatches. However, because some of the interface charges are covered by the velocity saturation length and make them ineffective, the mismatches of $I_{ds,sat}$ are obviously smaller than those of $I_{ds,op}$.

Table I. Summarized mismatch characteristics of n and pMOSFETs.

Conditions	$A_{Vt,op}$ (mV·μm)	$A_{Ids,op}$ (%·μm)	Device sizes
nMOS before stress	1.4	1.06	(um/um)
nMOS after HCI stress	2.6	2.05	$W/L =$
pMOS before stress	3.8	2.58	1/0.15,
pMOS after HCI stress	3.3	1.87	5/0.15
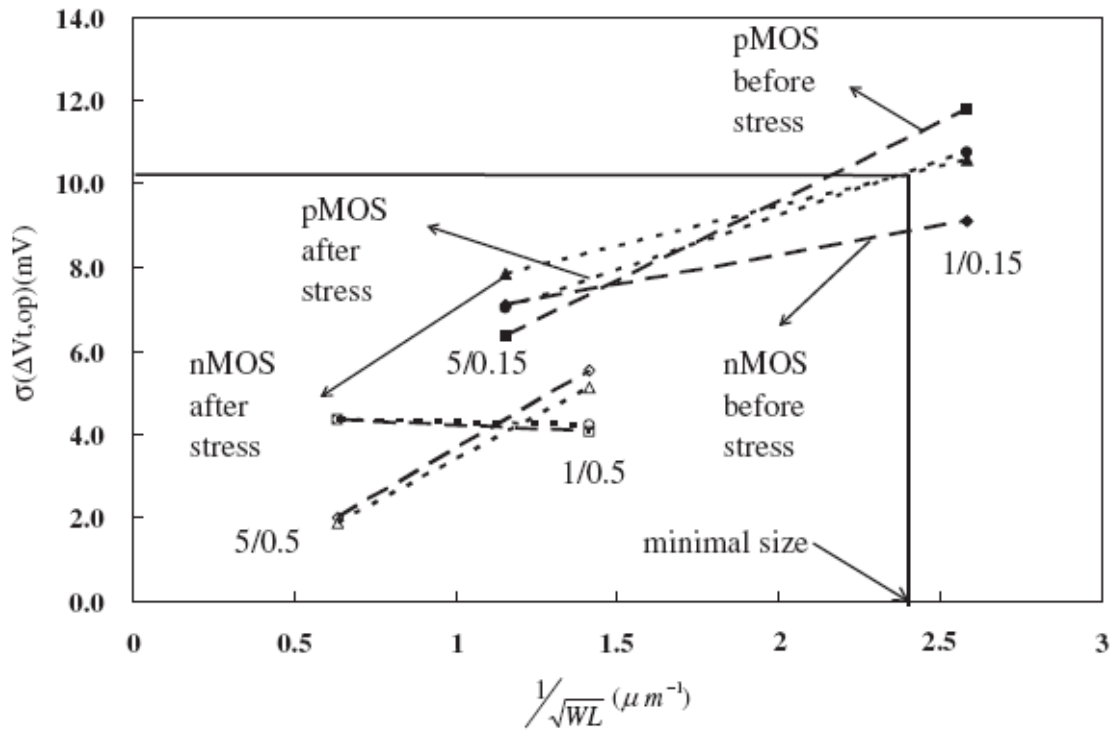
Fig. 1 Vt,op mismatches vs 1/(W*L)^0.5 gate area. Channel length/width and before or after stress of the tested data are indicated. The cross point of n and p MOS after-stress lines indicate the minimal size at which devices with a 0.15 um channel length will have the same or smaller mismatches.
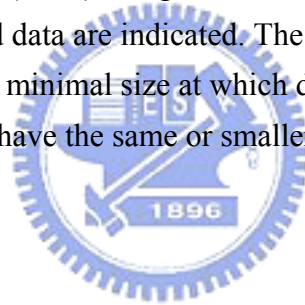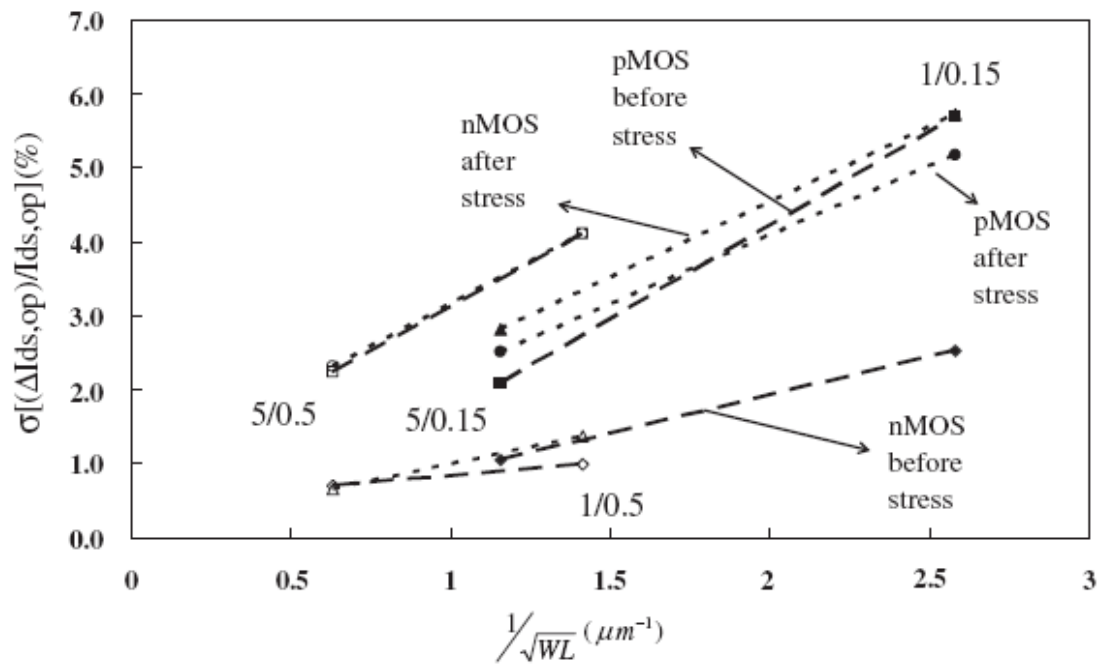
Fig. 2 Ids,op mismatches vs 1/(W*L)^0.5. The notation is the same as in Fig. 1. Note that the σ values of nMOSFET pairs particularly on L = 0.15 um devices are much more aggravated than those of pMOSFET pairs after stress although they possess higher degrees of mismatch initially.
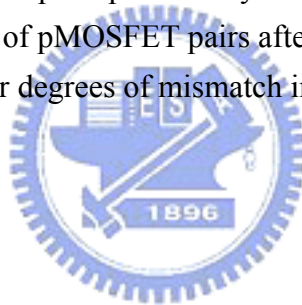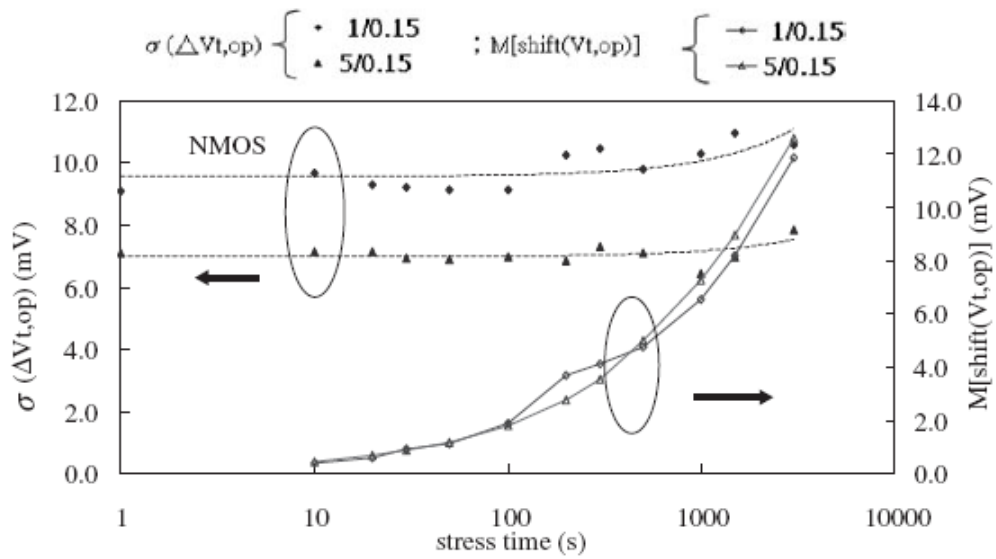
Fig. 3 Time history of mismatches of $\Delta Vt,op$ of each transistor pair and means of Vt,op shifts of tested nMOSFETs. The mismatches and particularly the means of Vt,op shifts increase with stress time for nMOSFETs of L = 0.15 um. The data at t = 1 s corresponds to the mismatch before HCI stress. This is also applicable for Figs. 4 to 8.
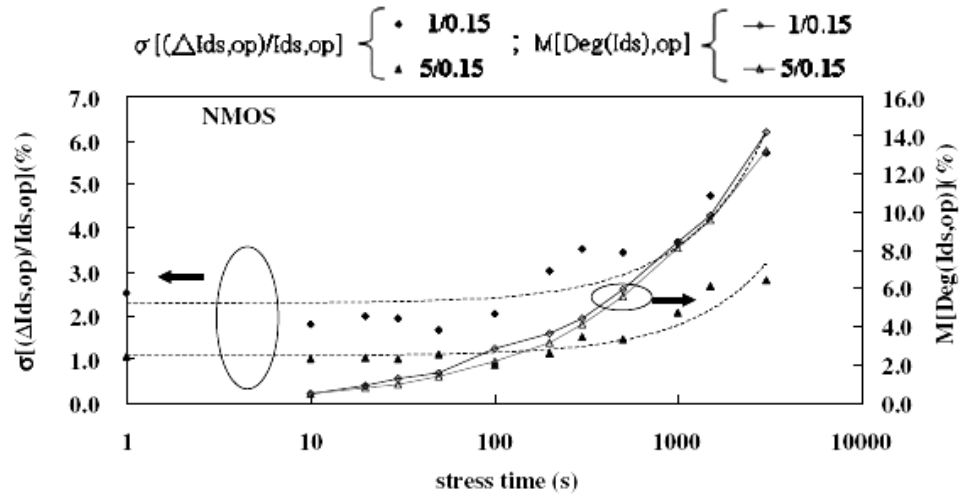
Fig. 4. Time history of mismatches of ΔIds,op/Ids,op of each transistor pair and means of Ids,op degradation ratios of tested nMOSFETs. The mismatches and the means of Ids,op degradation ratios increase with stress time for nMOSFETs of L = 0.15 um.
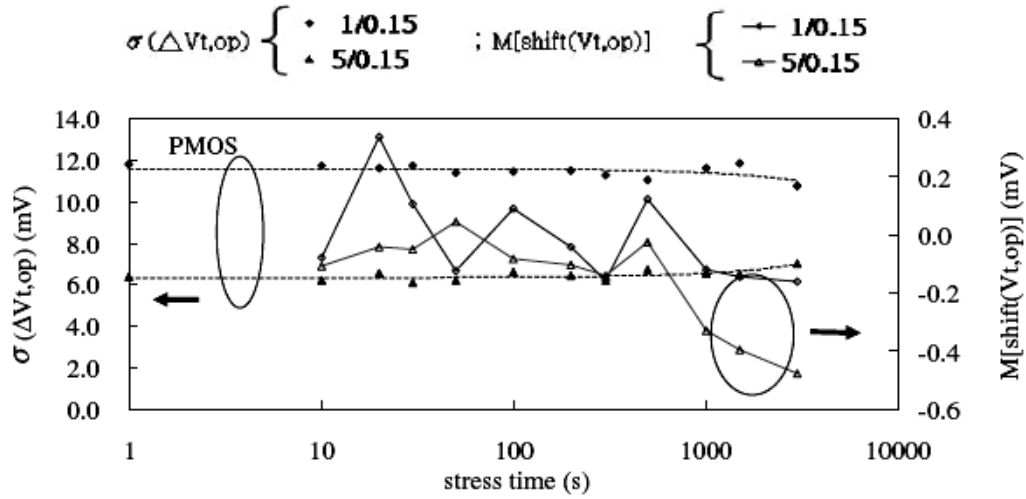
Fig. 5 Time history of mismatches of ΔVt,op of each transistor pair and means of Vt,op shifts of tested pMOSFETs. The Vt,op mismatches due to HC show different trends for different sizes, and the means of Vt,op shifts abnormally switch back and forth across the zero line and are smaller compared with those of nMOSFETs.
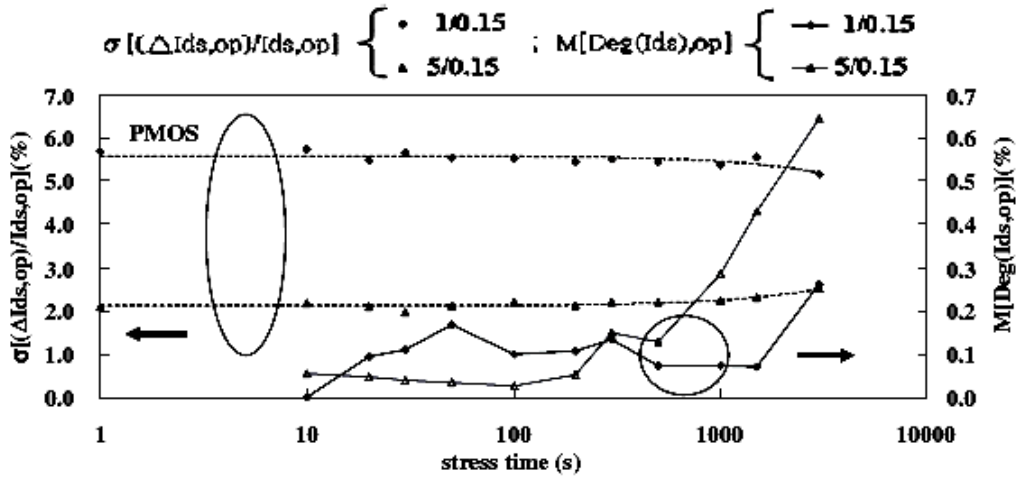
Fig. 6 Time history of mismatches of ΔIds,op/Ids,op of each transistor pair and means of Ids,op degradation ratios of tested pMOSFETs. The Ids,op mismatches due to HC show different trends for different sizes, and the means of Ids,op shifts are smaller compared with those of nMOSFETs.
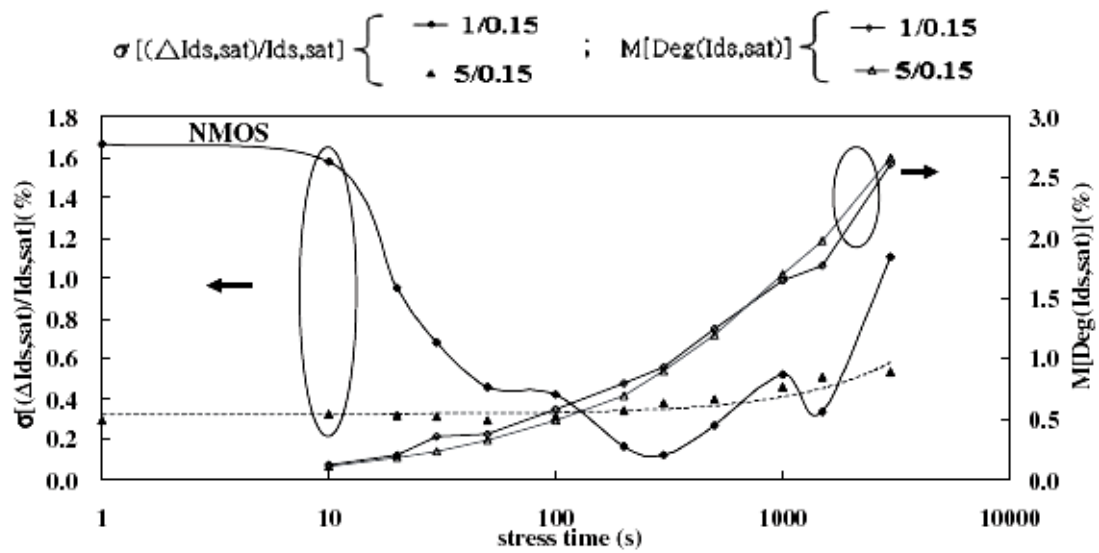
Fig. 7 Time history of mismatches of ∆Ids,sat/Ids,sat of each transistor pair and means of Ids,sat degradation ratios of tested nMOSFETs. The variations of mismatches and the means of Ids,sat degradation ratios are smaller than those of Ids,op in Fig. 4.
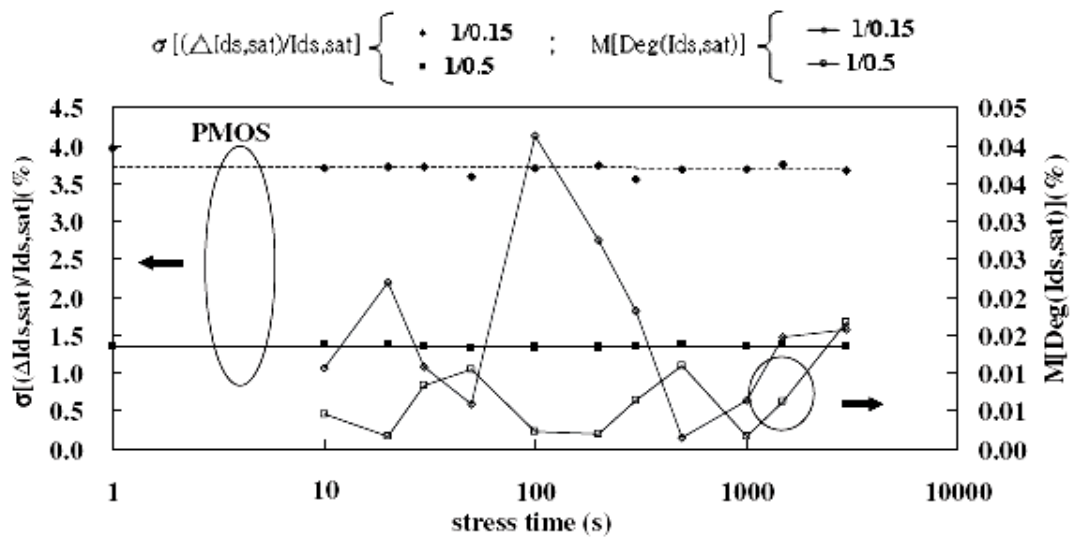
Fig. 8 Time history of mismatches of ΔIds,sat/Ids,sat of each transistor pair and means of Ids,sat degradation ratios of tested pMOSFETs. The variations of mismatches and the means of Ids,sat degradation ratios are smaller than those of Ids,op in Fig. 6.
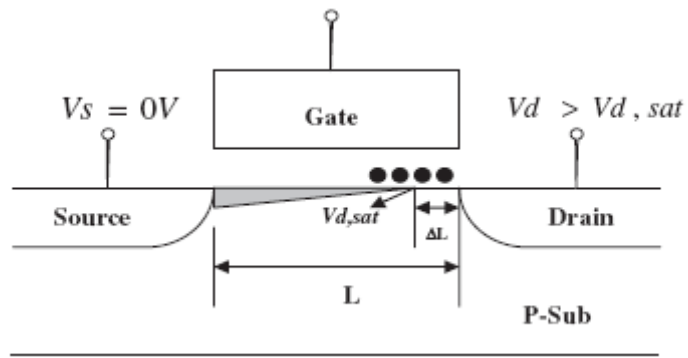
Fig.9 Schematic illustration showing that velocity saturation length ΔL will cover portion of local damage region.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

First of all, the post-thermal annealing effect impact on the reliability of 0.1 um CMOSFETs was inspected. For In halo nMOSFETs as well as As-halo pMOSFETs, device characteristics and hot-carrier-induced device degradation can be improved by post annealing particularly at medium temperatures with long time annealing without degrading the device performance.

Secondary, an investigation on hot carrier effect at elevated temperatures for n/pMOSFETs summarized in the following sentences:

1. The hot carrier injection does degrade the pMOSFETs properties due to holes trapped at Si-SiO$_2$ interface near drain region.

2. For core devices, it's found that the stress method with $V_g=V_d$ is the worst case, and the hot carrier degradation of $I_{d,op}$, which based on analog operation condition, is the worst case at high temperature. For digital consideration, $I_{d,sat}$ is worse than $I_{d,lin}$. We find temperature now has dominant effect on deciding the worst stress condition as the voltage did.

3. For I/O devices, we also found that the stress method with $V_g=V_d$ is the

worst case. On the contrary, the hot carrier degradation of $I_{d,op}$ is the worst

case at room temperature.

For the hot carrier mechanism, it is found that the worst case of HC induced

degradation on pMOSFETs has switched from low temperature to high temperature

and from DAHC stress mode to CHC mode. Additionally, the severity of degradation

on pMOSFETs has become comparable to their nMOSFET counterparts. By analysis

the measured I-V data and power law behaviors, the switching can be presumed by

the integration of HC and negative bias temperature instability (NBTI) effects, in

which the generation of interface states plays the major role in damaging the

pMOSFETs devices.
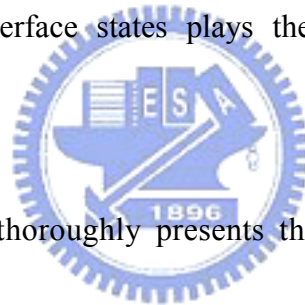
For the first time, we thoroughly presents the hot carrier stress impact on

mismatch properties of n and p MOS transistors with different sizes produced

using 0.15 μ m CMOS technology for analog applications. The hot carrier

injection does degrade matching of nMOSFETs' properties. For pMOSFETs, the

changes are minor. It is also found that the mismatch plots of n and pMOSFETs

after stress reveal cross points. The cross points can be used to indicate the

minimal size for n and p pairs to have the same degree of mismatches in design

phase, such that the circuit performance can be more reliable. Based on these cross

points, it is proposed that the minimal gate area should be 0.25 μ m2 at

($\Delta Vt,op$) = 8.4 mV when Vt mismatch is the first priority. Likewise, the minimal

gate area should be about 0.18μ m2 at $[(\Delta Ids,op)/Ids,op]$ = 5% if Ids

mismatch is to be firstly considered.

7.2 Future Work

After this research, the following researchers may keep on discussing other

analog parameters such as high-speed analog circuits, power dissipation analysis, cut

off frequency (f_T), gm/Id, linearity, noise, logic delay, NBTI, PBTI and analog

reliability. However, some of those issues may trade-offs for mixed mode application.

How to make your choice is important for device designers. Maybe one day, it is

possible to create a standard mixed mode process.
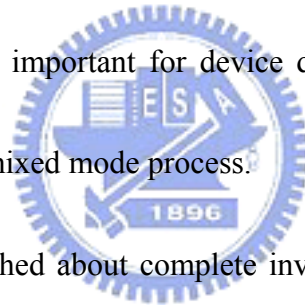
The work has been finished about complete investigation on the HC effects of

0.13μm technology. The characterization skills of charge pumping and gated diode

techniques could also be used to do more accuracy analysis for quantity of the charge

and postition. The following researchers will focus on this issue such that more

accurate analysis can be performed. To keep the pace with the advance of technology,

HCI on 65nm node or smaller should be an interesting issue. Another important

reliability factor-NBTI should also take care in the future.

So for matching degradation behavior, here it was only showed the impact after HCI stress, there still many failure mechanisms from the device reliability viewpoint. It will be more and more important in the industry today for device designers and circuit designers. Since different products or processes have different concerns, for example, analog circuit in DRAM will use the buried channel device, the NBTI will not be a critical reliability limitation on device design. But for the next product stage for DDR-III , the PMOS will be surface channel device. Therefore in that time, such mismatching degradation will be an import topic for designers. Thus, there is room for further investigation on those points. We fall into three categories as follows:

1. Matching performance should be considered under PBTI stress for nMOSFETs and NBTI stress for pMOSFETs.

2. Matching performance of different layout structures should be considered under the same stress case (HCI, PBTI, and NBTI).

3. Matching performance of different process steps or technologies also should be considered under the same stress case (HCI, PBTI, and NBTI).

CMOS device is one of the candidates chosen to serve for the next generation of wireless communications, especially for the upcoming system-on-a-chip (SoC) design in which RF subsystem, mixed-mode subsystem, and digital subsystem will be

implemented on the same chip. To achieve a better performance of the analog

subsystem with current process major for the digital logic circuit, it is still a lot of

works needed to do.

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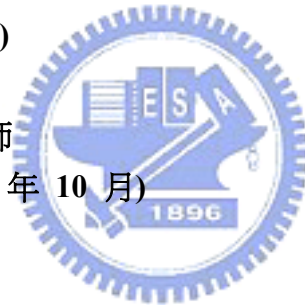
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論文題目：

元件可靠度的改善及類比電路應用時之影響

(Reliability investigation for process improvement and on analog circuit application)