A Complete Model of the *I–V* Characteristics for Narrow-Gate MOSFET's

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Abstract—**This paper provides a unified and process-independent MOSFET model for accurate prediction of the *I–V* characteristics and the threshold voltages of narrow-gate MOSFET's. It was developed based on several enhancements of the SPICE2 LEVEL3 MOS model and our previous subthreshold *I–V* model. The expressions achieved for the drain current hold in the subthreshold, transition, and strong inversion regions. In the strong inversion region, five parameters are used in the *I–V* formulation, while in the subthreshold region, two parameters are used. A continuous model in the transition region is proposed using a new scheme that will ensure that both the current and conductance are continuous and will not cause convergence problems for circuit simulation applications. All of the modeled parameters are taken from experimentally measured *I–V* characteristics and preserve physical meaning. A new and simple threshold voltage model of narrow-gate MOSFET's with implanted channel is also successfully developed. Comparisons between the measured and modeled *I–V* characteristics show excellent agreement for a wide range of channel widths and biases. The developed model is well suited for circuit simulation in SPICE.**

NOMENCLATURE

a	Body effect charge sharing factor.
α	Fitting parameter.
β	Mobility degradation factor in the width direction.
C_{ox}	Oxide capacitance per unit area.
C'_{ox}	Oxide capacitance per unit length.
ΔL	Channel length reduction.
ΔV_T	Threshold voltage shift.
δ	Fitting parameter of the narrow-gate effect for SPICE2 LEVEL3.
δw	Bird's beak length on one side.
ΔW	Channel width reduction due to the bird's beak and field-implant encroachment.
ϵ_{si}	Dielectric constant of silicon.
I_D	Drain current (in amperes).
$I_{D,S}$	Drain current (drift component) in strong inversion.
$I_{D,W}$	Drain current (diffusion component) in the subthreshold region.
I_{ON}	Constant current in the subthreshold region.
K_1, K_2	Body factor for short- and long-channel devices.
K_3, K_4	Body factor for narrow-gate device.
$K_L(L, V_{BS})$	Effective body factor for short- and long-channel devices.
$K_W(W, V_{BS})$	Effective body factor for narrow-gate device.
L	Effective channel length.
λ	Fitting parameter.
L_m	Mask channel length.
m	Slope of the subthreshold $\log(I_D L/W)$–V_{GS} characteristics.
μ_n	Effective channel mobility.
μ_0	Low field mobility.
N_A	Substrate doping of n-channel MOSFET (in atoms per cubic centimeter).
Φ_S	Surface inversion potential.
q	Magnitude of electron charge (in coulombs).
Q'_B	Bulk charge per unit channel length.
ΔQ_B	Induced side charge per unit length due to the narrow-gate effect.
Q_B	Bulk charge per unit area.
Q_C	Channel carrier charge per unit area.
Q_G	Gate charge per unit area.
R_{DS}	Measured total resistance between the source and the drain (in ohms).
T	Device temperature (in kelvins).
t_F	Field oxide thickness (in angstroms).
θ	Mobility degradation factor in the direction perpendicular to the channel current.
t_{OX}	Gate oxide thickness (in angstroms).
V_{BIN}	Effective quantity of $V_{FB} + \Phi_S$.
V_{BS}	Back gate bias (in volts).
V_{DS}	Drain-to-source voltage.
V_F	Equilibrium Fermi potential in the semiconductor bulk measured from the intrinsic Fermi potential position.
V_{FB}	Flat-band voltage.
V_{GS}	Gate-to-source voltage.
V_{ON}	Subthreshold voltage corresponding to the constant current I_{ON}.
$V_N(y)$	Electron quasi-Fermi potential.
V_t	Thermal voltage ($=kT/q$).
V_{T0}	Theoretical threshold voltage of a long-channel wide-gate device.

Manuscript received September 30, 1988; revised October 9, 1989. This work was supported by the National Science Council, Taiwan, Republic of China, under Contracts NSC76-0404-E011-01 and NSC77-0404-E009-21. The review of this paper was arranged by Associate Editor P. K. Ko.

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IEEE Log Number 8932818.

0018-9383/90/0400-1020$01.00 © 1990 IEEE

V_T	Effective threshold voltage of MOSFET's extracted from terminal I_D–V_{GS} characteristics.
$v(y)$	Carrier drift velocity.
W	Effective channel width ($= W_m - \Delta W$).
W'_{CE}	Effective channel width in the subthreshold region.
W_G	Geometrical gate width of thin gate oxide ($= W_m - 2\delta w$).
W_m	Mask gate width.
x	Depth or thickness direction of the channel.
X_d	Depletion layer width in the x direction.
y	Length direction of the channel.
z	Width direction of the channel.

I. Introduction

As small-geometry MOS transistors are widely used in VLSI circuit design, the demand for accurate device and circuit models is growing rapidly. In the past, much work has been devoted to the study of the I–V characteristics of short-channel MOSFET's [1]–[3]. The SPICE3 program provides four built-in MOS transistor models in which a recent one, called BSIM [4], was developed based on a semi-empirical approach and has proved to be a better model in terms of accuracy and simplicity in formulations for *short-channel* MOS devices. In contrast, studies on the I–V characteristics of narrow-gate (width) MOSFET's are quite few. A narrow-gate MOSFET model is not available in BSIM. Also, most studies on narrow-gate MOSFET's focus on investigating independently the device parameter variations only, such as the threshold voltage [5]–[7], the effective channel width [6]–[8], subthreshold softening [9], and an abnormal characteristic called inverse narrow-width (INW) effect due to a peculiar isolation structure with fully recessed field oxide [10]. However, we still lack a complete I–V model for narrow-gate MOSFET's that will cover the whole device operating region and is suitable for circuit simulation applications.

Two basic issues that will be investigated in this paper include a new threshold voltage model and a continuous I–V model throughout the whole operating regime for narrow-gate MOSFET's. On developing the threshold voltage model, currently used models in SPICE are not suitable for devices with channel/field implant. For example, in SPICE2, theoretically developed analytical threshold voltage models based on the so-called "charge sharing" scheme for narrow-gate MOSFETs can be applied only to devices with *uniform substrate doping*. However, present CMOS technologies, particularly for submicrometer device technology, require a widespread implant in the channel and deep-bulk regions for threshold voltage adjustment and punchthrough prevention. Existing models in SPICE2 have difficulty predicting device performance for devices with a *nonuniformly doped substrate*. Therefore, we are in need of a simple and accurate threshold voltage model for devices with a channel/field implant that can be used for circuit simulation applications.

On the other hand, there is discontinuity problem at the near-threshold region (which we call a *transition region* between the subthreshold and strong inversion regions) for MOS device I–V characteristics in SPICE2 that will cause convergence problems, as first pointed out by Antognetti *et al.* [11]. In BSIM [4], an approach similar to that of [11] has been demonstrated. Our study shows that discontinuity still occurs for narrow-gate devices using either the method of Antognetti *et al.* or BSIM. Therefore, this paper will have another objective: to develope a unified I–V model of narrow-gate MOSFET's that will solve the above discontinuity problem.

In this paper, the accuracy and the discontinuity problems of the LEVEL3 MOS model in SPICE2 will be enhanced through the addition of several new features and improvements. A consistent method for determining the model parameters (which are the parameters that can be extracted from measurements directly and will be simplified as *parameters* hereafter) is deduced from the experimentally measured I–V curves based on a new extraction procedure. The model equations allow efficient and simple extraction of device parameters from a set of MOS devices with a LOCOS field oxide structure and double-implanted channel. A new threshold voltage model for narrow-gate MOSFET's is developed first and given in Section II. Formulation of an I–V equation and the associated extraction methods are developed in Section III. In addition, a special technique is also employed to model the transition region I–V characteristics such that the discontinuity problem can be avoided in the new model. Section IV presents a verification of the present model with the experimental results and its comparison with other reported models. A summary and conclusion are given in the last section.

II. The Threshold Voltage Model

Among the device parameter variations due to the narrow-gate effect (NGE), threshold voltage is the most important. Numerous studies have been made to analytically model the threshold voltage using a charge-sharing scheme [5] based on the geometrical approach. However, they have limited application in the present CMOS technology for several reasons. One is that most of the models can be applied only to MOS devices with uniform substrate doping. For devices with a channel or field implant, these models are either not accurate or too complicated for circuit simulation applications [3]. These drawbacks can be overcome by using the semi-empirical approach developed in this paper in which model parameters are built upon experimentally measured data rather than from a simple analytical method.

A. Model Formulation

The narrow-gate effect of long-channel but narrow-gate-width n-MOS devices with a LOCOS field oxide structure

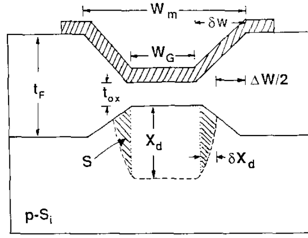


Fig. 1. The schematic diagram of MOSFET with LOCOS gate oxide structure. The shaded area S shown is the approximation used in SPICE LEVEL3.

was modeled in this paper. Its schematic diagram in the width direction is shown in Fig. 1, where W_m is the mask gate width.

For large gate width, the conventional (theoretical) threshold voltage of an n-MOSFET with *uniform substrate doping* can be expressed by

$$V_{T0} = V_{FB} + \Phi_S + Q_B/C_{ox} \tag{1}$$

where

$$Q_B = qN_A X_d \tag{2}$$

is the bulk depletion charge per unit area and $X_d = \sqrt{2\epsilon_{si}(\Phi_S - V_{BS})/qN_A}$ is the depletion width. It is noted that V_{T0} is proportional to the first order of $(\Phi_S - V_{BS})^{1/2}$, while from the measured results it is proportional to the second order of $(\Phi_S - V_{BS})^{1/2}$ for devices with an implanted channel or nonuniformly doped substrate. Therefore, for a *nonuniformly doped substrate* MOS device with long channel length and large gate width, we may define its effective threshold voltage as the following:

$$V_T = V_{FB} + \Phi_S + K_1\sqrt{\Phi_S - V_{BS}} - K_2(\Phi_S - V_{BS}) \tag{3a}$$

or

$$V_T = V_{BIN} + K_L(L, V_{BS})\sqrt{\Phi_S - V_{BS}} \tag{3b}$$

where

$$K_L(L, V_{BS}) = K_1 - K_2\sqrt{\Phi_S - V_{BS}}. \tag{3c}$$

Here, $V_{BIN} = V_{FB} + \Phi_S$ using the notation as in SPICE2. V_{FB} is the flat-band voltage. Φ_S is the surface inversion potential. K_1 is the first-order body factor, and K_2 is the second-order body factor that exists due to the implanted channel. $K_L(L, V_{BS})$ is called the effective body factor. K_1 and K_2 can be obtained using a new approach and will be described in Section II-B.

As the channel width becomes narrower, there is lateral diffusion of the depletion layer boundary toward the field-oxide region which then results in an additional bulk side charge (bounded by the shaded area in Fig. 1) and an increase of the threshold voltage with decreasing channel width. If the area of the shaded region is S, the effective bulk depletion charge per unit length will become

$$\begin{aligned} Q_B' &= qN_A(X_d W_G + 2S) \\ &= Q_B W_G + \Delta Q_B \end{aligned} \tag{4}$$

where $\Delta Q_B (= 2qN_A S)$ is the total induced side charge due to the narrow-gate effect. W_G is the geometrical gate width of the thin gate oxide region and is related to the mask gate width by $W_G = W_m - 2\delta w$ ($2\delta w$ is the total bird's beak length). As a consequence, the threshold voltage expression can be modified to take into account the narrow-gate effect as

$$V_T = V_{FB} + \Phi_S + Q_B'/C_{ox}' \tag{5a}$$

where C_{ox}' is the capacitance per unit length. C_{ox}' can be simply approximated by $C_{ox} W_G$. Hence, (5a) can be reduced further to

$$\begin{aligned} V_T &= V_{FB} + \Phi_S + Q_B/C_{ox} + \Delta Q_B/W_G C_{ox} \\ &= V_{FB} + \Phi_S + Q_B/C_{ox} + \Delta V_T. \end{aligned} \tag{5b}$$

In the SPICE2 LEVEL3 MOS model, the shaded area is approximated by an ellipsoid with long and short axes of X_d and δX_d, respectively, so that the threshold voltage shift between a narrow-gate-width device and a large-width device is given by [2]

$$\begin{aligned} \Delta V_T &= qN_A 2S/W_G C_{ox} \\ &= (\delta\pi\epsilon_{si}/W_G C_{ox})(\Phi_S - V_{BS}) \end{aligned} \tag{6a}$$

which shows that ΔV_T is proportional to X_d^2 or $(\Phi_S - V_{BS})$ and δ is a fitting parameter. The above formula is valid for MOS devices with uniform substrate doping only. However, it fails for a nonuniformly doped substrate device with both a channel implant and an isolation field implant. Alternatively, we may assume that the lateral diffusion of the depletion layer in the width direction increases lower than that in the depth direction due to the isolation field implant. Hence, the edge charge is split into two components; one is proportional to X_d, and the other one is proportional to X_d^2. As will be shown later, ΔV_T can thus be fitted accurately with two empirical parameters as

$$\begin{aligned} \Delta V_T &= (K_3 + K_4\sqrt{\Phi_S - V_{BS}})\sqrt{\Phi_S - V_{BS}} \\ &\triangleq K_W(W, V_{BS})\sqrt{\Phi_S - V_{BS}} \end{aligned} \tag{6b}$$

in which $K_W(W, V_{BS}) = K_3 + K_4\sqrt{\Phi_S - V_{BS}}$ is called the effective body factor for narrow-gate MOS devices. K_3 and K_4 are the first- and second-order body factors dependent on the device width due to the combining effect of the gate width shrinking and channel/field implant effects for narrow-gate devices.

The final form of the threshold voltage model is obtained by incorporating (3b) and (6b), i.e.,

$$\begin{aligned} V_T = V_{BIN} &+ K_L(L, V_{BS})\sqrt{\Phi_S - V_{BS}} \\ &+ K_W(W, V_{BS})\sqrt{\Phi_S - V_{BS}} \end{aligned} \tag{7}$$

which is valid for *nonuniformly doped* channel MOS devices with *long channel length* and *narrow gate width*. From a set of test devices with different gate widths and the measured threshold voltages, the empirical parameters V_{BIN}, K_1, K_2, K_3, and K_4 can be determined.

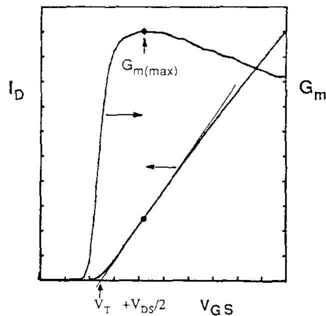


Fig. 2. Extrapolation of the effective threshold voltage and the variation of transconductance with V_{GS}.

B. Extraction of Model Parameters

The experimental n-channel MOS devices were fabricated using the standard poly-Si gate CMOS process. One set of test structures has a mask channel length of 10 μm, and the mask gate width is varied from 1.5 to 10 μm. Another set has a gate width 55 μm, and the mask channel length varied from 1.5 to 27.5 μm for determining the effective channel length. The silicon wafers used were (100) orientation, and the resistivity ranged from 15 to 25 Ω-cm. The shallow and deep implants were carried out by using energies of 25 and 150 keV and doses of 7.5 $\times$ 10^{15}/cm^2 and 4 $\times$ 10^{15}/cm^2, respectively. The source and drain junctions were formed by using an As^+ implant through a thin oxide (200 Å) with an energy of 60 keV and a dose of 6 $\times$ 10^{15}/cm^2. The gate oxide was measured to be 285 Å. The field-oxide thickness was 4040 Å. SEM photograph of the gate oxide gives a total bird's beak length of 0.9 μm. The source and drain junction depths are 0.3 μm. A GPIB-based IBM PC and an HP 4145B parameter analyzer were used for I-V measurements. The *effective threshold voltage* is defined by finding the *maximum slope* of the I_D-V_{GS} curve (Fig. 2) at small V_{DS} (e.g., 100 mV) and extrapolating to zero current, intersecting the V_{GS} axis at $V_T + 0.5V_{DS}$, from which V_T is determined.

Fig. 3 gives the extracted effective threshold voltage versus $\sqrt{\Phi_S - V_{BS}}$ for different gate widths. Here, for the sake of simplicity and the same reasoning as given in [12], $\Phi_S = 2V_F$ is used and $V_F = (kT/q) \ln (N_A/n_i)$. First, V_{BIN}, K_1, and K_2 can be obtained from the bottom curve for a long-channel and wide-gate device. The second-order fitting of this curve gives the intercept with the vertical axis V_{BIN}. Values of K_L at different backgate biases can be computed from (3b). Then, a typical plot of K_L versus $\sqrt{\Phi_S - V_{BS}}$ will be a straight line as shown in Fig. 4, in which K_1 and K_2 can be determined. K_2 is the slope of the curve that shows the channel doping modulation effect and will be zero for uniform substrate doping devices. By assuming constant V_{BIN}, formulation of (3b) and (3c) and the above procedures to determine K_1 and K_2 are also valid for short-channel devices as given elsewhere [13], in which K_1 and K_2 can be expressed as functions of

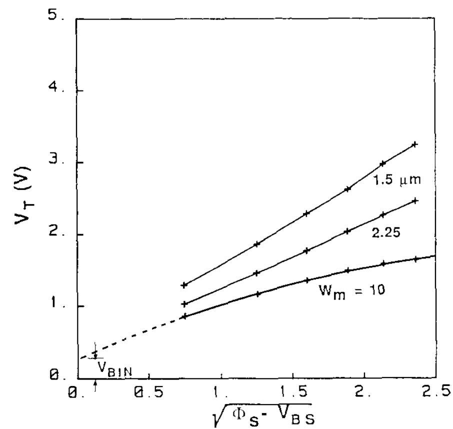


Fig. 3. Variation of effective threshold voltages with $\sqrt{\Phi_S - V_{BS}}$ at three different gate widths, W_m = 1.5, 2.25, and 10 μm.

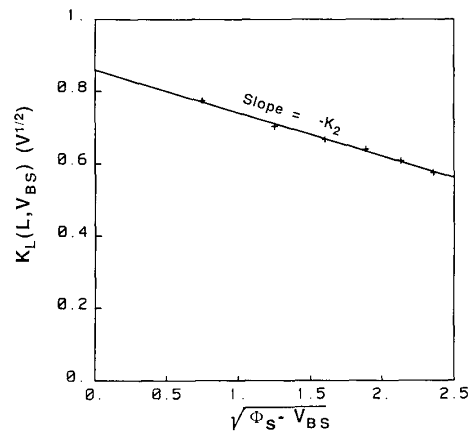


Fig. 4. Determination of K_1 and K_2 for a large device with $L_m = W_m$ = 10 μm.

channel length for short-channel devices. In fact, K_L accounts for the short-channel effect and the channel implantation effect. Once the values of K_L and V_{BIN} for a wide-gate-width device (bottom curve of Fig. 3) are known, the parameters for narrow-gate devices can be determined as follows. Using the bottom curve (10 μm) as the reference and taking the difference of their values between this and any of the other curves, the threshold voltage shifts (ΔV_T) for different gate width devices as a function of backgate bias are thus computed. Again, based on (6b), K_W can be determined and its plot against $\sqrt{\Phi_S - V_{BS}}$ gives Fig. 5 with the gate width as a varying parameter. Finally, variations of K_3 and K_4 as functions of channel width can be plotted and fitted as shown in Fig. 6. The increase of K_3 and K_4 with reducing channel width is consistent with the fact that the narrow-gate MOS device has a higher threshold voltage. Note that K_W approaches zero for large W, which means that there is zero threshold voltage shift (see (6b)) for the wide-gate device.

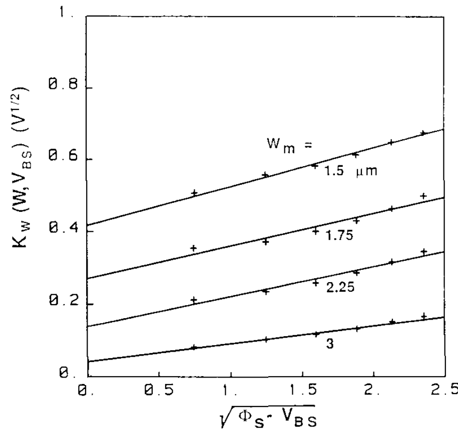


Fig. 5. Determination of $K_W(W, V_{BS})$ for different channel widths.

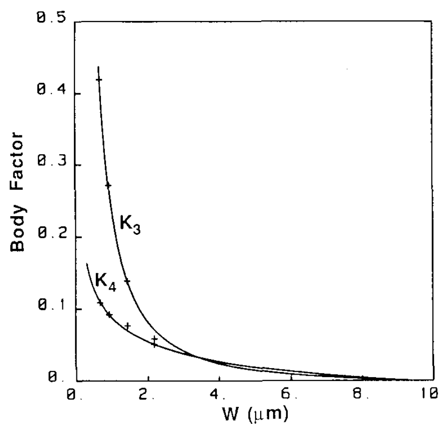


Fig. 6. Variations of the extracted values of K_3, K_4 with effective channel width. $K_3 = 0.25\ W^{-1.44}$, $K_4 = 0.18\ W^{-0.3} - 0.093$. (+ + + +) extracted; (——) fitted.

III. The I–V Model Formulation

In this section, the improved semi-empirical I–V characteristics of narrow-gate MOSFET's and the extraction of model parameters will be demonstrated and illustrated with examples. The present I–V model is built upon the LEVEL3 MOS model with many modifications such as mobility degradation, subthreshold I–V characteristics, and a new formula to model the subthreshold and transition region I–V characteristics. In the *strong inversion region* (include both the linear and saturation regions), five parameters will be used in the I–V formulation, i.e., channel width reduction ΔW, due to the bird's beak and field-implant encroachment, low field mobility μ_0, mobility degradation factors θ and β, and the effective threshold voltage V_T. In the *subthreshold region*, the subthreshold slope (m) and a new term V_{ON}, called the *subthreshold voltage* (a voltage close to and smaller than V_T), are used to describe its I–V characteristics. Moreover, in the transition region, a new approach is employed to achieve a smooth connection between the subthreshold region and the strong inversion region curves.

A. Strong Inversion Region

1) Linear Region Current ($V_{GS} > V_T$ and $0 < V_{DS} < V_{DSAT}$): Based on the LEVEL3 I–V model, the drain current of a MOSFET can be modified and given by the following equation:

$$I_D = \mu_n C_{ox}(W/L)\left[(V_{GS} - V_T) - 0.5aV_{DS}\right]V_{DS} \quad (8a)$$

where

$$\mu_n = \mu_0/\left[1 + \theta(V_{GS} - V_T)(1 + \eta V_{DS}) + \beta/W\right] \quad (8b)$$

$$a = 1 + \frac{0.5g(K_1 + K_3)}{\sqrt{\Phi_S - V_{BS}}} - (K_2 - K_4) \quad (8c)$$

and

$$g = 1 - \frac{1}{1.744 + 0.836(\Phi_S - V_{BS})}. \quad (8d)$$

Here, V_T is the effective threshold voltage and W is the effective channel width in the linear region for narrow-gate MOS devices. W can be expressed further by $W_m - \Delta W$, where ΔW is the channel width reduction due to the bird's beak of a LOCOS field-oxide structure and the field implant doping encroachment. a is the body effect charge-sharing factor [4]. It is worth noting that (8c) has a new form that is different from that in [4]. This is caused by the introducing of a new body effect term in (7). A detailed derivation of a is given in the Appendix. By considering the three-dimensional effect, the mobility degradation should be modified as in (8b) by adding an additional degradation factor β caused by width modulation. In (8b), μ_0 is the low field mobility, θ is the mobility degradation factor due to the normal or transversal field, and η is the velocity saturation factor. $\eta = 0$ is used in this paper for characterizing narrow-gate devices.

2) Saturation Region Current ($V_{GS} > V_T$ and $V_{DS} \geq V_{DSAT}$): In this region, the I–V characteristic is obtained by setting $V_{DSAT} = (V_{GS} - V_T)/\alpha$, which then gives

$$I_D = \mu_n C_{ox}(W/L)\left[V_{GS} - V_T\right]^2/2a. \quad (9)$$

B. The Subthreshold Region

The present model is a modified version of a previous subthreshold I–V model by Chung and Sah [9] in which an analytical approximation formula for narrow-gate MOSFET's can be simplified and given by

$$I_{D,W} = I_{ON}(W/L)\,e^{m(V_{GS} - V_{ON})}(1 - e^{-V_{DS}/V_t}) \quad (10a)$$

where

$$I_{ON} = \mu_0(W/L)(\alpha C_{ox})(V_t)^2. \quad (10b)$$

Here, m is the subthreshold slope and is a function of gate width and backgate bias. α is a fitting parameter. Note that V_{ON} is used in (10a) instead of V_T, where V_{ON} is the

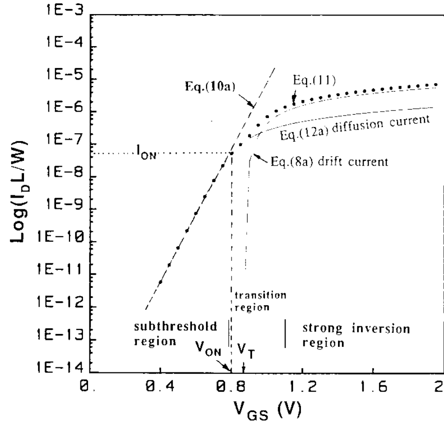


Fig. 7. Three regions of operation for an MOS device. Diffusion current is approximated by (12a). Drift current is computed from (8a). Dotted curve is computed from (11).

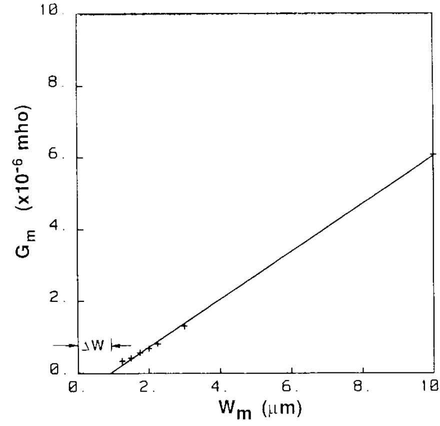


Fig. 8. Determination of the channel width reduction, $\Delta W = 0.81\ \mu$m.

voltage below V_T such that each different gate width device has the same constant current at this point. The best fit of the measured subthreshold I–V characteristics of narrow-gate MOSFET's using (10a) can be achieved by obtaining the gate-width- and V_{BS}-related functional forms for m and V_{ON}, i.e., $m = f(W, V_{BS})$ and $V_{ON} = f(W, V_{BS})$.

C. Transition Region

In the subthreshold region, the diffusion current is much larger than the drift current, and provides a good fit for the I–V curve in the region below V_{ON}, as shown in Fig. 7. Fig. 7 also shows the drift component. In the transition region, the diffusion current is comparable to the drift current. To model the I–V characteristic in this region, a continuous model for both current and conductance can be achieved by the following approximation formula:

$$I_{D,\text{total}} = I_{ON}(W/L) \ln \left[e^{(I_{D,S}L/WI_{ON})} + e^{m(V_{GS}-V_{ON})}\right] \cdot (1 - e^{-V_{DS}/V_t}) \qquad (11)$$

in which $I_{D,S}$ is the drift current from (8a). Equation (11) will match the following two extreme cases:

1) When $V_{GS} << V_T$, $I_{D,S}$ is zero in this region, (11) will be reduced to

$$I_{D,\text{total}} = I_{ON}(W/L) \ln \left[1 + e^{m(V_{GS}-V_{ON})}\right] \cdot (1 - e^{-V_{DS}/V_t}) \qquad (12a)$$

or

$$I_{D,\text{total}} \approx I_{ON}(W/L)\, e^{m(V_{GS}-V_{ON})}(1 - e^{-V_{DS}/V_t}) \qquad (12b)$$

since $\ln(1 + x) \approx x$ for $x << 1$. Equation (12a) becomes the diffusion component in the conventional drift-diffusion model and is shown in Fig. 7. Equation (12b) shows that the approximation formula, (11), will approach the diffusion current in the subthreshold region.

2) When $V_{GS} >> V_T$, the drift current is much larger than the diffusion current, and (11) reduces to $I_{D,\text{total}} = I_{D,S}$.

Moreover, in the transition region, (11) gives a good fit for the I–V curve as shown in Fig. 7. In fact, we can set $I_{D,S} = 0$ (i.e., zero drift current) in this region; then (11) will be reduced to (12a), which is the actual approximation of the diffusion current since the diffusion current will reach saturation at high gate voltages.

D. Extraction of Model Parameters

1) Determination of ΔW, ΔL: Fig. 2 also shows the variation of transconductance versus gate voltage (V_{GS}), which is defined by $G_m = (\delta I_D/\delta V_{GS})_{V_{DS}}$ at small V_{DS}. According to (8), the maximum value of transconductance $G_{m(\max)}$ is related to the mask gate width by

$$G_{m(\max)} = \mu_0 C_{ox}(W_m - \Delta W)\, V_{DS}/L. \qquad (13)$$

In practice, $G_{m(\max)}$ is determined as the maximum slope of the I_D–V_{GS} curve at small V_{DS}. Measurement of the I–V curves for various gate width (W_m) devices gives the plot of $G_{m(\max)}$ versus W_m as shown in Fig. 8, in which the intercept of the curve with the W_m axis gives ΔW. ΔL can be extracted in a similar manner as in [3] from a set of test samples with different channel lengths by eliminating the series resistance effect.

2) Determination of μ_0, θ, and β: At a small value of V_{DS} and high gate voltages (V_{GS}), μ_0, θ, and β can be determined from the linear region I_D–V_{GS} characteristics. In such a case, combining (8a) and (8b) gives

$$R_{DS} = V_{DS}/I_D = [1/\beta_0]\left[(V_{GS} - V_T)^{-1}(1 + \beta/W) + \theta\right] \qquad (14a)$$

where

$$\beta_0 = \mu_0 C_{ox}(W_m - \Delta W)/L. \qquad (14b)$$

From (14a), R_{DS} can be plotted as a function of $(V_{GS} - V_T)^{-1}$ for various gate width devices as shown in Fig. 9

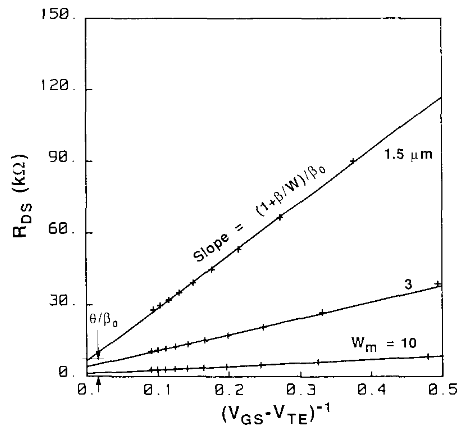


Fig. 9. Fitted curves of R_{DS} versus $(V_{GS} - V_T)^{-1}$ for W_m = 1.5, 3, and 10 μm.

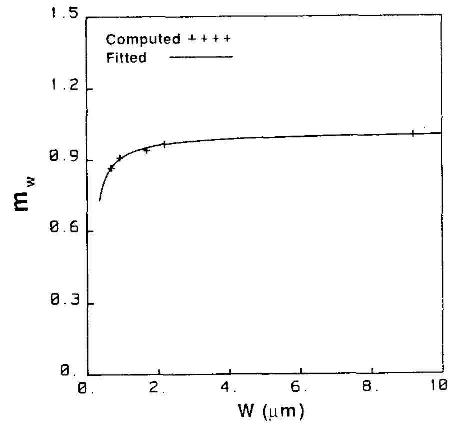


Fig. 11. Normalized subthreshold slope (m_w) from measured data and the fitted results for various widths. m_0 = 24.3. $m_w = 1 - 0.1\ \mathrm{W}^{-0.97}$.

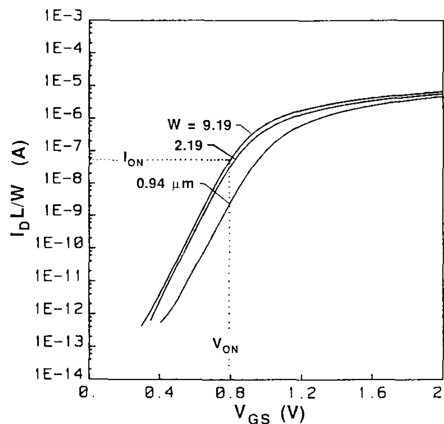


Fig. 10. Measured subthreshold characteristics for three different gate widths, W = 9.19, 2.19, and 1.44 μm at V_{BS} = 0 V. I_{ON} = 50 nA, m_0 = 24.3, and α = 6.7.

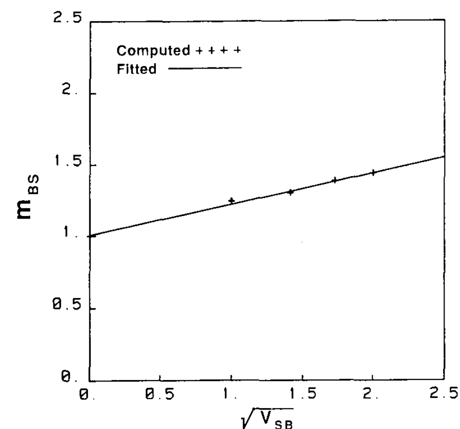


Fig. 12. Normalized subthreshold slope (m_{BS}) versus $\sqrt{V_{SB}}$ for W = 9.19 μm. $m_{BS} = 1 + \lambda\sqrt{V_{SB}}$, where $\lambda = 0.217\ \mathrm{V}^{-1}$.

and can be fitted with straight lines. The slope of these curves is $(1 + \beta/W)/\beta_0$ and the intercept with the vertical coordinate is θ/β_0. From the bottom curve for a wide-gate device ($L_m = W_m = 10\ \mu$m), its slope gives μ_0 = 544 cm^2/V-s since $\beta/W << 1$ and the intercept gives $\theta = 0.0812\ \mathrm{V}^{-1}$. From the other curves for different gate width devices, β can be obtained by plotting $1 + \beta/W$ versus W^{-1}, which then yields $\beta = 0.14\ \mu$m.

3) Determination of the Subthreshold Parameters m and V_{ON}: In the subthreshold formula (10a), the subthreshold slope and V_{ON} can be characterized as functions of W and V_{BS}. Considering first the variation of subthreshold slope due to the narrow-gate effect, a family of curves for different gate width devices is given in Fig. 10, in which the normalized drain current (I_DL/W) is plotted against gate voltage (V_{GS}). From the measured result of a wide-gate device (W = 9.19 μm in Fig. 10), we choose an appropriate I_{ON} whose corresponding gate voltage (V_{ON}) will lie in the region below V_T. In practice, the best fit of the subthreshold characteristics requires that I_{ON} is chosen to be located in the linear region of log (I_DL/W)–V_{GS} curves. Then α can be determined from I_{ON} and (10b). The subthreshold slope for each different gate width device can be obtained by a first-order least square fitting in the range $V_{GS} < V_{ON}$, which results in a set of data (+ symbols). From a set of three values of m thus obtained for three gate widths, the following formula can be used to interpolate the m values at the other gate widths

$$m_w = AW^{-n} + B \tag{15}$$

where A, B, and n are uniquely determined from three test transistors. m_w is the normalized value of the subthreshold slope of a narrow-gate device with respect to m_0, where m_0 is the subthreshold slope of a wide-gate device at V_{BS} = 0 V. Fig. 11 shows the comparison between the extracted result of m and the fitted result (solid line) using (15). Variations of m with V_{BS} can be made in the same manner by computing the subthreshold slope of a wide-gate device at different backgate biases and can be approximated by $m_{BS} = 1 + \lambda\sqrt{V_{SB}}$ as shown in Fig. 12.

Finally, the expression of m as a function of W and V_{BS} is given by

$$m(W, V_{BS}) = m_0 m_w m_{BS} = m_0(AW^{-n} + B)(1 + \lambda\sqrt{V_{SB}}). \quad (16)$$

Since V_{ON} is sometimes used as the definition of the threshold voltage as reported in the literature [14], the functional relationship between V_{ON} and W, V_{BS} can be characterized in the same way as V_T using (7) and the extraction procedures in Section II-A.

IV. Comparisons Between Experiments, New Models, and Reported Models

This section deals with comparisons of experimental and modeled results as well as a comparison between the new model and reported models [1], [4], [11].

Fig. 13 gives the verification of modeled threshold voltages against the measured threshold voltages for different gate widths at various back-gate biases. Excellent agreement is achieved. Note that simple formulation of the threshold voltage expression, (see (7)) makes it well suited for CAD applications. The strong inversion I_D-V_{GS} characteristics for wide-gate ($W = 9.19$ μm) and narrow-gate ($W = 0.94$ μm) devices are shown in Fig. 14(a) and (b), respectively, in which comparisons have also been made for the measured (solid lines) and modeled (dotted lines) results. Fig. 15(a) and (b) shows the accuracy test between measured and modeled I-V characteristics in the subthreshold and transition regions for wide-gate and narrow-gate devices, respectively. It was shown that reasonable agreement has been achieved, which strongly supports the validity of the model equations. Several major improvements in this work will be described and compared with reported models as follows.

Fig. 16 gives a comparison of the threshold voltages between the new model and SPICE2. The total threshold voltages using SPICE2 consist of two terms, (3b) and (5), where the average value of δ ($\delta = 0.5$) for various gate widths is calculated by matching experimental data with these equations. Here, the constant δ for different gate widths (this is the basic assumption of the *charge-sharing model* used in SPICE2) is used in Fig. 16. It shows that the SPICE2 model can not predict well, as is also shown in the comparison between the measured and SPICE2 data. The main discrepancies are described as follows. SPICE2 uses (6a) as the threshold voltage shift for narrow-gate devices. However, comparison of (6a) and (6b) shows that ΔV_T is proportional to $(\sqrt{\Phi_S - V_{BS}})^2$ only while a first-order term is included in the new model. This first-order term will model the narrow-gate effect and doping effect appropriately. However, the SPICE2 model does not consider the effects of channel or field implants due to the simplified charge-sharing approach. Therefore, we conclude that the threshold voltage model in SPICE2 may work well for a uniformly doped substrate device but is not suitable for an implanted-channel device.

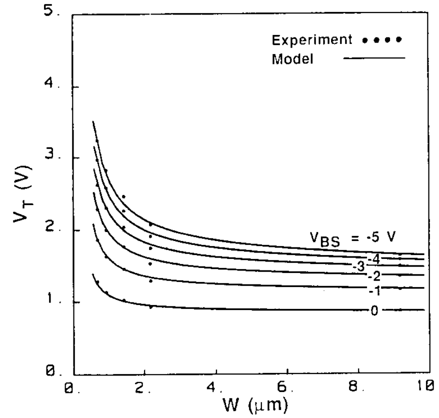
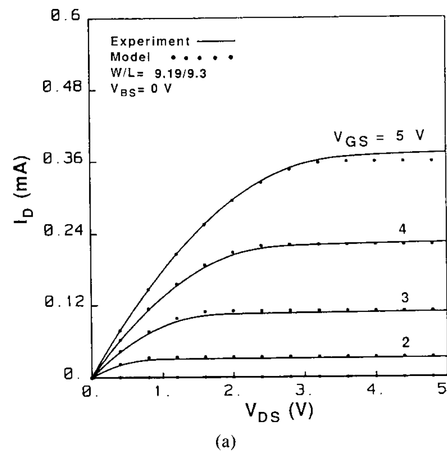
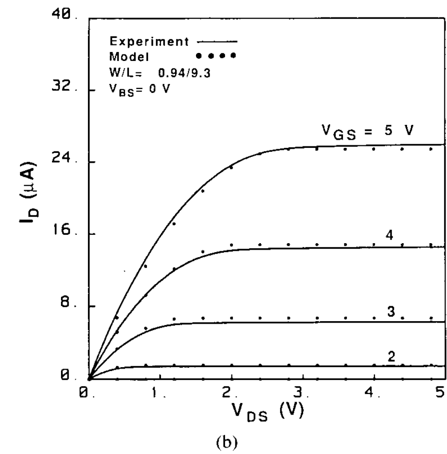


Fig. 13. Comparison of the measured and modeled V_T results at various back-gate biases.



(a)



(b)

Fig. 14. Comparison of the experimental results with modeled results. (a) $W/L = 9.19/9.3$. (b) $W/L = 0.94/9.3$.

In (7), if we combine K_1 with K_3 and K_2 with K_4, this equation will be reduced to the form of BSIM. However, accuracy has been improved based on a different extrac-

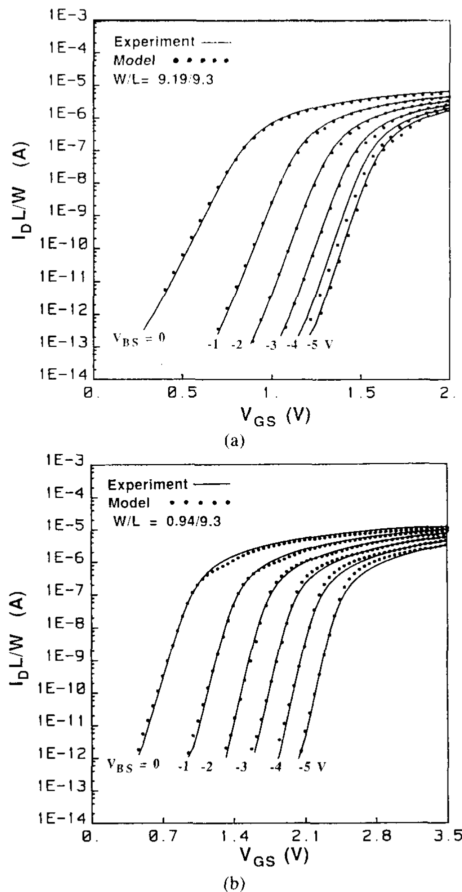


Fig. 15. Comparison of the subthreshold and transition regions I-V characteristics between measured and modeled results. (a) $W/L = 9.19/9.3$. (b) $W/L = 0.94/9.3$.

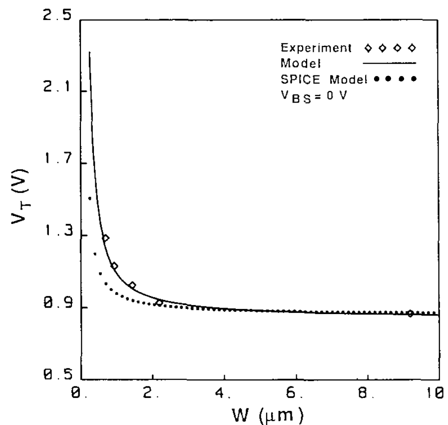


Fig. 16. Comparison of the threshold voltages for measured, modeled, and SPICE results.

tion method in the new model. First, BSIM simply uses $P_0 + P_1/W$ (inverse-geometry model) to model the narrow-gate effect parameter. As indicated by Hsu and Sheu in [15], this simple inverse-geometry model cannot predict very well the threshold voltage for the whole channel (or width) range. As a consequence, a modified model called a *clamped inverse-geometry model* [15] has to be used. However, in our new model, narrow-gate parameters K_3 and K_4 are fitted by $AW^{-n} + B$ (as shown previously in Fig. 6) with n different from 1, and an accurate threshold voltage can be predicted in the whole channel with range. Second, the narrow-gate effect can be independently derived in the new model; however, it is hard to tell the difference from a physical point of view between the extent of the narrow gate or doping effect and the threshold voltages in BSIM. The advantage of the formulation in (7) is that K_L and K_W can be used for accurately predicting the short-channel effect and the narrow-gate effect, respectively. For real applications, it has also been shown in [13] that (7) is suitable for small devices by adding the drain-induced barrier lowering effect.

In the strong inversion I-V equation, a new form of a is derived in which the $(K_2$-$K_4)$ term is neglected in BSIM. By doing so, the influence of backgate bias effect on the I-V characteristics due to short channel/narrow gate effect and doping effect can be clearly demonstrated.

In developing the transition region I-V characteristics, if we follow the method of Antognetti or BSIM (both approaches are basically the same), the discontinuity still occurs for narrow-gate devices at large backgate biases. Although there is a perceived deviation of the modeled I-V results (for example, the $V_{BS} = -5$ V curve shown in Fig. 14(b)), discontinuity can be avoided using the new approach. In addition, it reveals from (11) and (16) and the fitted results of Fig. 7 that a smooth connection between the subthreshold and strong inversion can be achieved. Also, the derivatives of the drain current (see (11)), with respect to V_{GS} and V_{BS} can be assured since all of the terms in the equation are a continuous function of bias. It is also expected that (11) and the associated extraction method can be extended to short-channel devices. In this case, subthreshold slope and V_T and V_{ON} are continuous functions of V_{DS} and the derivatives of drain current with respect to V_{DS} will also be continuous.

One final point that we would like to stress is that the derivation of the model equations and the extraction method are not restricted to one specific set of test samples. The present model is also expected to be applicable to more complicate field-oxide structure devices, such as the fully recessed field-oxide structure, since the extraction method is independent of device structure or process. The only difference between the two different structures or processes is the precise quantative description of the modeled parameters. For example, fully recessed field-oxide MOS devices will have reduced threshold voltages with decreasing gate width. It seems that the simple extraction procedure in Section II also can be applied. Further study of the model for fully recessed gate oxide MOSFET's using the proposed approach is needed and will be reported in a future paper when available.

V. Summary and Conclusion

In this paper, a unified I–V model for narrow-gate MOSFET's that is valid for devices operating from subthreshold region to the strong inversion region has been developed based on a semi-empirical approach. For the first time, a very simple-to-use threshold voltage expression has been developed with only four easily extracted parameters. Particularly, the proposed threshold voltage model is suitable for devices with channel/field implant. The present strong inversion I–V model was built upon the SPICE LEVEL3 MOS model, and the subthreshold I–V model was built upon our previous model with several major modifications and improvements. The methods of extracting model parameters from the measured I–V characteristics are also illustrated. Only seven major parameters are required to fully adapt the I–V model to a given process. In addition, in the *transition region*, a new scheme is employed to guarantee the smooth transition of the I–V curve at the near-threshold region such that both the drain current and the conductance are continuous. It has been shown that satisfactory agreement between experimental and modeled I–V results has been achieved for a wide range of gate widths and biases. Particularly, the threshold voltage comparison of the new model and of the SPICE2 model shows the inadequacy of the latter. The efficient use of the model results because the proposed I–V characteristics can be an additional feature to be incorporated with other reported short-channel I–V models for use in simulating VLSI circuits that consist of both short-channel and narrow-gate MOSFET's.

Appendix

The drain current of a narrow-gate MOSFET similar to BSIM but in a somewhat different form will be derived here. The drain current for MOS devices operating in the strong inversion region can be expressed by

$$I_D = \int_0^W Q_c v(y)\, dz \tag{A1a}$$

where $v(y)$ is the carrier drift velocity given by

$$v(y) = \mu_n\, dV_N/dy \tag{A1b}$$

and Q_c is the carrier change per unit area at any point y in the channel.

The gate charge is given by

$$Q_G = C_{ox}(V_{GS} - V_{FB} - \Phi_S - V_N) \tag{A2}$$

and the bulk charge is given effectively by

$$Q_B = C_{ox}K\sqrt{\Phi_S - V_{BS} + V_N} \tag{A3}$$

in which the effective body factor $K = (K_1 + K_3) - (K_2 - K_4)\sqrt{\Phi_S - V_{BS} + V_N}$ (by comparing with (7)) is used due to the contribution of the body effect caused by the channel implant and narrow-gate effect. Q_C is then given by

$$\begin{aligned} Q_C = Q_G - Q_B = C_{ox}\big[&V_{GS} - V_{FB} - \Phi_S - V_N \\ &- (K_1 + K_3)\sqrt{\Phi_S - V_{BS} + V_N} \\ &+ (K_2 - K_4)(\Phi_S - V_{BS} + V_N)\big]. \end{aligned} \tag{A4}$$

Combining (A1a), (A1b), and (A4) and integrating (A1a) along the channel gives

$$\begin{aligned} I_D &= \mu_n C_{ox}(W/L)\int_0^{V_{DS}} \big[V_{GS} - V_{FB} - \Phi_S - V_N \\ &\quad - (K_1 + K_3)\sqrt{\Phi_S - V_{BS} + V_N} \\ &\quad + (K_2 - K_4)(\Phi_S - V_{BS} + V_N)\big]\, dV_N. \\ &= \mu_n C_{ox}(W/L)\big\{(V_{GS} - V_{BIN} + (K_2 - K_4) \\ &\quad \cdot \sqrt{\Phi_S - V_{BS}})\, V_{DS} - [1/2 - (K_2 - K_4)]\, V_{DS}^2 \\ &\quad - (K_1 + K_3)\, F(V_{DS}, \Phi_S - V_{BS})\big\} \end{aligned} \tag{A5a}$$

where

$$\begin{aligned} F(V_{DS}, \Phi_S - V_{BS}) = (2/3)\big[&(V_{DS} + \Phi_S - V_{BS})^{3/2} \\ &- (\Phi_S - V_{BS})^{3/2}\big]. \end{aligned} \tag{A5b}$$

The later can be further approximated by [5]

$$\begin{aligned} &F(V_{DS}, \Phi_S - V_{BS}) \\ &\quad = \sqrt{\Phi_S - V_{BS}} + (0.25 g V_{DS}^2/\sqrt{\Phi_S - V_{BS}}) \end{aligned} \tag{A6a}$$

where

$$g = 1 - \frac{1}{1.744 + 0.836(\Phi_S - V_{BS})}. \tag{A6b}$$

Using the above approximation, (A5a) can be reduced to (8a), and the body effect charge sharing factor (a) is given in (8c).

Acknowledgment

The author would like to express his sincere thanks to Dr. D. C.-T. Chen, Dr. M.-K. Lee, and C.-N. Chen of ERSO, ITRI, Hsinchu, Taiwan, for providing test samples. Valuable suggestions from the reviewers are also gratefully acknowledged.

References

[1] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using SPICE2," Univ. of California, Berkeley, Memo. UCB/ERL M80/7, 1980.

[2] H. I. Hanafi, L. H. Camitz, and A. J. Dally, "An accurate and simple MOSFET model for computer aided design," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 882–891, 1982.

[3] C. Y. Wu and Y. W. Dai, "An accurate mobility model for the I–V characteristics of n-channel enhancement-mode MOSFET's with single-channel boron implantation," *Solid State Electron.*, vol. 28, pp. 1271–1278, 1985.

[4] B. J. Sheu, D. L. Scharfetter, P. K. Ko, and M. C. Jeng, "BSIM—

Berkeley short channel IGFET model for MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 558-565, 1987.
[5] L. A. Ackers, "Threshold voltage models of short, narrow and small geometry MOSFET's," *Solid-State Electron.*, vol. 25, pp. 612-641, 1982.
[6] C. R. Ji and C. T. Sah, "Two-dimensional numerical analysis of the narrow gate effect in MOSFET," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 635-647, 1984.
[7] S. S. Chung and C. T. Sah, "Threshold voltage models of the narrow gate effect in micron and submicron MOSFETs," *Solid-State Electron.*, vol. 31, pp. 1009-1021, 1988.
[8] Y.-R. Mar and K.-L. Wang, "A new method to electrically determine MOSFET channel width," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1825-1827, 1982.
[9] S. S. Chung and C. T. Sah, "A subthreshold model of the narrow gate effect in MOSFET," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2520-2529, 1987.
[10] L. A. Ackers, M. Sugino, and J. M. Ford, "Characterization of the inverse-narrow-width effect," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2476-2484, 1987.
[11] P. Antognetti *et al.*, "CAD model for threshold and subthreshold conduction in MOSFET's," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 454-460, 1982.
[12] M. El. Banna and M.El. Nokali, "A pseudo two-dimensional analysis of short channel MOSFETs," *Solid-State Electron.*, vol. 31, pp. 269-274, 1988.
[13] S. S. Chung, T.-S. Lin, and Y.-G. Chen, "An improved *I-V* model of small geometry MOSFETs for SPICE," in *Proc. IEEE CICC* (May 15-18, San Diego, CA), 1989, p. 9.5.1.
[14] H.-G. Lee, S.-Y. Oh, and G. Fuller, "A simple and accurate method to measure the threshold voltage of an enhancement-mode MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 346-348, 1982.
[15] M. C. Hsu and B. J. Sheu, "Inverse-geometry dependence of MOS transistor electrical parameters," *IEEE Trans. Computer-Aided Design*, vol. CAD-6, pp. 582-585, 1987.

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