<span id="page-0-0"></span>The measured  $E$ - and  $H$ -plane patterns are shown in Fig. 2. These patterns agree well with theoretical predictions for a



**Fig.** *2 Farrfield patterns for transistorjpatch element of Fig. I a H*-plane; *b E*-plane; - - - - crosspolarisation measurement

rectangular patch, except for the bumpy structure in the E-plane measurement. Additional measurements performed with metal tape covering the slot suggest that the variation in the E-plane measurement may be caused by some radiation from the slot. The dashed lines in the figure represent the crosspolarisation measurements, which are at least 8 dB down from the peak copolarisation measurement. Using these measured patterns, an estimate of the total radiated power was calculated to be 6mW, giving an effective isotropic radiated power (EIRP) of 40mW and a DC-to-RF efficiency of *5%.*  This output power is comparable to the lOmW generated by these FETs in a microstrip oscillator circuit.

*Conclusions:* A new integrated active-array element has been developed. This design features a single bias line and occupies relatively little substrate space because the transistor is embedded in the patch. Further work is underway to investigate variations in FET placement on the patch, scaling the design to higher frequencies and incorporating the active patch into quasioptical power combiners and transmit-receive arrays.

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## **References**

 $\Delta \sim 10^{11}$  and  $\Delta \sim 1$ 

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- **I THOMAS, U. I., FUDGE, D. L.,** and **MORRIS,** *e.:* 'Gunn source integrated with microstrip patch, *Microwaves* & *RF,* **1985,** pp. **87-89**
- *2*  **PERKINS,** T. 0.: 'Active microstrip circular patch antenna', *Microw*  J., **1987,** pp. **1 IC-1 <sup>17</sup>**

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- 3 CHANG, K., HUMMER, K. A., and **GOPALAKRISHNAN**, G. K.: 'Active radiating element using FET source integrated with microstrip patch antenna', *Electron. Lett.,* **1988,** *24,* pp. **1347-1348**
- **IMPATT** oscillator and active antenna', *IEEE Trans.*, 1988, **MIT-36,** p. **1670**

## **PERFORMANCE OF MULTISTAGE INTERCONNECTION NETWORKS FOR INTEGRATED SERVICES**

*Indexing terms: Telecommunications, Switching* 

The performance **of** multistage interconnection networks used to switch prioritised packets is examined. The relationship between the normalised throughput for each class **of**  packet and that when packets are not categorised into priworks providing integrated services where packets of different types of information have different priorities.

*Introduction:* Multistage interconnection networks (MINs) have been widely considered for use in constructing the switching fabrics in communication networks. An  $N \times N$ MIN with  $N = \alpha^n$  is constructed by *n* stages of crossbar switching elements (SEs) of size  $\alpha \times \alpha$ . Each stage consists of  $N/\alpha$  such SEs and the interconnection pattern between stages is an  $\alpha$  shuffle.<sup>1</sup> Self-routing, potential VLSI implementation, and ease of fault diagnosis are the main benefits that make MINs attractive. The normalised throughputs of MINs under the uniform traflic assumption can be computed by the use of a simple recursive formula.' It was found that MINs are more cost effective than single-stage crossbar networks for large systems. Fig. 1 illustrates an example of a 3-stage MIN with *<sup>a</sup>*= 2.





 $\alpha=2$ 

To date, most of the results regarding the performance of MINs considered all packets to be equally important. A SE will randomly select a packet and route the selected packet to its destination output link whenever there is a conflict. No priority scheme is imposed in such an operation. In a network providing integrated services, packets of different types of information arc likely to have different priorities. In this letter, we explore the performance of unbuffered MINs when they are used to switch prioritised packets.

*System model:* The MINs considered operate in a synchronous format. Time is divided into slots called network cycles. A network cycle is further divided into two portions  $\tau_1$  and  $\tau_2$ . In  $\tau_1$ , control signals are passed across the network to determine which inlets are granted to transmit their packets. In  $\tau_2$ , packets are transmitted in accordance with the control signals.

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In this study, data packets are categorised into **s** classes. **A**  class *i* packet enjoys a higher priority than a class j packet if  $i < j$ . The packet with the highest priority is selected if there is a conflict. The random choice scheme is adopted when there is a tie. The following assumptions are made for the sake of mathematical tractability:

*(a)* Each inlet generates at most one packet in a network cycle and the probability that an inlet generates a packet in a network cycle is equal to  $\rho$  ( $0 \le \rho \le 1$ ).

(b) A fraction  $r_i$ ,  $i = 1, 2, ..., s$ , of the packets generated by each inlet is of class  $i \sum_{i=1}^{s} r_i = 1$ .

*(c)* The packets generated by an inlet are independent of the packets generated by other inlets. The packets generated in a network cycle are also independent of the packets generated in the previous cycles.

(d) Blocked packets are lost.

*Performance analysis:* Since crossbar **SEs** are the building blocks of MINs, we consider the performance of crossbar networks of size  $\alpha \times \alpha$  first. For convenience, let  $\rho_i = r_i \rho$  and  $q_i = \sum_{k=1}^i \rho_k$ ,  $i = 1, 2, ..., s$ . Let  $p_i$  denote the probability that an outlet receives a packet of class 1, class 2, ..., or class *i*. Then we have the following result:

*Lemma 1:* The probability  $p_i$  is equal to  $1 - (1 - q_i/\alpha)^x$ .

It is not hard to see that the probability that an outlet does not receive a packet of class 1, class 2, ..., or class *i* from a particular inlet is equal to  $1 - q_i/\alpha$ . With this in mind, one can easily prove Lemma 1. The probability that an outlet receives a packet of class *i* is given by  $p_i - p_{i-1} = (1 - q_{i-1}/x)^{\alpha}$  –  $(1 - q_i/\alpha)^{\alpha}$ .

Now consider the performance of the MINs. Consider a SE at stage *k*. Let  $\rho_i^{(k)}$ ,  $1 \le i \le s$ , denote the probability that an output link of the SE receives a class *i* packet. Notice that  $\rho$ represents the input rate of class *i* packets to each inlet of the MIN and hence is equal to  $r_i \rho$ . For convenience, let  $q_i^{(k)} = \sum_{j=1}^i \rho_j^{(k)}$ ,  $0 \le k \le n$  and  $1 \le i \le s$ , with  $q_0^{(k)} = 0$  for all *k*. Then, according to the results obtained for crossbar networks, we obtain

$$
\rho_i^{(k)} = (1 - q_{i-1}^{(k-1)}/\alpha)^{\alpha} - (1 - q_i^{(k-1)}/\alpha)^{\alpha} \qquad 1 \le i \le s
$$

The normalised throughput of class *i* packets is given by  $\rho_i^{(n)}$ .

*Results and discussion:* It is worth mentioning that  $q_s^{(n)}$  is equal to the normalised throughput of an n-stage MIN when packets are not categorised into priority classes.  $r_i q_s^{(n)}$  is equal to the normalised throughput of class *i* packets if the packets are categorised into classes but without priorities. Let  $z_i = \rho_i^{(n)} - r_i q_s^{(n)}$  denote the increment of the normalised throughput of class i packets. It is clear that the net increment is zero since  $\sum_{i=1}^{\infty} z_i = 0$ . The priority scheme does not change the normalised throughput of a MIN. Similarly, if  $y_i$  represents





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the percentage of increment of the normalised throughput of class *i* packets, i.e.  $y_i = z_i/r_i q_s^{(n)}$ , then  $\sum_{i=1}^{s} r_i y_i = 0$ .

[Fig. 2](#page-0-0) shows the curves of the probability of success against input rate  $\rho$  for  $n = 6$ ,  $\alpha = 2$ ,  $s = 2$ , and  $r_1 = 0.1$ . Here the probability of success of a class *i* packet is defined as  $\rho_i^{(n)}/\rho_i^{(0)}$ . By multiplying the probability of success with the input rate, one can obtain the normalised throughput of each class of packets. The maximal increment of the normalised throughput of class 1 packets is about 0.051 which occurs at  $\rho = 1$ . The curve labelled 'nonprioritised' represents the probability of success when packets are not categorised into priority classes. The percentage of increment of class **1** packets, which can be derived from the values of these curves, is roughly 141% when  $\rho = 1$ .

**Figs.** 3 and 4 show similar results for the same network with  $r_1 = 0.5$  and 0.9, respectively. The increments of the normalised throughput of class 1 packets are also maximised at  $\rho = 1$ 









**Fig. 4** *Probability* of **success** *against input rate*   $n = 6$ ;  $\alpha = 2$ ;  $s = 2$ ;  $r_1 = 0.9$ 

and are about 0.094 and 0.025 for  $r_1 = 0.5$  and 0.9, respectively. The percentage of increments of class **1** packets when  $\rho = 1$  are roughly 52.1% and 7.7% for  $r_1 = 0.5$  and 0.9, respectively. From Figs. 2-4, one can see that the percentage of increment decreases as  $r_1$  increases.

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## **References**

- 1 **PAEL,** I. **H.:** 'Performance of processor-memory interconnections for multiprocessors', *IEEE Trans.,* 1981, *C-30,* pp. **771-780**
- **2**  MCMILLAN, M. C.: 'A survey of interconnection networks'. Proc. **GLOBECOM'84,** Atlanta, **CA,** Dec. 1984, pp. 105-113 **KRUSKAL,** *c.* **P., and SNIR, M.:** 'The performance of multistage inter-
- 3 connection networks for multiprocessors', *IEEE Trans.,* **1983, C-32,** pp. **1091-1098**

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