$R(n)$ in (A.1) is

$$C(n) = R(n)^{-1} = (\overline{R} + \delta R)^{-1} \approx \overline{R}^{-1} - \overline{R}^{-1}\delta R\overline{R}^{-1}. \quad \text{(A.9)}$$

Taking the expectation of (A.9) results in

$$E[C(n)] = \overline{R}^{-1} - \overline{R}^{-1}E[\delta R]\overline{R}^{-1}. \quad \text{(A.10)}$$

Since we assume that $E[\delta R] = 0$, (A.10) simplifies to

$$E[C(n)] = \overline{R}^{-1} = E[R(n)]^{-1}. \quad \text{(A.11)}$$

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The Signal Delay in Interconnection Lines Considering the Effects of Small-Geometry CMOS Inverters

MING-CHUEN SHIAU AND CHUNG-YU WU

***Abstract*—A new physical timing model for small-geometry CMOS inverters with interconnection lines has been developed. Large-signal equivalent circuits of CMOS inverters and 10-section *RC* ladder networks for interconnection lines are considered together with nonstep input waveforms and initial delay times. Due to more realistic and complete considerations, the model accuracy is expected to be higher than the conventional delay models. Extensive comparisons between model calculations and SPICE simulations have shown that the model has a maximum relative error of 16% on the delay times of CMOS inverters with interconnection lines of different *R* and *C* values and section numbers *N*, different gate sizes, device parameters, and even input excitation waveforms. Reasonable accuracy, wide applicable range, and high computation efficiency make the developed timing models quite attractive in MOS VLSI timing verification and auto-sizing.**

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I. Introduction

As device dimensions are scaled down, the delay of interconnection lines among logic gates becomes as important as the logic-gate delay in determining the overall speed performance of a VLSI chip. It has been shown in [1] that the optimal speed can be achieved only when the interconnection delay is equal to the gate delay. This means neither of them can be overlooked in determining the total delay.

Generally, accurate and efficient gate/interconnection delay models are useful in various CAD applications in VLSI, such as timing verification, optimization, logic simulation, and auto-sizing.

Recently, many interconnection delay models [2]–[8] have been developed. However, there are some problems to be solved. The first problem is that the effect of a logic gate on the interconnection delay and the effect of interconnection on the gate delay [9] were not characterized appropriately. Modeling these effects separately [2], [5]–[8] or modeling a logic gate by a single linear *RC* circuit [3], [4] may lead to a significant error or untolerant inaccuracy in high performance design [10].

The second problem is related to input excitation waveforms. Since the actual internal voltage waveforms in an IC chip are some sort of characteristic waveform [11]–[13] rather than step waveforms, and the input signal waveform has a strong influence on delay times [14], the step-response models [2]–[8] are not accurate enough in characterizing the internal delay times of an IC.

In some modeling approaches [15], [16], the *RC* values used in a simplified gate model can be adjusted according to the input waveforms and the device operating regions to obtain a higher delay accuracy. This, however, leads to limited applicable ranges and numerical difficulties in optimization or design automation [10]. For efficient design automation, good analytical delay macromodels are required [10], [12], [13].

The third problem is on the initial delay. When a logic gate is excited by an input voltage, its output voltage shows a certain delay time before the suitable response occurs. This delay is called the initial delay [12], [13], which strongly affects the transient behavior of an interconnection line. Thus it has to be considered in modeling the interconnection delay.

Taking the above-mentioned effects into consideration, a new modeling technique is developed in this paper to accurately characterize the signal timing of small-geometry CMOS inverters with interconnection lines [17] for the above mentioned applications. In this modeling approach, the large-signal equivalent circuits of a logic gate and the lumped multisection *RC* ladder equivalent circuit of an interconnection line are considered together. The waveforms under characterization are of the non-step characteristic waveforms with the initial delay times. Using the mathematical linearization techniques, the analytical delay equations are derived and some fundamental transient behaviors are also explored. Through extensive comparisons with SPICE simulation results, it is shown that the maximum relative error of the developed model is below 16%. Circuit examples are also presented to demonstrate the applications of the developed model in timing verification.

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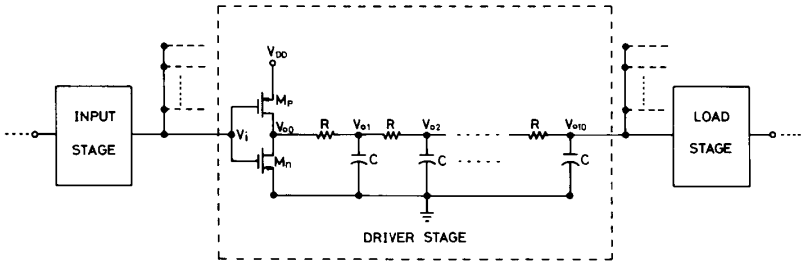

Fig. 1. A chain of identical CMOS inverters each with 10 sections of *RC* ladder interconnection network.

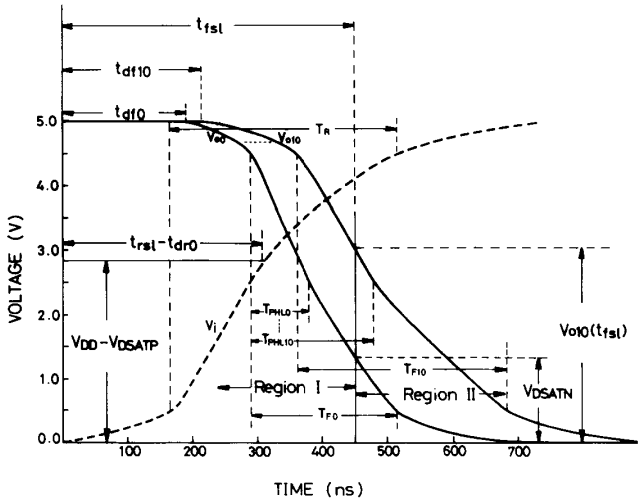

Fig. 2. Typical fall characteristic waveforms of a CMOS inverter with 10 sections of *RC* ladder network.

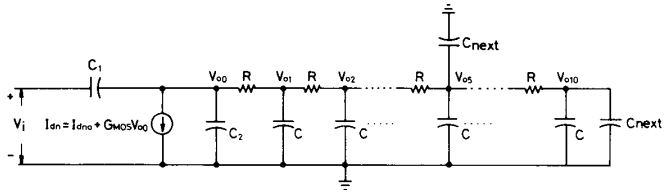

Fig. 3. Large-signal equivalent circuit of a CMOS inverter with 10 sections of *RC* ladder network during the fall-time period.

II. Timing Models

2-1. Waveform Generation, Timing Definition, and MOSFET Region Location

It has been shown in [2] that the ladder network with at least 10 lumped *RC* sections can be used to accurately simulate the behaviors of an interconnection line under various operating conditions. Consider a string of identical 1.5-μm CMOS inverters with interconnection lines represented by lumped *RC* ladder circuits as shown in Fig. 1, where the section number N of the *RC* ladder is 10. The typical characteristic waveforms obtained from SPICE simulations for the rising input voltage V_i and the falling output voltages V_{o0} and V_{o10} at the interconnection nodes 0 and 10, respectively, are plotted in Fig. 2. At any interconnection node j, the falling waveform of the node voltage V_{oj} has an initial time t_{dfj}, fall time T_{Fj}, and fall delay time T_{PHLj}, as indicated in Fig. 2.

If the fall time of the output voltage V_{o5} at the fifth interconnection node is to be characterized, the operating regions of the MOSFET's *Mp* and *Mn* and those in the load stage are first determined from their drain–source voltages V_{DS} and drain–source saturation voltages V_{DSAT}. According to the MOSFET operating regions, the falling waveform of V_{o5} during the fall-time period T_{F5} can be divided into Regions I and II as indicated in Fig. 2. In Region I, *Mp* is nearly off and *Mn* is saturated. In Region II, however, *Mp* is off and *Mn* is linear. For the load stage in both regions, its PMOS is saturated and the NMOS is linear.

On the waveform of V_{o0}, the boundary point between Regions I and II can be determined by letting $V_{o0}(=V_{DSN})$ be equal to the saturation voltage V_{DSATN} which can be calculated from the V_{DSAT} equation in the level-2 model of SPICE with the corresponding $V_i(=V_{GSN})$. The time period t_{fsl} during which the voltage $V_{o0}(t)$ lowers from V_{DD} to V_{DSATN} can then be calculated from the equation of $V_{o0}(t)$ to be derived later. From the calculated t_{fsl}, the corresponding boundary point on each voltage waveform can be found. In this way the voltage $V_{o5}(t_{fsl})$ of $V_{o5}(t)$ at the boundary point between Regions I and II can be calculated.

2-2. Large Signal Equivalent Circuit Generation and Current/Capacitance Linearization

The overall large-signal equivalent circuit during T_{F5} is given in Fig. 3 where the linearized equations of the drain current I_{dn} in Region I (saturation) and Region II (linear) are given in Table I. The linearized saturation drain current is obtained by using the lambda model [18] with a fixed value of the parameter λ. In Region I, this value is determined by the slope of the drain currents between $V_{o0}=V_{DSATN}$ and $V_{o0}=(V_{DD}+V_{DSATN})/2$ which is calculated from SPICE level-2 equations with the averaged value of V_{GSN} in this region. In Region II, the value of λ can be determined by the slope of the drain currents between $V_{o0}=0.0$ and $V_{o0}=V_{DSATN}/2$. As compared to SPICE simulations, the linearized drain current equation has a maximum error of 10 percent at the saturation-linear boundary.

The load capacitance C_{next} and the device capacitances C_1 and C_2 are all voltage-dependent. All the voltage-dependent capacitances as well as the voltage-dependent device parameters and the input voltage V_i in the drain current equation are further linearized by fixing their values at the linearization point. The linearization point in Region I is optimally determined at the center point with $t=t_{fse}$ where $V_{o0}(t_{fse})=(V_{DD}+V_{DSATN})/2$, whereas that in Region II is at the center point $t=t_{fle}$ where $V_{o0}(t_{fle})=V_{DSATN}/2$. The times t_{fse} and t_{fle} and the linearized input voltages $V_i(t_{fse})$ and $V_i(t_{fle})$ have their equations listed in Table I. Their derivations will be described later. After linearization, the equivalent circuit of Fig. 3 becomes a linear circuit.

2-3. Effective Dominant Pole Calculation

The S-domain nodal equations of the linearized large-signal equivalent circuit in Fig. 3 can be written in a matrix form as

$$\begin{bmatrix} S(C_1+C_2)+G_{MOS}+G & -G & 0 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ -G & SC+2G & -G & 0 & \cdots & \cdots & \cdots & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & 0 & -G & S(C+C_{next})+2G & -G & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & \cdots & \cdots & \cdots & 0 & -G & SC+2G & -G \\ 0 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & -G & S(C+C_{next})+G \end{bmatrix}_{11\times 11}$$

$$\cdot \begin{bmatrix} V_{o0}(S) \\ V_{o1}(S) \\ \cdots \\ V_{o5}(S) \\ \cdots \\ V_{o9}(S) \\ V_{o10}(S) \end{bmatrix}_{11\times 1} = \frac{1}{S} \begin{bmatrix} S(C_1+C_2)V_{o0}(0^-)-I_{dno} \\ SC\times V_{o1}(0^-) \\ \cdots \\ S(C+C_{next})V_{o5}(0^-) \\ \cdots \\ SC\times V_{o9}(0^-) \\ S(C+C_{next})V_{o10}(0^-) \end{bmatrix}_{11\times 1} + S \begin{bmatrix} C_1 \\ 0 \\ \cdots \\ 0 \\ \cdots \\ 0 \\ 0 \end{bmatrix}_{11\times 1} V_i(S) \tag{1}$$

where $V_{oj}(0^-)$ represents the initial voltage at the interconnection node j and $G=1/R$. The feedthrough current from the input node V_i to any output node is negligibly small so that the last term of (1) can be neglected. Then the voltage $V_{oj}(S)$ at any node can be solved from (1) and written as

$$V_{oj}(S)=\frac{(b_{11}S^{11}+b_{10}S^{10}+\cdots+b_2S^2+b_1S+1)b_0}{S(a_{11}S^{11}+a_{10}S^{10}+\cdots+a_2S^2+a_1S+1)a_0} \tag{2}$$

where b_i and a_i are positive and real coefficients which can be formulated from (1). Dividing the denominator by the numerator, we have

$$V_{oj}(S)=\frac{b_0}{a_0S[1+(a_1-b_1)S+(a_2-b_2-a_1b_1+b_1^2)S^2+\cdots]}. \tag{3}$$

The effective finite dominant pole of $V_{oj}(S)$ can be calculated from (3) as [19]

$$\frac{1}{p_{fj}}=\left[(a_1-b_1)^2-2\times(a_2-b_2-a_1b_1+b_1^2)\right]^{1/2}$$
$$=\left[(a_1^2-2\times a_2)-(b_1^2-2\times b_2)\right]^{1/2}. \tag{4}$$

In this expression, the second term in the square root represents the dominant zero. Since this method takes the dominant zero into consideration in finding the effective dominant pole and differs from the previously proposed dominant-pole-dominant-zero (DPDZ) method, it is called the modified DPDZ (MDPDZ) method. Using the MDPDZ method, the effective dominant poles in Regions I and II can be found similarly.

2-4. Voltage Waveform Function Calculation

Using the single-pole-response approximation in each region, the output voltage waveform at any interconnection node can be analytically expressed in terms of its initial delay, effective dominant pole, and initial and final voltages of Regions I and II. During the fall time period, the initial and final values of the output voltage waveform in Region I are V_{DD} and $-1/\lambda n$, respectively, as may be calculated from (2). However, in Region II they are $V_{oj}(t_{fsl})$ and 0 where $V_{oj}(t_{fsl})$ is the voltage of V_{oj} at the boundary point between Regions I and II, which will be formulated later. If the beginning point of the input voltage waveform is chosen as the origin of time axis, the output voltage

waveform $V_{oj}(t)$ at any interconnection node j can be expressed as

$$V_{oj}(t)=\begin{cases}\left(V_{DD}+\dfrac{1}{\lambda n}\right)e^{-P_{fsj}(t-t_{dfj})}-\dfrac{1}{\lambda n}, & t_{dfj}\leqslant t<t_{fsl}\ \text{(Region I)}\\ V_{oj}(t_{fsl})e^{-P_{flj}(t-t_{fsl})}, & t_{fsl}\leqslant t<\infty\ \text{(Region II)}\end{cases}\tag{5}$$

where P_{fsj} and P_{flj} represent the effective dominant poles in Regions I and II, respectively, at the interconnection node j; t_{dfj} is the initial delay at the interconnection node j as shown in Fig. 2.

From the waveform function $V_{o0}(t)$, the equations of t_{fsl}, t_{fse}, and t_{fle} as listed in Table I can be derived according to their definitions given in Sections 2-1 and 2-2. Substituting the expression of t_{fsl} into (5), all the output voltages $V_{oj}(t_{fsl})$ in (5) for $0\leqslant j\leqslant 10$ can be written as

$$V_{oj}(t_{fsl})=\left(V_{DD}+\frac{1}{\lambda n}\right)\times\left[\frac{V_{DSATN}+\dfrac{1}{\lambda n}}{V_{DD}+\dfrac{1}{\lambda n}}\right]^{P_{fsj}/P_{fs0}}-\frac{1}{\lambda n}.\tag{6}$$

2-5. Rise/Fall Time and Delay Time Formulation

From (5), the characteristic fall time T_{Fj} at any interconnection node j can be written as

$$T_{Fj}=\frac{1}{P_{fsj}}\ln\left[\frac{0.9V_{DD}+\dfrac{1}{\lambda n}}{V_{oj}(t_{fsl})+\dfrac{1}{\lambda n}}\right]+\frac{1}{P_{flj}}\ln\left[\frac{V_{oj}(t_{fsl})}{0.1V_{DD}}\right],\quad \text{if } V_{oj}(t_{fsl})\geqslant 0.1V_{DD}\tag{7}$$

$$T_{Fj}=\frac{1}{P_{fsj}}\ln\left[\frac{0.9V_{DD}+\dfrac{1}{\lambda n}}{0.1V_{DD}+\dfrac{1}{\lambda n}}\right],\quad \text{if } V_{oj}(t_{fsl})<0.1V_{DD}.\tag{8}$$

Similarly, the output voltage waveform during the rise time period and the characteristic rise time T_{Rj} at any interconnection node j can be expressed in terms of the initial delay t_{drj} and the effective dominant poles of the two regions.

In the calculation of T_{Fj}, V_i represents the rising characteristic input waveform which has also two different regions with different effective dominant poles. To formulate $V_i(t_{fse})$ and $V_i(t_{fle})$, single-pole-response approximation is used and $V_i(t)$ can be expressed as

$$V_i(t)=V_{DD}(1-e^{-P_{rk}t})\tag{9}$$

where

$$P_{rk}=\frac{1}{T_{Rk}}\ln(9.0).\tag{10}$$

In the above equations, P_{rk} is the characteristic rise pole at the interconnection node k. Substituting the expressions of t_{fse} and t_{fle} into (9), the equations of $V_i(t_{fse})$ and $V_i(t_{fle})$ in Table I can be derived. In these two equations, two empirical and universal constants are assigned to the pole-delay product $p_{r10}t_{df0}$ which has been proven to be a nearly constant physical parameter [12], [13].

TABLE I
THE LINEARIZED EQUATIONS OF THE NMOS DRAIN CURRENT I_{dn} IN REGIONS I AND II

$$I_{dn}(V_{GSN}=V_i,\ V_{DSN}=V_{o0}) = I_{dno}(1+\lambda n V_{o0}) = I_{dno}+G_{MOS}V_{o0}$$

Region I

$$G_{MOS}=\frac{I_{dn}(V_i(t_{fse}),(V_{DD}+V_{DSATN})/2)-I_{dn}(V_i(t_{fse}),V_{DSATN})}{(V_{DD}-V_{DSATN})/2}$$

$$I_{dno}=\frac{I_{dn}\left(V_i(t_{fse}),V_{DSATN}\right)\frac{V_{DD}+V_{DSATN}}{2}-I_{dn}\left(V_i(t_{fse}),\frac{V_{DD}+V_{DSATN}}{2}\right)V_{DSATN}}{\frac{V_{DD}-V_{DSATN}}{2}}$$

$$\lambda n=\frac{G_{MOS}}{I_{dno}}$$

Region II [12]

$$G_{MOS}=\frac{I_{dn}(V_i(t_{fle}),V_{DSATN}/2)-I_{dn}(V_i(t_{fle}),0.0)}{V_{DSATN}/2}$$

$$I_{dno}=0.0$$

$$\lambda n=\infty$$

$$t_{fsl}=t_{df0}+\frac{1}{P_{fs0}}\ln\left[\frac{V_{DD}+\frac{1}{\lambda n}}{V_{DSATN}+\frac{1}{\lambda n}}\right]$$

$$t_{fse}=t_{df0}+\frac{1}{P_{fs0}}\ln\left[\frac{V_{DD}+\frac{1}{\lambda n}}{\frac{1}{2}(V_{DD}+V_{DSATN})+\frac{1}{\lambda n}}\right]$$

$$t_{fle}=t_{df0}+\frac{1}{P_{fs0}}\ln\left[\frac{V_{DD}+\frac{1}{\lambda n}}{V_{DSATN}+\frac{1}{\lambda n}}\right]+\frac{1}{P_{fl0}}\ln(2)$$

$$V_i(t_{fse})=V_{DD}\left\{1-e^{-P_{r10}t_{df0}\left[\frac{\frac{1}{2}(V_{DD}+V_{DSATN})+\frac{1}{\lambda n}}{V_{DD}+\frac{1}{\lambda n}}\right]^{P_{r10}/P_{fs0}}}\right\}$$

$$P_{r10}t_{df0}=0.6$$

$$V_i(t_{fle})=V_{DD}\left\{1-e^{-P_{r10}t_{df0}\left[\frac{V_{DSATN}+\frac{1}{\lambda n}}{V_{DD}+\frac{1}{\lambda n}}\right]^{P_{r10}/P_{fs0}}2^{-P_{r10}/P_{fl0}}}\right\}$$

$$P_{r10}t_{df0}=0.6$$

Through $V_i(t_{fse})$ and $V_i(t_{fle})$, T_{Fj} becomes a function of T_{Rk} and vice versa. Simple iterations are required to solve T_{Fj} and T_{Rk}. Usually the resulting iteration number is less than 5.

According to the delay definition in Fig. 2, the rise propagation delay T_{PLHj} and fall propagation delay T_{PHLj} between the input node k and any output interconnection node j can be expressed as

$$T_{PLHj}=t_{drj}+T_{ROj}-T_{FOk}\tag{11}$$

$$T_{PHLj}=t_{dfj}+T_{FOj}-T_{ROk}\tag{12}$$

where T_{ROj} (T_{ROk}) stands for the time interval during which $V_{oj}(t)$ ($V_{ok}(T)$) rises from 0 to $0.5V_{DD}$ at the interconnection node j (k), and T_{FOj} (T_{FOk}) for the time interval during which $V_{oj}(t)$ ($V_{ok}(t)$) lowers from V_{DD} to $0.5V_{DD}$.

For simplicity, empirical laws for the initial delay times t_{drj} and t_{dfj} were found. As a result, the rise propagation delay T_{PLHj} and fall propagation delay T_{PHLj} at any interconnection node j can be reformulated by the simple relations

$$T_{PLHj}=(0.1152T_{ROj}-0.0211T_{FOj}+0.5465T_{FOk})+T_{ROj}-T_{FOk},\quad j=0,1,2,\cdots 10;\ k=10\tag{13}$$

$$T_{PHLj}=(0.3538T_{FOj}-0.2346T_{ROj}+0.5962T_{ROk})+T_{FOj}-T_{ROk},\quad j=0,1,2,\cdots 10;\ k=10.\tag{14}$$

Note that the above equations are universal and can be used to calculate the delay times under various conditions with satisfactory accuracy.

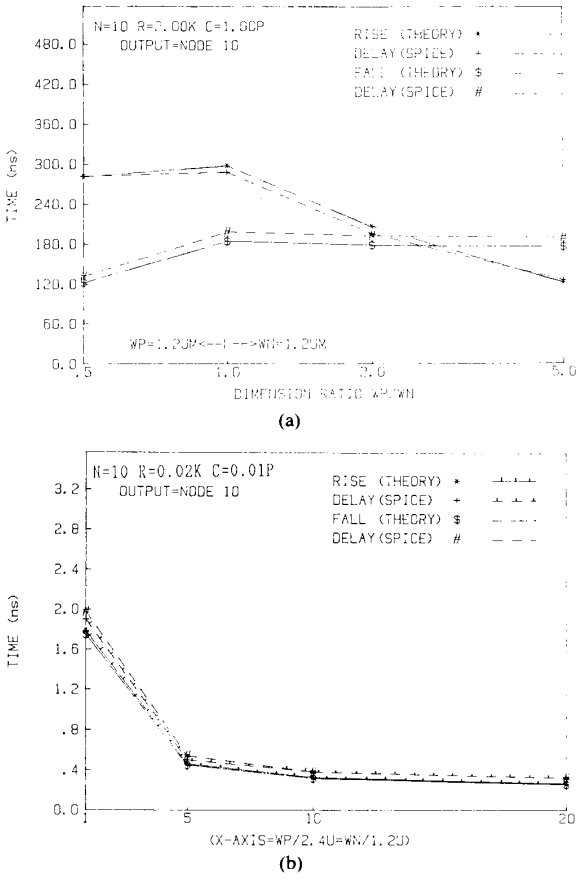

Fig. 4. (a) Calculated and simulated rise/fall delay as a function of channel width ratio for 1.5-μm CMOS inverters with 10-section R(2.0 kΩ)C(1.0 pF) ladders. (b) Calculated and simulated rise/fall delay as a function of Wp/2.4 μm or Wn/1.2 μm for 1.5-μm CMOS inverters with 10-section R(0.02 KΩ)C(0.01 pF) ladders.

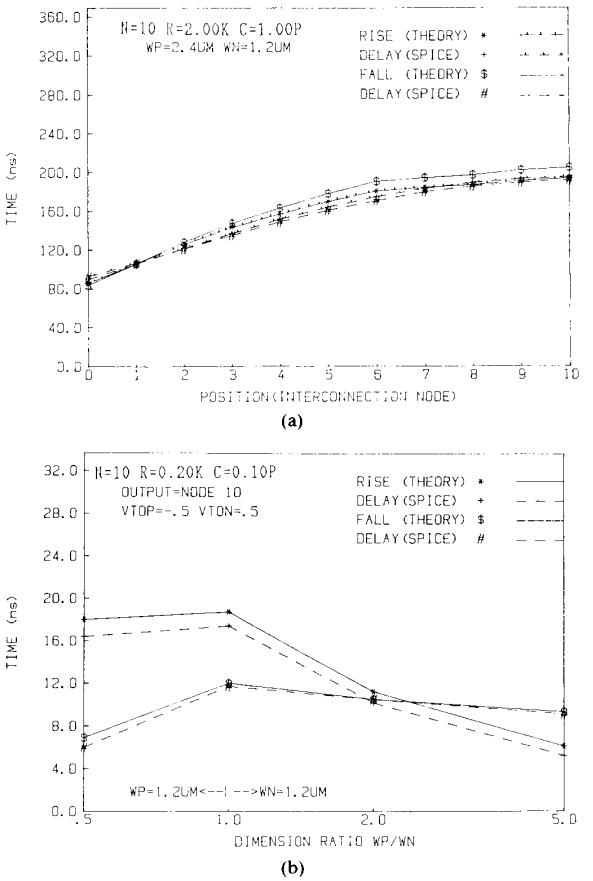

Fig. 5. (a) Calculated and simulated rise/fall delay as a function of interconnection node positions for 1.5-μm CMOS inverters with 10-section R(2.0 kΩ)C(1.0 pF) ladders. (b) Calculated and simulated rise/fall delay for 1.5-μm CMOS inverter with 10-section R(0.2 kΩ)C(0.1 pF) ladders and reduced threshold voltages V_{TOP} and V_{TON}.

III. Comparison with SPICE Simulations

To verify the accuracy of the developed analytical delay models, extensive comparisons between theoretical calculations and SPICE simulations were made for CMOS inverters with RC ladder interconnection networks of different RC values and section numbers N, different gate sizes, device parameters, and even input excitations. Part of the comparisons are shown in Fig. 4(a) for the delay times of CMOS inverters with 10-section RC ladder interconnection network ($R = 2.0$ kΩ and $C = 1.0$ pF). It is shown that the maximum relative error in the delay times is 16 percent for CMOS inverters with different channel width ratios. Similar comparisons for the inverters with different size factors from 1 to 20 are shown in Fig. 4(b). The error characteristics are still the same. Since the delay times are expressed by equations in the developed model, the CPU time consumed in the delay calculation is about two orders of magnitude smaller than that in point-by-point full transient analysis in SPICE.

The accuracy of the timing models in calculating the signal timing at every interconnection node under device parameter variations was also investigated. Fig 5(a) shows the calculated and the simulated rise/fall delay times at all interconnection nodes for inverters with 10-section equivalent R(2.0 kΩ)C(1.0 pF) ladder network. Fig. 5(b) shows the delay times at the tenth interconnection node for inverters with different width ratios and reduced threshold voltages V_{TOP} and V_{TON}. All the comparisons show the same relative error characteristics.

Although a 10-section RC ladder is enough to characterize the interconnection delay [2], the developed model can be applied to the cases where the interconnection line is represented by a N-section lumped RC ladder with N greater than 10. The relative error is still the same.

IV. Applications

As mentioned in the previous section, the developed model equations contain the constant product of the input pole and the initial delay. Moreover, the output fall(rise) time is a function of the input rise(fall) time. Through these relations, the input waveform effect has been implicitly incorporated into the model. Thus it can be applied to noncharacteristic waveform cases where the input may be a step voltage or has a waveform two times slower in rise/fall times than the characteristic waveform. The general relative errors for the delay times are still below 16 percent. The ability to calculate the noncharacteristic waveform timing makes the developed timing models more practical and versatile.

Consider a string of 7 identical 1.5-μm CMOS inverters each with a 10-section RC ladder interconnection network. The first

TABLE II
THE CALCULATED AND SIMULATED SIGNAL TIMING FOR A STRING OF IDENTICAL 1.5-μm CMOS INVERTERS EACH WITH A 10-SECTION *RC* LADDER INTERCONNECTION NETWORK

Stage Number	Data Type	T_R(ns) or T_F(ns)	T_{PLH}(ns) or T_{PHL}(ns)	Total Delay
1	THEORY	17.0	9.37	9.37
	SPICE	17.6	8.4	8.4
	ERROR	-3.4%	+11.5%	+11.5%
2	THEORY	17.6	12.3	21.67
	SPICE	18.25	12.4	20.8
	ERROR	-3.6%	-0.8%	14.2%
3	THEORY	21.73	12.78	34.45
	SPICE	20.4	12.5	33.3
	ERROR	+6.5%	+2.2%	+3.5%
4	THEORY	18.6	12.6	47.05
	SPICE	18.5	12.6	45.9
	ERROR	+0.5%	0.0%	+2.5%
5	THEORY	21.8	12.8	59.85
	SPICE	20.65	12.4	58.3
	ERROR	+5.6%	+3.2%	+2.7%
6	THEORY	18.7	12.6	72.45
	SPICE	-18.5	12.6	70.9
	ERROR	+1.1%	0.0%	+2.2%
7	THEORY	21.6	12.7	85.15
	SPICE	20.4	12.2	83.1
	ERROR	+5.9%	+4.1%	+2.5%

Condition: L_{mask}=1.5UM W_P=2.4UM W_N=1.2UM N=10
R = 0.20KΩ C = 0.10PF OUTPUT=NODE 10

stage is driven by a falling step-input voltage and the accumulated delay at the tenth interconnection node in each stage is to be calculated by using the developed model as an application example. Table II shows the calculated and the simulated results where the relative error in the total delay is as small as 2.5 percent.

V. CONCLUSION

Physical delay models for CMOS inverters with *RC* ladder interconnection networks have been developed successfully. Based upon this modeling technique, the delay models of various CMOS static logic gates with interconnection trees as well as the applications of the models in auto-sizing and optimization are now under development.

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A Realization Method of Two-Dimensional Rational Transfer Functions

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***Abstract*—In this paper, we propose a method for realizing the two-dimensional transfer functions (TDTF). By using our method, realizations can be directly obtained from the coefficients of the TDTF, without performing canonical decomposition of the state equations and solving nonlinear equations. Consider the possibility of reducing the realization dimension in our realization method, and obtain conditions imposed on the TDTF for the reduction. Moreover, we present a class of TDTF that can be realized with a minimal dimension with respect to both of the two variables.**

I. INTRODUCTION

The transfer characteristics of two-dimensional digital systems, mixed lumped and distributed networks, networks containing variable parameters, delay-differential systems, and systems with time delays, can all be approximately expressed by two-dimensional rational transfer functions.

A method for constructing the special class of mixed lumped and distributed networks was reported in the past [1]. It is a very effective method in the case of special network functions, but it cannot be applied to the case of general two-dimensional transfer functions (TDTF).

Various studies have also been done on the realization problem of a separable-denominator TDTF [2]–[7]. However, they cannot be applied to the case of general TDTF, similarly.

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