

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

具電場增強式奈米線結構之複晶矽薄膜
電晶體非揮發性記憶體之研究

The logo of National Central University (NCU) is a circular emblem. It features a central figure of a person holding a torch, with a banner below it containing the year '1896'. The emblem is surrounded by a gear-like border.

**Study on the Poly-Si TFT Nonvolatile Memory
with a Field-Enhanced-Nanowire Structure**

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中華民國 九十八 年 七 月

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多晶矽薄膜電晶體在過去已經廣泛地被使用在顯示面板上。為了未來更進一步系統面板的整合應用，在資料儲存、訊號處理以及可攜帶式系統的減少功率方面都必須去研發多晶矽的非揮發性記憶體技術。由於與多晶矽薄膜電晶體製程匹配性較好的原因，矽氧氮氧矽(SONOS)非揮發性記憶體比傳統的懸浮式閘極(floating gate)非揮發性記憶體在未來系統面板的應用上要來的更有潛力。然而，SONOS非揮發性記憶體有寫入與抹除速率比懸浮式閘極非揮發性記憶體慢的缺點。為了改善這個缺點，在本論文中我們提出具電場增強式奈米線結構之複晶矽薄膜電晶體的SONOS非揮發性記憶體(FEN POAT SONOS)以及以真空取代穿隧氧化層(tunneling oxide)的具電場增強式奈米線結構之複晶矽薄膜電晶體的矽氧氮真空矽(FEN POST SONVAS)非揮發性記憶體去提升寫入、抹除速率以及改善

元件的可靠度。

在第二章中，我們利用一種簡單且低成本的方式製作出具電場增強式奈米線結構之複晶矽薄膜電晶體的SONOS非揮發性記憶體(FEN POST SONOS)。在製作過程中我們利用間隙壁技術(Spacer Technique)來製作奈米通道而不需要用先進的微影技術。由於電場增強式的奈米線結構能有效的提升穿隧氧化層的電場同時降低阻擋氧化層 (blocking oxide) 電場，因此能有效的提高寫入、抹除速率。我們提出的FEN POST SONOS非揮發性記憶體與傳統平面式SONOS (CP SONOS)比起來擁有較好的記憶體特性。FEN POST SONOS非揮發性記憶體在閘極電壓+15 V的寫入以及-15 V的抹除分別可以在一毫秒得到2.71 V和2.11 V (0.49 V和-0.32 V for CP SONOS) 臨界電壓的改變。在可靠度方面，我們提出的FEN POST SONOS非揮發性記憶體在經過十年之後能保持1.1 V的記憶窗(memory window)的保持力(retention)以及在經過一萬次的寫入與抹除的操作下仍擁有1.68 V的記憶窗的耐久性(endurance)。

在第三章中，我們提出了另一種以真空取代穿隧氧化層的FEN POST SONVAS非揮發性記憶體結構去更進一步提升前面所提出的FEN POST SONOS非揮發性記憶體的耐久性。此外，由於真空的低介電係數特性能更有效的提升穿隧層(tunneling layer)的電場，我們提出的FEN POST SONVAS非揮發性記憶體也表現出比先前所提的FEN POST SONOS非揮發性記憶體擁有更好的寫入與抹除效率。我們提出的FEN POST SONVAS非揮發性記憶體在閘極電壓+15 V的寫入和-15 V的抹除分別可以在一毫秒得到3.17 V和2.68 V臨界電壓的改變。在可靠度方面，我們提出的FEN POST SONOS非揮發性記憶體在經過十年之後能保持1.4 V的記憶窗(memory window)的保持力(retention)以及在經過一萬次的寫入與抹除的操作下仍擁有2.4V的記憶窗並且只有0.5 V的記憶窗位移的耐久性(endurance)。

最後，一個簡短的總結。我們提出的FEN POST SONOS和FEN POST SONVAS非揮發性記憶體在未來的系統面板和三維立體積體電路上都有很大的發展潛力。

Study on the Poly-Si TFT Nonvolatile Memory with a Field-Enhanced-Nanowire (FEN) Structure

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Polycrystalline silicon thin film transistors (poly-Si TFTs) have been widely used as pixel switching elements in active-matrix displays. For further achieving system-on-panel (SOP) applications, nonvolatile memory (NVM) based on poly-Si TFT technology are also needed to develop for data storage, signal processing, and power saving in a portable electronic system. And, due to the process compatibility with poly-Si TFT, silicon-oxide-nitride-oxide-silicon (SONOS)-type devices, instead of traditional floating-gate ones, have been considered as a promising NVM candidate for SOP applications. However, the program/erase efficiency of SONOS-type memory is lower than traditional floating-gate memory. To resolve this issue, we proposed a field-enhanced-nanowire Poly-Si TFT SONOS (FEN POST SONONS) and a field-enhanced-nanowire Poly-Si TFT

silicon-oxide-nitride-vacuum-silicon (FEN POST SONVAS) structure, which tunneling oxide was replaced with vacuum, to improve the program/erase efficiency and reliability.

In chapter 2, a simple and low-cost method was used in fabricating the FEN POST SONOS devices. The spacer technique was used to form the nanowire channels without any advanced lithography. The fabricated FEN POST SONOS exhibited excellent electrical performance as compared with conventional planar TFT SONOS (CP SONOS) due to much enhanced electric field in the tunneling layer and lower electric field in the blocking oxide as compared to CP SONOS. The FEN POST SONOS exhibited a V_{th} shift of 2.71 V and 2.11 V (0.49 V and -0.32 V for CP SONOS) at $V_{GS} = +15/-15$ V in 1 ms for FN programming and erasing operations, respectively. In addition, the proposed FEN POST SONOS exhibited 1.1V memory window of retention after ten years and 1.68V memory window of endurance after 10^4 P/E cycles.

In chapter 3, a novel FEN POST silicon-oxide-nitride-vacuum-silicon (FEN POST SONVAS), which tunneling oxide was replaced with vacuum, was fabricated to improve the reliability of FEN POST SONOS. In addition, the FEN POST SONVAS also showed better P/E efficiency than FEN POST SONOS due to low-k property can enhance the electric field in the vacuum tunneling layer. The FEN POST SONVAS exhibited a V_{th} shift of 3.17 V and 2.68 V at $V_{GS} = +15/-15$ V in 1 ms for FN programming and erasing operations, respectively. For reliability, the proposed FEN POST SONOS exhibited 1.4 V memory window of retention after ten years and 2.4 V memory window and only 0.5 V window shift of endurance after 10^4 P/E cycles.

At last, conclusions have been briefly summarized. The proposed FEN POST SONOS and FEN POST SONVAS are very promising for the future applications in SOP and 3-D ICs.

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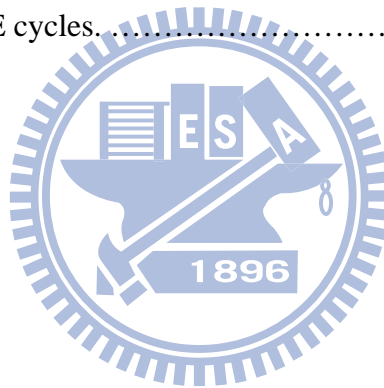


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Chapter 1

Introduction

1-1. Introduction of the Polycrystalline Silicon Thin-Film Transistor

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have attracted much attention because of their applications in active matrix displays, such as active matrix liquid crystal displays (AMLCDs) [1] and active matrix organic light emitting displays (AMOLEDs) [2], and potential for the application on three- dimension integrated circuits (3-D ICs). In recent years, the high performances of poly-Si TFTs also have been demonstrated by scaling down device dimensions or utilizing novel crystallization technologies to enhance poly-Si film quality [3, 4]. This provides opportunity of using poly-Si TFTs in integrated peripheral driving circuits.

The possibility of integrating driving circuitry as well as switching devices on the same substrate represents a major advantage of the polysilicon technology over the amorphous silicon, because the mobility of poly-Si TFTs is usually large than 10 $\text{cm}^2/\text{V}\cdot\text{s}$, that is higher than amorphous Si TFTs and enough for peripheral driving circuits with n- and p-channel devices. So, the pixel array and the peripheral circuits can be made on the same glass substrate [5-7], a potential system-on-panel (SOP) technology. In addition, due to higher mobility, the poly-Si TFTs can be made smaller compared to that of the amorphous Si TFTs.

In CMOS technology, many high-performance multiple gates structures in a silicon-on-insulator (SOI) MOSFET, such that double-gate [8], tri-gate [9], FinFET

[10] and gate-all-around [11], have been reported to exhibit superior gate control over the channel than a conventional single-gate MOSFET and reduced short-channel effects.

1-2. Introduction of the SONOS Nonvolatile Memory Devices

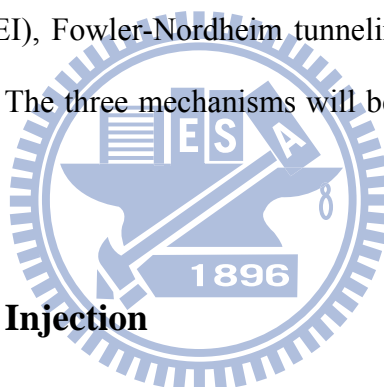
1-2-1. The SONOS Nonvolatile Memory Devices

It is well known that the nonvolatile memory is widely utilized for data storage in portable electronic systems due to its properties of low power consumption and nonvolatility. The conventional floating gate (FG) memory (shown in Fig. 1-1) employed poly-Si film as a charge-storage layer that can achieve high-density integration and good program/erase (P/E) speed; however, there are some concerns regarding the capability to scale down the tunneling dielectric thickness [12]. When the tunneling oxide thickness is below 10 nm, the storage charges in the floating gate lose easily through defects created in the tunneling oxide after repeated P/E cycles [13]. The poly-Si–oxide–nitride–oxide–silicon (SONOS)-type structure memories (shown in Fig. 1-2) have been investigated as an approach to solve the issue of scaling FG memory [14]. Due to their spatially isolated deep-level traps, SONOS memories exhibit better charge retention than FG memories that have a bitcell tunneling oxide thickness less than 10 nm. Consequently, a single defect in the tunneling oxide will not lead to the discharge of the memory cell. However, many concerning issues are still presented for SONOS memories. For SONOS memories, erase saturation and

vertical stored charge migration [15, 16] are the major drawbacks. In addition, it is very difficult to promote the P/E speed and data retention simultaneously. In recent years, different device structures [17, 18] and alternating materials [19-21] have been explored to improve the P/E speed and data retention at the same time.

1-2-2. Program/Erase Mechanisms of SONOS Nonvolatile Memory

In general, the program/erase mechanisms employed in SONOS include channel hot electron injection (CHEI), Fowler-Nordheim tunneling (FN tunneling) and band to band tunneling (BTBT). The three mechanisms will be illustrated in the following sections.



Channel Hot Electron Injection

The channel hot electron injection can be well described by “lucky-electron model” [22]. The injection of channel hot electrons into the gate oxide region occurs at large drain-to-source voltage, as shown schematically in Fig. 1-3. Electrons which flow from source to drain gain energy from the high-field region near the drain junction. Because the effective mass of hole is heavier than the electron, in addition, and the barrier height of valence band is also higher than the conduction band, it is much more difficult for holes to obtain enough energy to surmount the oxide barrier. Therefore, hot-hole injection is rarely employed in nonvolatile memory operation. A merit of CHEI mechanism is to achieve NROM [23], SONOS with 2Bit/Cell. By employing CHEI, the charge can be programmed into drain or source terminals

respectively, then the data can be sensed by “reverse read”.

Fowler-Nordheim Tunneling

The tunneling mechanism is a kind of quantum-mechanical process during which the carriers may tunnel through the forbidden region of the insulator into the allowed states of the insulator or the opposite electrode material. Due to different electric field strength across the insulator, the tunneling mechanism can be classified into direct tunneling and FN tunneling. If the electric field strength across the tunneling oxide (E_{ox}) is smaller than $\frac{q\phi_1}{t_{ox}}$, where $q\phi_1$ is the barrier height between Si channel and tunneling oxide, the carriers may tunnel into nitride trapping layer by direct tunneling. The current density is expressed as:

$$J = AE_{ox}^2 \left(\frac{\phi_1}{V_{ox}} \right) \left(\frac{2\phi_1}{V_{ox}} - 1 \right) e^{-B \left[1 - \left(\frac{V_{ox}}{\phi_1} \right)^2 \right]^{3/2}} \dots\dots\dots(1-1)$$

where $A = \frac{q^3 E^2}{8\pi h \phi_1}$, $B = \frac{8\pi \sqrt{2m_{ox}} \phi_1^2}{3hq}$, and the electron effective mass, m_{ox} , is $0.5m_0$.

Direct tunneling is illustrated in Fig. 1-4(a).

If $E_{ox} > \frac{q\phi_1}{t_{ox}}$, the carriers may tunnel into nitride trapping layer by FN tunneling.

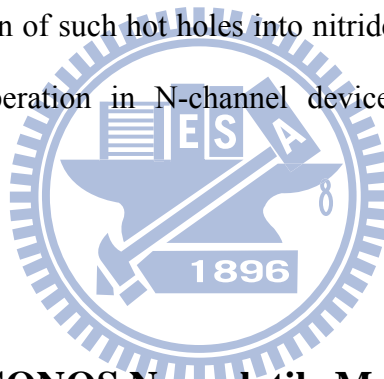
The current density is expressed as:

$$J = AE_{ox}^2 e^{-\frac{B}{E_{ox}}} \dots\dots\dots(1-2)$$

FN tunneling is illustrated in Fig. 1-4(b) [24, 25].

Band to Band Tunneling

In N-channel devices, when a negative gate voltage and a positive drain voltage are applied to the cell, electron-hole pairs are generated by BTBT in the n^+ drain region [1.25]. The phenomenon of BTBT occurs in the n^+ drain region overlapping the gate. The strength of electric field in the region must be sufficiently high to cause deep-depletion situation. During the operation, electrons tunnel directly or are assisted by traps in the gap from valence band to conduction band at the drain region. At the same time, holes are generated in the deep-depletion region, and are then accelerated by the strong field and may be attracted by the negative gate bias into the nitride trapping layer. The injection of such hot holes into nitride through the tunnel oxide is used for a new erase operation in N-channel devices [26]. The processes are illustrated in Fig. 1-5.



1-2-3. Reliability of SONOS Nonvolatile Memory

Retention

Retention is a measure of the time that a nonvolatile memory cell can retain the charge in the trapping layer. In nonvolatile memory technology, it is essential to retain data for over ten years. This means the loss of charge stored in the storage medium must be as minimal as possible. Figure 1-6 shows the band diagram for illustrating the charge loss paths in SONOS cells. There are two major leakage current components in relating to charge loss, one is the thermionic emission following Frenkel-Poole mechanism, another one is tunneling through tunneling oxide. The tunneling

mechanisms include trap-to-band (T-B) tunneling, trap-to-trap (T-T) tunneling, and band-to-trap (B-T) tunneling. The trapped electrons in nitride can tunnel back to the conduction band of the silicon substrate (T-B tunneling), or to the interface traps between tunneling oxide and channel (T-T tunneling). In addition, holes from the silicon valence band may tunnel into the nitride traps under the influence of the internal electric field (B-T tunneling).

Endurance

Endurance is the ability of a nonvolatile memory to endure the damage of numerous cycles of programming and erasing, i.e., the number of erase/write cycles that the memory will retain the required memory window and continue to operate as specified in the initial data window. Since the carriers for programming and erasing have energy, they will cause the degradation of tunneling oxide and trapping layer in every operation. In addition, high electric field stress across tunneling oxide will increase the current density at low electric field. The excess current at low electric field after stress is called stress-induced leakage current (SILC) [27]. SILC is attributed to stress-induced oxide defects, which lead to a trap assisted tunneling.

1-3. Motivation

Recently, the high performance poly-Si TFTs were demonstrated to be integrated with peripheral driving circuits [28]. For further achieving system-on-panel (SOP) applications, other functional elements based on poly-Si TFT technology, such as

memories, sensors, drivers, and controllers, are also needed to develop to fully integrate on the same display panel [29-31]. It is well-known that the nonvolatile memory (NVM) is a critical element for data storage, signal processing, and power saving in portable electronic systems [32]. Furthermore, due to the process compatibility, poly-Si TFT silicon-oxide-nitride-oxide-silicon (TFT SONOS) devices, instead of floating-gate type ones, have been considered as a promising candidate NVM for the realization of SOP electronics. However, unlike floating-gate type NVM, conventional planar TFT SONOS (CP SONOS) memories do not have gate-coupling design, thus suffering from the insufficient programming/erasing (P/E) efficiency. To improve this issue, poly-Si protrusion tips, produced by sequential lateral solidified (SLS) crystallization, and nanowire TFT SONOS with a tri-gate structure produced by e-beam lithography have been reported to enhance the electric field to improve the P/E efficiency [33, 34]. However, for SLS method, the location and height of the protrusion tips may be difficult to control. The uniformity of devices may be serious issue. For nanowire by e-beam lithography method, the e-beam lithography is a expensive and slow process, so the cost and throughput are also issues. In this thesis, a field-enhanced nanowire poly-Si TFT SONOS (FEN POST SONOS) with a gate-all-around (GAA) structure and a field-enhanced nanowire poly-Si TFT silicon-oxide-nitride-vacuum-silicon (FEN POST SONVAS) with a gate-all-around (GAA) structure are proposed with a simple process sequence to improve the P/E efficiency and reliability. Using the sidewall spacer method, etch nanowire channel has three sharp corners and the uniformity issue can be suppressed because the size of nanowire channel can be controlled easily by adjusting the relative ion etch (RIE) time. With a GAA structure, the FEN POST SONOS device also has better transistor performance than CP SONOS device due to better gate control ability. So it is a promising candidate for future high density circuits and SOP applications.

1-4. Thesis Organization

In chapter 1, brief introductions of poly silicon TFTs and SONOS nonvolatile memory (NVM) are given to explain the significance and potential of poly silicon TFTs and SONOS nonvolatile memory for future system on panel applications. Then, basic mechanisms of SONOS NVM are illustrated and the motivations of this work are subsequently explained to introduce this thesis.

In chapter 2, the fabrication sequences of FEN POST SONOS memory with a gate-all-around structure are illustrated. The important processes are analyzed by scanning electron microscope (SEM) and transmission electron microscope (TEM). And, the electrical characteristics of FEN POST SONOS are investigated.

In chapter 3, the fabrication sequences of FEN POST SONVAS memory with a gate-all-around structure are illustrated. The important processes are analyzed by scanning electron microscope (SEM). And, the electrical characteristics of FEN POST SONAS are investigated.

Finally, the summary and conclusions are given in chapter 4.

Chapter 2

Field-Enhanced-Nanowire Poly-Si TFT SONOS (FEN POST SONOS) Memory with a Gate-All-Around Structure

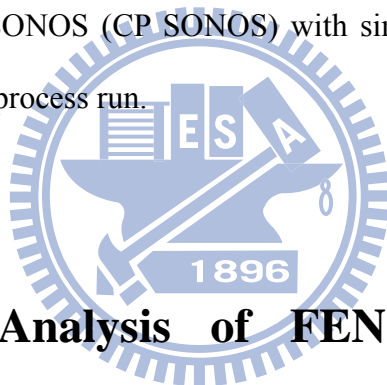
2-1. Introduction

In recent years, poly-Si thin film transistors (TFTs) have been widely used as pixel switching elements in active-matrix displays. For further achieving system-on-panel (SOP) applications, other functional elements based on poly-Si TFT technology, such as memories, sensors, drivers, and controllers, are also required to fully integrate on the same display panel [35-39]. It is well-known that the nonvolatile memory (NVM) is a critical element for data storage, signal processing, and power saving in portable electronic systems [40]. Silicon-oxide-nitride-oxide-silicon (SONOS) flash memory has been investigated to realize vertical scaling of flash memory. The faster programming speed and lower operating voltage of SONOS devices were accomplished in the past by reducing the tunnel-oxide thickness [41-44]. However, this seriously degrades the retention capability of the memory devices. Several efforts have been made to improve the retention time of SONOS devices. And, due to the process is compatible with poly-Si TFT, silicon-oxide-nitride-oxide-silicon (SONOS)-type devices, instead of traditional floating-gate ones, have been considered as a promising nonvolatile memory candidate for future System on Panel (SOP) applications [45-47].

2-2. Fabrication Sequences of FEN POST SONOS Memory with a Gate-All-Around Structure

The fabrication steps of field-enhanced-nanowire poly-Si TFT SONOS (FEN POST SONOS) with gate-all-around (GAA) structure devices are schematically shown in Fig. 2-1. At first, a 50-nm-thick Si_3N_4 (as etch-stop layer) and a 300-nm-thick tetra-ethyl-ortho-silicate (TEOS) SiO_2 (as sacrificial layer) films were sequentially deposited on oxidized silicon wafer by low pressure chemical vapor deposition (LPCVD) system at 580 °C and 700 °C, respectively. Several strips with step height of 100-nm as shown in Figs. 2-1(a) and 2-1(b) were patterned on surface of the sacrificial SiO_2 layer by reactive ion etch (RIE), and followed by a conformal deposition of 100-nm-thick a-Si layer by LPCVD at 550 °C. After source/drain (S/D)-pad lithography and its RIE process, couples of spacer nanowires were in-situ resided against the sidewall of those designed strips and naturally connected to the S/D pads as shown in Figs. 2-1(c) and 2-1(d), which were formed to be the device active region. It should be noted that each spacer nanowire inherently features three sharp corners, and the nano-scale dimension of the nanowire channels can be defined only by controlling the RIE time without any advanced lithography [48-50], each dummy strip produces twin nanowire channels, as well as the multiple channels can be designed with patterning several dummy strips (n strips \times 2 wires/strip = $2n$ wires). Subsequently, a solid phase crystallization (SPC) at 600 °C in N_2 ambient for 24 hours was performed to transform the a-Si into poly-Si. After that, the suspending channels were formed by etching the sacrificial SiO_2 layer with 3:50 diluted HF, and the etching-stopper layer would stop etching process down to the buried oxide as shown in Figs. 2-1(e) and 2-1(f) in the tilted and cross-section views, respectively. Then,

a 5-nm-thick tunneling oxide, a 10-nm-thick nitride trap layer, a 10-nm-thick blocking oxide, and a 200-nm-thick phosphorous in-situ doped poly-Si were sequentially deposited conformally to wrap around those suspending spacer nanowires by LPCVD systems. The poly gate was defined as shown in Figs. 2-1(g) and 2-1(h) in the tilted and cross-section views, respectively, and a phosphorous ion implantation was performed with a dosage of $5 \times 10^{15} \text{ cm}^{-2}$ and a energy of 30 keV. Then, a 300-nm-thick passivation oxide deposition and S/D activation were sequentially performed. The contact holes were patterned to etch the passivation layer by RIE and the Al metal layer was deposited by sputter system. Finally, the Al metal layer were patterned and etched by RIE to complete the fabrication. For the purpose of comparison, the conventional planar TFT SONOS (CP SONOS) with single top-gate structure were also fabricated at the same process run.



2-3. Materials Analysis of FEN POST SONOS Memory with a Gate-All-Around Structure

The previous section briefly describes the process sequence of the FEN POST SONOS. In this section, the scanning electron microscope (SEM) and transmission electron microscope (TEM) have been used to analyze the detailed process parameter in the fabrication of FEN POST SONOS.

Figures 2-2(a) and 2-2(b) show the SEM images before and after sacrificial oxide stripping by HF acid, respectively. And, Figs. 2-2(c) and 2-2(d) show their corresponding schematic images. It can be shown that the sacrificial SiO_2 layer has been removed and there are two suspending nanowires remained after oxide stripping.

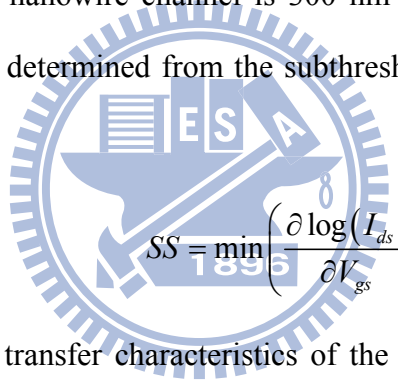
Figures 2-3(a) and 2-3(b) show the tiled-view SEM image and the corresponding schematic image of the multiple suspending nanowire channels after HF etching. Different channel width can be easily designed by adjusting the number of sacrificial SiO₂ strips. The cross-section view SEM image and the corresponding schematic image of the suspending channels are shown in Figs. 2-4(a) and 2-4(b), respectively. The multiple nanowire channels are hung in the air with a height 200 nm above the Si₃N₄ etch-stop layer and connected to the source and drain pads. With the aid of the suspending nanowire channels, the ONO dielectric layers and poly gate deposited by LPCVD can be easily surrounding the channel to form the GAA structure. Figures 2-5(a) and 2-5(b) show the top view SEM image and the corresponding schematic image after patterning gate, respectively. It should be noted that there are residual bottom gates remained below the source/drain extensions after gate patterning. The source/drain extensions shield (prevent) the residual bottom gates from the anisotropic RIE. Figure 2-6 exhibits the cross-section TEM image of each gate-all-around nanowire and shows the ONO dielectrics and poly gate which were conformally deposited on the three sharp corners. The polycrystalline nanowire channel in the center of graph is formed by the TCP-RIE and the dimension of nanowire is precisely controlled by etching time. The TEM image shows that the vertical sidewall thickness, the horizontal width and bevel length of each NW channel are about 85 nm, 85 nm and 130 nm, respectively. Thus the total surrounding width of each NW channel is 300 nm.

2-4. Results and Discussions

The constant drain current method is used to determinate the threshold voltage. The threshold voltage (V_{th}) is defined as the gate voltage required to achieve a normalized drain current as 10nA at $V_{ds}=0.1$ V

$$V_{th} = V_{gs} @ I_{ds} = \frac{W}{L} \times 10nA \dots\dots\dots(2-1)$$

where the W and L are the channel width and length, respectively. It should be noted that the channel width of FEN POST SONOS is defined as $0.6n \mu m$ ($W = n \text{ strips} \times 2 \text{ wires/strip} \times 300 \text{ nm/wire} = 0.6n \mu m$), where the n is the number of dummy strip. The surrounding width of each nanowire channel is 300 nm as shown in Fig. 2-6. The subthreshold swing (SS) is determined from the subthreshold region of I_{ds} - V_{gs} curve at $V_{ds}=0.1$ V.



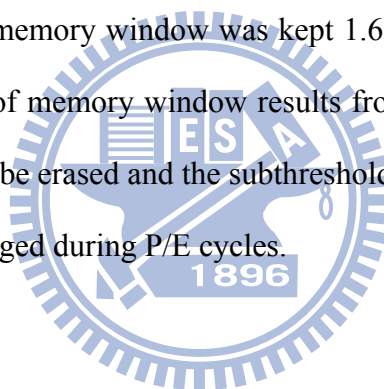
$$SS = \min \left(\frac{\partial \log(I_{ds})}{\partial V_{gs}} \right)^{-1} @ V_{ds} = 0.1V \dots\dots\dots(2-2)$$

Figure 2-7 shows the transfer characteristics of the CP and the proposed FEN POST SONOS. It is obvious that (as shown in Table 2-1) the FEN POST SONOS with GAA structure device has superior performance than CP device with higher on current, smaller V_{th} and steeper subthreshold swing (SS), higher on/off ratio, and higher mobility, which are contributed to the enhanced gate control ability by the three sharp corners and GAA structure together with the reduced number of grain-boundary defect in the nanowire channel [48]. For memory operations, in this work, the TFT SONOS memory is programmed and erased by Fowler-Nordheim (FN) tunneling mechanism. Figure 2-8(a) and 2-8(b) show the transfer characteristics of the CP and the proposed FEN POST SONOS devices after DC stress at $V_{gs}=7$ V condition. The results, clearly, indicate the transfer characteristics are the same even

the stress time is 1000 sec. Thus, the read disturb can be neglected under the normal transistor operation. Figure 2-9 and 2-10 show the transfer characteristics of the CP and FEN POST SONOS devices with various programming times at a gate voltage 15 V, respectively. For erasing operations, the transfer characteristics of the CP and FEN POST SONOS devices with various erasing times at gate voltage -15 V are shown in Figs. 2-11 and 2-12, respectively. It is obviously found that the program/erase (P/E) efficiency of the FEN POST SONOS device is significantly better than the CP one. In the programming characteristics, the FEN POST SONOS exhibit a large V_{th} shift of 2.71 V in 1 ms at a gate pulse of +15 V, while there is only 0.49 V shift in CP device. The erase characteristics also show that the FEN POST SONOS devices are much faster (a V_{th} shift of 2.11 V in 1 ms at a gate pulse of -15 V) than the CP counterparts. The improvement on P/E speed and window can be attributed to the field enhancement from the three sharp corners to promote carrier injection through the tunneling oxide into the nitride storage layer. The V_{th} shifts after programming and erasing operation for the CP and FEN POST SONOS devices with various voltage are plotted in Figs. 2-13(a) and 2-13(b).

For further clarifying this P/E efficiency enhancement, the simulations of electrical fields for the CP and FEN POST SONOS structures were performed by ISE-TCAD simulator. The distribution of electrical field and band diagrams across the stacked ONO dielectrics was numerically simulated at a gate bias of 15 V for the CP and FEN POST SONOS devices as shown in Fig. 2-14 and 2-15, respectively. The sharp geometry of these three corners enhances the electric field at the Si/tunneling oxide interface and depresses the electric field in the blocking oxide. The large field at the Si/tunneling oxide interface enhances the carrier-injection probability and thus increases both the P/E speeds of FEN POST SONOS device. In addition, the reduction of the electric field in the blocking oxide prevents charges tunneling from

the nitride to the poly-gate and from the poly-gate to the nitride. The P/E activity is thus facilitated between the channel and tunneling oxide rather than between the blocking oxide and the gate. In contrast, for CP SONOS structures, as shown in Fig. 2-14, the electric field in the tunneling oxide is equal to that in the blocking oxide, leading to lower P/E efficiency. In addition, Figure 2-15 exhibits the FEN POST SONOS device has shorter tunneling distance than the CP SONOS device. Figure 2-16 shows the retention characteristic of FEN POST SONOS device, where the memory window is maintained with negligible degradation up to the tested time of 10^4 sec. It shows the memory window will be larger than 1.1 V after extrapolating to retention time of 10 years. The endurance characteristic of FEN POST SONOS device is shown in Fig. 2-17, the memory window was kept 1.68V and rises about 1 V after 10^4 P/E cycles. The rising of memory window results from both the charges in Si_3N_4 deep level traps are hard to be erased and the subthreshold swing is degradation due to the tunneling oxide is damaged during P/E cycles.



2-5. Summary

In summary, we have demonstrated the FEN POST SONOS devices, the FEN POST SONOS devices have superior performance than CP devices with higher on current, smaller V_{th} , steeper subthreshold swing (SS), higher on/off ratio, and higher mobility which are contributed to the enhanced gate control ability by the three sharp corners and GAA structure together with the reduced number of grain-boundary defect in the nanowire channel. In addition, the proposed FEN POST SONOS exhibits higher P/E speed than CP SONOS due to larger electric field in the tunneling layer

and lower electric field in the blocking oxide. The proposed FEN POST SONOS also exhibits stable endurance/retention characteristics. And, the process simplicity and good device performance is very promising for future SOP and 3-D ICs applications.



Chapter 3

Field-Enhanced-Nanwire Poly-Si TFT Silicon-Oxide-Nitride-Vacuum-Silicon (FEN POST SONVAS) Memory With a Gate-All-Around Structure

3-1. Introduction

The conventional SONOS-type memories use SiO₂ as blocking oxide and tunnel dielectric, which may be modified to achieve higher speed and lower voltage operation by using high-*k* dielectric as blocking oxide [51-53]. Less voltage dropped in blocking layer and more voltage dropped in tunneling layer when using high-*k* dielectric for blocking dielectric, so the program/erase efficiency can be enhanced. In addition, the use of high-*k* material as the tunnel dielectric and trapping layer has also been introduced to enable further scaling [54-57].

Endurance is the ability of a nonvolatile memory to endure the damage of numerous cycles of programming and erasing, i.e., the number of program/erase cycles that the memory will retain the required memory window. Since the carriers for programming and erasing have energy, they will cause the degradation of tunneling oxide and trapping layer in every operation. In previous chapter, Fig. 2-16 shows the endurance characteristic of FEN POST SONOS. The memory window rising results from both the charges in Si₃N₄ deep level traps are hard to be erased and the subthreshold swing is degradation due to the tunneling oxide is damaged during P/E cycles. To suppress the degradation of tunneling oxide during P/E cycles, we

proposed a field-enhanced-nanowire poly-Si TFT silicon-oxide-nitride-vacuum-silicon (FEN POST SONVAS) structure which tunneling oxide was replaced with vacuum. So, the damage of tunneling layer during P/E operation can be suppressed. In other words, the FEN POST SONVAS structure can enhance the endurance characteristic of the devices. In addition, in this work, we used the low- k (vacuum) material to replace the tunneling oxide to enhance the endurance characteristics. At the same time, the lowest- k property of vacuum make higher voltage dropped in the vacuum tunneling layer. This phenomenon can enhance the electric field in tunneling and lower the electric field in blocking oxide. In other words, the program/erase efficiency can be enhanced similar as the introduction of high- k blocking dielectric.



3-2. Fabrication Sequences of FEN POST SONVAS with a Gate-All-Around Structure

The fabrication sequence of proposed FEN POST SONOS memory has been described in the previous chapter. A 5-nm-thick tunneling oxide, a 10-nm-thick nitride trap layer, a 10-nm-thick blocking oxide, and a 200-nm-thick phosphorous *in-situ* doped poly-Si were sequentially deposited conformally to wrap around those suspending spacer nanowires by LPCVD systems after sacrificial oxide was removed by diluted HF. After gate patterning, the *in-situ* doped poly-Si, blocking oxide and Si₃N₄ trap layer were etched out by RIE and tunneling oxide was still remained as shown in cross-section schematic image in Fig. 3-1. A phosphorous ion implantation was performed with a dosage of $5 \times 10^{15} \text{ cm}^{-2}$ and an energy of 35 keV. A 200-nm-thick

Si_3N_4 was deposited and then etched back to form two Si_3N_4 spacers resided against the poly-Si gate and on the tunneling oxide layer as shown in cross-section schematic image in Fig. 3-2. The tunneling oxide was side-etched for 350-nm with (1:10) diluted BOE as shown in Fig. 3-3. A 300-nm-thick passivation oxide was deposited by SiH_4 -based PECVD system and the remaining processes were same as the previous FEN POST SONOS device. The FEN POST SONVAS structure is shown in cross-section schematic image in Fig. 3-4.

3-3. Materials Analysis of FEN POST SONVAS with a Gate-All-Around Structure

The previous section briefly describes the process sequence of the FEN POST SONVAS device. In this section, the scanning electron microscope (SEM) and transmission electron microscope (TEM) have been used to analyze the detailed process parameter in the fabrication of FEN POST SONVAS.

Figure 3-5 exhibits the tiled-view SEM image of the FEN POST SONVAS device. It shows the nitride spacers resided against the S/D extensions and the empty gap on the nanowire channel. The cross-section schematic image of nanowire channel with vacuum tunneling layer as shown in Fig. 3-6.

3-4. Results and Discussions

In this work, the FEN POST SONVAS memory is also programmed and erased

by Fowler-Nordheim (FN) tunneling mechanism. Figure 3-7 show the transfer characteristics of the FEN POST SONVAS devices with various programming times at a gate voltage of 15 V. For erasing operations, the transfer characteristics of the FEN POST SONVAS devices with various erasing times at gate voltage of -15 V are shown in Figs. 3-8. The V_{th} shifts after programming and erasing operation at a gate voltage 15 V and -15 V, respectively, for the CP, FEN POST SONOS and FEN POST SONVAS devices are shown in Table 3-1. It is clear found that the program/erase (P/E) efficiency of the FEN POST SONVAS device is better than the FEN POST SONOS.

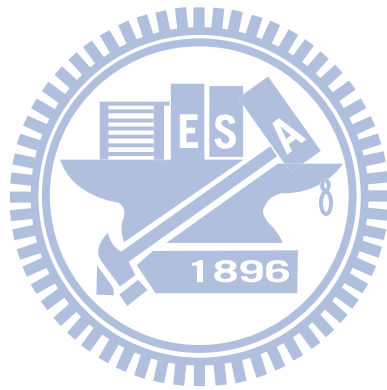
For further clarifying this P/E efficiency enhancement, the simulations of electrical field for the FEN POST SONOS and FEN POST SONVAS structures were performed by ISE-TCAD simulator. The distribution of electrical field across the stacked ONO dielectrics was numerically simulated at a gate bias of 15 V for the FEN POST SONOS and FEN POST SONVAS devices as shown in Figs. 3-9 and 3-10, respectively. Figs. 3-9 and 3-10 indicate that the FEN POST SONVAS device has larger electric field in the tunneling layer and lower electric field in the blocking oxide. The larger electric field in the vacuum layer results from its low-k property. There is higher percentage of voltage dropped in the vacuum layer. The large field in the vacuum layer enhances the carrier-injection probability and thus increases both the P/E speeds in FEN POST SONVAS device. In addition, the reduction of the electric field in the blocking oxide prevents charges tunneling from the nitride to the poly-gate and from the poly-gate to the nitride. The P/E activity is thus facilitated between the channel and vacuum layer rather than between the blocking oxide and the gate. The band diagram was numerically simulated at a gate bias of 15 V for the FEN POST SONVAS device as shown in Fig. 3-11. It shows the FEN POST SONVAS device also has shorter tunneling distance. Fig. 3-12 shows the retention characteristics of FEN

POST SONOS and FEN POST SONVAS devices after 10^4 cycles, where the memory window of FEN POST SONVAS device is maintained with little degradation up to the tested time of 10^4 sec. It shows the memory window will be larger than 1.4 V after extrapolating to retention time of 10 years. The larger memory window after extrapolating to retention time of 10 years for FEN POST SONVAS device results from its higher P/E speed. The endurance characteristic of FEN POST SONVAS device is shown in Fig. 3-13. The 2.4-V memory window was kept and the window rises only 0.5 V after 10^4 P/E cycles. The less memory window shift after 10^4 P/E cycles for FEN POST SONVAS device results from less dangling bonds and interface traps produced during P/E cycles. The subthreshold swing of FEN POST SONOS and FEN POST SONVAS devices after P/E cycles is shown in Fig. 3-14 and Table 3-2, respectively. The subthreshold swing of FEN POST SONOS device changed from 390 mV/decade to 523 mV/decade and that of FEN POST SONVAS device changed only from 345 mV/decade to 384 mV/decade after 10^4 P/E cycles.

3-5. Summary

In summary, we have demonstrated the poly-Si FEN POST SONOS structure in the previous chapter; the proposed FEN POST SONOS device exhibits superior memory device characteristics with higher P/E efficiency and stable endurance/retention characteristics. And, the process simplicity is very promising for future SOP applications. In this chapter, we have demonstrated the FEN POST SONVAS structure. The proposed FEN POST SONVAS device exhibits higher P/E speed than FEN POST SONOS due to larger electric field in the tunneling layer and

lower electric field in the blocking oxide. In addition, the FEN POST SONVAS device also exhibits better data retention and endurance characteristics than the previous FEN POST SONOS device.



Chapter 4

Conclusions

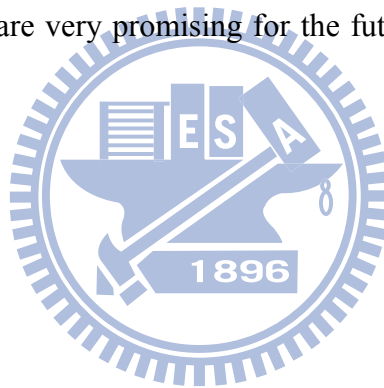
In this thesis, novel FEN POST SONOS and FEN POST SONVAS memory devices with gate-all-around structures have been demonstrated in previous chapters. In this chapter, the both memory devices are discussed and summarized in detail.

In chapter 2, a simple and cost-effective method was performed to fabricate the FEN POST SONOS device. The simple spacer technique was used to form the nanowire channels without any advanced lithography. The FEN POST SONOS devices have superior performance than CP SONOS devices with higher on current, smaller V_{th} , steeper subthreshold swing (SS), higher on/off ratio, and higher mobility, which are contributed to the enhanced gate controllability by the three sharp corners and GAA structure together with the reduced number of grain-boundary defect in the nanowire channel. In addition, the proposed FEN POST SONOS device exhibits higher P/E speed due to much enhanced electric field in the tunneling layer and lower electric field in the blocking oxide as compared to the CP SONOS devices. The FEN POST SONOS device exhibited a V_{th} shift of 2.71 V and 2.11 V at $V_{GS} = +15/-15$ V in 1 ms for FN programming and erasing operations, respectively; while the reference CP SONOS devices only showed the negligible change. And, the FEN POST SONOS devices also showed stable retention and reasonable endurance characteristics. For retention, the FEN POST SONOS device maintained 1.1V memory window after ten years. For endurance, the FEN POST SONOS device kept 1.68V memory window after 10^4 P/E cycles.

In chapter 3, a novel FEN POST SONVAS device which tunneling oxide was replaced with vacuum is demonstrated in this work. The proposed FEN POST

SONVAS device exhibits higher P/E speed than FEN POST SONOS device due to larger electric field in the vacuum tunneling layer and lower electric field in the blocking oxide. It exhibited a V_{th} shift of 3.17V and 2.68 V at $V_{GS} = +15/-15$ V in 1 ms for programming and erasing operations, respectively. And, the FEN POST SONVAS device also showed better retention and endurance characteristics. For retention, the FEN POST SONVAS maintained 1.4V memory window after ten years. For endurance, the FEN POST SONVAS kept 2.4V memory window and only 0.5V memory window shift.

Since the FEN POST SONOS and FEN POST SONVAS devices exhibited excellent performance, such as good electrical characteristics, high P/E efficiency, and stable reliability, they are very promising for the future applications in SOP and 3-D ICs.



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	V _{th} (V)	S.S. (mV/decade)	Mobility (cm ² /V-s)	On/off ratio
FEN POST SONOS	<i>0.91</i>	<i>390</i>	<i>26</i>	<i>1.65x10⁷</i>
CP SONOS	1.41	544	16	1.26x10 ⁶

Table 2-1 Electrical characteristics of the FEN POST SONOS and CP SONOS devices.

Program				Erase			
	CP SONOS	FEN POST SONOS	FEN POST SONVAS		CP SONOS	FEN POST SONOS	FEN POST SONVAS
Time (sec)	V _{th} - shift (V)			Time (sec)	V _{th} - shift (V)		
1.E-06	<i>0.35</i>	<i>1.48</i>	<i>1.8</i>	1.E-06	<i>-0.15</i>	<i>-0.27</i>	<i>-0.51</i>
1.E-05	0.42	1.99	2.29	1.E-05	-0.20	-0.57	-0.98
1.E-04	0.44	2.4	2.77	1.E-04	-0.27	-1.67	-2.02
1.E-03	0.49	2.71	3.17	1.E-03	-0.32	-2.11	-2.68
0.01	0.56	3.24	3.78	0.01	-0.48	-2.68	-2.92
0.1	0.78	3.9	4.21	0.1	-0.50	-2.83	-3.13
1	0.95	4.41	4.74	1	-0.54	-3.01	-3.34

Table 3-1 The V_{th} shifts after programming and erasing operation at V_{GS}= 15 V and -15 V for the CP, FEN POST SONOS and FEN POST SONVAS devices.

	cycles (times)	initial	10	100	1000	10K
FEN POST SONVAS	S.S. (mV/decade)	345	347	351	360	384
FEN POST SONOS	S.S. (mV/decade)	390	400	412	457	523

Table 3-2 The subthreshold swing of FEN POST SONOS and FEN POST SONVAS devices after P/E cycles.

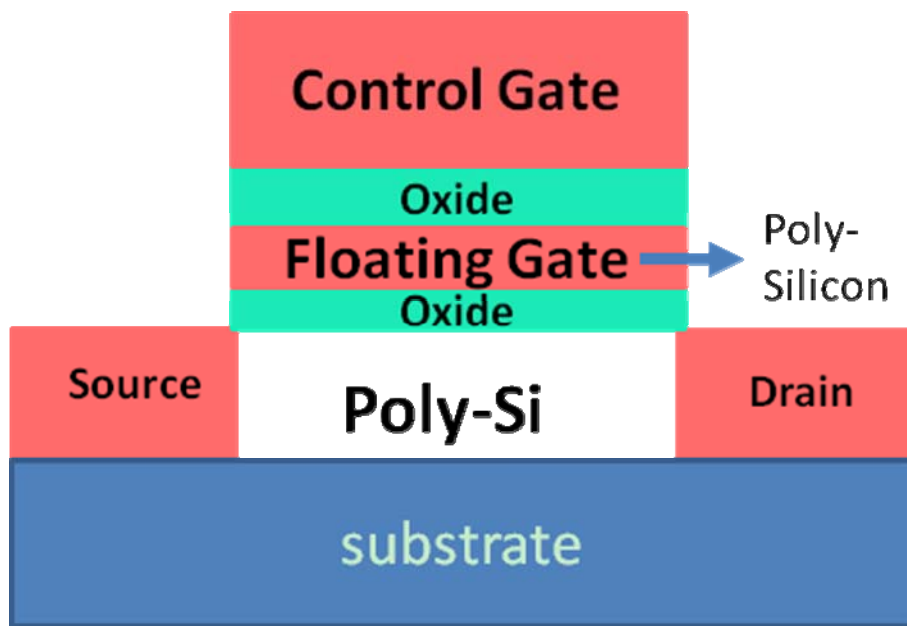


Fig. 1-1 The structure of the conventional floating gate nonvolatile memory device. The poly-Si floating gate is used as the charge storage element.

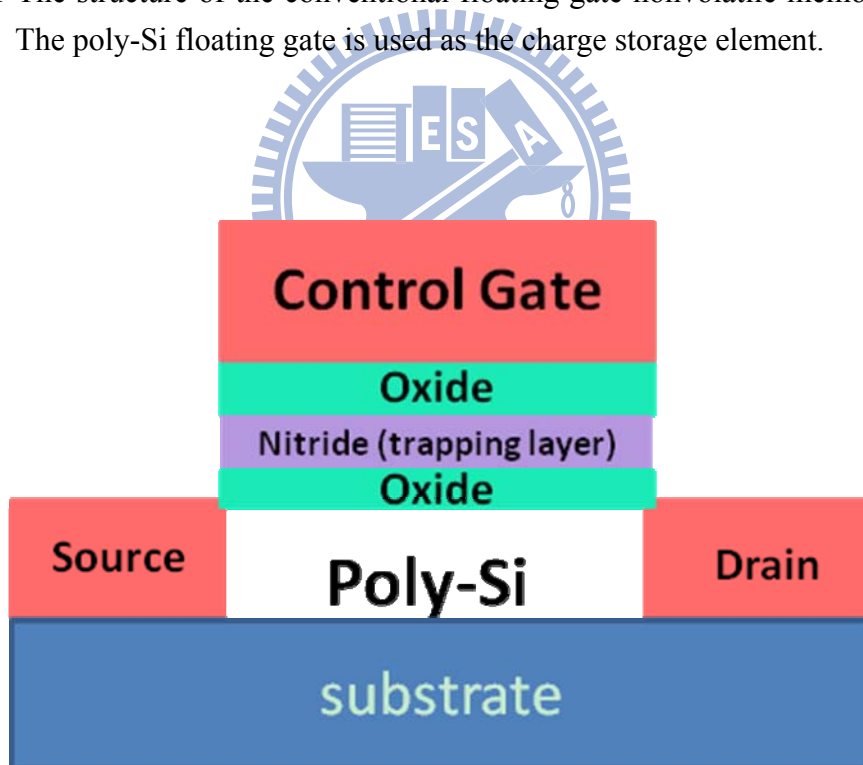


Fig. 1-2 The structure of the SONOS nonvolatile memory device. The nitride layer is used as the charge-trapping element.

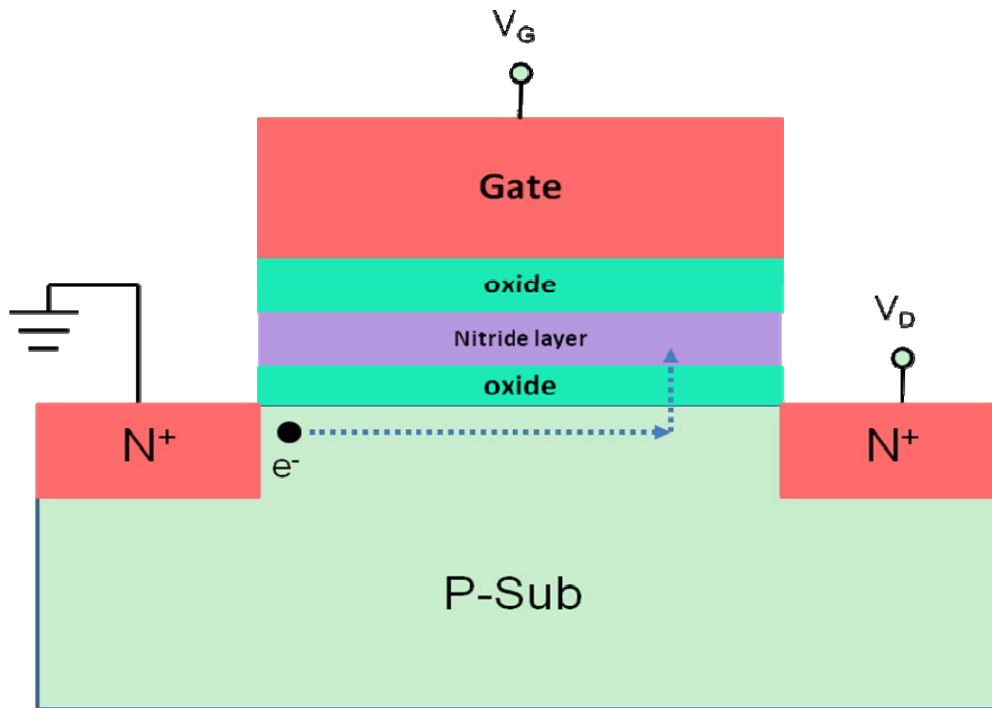


Fig. 1-3 Proposed trajectory of an emitted channel electron. An energetic electron is redirected toward the interface by an acoustic phonon scattering.

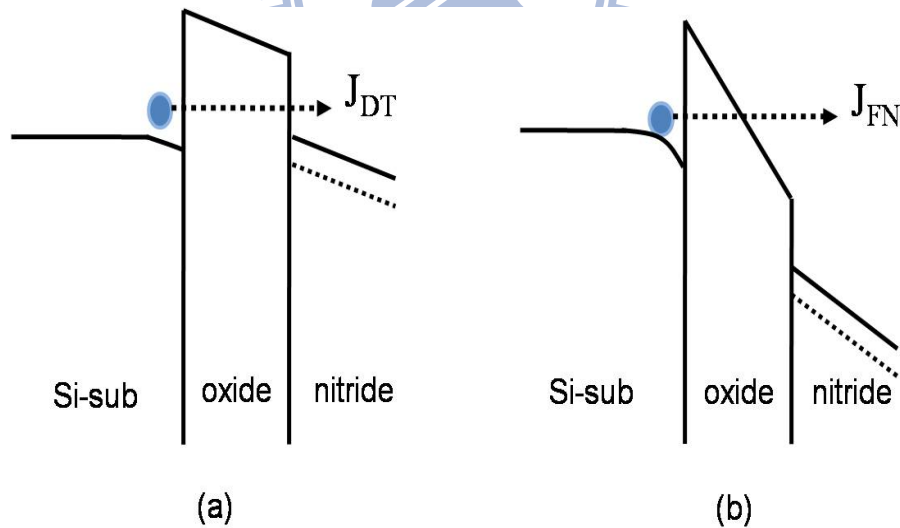


Fig. 1-4 (a) Direct tunneling is associated with transversal of a trapezoidal barrier. (b) Fowler-Nordheim Tunneling is associated with transversal of a triangular barrier.

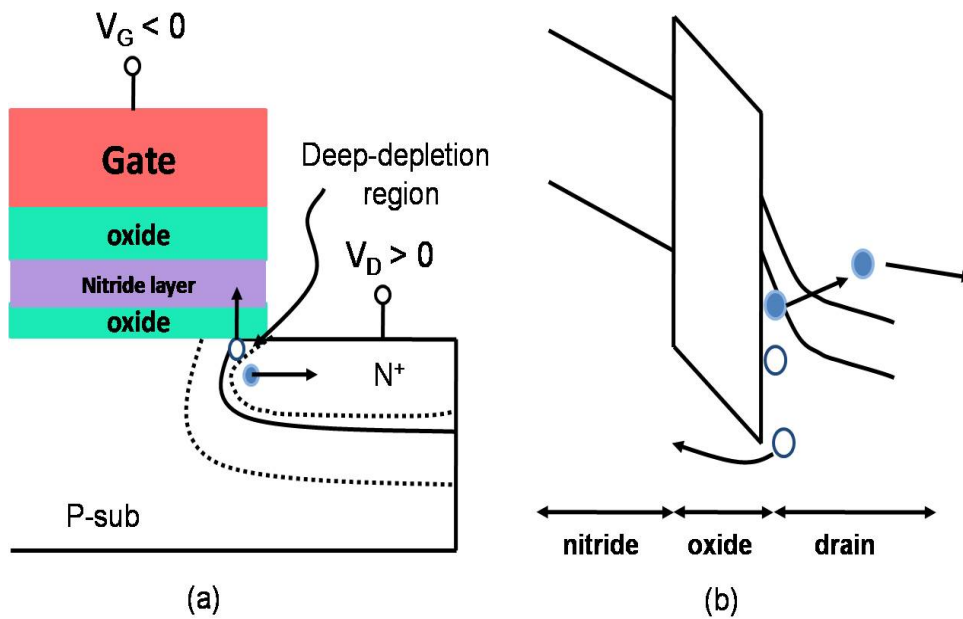


Fig. 1-5 Illustration of Band to band tunneling. (a) Electron-hole pair appear in the deep-depletion region layer in the n⁺ drain. (b) The path of electron-hole pair in energy band diagram.

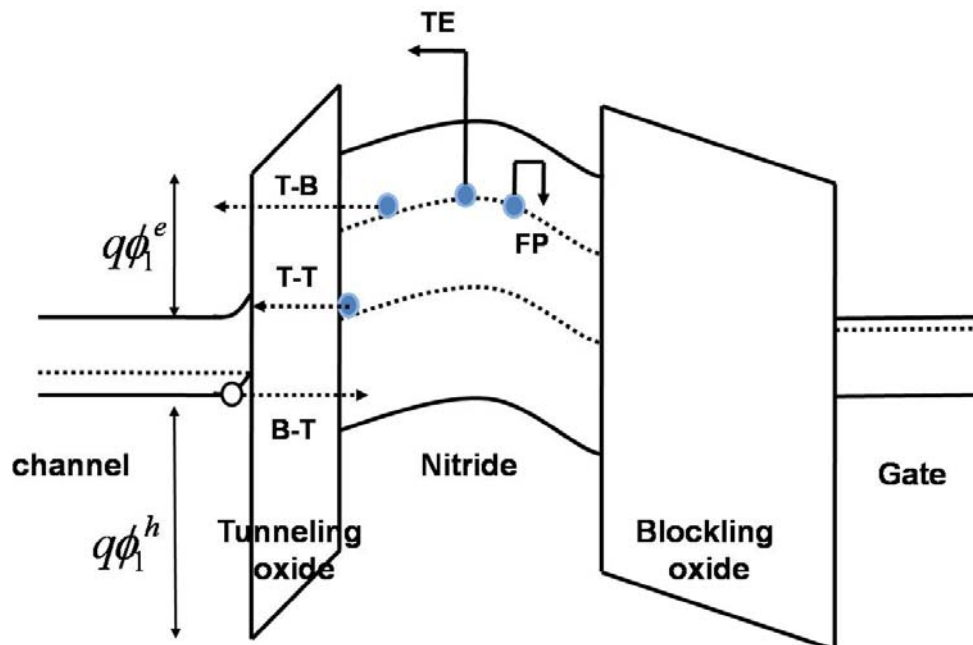


Fig. 1-6 Band diagram of trapped charges loss path in SONOS: trap-to-band tunneling (T-B), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE) and Frenkel-Poole emission (FP).

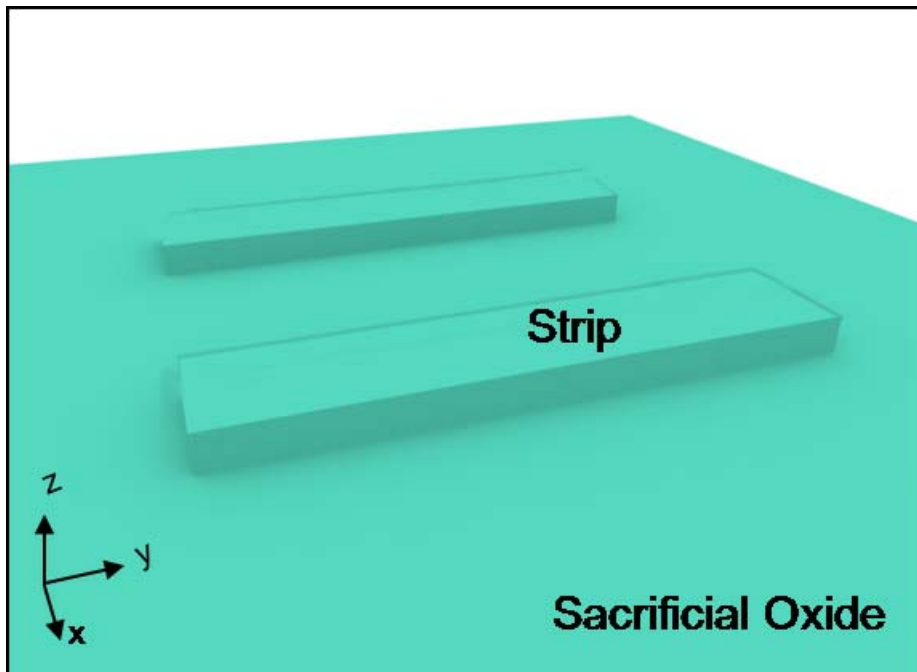


Fig. 2-1(a) The tilted view process step of the strip formation.

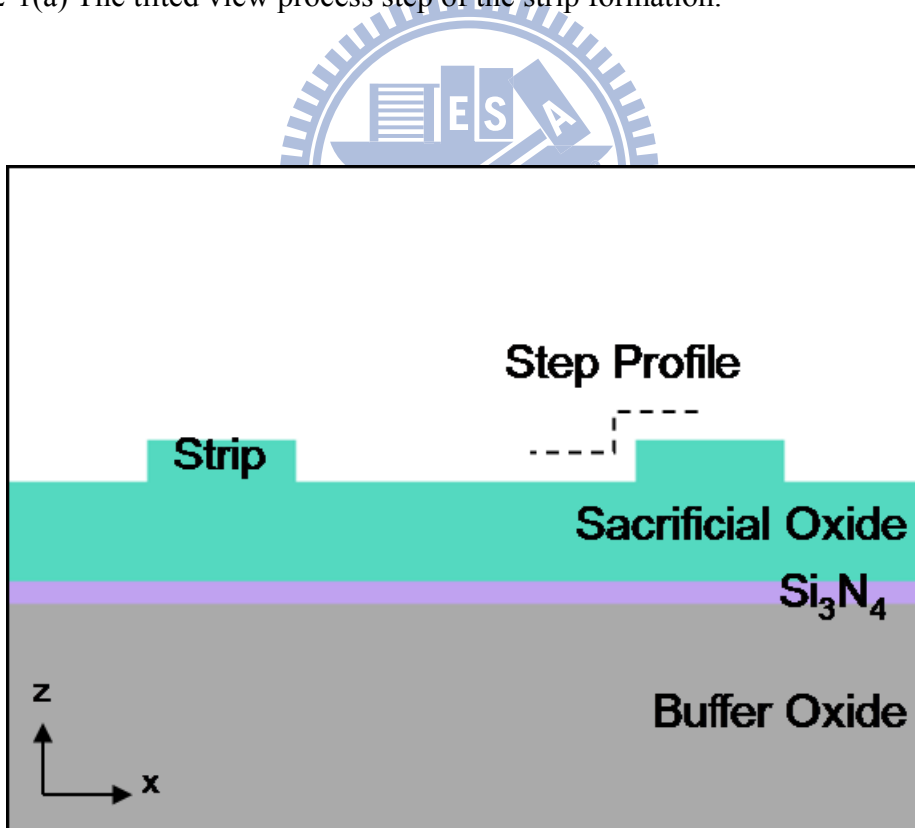


Fig. 2-1(b) The cross-section view step of the strip formation.

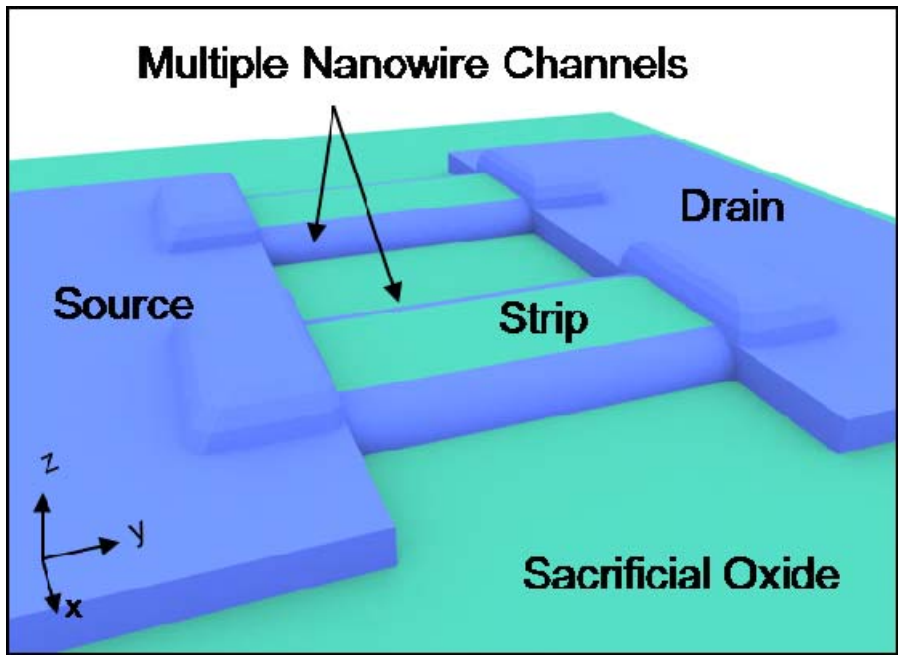


Fig. 2-1(c) The tilted view step of the nanowire-channel formation.

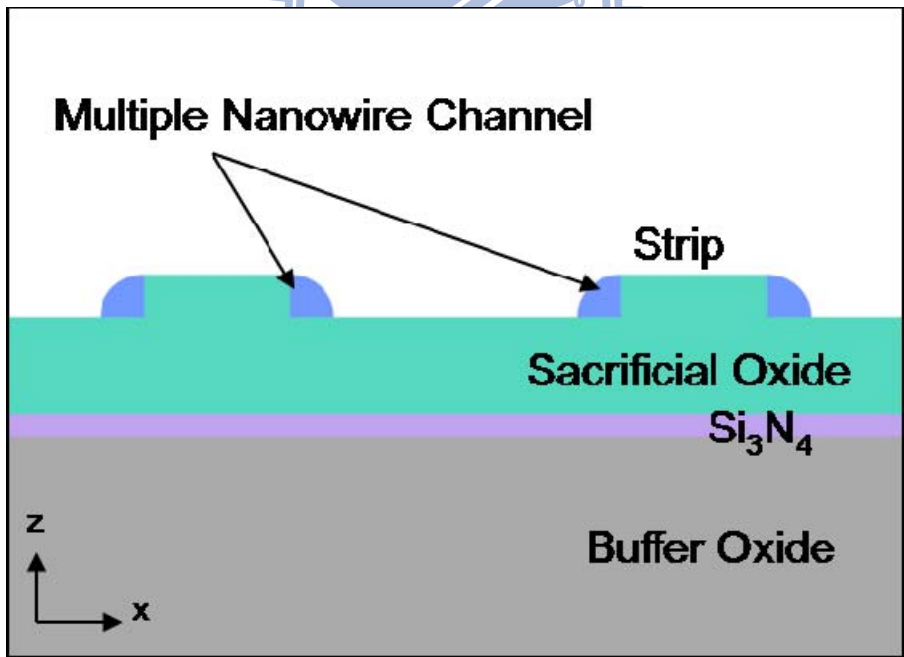


Fig. 2-1(d) The cross-section view step of the nanowire-channel formation.

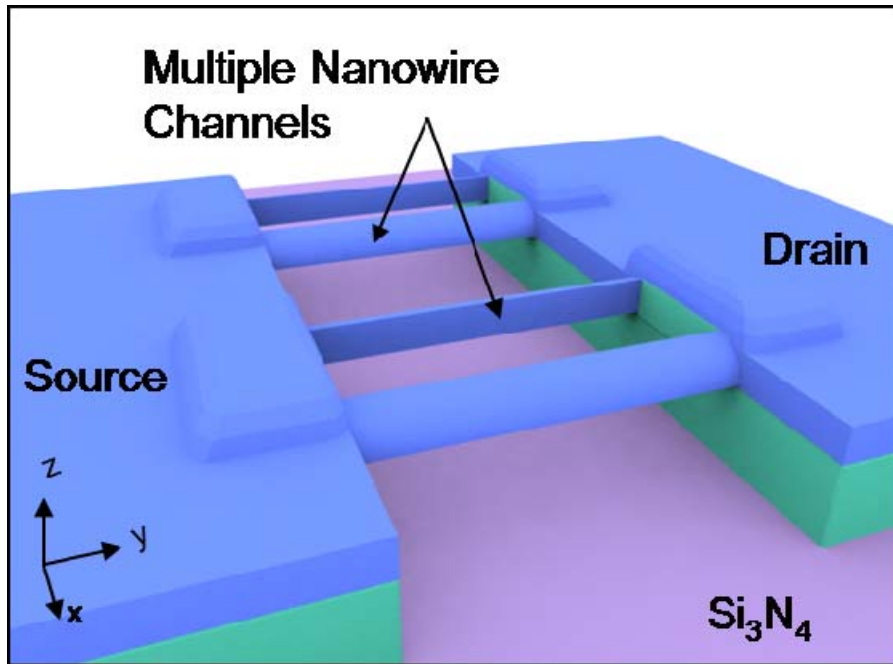


Fig. 2-1(e) The tilted view step of the suspending nanowire-channel formation.

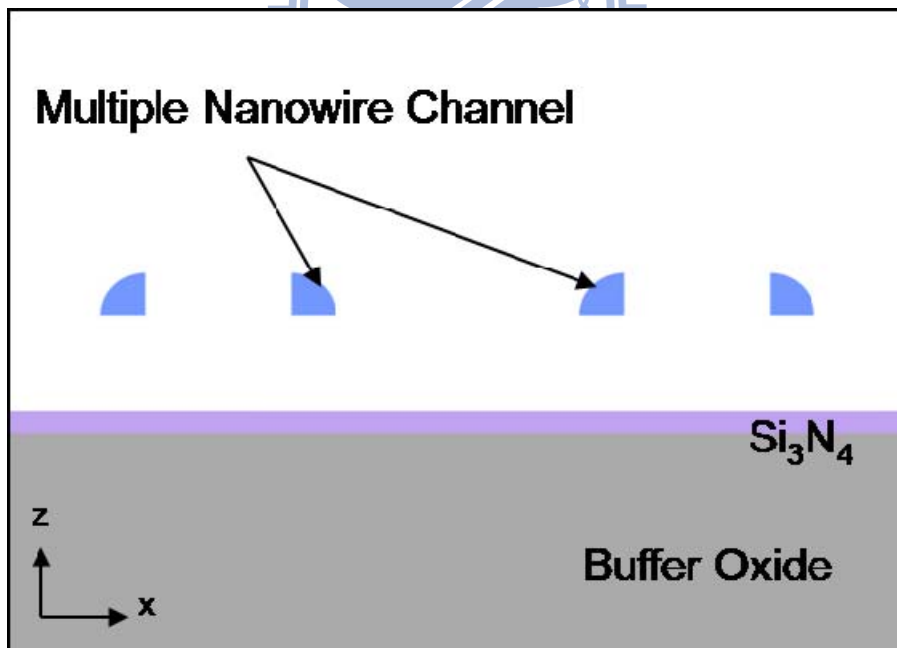


Fig. 2-1(f) The cross-section view step of the suspending nanowire-channel formation.

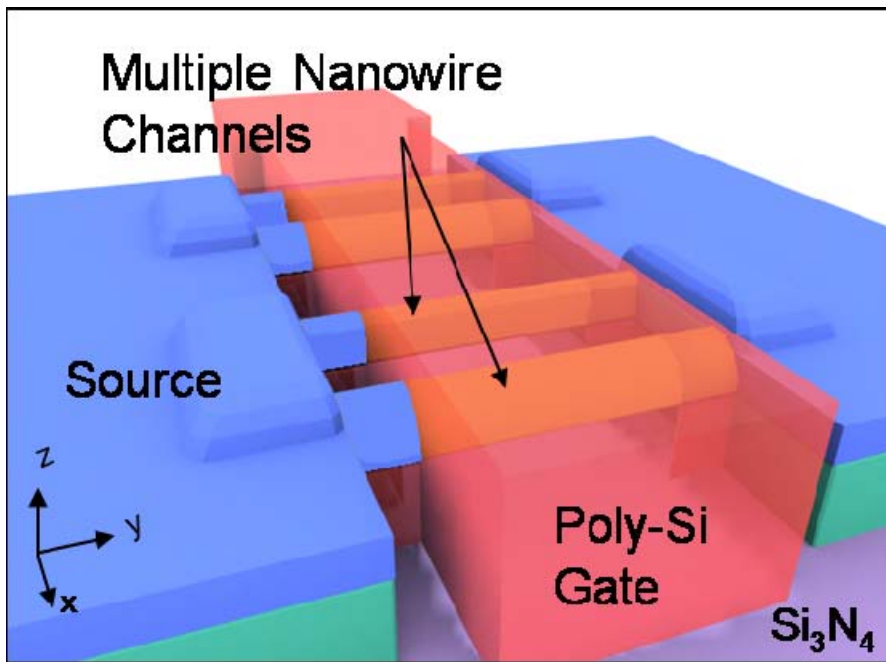


Fig. 2-1(g) The tilted view step of the gate formation.

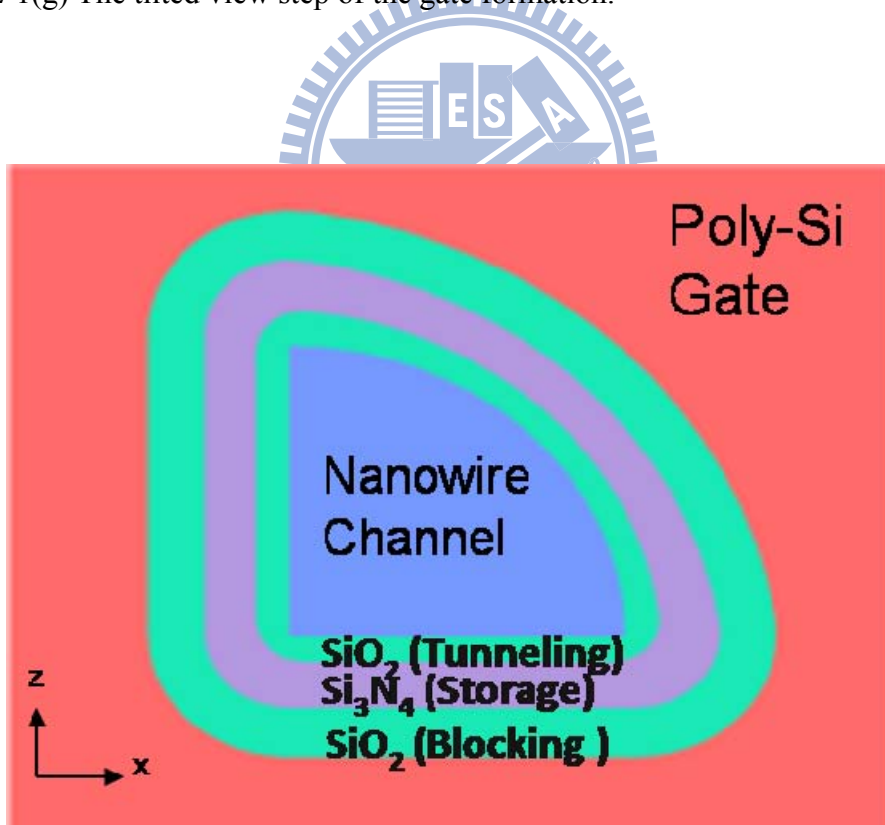


Fig. 2-1(h) The cross-section view step of the gate formation.

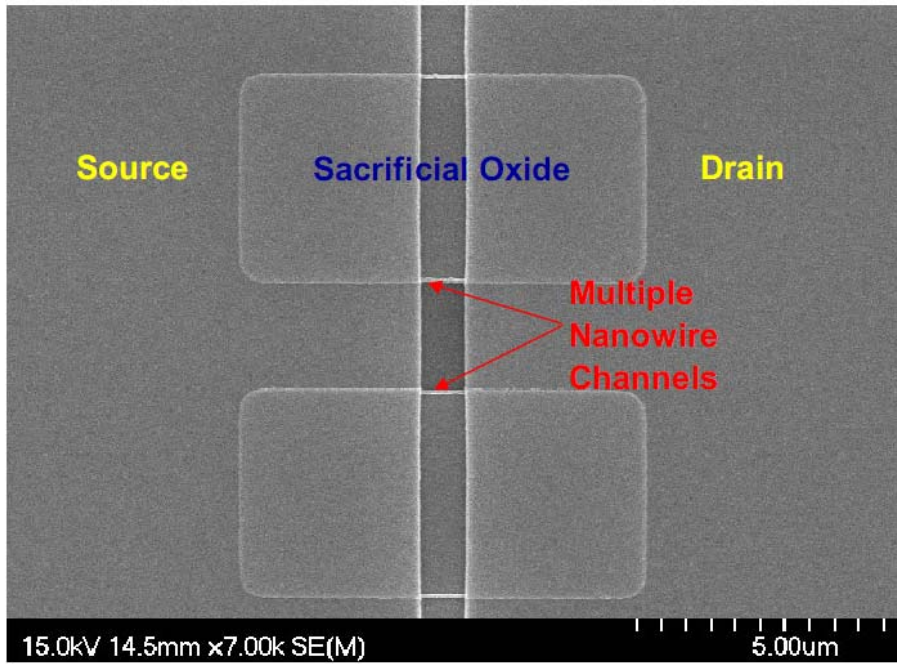


Fig. 2-2(a) The top view SEM image of one sacrificial strip with twin spacer nanowire before HF etching.

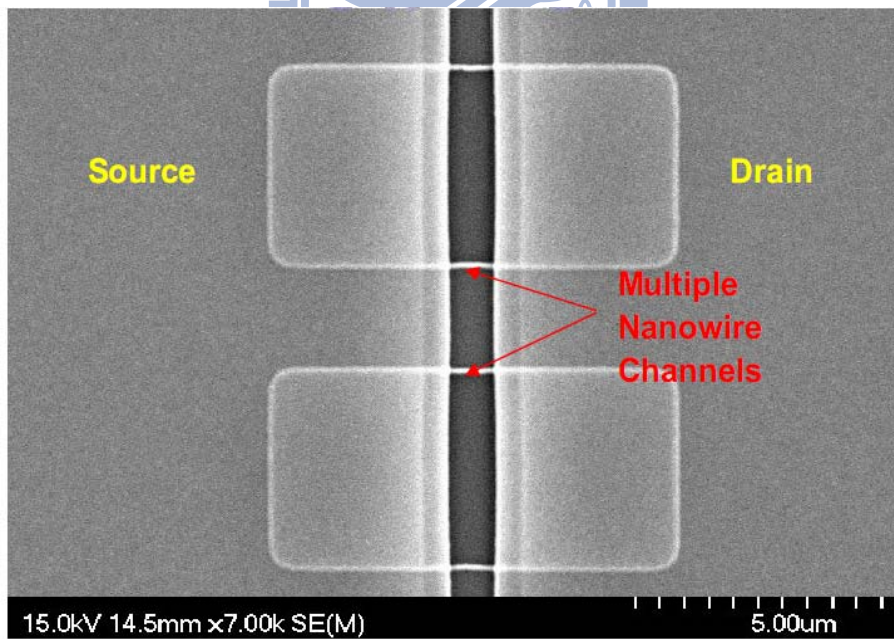


Fig. 2-2(b) The top view SEM image of one sacrificial strip with twin spacer nanowire after HF etching.

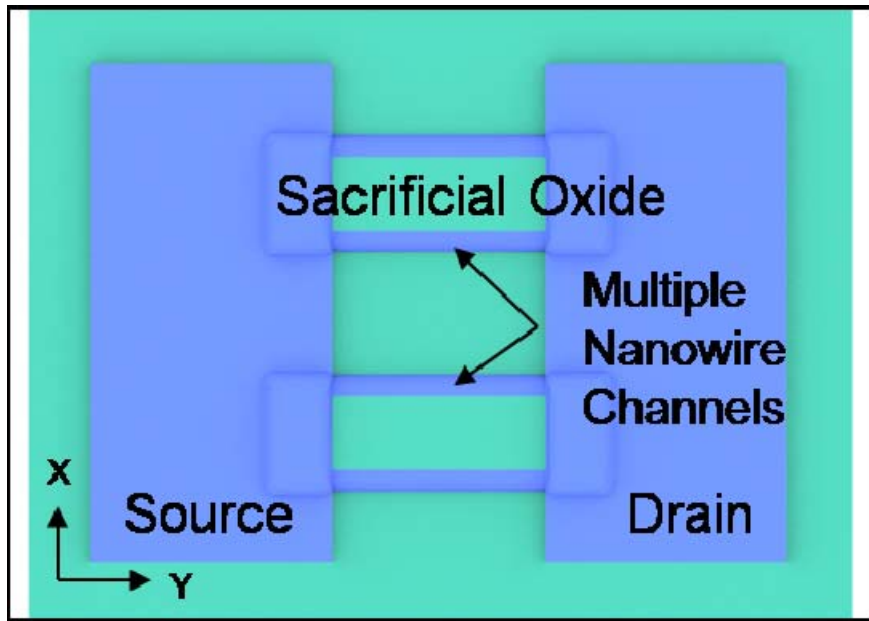


Fig. 2-2(c) The corresponding process step of one sacrificial strip with twin spacer nanowire before HF etching in top view.

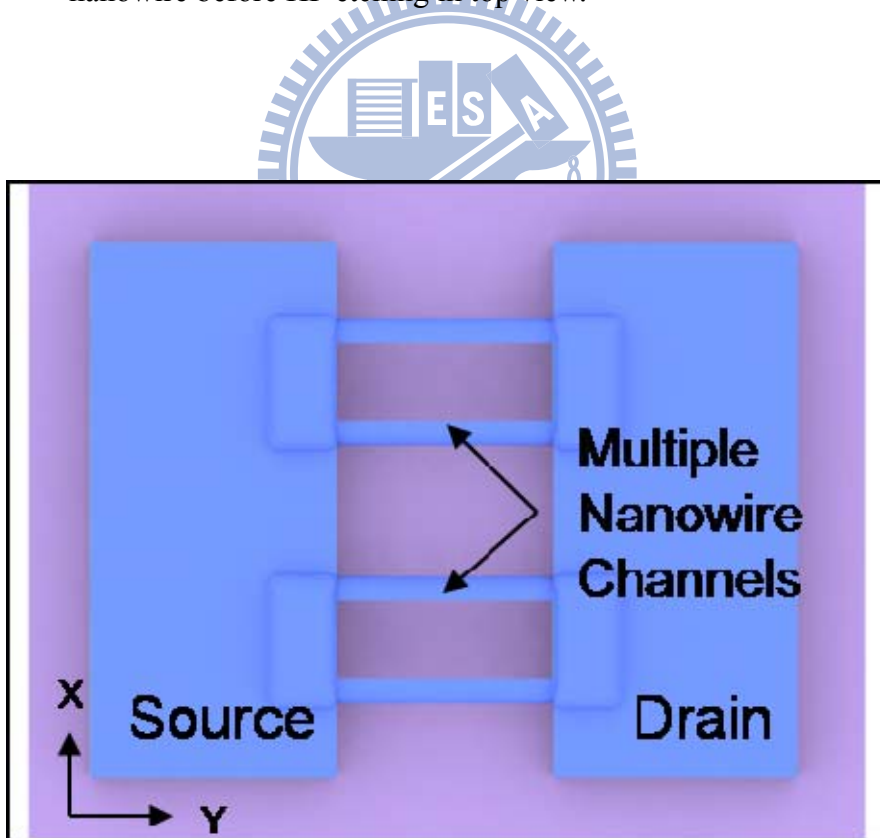


Fig. 2-2(d) The corresponding process step of one sacrificial strip with twin spacer nanowire after HF etching in top view.

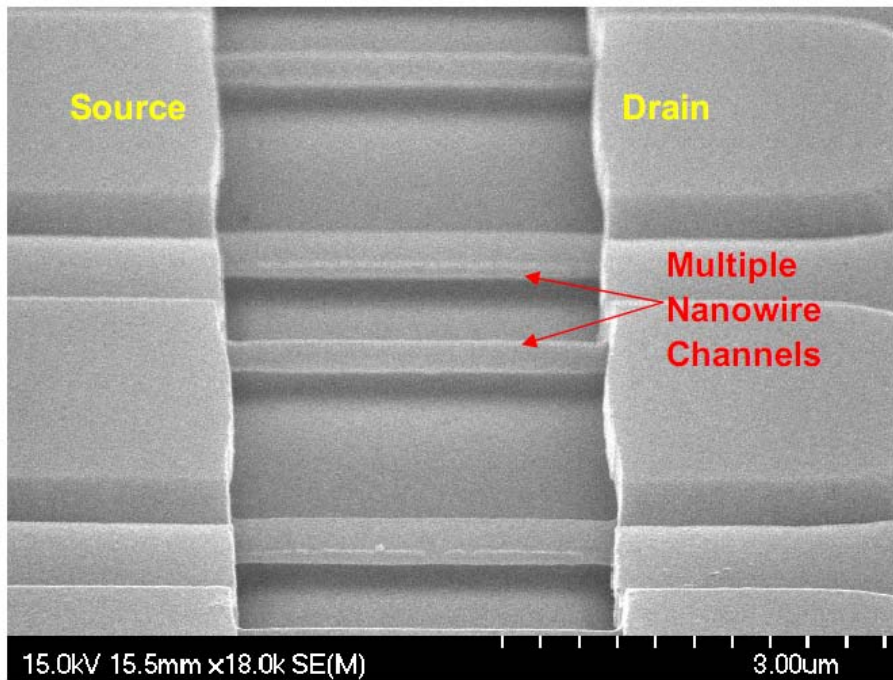


Fig. 2-3(a) The tiled view SEM image of multiple nanowire channels after HF etching.

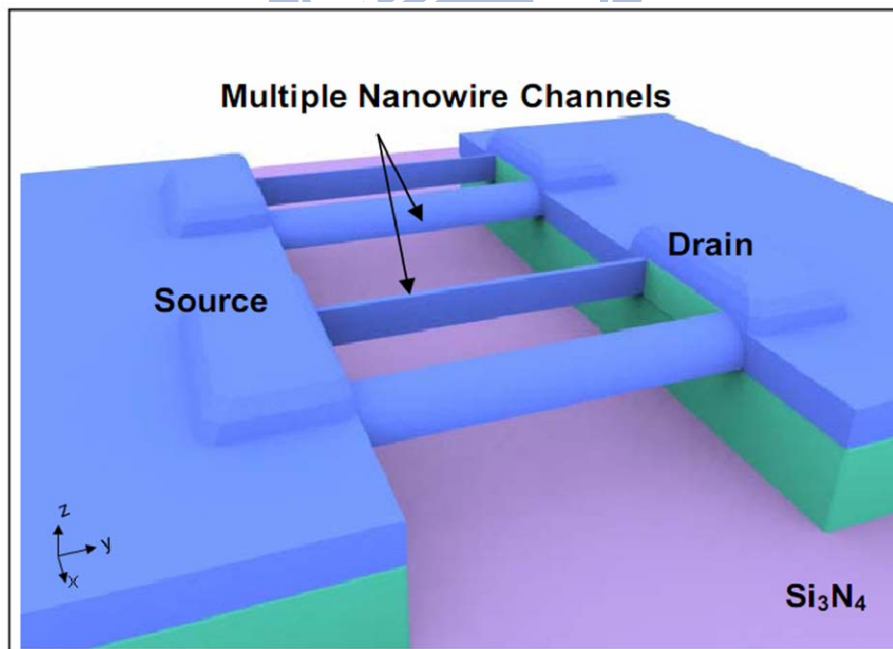


Fig. 2-3(b) The corresponding process step of multiple nanowire channels after HF etching in tiled view.

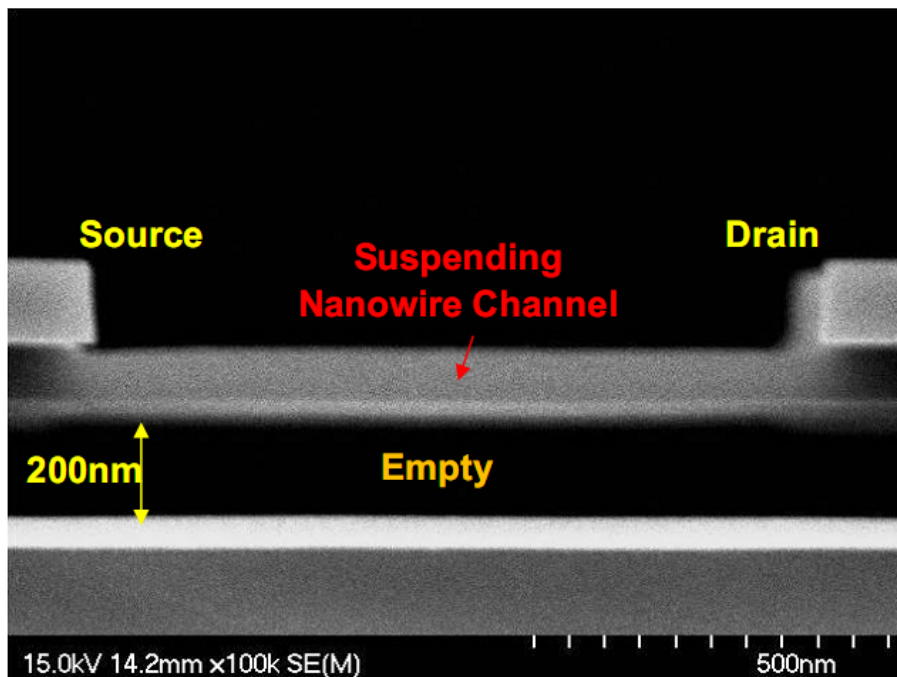


Fig.2-4(a) The cross-section SEM image of suspending channels.

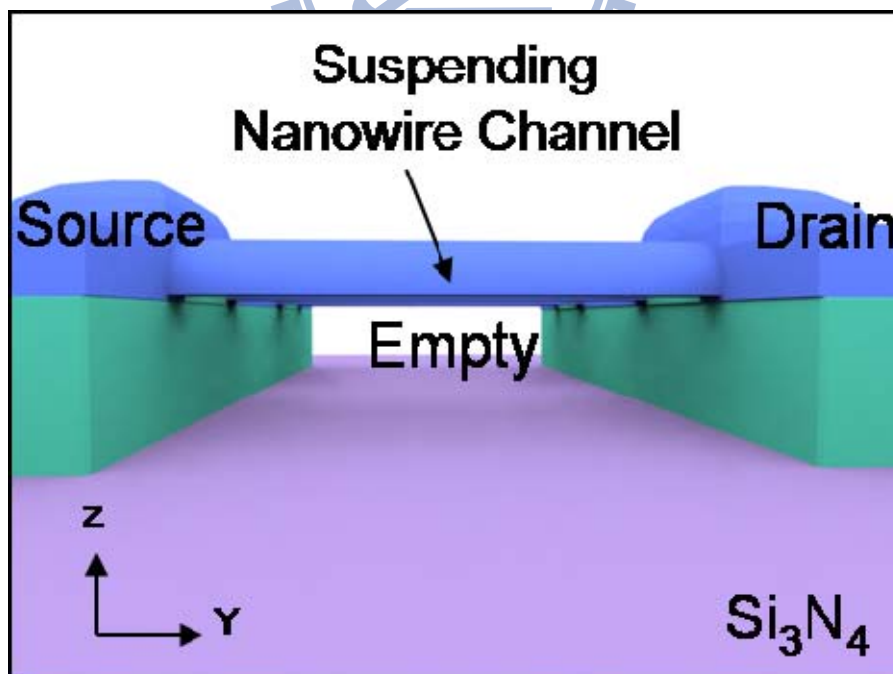


Fig. 2-4(b) The corresponding process flow of multiple nanowire channels after HF etching in cross-section view.

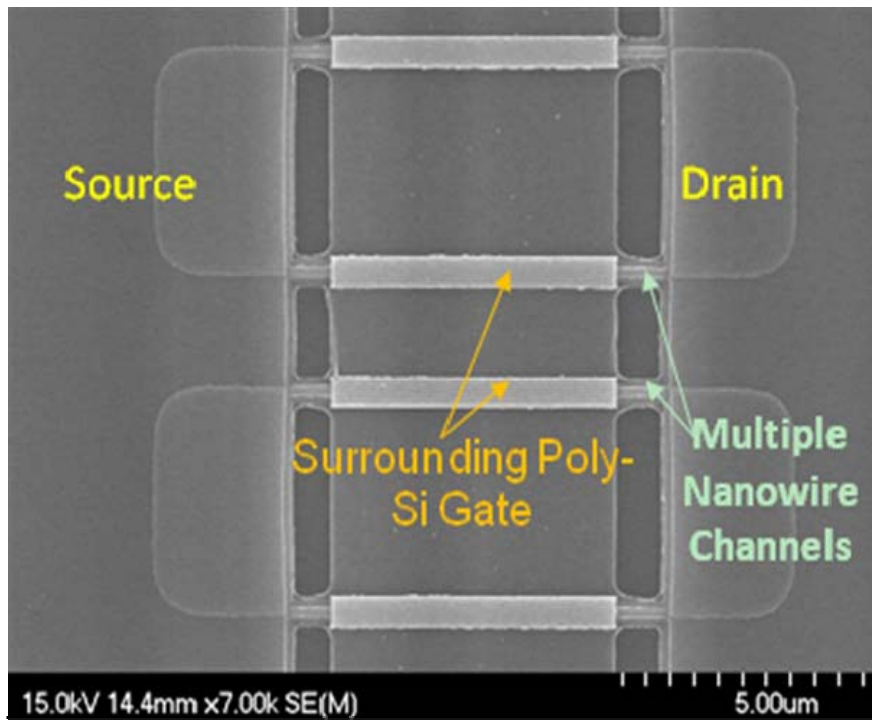


Fig. 2-5(a) The top view SEM image after patterning gate.

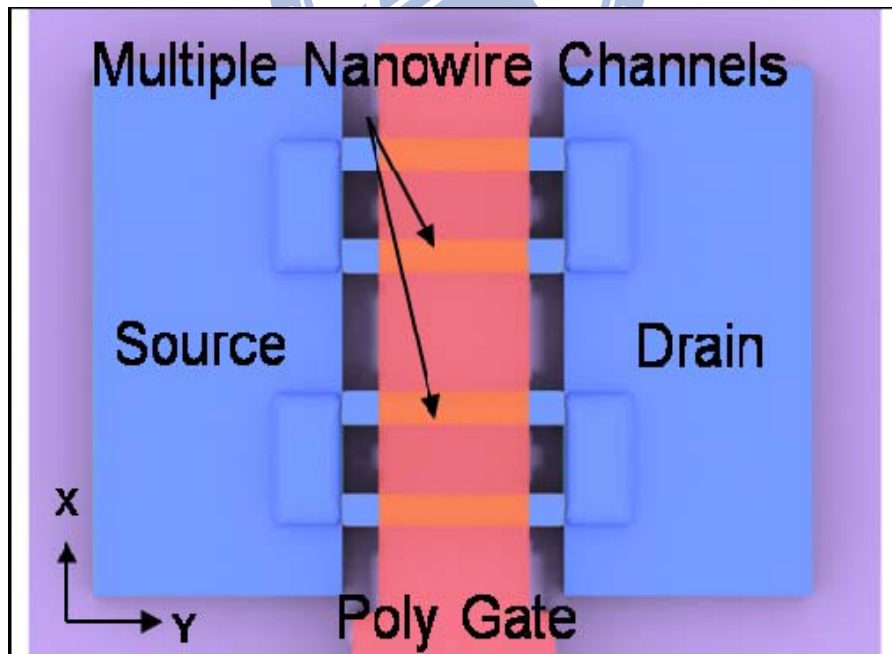


Fig. 2-5(b) The corresponding process step after patterning gate in top view.

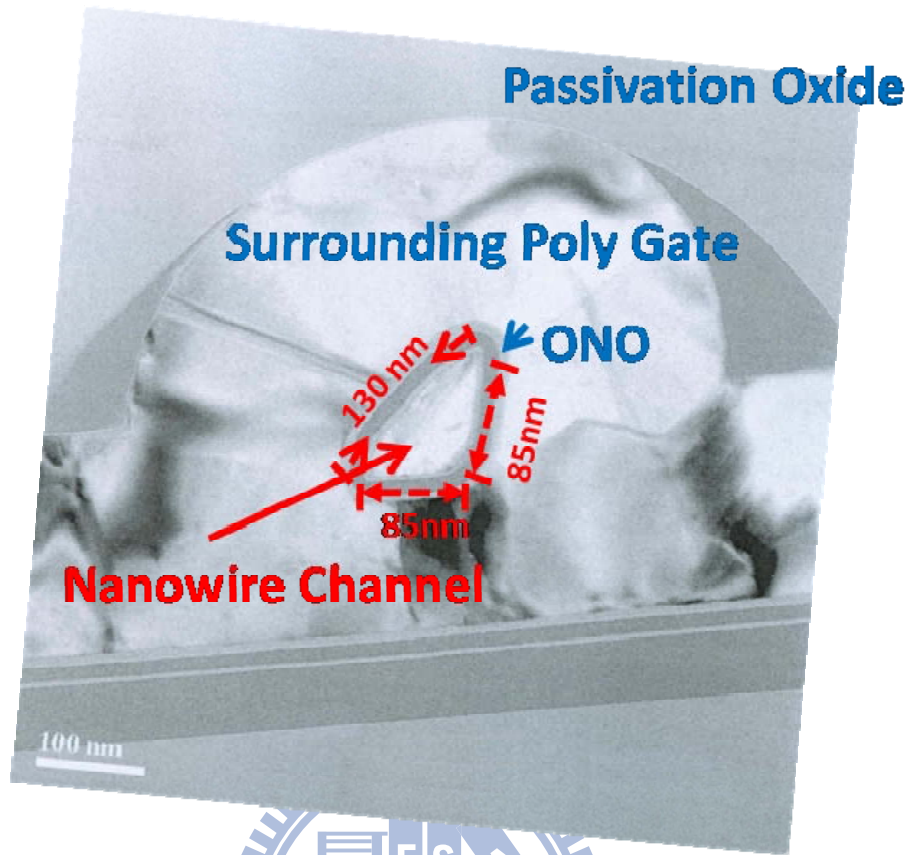


Fig. 2-6 The cross-section TEM image after patterning gate.

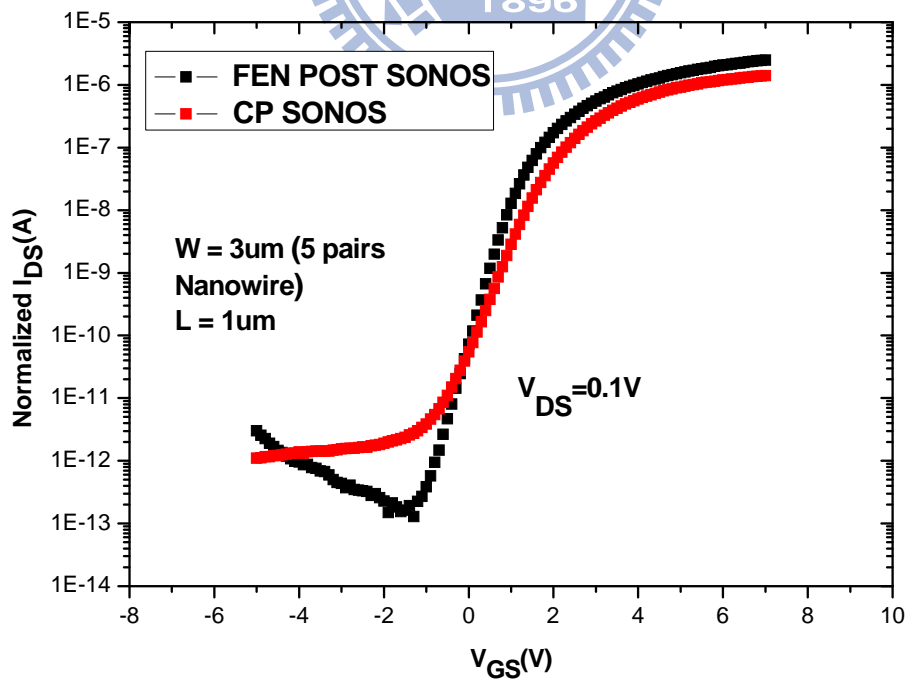


Fig. 2-7 Transfer characteristics of the CP and the proposed FEN POST SONOS devices.

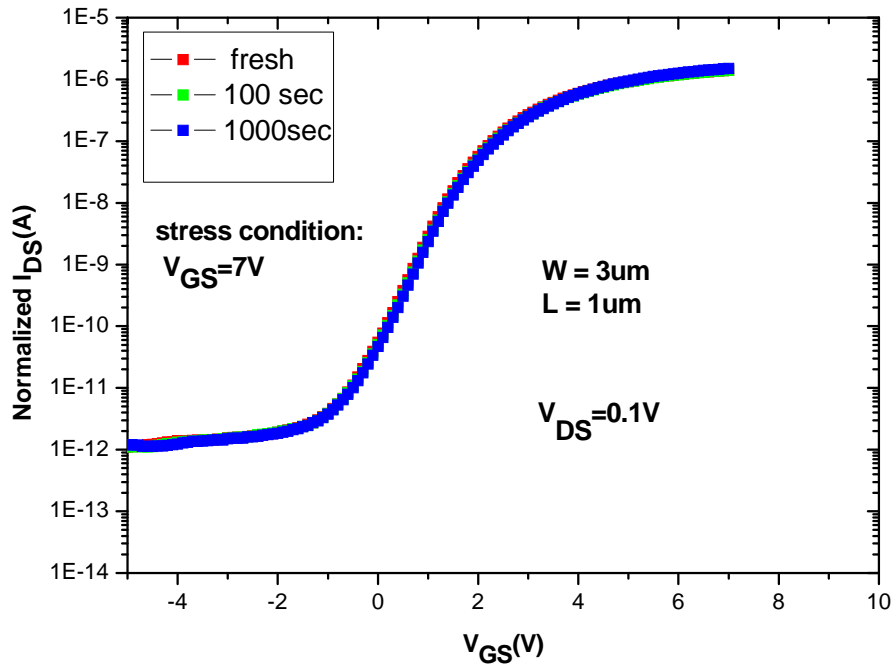


Fig. 2-8(a) Transfer characteristics of the CP SONOS device after DC stress at $V_{GS} = 7$ V condition.

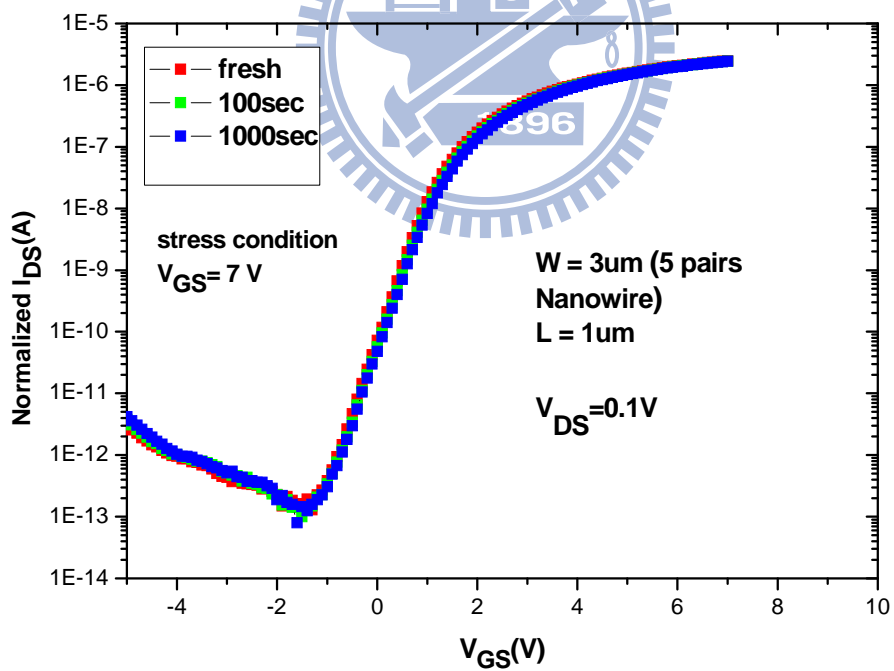


Fig. 2-8(b) Transfer characteristics of the FEN POST SONOS device after DC stress at $V_{GS} = 7$ V condition.

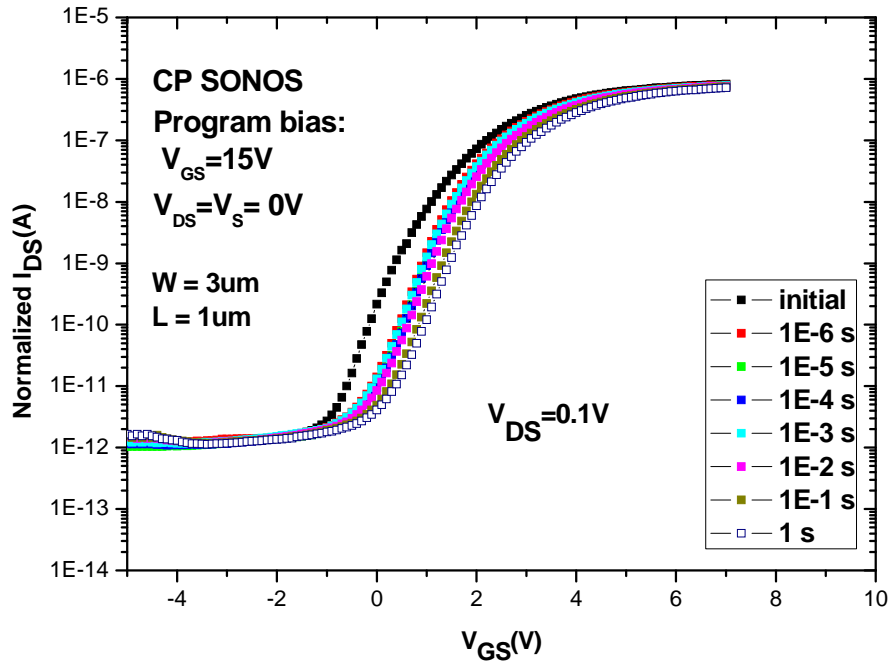


Fig. 2-9 Transfer characteristics of the CP SONOS device with various programming times at $V_{GS} = 15 V$.

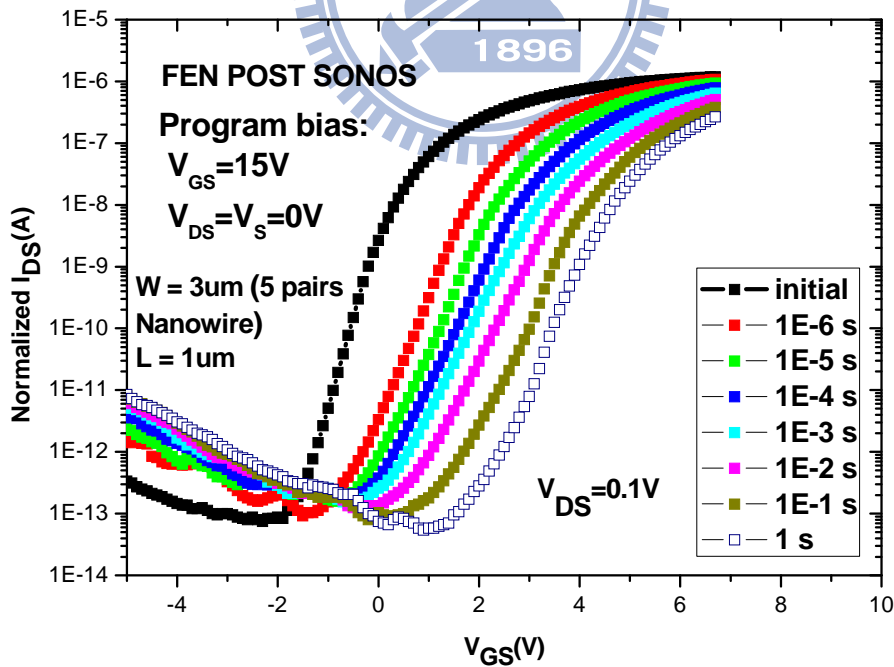


Fig. 2-10 Transfer characteristics of the FEN POST SONOS device with the various programming times at $V_{GS} = 15 V$.

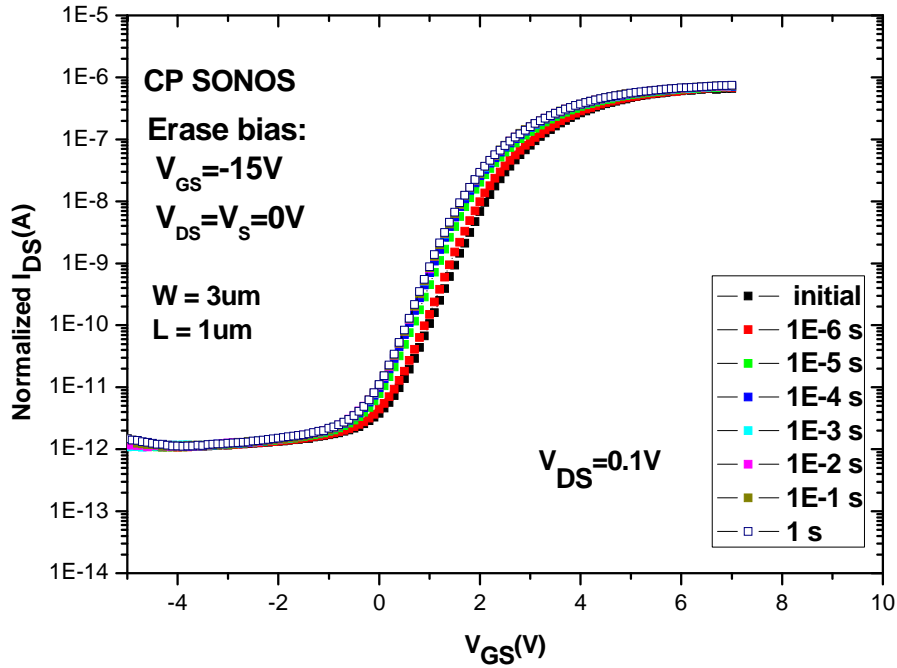


Fig. 2-11 Transfer characteristics of the CP SONOS device with the various erasing times at $V_{GS} = -15$ V.

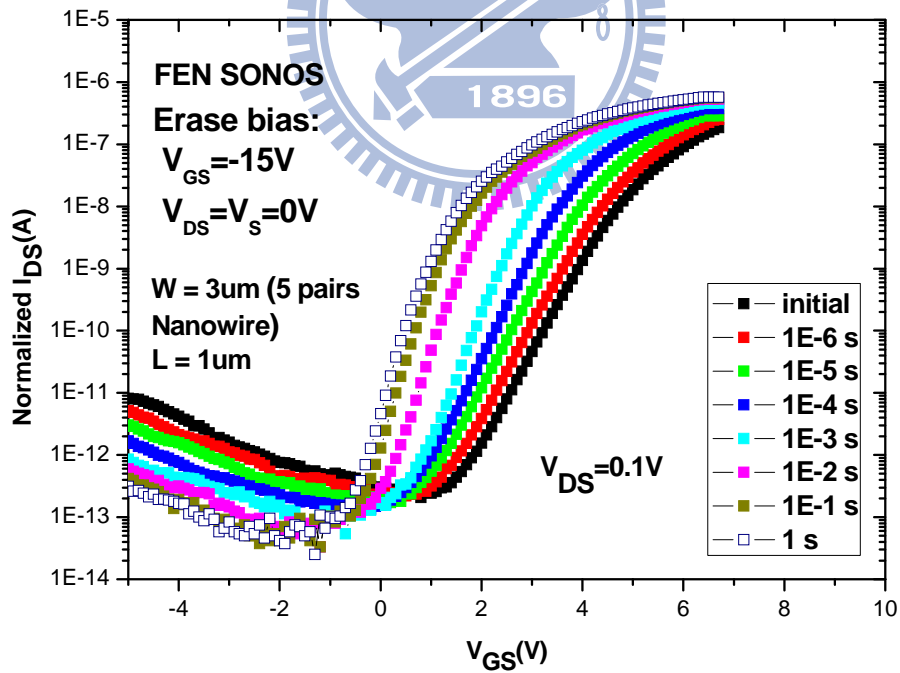


Fig. 2-12 Transfer characteristics of the FEN POST SONOS device with the various erasing times at $V_{GS} = -15$ V.

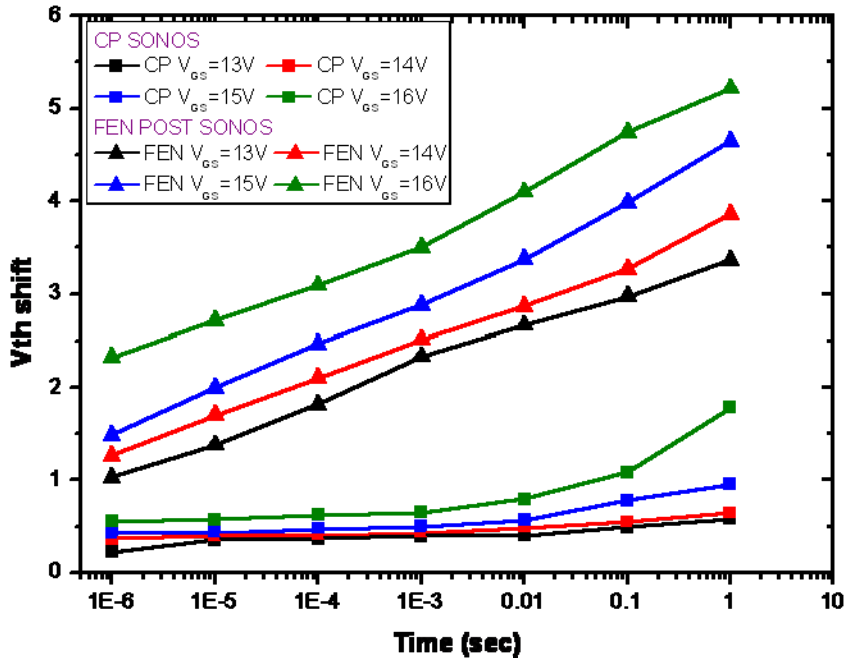


Fig. 2-13(a) V_{th} shifts after programming for the CP SONOS and FEN POST SONOS devices with various gate voltage

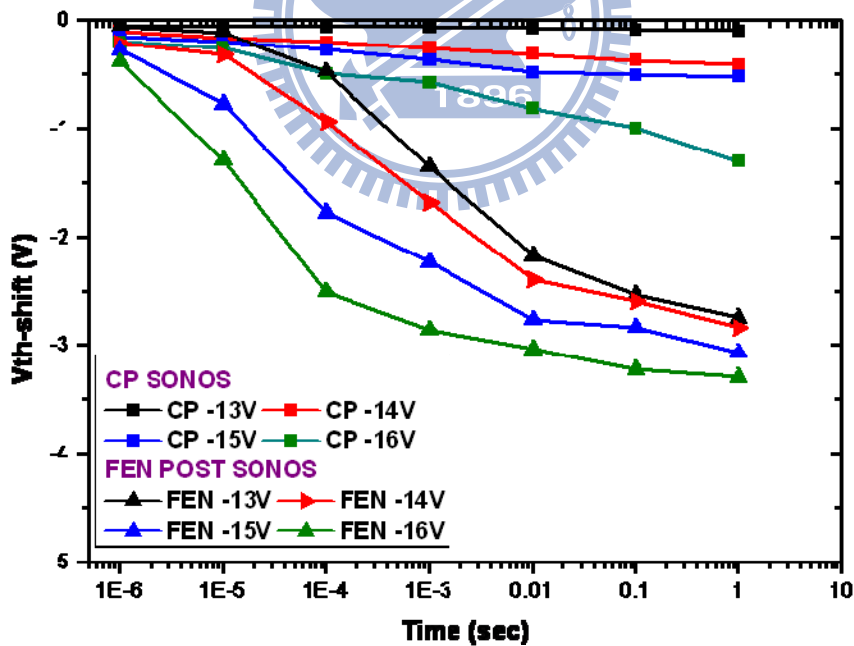


Fig. 2-13(b) V_{th} shifts after erasing operation for the CP SONOS and FEN POST SONOS devices with various gate voltage.

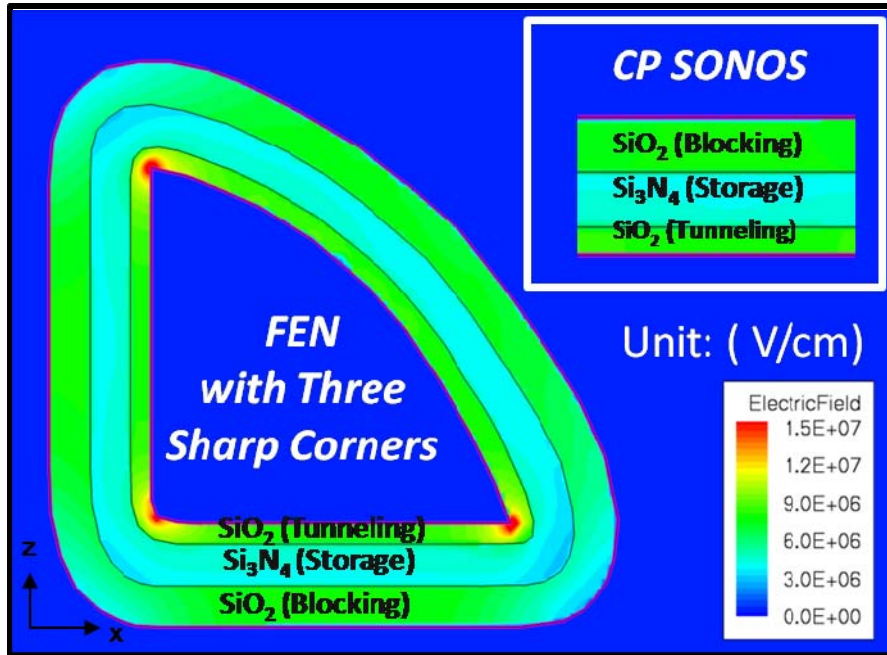


Fig. 2-14 The distribution of electrical field across the stacked ONO dielectrics for the CP and FEN POST SONOS devices at $V_{GS} = 15$ V.

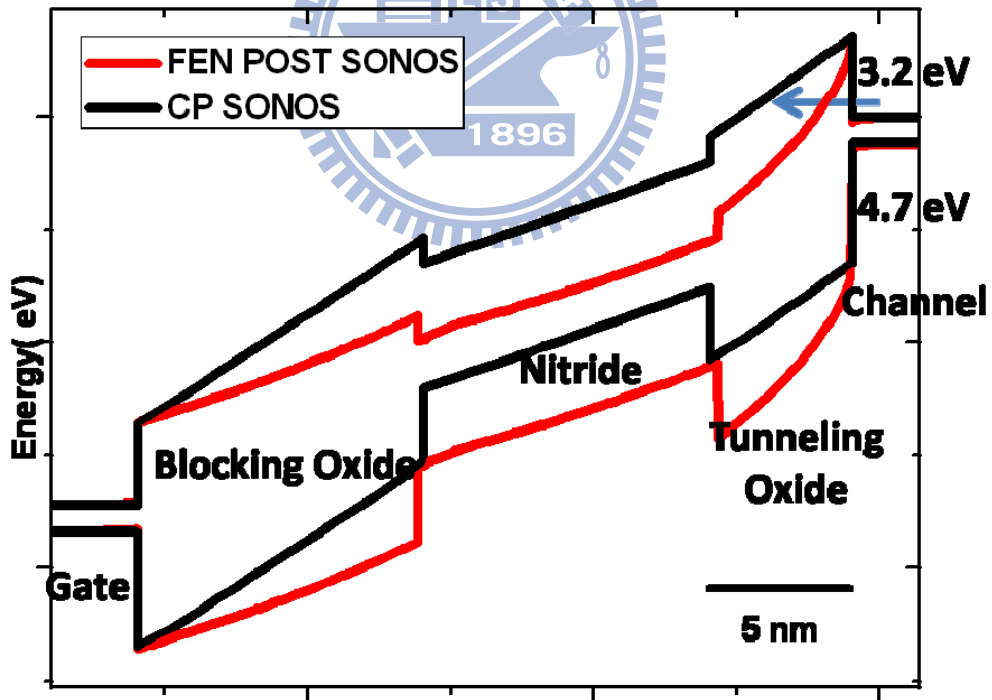


Fig. 2-15 The band diagrams of the CP and FEN POST SONOS devices at $V_{GS} = 15$ V.

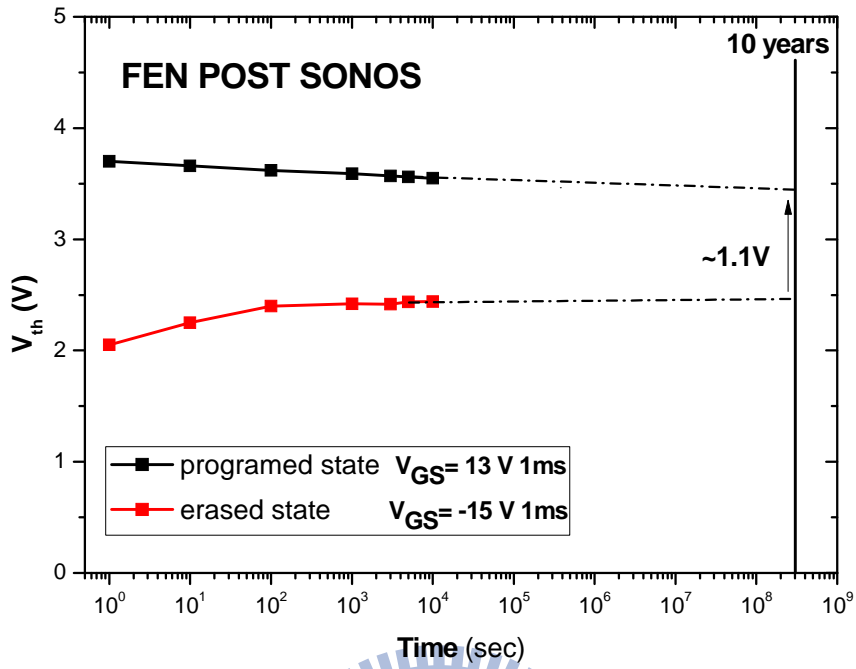


Fig. 2-16 Retention characteristic of the FEN POST SONOS device after 10^4 P/E cycles.

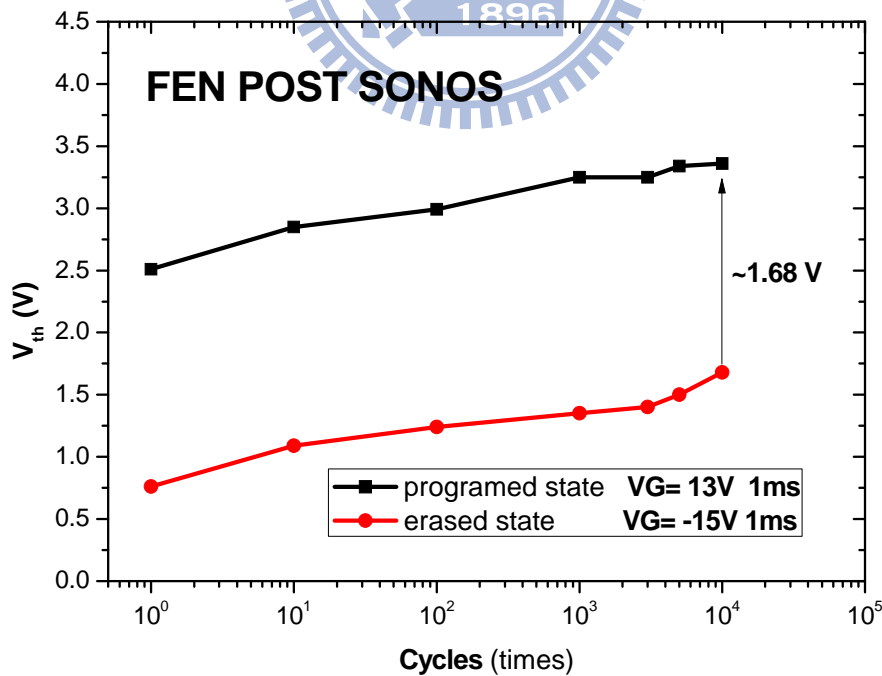


Fig. 2-17 Endurance characteristic of the FEN POST SONOS device.

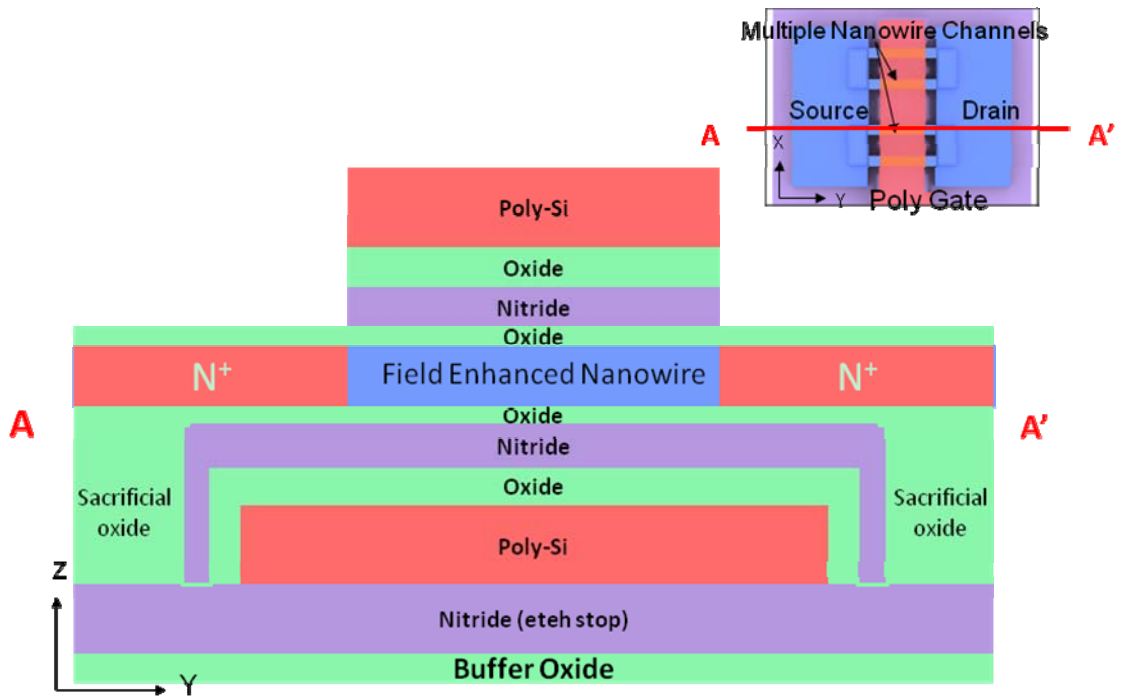


Fig.3-1 The cross-section schematic image after patterning the in-situ doped poly-Si gate

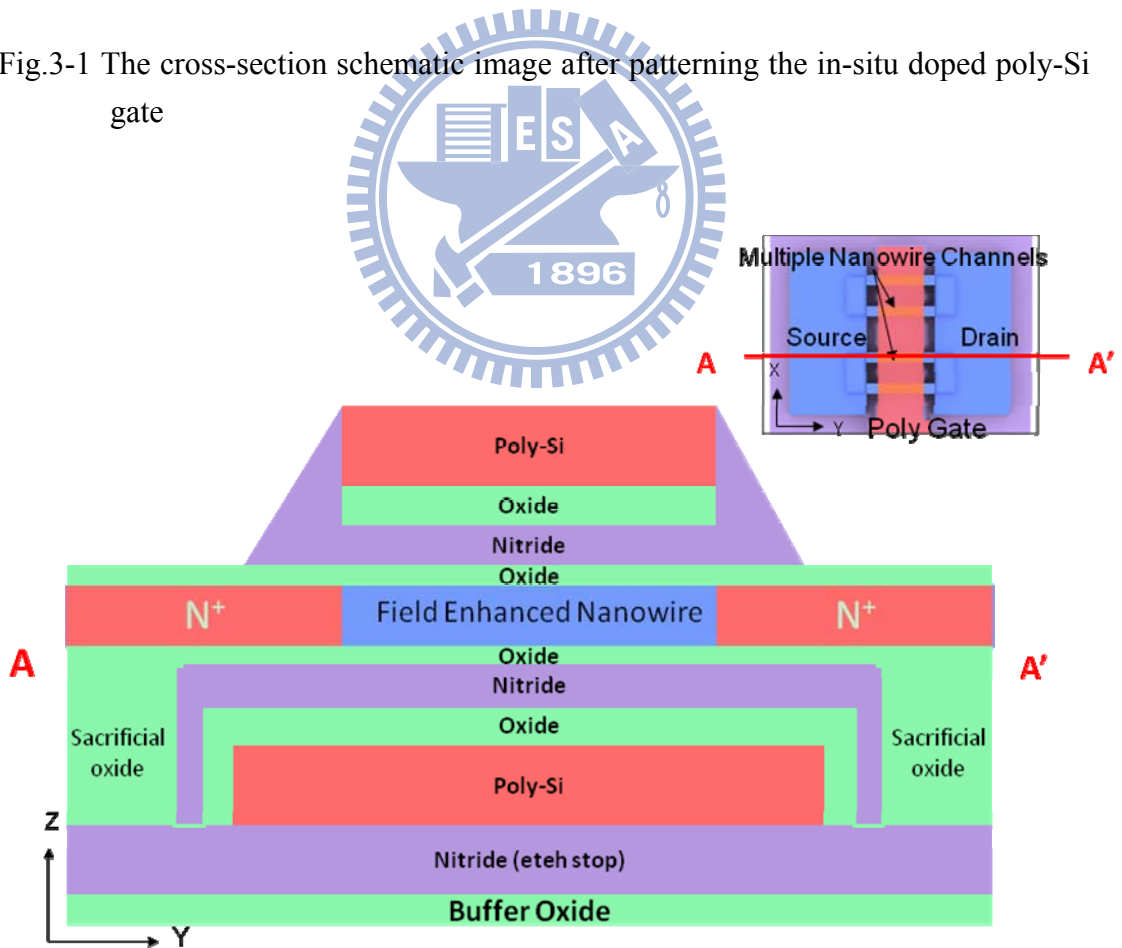


Fig.3-2 The cross-section schematic image after nitride spacers formed.

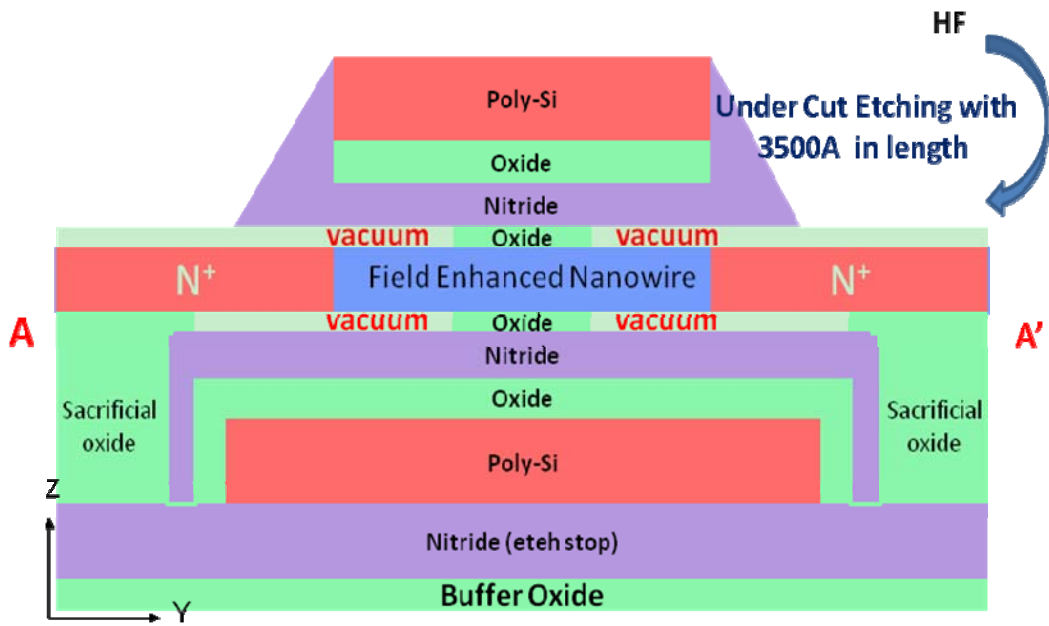


Fig. 3-3 The cross-section schematic image after tunneling oxide etched with 1:10 diluted BOE

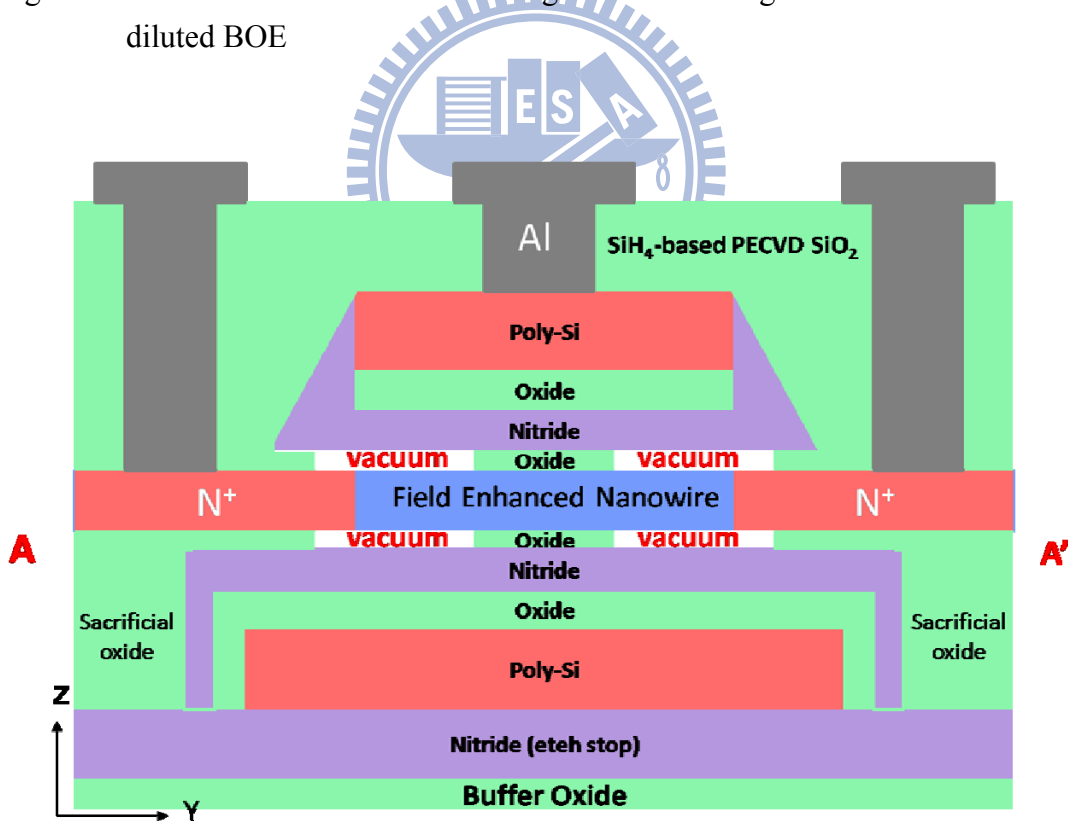


Fig. 3-4 The cross-section schematic image after patterning Al metal pads.

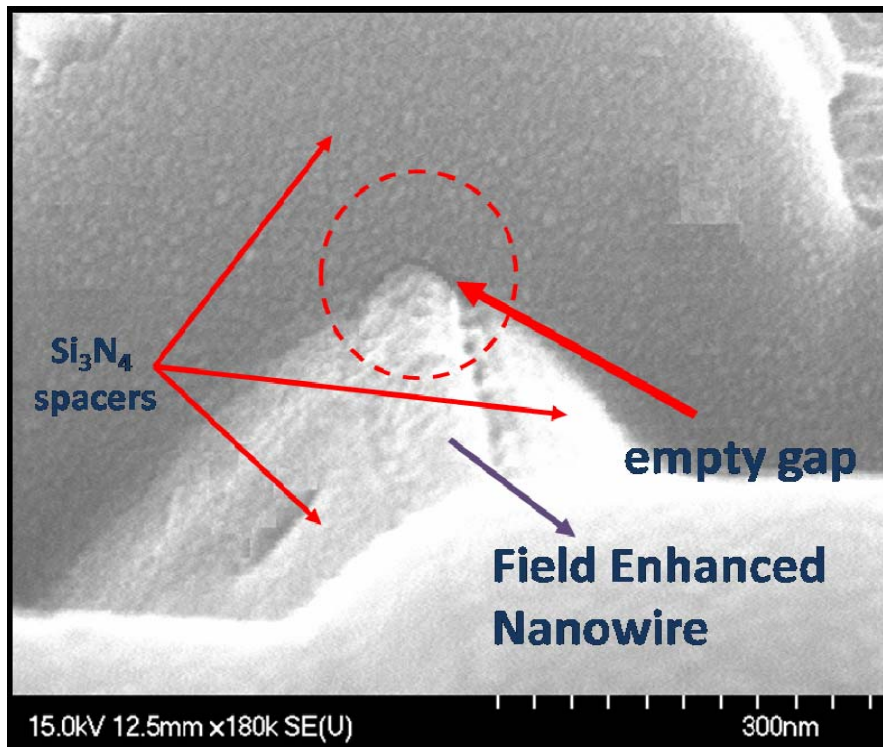


Fig. 3-5 The tiled-view SEM image of the FEN POST SONVAS device

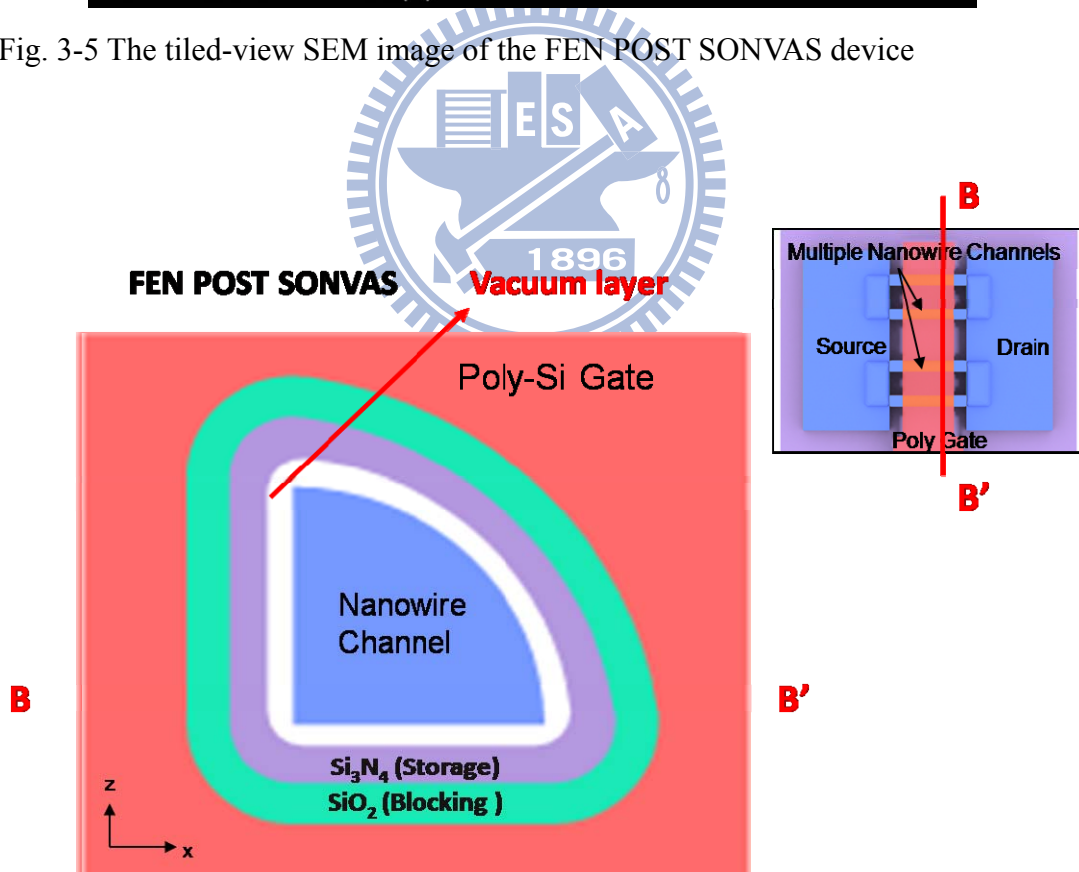


Fig. 3-6 The cross-section schematic image of nanowire channel with vacuum tunneling layer.

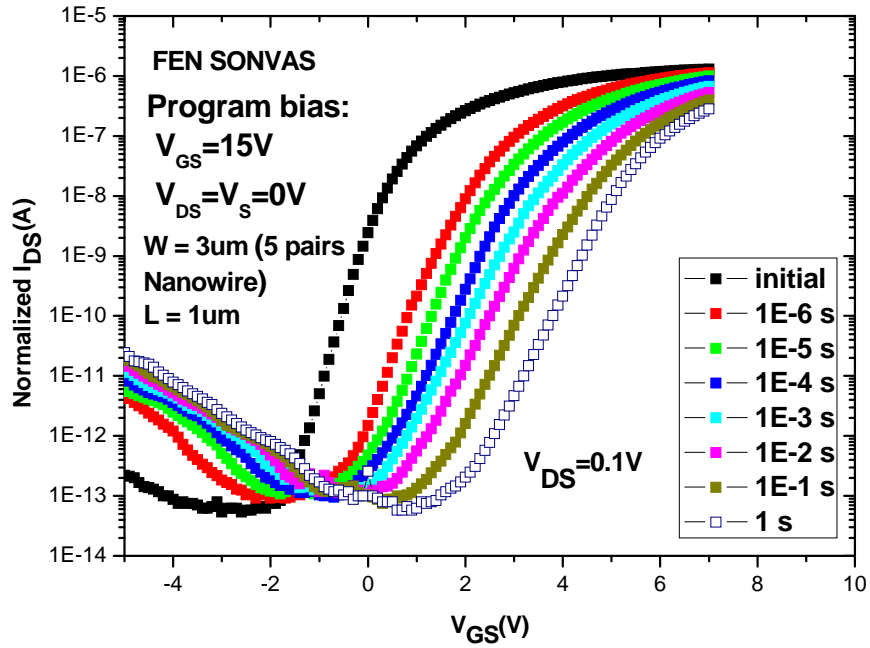


Fig. 3-7 Transfer characteristics of the FEN POST SONVAS device with various programming times at $V_{GS} = 15$ V.

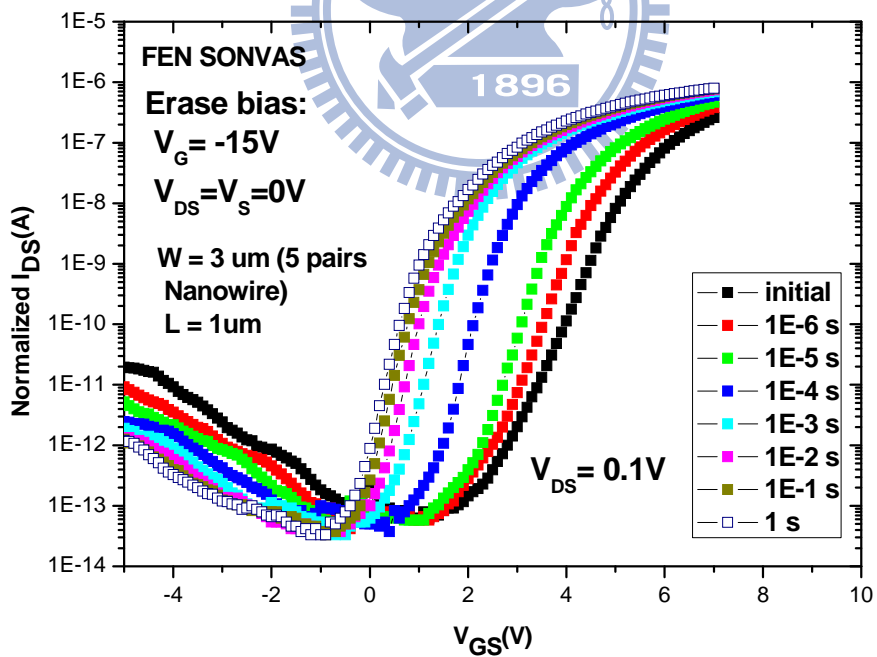


Fig. 3-8 Transfer characteristics of the FEN POST SONVAS device with various erasing times at $V_{GS} = 15$ V.

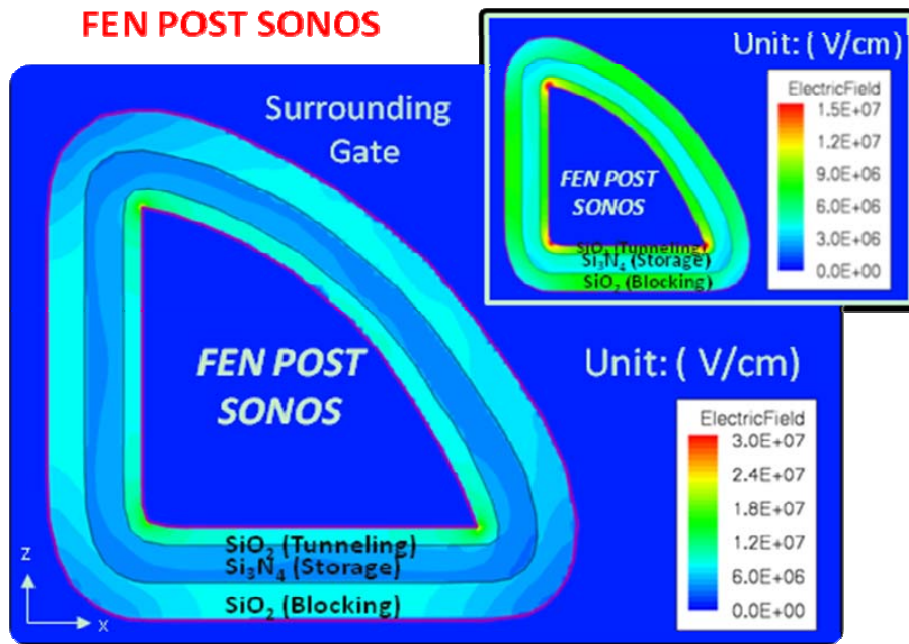


Fig. 3-9 The distribution of electrical field across the stacked ONO dielectrics for the FEN POST SONOS devices at $V_{GS} = 15$ V.

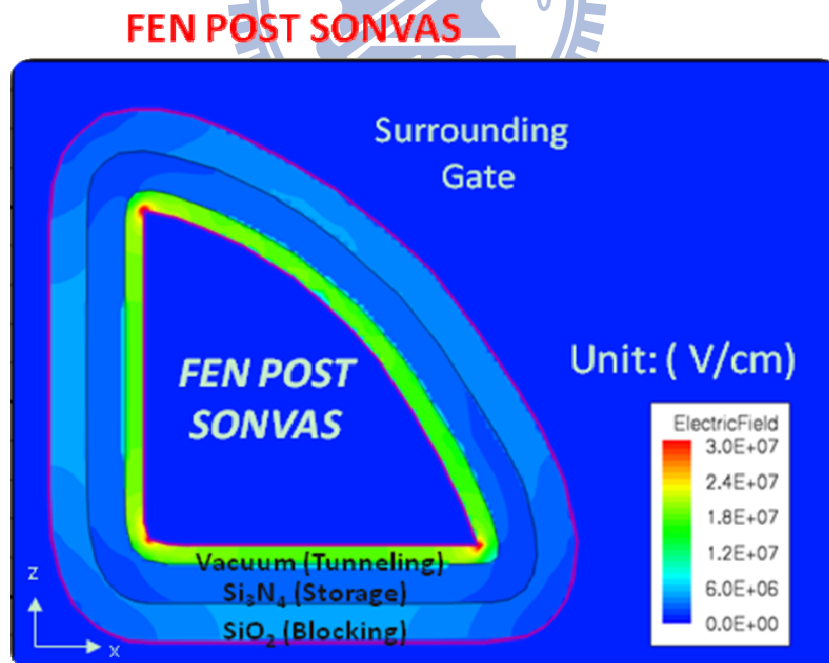


Fig. 3-10 The distribution of electrical field across the stacked ONO dielectrics for the FEN POST SONVAS devices at $V_{GS} = 15$ V.

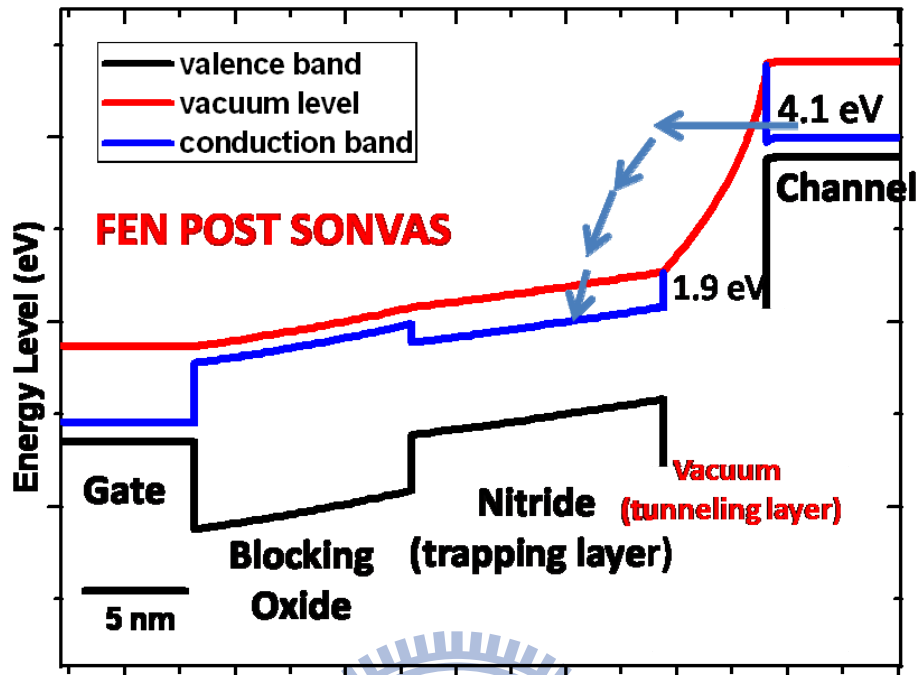


Fig. 3-11 The band diagrams of the FEN POST SONVAS devices at $V_{GS} = 15$ V.

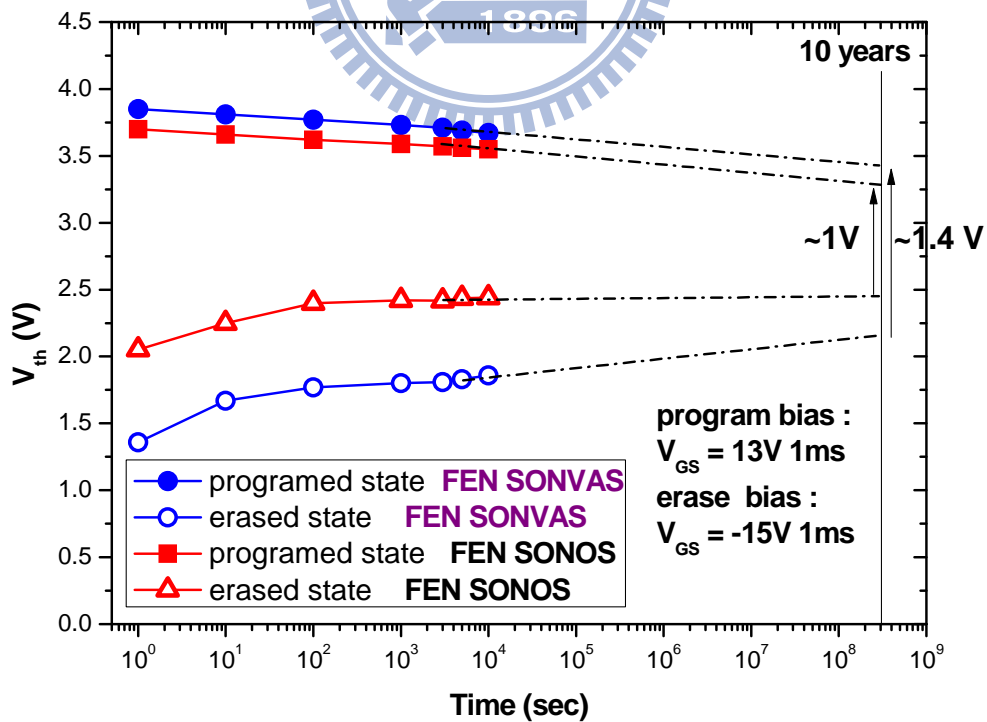


Fig. 3-12 Retention characteristic of FEN POST SONVAS device after 10^4 P/E cycles.

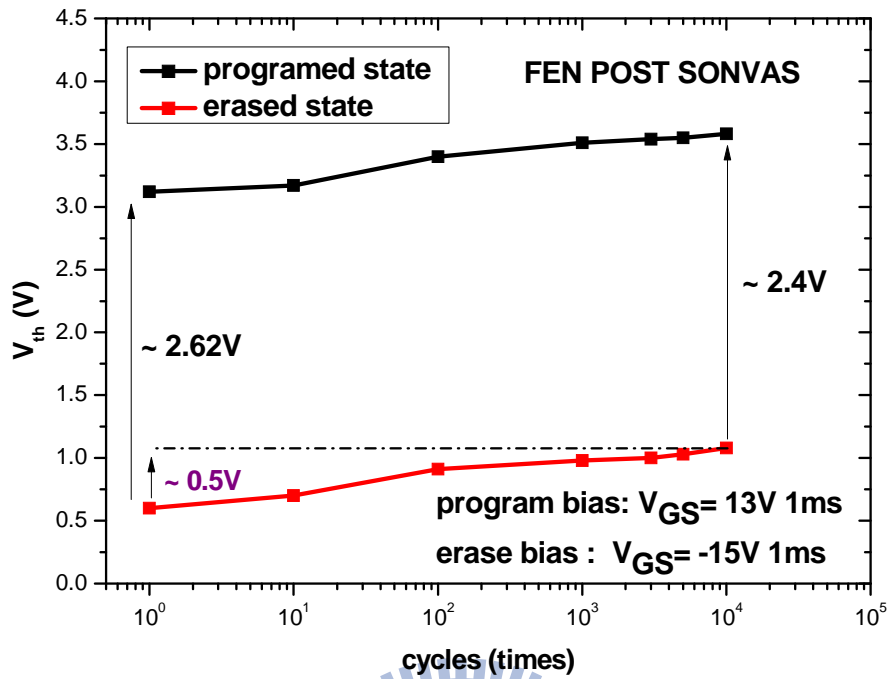


Fig. 3-13 Endurance characteristic of the FEN POST SONOS device.

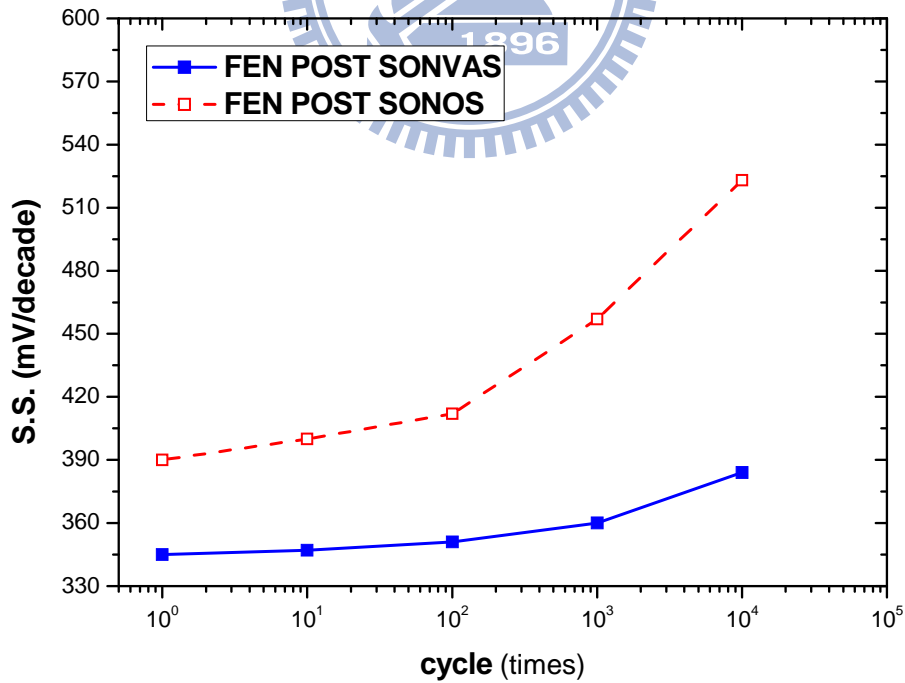


Fig. 3-14 The subthreshold swing of the FEN POST SONOS and FEN POST SONVAS devices after P/E cycles.

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(96 年 9 月~98 年 9 月)

論文題目：具電場增強式奈米線結構之複晶矽薄膜電晶體非揮發性記憶體
之研究

Study on the Poly-Si TFT Nonvolatile Memory with a
Field-Enhanced-Nanowire Structure