# 國立交通大學

電子工程學系 電子研究所碩士班

# 碩士論文

氮化矽快閃記憶體的暫態行為模擬及其應用

# Numerical Simulation of Transient Behaviors for Nitride Based Flash Memory and its Applications.

研 究 生：杜 文 仙

指導教授：汪 大 暉 博士

中華民國 九十八 年 六 月

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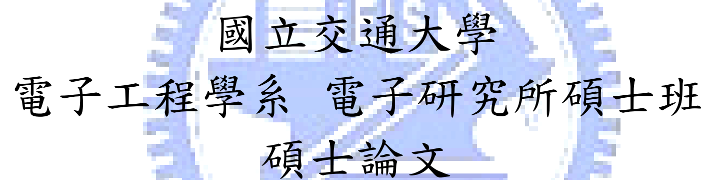

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碩士論文

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## 摘要

為了了解以及改善快閃記憶體所有暫態操作行為模式，建立一個可以包含寫入、讀出，以及抹除的行為魔性是需要的。藉由所建立出的模型，可以最佳化氮化矽快閃記憶體的儲存能力。在之前的研究裡面，有關寫入以及讀出的模型已被成功的建立以及驗證。此論文中，將重點先放在有關抹除的暫態行為模型建立以及驗證。藉由建立出來的模型，不但可用來成功的模擬 n 型閘極以及 p 型閘極的 SONOS 結構快閃記憶體暫態行為，也可以用在 TANOS(鉭化矽閘極+氧化鋁介電層)結構的快閃記憶體。將所有建立的暫態行為模型結合，可以同時用來最佳化 SONOS 以及 TANOS 的製程條件。由實驗結果發現，對於 SONOS 快閃記憶體來說很難同時達到三種行為的要求，但對於 TANOS 來說，可以得到一最佳化的厚度範圍來滿足所有操作模式的需求。此外，由建立的模型可以發現喘痛用外插方式粹取讀取條件的方式是會低估其可以容許的讀取偏壓。最後，由模型可以預期帶未來走向圓形結構的快閃記憶體是最有淺力取代現有的平面結構快閃記憶體選擇，其在不但免疫雜訊更可以有較大的儲存空間。

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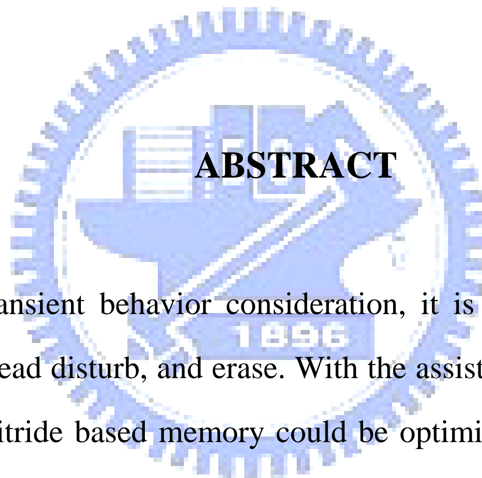


## ABSTRACT

For the overall transient behavior consideration, it is necessary to establish the model for program, read disturb, and erase. With the assist of model, the issue for the limited window of nitride based memory could be optimized. In the previous study, program and read disturb characteristics is well built. Here, we focus on the erase behavior at the first place. The erase characteristics of a SONOS-based structure are emulated not only for $n^+$-poly and $p^+$-poly gates but also for TaN-gate+$Al_2O_3$ combination. By incorporating all our work, performances including program, erase, and read disturb can be reviewed for both SONOS and TANOS devices. Unsurprisingly, it is hard to satisfy all requirements by using a SONOS device. In a TANOS device, an optimal bottom oxide thickness can be specified with the consideration of the three factors simultaneously. Moreover, it is found that conventional extrapolation methodology is inadequate to predict the lifetime of a TANOS device and tends to under-estimate the tolerable read bias. Eventually, the cylindrical cell with the geometrical benefit could be an prominent candidate to for the future Flash structure. In our study, the cylindrical cell is not only immune to noise but also has improved window.

# 致謝

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# Chapter I

# Introduction

Unlike a floating gate device, the structures of a SONOS-based device are still controversial. Various materials are tried to replace the poly-gate, the top oxide, and the nitride layer to improve the performances including program, erase, and read disturb [1-5]. Even for a TANOS device, which is the most mature structure among them, its optimal thickness of the three stacks is not concluded yet [1-2]. An accurate model is thus essential to predict operation performances of a SONOS based structure. In our previous studies, a transient model is developed and both program and read disturb behaviors have been well emulated [8-9]. In this thesis, erase model with the cogitation on electrons back tunneling (EBT) is developed. This unwanted gate injection process restricts the erase capability in a SONOS cell [1], [5]. Although much works have been demonstrated to improve erase performance by replacing $n^+$-poly with $p^+$-poly as gate [5-7] or using a TANOS structure [1-2], a consistent erase model for them had not been accomplished. In this paper, with the help of developed model, process margins for either a SONOS cell or a TANOS cell can be examined according to its program speed, read disturb, and erase performance inclusively. Otherwise, it has proved that there are many benefits for SONOS with gate-all-around geometry.[10-11]. With the superiority of its structure, it needs lower operation bias for both erase and program operation. In the thesis, operation model and optimization is taken into discuss.

There are five chapters in this thesis. Chapter 1 is Introduction and we would give a brief outline of the dissertation. Chapter 2 erase model and mechanism is constructed and emulated. The experiments and simulations are well cogitated and coincident to confirm the accuracy of the model. Chapter 3 is based on the accomplished model

above and constructs the overall consideration for process margin for SONOS or TANOS. Otherwise, the suitable material of gate to fulfill the requirement takes into account. With the established model above, the transient erase model for gate-all around geometry SONOS cell is analyzed in Chapter 4. Eventually, the summary and conclusion will be taken in Chapter 5.

# Chapter 2

# Erase Mechanism and Model for SONOS cell

## 2.1 Introduction

To predict the over all operation performance for SONOS base structure, the accurate model is essential. The program transient and read disturb model has been established and well emulated [8-9]. However, the erase model has not been accomplished. The unwanted gate injection process, which restricts the erase capability in a SONOS cell, has been notorious [3-4]. In this chapter, this electron back tunneling (EBT) current, which result to erase saturation, is analyzed for its mechanism and taken into the complimentary erase model.

From the developed erase model above, verification between the experiment data and simulation is needed to confirm. To improve the erase performance, much works have been demonstrated to improve erase performance by replacing $n^+$-poly with $p^+$-poly as gate [5-7]. The erase window, however, does not increase as much as predicted with $p^+$-poly gate instead of $n^+$-poly gate. The transient model, which emulates well for both types of SONOS is applied to get the optimum process margin.

## 2.2 Erase Mechanism

Fig.2.1 illustrates the schematic energy band diagram and current flows under erase operation. A competition between gate electrons ($J_{EBT}$) and substrate holes ($J_h$) can be identified as a key factor to an erase characteristic. Other possible factors such as capture/emission currents contributed from nitride traps and currents tunneled out from a nitride layer are also indicated. The trapped charges exhibit the probability to emit via FP emission process and subsequently tunnel out through the top oxide .

However, in Fig.2.2, it is found that temperature dependence of an erase transient is irrelevant. Possible explanations are as follows; first, the hole barrier between nitride and $SiO_2$ [12] is large enough to retard out-going holes ($J_{h\text{-}out}$) from a nitride layer to the gate. Second, during erase operation, electric field across the bottom oxide decrease and out-going electrons ($J_{e\text{-}out}$) from nitride thus become less important. During erase, the injected hole will decrease the storage charge built-up potential, which reduces the bottom oxide field but results to the increase of top oxide feld continuously. Therefore, the tunneling current through bottom/top oxide will decrease/increase respectively due to the field dynamic status. $V_T$ shift ($\Delta V_T$) decrease and eventually saturates when $J_{EBT}$ balances with $J_h$.

All of the tunneling currents are selected by the top/bottom oxide electric field. The three tunneling mechanisms are FN tunneling, direct tunneling and Modified FN tunneling. If the tunneling barrier determined by the oxide fields is larger than the physical barrier ($\Phi_{so}$) determined by block layer (oxide) conduction/valance band difference with gate (silicon), the current is from FN tunneling. With the decreasing bottom oxide electric field, the tunneling barrier is less than $\Phi_{so}$ but larger than band difference between block oxide and nitride ($\Phi_{on}$), the current is from direct tunneling. Eventually, when the tunneling barrier reduces to be smaller than $\Phi_{so}$ and $\Phi_{on}$, the current comes from the modified FN tunneling. The formulas for all the tunneling current included above are summarized in Table.1.

The simulation flowchart and critical parameters are given in Fig.2.3.

## 2-3 Erase Saturation from Back Gate Tunneling

Using a $p^+$-poly gate to reduce a gate injection current is a popular way [5-7]. Comparing with an $n^+$-poly gate, no inverted electrons can be supplied but only valence electrons, which are 1eV lower than that of an inverted one. Unfortunately, early erase saturation is still observed in literatures [5-7] and in our experiments.

According to the literature [13], Shockley-Read-Hall ($J_{SRH}$) tunneling, band- to-trap-to -band ($J_{BTB}$) tunneling and the band-to-band ($J_{BB}$) tunneling process are all the possible mechanism for the back gate tunneling current. Back gate current from $J_{SRH}$ , which is shown in Fig.2.4 (a), come from the recombination /generation via top gate traps ($J_{dep}$) and interface traps ($J_{Dit}$) existing between gate and block layer. The gate current density from SRH mechanism verse gate bias is given in Fig.2.4 (b). On the other hand, back gate current from $J_{BTB}$, which is shown in Fig.2.5 (a), come from electrons tunneling from valance band to the most active bulk traps in the depletion region, which locates near the middle of bandgap, jump up to conduction band, and then tunnel to bulk ($J_a$) and electrons near the poly gate/block oxide interface will tunnel from valance band to interface states directly, instead of tunneling to bulk traps ($J_b$). The gate current density from BTB mechanism verse gate bias is also given in Fig.2.5 (b). Moreover, back gate current from $J_{BB}$, which is shown in Fig.2.6 (a), comes from electrons gate valance band tunneling through gate energy gap to conduction band when electron tunneling barrier is larger than gate energy gap. The gate current density from BB mechanism verse gate bias is also given in Fig.2.6 (b). From the analysis and comparison of three mechanisms, $J_{BB}$ could possibly the dominant current of EBT since its magnitude is larger several order than others.

## 2-4 Comparison of $p^+$ poly gate and $n^+$ poly gate SONOS

To confirm the erase model established above, erase characteristics of a SONOS cell with an $n^+$-poly gate and a 1.5nm bottom oxide are then emulated in Fig.2.7 and acceptable results are obtained. In Fig.2.8, a good agreement is also found between simulation and measurement of a $p^+$-poly gate SONOS.

With the proposed model, $V_T$ shifts before erase saturation occurs are compared for different $\phi_B$ under three applied gate biases for both $p^+$-poly and $n^+$-poly gate

SONOS with a same ONO stack (8nm/6nm/3nm). Form the Fig.2.9,if the $\phi_B$ increase as much as 1eV, which is nearly the bandgap of silicon, the erase window should enhance to 5V. However, the erase window enhances for the $p^+$-poly comparing to the $n^+$-poly one is not much as expect. It is clear that the effect of using a $p^+$-poly gate does not increase the tunneling barrier of back tunneling electrons by 1eV but only about 0.4eV. That is why the reduction of erase saturation is always limited by using a $p^+$-poly gate.

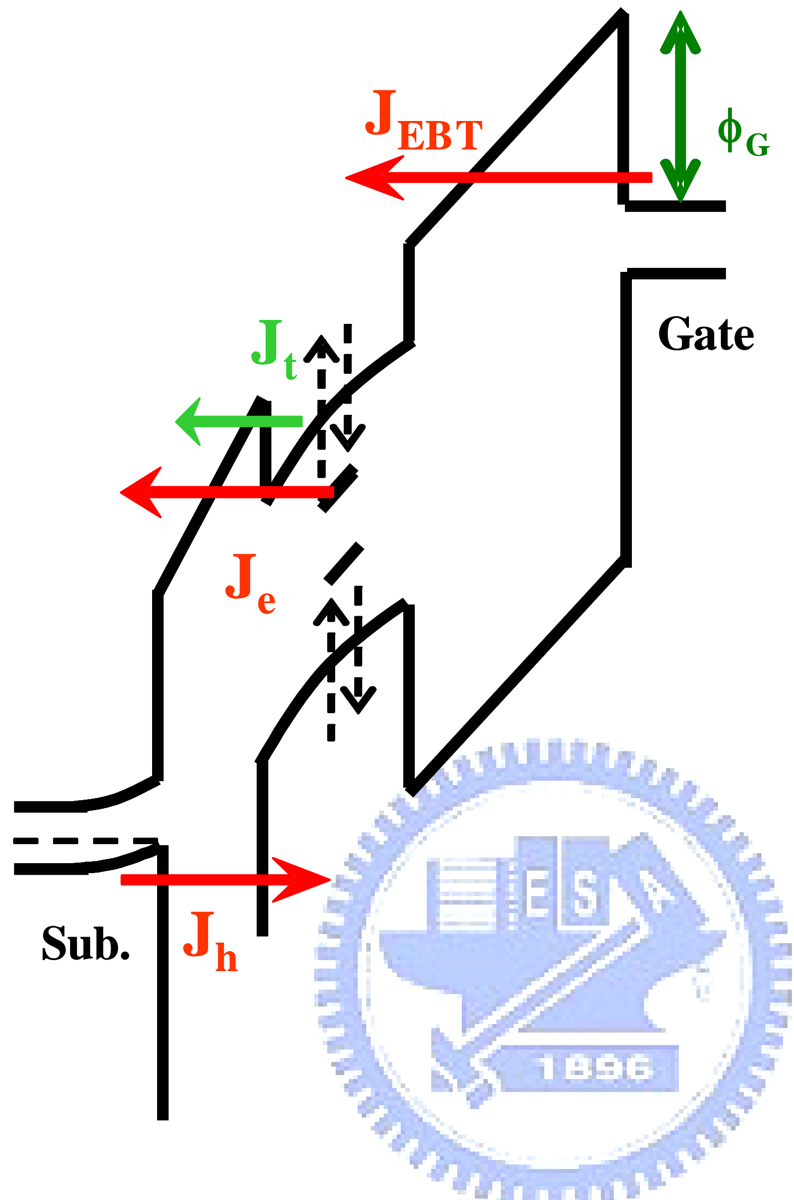



**Fig.2.1 Schematic energy band diagram and current flows during erase operation for a SONOS cell.**

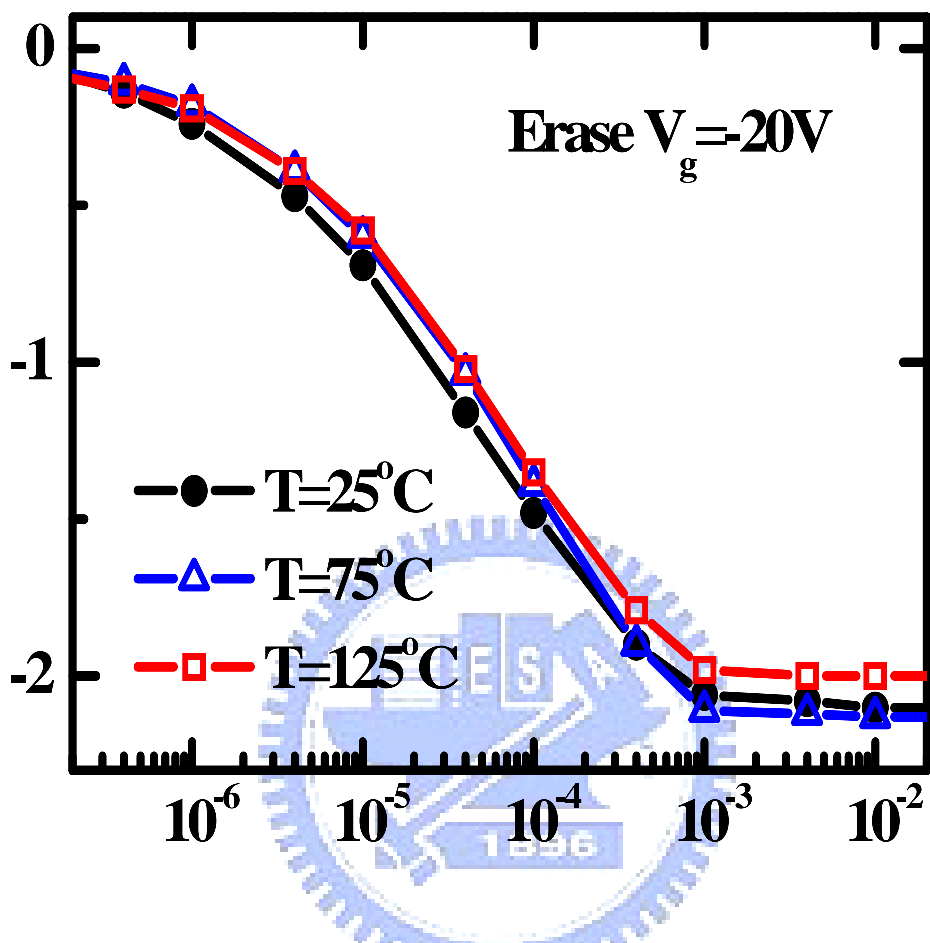



**Fig.2.2 Erase transient at different operation temperatures (T=25°C, 75°C, and 125°C, respectively) for a SONOS cell with ONO stack is 8nm/6nm/3nm.**

$$J_{FN}=A\cdot E_{OX}^{2}\cdot\exp\left(-\frac{B}{E_{OX}}\right)\text{ where }A=\frac{q^{3}}{16\pi^{2}\hbar\Phi_{1}},B=\frac{4}{3}\frac{\sqrt{2m_{OX}}}{q\hbar}\Phi_{1}^{3/2}$$

$$J_{DT}=A\cdot E_{OX}^{2}\cdot\exp\left(-\frac{B}{E_{OX}}\right)\text{ where }B'=B\cdot\left(1-\left(\frac{E_{OX}\cdot t_{OX}}{\Phi_{1}}\right)\right)^{3/2}$$

$$J_{MFN}=\frac{m_{0}}{m_{OX}}\cdot\frac{q^{3}}{16\pi^{2}\hbar}E_{OX}{}^{2}\frac{1}{\left[(q\Phi_{1})^{1/2}-(q\Phi_{1}-qE_{OX}d_{OX})^{1/2}+\gamma\sqrt{m_{N}/m_{OX}}(q\Phi_{1}-q\Phi_{2}-qE_{OX}d_{OX})^{1/2}\right]^{2}}$$
$$\cdot\exp\left[-\frac{4\sqrt{2m_{OX}}\left[(q\Phi_{1})^{3/2}-(q\Phi_{1}-qE_{OX}d_{OX})^{3/2}\right]+\gamma4\sqrt{2m_{N}}(q\Phi_{1}-q\Phi_{2}-qE_{OX}d_{OX})^{3/2}}{3q\hbar E_{OX}}\right]$$

$$\text{where }\gamma=\frac{\varepsilon_{N}}{\varepsilon_{OX}}$$

$$J_{loss}=Q\cdot v_{E}\cdot\exp\left(-\frac{\Phi_{t}-q\sqrt{\frac{qE}{\pi\varepsilon_{N}}}}{kT}\right)\cdot P_{TUN}\text{ where }P_{TUN}=\exp\left(-\frac{4}{3}\frac{\sqrt{2m_{OX}}}{q\hbar E_{OX}}\Phi_{2}^{3/2}\right)$$

**where $\Phi_1$ is the conduction band offset butween Si/SiO**

**$\Phi_2$ is the conduction band offset butween SiN/SiO**

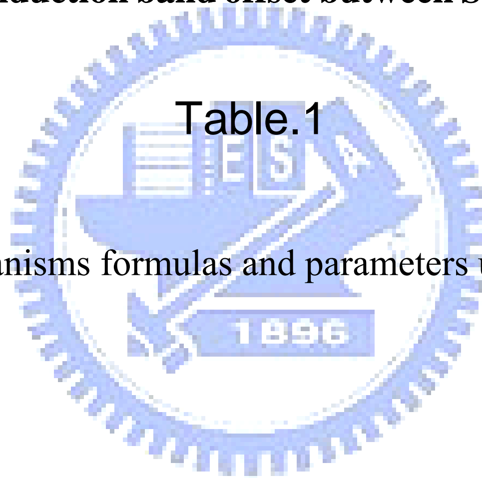


Table.1

Tunneling mechanisms formulas and parameters used for simulation

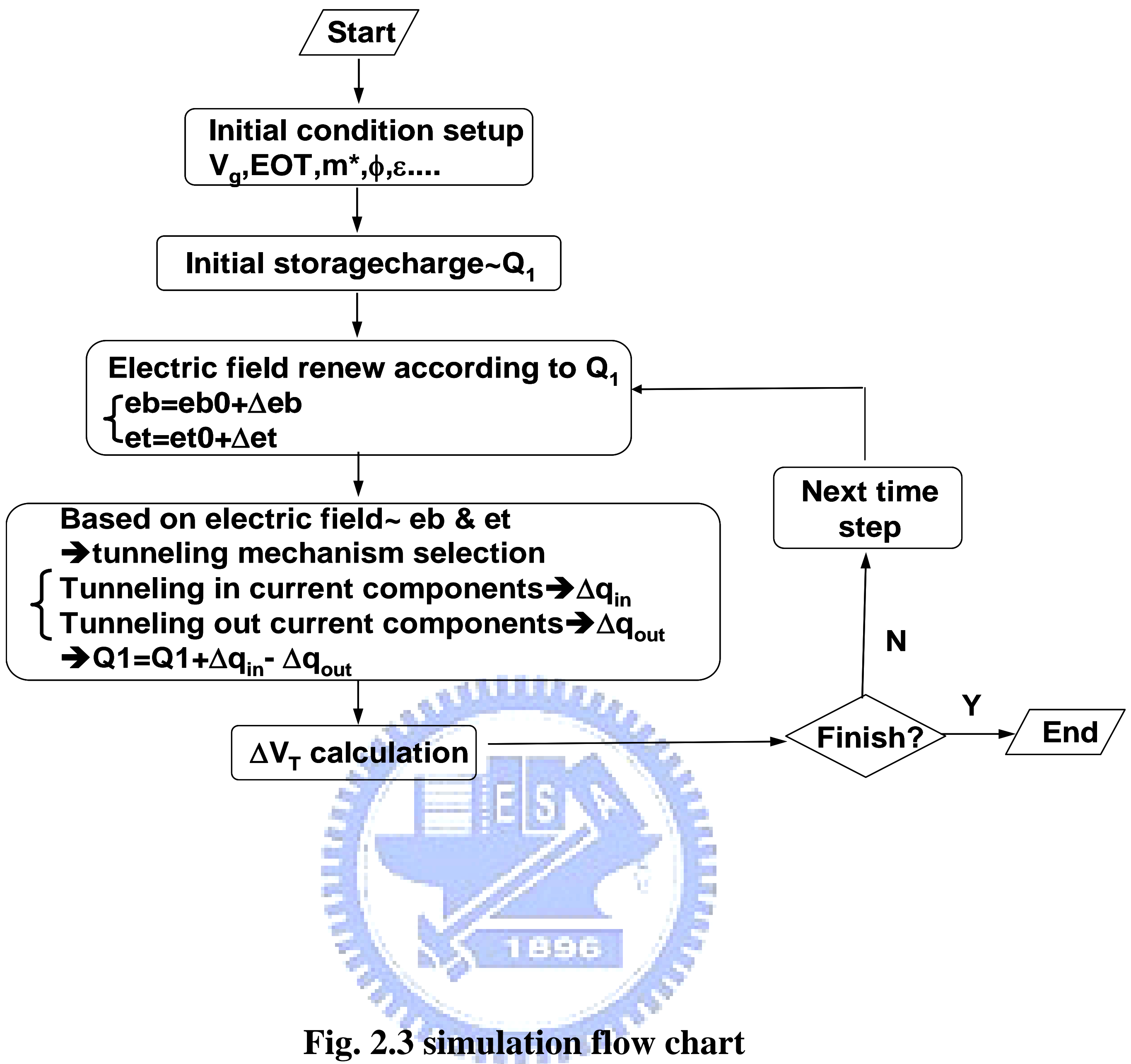



Fig. 2.3 simulation flow chart

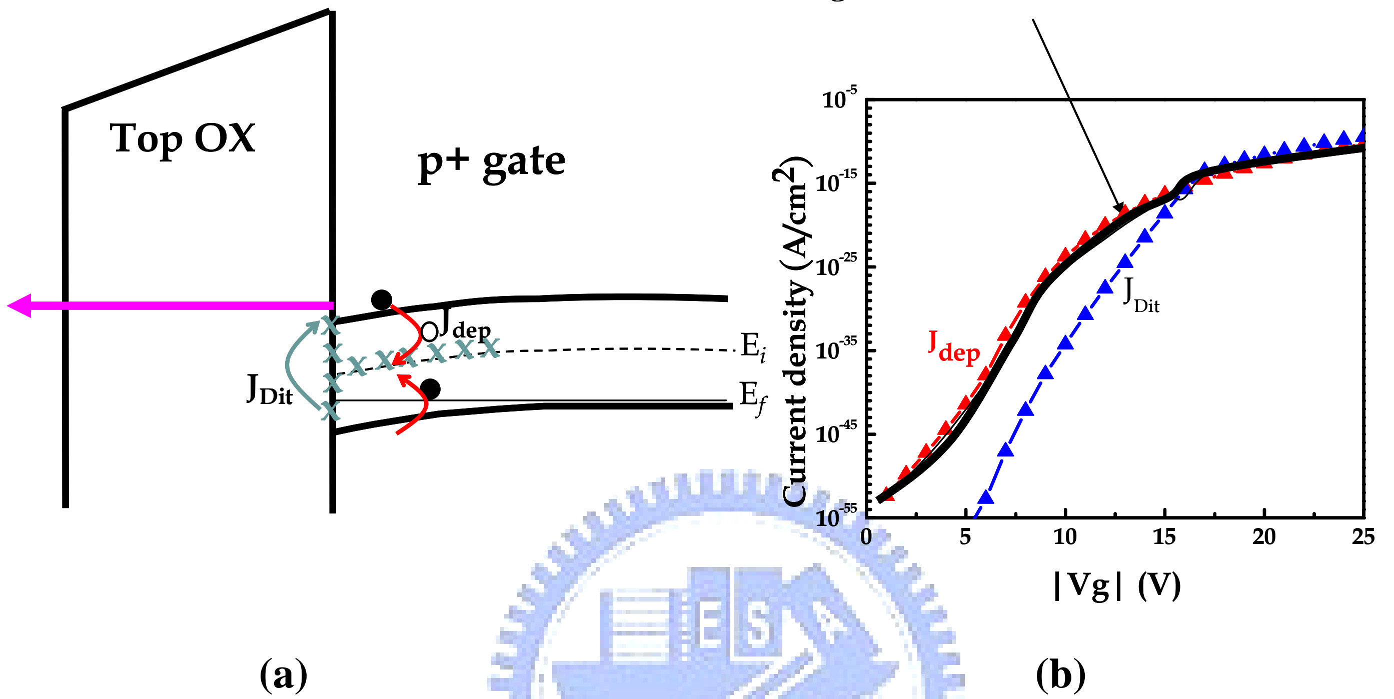



**Fig.2.4 (a)Schematic energy band diagram and Shockley-Read-Hall ($J_{SRH}$) tunneling current flows during erase (b) Back gate tunneling current density from Shockley-Read-Hall density**

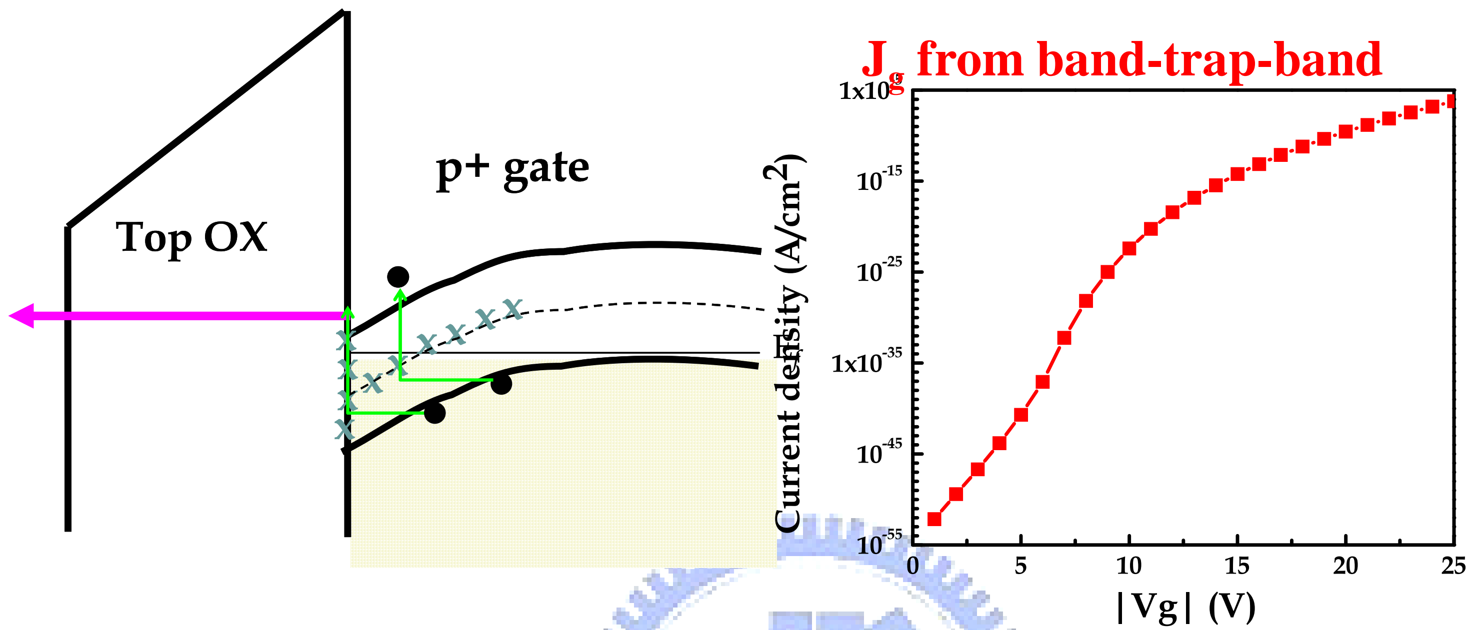
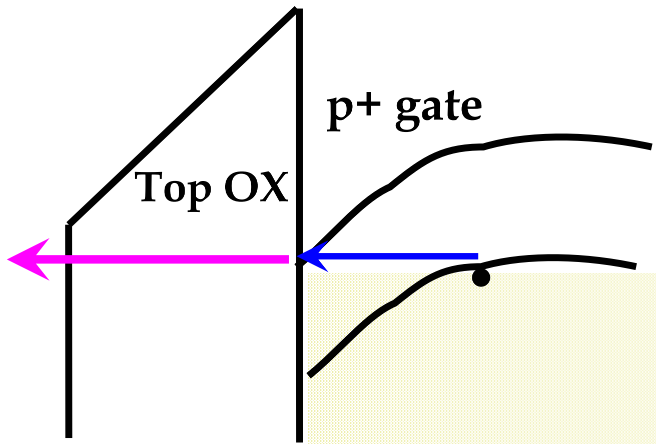
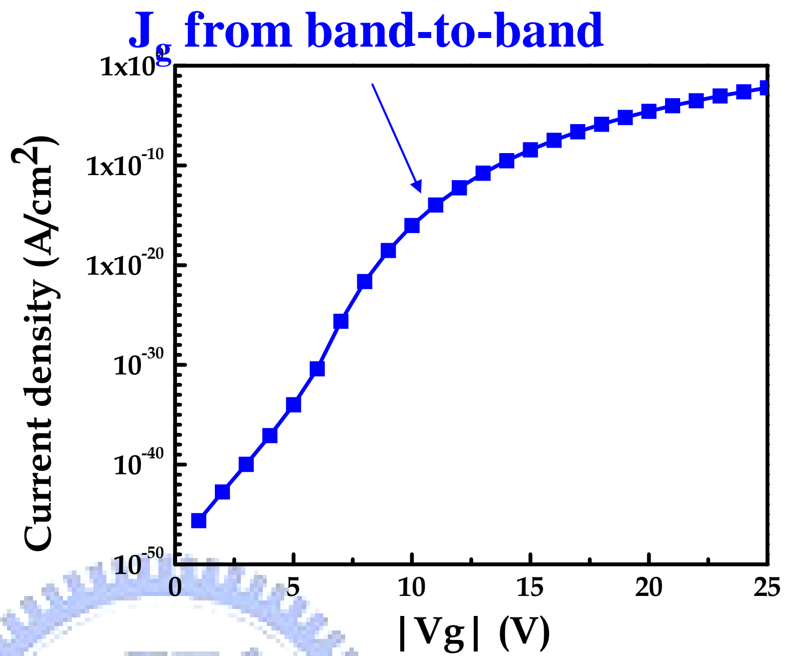



**Fig.2.5 (a)Schematic energy band diagram and band-to- trap- to band tunneling current ($J_{BTB}$) flows from path a and path b during erase**
**(b) Back gate tunneling current density from band-to- trap- to band**




(a) (b)

**Fig.2.6 (a)Schematic energy band diagram and band-to- band tunneling current ($J_{BBa}$) flows during erase**
**(b) Back gate tunneling current density from band-to- band**

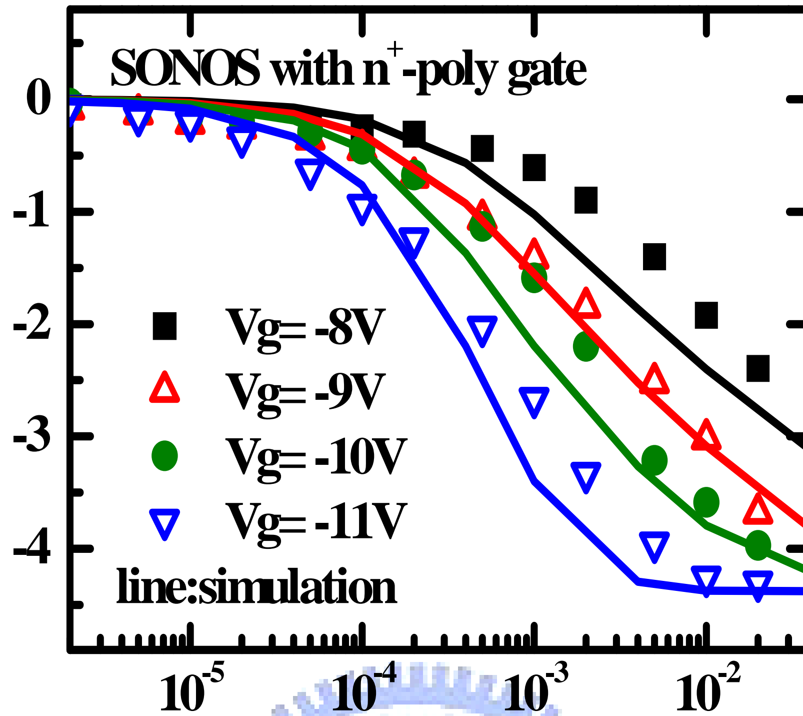



**Fig.2.7 Measured (symbol) and simulated (line) erase transient at various $V_g$ in a SONOS cell with n+ poly gate. ONO stack is 6nm/6nm/1.5nm.**

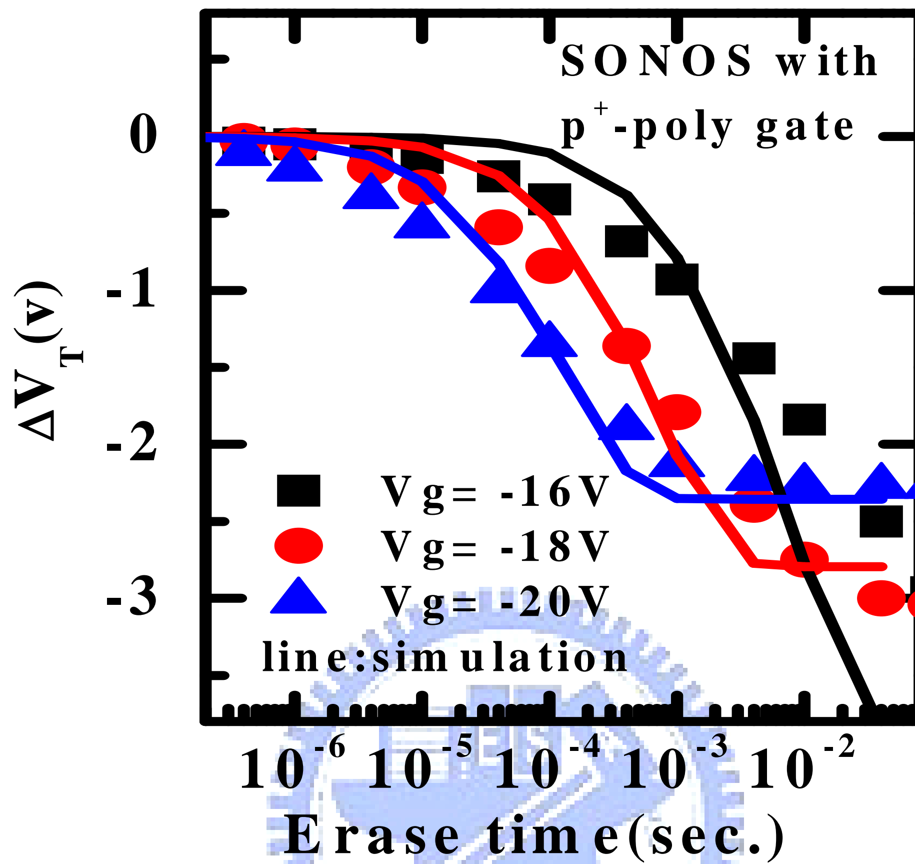



**Fig.2.8 Measured (symbol) and simulated (line) erase transient at various $V_g$ in a SONOS cell with p+ poly gate. ONO stack is 8nm/6nm/3nm**

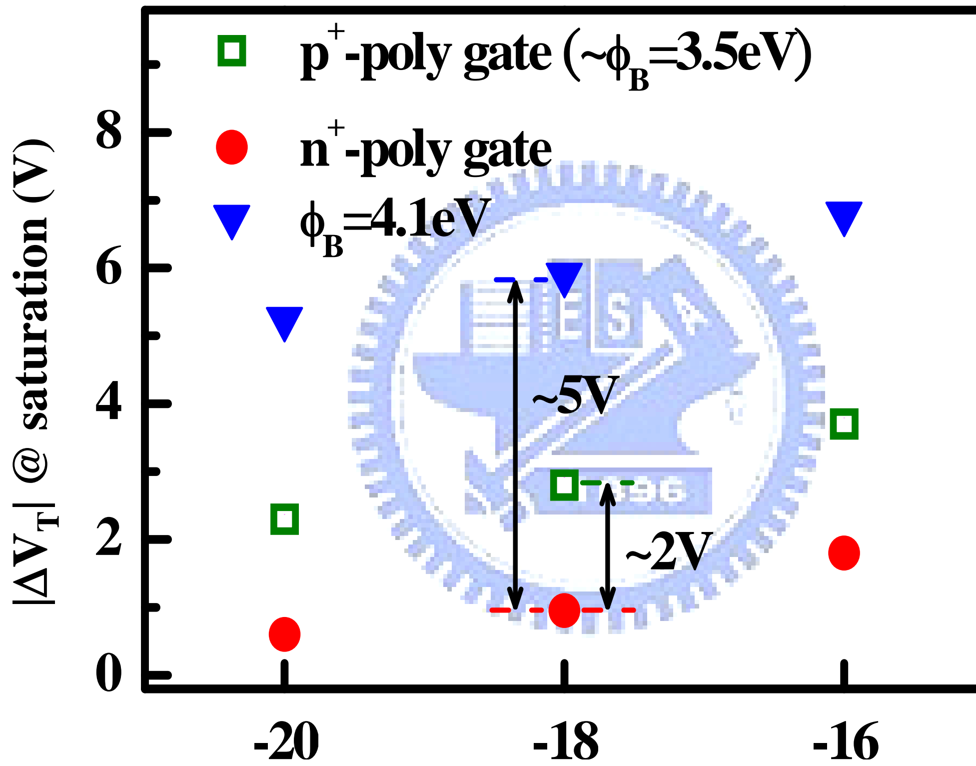



**Fig.2.9 Compare the erase capability under various gate biases and $\phi_B$. $\phi_B$ is the band offset between gate material and blocking oxide.**

# Chapter 3

# Overall Performance Consideration

## 3.1 Introduction

By incorporating our previous studies [8-9], performances including program, erase, and read disturb can now be reviewed for a SONOS based structure. The criterion of Vth shift window comes from program time 1ms; erase time 2ms and read disturb 10 years. It could be found that it is hard to fulfill the overall performance consideration for SONOS based cell unless with other material as blocking layer.

Otherwise, in this chapter, the performance for the TANOS based structure is also taken into analyzed. The model for TANOS would be confirmed first with experimental data and simulation and then the model is applied to get overall performance consideration as for SONOS based structure. With the method used above, the optimum bottom oxide thickness margin with the fixed EOT is achieved with the same criterion of performance, erase and read disturb time.

## 3.2 Process Margin of SONOS

With the assistance of our previous studies [8-9], performances including program, erase, and read disturb can now be clarify for a SONOS based structure. In cooperating with the model constructed above, the $V_{th}$ shift window could be gotten from its transient behavior with program time 1ms, read disturb 10 years and erase time 2ms. In Fig. 3.1, the $T_{ox}$ thickness, which meets both program speed and read disturb criteria, is ranged from 4.7nm to 5.1nm. However, it is shown in Fig.3.2 that erasing a cell to achieve $\Delta V_T$=4V within 2ms, $T_{ox}$ of 2.3nm or thinner is a must even with a $p^+$-poly gate. Therefore, the other way to enhance erase window with the

satisfied bottom oxide thickness is to increase the tunneling barrier of back tunneling electrons. In Fig. 3.3, erase capability versus the back tunneling band offset $\Phi_B$ is simulated under fixed EOT and $T_{ox}$=4.8nm which is within the program and read criteria margin. It is clear that to fulfill the erase requirement, $\Phi_B$ should be as high as 4.25eV.

To our best knowledge, suitable metal material is not found in semiconductor related publications. Therefore, it is hard to fulfill the overall performance simultaneously on the SONOS base structure.

## 3-3 Process Margin of TANOS

Using a high κ material as a top-blocking layer could assist to relieve the demand for a high work-function metal gate. From kinds of cells, a TANOS (TaN+$Al_2O_3$) cell is the most successfully case. In Fig.3.4, the data of reference [2] is quoted and our simulations fit both on its program and erase behaviors well. In simulation, a smaller electron tunneling probability at the top layer, which is due to a high κ dielectric always suffer a lower electric field on blocking layer, is probably the reason that the erase ability is enhanced and the enhanced program window. In Fig3.5 we could find that the program window with one step program bias increment is about 0.8, which is larger than its of SONOS cell. The improved program window could be verified from less tunneling-out current portion of tunneling-in current. Moreover, in Fig. 3.6(a), the read retention time is also emulated and compared with reference [2]. Discrepancy between the experimental data and simulation is observed when the read bias is lower than 5V. In Fig. 3.6(b), the simulated time evolution at $V_{read}$=5V is plotted. This $\Delta V_T$ transient shows two distinct slopes, which means the tunneling mechanism of read disturb varies from direct tunneling (a trapezoid oxide barrier only) to modified FN

tunneling (a trapezoid oxide barrier with a triangular nitride barrier) with time. As shown in Fig. 3.6(b), the existence of such phenomenon may lead to a large error when an extrapolated method is used to get read disturb $\Delta V_T$ shift from experimental data in which probably only direct tunneling behavior occurs. Therefore, cares should be taken during extrapolation method used from experimental data.

With the same method used above, the overall performance consideration for the process margin for TANOS could also be established. Fig. 3.7 shows the bottom oxide thickness effect on program, erase, and read disturb for a TANOS cell under EOT= 11.7nm. The EOT is determined by our well emulated referenced [5] in which $Al_2O_3/Si_3N_4/SiO_2$ is 10/6/3.5 nm. With the assist of the overall performance consideration for program, erase and read disturb simultaneously, 5.75/6.0/5.6nm is suggested for an $Al_2O_3/Si_3N_4/SiO_2$ stack. Unfortunately, an $Al_2O_3$ film of 5.75nm may raise another issue such as anomalous leakage [13].

## 3-4 Conclusion for Overall Performance of Planar Cell

An erase model is developed and verified. For a p+-poly gate, the gate injection procedure includes band-to-band tunneling in a poly Si followed by electrons tunneling through a top-blocking layer and the effective barrier increment is merely 0.4eV. Hence, it is hard to find an optimal thickness combinations of ONO stack to satisfy program, read disturb, and erase performances at a same time. Using a TANOS cell can help to relieve the demand for a high work-function metal. A 5.75/6.0/5.6nm is suggested for an Al2O3/Si3N4/SiO2 stack under EOT=11.7nm. However, a very high quality Al2O3 is required at this case. By the way, cares should be taken when a read disturb is extrapolated at a TANOS cell.

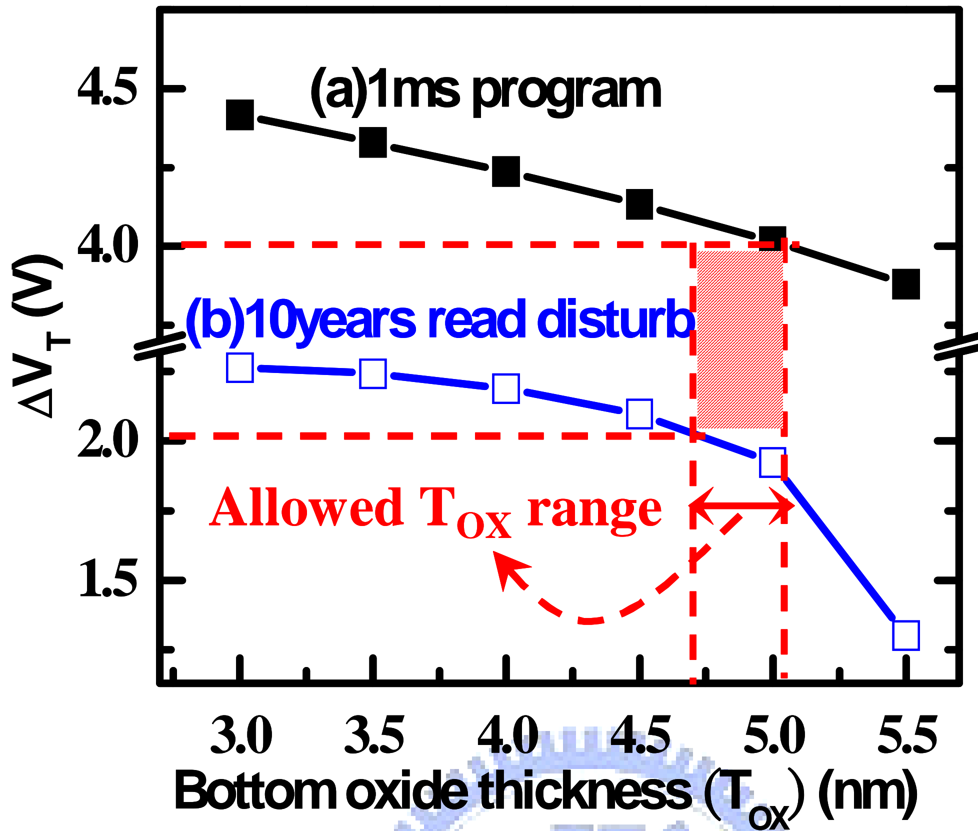



**Fig.3.1 simulated $\Delta V_T$**

**(a) at program time=1ms and**

**(b) at disturb time=10 years for different $T_{OX}$ but under the same EOT. Here, Program voltage=17V and Read disturb voltage=5.7V**

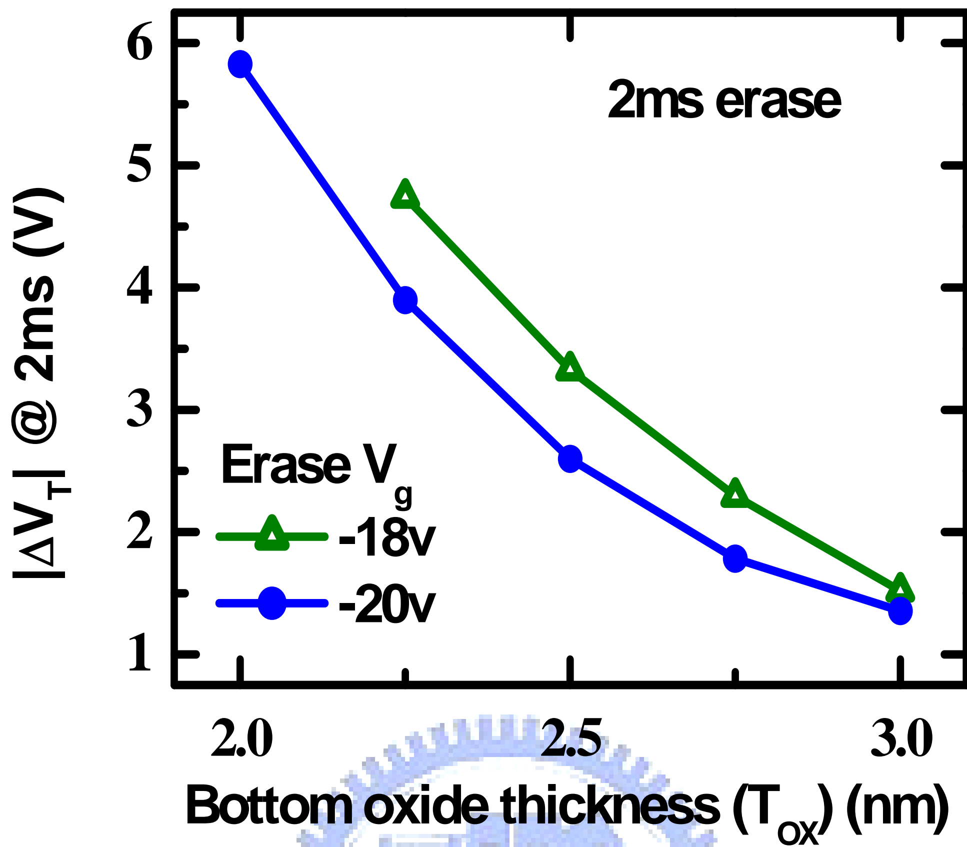



**Fig.3.2 simulated erase window $\Delta V_T$ under the same EOT for Erase voltage -18V and -20V.**

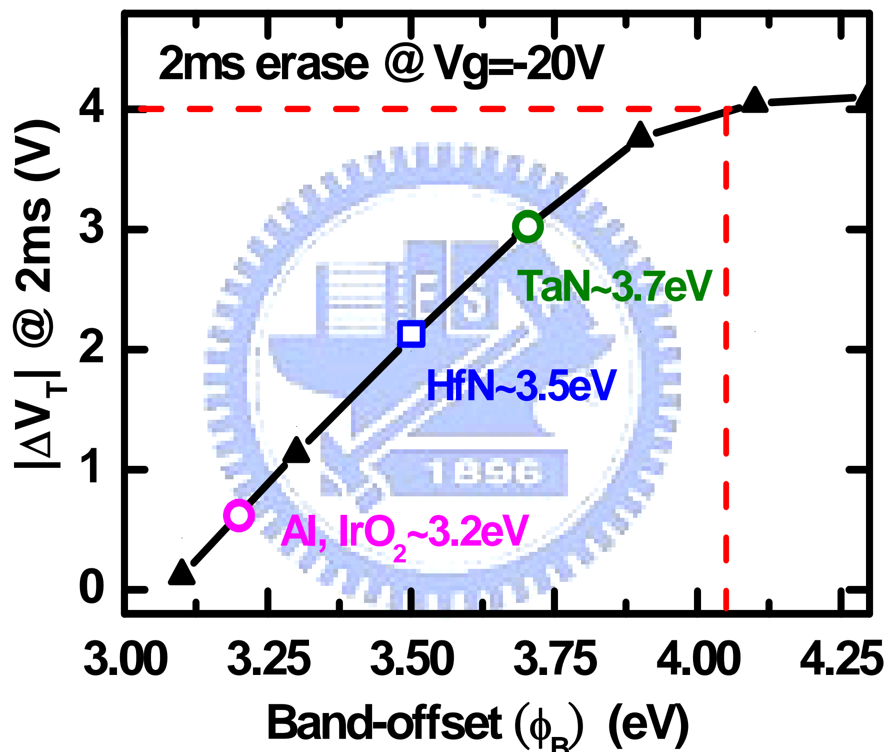



**Fig.3.3 Simulated $\Delta V_T$ at erase time =2ms under erase voltage=-20V for various $\phi_B$.**
**ONO stack now is 6.2nm/6nm/4.8nm to satisfy the program and disturb criteria. Several metal materials are also labeled.**

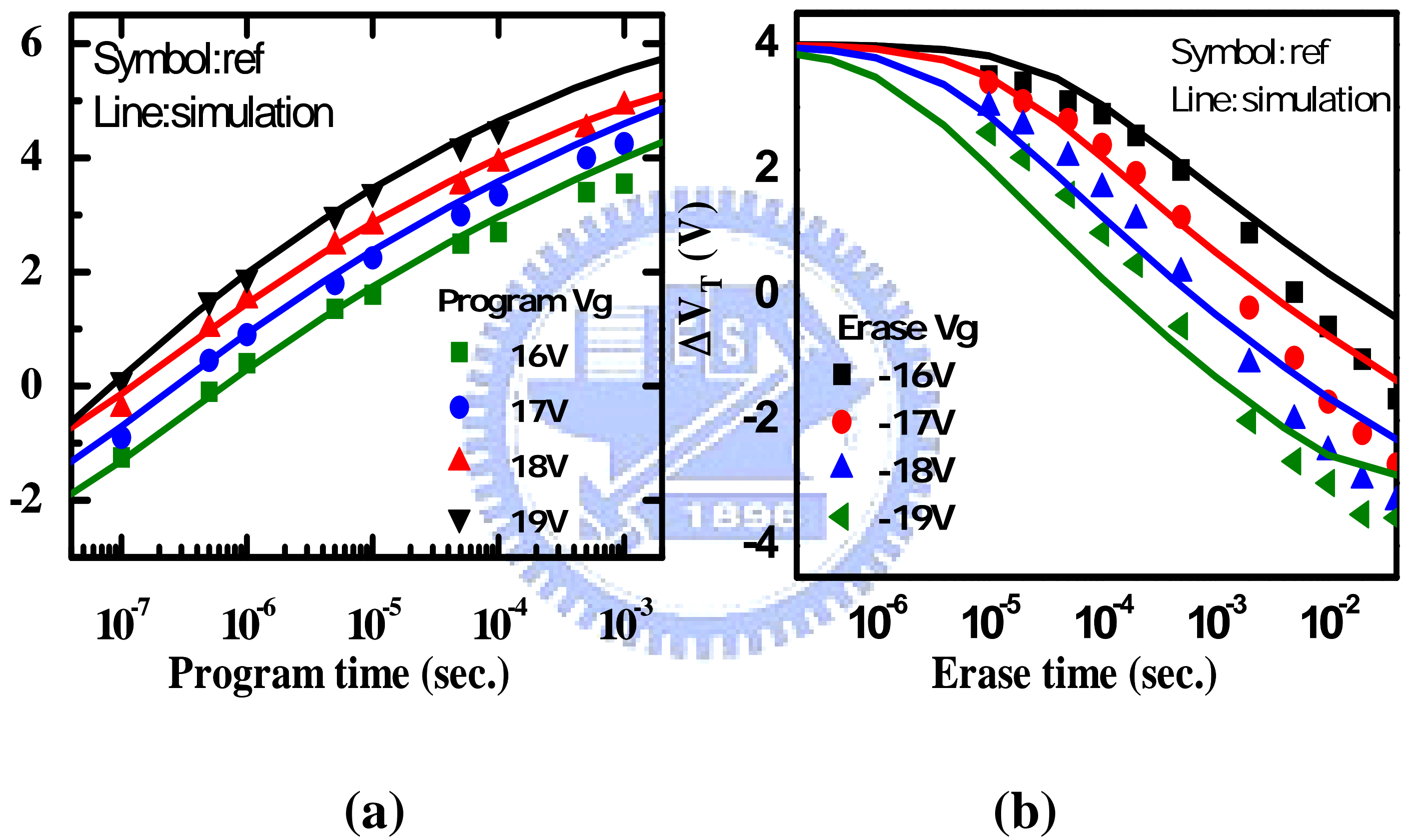



**Fig.3.4 (a) Program and (b) erase characteristics for a TANOS cell. Symbols are reported by [5] and lines are our simulation results.**

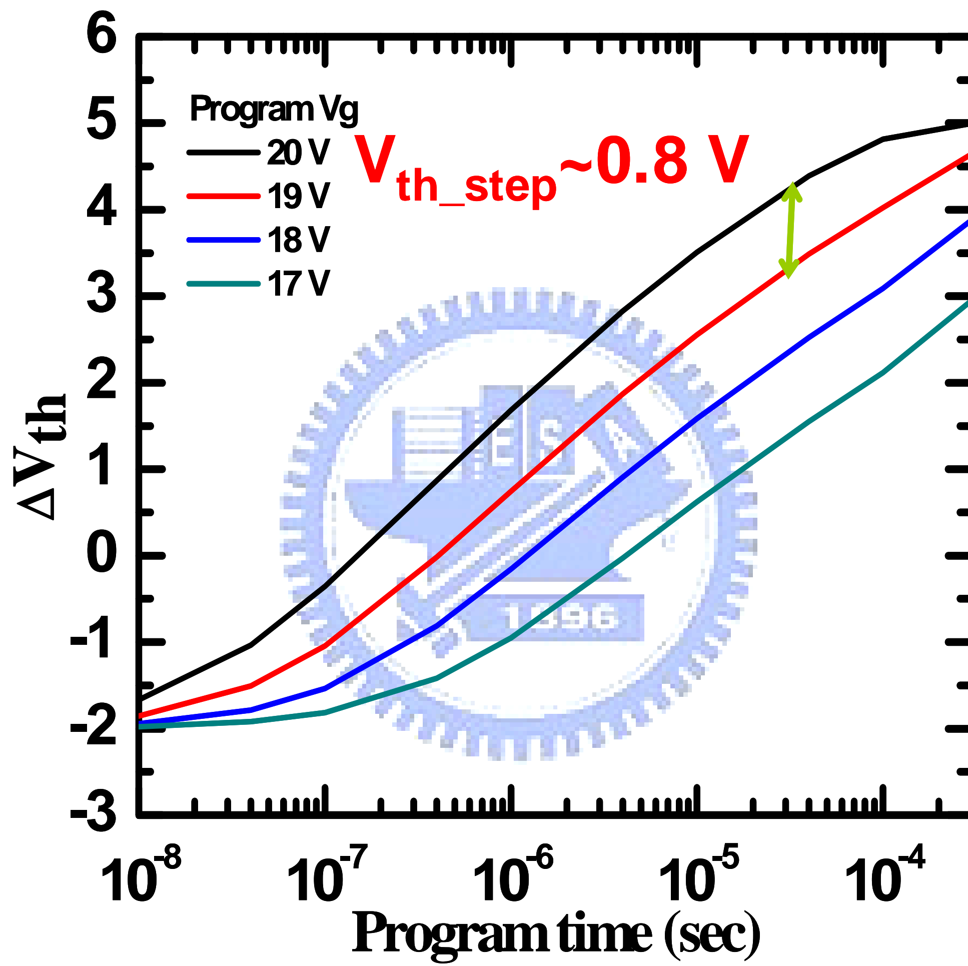
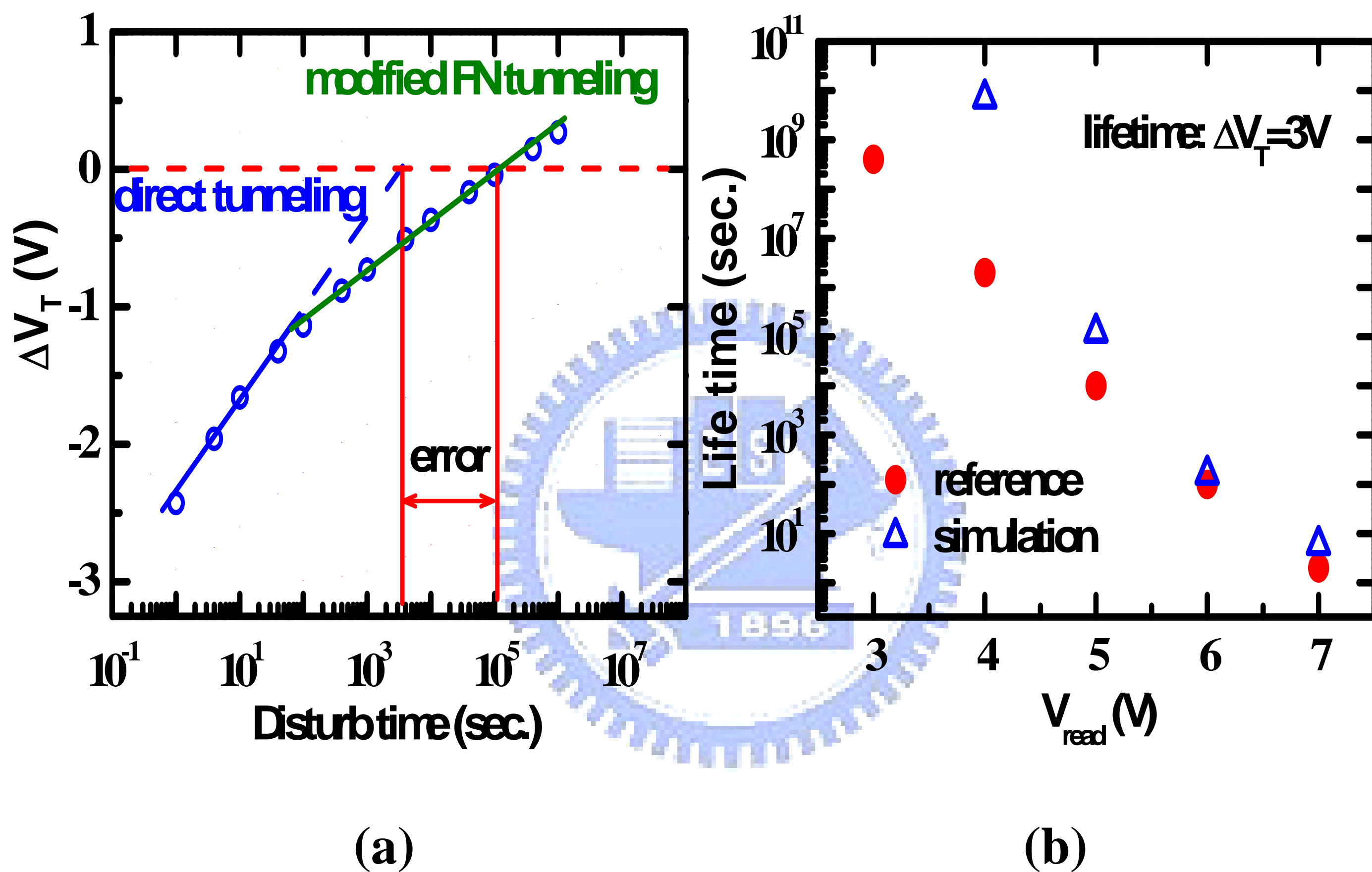



**Fig.3.5 enhanced program window of TANOS .**




**(a)** **(b)**

**Fig.3.6 (a) Read retention of a TANOS cell. Solid symbols are quoted from [5] and open symbols are simulated results based on our previous work[7].(b)discrepency of read disturb lifetime**

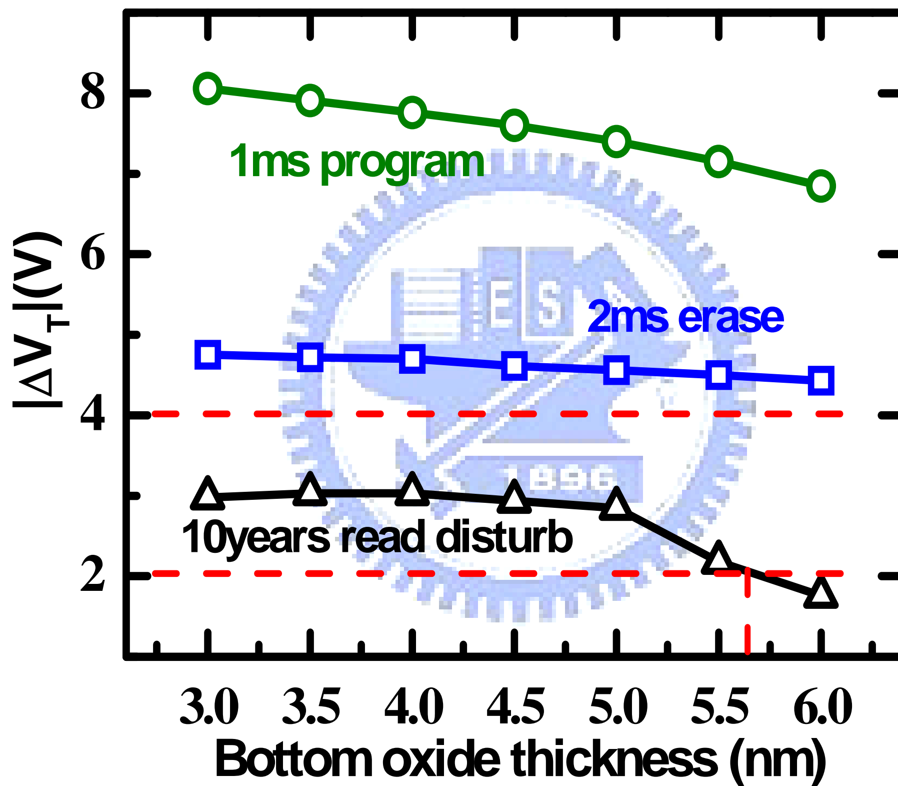



**Fig.3.7 Optimal bottom oxide thickness range extraction for a TANOS cell with EOT=11.7nm. Program $V_g$= 17V. Erase $V_g$= -18V. Read $V_g$=4.25V.**

# Chapter 4
# Cylindrical Cell

## 4.1 Introduction

The scaling limitation with the overall performance fulfill of the conventional planar cell is coming to face no matter what base of planar is used. The multi-gate devices feature a narrow channel body; therefore, the impact of discrete trapped charge on the channel conduction is large [14]. Therefore the combining nitride trap layer with tri-gate Fin-FETs, SONOS devices demonstrated good memory performance [15]. In the race of multigate devices, the cylindrical nanowire SONOS is being considered as a potential candidate to advance, due to its better memory window and reliability. Owing to its cylindrical geometry and the inverse logarithmic dependence of the insulator capacitance on the oxide thickness, the gate length in these devices can be scaled with channel diameter without reducing the gate dielectric thickness. Therefore, cylindrical NW devices represent the most perspective architecture for SONOS-type NVM applications, where the tunneling layer can hardly be scaled due to the severe retention properties (10 years) that are to be met. Recently, Suk *et al.* [16] presented a cylindrical lateral-twin-Si-NW SONOS memory with excellent performance. In this chapter, the erase transient behavior of cylindrical is also established and compared with planar cell.

## 4.2 Transient Behavior Model for Cylindrical Cell

Fig. 4.1 shows a structure of 3D cylindrical SONOS cell. We assume the radius (R) of the central silicon nanowire is 15nm and the thicknesses of the O/N/O stack (d) are 8nm (top oxide), 6nm (nitride) and 3nm (bottom oxide) (8/6/3nm), respectively.

Unlike a planar cell structure, the amplitudes of electric field for a cylindrical

cell across the bottom and top oxide layers are different. From Gauss' law, it is known that with the fixed magnitude of electric flux, the larger the area of surface flux passes through, the smaller the electric field across the surface is. Therefore, under the same electric field across tunneling layer for both planar cell and cylindrical cell, the electric field across the blocking layer for the cylindrical cell, whose blocking surface area is larger than the tunneling one, is much smaller. The band diagram comparison between the planar cell and cylindrical cell both for program and erase operation is showing in (Fig 4.2). We could found the cylindrical cell has predominance both on the program and erase operations. For program operation, the charge loss though top layer is smaller. Otherwise, assuming the program bias is 20V, Cylindrica cell needs only 13.5 V for the same tunneling layer electric field as the planar cell's. Fig 4.3 demonstrates the program characteristics for different cells.

For erase operation, the EBT from the gate is smaller which leads to large erase window. Fig 4.4 is the EBT probability comparison for the planar and cylindrical cell. From the above chapters, we could realize that the EBT current is a key factor to constrain the erase window. With the smaller electric field of blocking layer, the EBT current for the Cylindrical cell is markedly reducer without degrading erase current. From Fig 4.5, the EBT probabilities of planar SONOS, planar TANOS and cylindrical cell under the different bottom electric field are all taken into comparison. The comparison could also response the benefit of TANOS from SONOS cell which we discuss before. It is clear that, from the geometric benefit from cylindrical cell, the EBT current could be markedly reduced than without involving new material. In conclusion, the erase window eventually could be dramatically improved for cylindrical cell.

At a given gate bias, the electric field at any distance (r) from origin point O can be stated as (Fig.4.6)

$$E(r)=\frac{V_g}{r\cdot\ln\left(\frac{R+d}{R}\right)}$$

During erase process, the relation between the electric field across blocking-layer/nitride ($\Delta E_t$) and nitride/tunneling-layer ($\Delta E_b$) difference and the expunged stored charges ($\Delta Q_N$) can be devised as

$$\Delta E_t=\frac{\Delta Q_N}{\varepsilon_0}\cdot\left(\frac{R+d-x_c}{R+d}\right)\cdot\frac{\ln\left(\frac{R+d-x_c}{R}\right)}{\ln\left(\frac{R+d-x_c}{R}\right)+\ln\left(\frac{R+d-x_c}{R+d}\right)}$$

And

$$\Delta E_b=\frac{\Delta Q_N}{\varepsilon_0}\cdot\left(\frac{R+d-x_c}{R}\right)\cdot\frac{\ln\left(\frac{R+d-x_c}{R+d}\right)}{\ln\left(\frac{R+d-x_c}{R}\right)+\ln\left(\frac{R+d-x_c}{R+d}\right)}$$

where $x_c$ is the stored charges centroid position in a nitride layer.

Besides, the erase window

$$\Delta V_T=\frac{Q_N}{\varepsilon_0}\cdot\left(R+d+x_c\right)\cdot\ln\left(\frac{R+d}{R}\right)\cdot\frac{\ln\left(\frac{R+d-x_c}{R+d}\right)}{\ln\left(\frac{R+d-x_c}{R+d}\right)+\ln\left(\frac{R+d-x_c}{R}\right)}$$

where $Q_N$ is the total erased charges.

## 4-3 Enhanced window of cylindrical cell

Fig. 4.7 illustrates the program and erase characteristics of various structures. The data of a TANOS cell from [5] and a SONOS from the experiment are all demonstrated for contrast. As expected, in a 3D cylindrical structure, a lower gate bias is required to acquire the compatible erase speed in a planar SONOS and TANOS cells. Moreover, no erase saturation phenomenon is observed in a 3D gate-around structure due to its negligible EBT probability. Moreover, with the assistance of simulation, we could predict that the program window of cylindrical cell could be more improved than TANOS to 0.85V (Fig4.8). The window $\Delta V_T$ at 1ms under the same gate bias versus width (2R) is exhibited in Fig. 4.9. With the benefit of radius effect, we could enhance the window without any process changed.

In summary, by the numerical simulation, the 3D cylindrical structure demonstrates better erase efficiency without erase saturation even under a lower gate bias condition. Beside, enlarging erase window can be easily achieved in a 3D gate-around structure with scaling down radius.

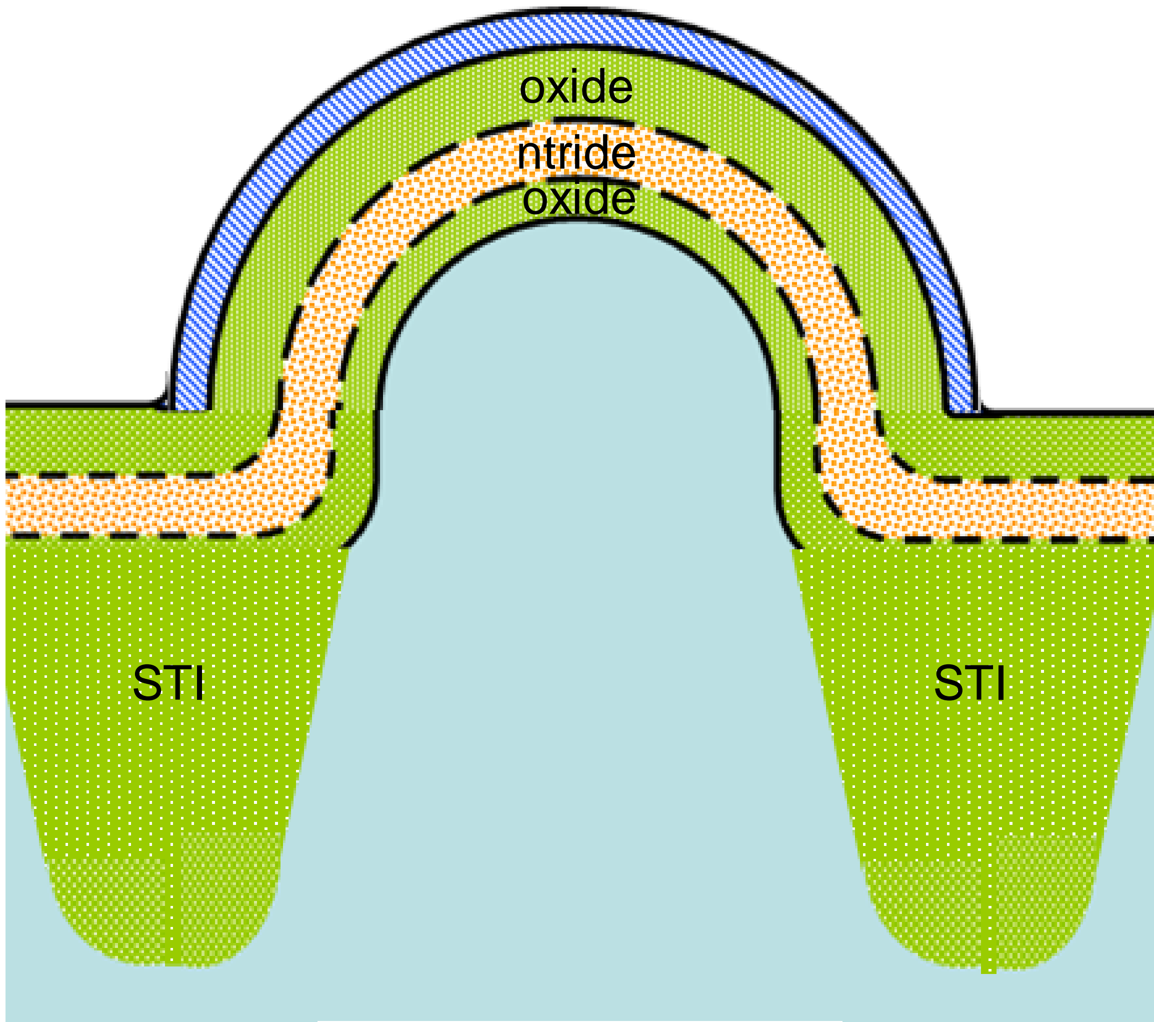
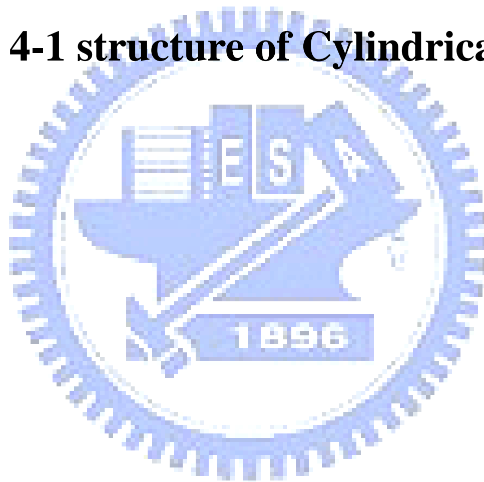



**Fig 4-1 structure of Cylindrical Cell**



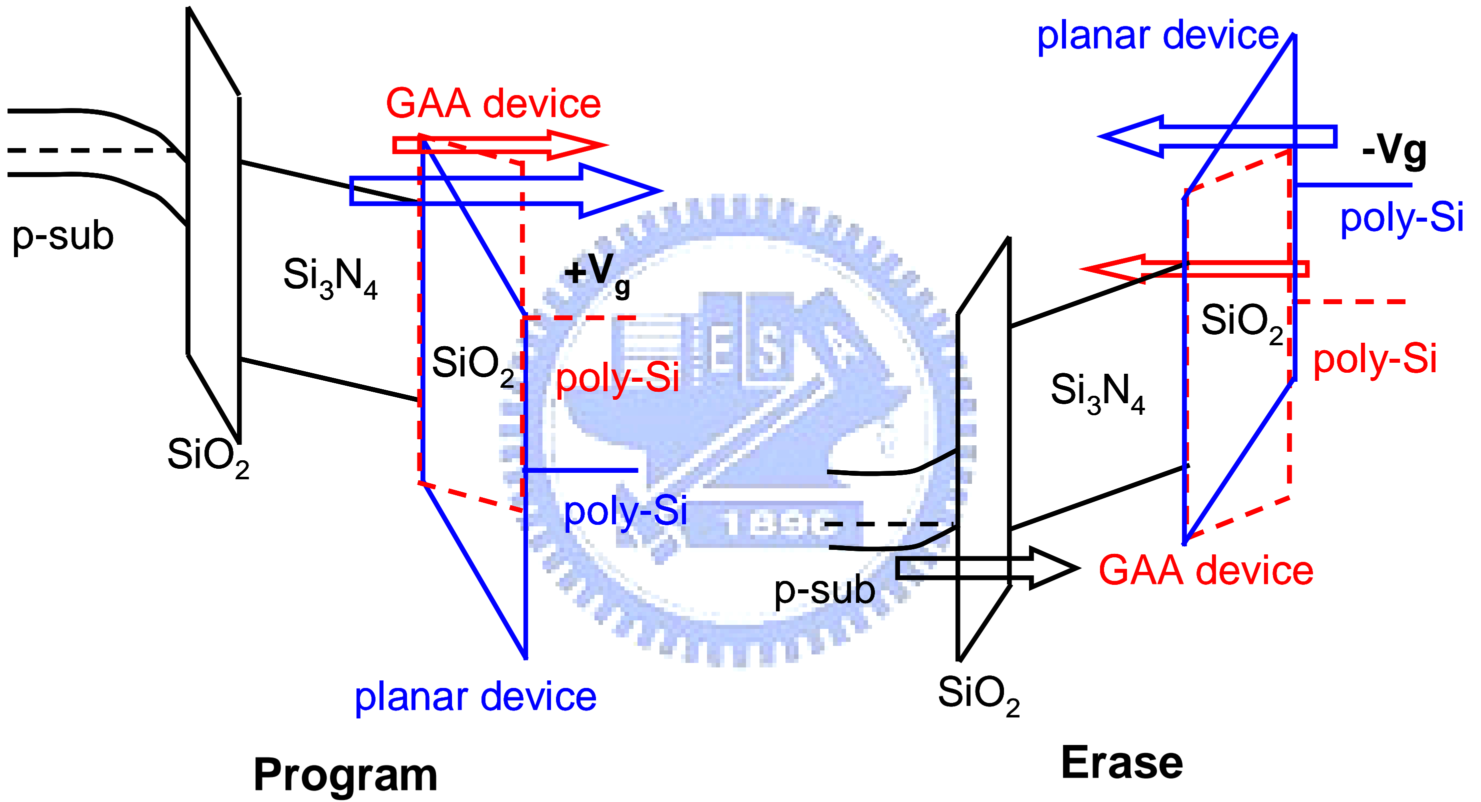



**Fig 4-2 band diagram shame comparison between Planar and Cylindrical Cell**

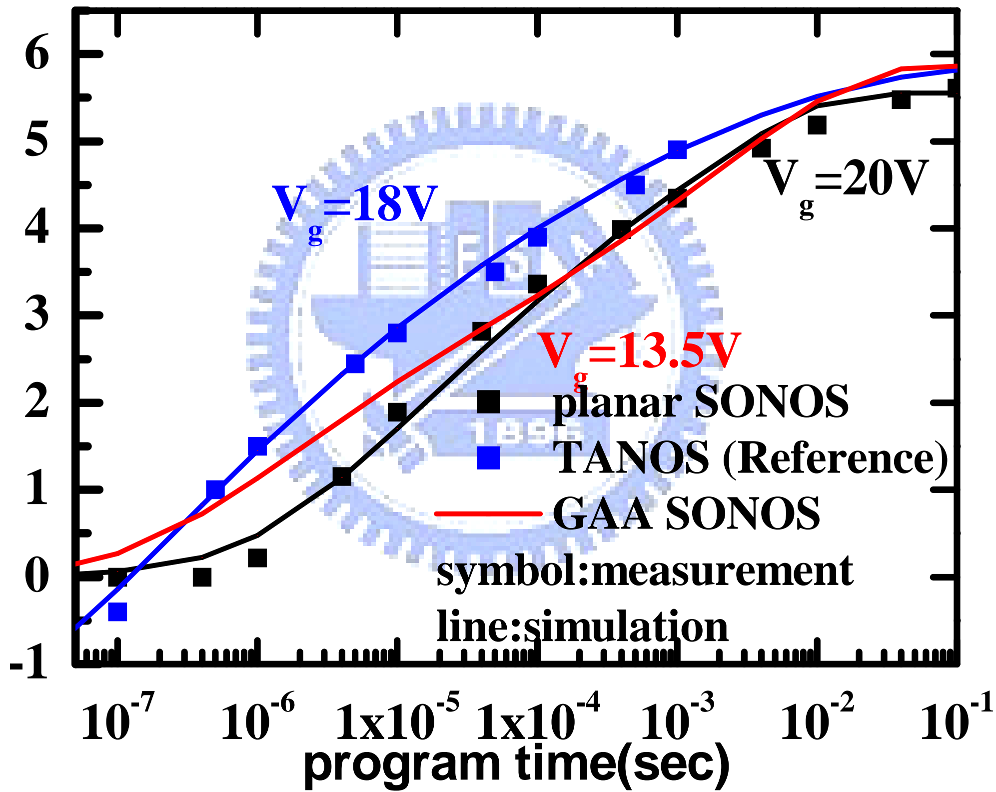



**Fig 4-3 program behavior comparison between Planar SONOS, TANOS and Cylindrical Cell**

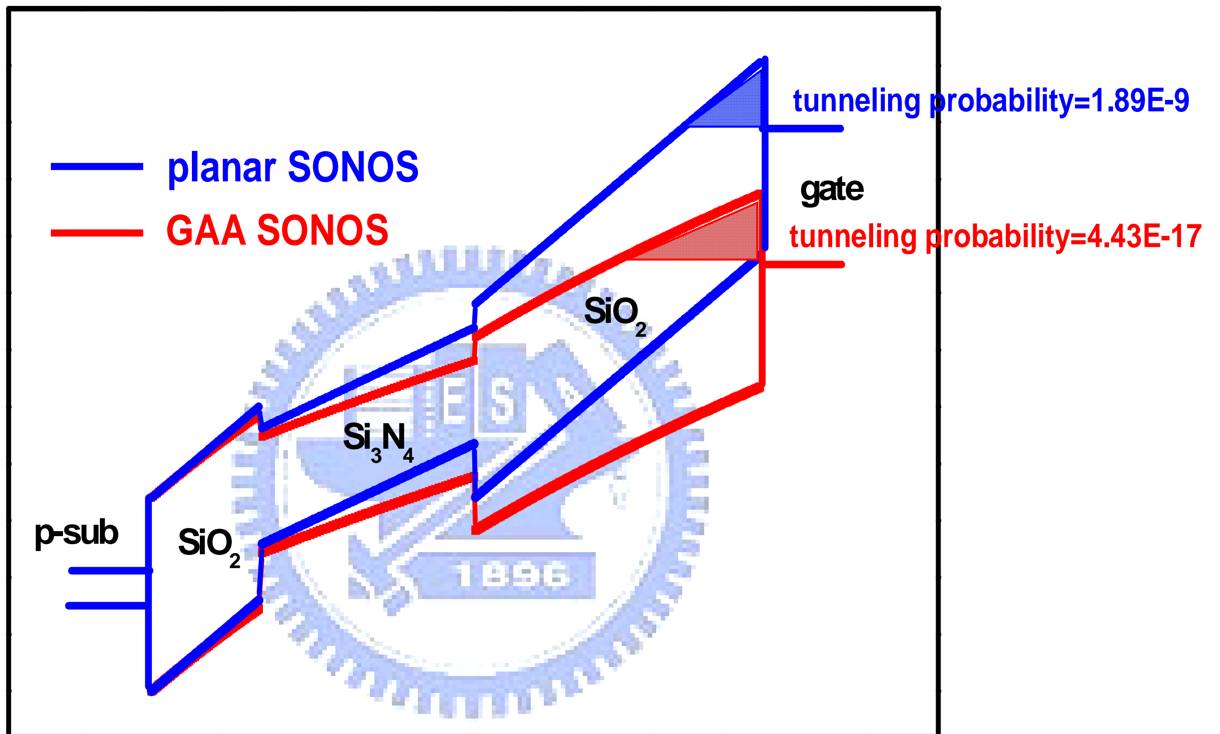



**Fig 4-4 The band diagram at erase comparison under the same bottom layer electric field between Planar and Cylindrical SONOS Cell**

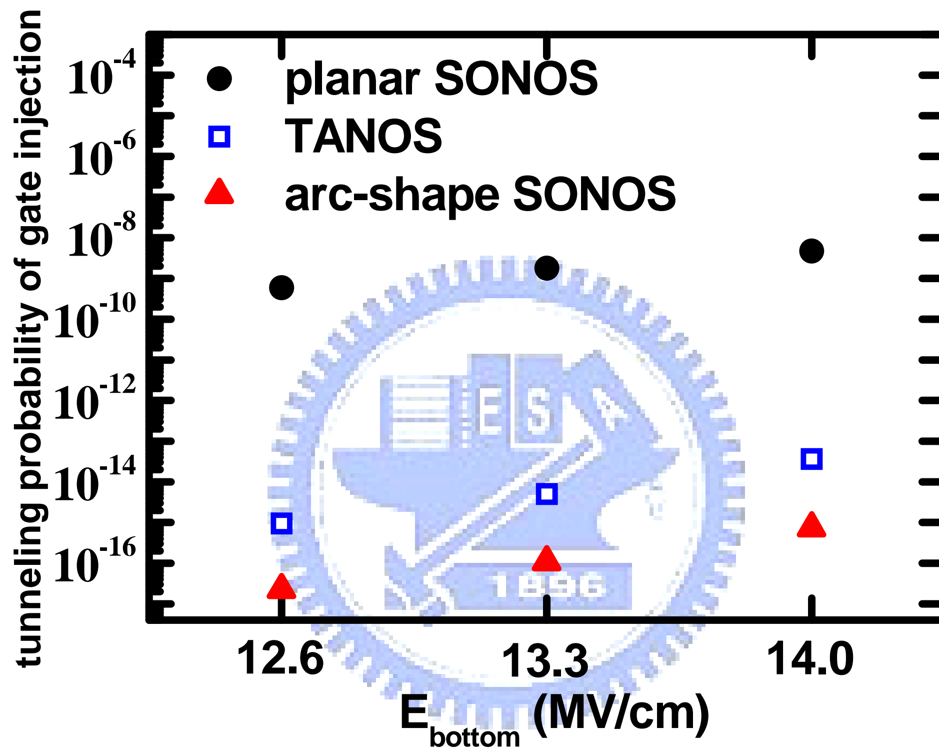



**Fig 4-5 The EBT probability comparison under the same bottom layer electric field between Planar SONOS, TANOS and Cylindrical SONOS Cell**

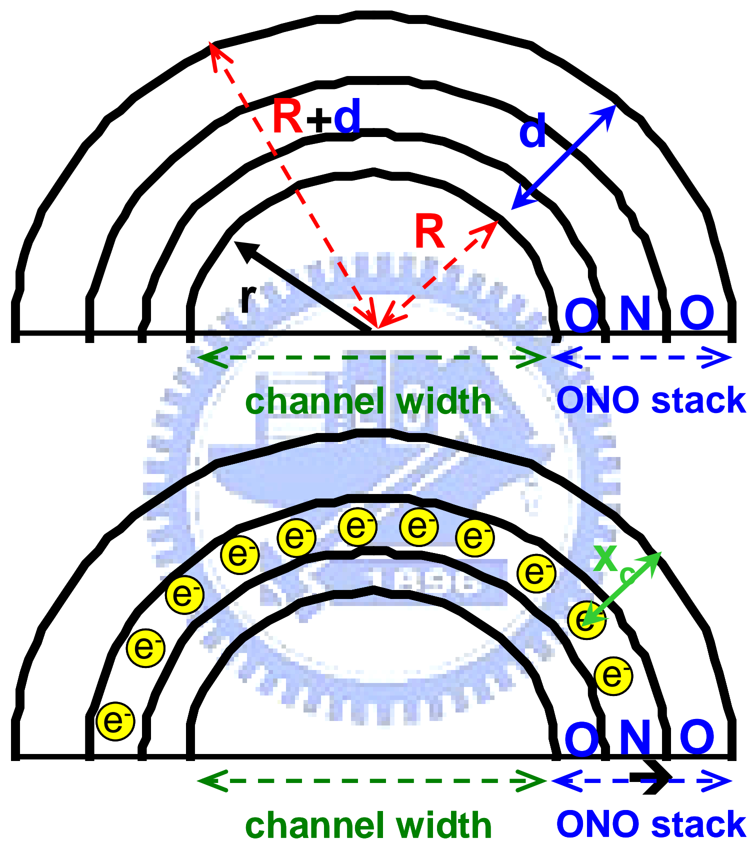



**Fig 4-6 parameters for electric field formula of**

**Cylindrical cell**

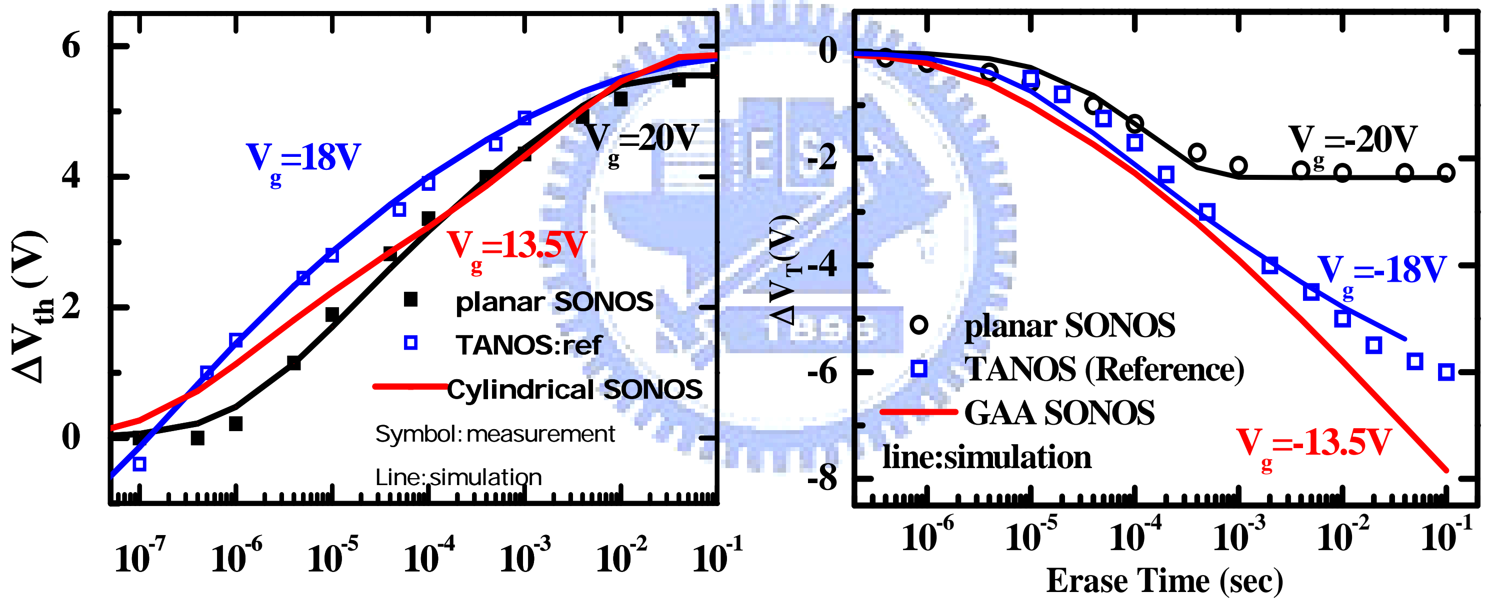



**Fig 4-7 Erase (a) and Program (b) behavior comparison between Planar SONOS, TANOS and Cylindrical SONOS cell**

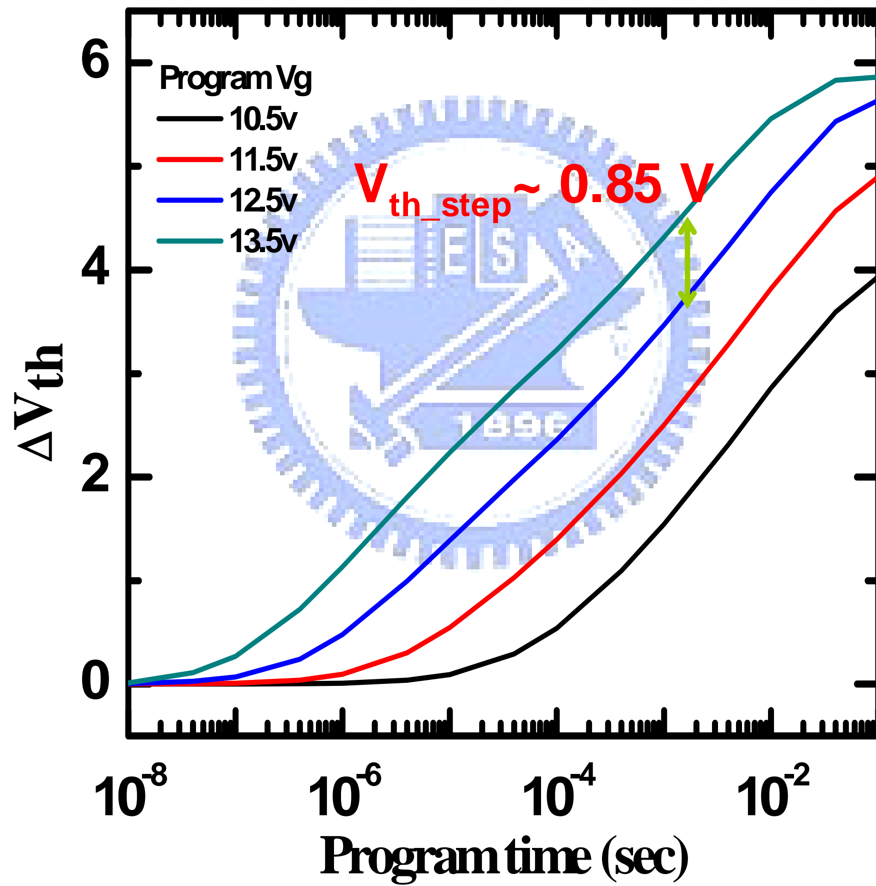



**Fig 4-8 Enhanced program window of cylindrical cell**

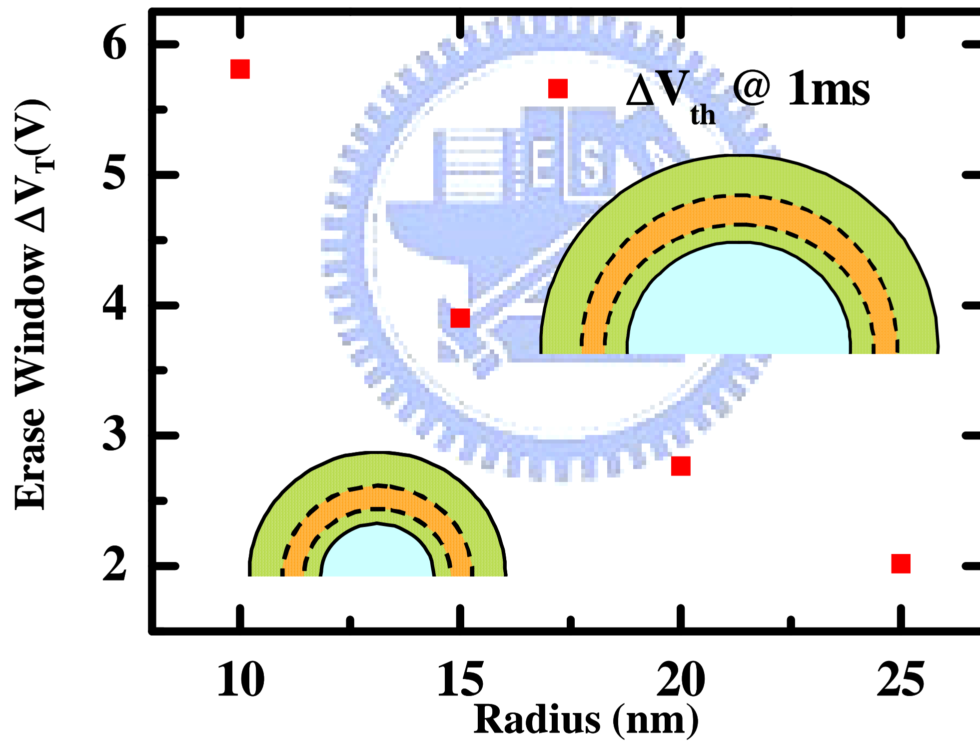



**Fig 4-9 Enhanced windows under the same Erase voltage for different radius**

# Chapter 5
# Conclusion

A program and erase model are developed and verified by measurement or reference data. For a $p^+$-poly gate, the gate injection procedure includes band-to-band tunneling in a poly Si followed by electrons tunneling through a top-blocking layer and the effective barrier increment is merely 0.4eV. Hence, it is hard to find an optimal thickness combinations of ONO stack to satisfy program, read disturb, and erase performances at a same time. Using a TANOS cell can help to relieve the demand for a high work-function metal. A 5.75/6.0/5.6nm is suggested for an $Al_2O_3/Si_3N_4/SiO_2$ stack under EOT=11.7nm. However, a very high quality $Al_2O_3$ is required at this case. By the way, cares should be taken when a read disturb is extrapolated at a TANOS cell.

Otherwise, since there is some limit to fulfill all the operation considerations for planar cell except new material replaced, 3D structure cell is developed as a potential candidate. In a 3D gate-all-around structure, the EBT probability can be significantly reduced due to a lower electric field across top oxide. By the numerical simulation, the 3D gate-all-around structure demonstrates better erase efficiency without erase saturation even under a lower gate bias condition. Beside, is possesses more effective program which comes from less electron loss from the blocking layer. Eventually,

enlarging erase window can be easily achieved in a 3D gate-around structure with scaling down radius.

Reference:
[1]. C. H. Lee et al., *IEDM*, pp.613-616, 2003.
[2]. C. H. Lee et al., *VLSI*, pp.21-22, 2006.
[3]. Y. Q. Wang et al., *TED*, pp.2699-2705, 2007.
[4]. Y. Q. Wang et al., *IEDM*, pp.162-165, 2005.
[5]. H. Reisinger et al., *VLSI*, pp.113-114, 1997.
[6]. C. W. Kuo et al., *MTDT*, pp.77-79, 2006.
[7]. C. Friederich et al., *IEDM*, pp.963-9663, 2006
[8]. C. H. Lee et al., *NVSMW*, pp.109-110, 2008.
[9]. C. H. Lee et al., *SSDM*, pp.826-827, 2008
[10]. J. Fu et al., EDL, Vol.29, No.5,2008
[11]. Dake Wu et al., Semiconductor Science and Technology, 2008
[12].H. Bachhofer et al., *JAP*, pp.2791-2800.
[13] C. H. Lin et al., *IEEE TED*, pp.2125-2130, 2001
[14] M. Saitoh et al., *IEDM Tech. Dig.*, 2002, pp. 181–184.
[15] P. Xuan et al.,*IEDM,* 2003, pp. 609–612.
[16] S. D. Suk et al., *VLSI Symp. Tech. Dig.*, 2007, pp. 142–143.