國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

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The Role of Oxygen Vacancies and Phase Change in $TiN/SiO_2/PtFe$ Resistance nonvolatile Random Access Memories

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摘要

近年來，由於非揮發性記憶體的應用與發展受到矚目，加上快閃記憶體微縮極限，所以新世代非揮發性記憶體的研究正緊鑼密鼓地展開。其中，電阻式非揮發性記憶元件具有高密度、高操作速度、低功率消耗、高耐久性、微縮能力高及非破壞性資料讀取等優點，使其成為新世代非揮發性記憶元件的熱門人選。

在本篇論文中，提出電阻轉換特性的物理模型與理論基礎在氮化鈦/二氧化矽/鐵白金的結構上，且與氧空缺和相變化有關。其內容可分為三大部份，包含利用結構上的不同，亦或不同熱處理的方式與小尺寸元件效應，來驗證論文中所提到的物理模型與電性特性的研究。在利用不同結構來檢視記憶體特性部份，置換不同上下電極材料與二氧化矽厚度，來檢視電阻有效轉態區的位置。其結果驗證有效轉態區位置在鐵白金底電極與二氧化矽的界面上，且和 Fe 元素有一定的相關性。在利用不同的熱處理方式來檢視電阻轉態特性部分，驗證了氧化鐵與氧空缺量的多寡程度亦會影響到轉態週期與電流特性。最後，製作小尺寸元件來檢視轉態特性，發現實驗結果與電性水管理論的結果相似，並且可從電性結果更加驗證物理模型的確立。最後提出電性水管的基本物理與數學模型，做為未來可能再增進的研究方向。

The Role of Oxygen Vacancies and Phase Change in TiN/SiO_2/PtFe Resistance nonvolatile Random Access Memories

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Abstract

Recently, since nonvolatile memories acquire a lot of attention and flash memories are facing with the scale limit issue, the next generation nonvolatile memory has been carried out to discover extensively. The resistive random access memories (ReRAMs) that have the strengths of high cell density array, high operation speed, low power consumption, high endurance, lower scale limit and non-destructive readout, are one of the most potential candidate for flash memories.

In this thesis, a physical model and mechanism which is about the role of oxygen vacancies and phase change in TiN/SiO_2/PtFe resistance nonvolatile random access memories is proposed. This study can be categorized into three parts, different structures, different thermal treatments and small size devices, all of these electrical results can support the model and mechanism. In the first part, replacing metal electrode materials and SiO_2 thickness with different structures was found the results which the effective resistance switching region is at interface region, and Fe element

plays an important role to cause resistance switching behavior. In the second part, with different thermal treatments to examine the resistance switching characteristics, was discovered that amount of Fe_2O_3 and oxygen vacancies would affect endurance reliability and electric characteristics. In the third part, using small size cells to examine the resistance switching characteristics was found the results which are similar with the electric faucet theory and the proposed model. Moreover, a possible model about electric faucet is proposed by physical and mathematical methods. Further investigation, including interfacial electric faucet structure and electrode effects, would help to achieve a better understanding.

誌謝

給所有曾經幫助過我的人，跟我最愛的人，此論文獻給你們。

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Chapter 1

Introduction

1.1 Introduction to non-volatile memory

Recently, the portable electronic products possess wide applications. These products are all based on flash memory which is considered as a technology drivers for semiconductor industry in the next generation. It can be classified into two major markets: code storage application and data storage application. NOR type flash memory [1] has been targeted at code storage application, such as PC bios and DVD player. NAND type flash memory [2] is the most suitable for code storage application, such as PDA, memory cards, MP3 audio players, digital cameras, and USB flash personal disc etc. These products are all based on flash memory that is nonvolatile and can keep stored information when the power supply is switched off. The first NVM is the floating-gate nonvolatile memory, invented by S. M. Sze and D. Kahng at Bell Labs in 1967 [3]. A perfect NVM should possess the properties including low operation voltage, simple structure, low power consumption, non-destructive readout, high operation speed, long retention time, high endurance, and small cell size [4, 5]. There have been many kinds of nonvolatile memories invented so far, such as flash memory, erasable programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), phase change memory (PCRAM), ferroelectric random access memory (FeRAM), magnetoresistive random access memory (MRAM), and resistance random access memory (RRAM). Today, flash memory is the mainstream among the NVMs.

The following will concentrate on the next generation nonvolatile memory, ReRAM. Flash memories are also introduced.

1.1.1 Flash

Flash memory, invented by Gerard Dixon, is a form of nonvolatile computer memory, which can be electrically erased and reprogrammed.

Flash memory stores information in an array of floating gate transistors, called "cells", each of cells stores one bit of information. The latest flash memory devices, often referred to as multi-level cell devices, could store more than 1 bit per cell, by using more than two levels of electrical charge which is placed on the floating gate of a cell. The writing times for common flash memory devices are in the order of 1 ms, and reading times are typical 10 ns.

When manufacturers increase the density of flash devices, each cells shrink and the number of electrons in any cells become few. Coupling effect between adjacent floating gates could change the cell characteristics. New designs, like charge trap flash, try to provide better isolation between adjacent cells.

Although the flash memory is the mainstream device of NVM, flash memory possesses the defects including high operation voltage, low operation speed, and low endurance. Moreover, following the device scaling, tunneling oxide would be shrunken, which would lead to a large leakage current due to tunneling current. Hence, because of device scaling, the retention time of flash memory would be reduced.

1.1.2 Resistive random access memory (ReRAM)

Resistive random access memory (ReRAM) is one of candidates for the next

generation nonvolatile memory devices. RRAMs use of the resistance changes as different memory states. By electrical field or current effects, the conductivity could be switched between high and low resistance reproducibly. The bistable resistance states represent different digital states as a memory device. The advantages of RRAM are the high cell density array, high operation speed, low power consumption, high endurance and lower scale limit. Moreover, RRAMs possess the features of nonvolatility, long retention time, and non-destructive readout. In next section, the properties of structure, fabrication, material classification, operation and circuit realization will be discussed.

1.1.3 Structure and fabrication

The basic structure for RRAM is made up of only metal-insulator-metal, M-I-M, which could be further integrated into 1D1R (a diode and a resistor) or 1T1R (a transistor and a resistor) structures (discussed later) [6, 7]. The top and bottom electrodes could be made by metals or conducting transition metal oxides [6], the choice of which would impact on the resistive switching properties because of their different crystallinities, work functions and the ability of oxygen gettering [8-10].

The main character of resistive switching is the insulator layer sandwiched among the electrodes. The insulator for the M-I-M structure may be not really insulating, but also semiconducting, depending on the composition and stoichiometry [11]. The insulator would be called “resistance switching layer” in the following sections. The different qualities deposited by different methods would possess connection with the resistive switching characteristics [12].

1.1.4 Material classification

The resistive switching phenomena have been discovered in many materials. The research mainstream concentrates on several groups, including binary oxides, perovskite oxides, manganites, and organic or polymers.

The binary oxides adopted in RRAM application, such as TiO_2 [13], ZrO_2 [14], NiO [15], Al_2O_3 [16], Cu_xO [17], Fe_2O_3 [18], ZnO [19], HfO_2 [10], SiO_2 [20, 21] and MoO_x [22], are candidates or have been widely used in other field of CMOS devices. Thus, the compatibility with modern CMOS process would not be a serious issue. Moreover, these binary oxides possess simpler element and it could be easier to control the proportion metal and oxygen composition.

1.1.5 Operation and circuit realization

Basic operation of bistable resistive switching in one cell could be achieved by DC sweep or pulse modes. Fig. 1-1 and Fig. 1-2 show a typical *I*-*V* plot under DC sweep operation, unipolar and bipolar mode [23]. First, assuming the resistance state is held in high resistance state, the current would suddenly increase when DC bias sweeps toward the same (or opposite) direction. Hence, the resistance would become low resistance state, which is defined as a process of "set". Then the opposite (or same) direction bias is applied to switch back to high resistance state with an enormously current drop at the switching voltage, which is defined as a process of "reset". It should be noted that this operation requiring different (or same) voltage polarities to switch, whether negative on/positive off or negative off/positive on (or positive on/positive off or negative off/negative on), is called bipolar operation (unipolar operation). For reading operation, the bias should not exceed the switching voltage (set or reset) to prevent memory state variation. Fig. 1-1 and Fig. 1-2 do not show the

forming process which is required to initiate the resistive switching properties of oxide films. The forming process is similar to soft breakdown, leading to the conducting paths (filaments) composed of clusters of point defects. In order to unify the operation parameters in the following text, the "set" and "reset" would be used to describe the switching operation; "V_{set}", "V_{reset}", "R_{LRS}" and "R_{HRS}" would be used to describe the set voltage, reset voltage, the resistance at low resistance state (LRS) and the resistance at high resistance state (HRS).

In the real circuits, it is the pulse mode of switching that is the practical operation method due to fast operation speed and lower power consumption. The waveforms of set and reset process are shown in Fig. 1-3(a) and (b) respectively. The pulse heights and widths for set and reset must take a balance. The larger of pulse heights are, the shorter of the pulse widths are needed. The reading pulses with small pulse heights are also designed not to vary the memory states.

For the memory array structure, 1D1R (1 diode and 1 resistor) or 1T1R (1 transistor and 1 resistor) structure (Fig. 1-4 and Fig. 1-5) must be used to prevent misreading as shown in Fig. 1-6. I. G. Baek *et al.* [24] reported that if a cell is in high resistance state and its neighboring cells are in low resistance state, it will be misread as low resistance state due to the leakage current path around its neighboring cells. Hence, a rectifying element is required for each cell in an array to limit the current paths. The minimum sizes for 1D1R and 1T1R structures are $4F^2$ and $6F^2$ respectively, and these structures would meet the requirement for high density arrays.

1.2 Conducting mechanisms in oxides [25]

Based on conductivity, transition metal oxides could be insulator, semiconductor or metal depending on the composition of the oxide materials. Hence the conducting mechanisms may vary because of their different physics and chemistry characteristics. The widely discussed materials in RRAM application generally belong to insulator or semiconductor according to the constitution and stoichiometry, and the electron conduction mechanisms mostly involved are Ohmic conduction, space charge limited current, Schottky emission, Frenkel-Poole emission and Tunneling. Furthermore, the current fitting procedure would give insight into the conduction mechanisms.

1.2.1 Ohmic conduction

Ohmic conduction takes place when the injected carrier density is far less than the thermally-generated carrier density. Generally, it applies to the condition of low electric field region in which thermally-generated carriers are dominant in conduction. The current-voltage characteristics follow Ohm's law that the current passing through a resistor from one terminal to the other is proportional to the voltage drop across two points. In addition, the temperature effect is also described in Ohmic conduction behavior. Due to the electron and phonon scattering effects, the conductivity rises with increasing temperature for conduction in semiconductor, while with decreasing temperature for metal conduction. The following is the expression for Ohmic conduction:

$$J = aV \exp\left(-\frac{c}{T}\right)$$

where a (and c) is constant, and V is the applied voltage.

1.2.2 Space charge limited current

The mechanism of space charge limited current (SCLC) is attributed to defects and usually exists in the dielectric stress by high electric fields. After charge injection from an electrode, the space charge may form if the charge carriers are trapped and distributed over a region of area without being neutralized. The further flow of charge carriers would be impeded by this space charge region. It should be noted that the injected carriers are most electrons. As for conductive media, the trapped carriers can be neutralized or screened rapidly; therefore, the space charge region would not form.

The completely trapped and controlled SCLC mechanism is composed into two stages [24], trap-unfilled SCLC and trap-filled SCLC, both can be written as the following expression:

$$J = \left(\frac{\theta}{\theta+1}\right)\frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

J is the current density, θ is the ratio of free electron to trapped electron, N_C is the effective density of states in the conductive band, Nt is the number of emptied electron traps, ε_0 is the permittivity of free space, ε_r is the static dielectric constant, μ is the electron mobility, V is the applied voltage and L is the film thickness. At first stage, the traps that are not filled with charges and the formula can be rewritten with θ <<1 as the following:

$$J = \theta\frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

As the voltage increases, the majority of traps are occupied by the injected carriers, and the current-voltage characteristics can be again rewritten with θ >>1:

$$J = \frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

1.2.3 Schottky emission

Schottky emission is mainly attributed to the Schottky contact of the metal-insulator interface. For the carriers to transport, they must jump across the barrier height of one of the interfaces, travel through the dielectric film, and eventually reach the other side. It is the thermionic emission that enables the carriers (most electrons) to overcome the interface barrier height. Therefore, temperature is the key factor that energetic carriers (hot carriers) are easier to jump across the barrier. The formula of Schottky emission is expressed as below:

$$J = A^* T^2 \exp\left(\frac{-q(\phi_b - \sqrt{qV/4\pi\varepsilon_r\varepsilon_0 d}}{kT}\right)$$

where A^* denotes Richardson constant, Φ_b is the Schottky barrier height, ε_0 is the permittivity of free space, ε_r is the dynamic dielectric constant, V is the external applied voltage and d is the insulator thickness.

1.2.4 Frenkel-Poole emission

Frenkel-Poole emission is pretty much similar to Schottky emission mechanism. The main differences are that Frenkel-Poole emission describes the process for carriers to overcome the barriers resulted from the defect states in the dielectric material, and the barrier lowering is twice as large as that in Schottky emission mechanism. Temperature is also crucial for this carrier transportation process, while electric field plays a more important role in this mechanism than in Schottky emission, which suggests that field effects possess greater impact on defect-related behavior. The current-voltage relationship can be written as the following formula:

$$J = BV \exp\left(\frac{-q(\phi_t - \sqrt{qV/4\pi\varepsilon_r\varepsilon_0 d}}{kT}\right)$$

where B is a material-related constant, Φ_t is the trap level, and other parameters are the same as those in Schottky emission.

1.2.5 Tunneling

Tunneling is the most common conduction mechanism through insulators under high fields. The tunnel emission is a result of quantum mechanism by which the electron wave function can penetrate through a potential barrier. It has the strongest dependence on applied voltage, but it is essentially independent of the temperature. Tunneling mechanism can be divided into direct tunneling and Fowler-Nordheim tunneling where carrier tunnel goes through a partial width of the barrier. The current-voltage relationship can be written as the following formula:

$$J \propto \xi_i^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar\xi_i}\right] \propto V^2 \exp\left(\frac{-b}{V}\right)$$

where ξ_i is the electric field in insulator, m^* is the effective mass, ϕ_B is the barrier height, and V is the applied voltage.

1.3 Models of resistive switching mechanisms

The major possible models having been proposed by other research groups are sorted partially as two parts, one is filament-type resistance switching and another is interface-type resistance switching [23]. The two models may be applied for some combinations of electrodes and oxide materials. For these models, however, are derived by indirect observation or electrical measurements, but the switching mechanisms are still well know because of the lack of directly proved evidence.

1.3.1 Filament-type resistive switching [23]

The filament-type model comes from the nature of oxide breakdown and integrity that defects existing in an oxide bulk, such as the interstitials, oxygen vacancies and metals constitute the leakage current path, indicated in Fig. 1-7 [28]. This model has been proposed since 1970's and is one of the earliest models in resistive switching mechanism [29, 30]. Recently, since nonvolatile memories possess obtained a lot of attention, the further and more detailed studies have been realized to investigate the possible mechanisms. All these proposed models, it is the filament-type model that prevails in many binary oxide films, such as TiO_2 [31], ZrO_2 [11], NiO [24] and Cu_xO [17]. The most obvious evidences for the filament-type model are conductive atomic force microscopy (CAFM) mapping results at low resistance state. C-AFM is one of the power tools to study the local conductivity throughout the film. B. J. Choi *et. al.* and reported that by scanning the film surface with CAFM, only several conductive points exist and account for the current conduction, as shown in Fig. 1-8 [12].

1.3.2 Interface-type resistance switching [23]

The interface-type resistance switching model is wide-spreading especially in the material system of PCMO [32] and Nb;STO [33]. This model can be further classified into two types in accordance with the type of semiconductor, the n-type semiconductor and p-type semiconductor. For example, the schematic for p-type semiconductor is illustrated in Fig. 1-9 [23].

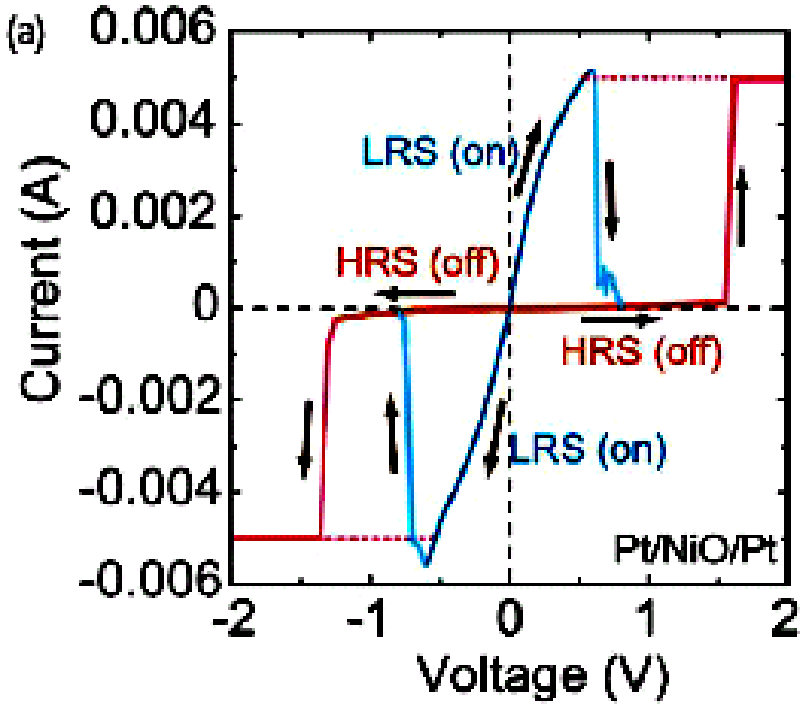


Figure 1-1. Typical linear *I-V* curves of RRAM switching in voltage sweeping mode (unipolar) [23].

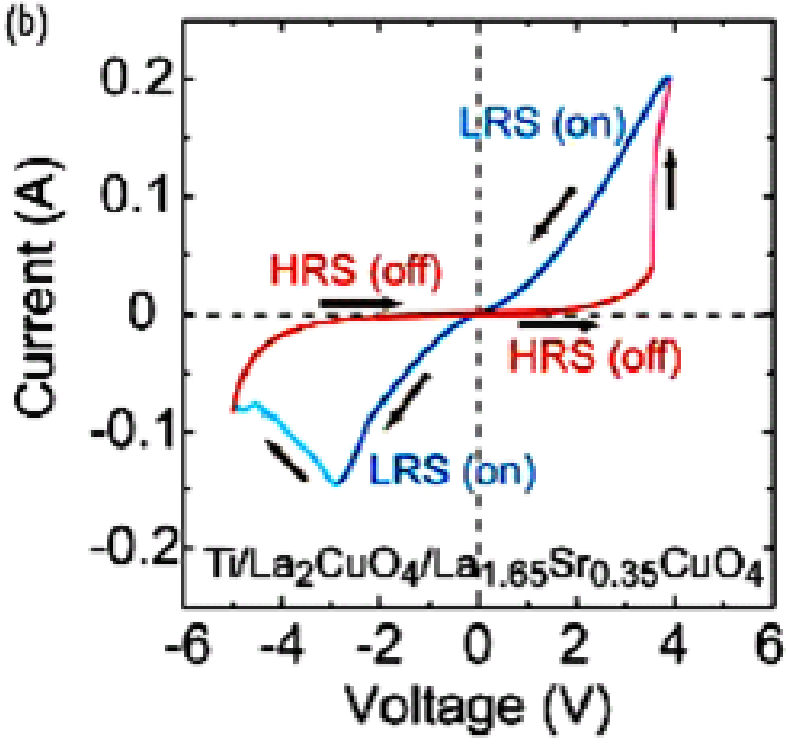


Figure 1-2. Typical linear *I-V* curves of RRAM switching in voltage sweeping mode. (bipolar) [23]

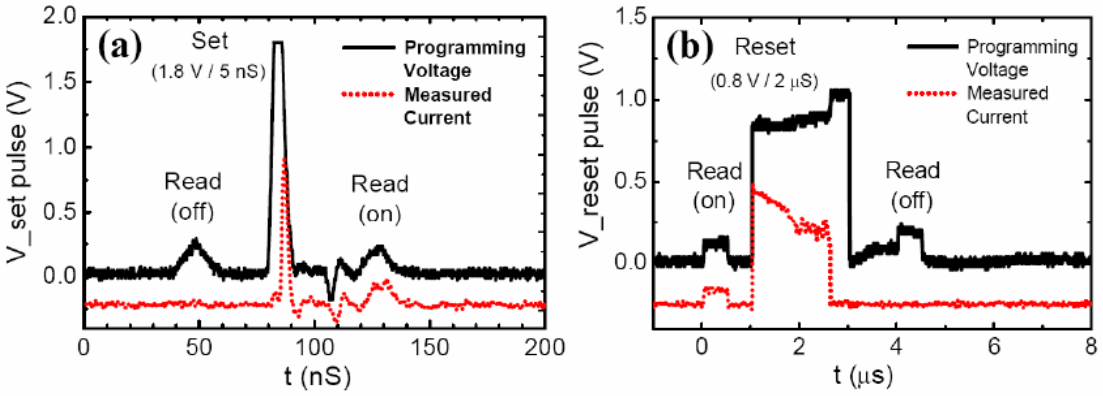


Figure 1-3. Switching dynamics monitored with programming and reading pulses. Pulse waveforms and transition for (a) set process and (b) reset process. [24]

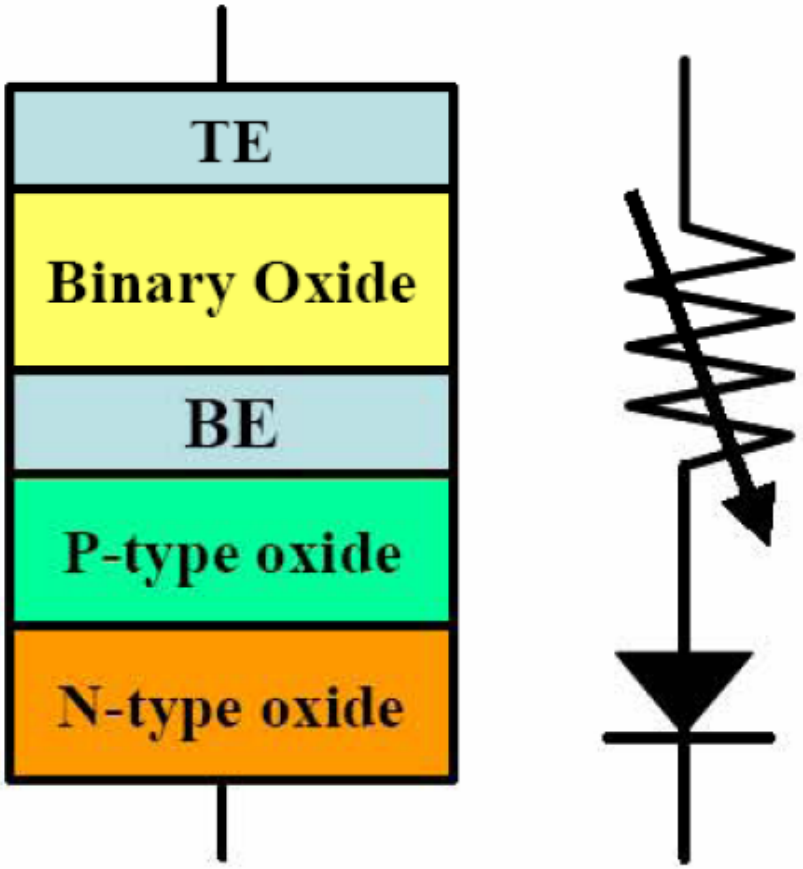


Figure 1-4. Conceptual schematic of 1D1R structure. [24]

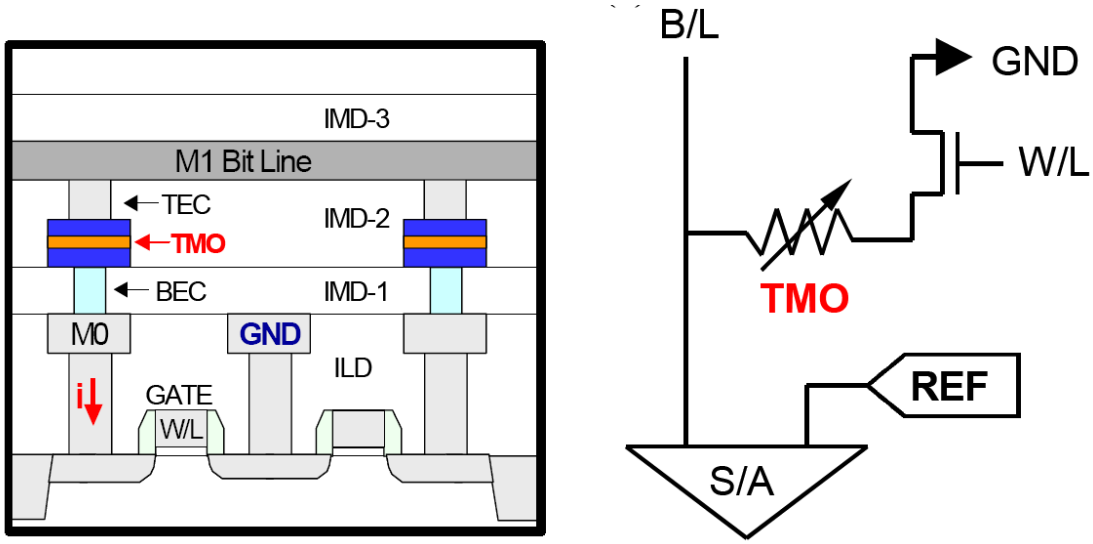


Figure 1-5. Cross-sectional schematic and basic circuit diagram of 1T1R structure. [26]

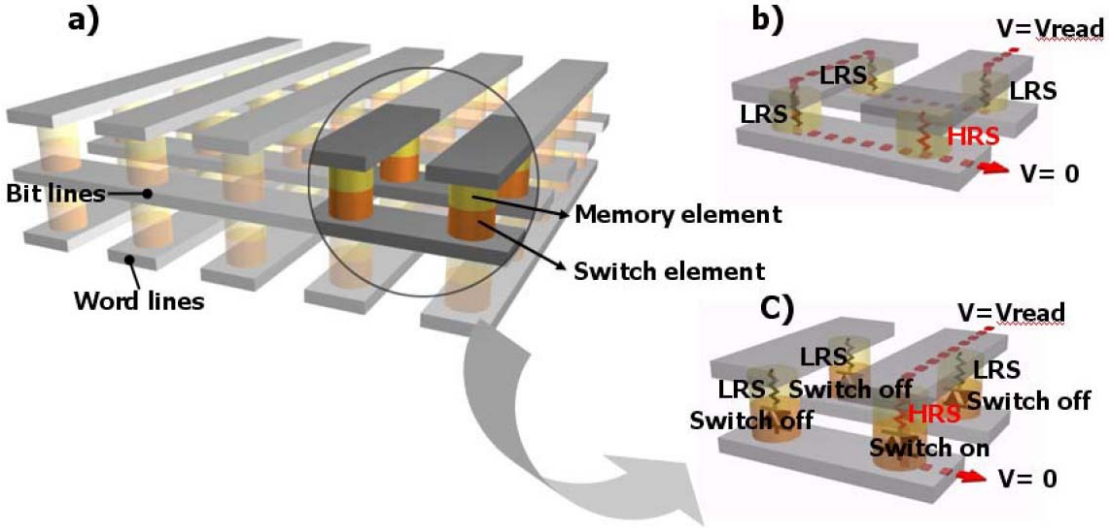


Figure 1-6. (a) Generalized cross-point structure with memory and switching elements. (b) Reading interference without switch elements. (c) Rectified reading operation with switch elements. [27]

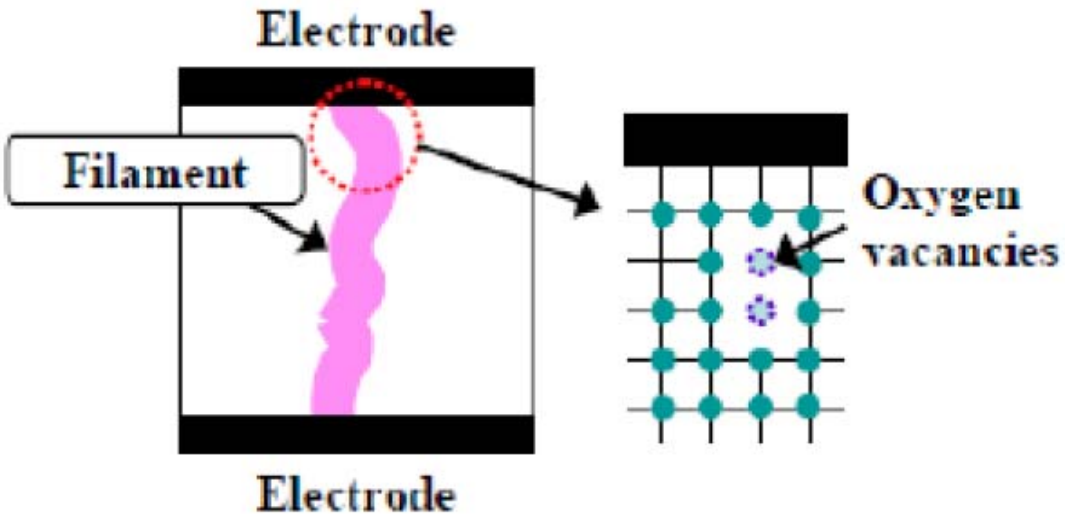


Figure 1-7. Schematic of the filament in an oxide. [28]

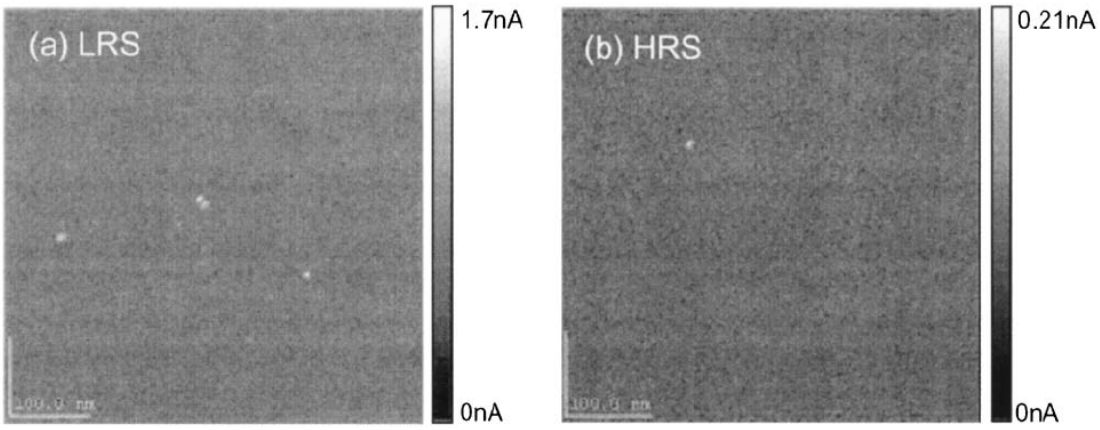


Figure 1-8. Conductivity mapping results of the (a) low resistance and (b) high resistance state TiO_2 films, using conductive AFM (CAFM). The bright spots represent the conducting points. [12]

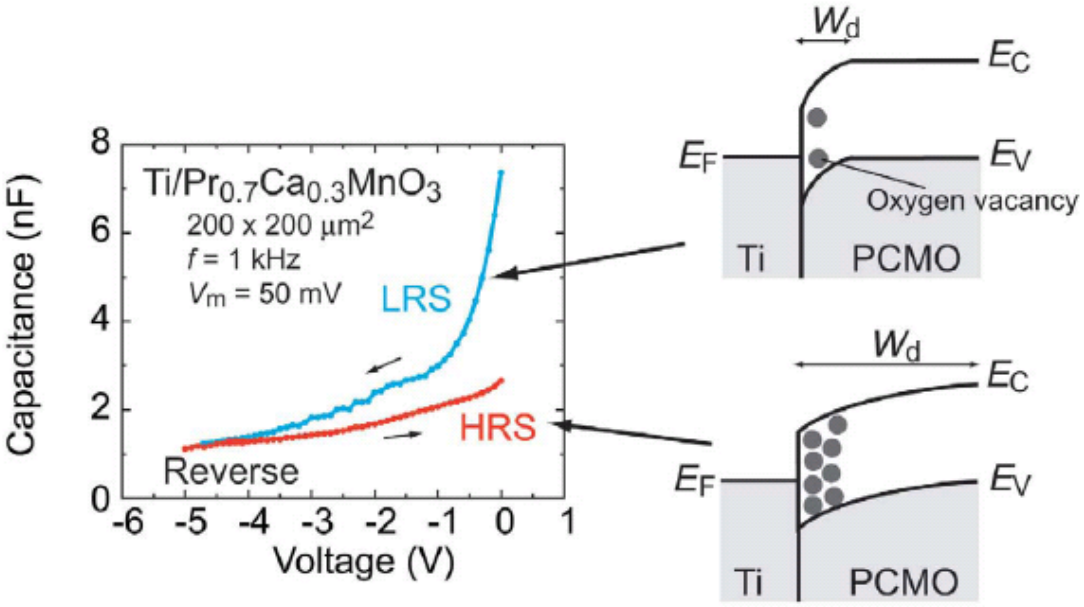


Figure 1-9. Band diagram with the conditions of p-type semiconductor for on state (LRS) and off state (HRS), respectively. [23]

Chapter 2

Experiment details

2.1 Motivation

The binary oxides adopted in RRAM application, such as TiO_2 [13], ZrO_2 [14], NiO [15], Al_2O_3 [16], Cu_xO [17], Fe_2O_3 [18], ZnO [19], HfO_2 [10], SiO_2 [20, 21] and MoO_x [22], are candidates or have been widely used in other field of CMOS devices. However, few researchers study SiO_2 which is a common and compatible material for CMOS process [20, 21]. Even through several models for the phenomenological results have been suggested [28], the universal physical origins of the resistance switching properties are still in question. Hence, in this thesis, SiO_2 with different metal electrode materials and structures, different thermal treatments, and small size structures are studied, and try to find out a possible model and resistance switching mechanism to explain.

2.2 Sample fabrication

In this thesis, the basic structure for studying SiO_2 resistance switching behaviors is depicted in Fig. 2.1. It was fabricated on P-type (100) silicon substrates (20-100 Ω-cm). After a standard RCA cleaning, a 500 nm SiO_2 film was grown as a buffer oxide by LPCVD. Subsequently, 50-nm-thick $Fe_{0.73}Pt_{0.27}$ layers were deposited by DC magnetron reactive sputtering method. The PtFe alloy electrode was Co-sputtered with Fe and Pt targets and its composition was measured by Inductively Coupled

Plasma Mass Spectroscopy (ICP-MS). 50nm SiO_2 layers were deposited by plasma enhanced chemical vapor deposition (PECVD) on $Fe_{0.73}Pt_{0.27}$ electrode at 300°C ambient. Finally, TiN top electrodes with defining area were formed on the SiO_2 films by DC magnetron reactive sputtering. And then 200nm passivation oxide was deposited to prevent humid environment. The process flow is depicted in Fig. 2.2, and all the details in each process are stated below.

2.2.1 Standard RCA clean

The bare Si wafers must be cleaned before further processes. The RCA clean is the industry standard for removing contaminants from wafers, and the main steps are narrated as the following. The wafers were submerged in Caro's acid (also called SPM), a solution of 3:1 H_2SO_4:H_2O_2, for 10 minutes at around 80°C to remove organic contaminants from the surface of wafer. Then, the wafers were in 1:100 HF: H_2O (diluted HF, DHF) to etch chemical oxide produced in the previous step. The following steps were standard clean 1 (SC1) and standard clean 2 (SC2), in which the wafers were soaked in a solution with 1:4:20 NH_4OH:H_2O_2:H_2O and 1: 1:6 HCl: H_2O_2: H_2O, respectively, both for 10 minutes at around 80°C to eliminate particles and metallic contamination. Finally, the wafers were dipped in DHF again to remove the chemical oxide grown in the previous standard clean steps. It should be noted that each step was separated by DI water rinse for 5 minutes.

The mechanism for Caro's acid to remove organic contaminants comes from its strong capability of dehydrating and oxidizing organic compound containing C-H bonding. As for SC1, the surface of Si wafer is oxidized by H_2O_2 into a thin SiO_2 layer, the footing layer for particles and in the meantime etched by NH_4OH. The particles attached on the surface would be removed as SiO_2 layer on the surface

finally vanishes. The following SC2 step further takes I_A and II_A metal ions away, in which chlorides resulting from the combination of I_A, II_A and Cl^- would dissolve in water and thus the metal ions are eliminated. On the other hand, III_A metal ions such as Al would be reactive with NH_4OH in SC1 and generates $AlOH_3$ which later forms chlorides in SC2. Hence, to remove particles and metal ions effectively, the sequential order of SC1 and SC2 cannot be reversed.

2.2.2 Growth of buffer SiO_2

After RCA clean, 6-in-boron-doped Si wafers were sent into a furnace immediately for thermal oxidation, in which SiO_2 was grown at 980°C in O_2 and H_2 atmosphere. The SiO_2 layer that plays a role of insulating layer avoiding current leakage from the Si substrate was expected to be 500 nm in thickness.

According to different mechanisms, there are two types of thermal oxidation, dry and wet oxidation. The former is oxidized in O_2 ambient, in which oxygen ions are combined with Si atoms to form SiO_2. The diffusion barrier for oxygen ions moving through the existed SiO_2 toward Si is getting larger as SiO_2 is becoming thicker, and thus dry oxidation is not suitable for the growth of thick SiO_2. For the 500-nm SiO_2 required in this study wet oxidation was adopted, using O_2/H_2 and forming OH^- ions which possess higher mobility going through SiO_2, to obtain higher growth speed.

2.2.3 Deposition of bottom electrode

50-nm-thick $Fe_{0.73}Pt_{0.27}$ layers were deposited by DC magnetron reactive sputtering method. The PtFe alloy electrode was Co-sputtered with Fe and Pt targets and its composition was measured by Inductively Coupled Plasma Mass Spectroscopy (ICP-MS). We also fabricated two different type electrodes in the bottom to

examination the resistance switching characteristics which would discuss in next section. 50-nm-thick Pt and 5-nm-thick Fe / 80-nm-thick Pt / 20-nm-thick Ti layers were also deposited by DC magnetron reactive sputtering method.

Sputter systems are widely adopted in film deposition due to the simple equipment structure, low cost and the capability of depositing all kinds of films. They use the ions in the plasma to bombard the target, and sputter out a large amount of target species onto the wafer, achieving the purpose of film deposition.

2.2.4 Preparation of insulator SiO_2

50-nm-thick or 30-nm-thick oxide is deposited by plasma enhanced chemical vapor deposition (PECVD) system at 300°C. The SiO_2 film is an insulator film, and studies the resistance switching characteristics on (beneath) different metal electrode materials.

2.2.5 Deposition of top electrodes

After deposition of insulator SiO_2, the top electrodes are prepared to form the structure of metal/insulator/metal. In the part of different structures to survey the resistance switching behaviors, the electrodes of 400-nm-thick aluminum (Al) or 80-nm-thick titanium (Ti) / 30-nm-thick titanium nitride (TiN) are deposited by the same DC magnetron reactive sputter system in 24 sccm Ar ambient (TiN electrode is in 24 sccm Ar + 5 sccm N_2). Furthermore, the tungsten (W) probe also can be our top electrode with the utmost care that the tip does not scratch or perforate the oxide surface.

Two kinds of the top electrodes (Al or Ti/TiN) mentioned above were patterned

by lithography and etching having the square-shaped patterns with side of 100 μm, i.e. areas of $1x10^{-4}$ cm^2. Furthermore, the W probe was the dot-shaped needle which diameter was 5 μm, i.e. areas of 19.63 μm^2. Moreover, different small size electrodes (30-nm-thick TiN) were also patterned by lithography and etching having the rectangle-shaped patterns with side matrix of 0.3, 0.6, 1.5, 3.0 and 5.0 μm.

2.2.6 Deposition of passivation oxide

In order to probe the pattern for small size electrode and prevent humid environment, deposition of the passivation oxide was needed. After the lithography and etching process for small size electrode structure, 200-nm-thickness passivation oxide was deposited by PECVD at 300°C. Then, the lithography and etching process were again needed to etch contact via for probing electrode (contact via is smaller than the top electrode) and bottom electrode (contact hole was square-shaped pattern with side of 100 μm).

2.2.7 Deposition of probing electrodes

After the contact via and contact hole were finished, the probing electrodes (Ti) for small size structure were deposition by DC magnetron reactive sputter system. Deposition of 800-nm-thick Ti on top electrode was patterned by lithography and etching process having the rectangle-shaped patterns with 100 μm side.

2.3 Analyses and measurements

In this thesis, several material analyses and electrical measurements were carried out to study the relationship between material properties and electrical characteristics.

The details will be stated in the following paragraphs.

2.3.1 Inductively coupled plasma-mass spectrometry (ICP-MS)

In order to know PtFe electrode composition, inductively coupled plasma-mass spectrometry is a useful tool to analyze. ICP-MS (Inductively coupled plasma mass spectrometry) is a type of mass spectrometry. It is highly sensitive and can determine a range of metals and several non-metals at concentrations below 10^{12}. Its mechanism bases on coupling together inductively coupled plasma, which produces ions (ionization), and a mass spectrometer will separate and detect the ions.

2.3.2 X-ray diffraction (XRD)

X-ray crystallography is the science that can determine the arrangement of atoms within a crystal. The mechanism of X-ray diffraction (XRD) is a beam of X-rays that are scattered from the electrons within the crystal. The most important step in X-ray crystallography is the diffraction of X-rays from a crystalline material.

2.3.3 X-ray photoelectron spectrometer (XPS)

X-ray photoelectron spectroscopy (XPS or someone called Electron spectroscopy of chemical analysis, ESCA) is a quantitative spectroscopic technique and a power tool that can measure the elemental composition, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by X-rays shoot on thin films while simultaneously detecting the kinetic energy (KE) and a number of electrons that escape from the top 1 to 10 nm depth of the material.

2.3.4 Auger electron spectroscopy (AES)

Auger electron spectroscopy (AES) is a normally analytical technique used in the

study of surfaces. Basically, the spectroscopic technique is the Auger effect. This analyzed technique is based on the analysis of energetic electrons emitted from an excited atom after a series of internal relaxation events. AES is a practical and straightforward characterization technique for probing chemical and compositional of surface.

2.3.5 Secondary ion mass spectroscopy (SIMS)

Secondary ion mass spectrometry (SIMS) is the mass spectrometry of ionized particles which are emitted from a surface that is bombarded by energetic primary particles, such as electrons, ions, neutrals or photons. The emitted secondary particles will be electrons, neutral species atoms, molecules, atomic or cluster ions. The emitted species are neutral but are the secondary ions, which will be detected and analyzed by a mass spectrometer. It can provide a mass spectrum of a surface composition and enable a detailed chemical analysis of a surface. Furthermore, SIMS can also provide a concentration profile of depth because Ar ions can bombard the surface and etch down.

2.3.6 Electrical measurements

The electrical properties were measured by the apparatuses consisting of a probe station with temperature controller, Keithley 4200 semiconductor characterization analyzer and low leakage switch, controlled by a Keithley 4200 computer.

The electrical measurements in this thesis are divided into 2 items, in which bistable resistive switching and endurance for memory device application. Both items will be studied for the fundamental resistive switching mechanisms.

2.3.6.1 Bistable resistive switching

This measurement was performed by Keithley 4200, detecting the conducting current while applying and dual sweeping DC biases on the devices. From the *I-V* curve, the low resistance state (LRS) has low resistance and high conductivity property, and the high resistance state (HRS) possesses high resistance and low conductivity feature, respectively.

2.3.6.2 Endurance

Endurance is a key feature about memory devices. After enormous number of switching cycles, the memory devices must meet the operation requirements in many applications, such as random access memory (RAM) and solid state disk (SSD). Because these applications need many data write-in operation without any failures, endurance is a basic requirement in almost every type of memory devices. The tests of endurance were carried out by DC biases, and the DC biases were applied to switch devices between LRS and HRS at room temperature (RT).

2.3.6.3 Retention

Retention is also a key feature about nonvolatile memory devices. It stands for the capability of retaining memory data for a long period without any data loss. For a commercially available nonvolatile memory product, the performance of retention is requested to keep ten years. The retention tests were carried out by DC biases which would switch devices to LRS or HRS at RT. Then, the data states were read out at RT once in a given period by applying a 0.2 V (or 0.5V) reading bias and the reading bias must be small enough in order not to vary the existed memory states.

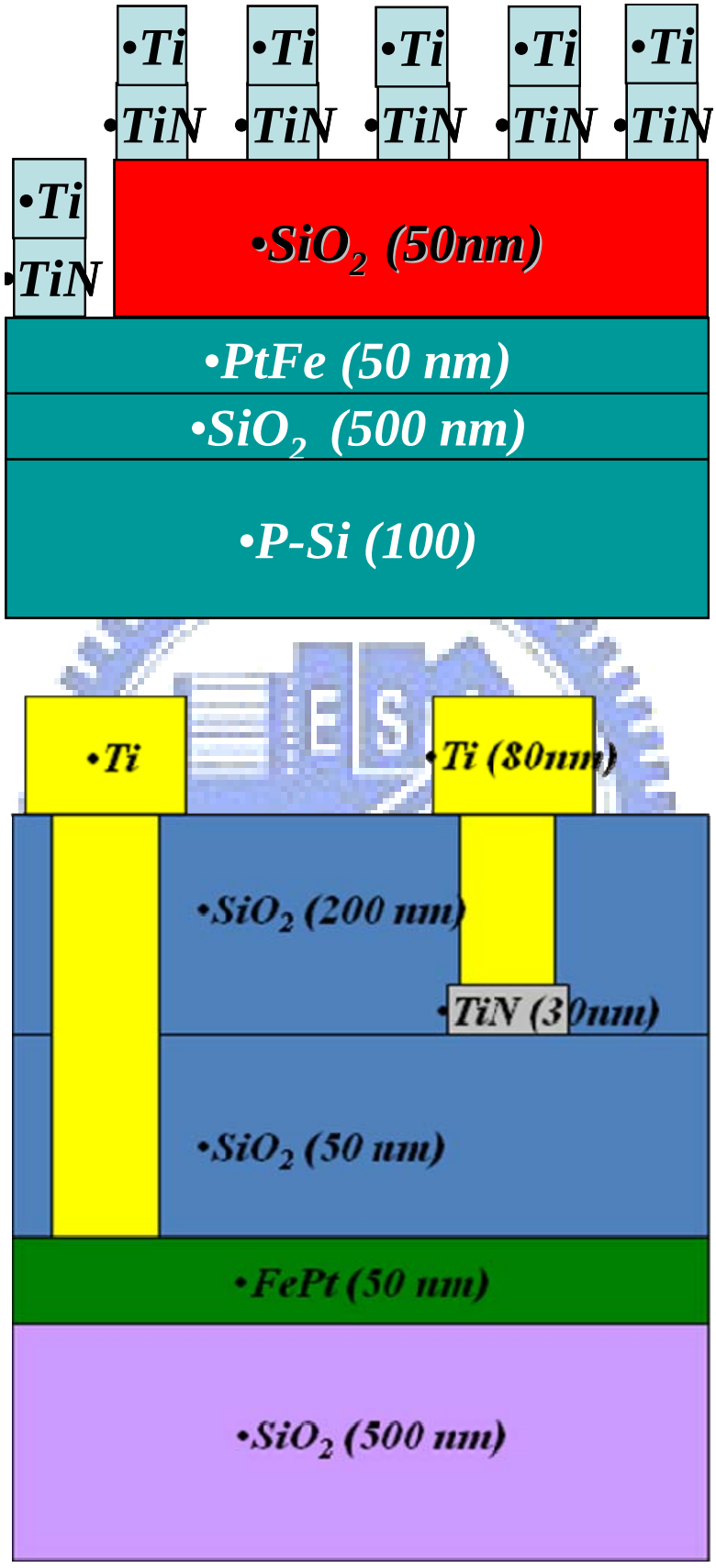


Figure 2.1. Schematic diagram of Ti/TiN/SiO_2/PtFe/SiO_2/Si structure, and its small size structure.

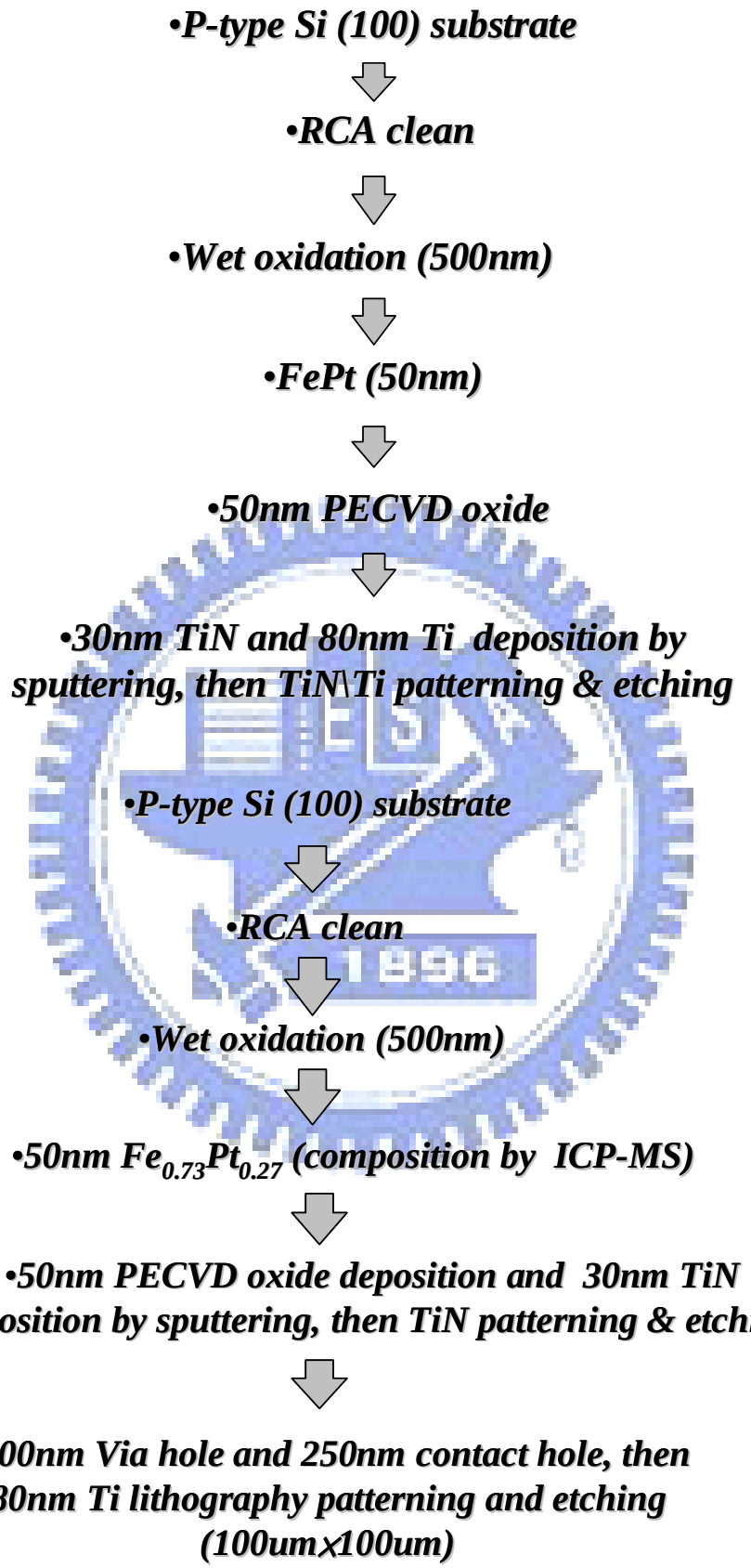


Figure 2.2. Process flows of Ti/TiN/SiO_2/PtFe/SiO_2/Si structure, and its small size structure.

Chapter 3

Results and discussions

In this chapter, four sections will be discussed. All of the devices are applied voltage in bottom electrodes, and the top electrodes are ground (Fig. 3-1).

(a) Device structures and characteristics.

(b) Bottom electrode metal effect.

(c) Thermal treatment effect.

(d) Small size effect.

3.1 Device Structures and Characteristics

In section 3.1, the resistive switching properties of different structures are examined and divided into three parts, including results of various bottom electrode metals, various top electrode metals, and various SiO_2 thickness.

3.1.1 Various bottom electrode metals

First of all, the resistive switching phenomenon is studied in Al (400nm) / SiO_2 (50nm) / Pt (50nm) structure and its depiction of process flows in Fig. 3-2 and Fig. 3-3. The initial state of as deposition Al / SiO_2 / Pt structure processes high resistance value before forming process (Fig. 3-4). It should be noted that, in the previous research, the Au/SiO_2/Al structure had resistance switching behavior [34]. However,

the Al/SiO_2/Pt structure in my thesis does not possess resistance switching phenomena after the forming process (Fig. 3-5).

In order to study resistance switching behavior for SiO_2 on alloy electrode, the Al (400nm) / SiO_2 (50nm) / PtFe (50nm) is fabricated. Its structure and process flows are depicted in Fig. 3-6 and Fig. 3-7. Unlike Al / SiO_2 / Pt structure, the Al / SiO_2 / PtFe structure processes stably and repetitively resistance switching behaviors after the forming process (Fig. 3-8). In order to clarify the mechanisms of resistance switching behavior, seven parts will be discussed in this section.

3.1.1.1 Mechanism of Forming Process

The forming process means that the application of a large voltage a will soften the breakdown of a device. In order to avoid the device being permanent damage, the measurement parameter would set a compliance current which is controlled by a feedback system in apparatus, like Fig. 3-9. A large voltage would produce a high electrical field which induces impact ionization breakdown (Fig. 3-10) in SiO_2 for Al / SiO2 / Pt structure [25]. Hence, there are many low resistance paths produced, like Fig. 3-11.

For the Al / SiO_2 / PtFe structure, it is at initial state and processes high resistance value before forming process (Fig. 3-12). During the forming process (Fig. 3-13), bottom PtFe electrode is applied in a large negative voltage which will produce a high electrical field. Hence, the breakdown of impact ionization would happen in SiO_2 and Fe_2O_3 which is formed on PtFe alloy electrode during the fabrication process (Fig. 3-14). Then, there are many low resistance paths produced in SiO_2, and an "electric faucet" would form in Fe_2O_3, depicted as Fig. 3-15 [37]. Further discussions

would be continued and its related switching mechanisms are similar with the set process.

3.1.1.2 Mechanism of Phase Change in the Reset Process

After the set and forming process, reset process is the second step to switch resistance. The reset process is that the bottom electrode applies positive voltage, and the top electrode is grounding, like Fig. 3-1. Due to the electrical field direction (Fig. 3-16) and high current flowed through the "electric faucet" [37], the oxygen ion and localization Joule heating (Fig. 3-17) [39] cause the phase change of Fe_3O_4 (Fig. 3-18) which is formed during the forming or set process. The chemical reaction possesses relationship as following [18]:

$$2\ Fe_3O_4 + O^{2-} \Rightarrow 3\ Fe_2O_3 + 2\ e^-$$

The resistance between Fe_2O_3 and Fe_3O_4 is different because the band gap of Fe_2O_3 and Fe_3O_4 are 2.6eV and 1.6eV, respectively [40, 41]. The total resistance of the insulating layer is the low resistance paths in SiO_2 series connection with Fe_2O_3 thin film which is less conductive. Hence, the phase change from Fe_3O_4 to Fe_2O_3 would switch the current or resistance from LRS to HRS in the process of reset.

3.1.1.3 Mechanism of Oxygen Vacancies in the Reset Process

To affect resistance switching behavior is another factor, the amounts of oxygen vacancies. Reset process follows the step of the set or following process. The voltage sweep mode is also the same with Fig. 3-1. Due to the electrical field direction (Fig. 3-16) and high current flowed through the "electric faucet" [37], the oxygen ion and localization Joule heating (Fig. 3-17) [39] would decrease the amounts of oxygen vacancies which are increased at electric faucet region during the forming or set

process. The chemical reaction possesses relationship as following [23]:

$$V^{\cdot\cdot} \text{ (donor)} + O^{2-} \Rightarrow O$$

Due to oxygen vacancies could be seen as donor type defects [23], they would supply electron concentrations in the intrinsic n-type Fe_2O_3 semiconductor (further discussion about band diagram would be continued in the next section) [38]. The less amounts of oxygen vacancies exist at the electric faucet, the less conductive paths would form. Therefore, after the reset process, the total resistance of the insulating layer is the low resistance paths in SiO_2 series connection with less oxygen vacancies of Fe_2O_3 thin film which is less conductive. The amounts of oxygen vacancies that are decreased in the intrinsic n-type Fe_2O_3 semiconductor would switch the current or resistance from LRS to HRS during the reset process.

3.1.1.4 Band diagram in the Reset Process

During the reset process, the phase change of Fe_2O_3 and oxygen vacancies both play important roles in causing resistance switching. After reset process, the band diagram of intrinsic n-type Fe_2O_3 semiconductor shows in Fig. 3-19. Finally, the Frenkel-Poole emission is predicted by current fitting with different temperature (shows in section 3.3.4) (Fig. 3-20).

3.1.1.5 Mechanism of Phase Change in the Set Process

After the reset process, set process is the second step to switch resistance. The set process is that the bottom electrode applies negative voltage, and the top electrode is grounding, like Fig. 3-1. Due to the electrical field direction (Fig. 3-21) and the applied power by measurement system, the electric faucet would be opened [37]. That means the phase change of Fe_2O_3 (Fig. 3-22) during the forming or set process. The

chemical reaction possesses relationship as following [18]:

$$2\ Fe_3O_4 + O^{2-} <= 3\ Fe_2O_3 + 2\ e^-$$

Due to band gap differences between Fe_2O_3 and Fe_3O_4, the total resistance of the insulating layer is the low resistance paths in SiO_2 series connection with Fe_3O_4 thin film which is conductive. Hence, the phase change from Fe_2O_3 to Fe_3O_4 would switch the current or resistance from HRS to LRS during the set process.

3.1.1.6 Mechanism of Oxygen Vacancies in the Set Process

The role of Oxygen Vacancies is also an important factor to cause resistance switching. First, the set process is the following step to switch resistance after reset process. The voltage sweep mode is also the same with Fig. 3-1. Due to the electrical field direction (Fig. 3-21) and the applied power by measurement system, the electric faucet would be opened in Fe_2O_3 after forming or set process [37]. The reason is that the amounts of oxygen vacancies would increase in some regions, and these regions represent highly conductive paths in Fe_2O_3 thin film. The chemical reaction possesses relationship as following [23]:

$$V^{"}\ (donor) + O^{2-} <= O$$

From the previous sections, oxygen vacancies could be seen as donor type defects, which could supply electron (donor) concentrations in the intrinsic n-type Fe_2O_3 semiconductor (further discussion about band diagram would be continued in the following section) [38]. The more amounts of oxygen vacancies exist at the electric faucet, the more conductive paths would form. Hence, after the set process, the total resistance of the insulating layer is the low resistance paths in SiO_2 series

connection with many oxygen vacancies of Fe_2O_3 thin film which is highly conductive. The amounts of oxygen vacancies increased in the intrinsic n-type Fe_2O_3 semiconductor would switch the current or resistance from HRS to LRS during reset process.

3.1.1.7 Band diagram in the Set Process

During the set process, the phase change of Fe_2O_3 and oxygen vacancies both play important roles to cause resistance switching. After set process, the band diagram of enhanced n-type Fe_2O_3 semiconductor shows in Fig. 3-23. Finally, the tunneling is predicted by current fitting with different temperature, where the current is less temperature sensitive at LRS (shows in section 3.3.4) (Fig. 3-24).

3.1.2 Effects of Top Electrode Metal Effects

In order to clarify where the key point to cause resistance switching is from, there were many studies had been done before. Therefore, many possible models have been proposed to explain where resistance switching occurred [28]. From the 3.1.1 section, the bottom PtFe electrode is the key point to cause resistance switching. Hence, in order to prove that two different top electrode metals (Al (400nm) and Ti (80nm) / TiN (30nm)) are fabricated, and using W probe becomes top electrode with the utmost care that tip does not scratch or perforate the oxide surface. The bistable resistance switching properties have been found in these three structures (Fig. 3-25 (a)-(c)). These evidences show that the top electrode region is not the dominant factor to cause resistance switching. Furthermore, work function difference (TiN: 4.8~5.3 eV; W: 4.5 eV; Al: 4.1 eV) in some cases would affect the resistance switching behavior, like contact between metal and p-type or n-type semiconductor [32, 33]. However, this effect does not observe in our case. To Sum up, the top electrode metals do not

affect the resistance switching behavior about the electrode/SiO_2/PtFe structure.

3.1.3 Effects of SiO_2 Thicknesses

The final part wants to discuss different SiO_2 thickness effects. Two different structures have been fabricated, and they only adjust SiO_2 thickness (50nm and 30nm) in both structures (Fig. 3-26 (a)-(b)). In order to let them possess bistable resistance switching characteristics, forming process must do in both structures. From the electrical results, both structures need the same forming electric field (~5MV/cm) to let devices possess bistable resistance switching (Fig. 3-27 (a)-(b)). These phenomena indicated that SiO_2 thickness would not affect resistance switching properties, and they only affect forming process (voltage amplitude) which lets SiO_2 thin film produces impact ionization breakdown.

3.1.4 Summary I

From the above analysis, we could conclude three points to cause resistance switching characteristics from these different structures.

(a) Bottom electrode contains Fe elements play an important role to cause bistable resistance switching. Proposed models and mechanisms about electric faucet, Redox of Fe_2O_3, oxygen vacancies, and band diagram could explain the bistable resistance switching behavior.

(b) In the SiO_2/FePt system, the resistive memory switching phenomena are independent of top electrode metal effects.

(c) SiO_2 thickness effects do not affect resistance switching behaviors when it suffers from impact ionization breakdown.

3.2 Effects of Bottom Electrode Metals

In order to understand more details about resistance switching characteristics for Ti/TiN/SiO_2/PtFe structure, the Ti/TiN/SiO_2/Fe/Pt/Ti structure is also fabricated to demonstrate why the Ti/TiN/SiO_2/FePt structure possesses resistance switching characteristics. Both structures and process flows show in Fig. 3-28 (a)-(c). It is interesting that the original structure (electrode/SiO_2/Pt) does not possess resistance switching behavior. However, if the original structure is inserted by a thin Fe film between SiO_2 and Pt, this modified structure comes to possess bistable resistance switching property.

3.2.1 Electrical properties

3.2.1.1 Bistable Resistance switching

Fig. 3-29 (a)-(b) are bistable resistance switching characteristics for Ti/TiN/SiO_2/FePt and Ti/TiN/SiO_2/Fe/Pt/Ti structures. The forming process needs between both structures, and the forming electrical field is 5.13MV/cm and 5.46MV/cm respectively. According to 3.1.3 section analysis, SiO_2 thickness will not affect resistance switching properties, and they only affect forming process (voltage amplitude) which lets SiO_2 thin film produces impact ionization breakdown. Hence, forming electrical field is almost the same between both structures. There is another key point behind these phenomena that is the interfacial Fe element that can cause resistance switching behavior (The original structure of electrode/SiO_2/Pt does not possess stable resistance switching behavior).

3.2.1.2 Current-Voltage Fitting

Fig. 3-30 shows the current-voltage fitting results of Ti/TiN/SiO_2/FePt and Ti/TiN/SiO_2/Fe/Pt/Ti structures. There are three important points in this result.

First, at low resistance state, the current transports of both structures are similar and the fitting results are Ohmic law (Slope of ln (I) vs. ln (V) curve is 1).

Second, at high resistance state low voltage bias region, the current transports of both structures are also similar and the fitting results are Ohmic law (Slope of ln (I) vs. ln (V) curve is 1).

Third, at high resistance state high voltage bias region, the current transports of both structures are similar again, and the fitting results are close to Frenkel-Poole emission (the relationship of ln (J/V) vs. $V^{1/2}$ curve is linear).

From the current-voltage fitting results, indicated that both of structures (Ti/TiN/SiO_2/FePt and Ti/TiN/SiO_2/Fe/Pt/Ti) possess the similar current transport characteristics.

3.2.1.3 I-V Characteristics Distribution

Fig. 3-31 (a)-(c) depicts that set (reset) voltage, set (reset) current and set (reset) power dissipation for the both structures. All the statistics results are extracted from five samples and 300 times bistable resistance switching per sample.

From the set and reset voltage distribution, PtFe bottom electrode structure need less value to cause resistance switching than Fe bottom electrode structure (area is 100*100um^2 and compliance current is 5mA).

From the set current distribution, PtFe bottom electrode structure also needs less value than Fe bottom electrode structure (the reset current distributions for both structures are not obviously different, but still possess the same tendency: PtFe structure needs less value to cause reset process than Fe structure).

Finally, from the set and reset power dissipation distribution, PtFe bottom electrode structure needs less value to cause resistance switching than Fe bottom electrode structure. From the above analysis, the conclusion is that the bottom PtFe electrode structure possesses property of saving more resistance switching power than bottom Fe electrode structure during set and reset process.

3.2.2 Summary II

To sum up, there are three conclusions between Ti/TiN/SiO_2/FePt and Ti/TiN/SiO_2/Fe/Pt/Ti structures.

(a) Interfacial Fe element is the most critical point to cause resistance switching.

(b) PtFe and Fe bottom electrode structures possess the similar electrical characteristics in HRS or LRS.

(c) During set and reset process, Ti/TiN/SiO_2/FePt structure saves more resistance switching power than Ti/TiN/SiO_2/Fe/Pt/Ti structure.

3.3 Thermal Treatment Effects

Three thermal treatment methods (as-deposition, furnace annealing 600^{o}C, 30min in vacuum and rapid thermal annealing 600^{o}C, 60s at atmospheric pressure in

N_2 or air condition) are studied for their resistance switching characteristics for Ti/TiN/SiO_2/FePt structure.

3.3.1 Electrical Characteristics

3.3.1.1 Bistable resistance switching and Endurance

Fig. 3-32 (a) and (b) show the bistable resistance switching behavior and its DC endurance for as-deposition condition of the Ti/TiN/SiO_2/PtFe structure. Although as-deposited sample possesses bistable resistance switching, its endurance is poor. The reading current of the LRS and HRS is too close to determine memory ability (the LRS/HRS current ratio at least 1 order) and the endurance reliability is less than 300 times. One thing in the forming electrical field that deserves to be mentioned is 5.13MV/cm.

Fig. 3-33 (a) and (b) depict the bistable resistance switching and its DC endurance for furnace annealing 600^{o}C 30min in vacuum of the Ti/TiN/SiO_2/FePt structure. Furnace annealing sample possesses bistable resistance switching, and its endurance reliability is better than as-deposited sample. The 0.2V reading current ratio of the LRS/HRS is higher than 1 order over 1000 times that can determine “1” or “0” by periphery circuit. Moreover, unlike the as-deposited sample, the forming electrical field of furnace annealing sample is 0.08 MV/cm.

Fig. 3-34 (a) and (b) indicate the bistable resistance switching and its DC endurance for rapid thermal annealing 600^{o}C 60s in N_2 (air the same) ambient of Ti/TiN/SiO_2/FePt structure. Rapid thermal annealing sample possesses bistable resistance switching as well as Furnace annealing and as-deposited sample. Furthermore, the endurance reliability is also good for rapid thermal annealing

600°C 60s sample. The 0.2V reading current ratio of the LRS/HRS is higher than 1 order over 1000 times which can let the periphery circuit determine “1” or “0” bit. Besides, the forming electrical field is 1.25 MV/cm for RTA sample.

Due to above analyses, the electrical characteristics and endurance reliability of different thermal treatment methods in Ti/TiN/SiO_2/FePt structure can sum up by Fig. 3-35 and Table 3-1 which point out three key points:

1. Endurance reliability: FA ~ RTA > As-Deposition.
2. LRS current value: FA > RTA > As-Deposition.
3. HRS current value: FA ≧ RTA > As-Deposition.

3.3.2 Material analysis

3.3.2.1 SIMS

SIMS results are shown in Fig. 3-36, indicating the Fe concentration in the 50-nm SiO_2 of different thermal treatment conditions. In RTA sample, like as-deposited sample, also possesses the similar Fe concentration profile which is near the interface region between SiO_2 and PtFe bottom electrode. However, the Fe concentration profile for FA sample is different with the others. Due to FA sample which suffers long time annealing property, Fe element possesses more time to diffuse in SiO_2 than as-deposited and RTA sample.

3.3.2.2 XPS

Fig 3-37 shows XPS results between SiO_2 and bottom PtFe electrode region in Ti/TiN/SiO_2/FePt structure, and indicates that all of the thermal treatments possess the

same chemical state, Fe and Fe^{3+} (the $2p_{3/2}$ binding energy is 707eV and 710.6eV, respectively) [35].

3.3.2.3 XRD

Fig. 3-38 shows XRD results of different thermal treatment conditions. In the XRD result of the as-deposited sample, there is no apparent Fe_2O_3 crystallinity at 33.19^o [36]. It means that the as-deposited sample possesses Fe^{3+} chemical state at SiO_2 and PtFe bottom electrode interface region from the XPS result, but the crystallinity of Fe_2O_3 is amorphous and small amount from the XRD result. However, FA and RTA conditions possess obvious crystallinity because both of them must be suffered high temperature annealing which would let Fe_2O_3 possess enough energy to crystallize. Furthermore, RTA sample has more crystalline than FA sample because of the annealing ambient difference. The annealing ambient of the FA sample suffered high temperature annealing (600^oC) in vacuum can not provide enough O element into SiO_2 and PtFe bottom electrode interface region. Hence, from the XRD result, the crystallinity peak of the Fe_2O_3 is broad. On the other hand, the annealing ambient of the RTA sample suffered high temperature (600^oC) in atmosphere can provide O element into SiO_2 and PtFe bottom electrode interface region. Therefore, from the XRD result, the crystallinity peak of the Fe_2O_3 is sharp.

3.3.3 Comprehensive Comparison

3.3.3.1 Endurance Reliability

From the above discussions, Fe_2O_3 thin film which is between SiO_2 and bottom PtFe electrode region in Ti/TiN/SiO_2/FePt structure is the most important component to cause bistable resistance switching, and the thermal treatment conditions would affect the endurance reliability and current value. Hence, XPS and XRD analyses are

the powerful tools which could provide the information about Fe_2O_3 chemical state and crystallinity. From the above electrical characteristics, as-deposited sample possesses the poorest reliability (about 300 times bistable resistance switching) in comparison with FA and RTA samples (over 1000 times bistable resistance switching). This property is similar with the XPS and XRD results because both of the analysis tools show small amounts of Fe_2O_3 chemical state (integral area of XPS fitting) and crystallinity for as-deposited sample. On the other hand, RTA and FA samples possess more amounts of Fe_2O_3 chemical state (integral area of XPS fitting) and better crystallinity than as-deposited sample. Therefore, the relationship between Fe_2O_3 thin film quality and endurance reliability is very close. FA and RTA samples possess good endurance reliability because they have large amounts of Fe_2O_3 thin film between SiO_2 and PtFe bottom electrode interface region and good crystallinity of Fe_2O_3. On the contrary, as-deposited sample does not possess good endurance reliability due to its less amounts of Fe_2O_3 thin film and bad crystallinity of Fe_2O_3.

3.3.3.2 The Low Resistance State

Fig 3-39 shows the possible mechanisms for FA and RTA condition at LRS. From the SIMS results, Fe element of FA sample diffuses deeper and higher concentrations in SiO_2 than RTA and as-deposited sample. These Fe ions produce many oxygen vacancies in SiO_2, and these oxygen vacancies would affect the forming electrical field and set voltage, like Fig. 3-40. The forming electrical field and set voltage for FA sample is smaller than RTA sample (as-deposited sample is similar). Furthermore, the more oxygen vacancies exist in SiO_2 and Fe_2O_3 thin film, the more conductive paths form during the set or forming process. FA sample makes more current flow than RTA sample under the same electric measurement condition.

3.3.3.3 The High Resistance State

From the SIMS results, Fe element of FA sample diffuses more depths and concentrations in SiO_2 than RTA and as-deposited sample. After the reset process, the electric faucets in Fe_2O_3 are close and the device is at high resistance state (the total resistance is dominated by Fe_2O_3 thin film resistance). These results indicate that the quality of the Fe_2O_3 layer (the amounts of oxygen vacancies) is the key point to influence the electrical characteristics at HRS. Hence, in FA sample, the amounts of the oxygen vacancies in Fe_2O_3 layer are more than in RTA sample. The current value of FA sample is a little larger than RTA sample at HRS, because these oxygen vacancies would provide extra carriers (donors) to dope lightly n-type semiconductor that would affect the resistivity of Fe_2O_3 thin film.

3.3.4 Summary III

To sum up, there are three conclusions for Ti/TiN/SiO_2/PtFe structure with different thermal treatment conditions.

(a) Thermal treatment would improve endurance reliability.

(b) RTA condition sample possesses the best electric characteristics in comparison with as-deposited and FA sample.

(c) The amounts of Fe_2O_3 and oxygen vacancies would affect the device endurance reliability and electrical characteristics.

3.4 Small Size Effects

3.4.1 Experimental

Structures for the RRAM devices were fabricated on P-type (100) silicon substrates (20-100 Ω-cm). After a standard RCA cleaning, a 500 nm SiO_2 film was grown as a buffer oxide by LPCVD. Subsequently, 50-nm-thick $Fe_{0.73}Pt_{0.27}$ layers were deposited by DC magnetron reactive sputtering method. The PtFe alloy electrode was Co-sputtered with Fe and Pt targets and its composition was measured using an Inductively Coupled Plasma Mass Spectroscopy (ICP-MS). 50nm SiO_2 layers were deposited by plasma enhanced chemical vapor deposition (PECVD) on $Fe_{0.73}Pt_{0.27}$ electrode at 300°C ambient. Finally, top electrodes TiN with defining area were formed on the SiO_2 films by DC magnetron reactive sputtering. And then 200nm passivation oxide was deposited to prevent humid environment. The electrical properties were measured using Keithley 4200 semiconductor characterization analyzer in DC sweep mode. To avoid a complete dielectric breakdown, we used compliance current to set a limit current flow.

3.4.2 Bistable Resistance Switching

Fig. 3-41 (a)-(d) depicts structure, structure process flows, and typical bipolar I-V curves of sample Ti/TiN/SiO_2/PtFe. The bottom electrode operated by voltage sweep mode and top electrode (7.5um^2) was grounded. The initial forming voltage was -8V to let PECVD oxide produce impact ionization breakdown. As can be seen, a conspicuous I-V hysteresis was observed when the bias was swept back and forth. Resistance switching from the high resistance state (HRS) to the low resistance state (LRS) is induced in voltage sweep mode by decreasing the voltage up to a value

(which we here defined as V_{set}) where an abrupt increase in current I was observed. The current of the LRS increased with increasing the voltage bias in the positive direction, and a rapid switching from LRS to HRS can be achieved at a positive bias voltage (which we defined as V_{reset}). The resistance ratio between the two states (HRS/LRS@0.5V) was about 500 times which is significant for sensing the different resistance states.

3.4.3 Material Analysis

Fig. 3-42 (a) and (b) show the depth profile of elements in SiO_2/FePt stack layers and examination of the transition region between oxide and bottom PtFe electrode by X-ray Photoelectron Spectroscopy (XPS). The XPS peak position at Fe ($2p_{3/2}$) and Fe_2O_3 ($2p_{3/2}$) is 707eV and 710.4eV in our experiment, respectively. Furthermore, there is a peak between Fe and Fe_2O_3, which indicated nonstoichiometric Fe_2O_3 in the transition region and may cause some oxygen vacancies and Fe^{3+} interstitials.

3.4.4 Current Fitting

For unambiguous understanding the possible current transport mechanism, the current transport of Ti/TiN/SiO_2/FePt structure is fitted in Fig. 3-43. There are three important parts in this result. First, at LRS, the current transport is fitting to Ohmic low (Slope of ln (I) vs. ln (V) curve is 1) and it is less temperature sensitivity (insert figure). Second, at HRS low voltage bias region, the current transport is also similar at LRS and its current characteristic is fitting to Ohmic low (Slope of ln(I) vs. ln(V) curve is 1). Third, at HRS high voltage bias region, the current transport fitting result is close to Frenkel-poole emission mode (ln (J/V) vs. $V^{1/2}$ curve is linear). Furthermore, at HRS high voltage bias region, the relationship of different temperature and current transport have also been done (insert figure). The fitting

result shows that Frenkel-Poole model was the possible mechanism.

3.4.5 Size Effects

From previous sections, a possible “electric faucet” model is proposal, where the “electric faucet” is represented some conductive paths at high resistance interface region. In order to construct a clearer image of resistance switching, the size-dependence was investigated in the Ti/TiN/SiO_2/FePt structure.

In Fig. 3-44, the HRS resistance was almost proportional to the area of the top TiN electrode. This indicates that, in HRS, the current flowed to all electrode area homogeneously. Hence, at HRS, the electric “faucet” closes, and electrons pass through some low resistance paths of SiO_2 and high resistance of Fe_2O_3. Because of electric circuit’s theory, if a high resistance series a low resistance, the total resistance is dominated by high resistance value. Here, HRS is the same condition, and total resistance is dominated by high resistance region of Fe_2O_3 thin film.

On the other hand, in Fig. 3-44, the resistance of LRS did not depend on the area of the top TiN electrode. This indicates that, in LRS, the current flowed inhomogeneously. Hence, at LRS, the electric “faucet” opens, and electrons pass through some low resistance paths of SiO_2 and some conductive paths in thin Fe_2O_3 film. Inoue *et. al.*, had also observed the similar phenomena and already proposed the “electric faucet” model [37]. However, how to produce or recover “electric faucet” is the key point to understand RRAM mechanism. Further discussion would be continued in the next sections.

3.4.6 Set Process with Different Sizes

Fig. 3-45 (a)-(c) show the different devices of Ti/TiN/SiO_2/PtFe structure and set parameters. From the Fig. 3-45 results, there are three important key points. First, from the Fig. 3-45 (a), set current density is decreased when top electrode area is increased. Hence, set current density is dependent upon top electrode area. Second, from the Fig. 3-45 (b), unlike set current density, set voltage is increased with top electrode area. This result indicates that set voltage is also dependent upon top electrode area. Finally, from the Fig. 3-45 (c), set power per area is independence with top electrode area.

To sum up, set process is related to the current density and voltage bias. Before set process, the initial state of sample is at HRS. According to section 3.4.5, the HRS resistance was almost proportional to the area of the top TiN electrode. This indicates that, in HRS, the current flowed to all electrode area homogeneously. Hence, at HRS, the electric "faucet" closes, and electrons pass through some low resistance paths of SiO_2 and high resistance of Fe_2O_3. Hence, both of set voltage that produced high electric field on thin Fe_2O_3 film and high set current density are critical factors to produce oxygen vacancies and phase change energy (J_{set} * E_{set} = set power per area) in the set process.

3.4.7 Reset Process with Different Sizes

Fig. 3-46 (a)-(c) show the different devices of Ti/TiN/SiO_2/PtFe structure and reset parameters. From the Fig. 3-46 results, there are also three important key points in the reset process. First, from the Fig. 3-46 (a), reset current is increased with top electrode area. Then, reset current density is dependent upon top electrode area. Second, from the Fig. 3-46 (b), unlike reset current, reset voltage is independent of

top electrode area. Finally, from the Fig. 3-46 (c), reset power (V_{reset} * I_{reset}) is independent of top electrode area.

To sum up the above results and analyses, resistance switching reset process is strongly related to current. Before reset process, the initial state of sample is at LRS. According section 3.4.5, the resistance of LRS did not depend on the area of the top TiN electrode. This indicates that, in LRS, the current flowed inhomogeneously. Thus, at LRS, the electric "faucet" opens, and electrons pass through some low resistance paths of SiO_2 and some conductive paths in thin Fe_2O_3 film. Then, the high reset current would flow through local "electric faucet", and that would cause high local Joule heating at the "electric faucet" region, not related to the top electrode area. The result from Fig. 3-46 (c) also agrees with this mechanism which the reset power (local Joule heating) is unconnected with top electrode area. Hence, both the reset currents that produced high local Joule heating at electric faucet region and reset power are critical factors to recover oxygen vacancies and to change their phase in the reset process.

3.4.8 Compliance Current and Switching Process

3.4.8.1 Physical Model of Electric Faucet

From section 3.4.5, electric faucet model is mentioned and examined by size effects. In the electric faucet model of Ti/TiN/SiO_2/PtFe structure, some low resistance paths in SiO_2 are smaller than some low resistance paths in Fe_2O_3 because of the electric characteristics of Al/SiO_2/Pt structure (Fig. 3-5 and Fig. 3-11). After the forming process of Al/SiO_2/Pt structure, there are some Si interstitials and defects produced in SiO_2, and they would form some low resistance paths. From the I-V curve (after forming process) of the Al/SiO_2/Pt structure (shows in Fig. 3-5), the

resistance of the Al/SiO_2/Pt structure is above 10Ω at 0.5V reading. Then, the resistance of the Ti/TiN/SiO_2/PtFe structure is dominated by thin Fe_2O_3 film which is approximated as 2kΩ at 0.5V reading at LRS). The relationship as following (LRS):

$$\because R_{SiO_2} < R_{Fe_2O_3}$$

Fig. 3-47 shows that the relationship between LRS reading resistance (50 times, 3 samples) distribution and different compliance currents. This result could descript the electric faucet characteristics more clearly. The resistance variation and average resistance at LRS is decreased with compliance current. According to the Ohmic law, the resistance possesses relationship as following:

$$R_{Fe_2O_3}|_{average} = \rho_{Fe_2O_3} \frac{d_{transition}}{A_{average}}$$

This formula indicated that when the resistance of Ti/TiN/SiO_2/PtFe structure is decreasing with the compliance current at LRS, the average electric faucet total cross sections are increasing, like Fig. 3-48. At small compliance current condition, the resistance variation increases because the small cross sections of electric faucet possess high variation property. However, at large compliance current condition, the resistance variation decreases because the large cross sections of electric faucet possess small variation characteristic. For the above analyses, there is an assuming condition that a normal cross section variation for every electric faucet is the same. When the electric faucet's cross section is small, the ratio causing by electric faucet variation is large. When the electric faucet's cross section is large, the ratio causing by electric faucet variation is small. This physical image could easily explain the electrical results of Fig. 3-47.

Due to the physical picture, the reset power must increase with compliance current at the same top electrode area (Fig. 3-48), and can be explained. Because the process of small compliance current produces small cross sections of electric faucet, the reset power indeed becomes small to recover oxygen vacancies and to change phase. However, the process of large compliance current would produce large cross sections of electric faucet, and the reset power is indeed large to recover oxygen vacancies and to change phase.

3.4.8.2 Mathematical Model of Electric Faucet

Even through physical model of electric faucet constructs, statistics mathematic methods can understand the electric faucet characteristics more clearly.

There are some parameters which need to be defined. First, the average cross section area of the electric faucet is defined by LRS reading current as following:

$$Faucet-Average-Area:\bar{x}=\frac{\sum_{i=1}^{n}x_i}{n}$$

Second, electric faucet variation is also defined by LRS reading current variation as following:

$$Electric-Faucet-Variation=\frac{\sum_{i=1}^{n}|(x_i-\bar{x})|}{n}$$

Fig. 3-49 shows that the relationship between compliance current and electric faucet variation, respectively. The linear and quadratic equations are fitting in with the data. Although the electric faucet variation possesses a tendency that small (large)

compliance current possesses large (small) electrical characteristic variation, the relationship between the electric faucet variations and the electrical distributions variations is not totally dependent. Therefore, the physical and mathematical models need to be modified by unknowing factors.

3.4.9 Summary

To summarize, there are two conclusions for Ti/TiN/SiO_2/PtFe structure with different thermal treatment conditions.

(a) Small devices of Ti/TiN/SiO_2/PtFe structure possess low power consumption properties.

(b) Electrical characteristics and parameters of small devices could understand more clearly the physical mechanism and current transport of resistance switching behaviors for Ti/TiN/SiO_2/PtFe structure.

Table 3.1. Average current of as deposition, RTA and FA sample at HRS (LRS).

Average current	As-deposit	RTA	FA
LRS (uA)	242.95	397.66	$3.47*10^3$
HRS (uA)	2.92	24.04	34.35

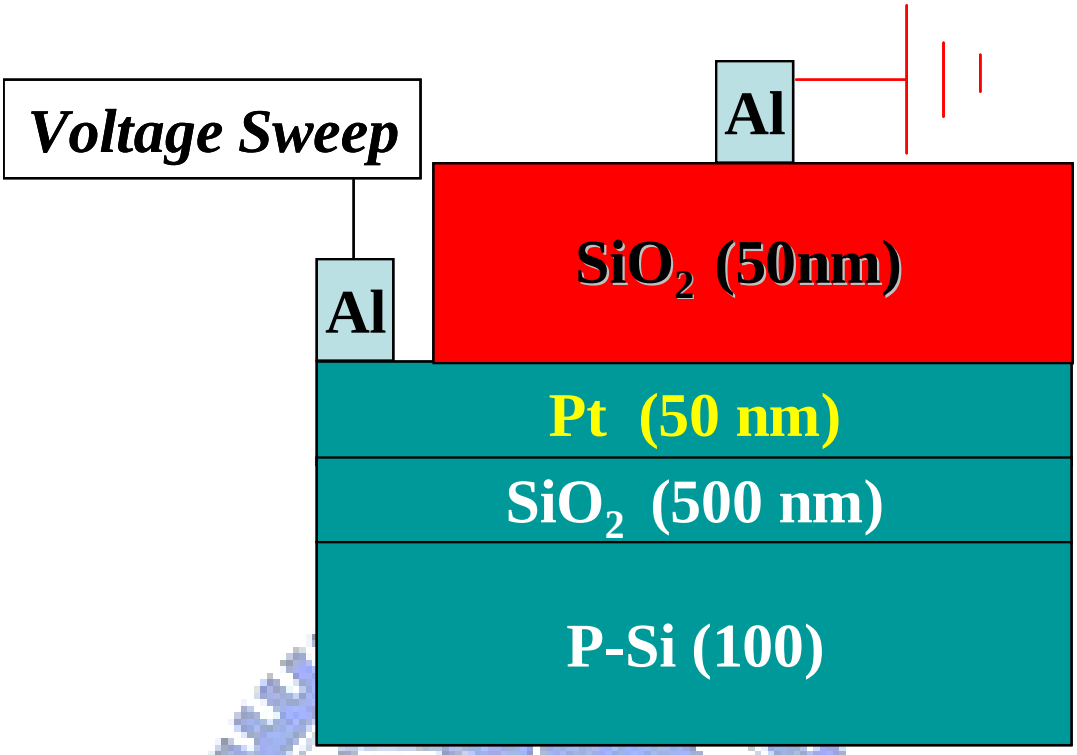


Figure 3.1. Schematic measurement setup diagram of Al/SiO_2/PtFe/SiO_2/Si structure.

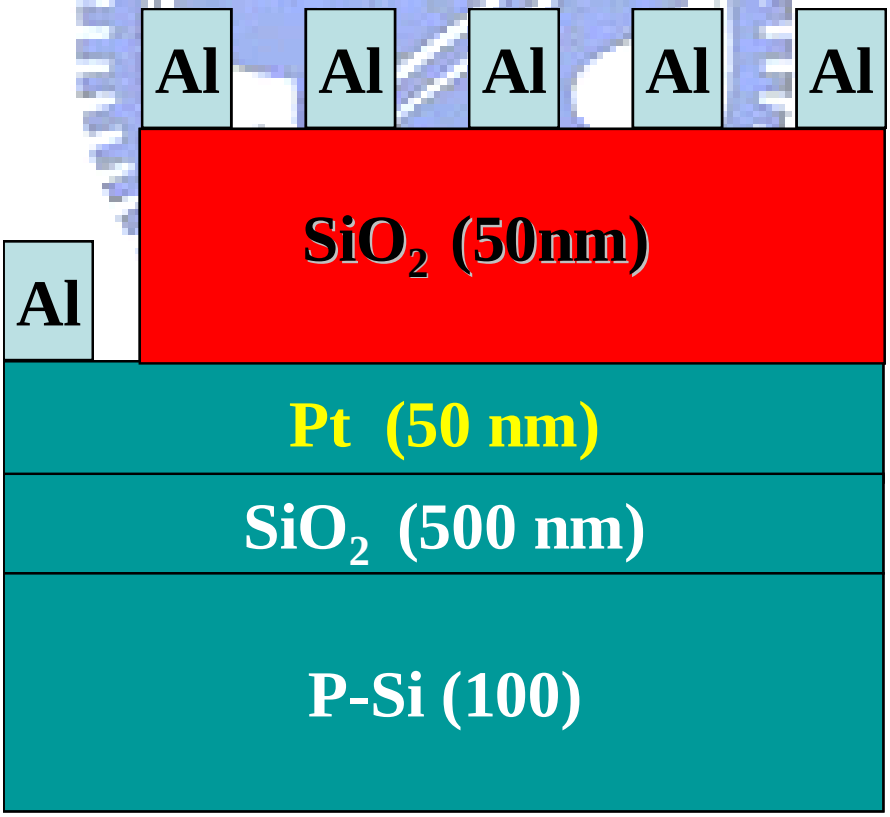


Figure 3.2. Schematic diagram of Al/SiO_2/Pt/SiO_2/Si structure.

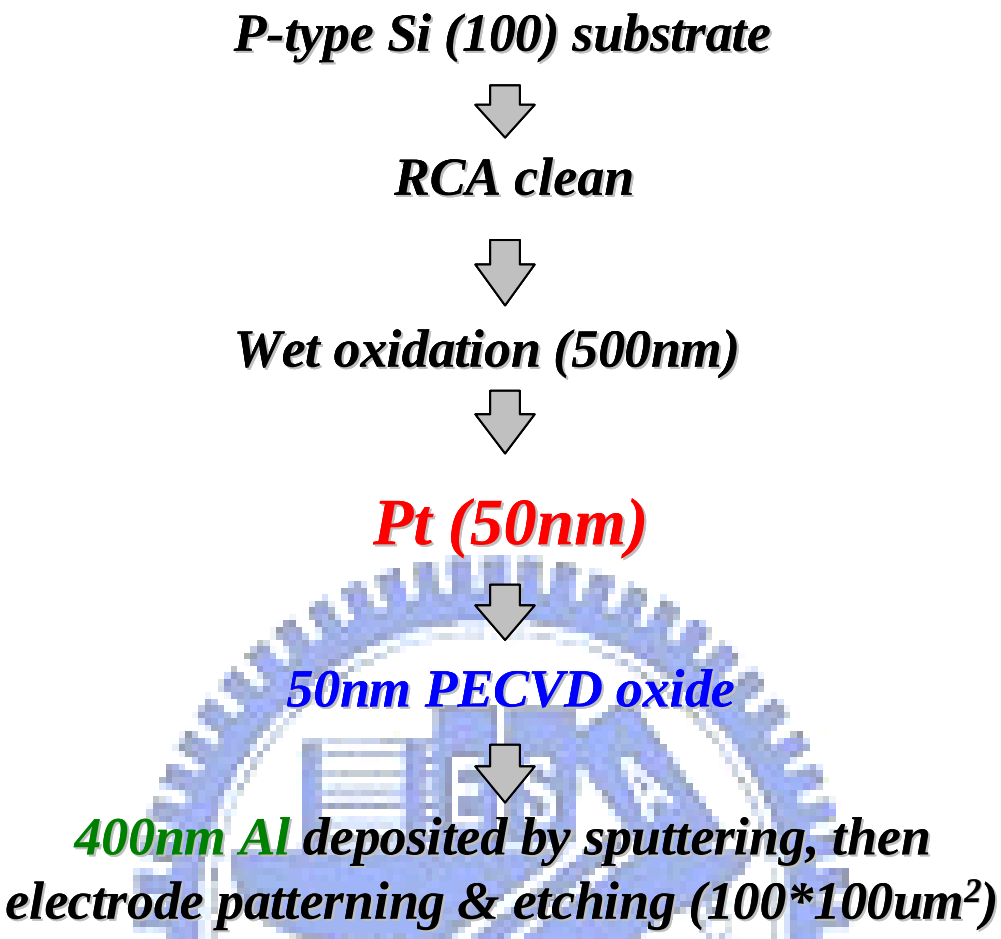


Figure 3.3. Process flows of Ti/TiN/SiO_2/Pt/SiO_2/Si structure.

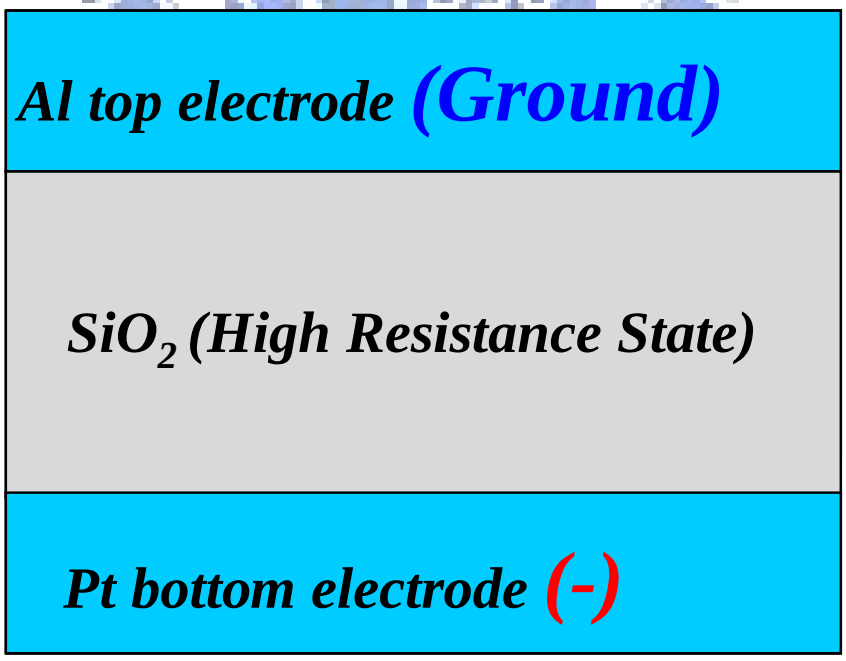


Figure 3.4. Initial state of Al/SiO_2/Pt/SiO_2/Si structure.

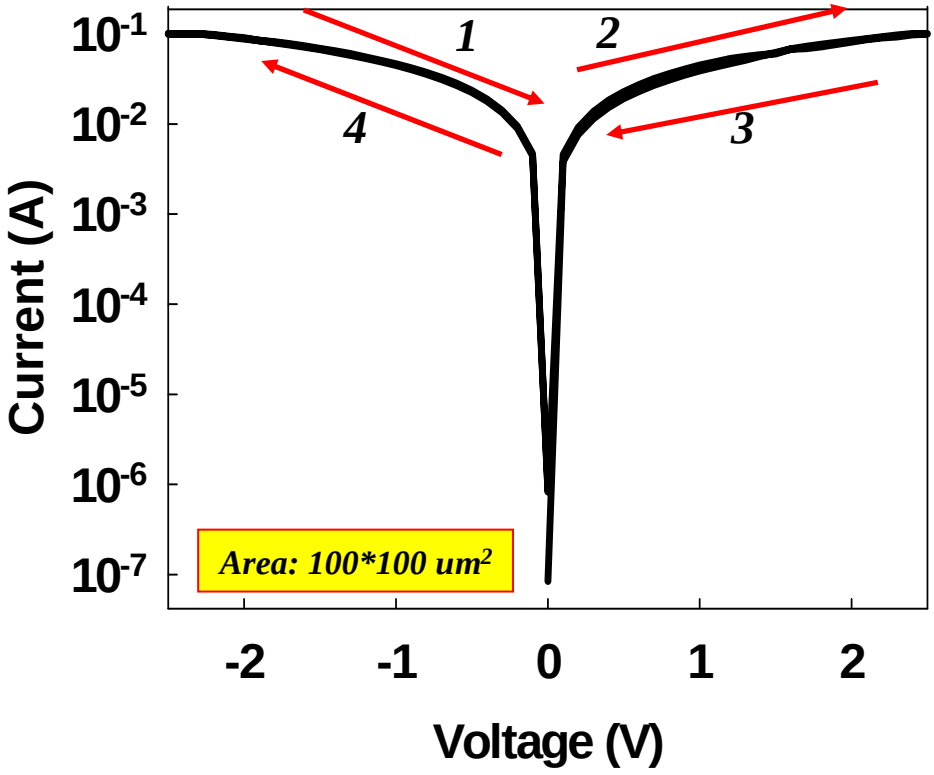


Figure 3.5. *I-V* characteristics of Al/SiO_2/Pt structure after forming.

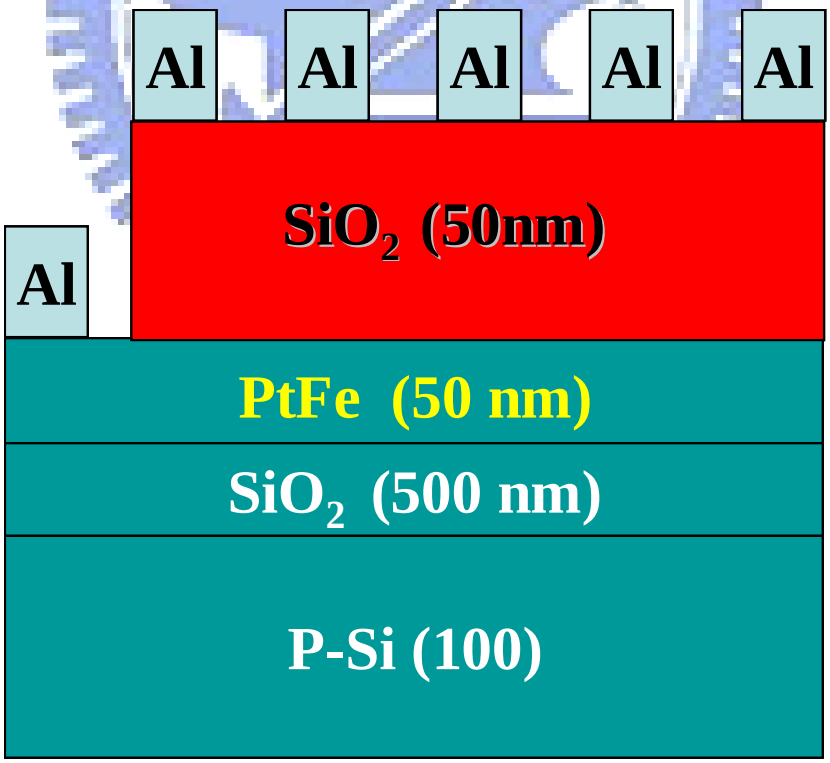


Figure 3.6. Schematic diagram of Al/SiO_2/PtFe/SiO_2/Si structure.

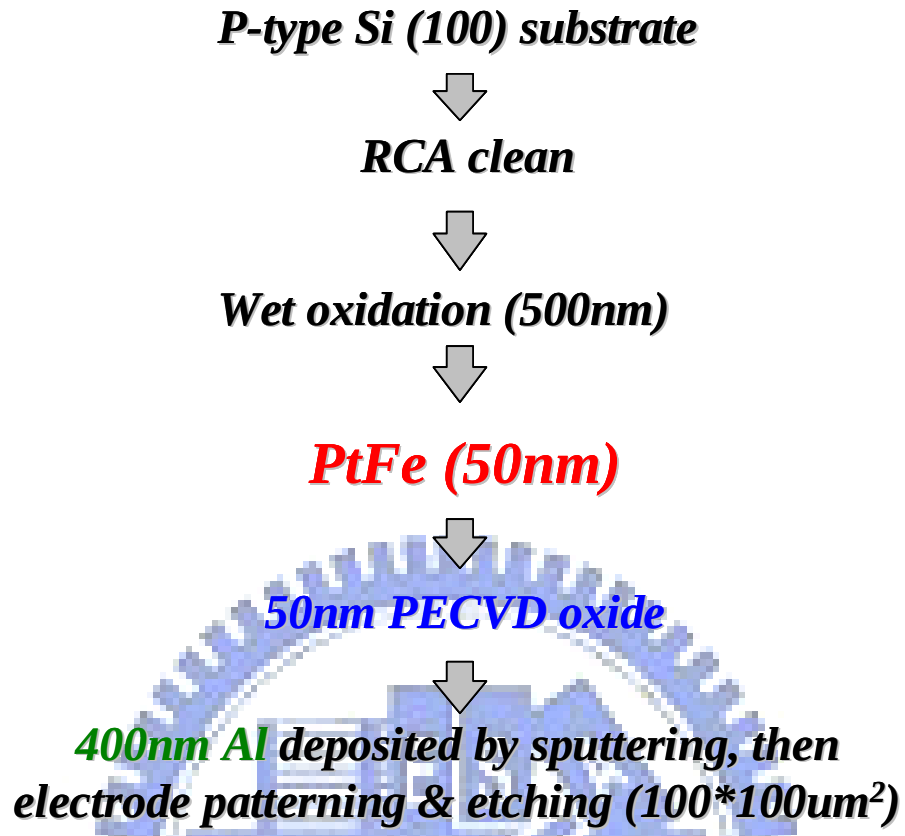


Figure 3.7. Process flows of Ti/TiN/SiO_2/PtFe/SiO_2/Si structure.

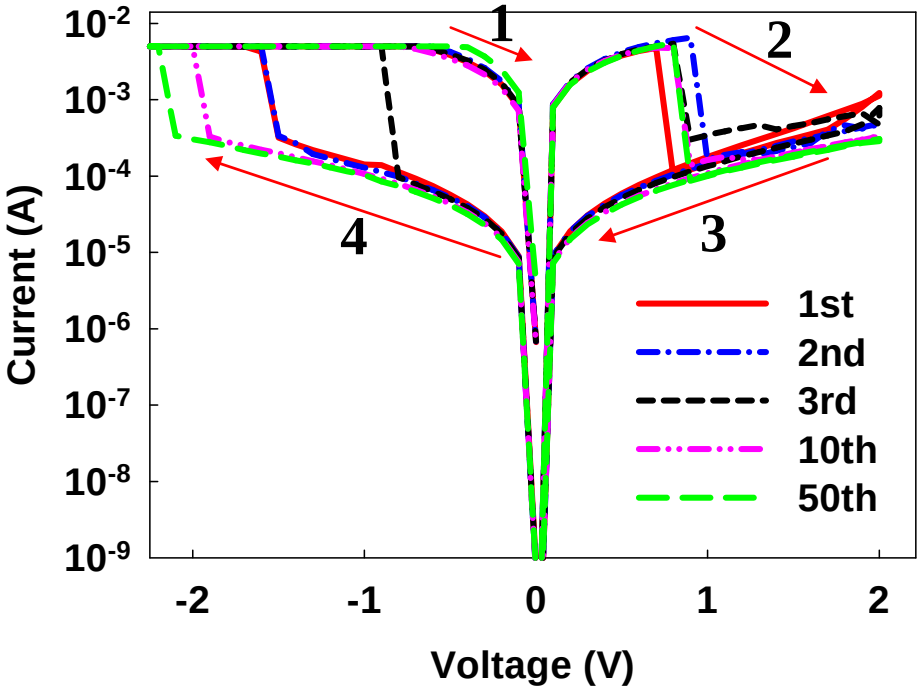


Figure 3.8. *I-V* characteristics of Ti/TiN/SiO_2/PtFe structure during set and reset processes.

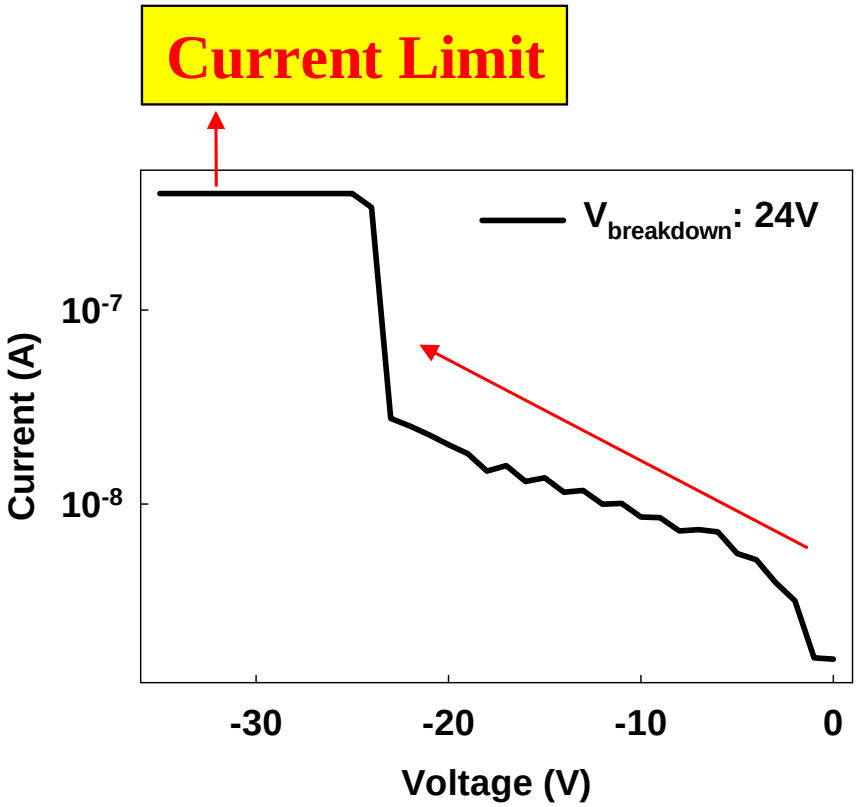


Figure 3.9. *I*–*V* characteristics during the forming process in the Al/SiO_2/Pt structure.

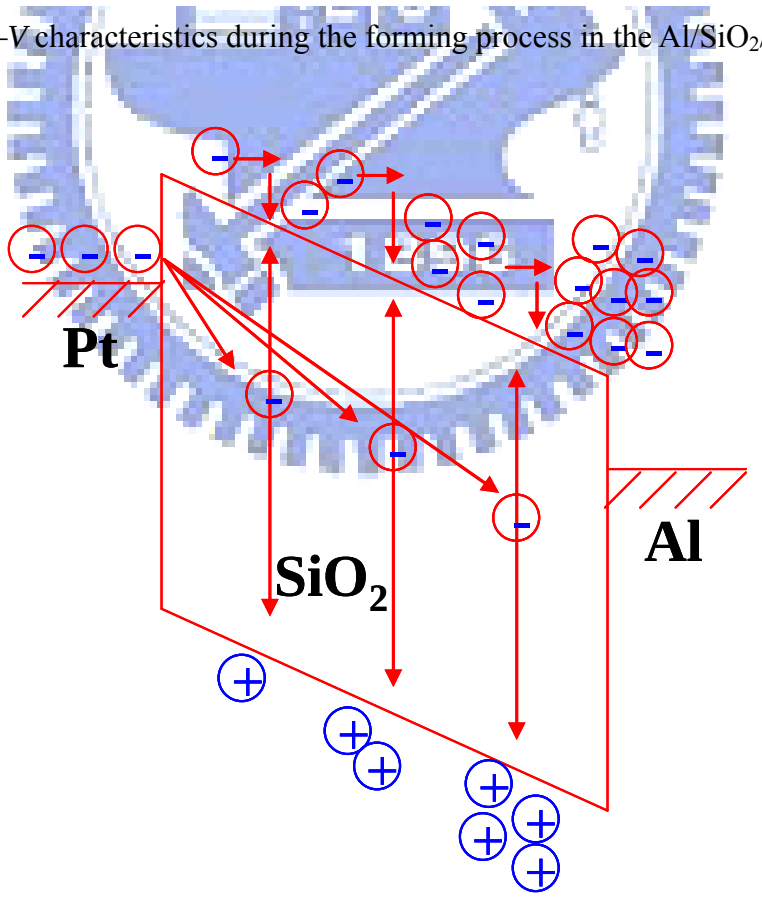


Figure 3.10. Impact ionization breakdown in the Al/SiO_2/Pt structure.

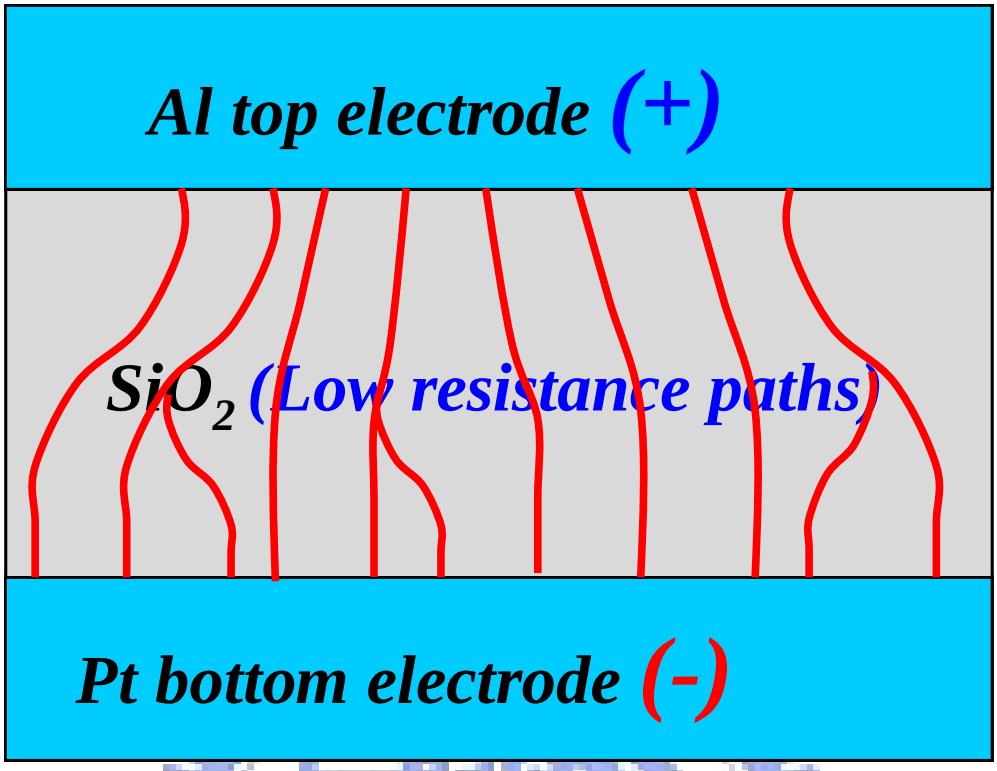


Figure 3.11. After forming process in Al/SiO_2/Pt/SiO_2/Si structure. There is some low resistance paths produced in SiO_2 insulating film.

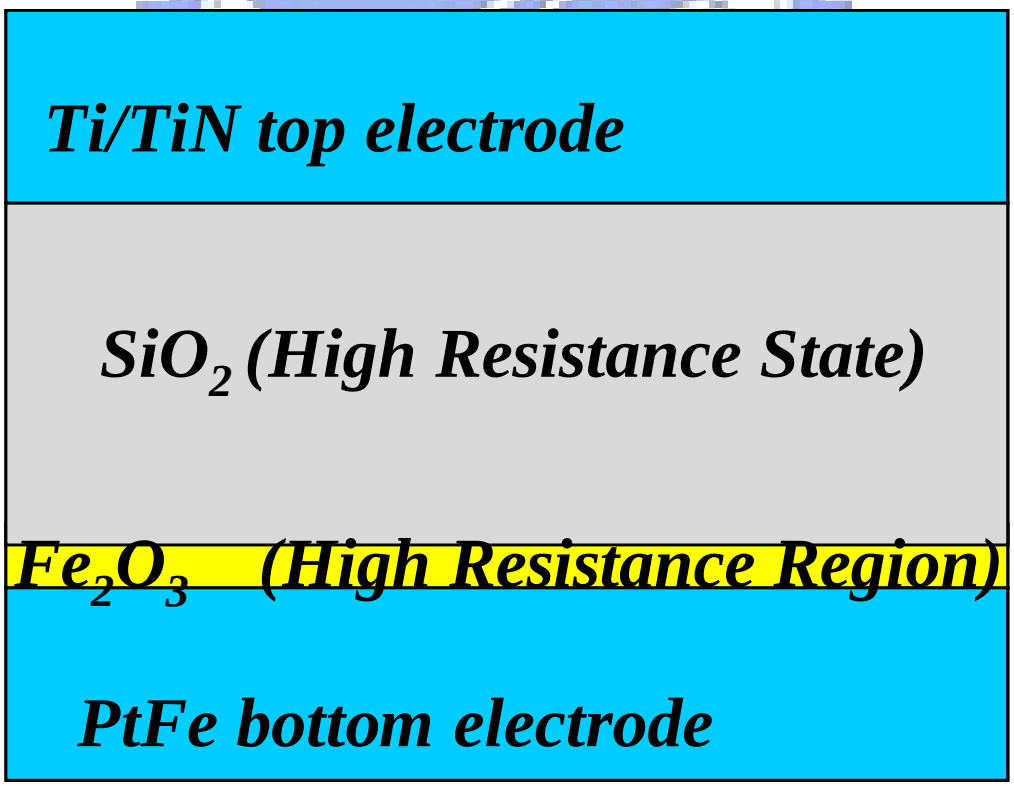


Figure 3.12. Initial state of Al/SiO_2/PtFe structure.

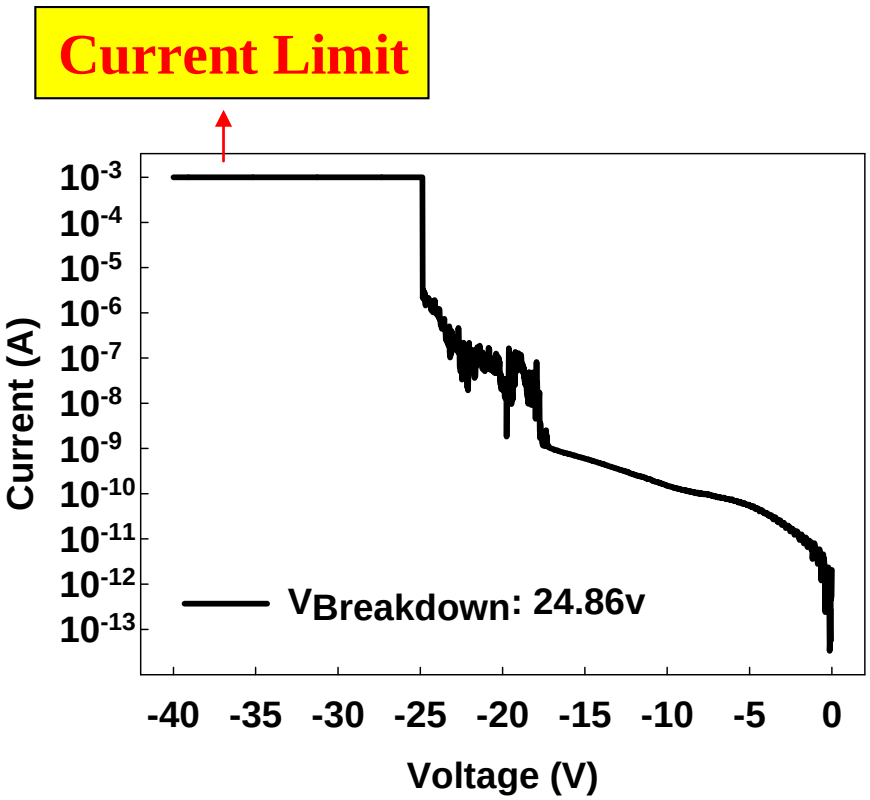


Figure 3.13. *I–V* characteristics during the forming process in the Al/SiO_2/PtFe structure.

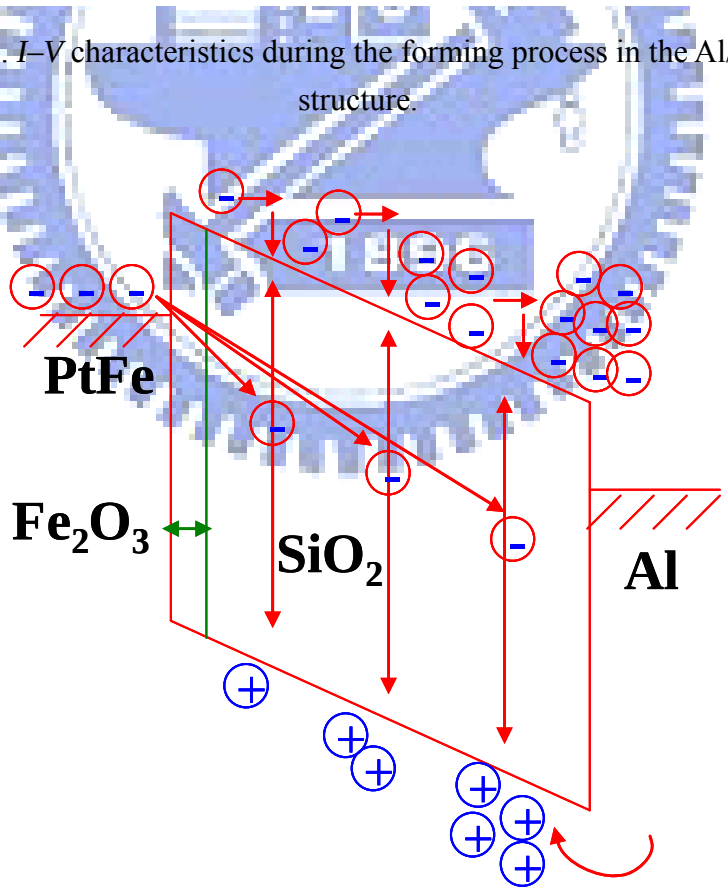


Figure 3.14. Impact ionization breakdown in Al/SiO_2/PtFe structure.

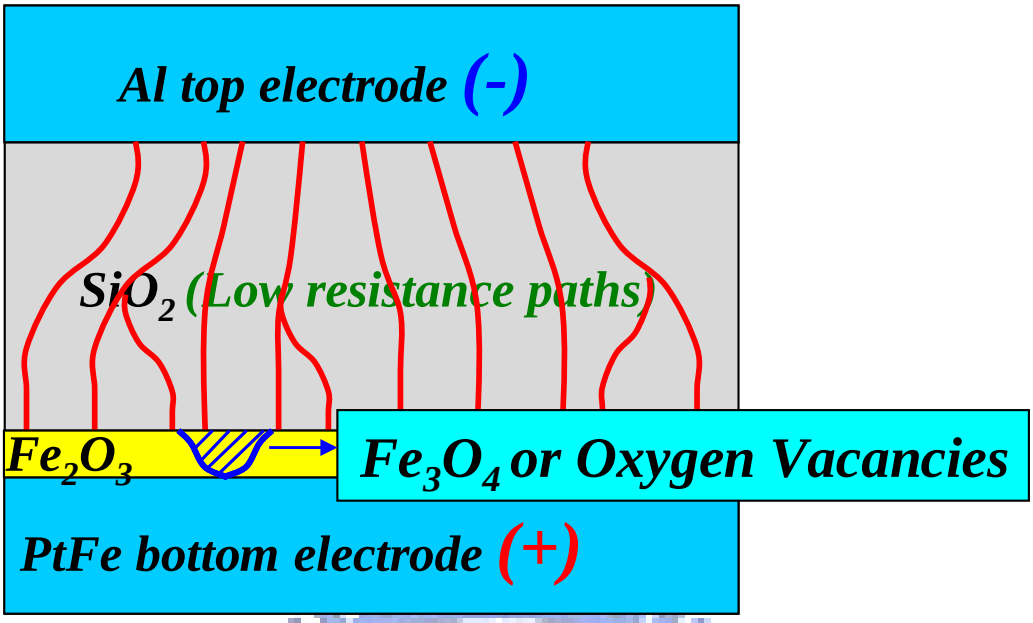
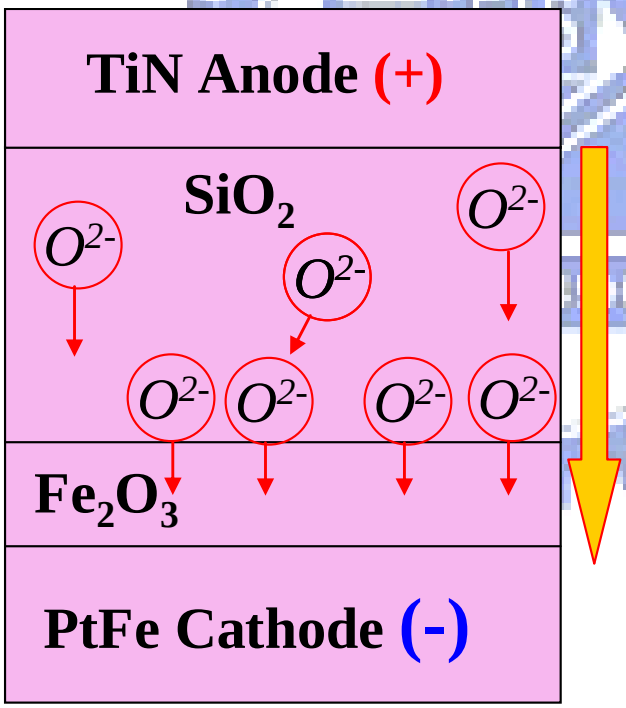


Figure 3.15. After forming process for Al/SiO_2/PtFe structure, there is some low resistance paths produced in SiO_2 and Fe_2O_3 insulating film.



$$\text{(a) } 2\,Fe_3O_4 + O^{--} \Rightarrow 3\,Fe_2O_3 + 2\,e^-$$

$$\text{(b) } O \xleftarrow{\text{Forward Bias}} V_{}^{''}\,(\text{donor}) + O^{2-}$$

Figure 3.16. During reset process for Al/SiO_2/PtFe structure, the oxygen ion would be attracted to the bottom electrode because of the electrical field.

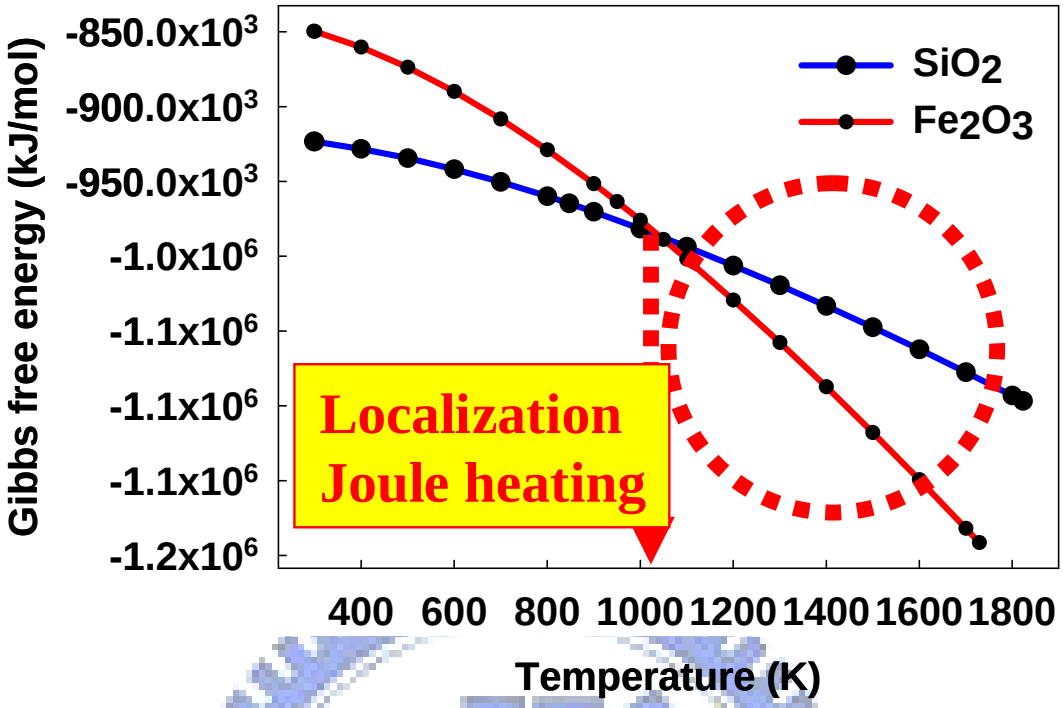


Figure 3.17. During reset process for Al/SiO_2/PtFe structure, the localization Joule heating up to 1000K would let Fe_2O_3 form.

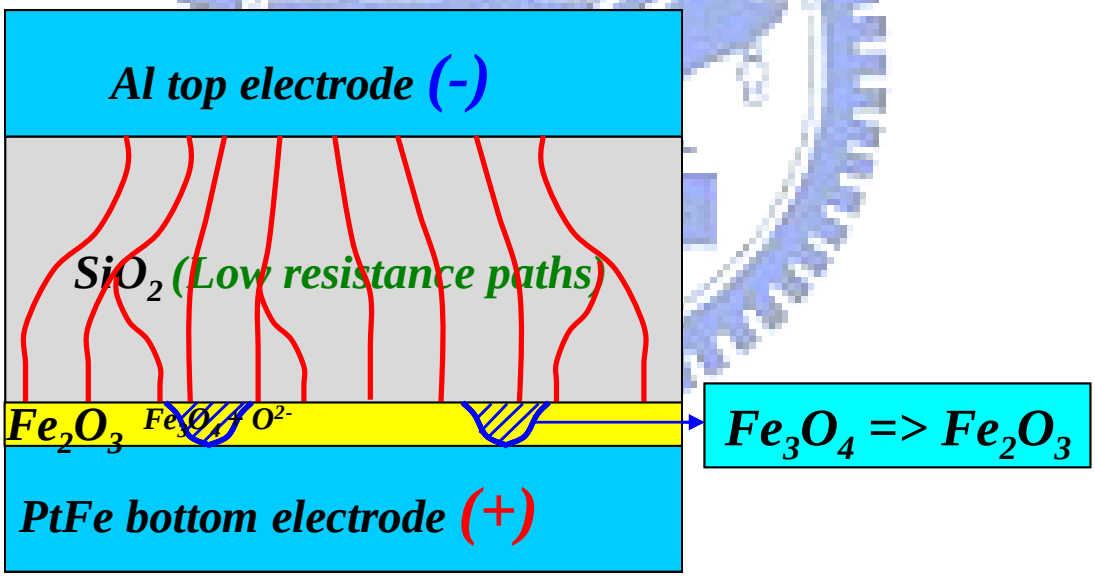


Figure 3.18. After reset process for Al/SiO_2/PtFe structure, the Fe_3O_4 would change phase to Fe_2O_3.

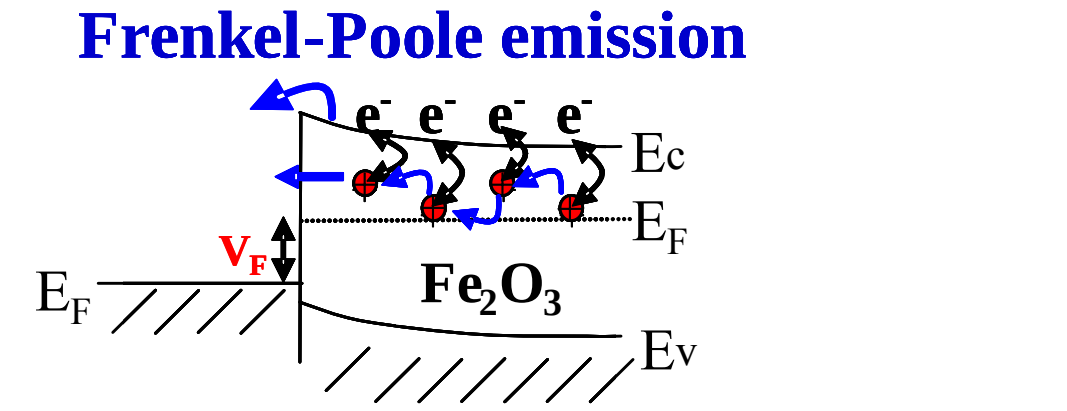


Figure 3.19. Band diagram of high resistance state for lighted n-type Fe_2O_3 semiconductor.

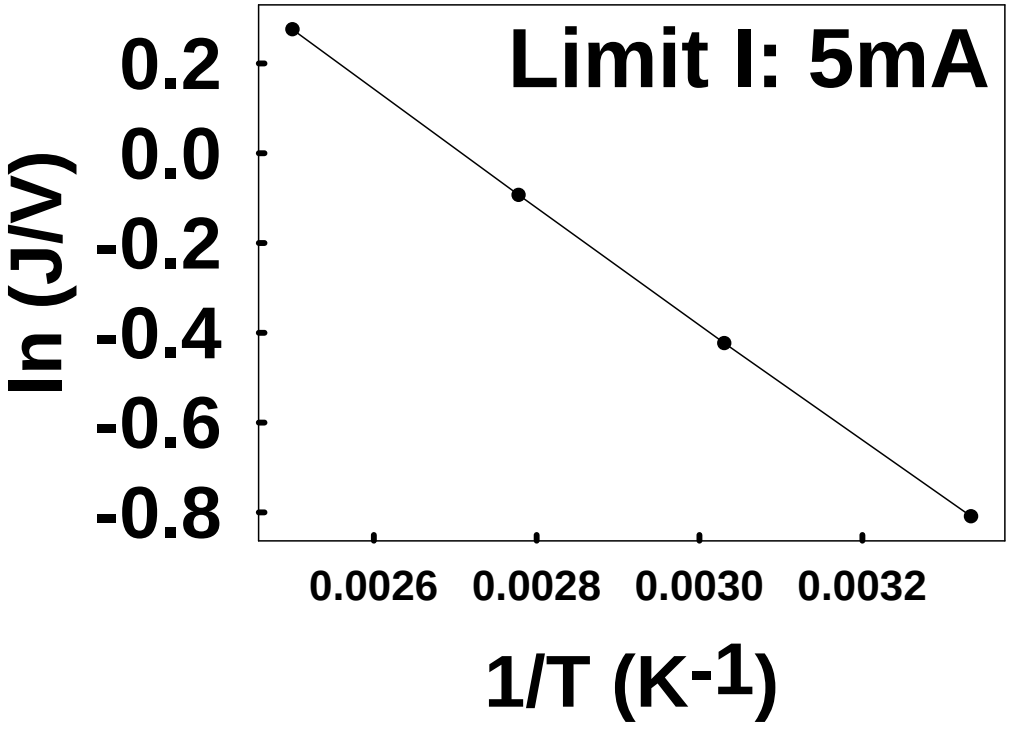


Figure 3.20. For Ti/TiN/SiO_2/PtFe structure, current fitting of Frenkel-Poole emission in the high bias region at HRS (section 3.4.4).

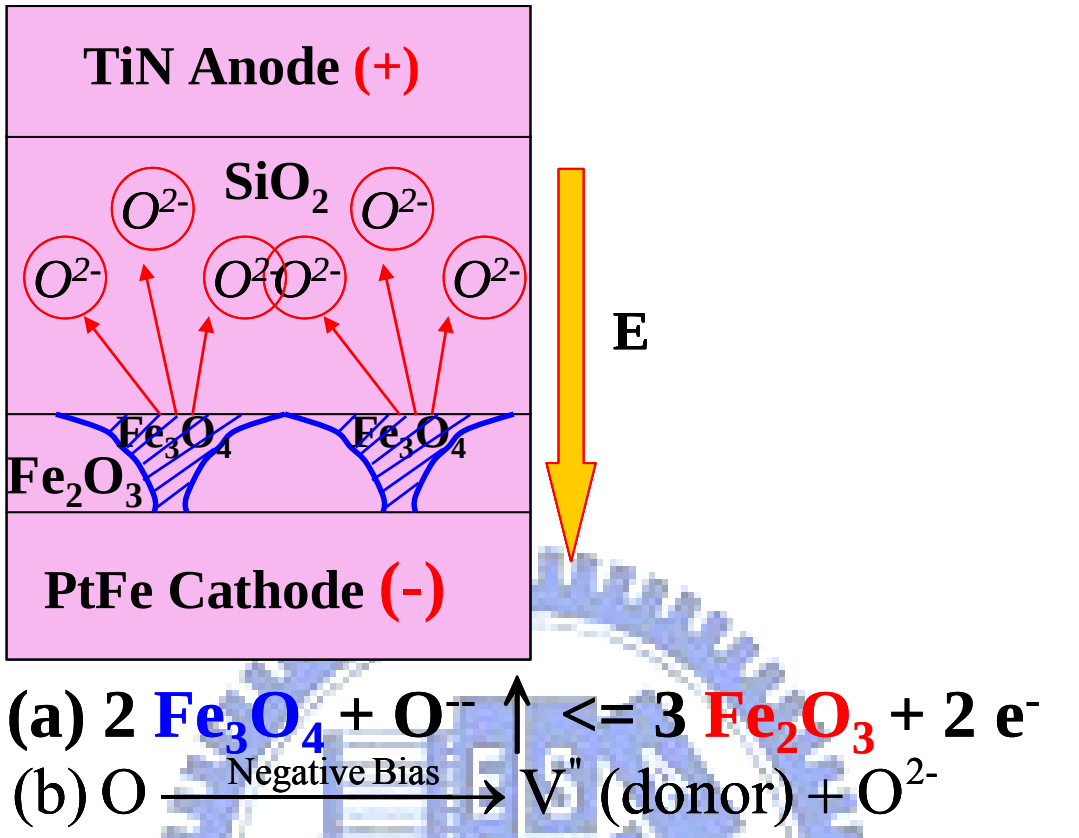


Figure 3.21. During set or forming process for Al/SiO_2/PtFe structure, the oxygen ion would be repelled to the bottom electrode because of the electrical field.

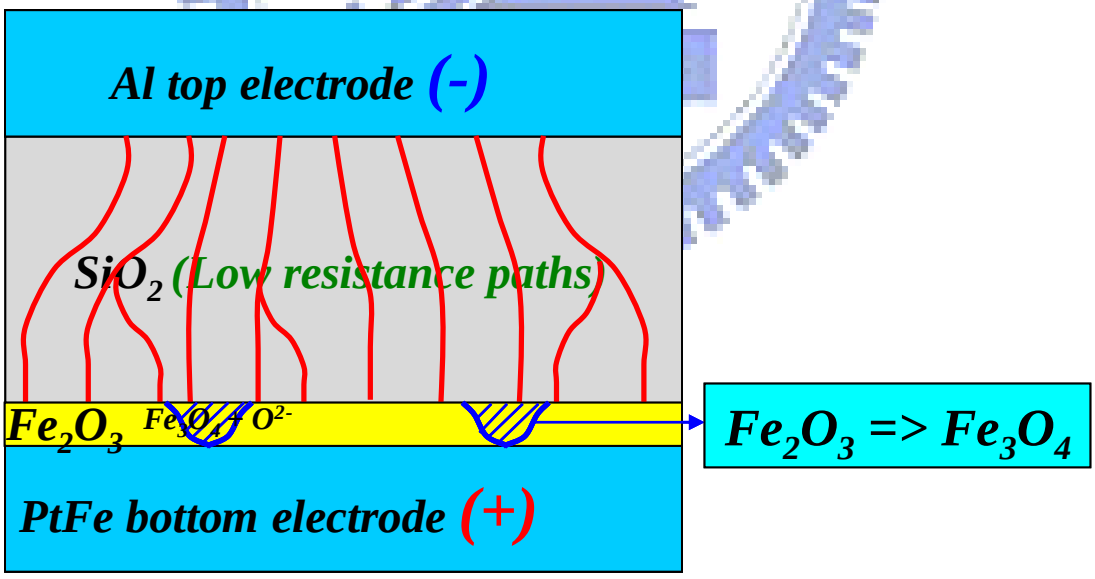


Figure 3.22. After set or forming process for Al/SiO_2/PtFe structure, the Fe_2O_3 would change phase to Fe_3O_4 at some electric faucet regions.

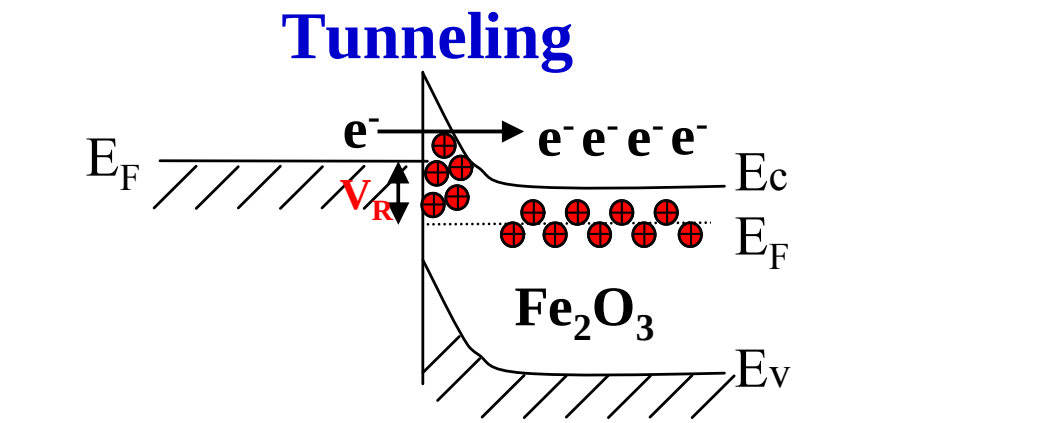


Figure 3.23. Band diagram of low resistance state for enhanced n-type Fe_2O_3 semiconductor.

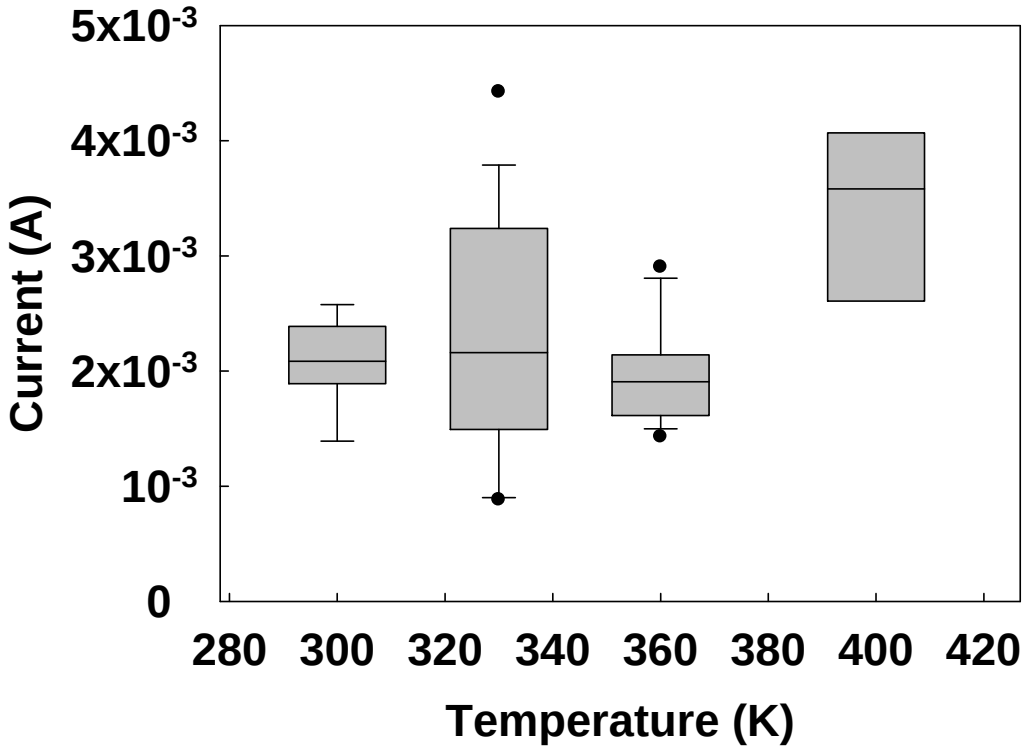


Figure 3.24. For Ti/TiN/SiO_2/PtFe structure, the relationship between tunneling current and different temperature at LRS (section 3.4.4).

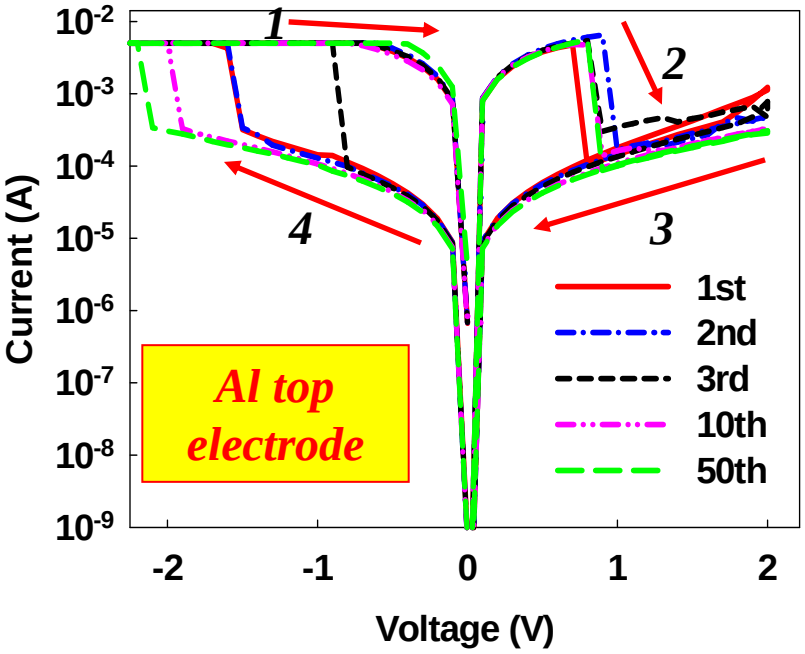


Figure 3.25 (a). *I-V* curve of Al/SiO_2/PtFe structure.

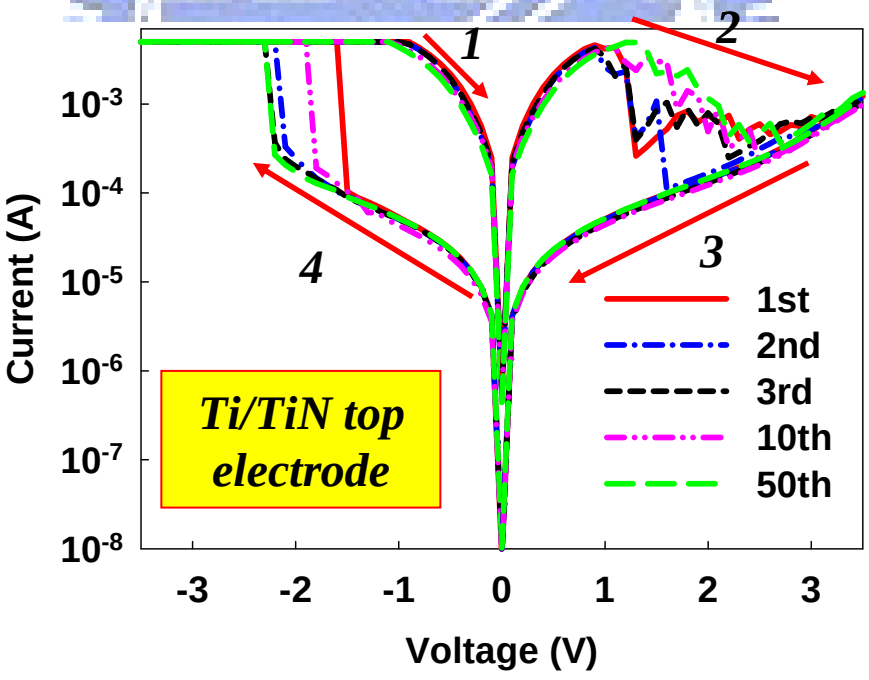


Figure 3.25 (b). *I-V* curve of Ti/TiN/SiO_2/PtFe structure.

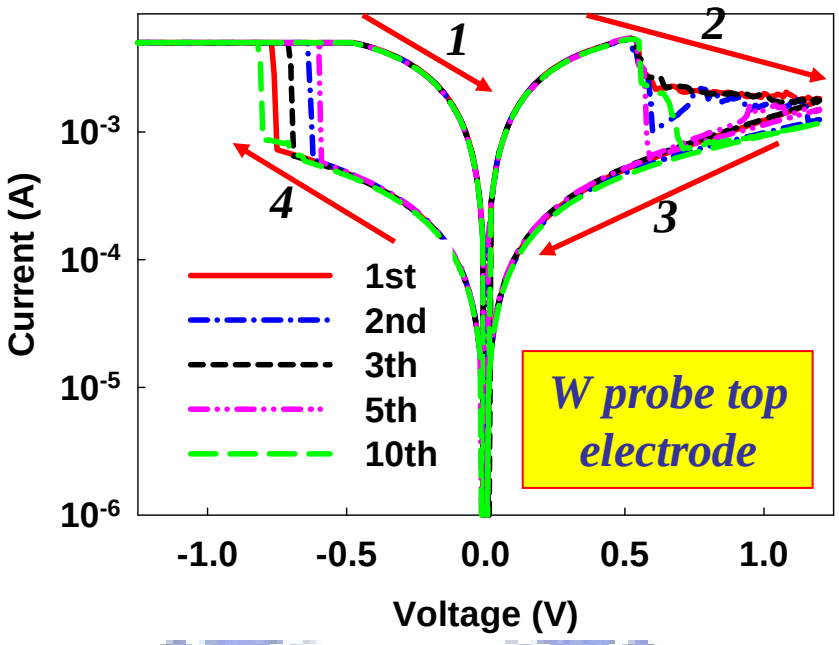


Figure 3.25 (c). *I-V* curve of W probe/SiO_2/PtFe structure.

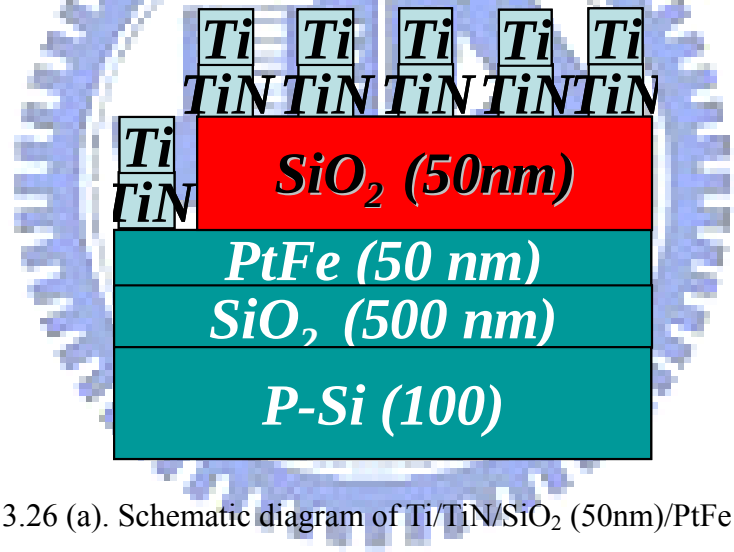


Figure 3.26 (a). Schematic diagram of Ti/TiN/SiO_2 (50nm)/PtFe structure.

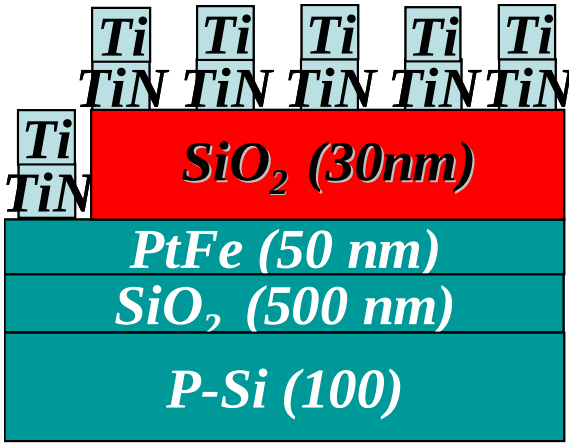


Figure 3.26 (b). Schematic diagram of Ti/TiN/SiO_2 (30nm)/PtFe structure.

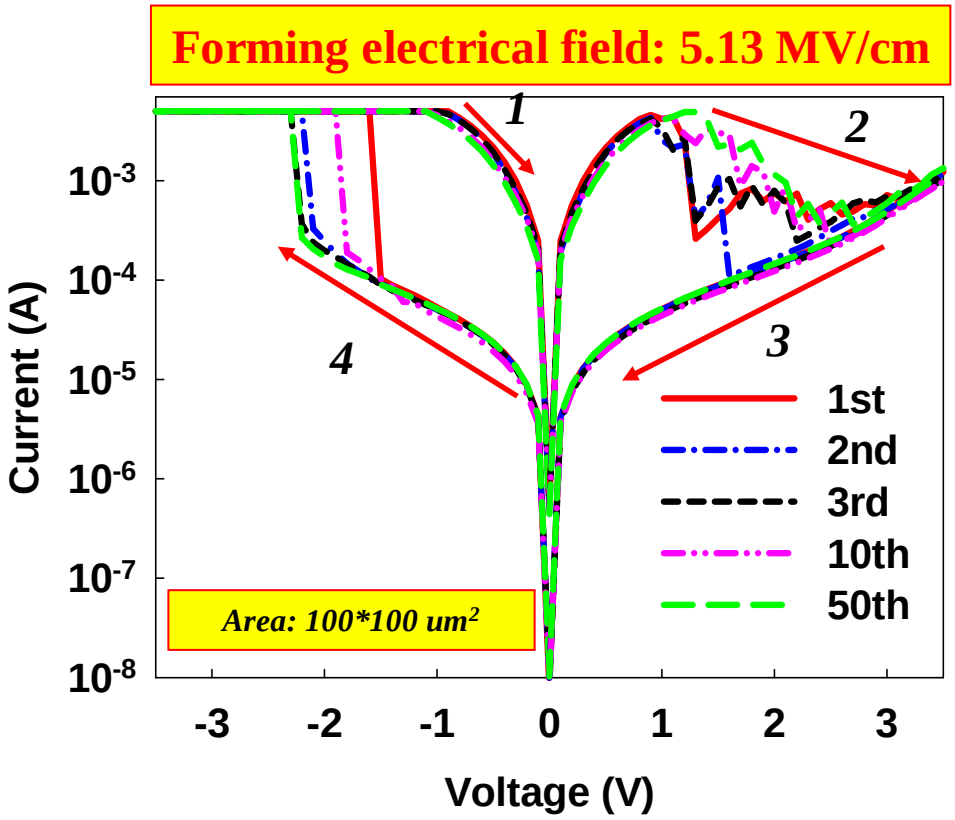


Figure 3.27 (a). *I-V* curve of Ti/TiN/SiO_2 (50nm)/PtFe/SiO_2/Si structure.

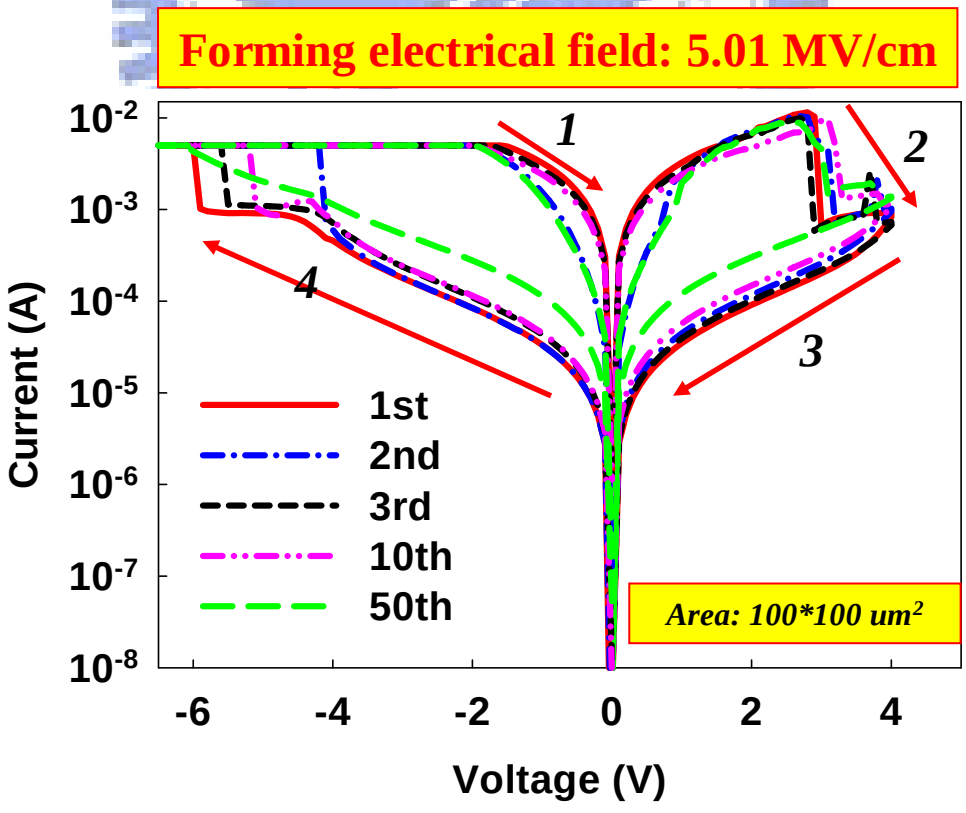


Figure 3.27 (b). *I-V* curve of Ti/TiN/SiO_2 (30nm)/PtFe/SiO_2/Si structure.

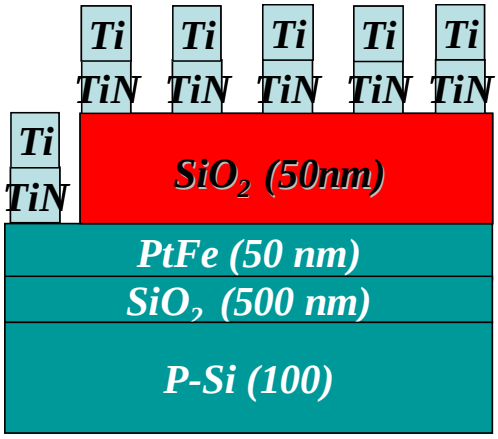


Figure 3.28 (a). Schematic diagram of Ti/TiN/SiO_2/PtFe structure.

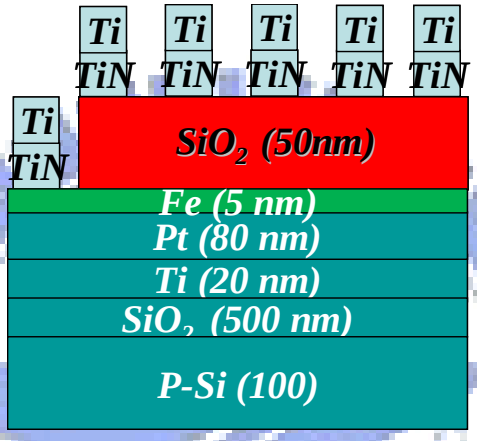


Figure 3.28 (b). Schematic diagram of Ti/TiN/SiO_2/Fe/Pt/Ti structure.

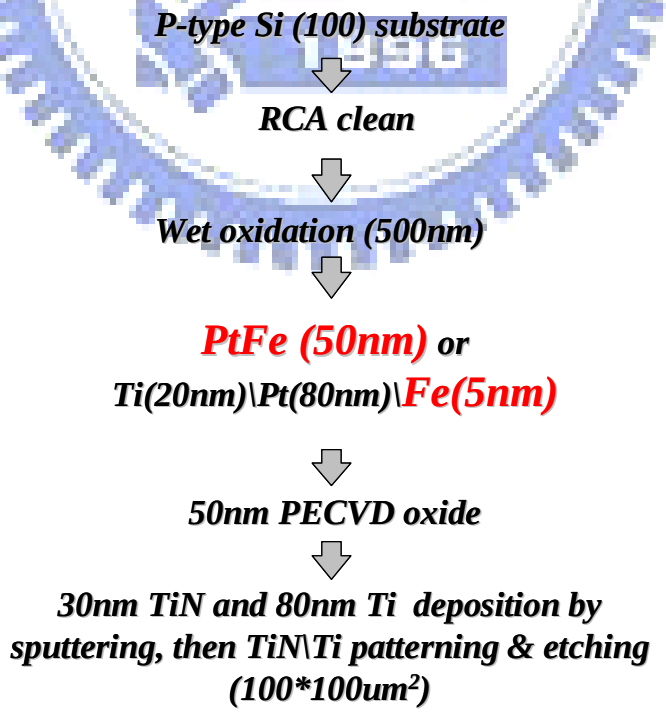


Figure 3.28 (c). Process flows of Ti/TiN/SiO_2/PtFe and Ti/TiN/SiO_2/Fe/Pt/Ti structures.

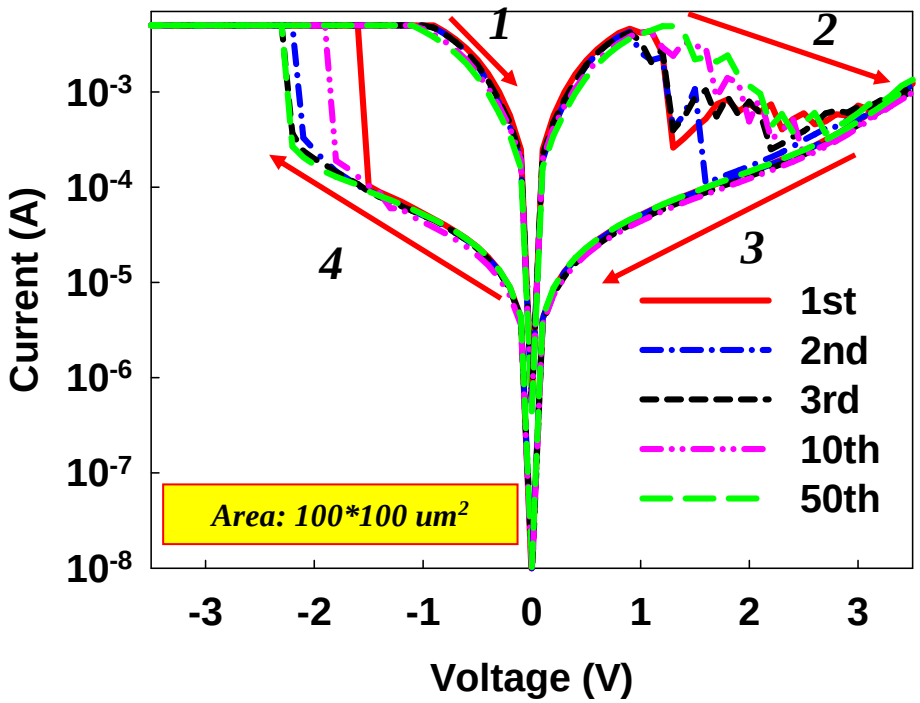


Figure 3.29 (a). *I-V* curve of Ti/TiN/SiO_2/PtFe structure.

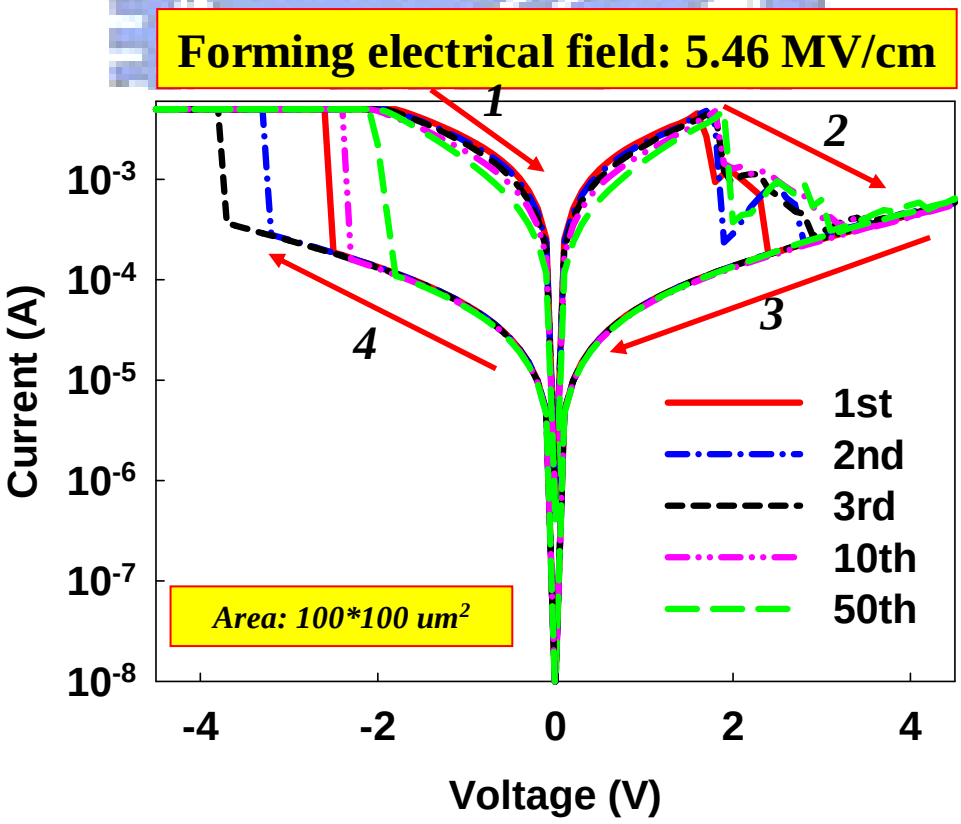


Figure 3.29 (b). *I-V* curve of Ti/TiN/SiO_2/Fe/Pt/Ti structure.

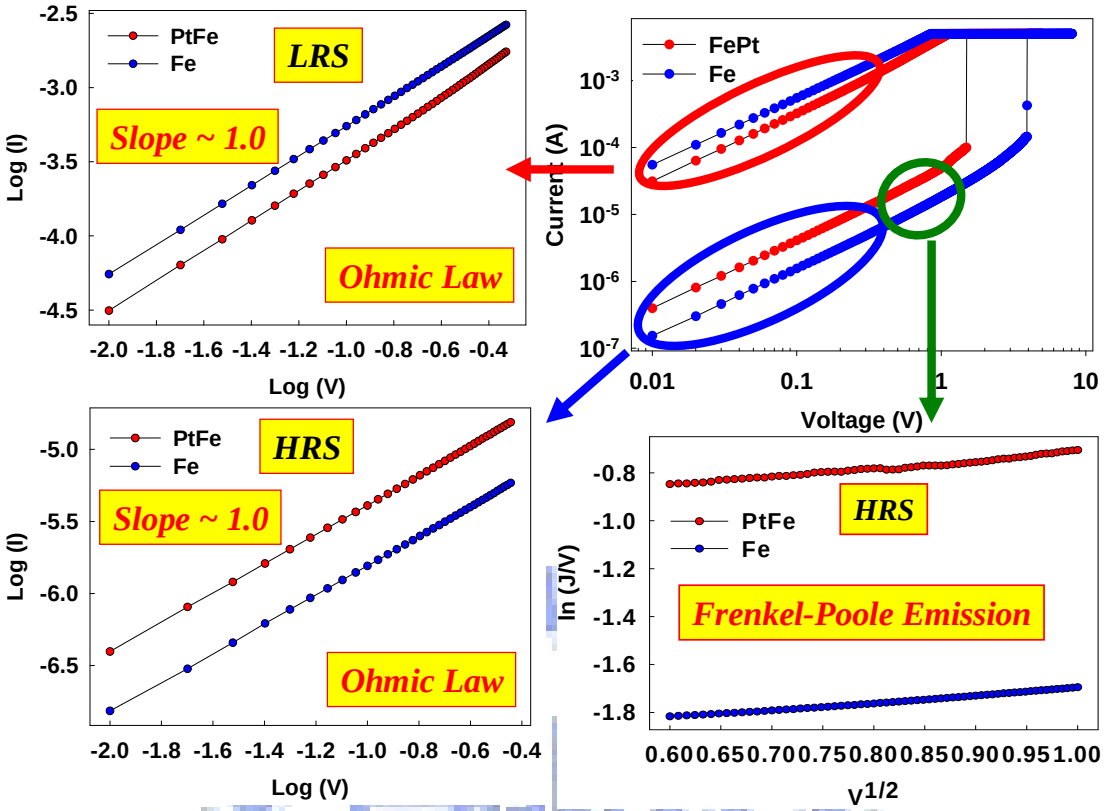


Figure 3.30. For PtFe and Fe bottom electrode structure, current fitting results of LRS (upper left), small bias region at HRS (lower left), and high bias region at HRS (lower right).

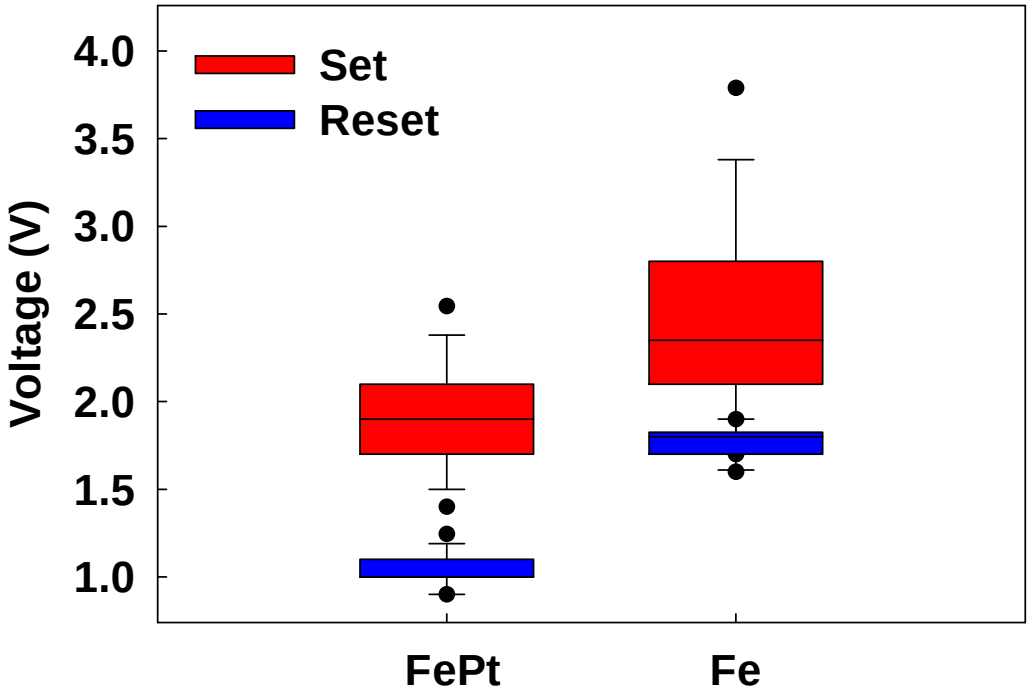


Figure 3.31 (a). Statistics plot of the relationship between set (reset) voltage and different bottom electrode structures.

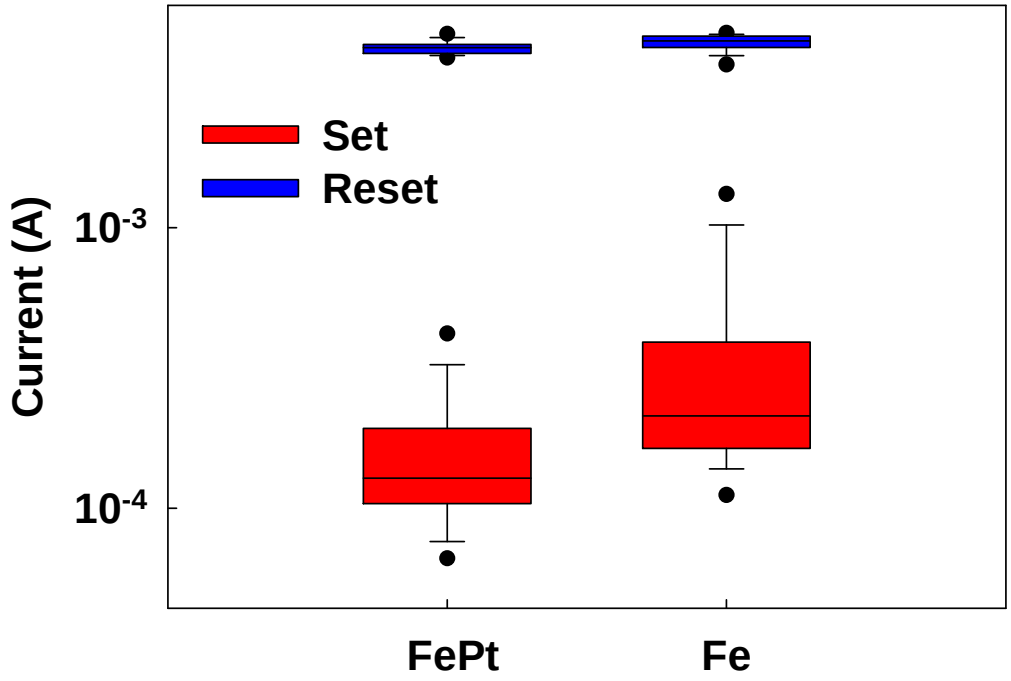


Figure 3.31 (b). Statistics plot of the relationship between set (reset) current and different bottom electrode structures.

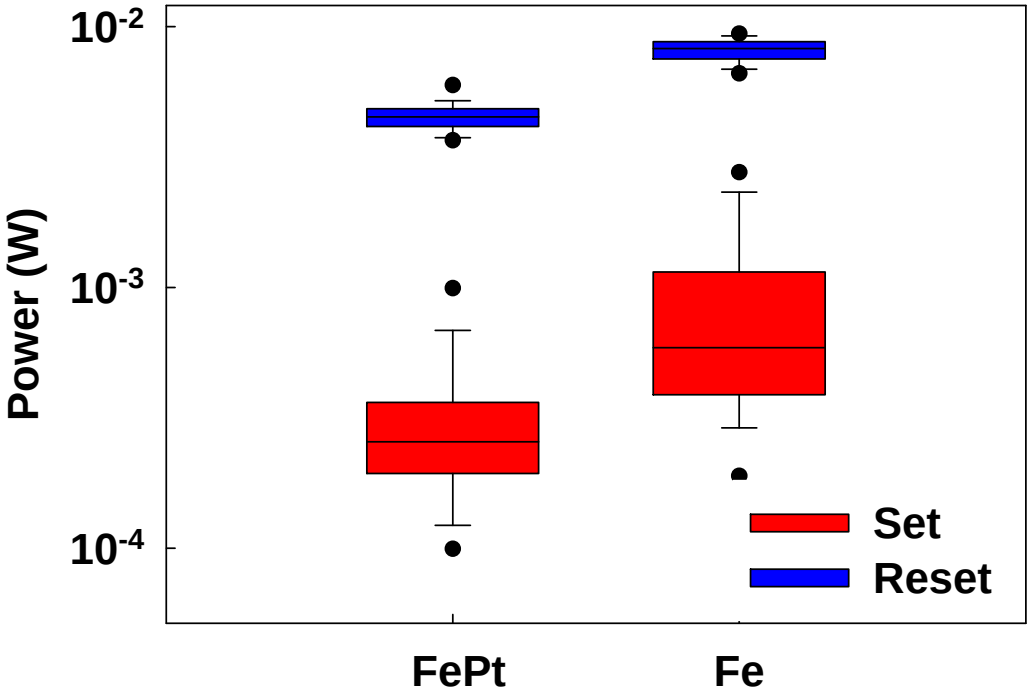


Figure 3.31 (c). Statistics plot of the relationship between set (reset) power and different bottom electrode structures.

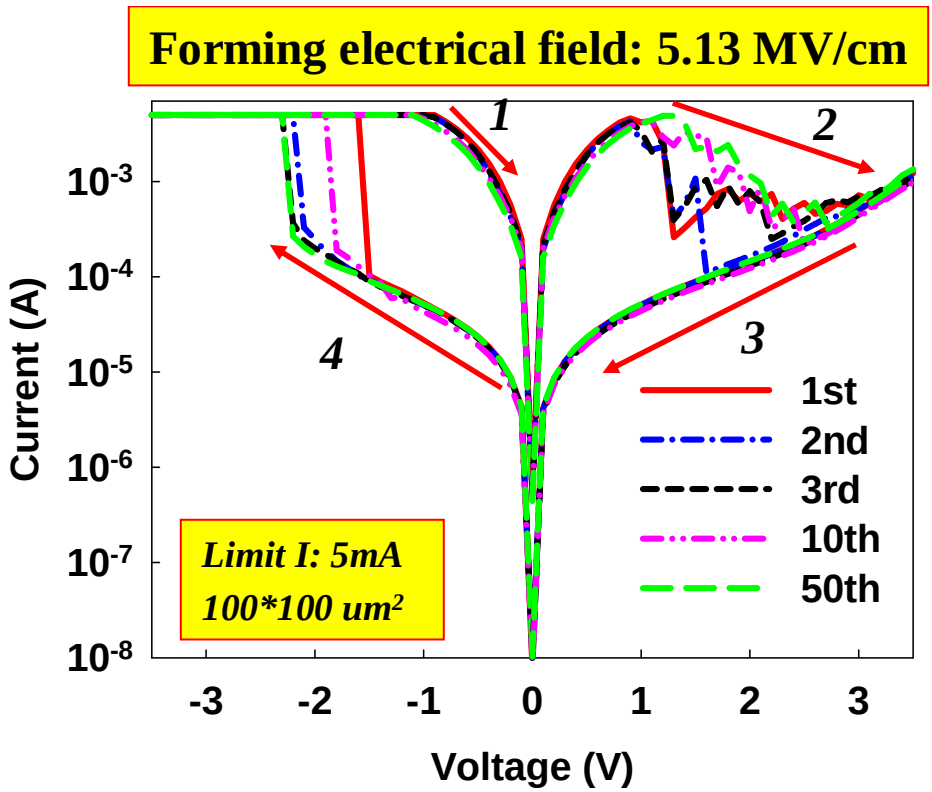


Figure 3.32 (a). *I-V* curve of Ti/TiN/SiO_2/PtFe structure (As deposition).

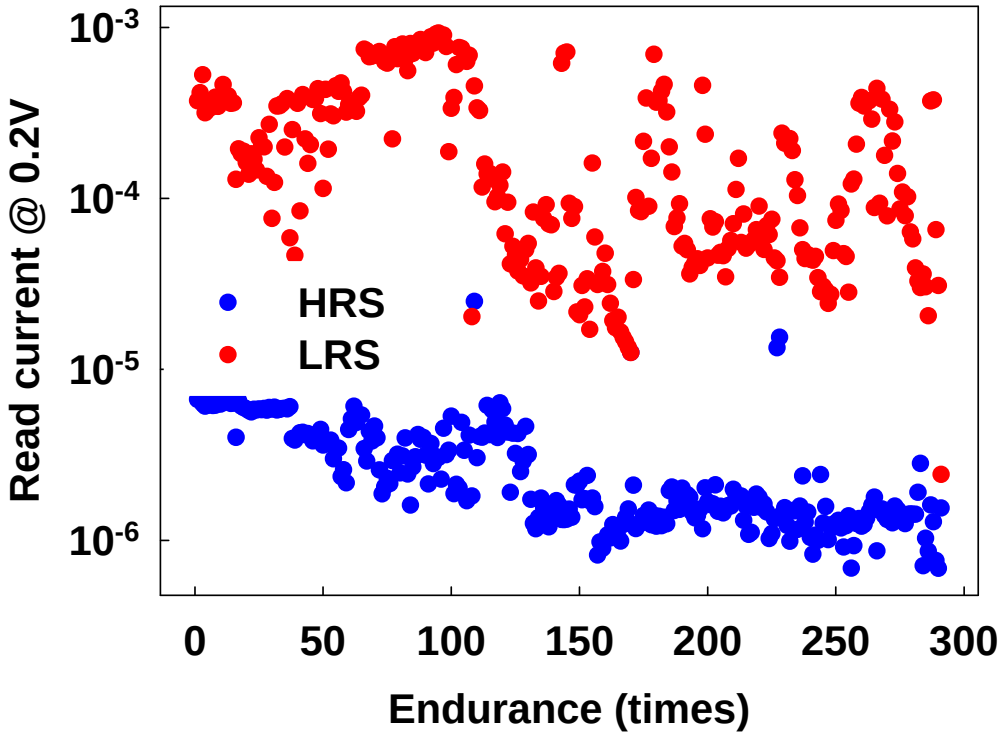


Figure 3.32 (b). Endurance of the Ti/TiN/SiO_2/PtFe structure about 300 times (As deposition).

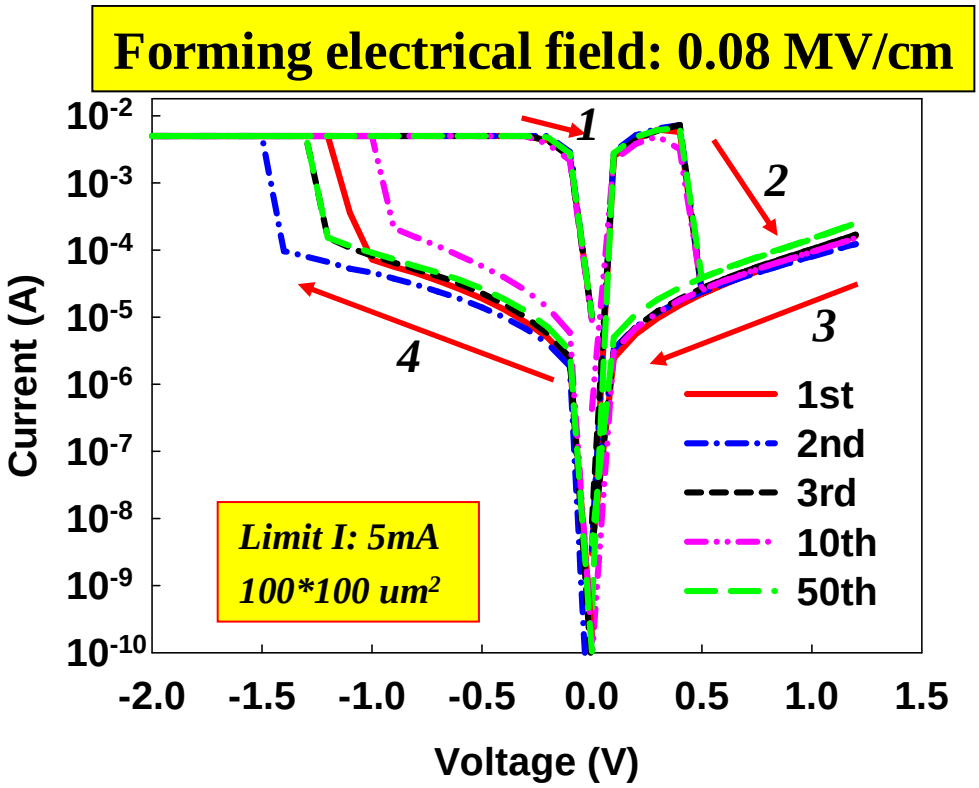


Figure 3.33 (a). *I-V* curve of Ti/TiN/SiO_2/PtFe structure (Furnace annealing 600°C, 30min in vacuum).

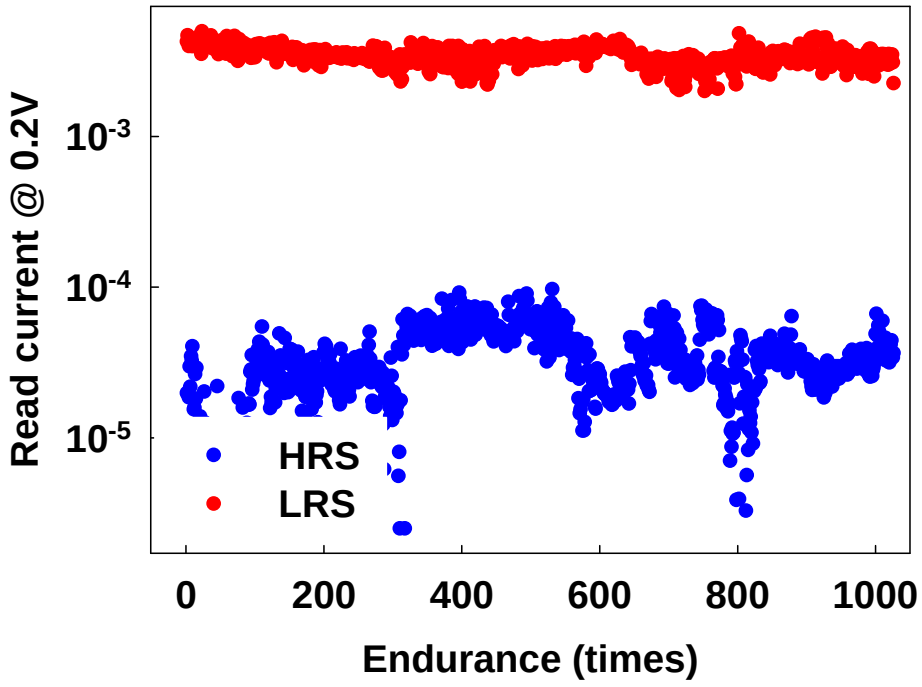


Figure 3.33 (b). Endurance of the Ti/TiN/SiO_2/PtFe structure over 1000 times (furnace annealing 600°C, 30min in vacuum).

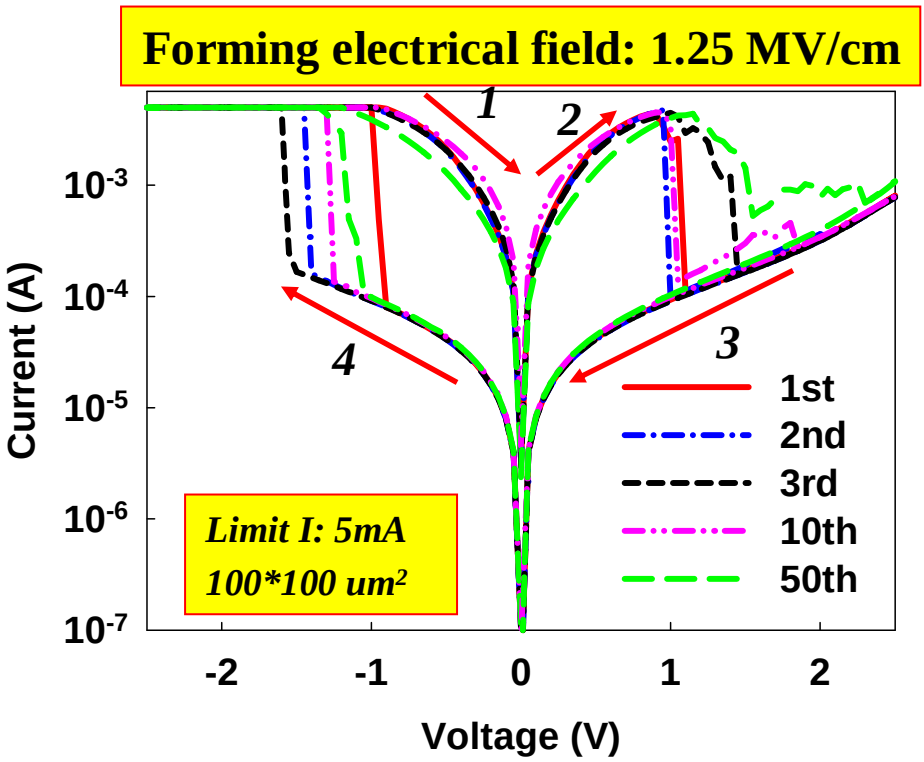


Figure 3.34 (a). *I-V* curve of Ti/TiN/SiO_2/PtFe structure (Rapid thermal annealing 600°C 60s, atmospheric pressure in N_2 or air condition).

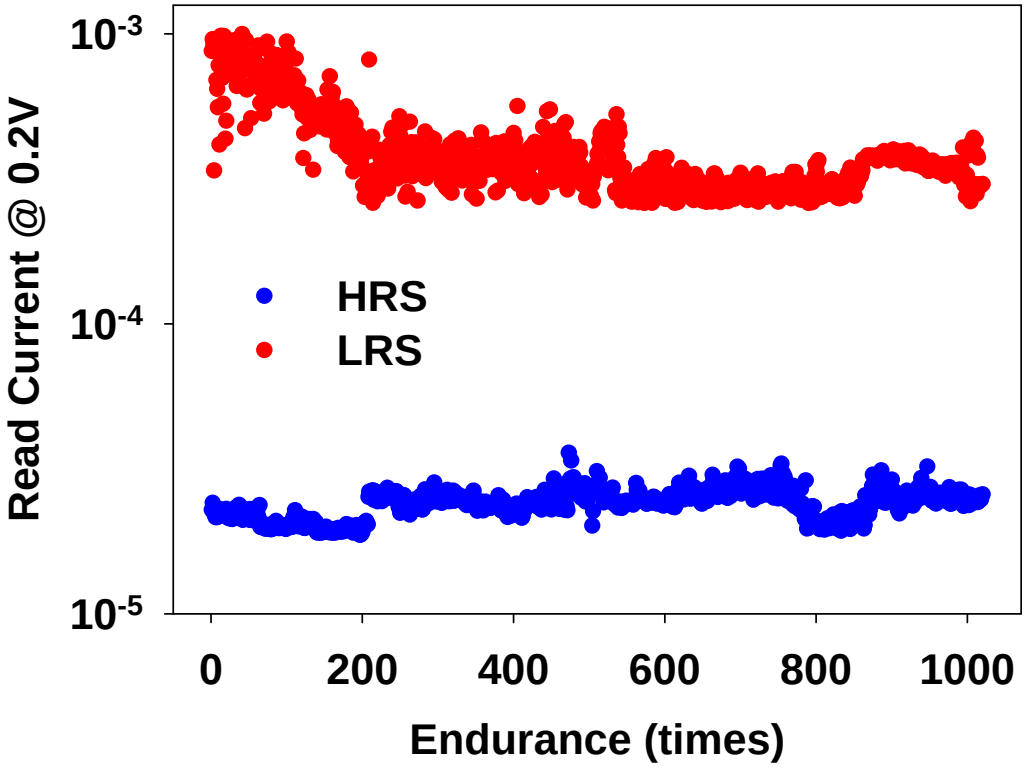


Figure 3.34 (b). Endurance of the Ti/TiN/SiO_2/PtFe structure over 1000 times (Rapid thermal annealing 600°C 60s, atmospheric pressure in N_2 or air condition).

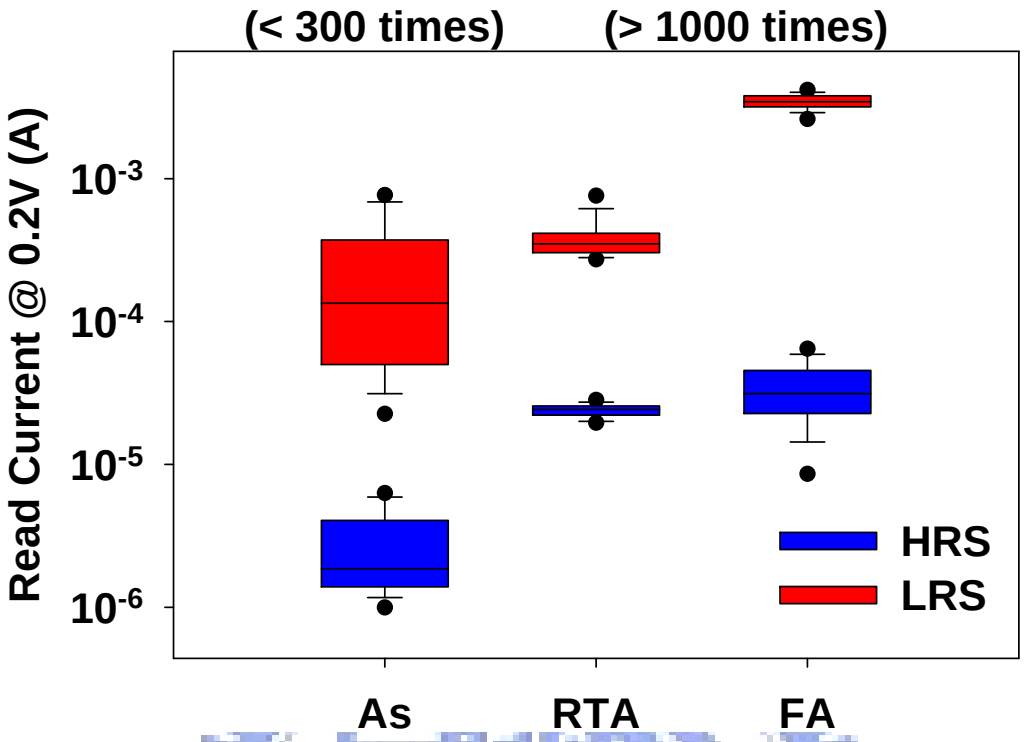


Figure 3.35. Statistics plot of the relationship between HRS (LRS) reading current at 0.2V and different thermal treatment conditions.

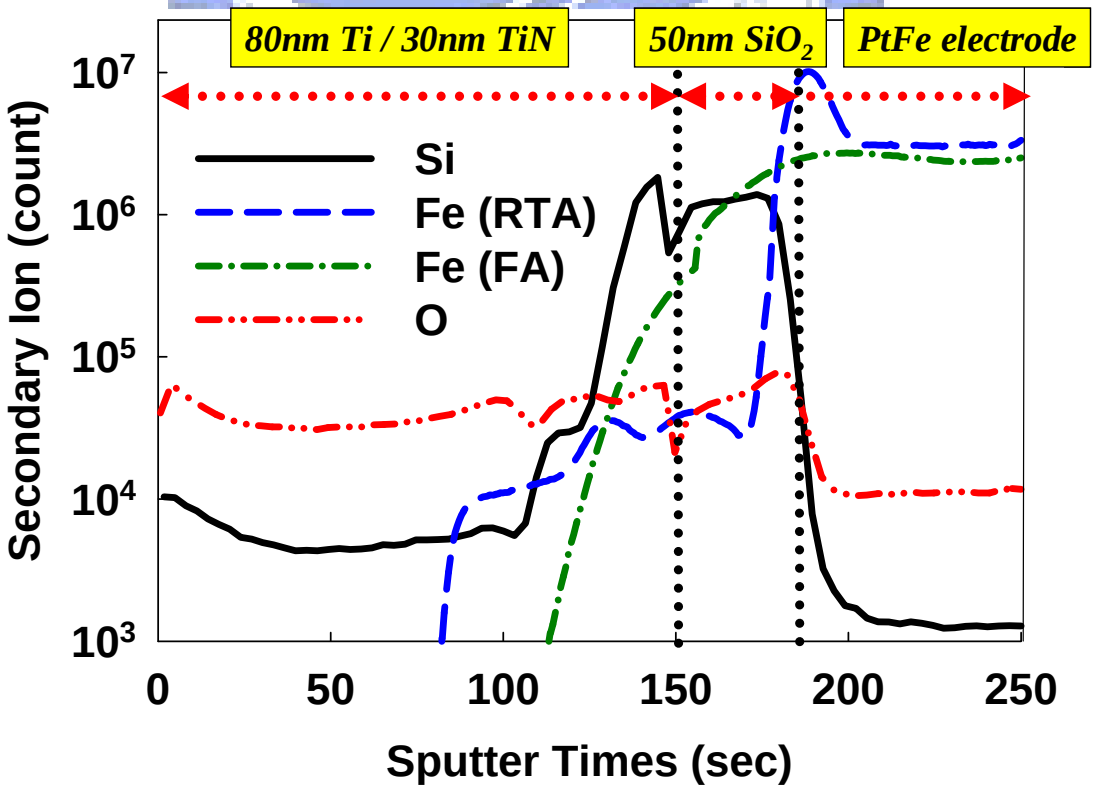


Figure 3.36. SIMS results of Ti/TiN/SiO_2/PtFe structure during RTA or FA thermal treatment.

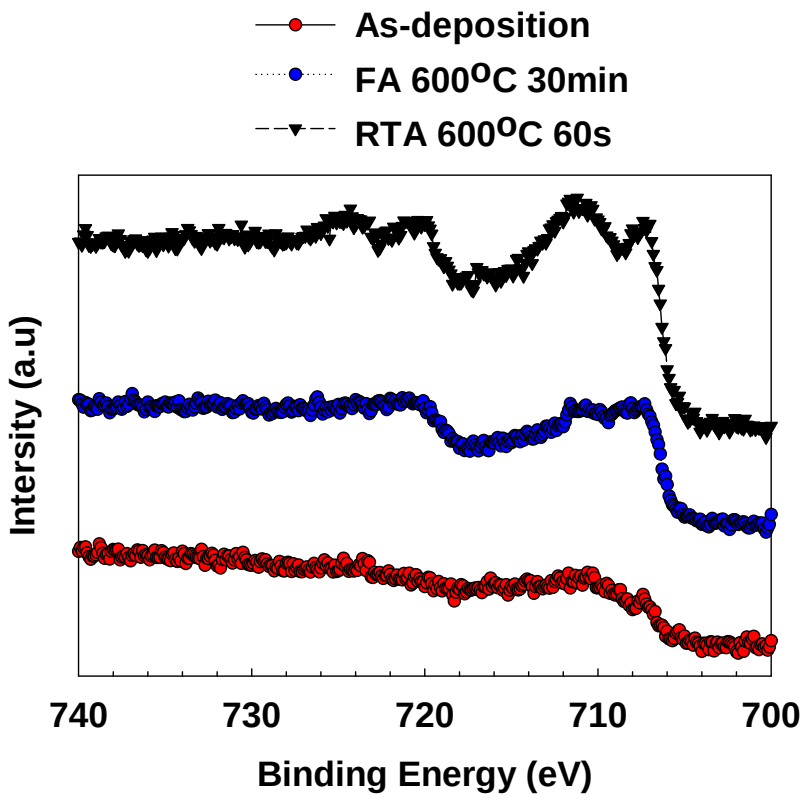


Figure 3.37. XPS results of SiO_2 and PtFe interface region (As-deposition, FA and RTA thermal condition).

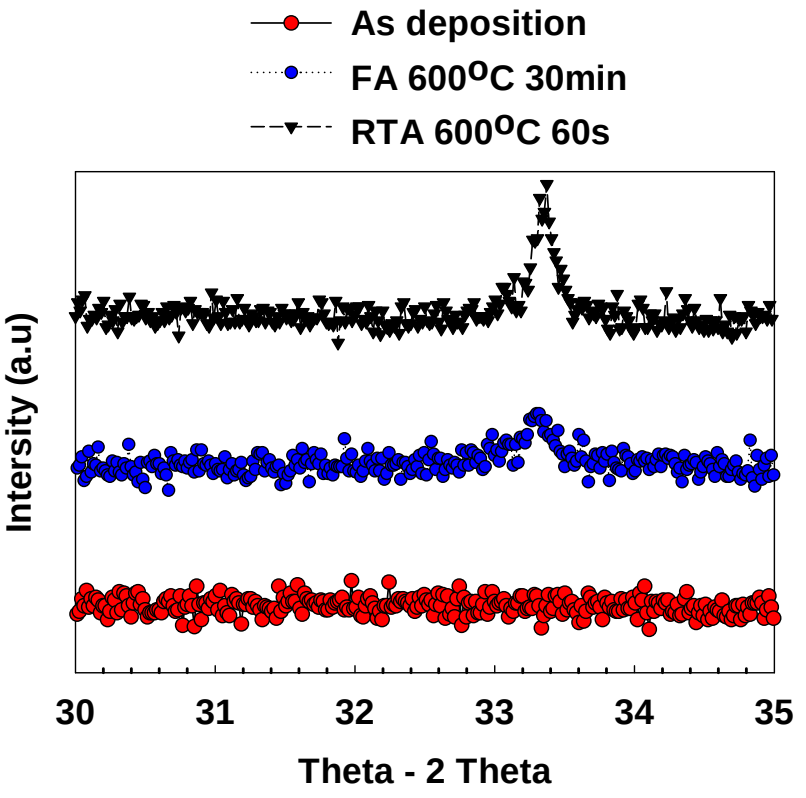


Figure 3.38. XRD results of As-deposited, FA and RTA sample.

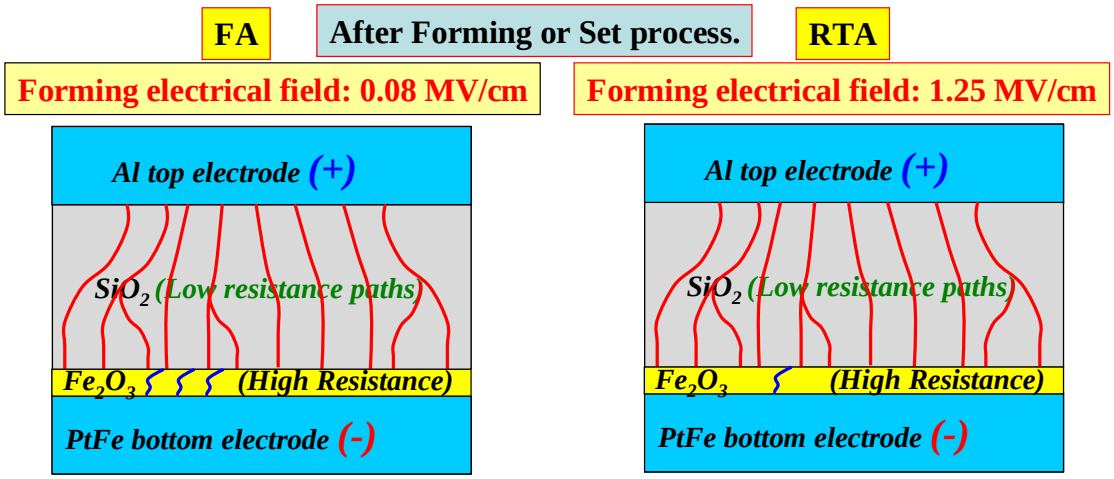


Figure 3.39. The possible mechanisms for FA and RTA sample after forming or set process.

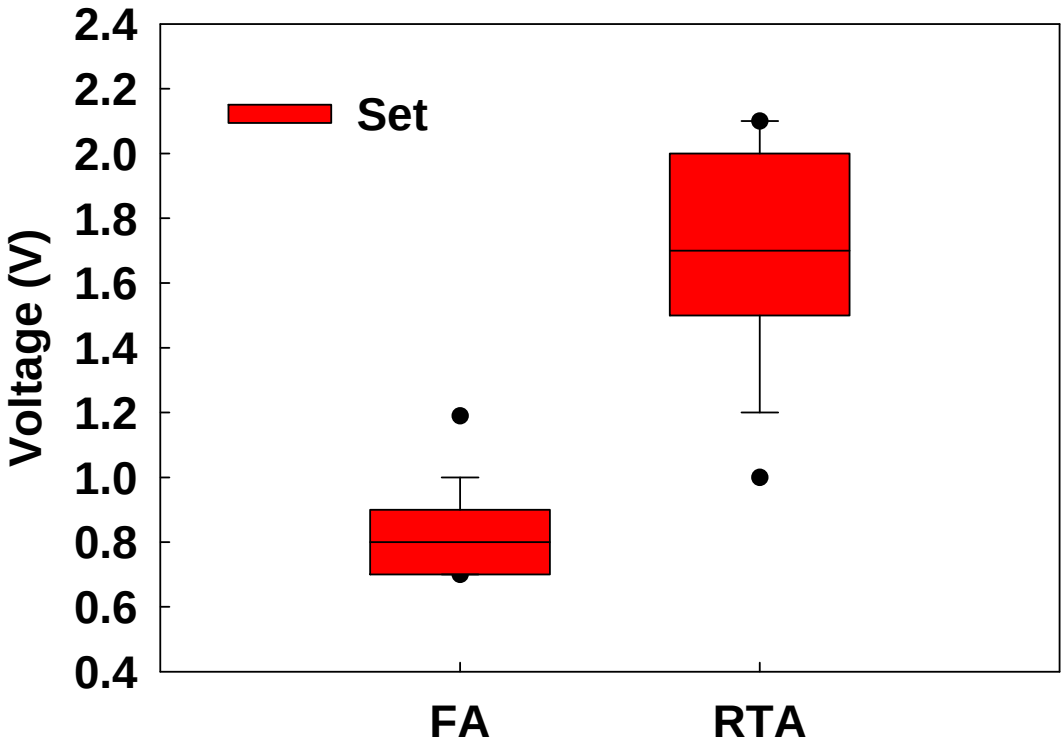


Figure 3.40. Statistics plot of the relationship between set voltage and different thermal treatment conditions.

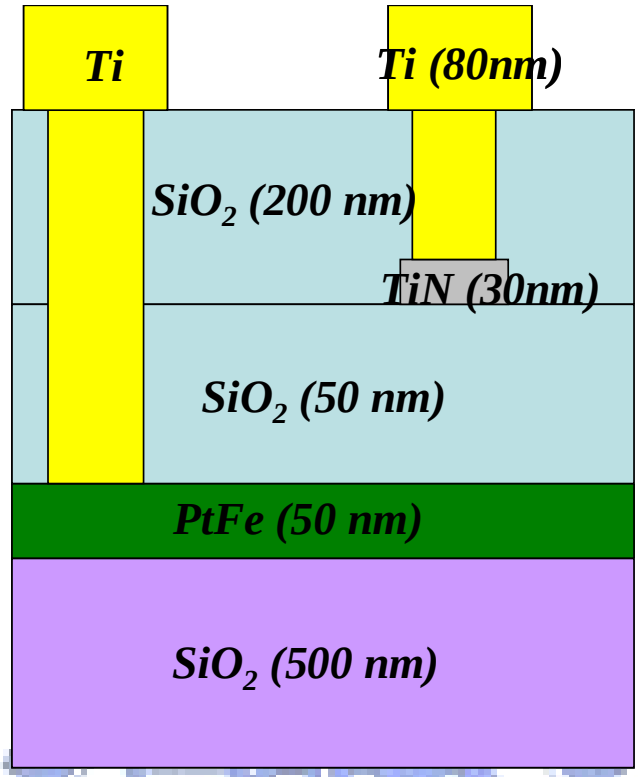


Figure 3.41 (a). Schematic diagram of small size Ti/TiN/SiO_2/PtFe/SiO_2/Si structure.

P-type Si (100) substrate

↓

RCA clean

↓

Wet oxidation (500nm)

↓

50nm $Fe_{0.73}Pt_{0.27}$ (composition by ICP-MS)

↓

50nm PECVD oxide deposition and 30nm TiN deposition by sputtering, then TiN patterning & etching

↓

200nm Via hole and 250nm contact hole, then 80nm Ti lithography patterning and etching (100um×100um)

↓

Rapid thermal annealing 600°C 60s

Figure 3.41 (b). Process flows of Small Size Ti/TiN/SiO_2/PtFe/SiO_2/Si structure.

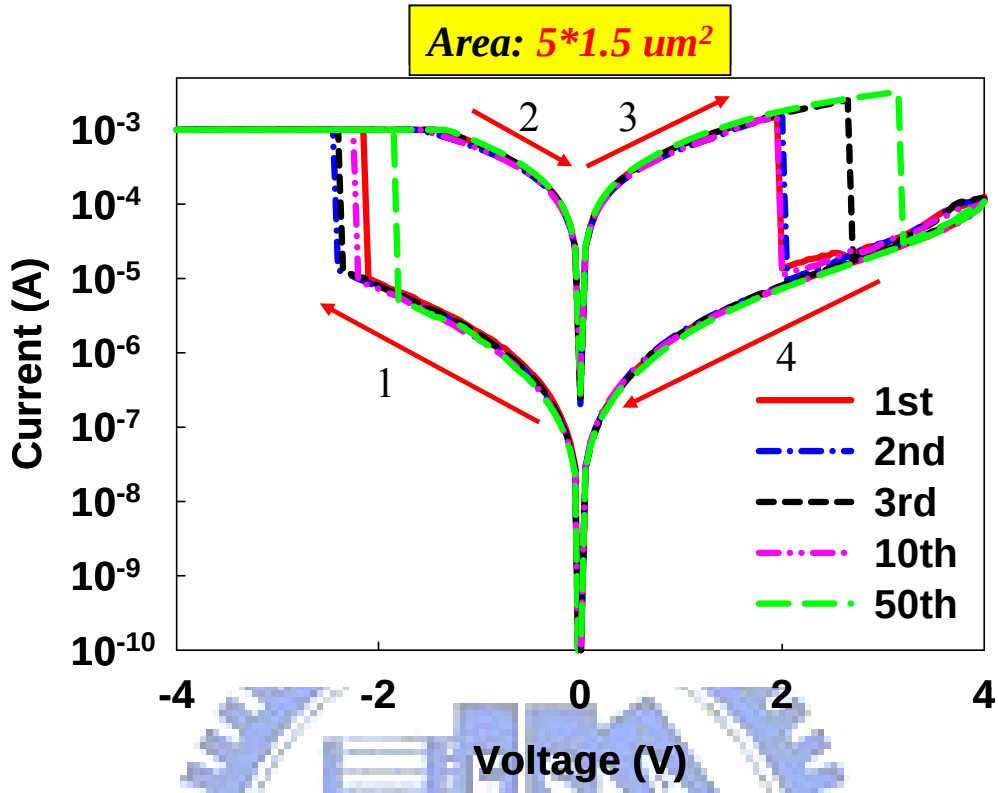


Figure 3.41 (c). *I-V* curve of Ti/TiN/SiO_2/PtFe structure (top electrode area: 7.5um^2).

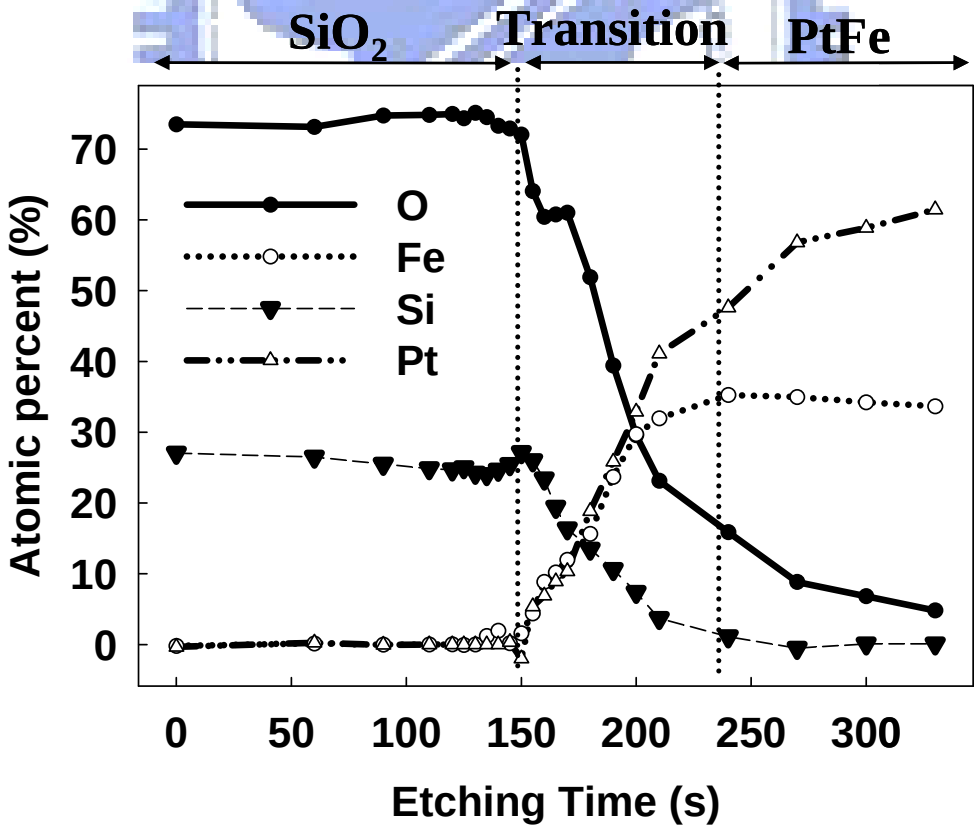


Figure 3.42 (a). AES results of small size Ti/TiN/SiO_2/PtFe structure.

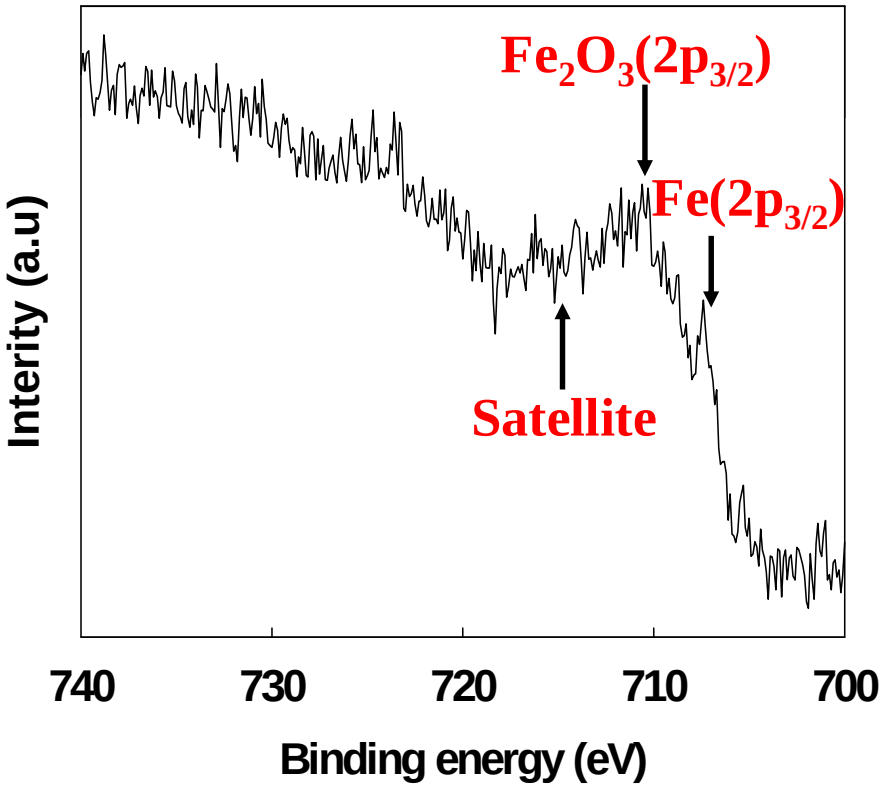


Figure 3.42 (b). XPS result between SiO_2 and PtFe bottom electrode interface region.

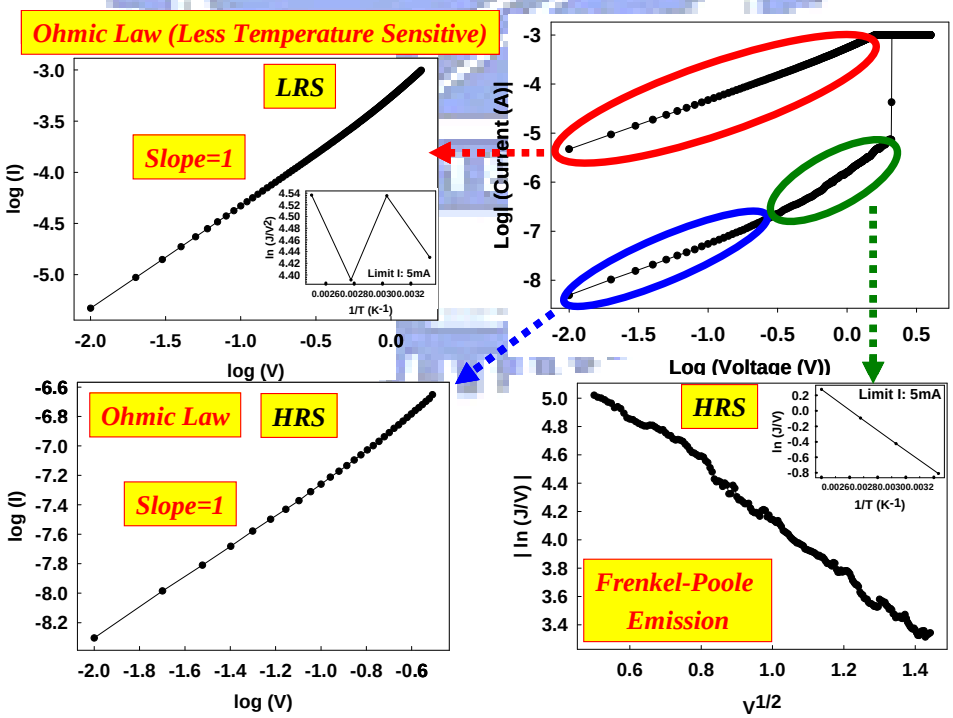


Figure 3.43. For small size structure, current fitting results of LRS (upper left, insert shows less temperature sensitivity), small bias region at HRS (lower left), and high bias region at HRS (lower right) (insert shows FP emission mode at difference temperature).

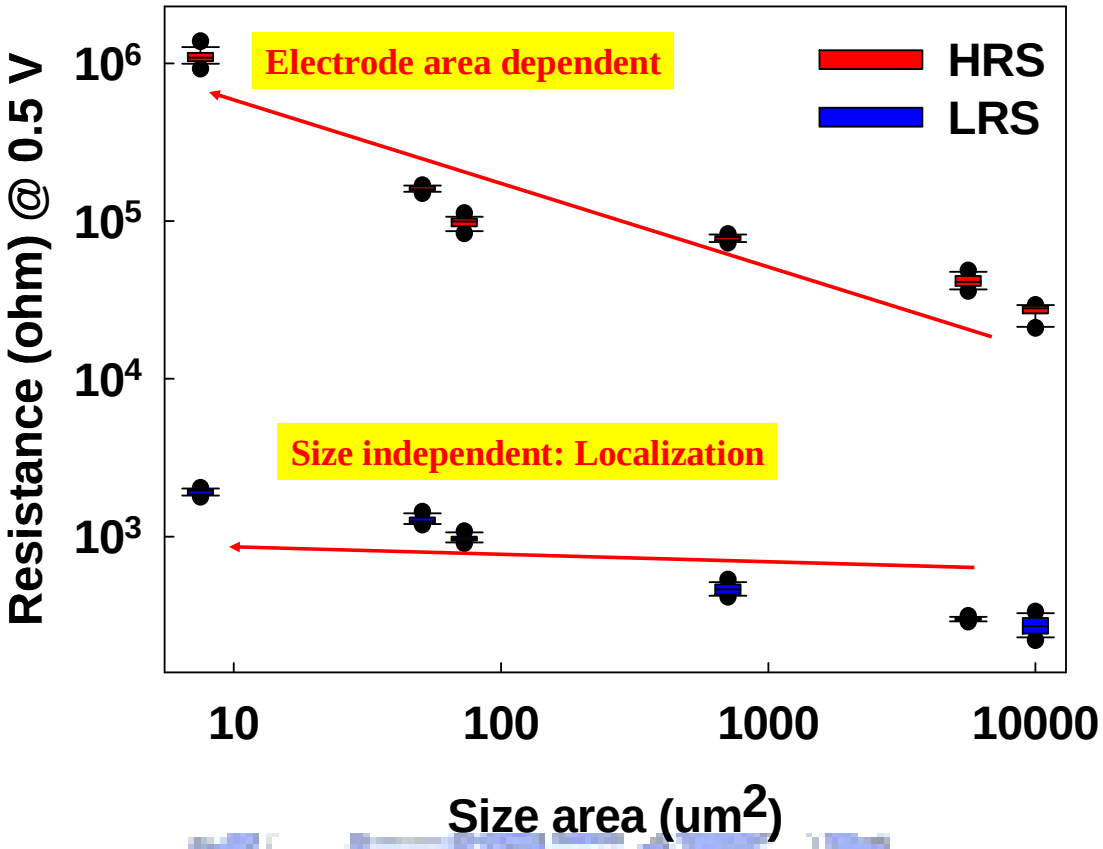


Figure 3.44. Statistics plot of the relationship between HRS (LRS) resistance and device size.

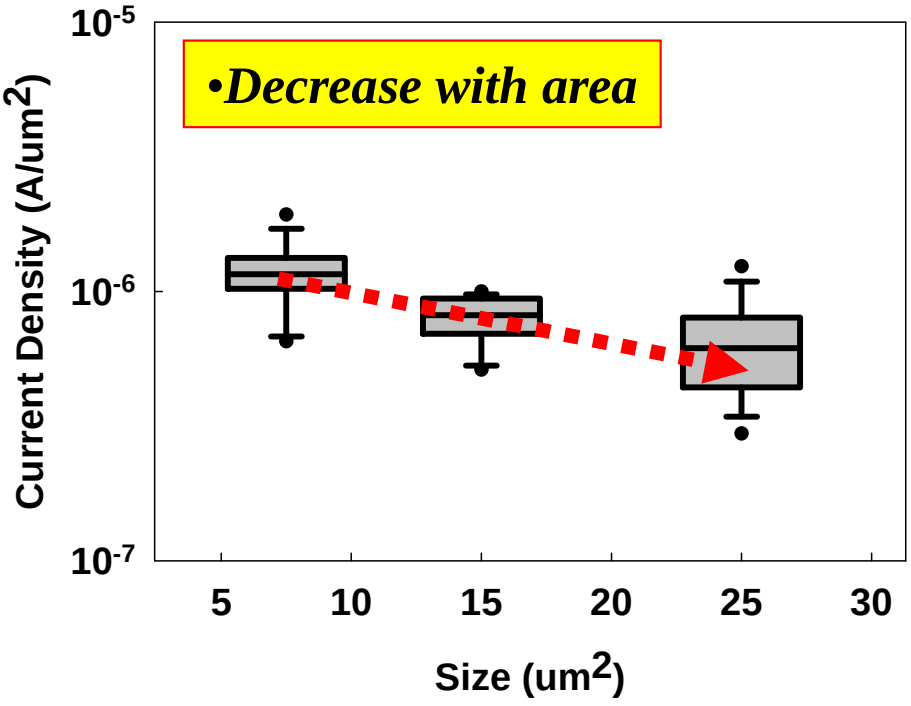


Figure 3.45 (a). Statistics plot of the relationship between set current density and device size.

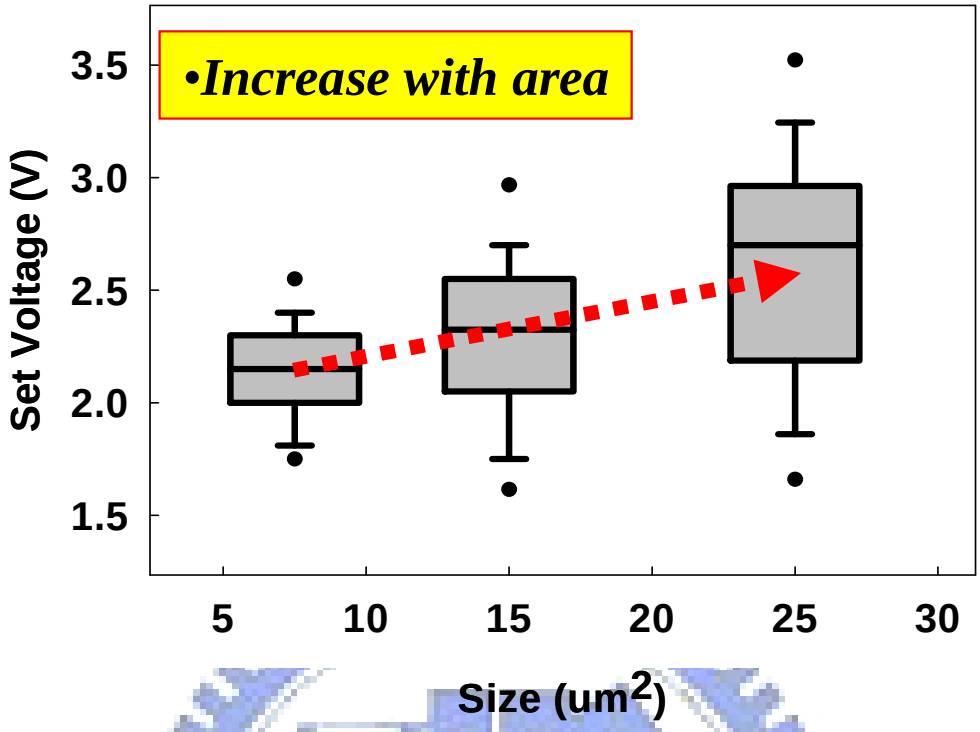


Figure 3.45 (b). Statistics plot of the relationship between set voltage and device size.

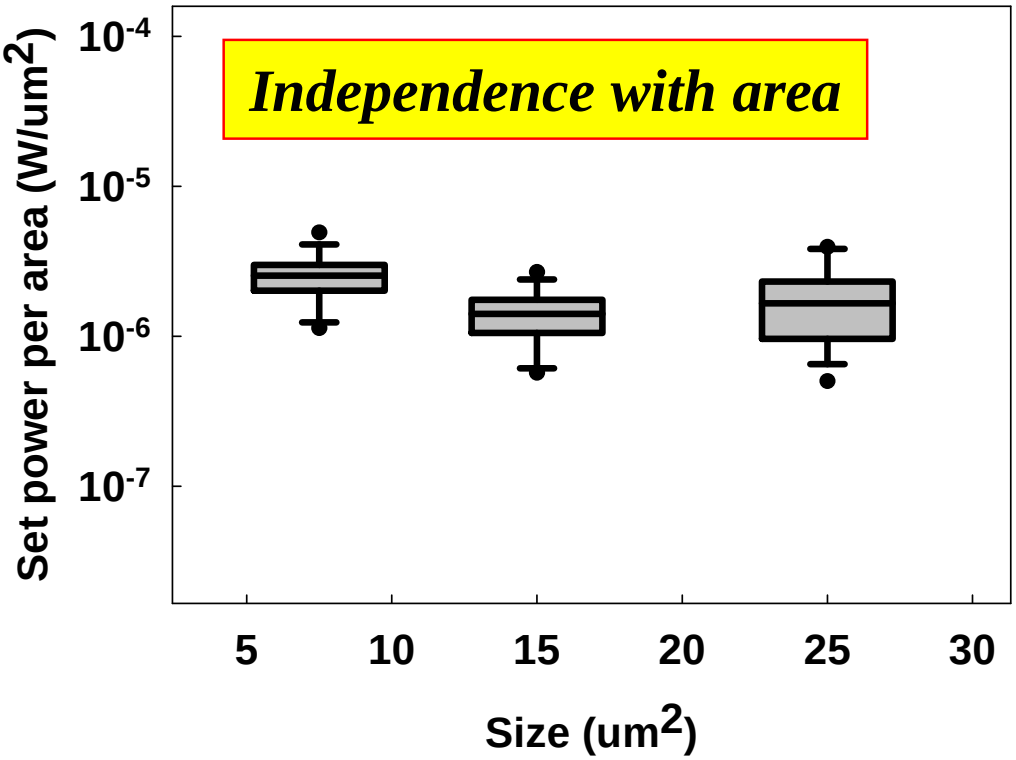


Figure 3.45 (c). Statistics plot of the relationship between set power per area and device size.

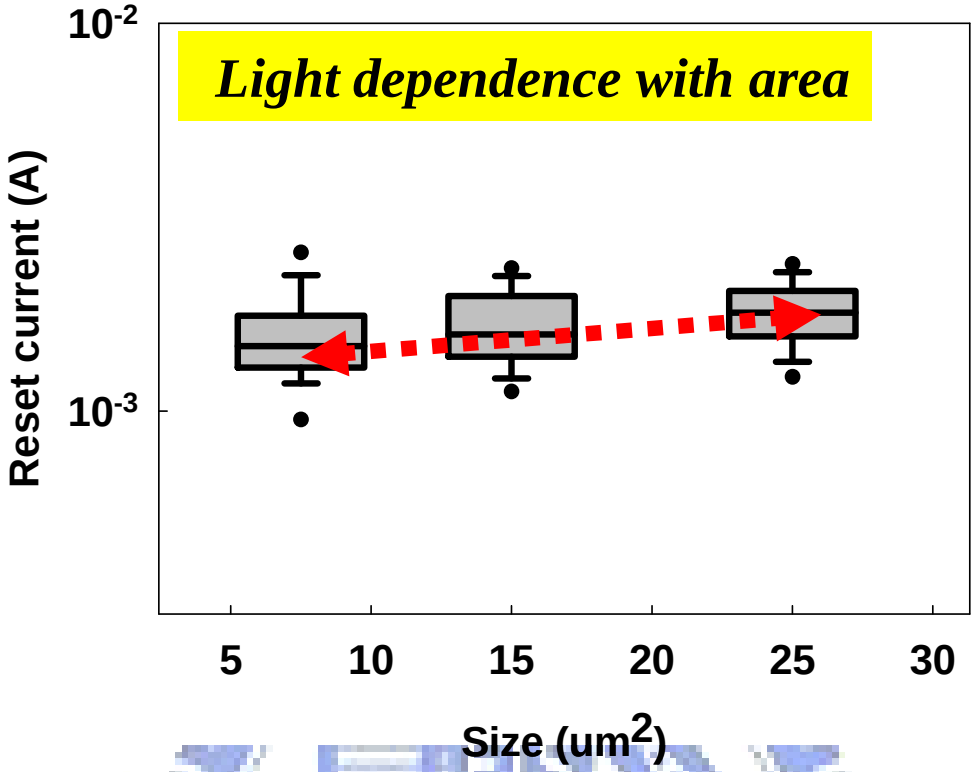


Figure 3.46 (a). Statistics plot of the relationship between reset current and device size.

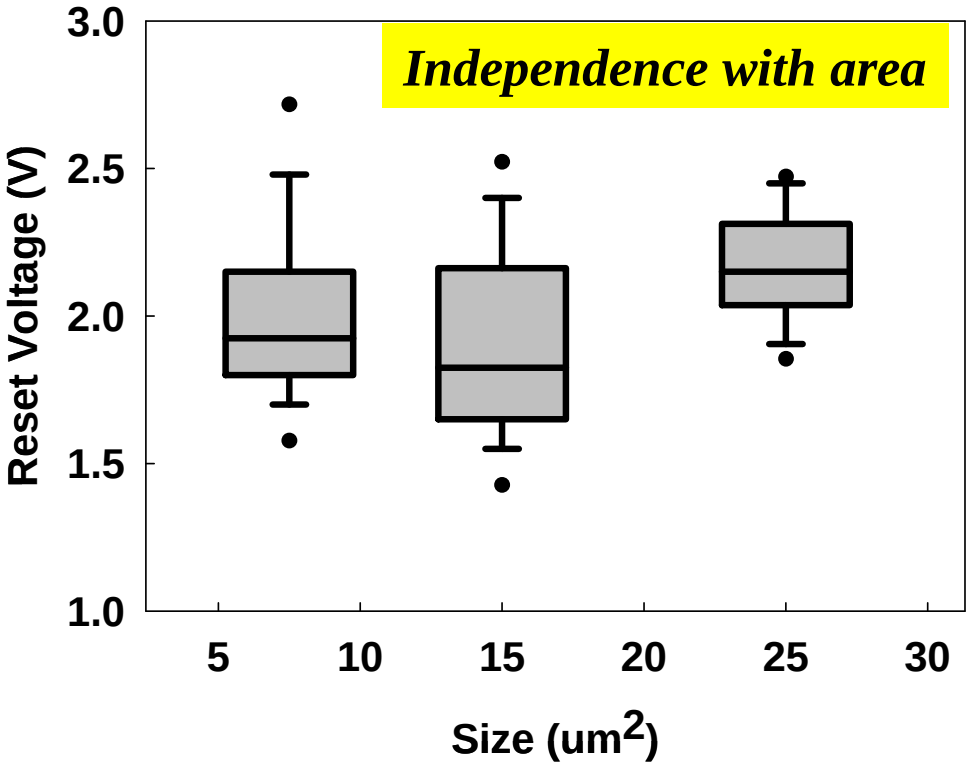


Figure 3.46 (b). Statistics plot of the relationship between reset voltage and device size.

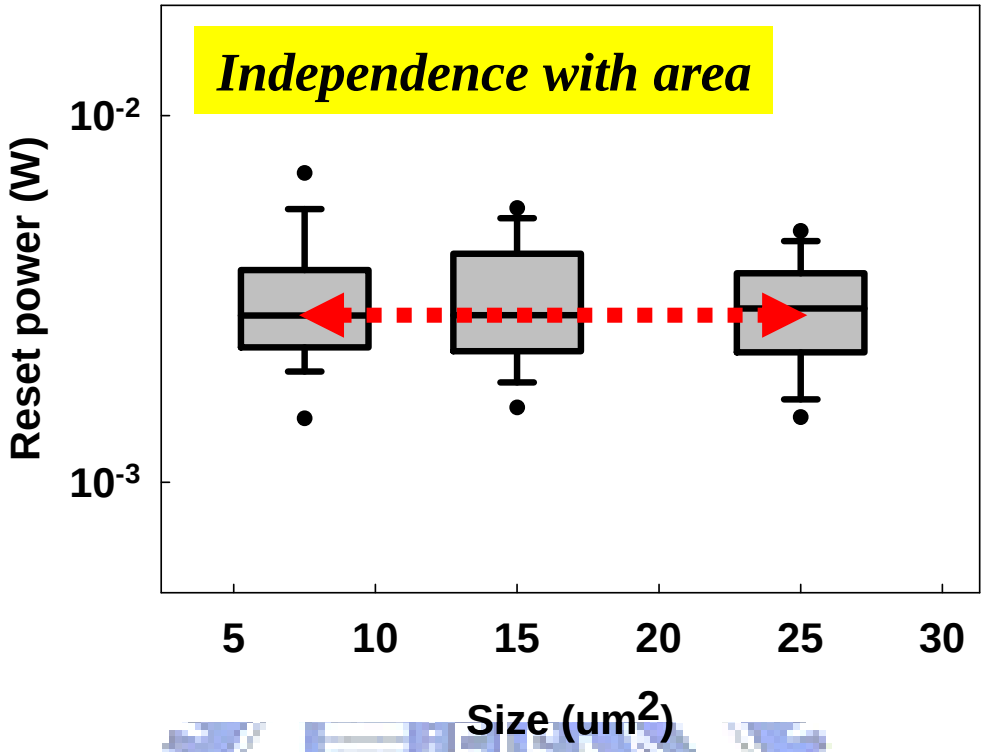


Figure 3.46 (c). Statistics plot of the relationship between reset power and device size.

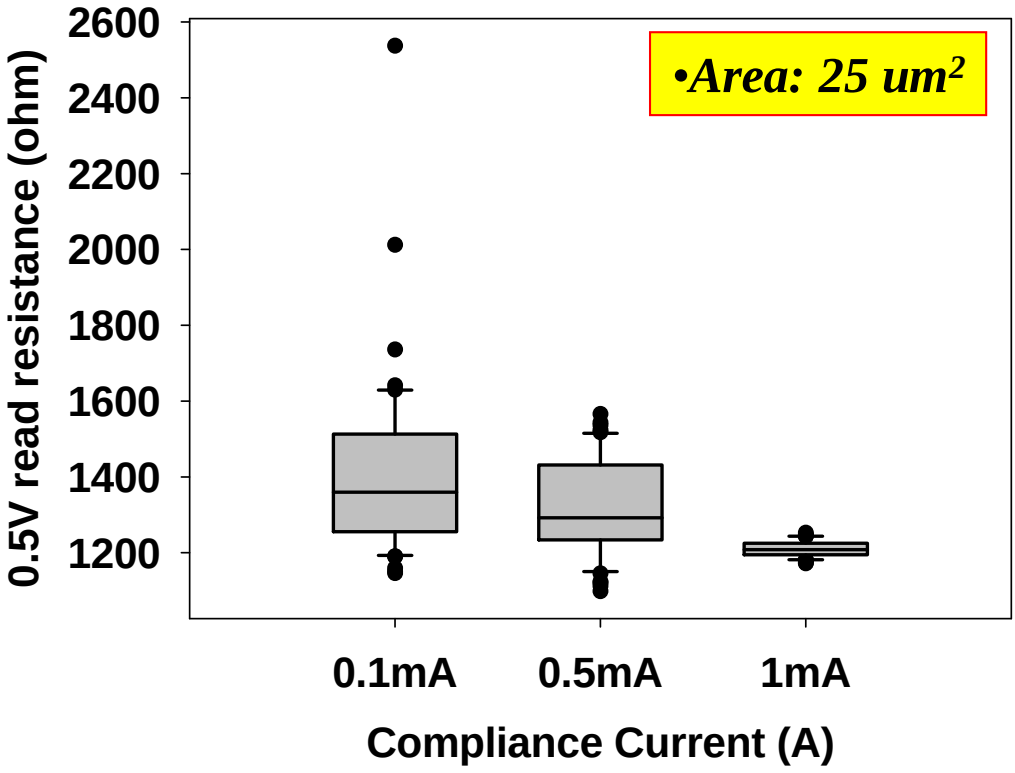


Figure 3.47. Statistics plot of the relationship between 0.5V read resistance and compliance current.

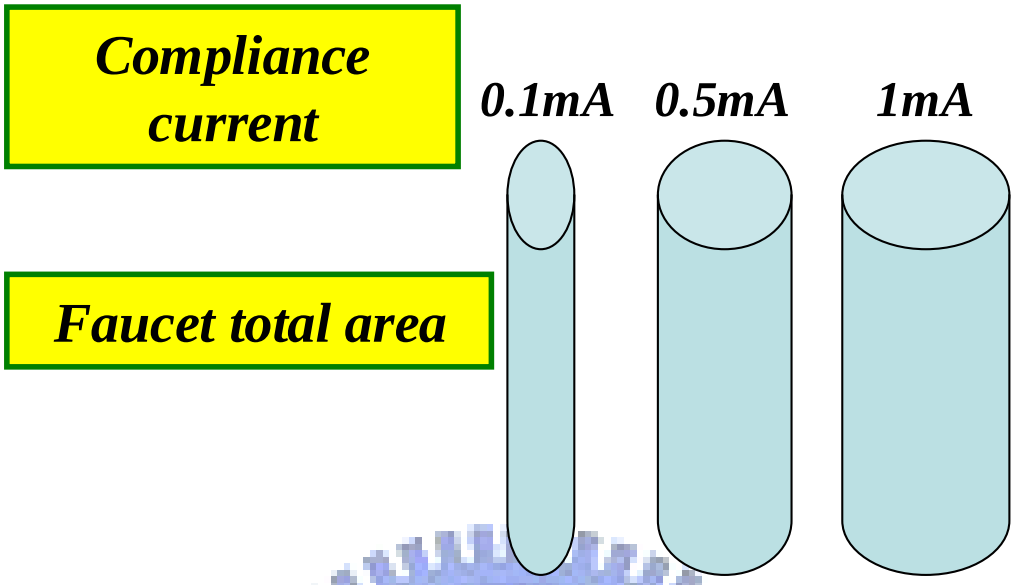


Figure 3.48. Relationship between electric faucet's cross section area and compliance current.

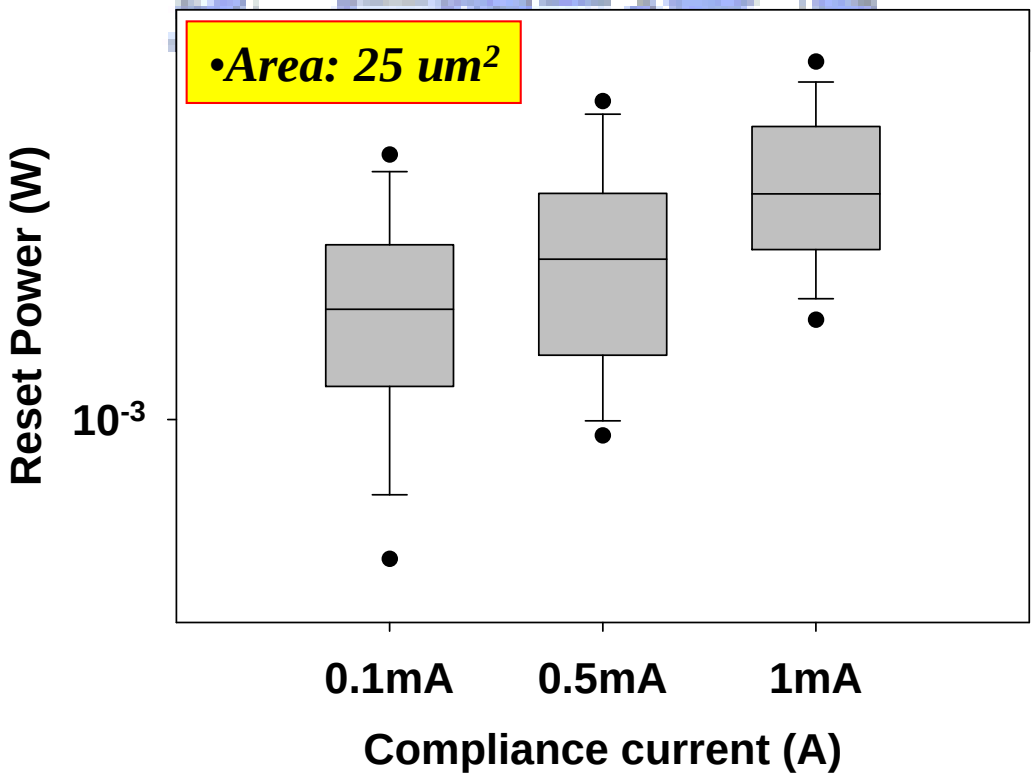
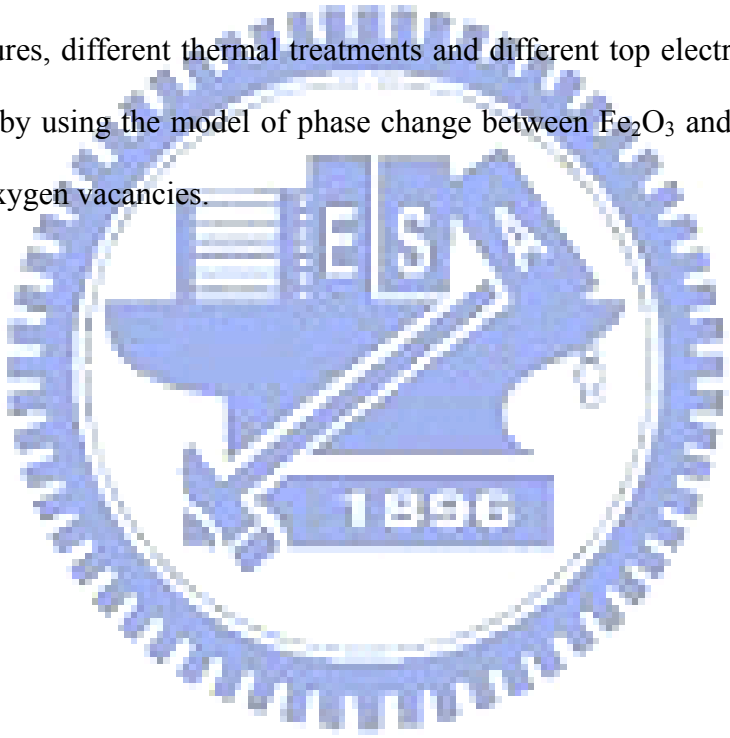


Figure 3.49. Statistics plot of the relationship between reset power and compliance current.

Chapter 4
Conclusion

In this thesis, it has been shown that the SiO_2 possesses resistive switching phenomena. We have proposed a possible model and mechanism to explain why oxygen vacancies and phase change between Fe_2O_3 and Fe_3O_4 in the Ti/TiN/SiO_2/PtFe structure which presents the resistance switching behavior. Different device structures, different thermal treatments and different top electrode sizes could be explained by using the model of phase change between Fe_2O_3 and Fe_3O_4, and the amounts of oxygen vacancies.



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