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碩士論文

鈦上電極對濺鍍法製備之氧化鋯薄膜於電阻式轉換記憶元件之研究

Resistive switching properties of sputtered ZrO_2 thin films with Ti top electrode

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摘要

隨著科技越來越進步， 各種消費性電子產品的發展快速，各種產品所需要的記憶體容量越來越大，而其中不需要電源供應仍能儲存資料的非揮發性記憶體，也漸漸受到矚目。其中，電阻式非揮發性記憶體具有高密度、高操作速度、低功率消耗、高耐久性、可微縮化、非破壞性讀取資料、能符合現在 CMOS 製程以及結構簡單等特性，因此有機會取代 flash memory，使其成為次世代非揮發性記憶體的熱門選擇。

在這篇論文中，電阻轉換特性研究是著重在鈦/氧化鋯/鉑的結構，包含製程條件可以分為大兩部份，第一部份是氧化鋯製程溫度的選擇，第二是部分氧化鋯製程結構的改變。

在氧化鋯製程溫度的選擇中，其成長溫度從 25°C，100 °C，150 °C，200 °C，

250 $^{\circ}$C 中，而成長厚度均為 30 奈米，其中 200 $^{\circ}$C 有最好的特性，其電性分析為:持久性可以達到 10000 次;動態脈衝可以以快速的 50 奈米寬的脈衝波轉態 1000 次;非破壞性讀取可以在 0.3V 下維持 10^6 秒而沒有資料的破壞。

接著以最佳的 200 $^{\circ}$C 製程溫度為主，另外作氧化鋯結構的改變，目的為分析轉態機制的探討，分為氧化鋯薄膜厚度的改變以及改變鈦上電極面積兩部分。首先藉由改變厚度，可以探討介面轉態的部份是發生元件的何處，因為鈦上電極的強吸氧性，形成一層介面轉態層，利用這層介面轉態層，跟元件的高良率、穩定的特性，轉態的極性有關，而改變厚度更可以證實利用介面轉態的機制。第二部份為鈦上電極面積的改變，利用改變面積的微影製程，結合改變厚度所得到的結論，來探討導電絲斷裂所形成的電阻大小。而電極面積越小,電阻會越大,在低阻態時電流不會下降，但高阻態時電流會下降，使鈦/氧化鋯/鉑的轉態機制能夠更加明瞭。

Resistive switching properties of sputtered ZrO_2 thin films with Ti top electrode

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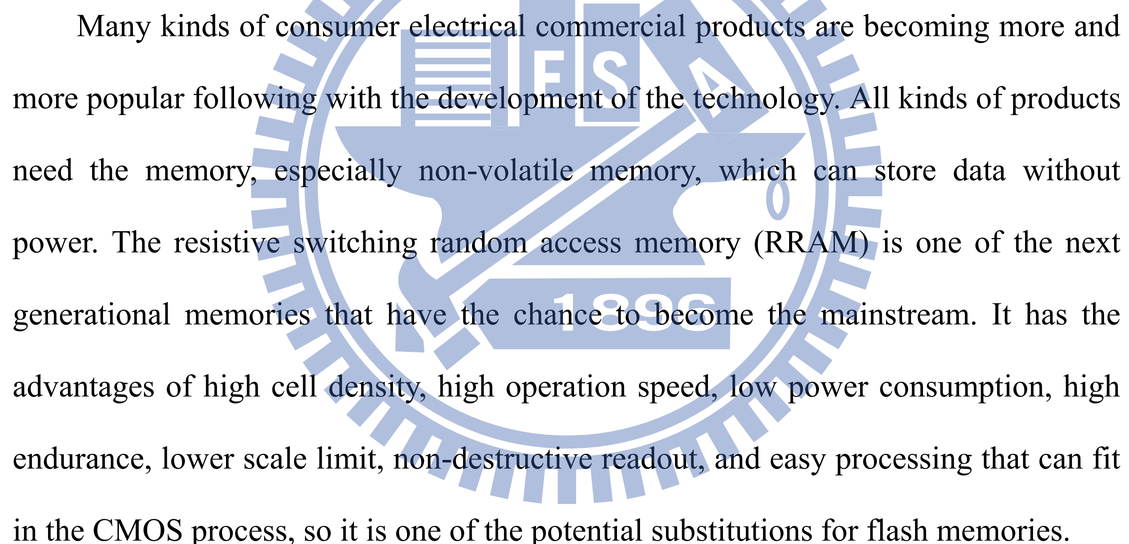
Abstract



Many kinds of consumer electrical commercial products are becoming more and more popular following with the development of the technology. All kinds of products need the memory, especially non-volatile memory, which can store data without power. The resistive switching random access memory (RRAM) is one of the next generational memories that have the chance to become the mainstream. It has the advantages of high cell density, high operation speed, low power consumption, high endurance, lower scale limit, non-destructive readout, and easy processing that can fit in the CMOS process, so it is one of the potential substitutions for flash memories.

In this thesis, the resistive switching characteristics are investigated based on the Ti/ZrO_2/Pt structure, and the research focus on two parts. First, the process temperature of ZrO_2 is changed. Second, the thickness of ZrO_2 and the area of the top electrode are changed.

In the first part, the process temperature of the ZrO_2 is changed to five temperatures: 25°C, 100°C, 150°C, 200°C and 250°C. The optimal value is 200°C,

so the following research of the mechanism will use this temperature. The performance of 200°C is good. DC sweep cycle times can achieve 10000 times; high speed 50ns pulse width can be switched at least 1000 cycle times; retention test is 10^6s; and there is no data loss at the nondestructive readout test for over 10000 seconds.

In the second part, the purpose is to know the mechanism of the RRAM, so the structure is changed by various thicknesses of the ZrO_2 and the various area of the top electrode. First, we can use the various thicknesses of the ZrO_2 to find where the switching part in the filament is. Because Ti is a strong absorption metal, so there is an interface layer to be formed. The high yield, steady performance, and the polarities of the switching is related with the interface layer, and we can use the various thicknesses of ZrO_2 to improve this mechanism. Second, the area of the top electrode is changed by the lithography. The resistance of the filament can be affected by this factor. At on-state, the current is not related with the area of the top electrode, but at off-state, the current is decreasing following the scale down of the top electrode. It is combined with the various thicknesses of ZrO_2, so the mechanism of Ti-ZrO_2-Pt is much clearer.

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Chapter 1
Introduction

1.1 Introduction to random access memory

Random access memory (RAM) is a kind of memory that can store the data, the random means that any piece of data can be returned in a constant time, regardless of its physical location and whether or not it is related to the previous piece of data. It can be classified into two groups according to whether their data can keep when the power turn on or off. The first group is called the volatile memory, which is that the storage data will lose directly as soon as the power is turned off. The second group is called the non-volatile memory, which is that the data can retain for a long period of time without the power supply. Theses two groups are discussed as the following description.

1.1.1 Volatile memory

There are two main kinds of volatile memory. The dynamic random access memory (DRAM) and static random access memory (SRAM) separately. First, Fig. 1-1 show the basic cell of the DRAM, which is consisted of one access transistor and one capacitor (1T1R) per bit. Although its advantage is for the high density (6-12F^2), but the leakage current from the capacitor makes the data lose within milliseconds, so it is needed to refresh the capacitor to retain the date. Next, the Fig. 1-2 shows the SRAM, it is not like the DRAM, it dose not need to periodically refresh the data for its combination is six transistor, and its merits is for the high speed write/erase than

the DRAM, but its disadvantage is for its bigger size (50-80F^2).

1.1.2 Non-volatile memory

Due to the popularity of the 3C products, like cell phone, mp3 player, and pc parts, the requirement of the non-volatile memory is increased dramatically in recent years. The ideal specs for the non-volatile memory is consisted with low operation voltage, low power consumption, high operation speed, high endurance, long retention time, nondestructive readout, simple structure, small size, low cost, etc[ ]. But the ideal non-volatile memory that suit for all the properties above is still not in this word for the real commercial products.

The mainstream non-volatile memory nowadays is flash, included NOR flash and NAND flash. The NOR flash has high operation speed, and the NAND flash has higher density for the larger data storage. A primary structure of flash memory is MOSFET-like transistor with a floating gate, which was invented by Sze, which is shown in Fig. 1-3. The charge stored in the floating gate can affect the threshold voltage, so we can use the different V_{th} to operate the logic of high or low.

However, the flash has some issues like high operation voltage, low operation speed, poor retention time, and coupling interface effect during scaling down [83]. Hence, some modified flash memory, such as charge-trapping flash (SONOS) is going to replace traditional flash. But researcher still want to find the next-generation non-volatile memory, it can combined with the advantages of DRAM, SRAM, Flash with the high write/erase speed. There are four possible candidates, including ferroelectric random access memory (FeRAM) [84v], magnetroresistive random

access memory (MRAM) [80], phase change random access memory (PCRAM) or ovonic unified memory (OUM) [76], and resistive random access memory, which are discussed as following.

1.1.3 Next-generation non-volatile memory

1.1.3.1 FeRAM

Ferroelectric random access memory material can be applied with a electric field to change it polarization, and its structure is the ABO_3 as shown in Fig. 1-3. The A, B, and O atoms are located at corner, body center, and face center of the cubic respectively. When a electric field is applied to the atom, the atom location will be decided by the polarity of the electrical field. The polarization hysteresis curve is shown in the Fig. 1-4. FeRAM can be subdivided into two groups; the first is called the metal-ferroelectric-semiconductor (MFSFET) as shown in Fig. 1-5. The structure is similar to the MOSFET except the oxide film is replaced by the ferroelectric film. The polarization (+Pr or -Pr) of the ferroelectric film will affect the drain current, hence it is non-volatile with nondestructive readout property. The second type is the DRAM-like (1T1C) similar with the Fig. 1-1, where the dielectric of the capacitor is replaced by the ferroelectric film, and this kinds of DRAM-like is destructive readout and need to re-write process.

1.1.3.2 MRAM

The basic cell of magnetroresistive random access memory is the magnetic junction that consist of one thin tunneling layer in the middle of two magnetic material layers as in Fig. 1-6 The magnetization of one magnetic layer (reference

layer) is fixed and kept in a specific direction. The other layer can be switched to parallel or anti-parallel to the reference layer by applying a specific magnetic field.. The logic of high or low is determined by the resistance of the parallel or anti-parallel. To read the state, a small current go through the tunneling layer and to detect the resistance. The issue of MRAM is that its scaling ability and it limit its further development.

1.1.3.3 PCRAM (OUM)

Phase change memory or called ovonic unified memory (OUM) is a promising technology for the ideal non-volatile memory. Its structure is shown in Fig. 1-7 [59], where the GeSbTe (GST) chalcogenide alloy material is an important material for PCRAM. The logic of high or low is determined by the phase of the amorphous or polycrystalline. In the off process, a high magnitude pulse with a short tailing edge is applied on the programmable phase change material. The temperature will exceed the melting point to eliminate the polycrystalline phase, and the device is cooled to freeze to the amorphous structure. In on process, a moderate magnitude pulse with sufficient duration is applied to ensure the phase has time for crystal growth. To read it, a low magnitude with long duration time is applied to read the amorphous (off-high) or polycrystalline (on-state). The issue of the PCRAM is that its consume high power during its switching for the high temperature it used.

1.1.3.4 RRAM

Resistive random access memory (RRAM) is another candidate for the next generation nonvolatile memory devices. In this thesis, the discussion is about RRAM,

so the complete introduction on RRAM is in the next section.

1.2 RRAM

Resistive random access memory can change its state by the electrical field or current effect, the conductive of the RRAM can be switched between on-state or off-state. As in Fig. 1-8 shows that on-state is the high conductive or low resistance; and the off-state is the low conductive or high resistance. The strengths of RRAM are the high cell density array, high operation speed, low power consumption, high endurance, simple structure, lower scale limit, long retention time, and non-destructive readout. In this section, the properties are discussed in view of the structure, fabrication, material classification, operation and circuit realization.

1.2.1 Structure

1.2.1.1 Basic structure

The basic structure of RRAM is made up of metal-insulator-metal (MIM) in Fig. 1-8 [28]. The top and bottom electrodes could be used by the metal or conducting transition metal oxides, the difference of the material is according to the crystalline, work functions and the ability of oxygen absorption. In the other hand, the adhesion layer should be also considered as well, and the main character of resistive switching is determined by the insulator layer that sandwiched between the electrodes.

1.2.1.2 1D1R and 1T1R

The advance structure is 1D1R (a diode and a resistor) in Fig. 1-9 [82] or 1T1R

(a transistor and a resistor) structures in Fig. 1-10 [86]. These structures must be used to prevent misreading as shown in Fig. 1-11. I. G. Baek et al. [28] shows that if a cell is at off-state and its neighboring cells are at on-state, it will be misread as on-state because of the leakage current path around its neighboring cells. So the reading value is not the correct logic we want to know. Therefore a rectifying element is required for each cell in an array to confine the current paths. The minimum sizes for 1D1R and 1T1R structures are $4F^2$ and $6F^2$ respectively, which meet the requirement for high density arrays.

1.2.2 Fabrication method

The insulator layer is called "resistance switching layer" in the following sections, and the deposition methods are many kinds, including radio-frequency (RF) magnetron sputtering, reactive sputtering, e-beam evaporation, spin coating (sol-gel), thermal oxidation, metal-organic chemical vapor deposition (MOCVD), pulsed laser deposition (PLD), atomic layer deposition (ALD), plasma-enhanced atomic layer deposition (PEALD), and melt-grown by FZ method, as listed in Table 1-1. The RF magnetron sputtering has lower cost and wide application but poor film uniformity; e-beam evaporation and spin coating has low process cost but poor film quality as well; thermal oxidation is suitable for high reactive metal like Ni, Ti or Cu to form metal oxides and the low process cost; MOCVD, PLD, ALD, and PEALD are able to produce high quality film with good step coverage but expensive; the FZ method is able to fabricate perfect crystals with exact component proportion but not practical in semiconductor fabrication process. The different methods has related with the resistive switching characteristics for the different quality of the deposition layer.

1.2.3 Material classification

The resistive switching phenomena have been found in many materials. The research mainstream is focused on several groups, including binary oxides, perovskite oxides, manganites, and other alloy or polymers.

1.2.3.1 Binary material

The binary oxides adopted in RRAM application, such as TiO_2 [1-16], , NiO [27-38], Al_2O_3 [4,65], Cu_xO [39-43], Fe_2O_3 [44], ZnO [45,46], HfO_2 [47], SiO_2 [48,49] and MoO_x [50]. In this thesis, the ZrO_2 [17-26] is used a major material. These candidates have been widely used in other field of CMOS device, hence the compatibility with modern CMOS process would be suitable. Moreover, this material group of binary oxides has simpler element components for it is easier to control the proportion of metal and oxygen elements.

1.2.3.2 Other materials

Another extensively studied material group is $(Ba,Sr)(Zr,Ti)O_3$, BSZT. It has been studied as a role of the high-k dielectric for a long time [51]. Many BSZT in RRAM are doped with V [52], Cr [66,67,70], etc. Dopants are prone to occupy sites of intrinsic oxygen vacancies, and thus restrain the formation of them [52]. Because of the more complicated chemical components, the control of the materials is not as easy as binary oxides. Besides, there are still problems in the CMOS etching process [27]. Hence, it is not the optimistic for this material to be the future RRAM material.

The manganites discussed in RRAM is the carrier-doped manganites with

perovskite structure, $R_{1-x}A_xMnO_3$, where R and A are rare-earth and alkaline-earth ions, respectively [53-58]. They are not classified in the above perovskite system here because of their unique characteristics of conducting ferromagnets below a Curie temperature [53]. The magnitude of the manganites with perovskite structures exhibit a magnetoresistive response that is many orders of larger than that found for other materials, beside the electrical resistive switching behaviors. It is the epitaxial sample that are generally prepared by PLD [55,57] or floating-zone melt-growth method [53] to obtain the precise element proportion and physical properties. For the same reason of perovskite oxides, the future for manganites in RRAM is not so promising.

The other materials such as chalcogenide (GeSbTe) [59], sulfides (e.g. $Cd_{1-x}Zn_xS$ [60]), and organic materials including Rose Bengal sodium salt (RB) [61], copperphthalocyanine (CuPc) [62], 2-amino-4,5-imidazole dicarbonitrile (AIDCN) [62] and so on, have been investigated for RRAM application. The chalcogenide material has been drawing many attentions recently due to Intel's support, while the others are newly introduced to semiconductor processes. Besides, many organic polymers tend to degrade easily. Chalcogenide seems a more practical candidate in this group of materials.

1.3 Operation mode

Basic operation of resistive switching in a single cell can be achieved by DC sweep or pulse switching methods. Fig. 1-12 shows a typical I-V plot under DC sweep operation. Assuming the resistance state is first held in off-state, the current will suddenly increases as the DC bias sweeps toward positive direction and become on-state, which is defined as "on process" of "turn on" as indicated in the figure. The

voltage where the current suddenly increase is the V_{on} and the current is I_{on}. Then a negative voltage bias is applied to switch back to off-state with a current drop at the V_{off} and the current is I_{on}, as indicated by the “off process” or “turn off” in the figure.

1.3.1 Bipolar mode

If the switching method is required the different polarities, like the Fig. 1-12 shows, it is need the positive voltage to turn on and the negative voltage to turn off, and another situation is apply the positive voltage to turn off and negative voltage to turn on, it is called the bipolar mode.

1.3.2 Non-polar mode

If the switching is not need the specific polarities to turn on or turn off, it is called the non-polar as Fig. 1-13 shown. In other word, it can use the positive voltage to turn on or turn off, or using the negative voltage to turn on or turn off.

1.3.3 Forming process

Before the switching process, most materials need this process. It is a process that make the switching layer to soft breakdown, leading to the filament can be formed, it is usually needed a bigger voltage than the switching voltage as shown in Fig. 1-17, and it is also need a current compliance during forming process to avoid it totally breakdown.

1.4 Top electrode

1.4.1 Ti top electrode

If the top electrode is Ti, and the switching layer is metal oxide, because Ti is a strong absorption oxygen metal, there is an interface layer to form as shown in Fig. 1-14. The interface layer usually dominate the switching to bipolar, because the interface layer can be a series resistance and oxygen sink, the oxygen ions can let the resistive layer to turn on or turn off according to different polarities as shown in Fig. 1-15. Besides, Fig. 1-16 shows that the variation of the Ti top electrode at V_{on}, V_{off}, and current of on-state and off-state is smaller compared with other top electrode metal, so this is one of the important reason that using the Ti to the further research in this thesis.

1.4.2 Other top electrode metal

If the top electrode is the weak absorption oxygen metal, the interface layer will not formed between the top electrode metal and switching layer, like Pt, Cu, Ni, Ag, hence the bulk layer will dominate the switching mechanism as shown in Fig. 1-15.

1.5 Carrier conduction mechanisms

There are two states that presented the logic high or low of RRAM, and the both logic state will follow the different carrier conduction mechanisms. The on-state mostly involved is Ohmic conduction, and off-state is mostly related with space charge limited current, Schottky emission, and Frenkel-Poole emission.

1.4.1 Ohmic conduction

Ohmic conduction takes place when the injected carrier density is far less than the thermally-generated carrier density. Generally, it applies to the condition of low electric field region in which thermally-generated carriers are dominant in conduction. The current-voltage characteristics follow Ohm's law that the current passing through a resistor from one terminal to the other is proportional to the voltage drop across the two points. In addition, the temperature effect is also described in Ohmic conduction behavior. Due to the electron and phonon scattering effects, the conductivity rises with increasing temperature for conduction in semiconductor, while with decreasing temperature for metal conduction. The following is the expression for Ohmic conduction:

$$J = aV\exp\left(-\frac{c}{T}\right)$$

where a and c are constants respectively, T is the temperature, and V the applied voltage.

1.4.2 Space charge limited current

The mechanism of space charge limited current (SCLC) is attributed to defects and usually exists in the dielectric stressed by high electric fields. After charge injection from the electrodes, the space charge may form if the charge carriers are trapped and distributed over a region of area without being neutralized. The further flow of charge carriers would be impeded by this space charge region. It should be noted that the injected carriers are mostly electrons. As for conductive media, the trapped carriers are able to be neutralized or screened rapidly; therefore the space charge region would not form.

The complete trapped controlled SCLC mechanism is composed of two stages

[24], trap-unfilled SCLC and trap-filled SCLC, both can be written as the following expression:

$$J = \left(\frac{\theta}{\theta+1}\right)\frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

where J is the current density, is the ratio of free electron to trapped electron, N_C is the effective density of states in the conductive band, N_t is the number of emptied electron traps, ˇ is the permittivity of free space, $_r$ is the static dielectric constant, is the electron mobility, V is the applied voltage and L is the film thickness. At first stage, the traps are not filled with charges and the formula can be rewritten with <<1 as the following:

$$J = \theta\frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

As the voltage increases, the majority of traps are occupied by the injected carriers, and the current-voltage characteristics can be again rewritten with >>1:

$$J = \frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

1.4.3 Schottky emission

Schottky emission is mainly attributed to the Schottky contact of the metal-insulator interface. For the carriers to transport, they must jump across the barrier height of one of the interfaces, travel through the dielectric film, and eventually reach the other side. It is the thermionic emission that enables the carriers (mostly electrons) to overcome the interface barrier height. Therefore temperature is the key factor that energetic carriers (hot carriers) are easier to jump across the barrier. The formula of Schottky emission is expressed as below:

$$J = A^*T^2 \exp\left(\frac{-q(\phi_b - \sqrt{qV/4\pi\varepsilon_r\varepsilon_0 d}}{kT}\right)$$

where A* denotes Richardson constant, $_b$ the Schottky barrier height, the permittivity of free space, $_r$ the dynamic dielectric constant, V the external applied voltage and d the insulator thickness.

1.4.4 Frenkel-Poole emission

Frenkel-Poole emission is pretty much similar to Schottky emission mechanism. The main differences are that Frenkel-Poole emission describes the process for carriers to overcome the barriers resulted from the defect states in the dielectric material, and the barrier lowering is twice as large as that in Schottky emission mechanism. Temperature is also crucial for this carrier transportation process, while electric field plays a more important role in this mechanism than in Schottky emission, which suggests that field effects have greater impact on defect-related behavior. The current-voltage relationship can be written as the following formula:

$$J = BV \exp\left(\frac{-q(\phi_t - \sqrt{qV / 4\pi\varepsilon_r\varepsilon_0 d})}{kT} \right)$$

where B is a material-related constant, $_t$ the trap level, and other parameters are the same as those in Schottky emission.

1.5 Switching mechanisms of RRAM

The major possible models in RRAM having been proposed by other research groups; however, the resistive switching mechanisms are still under debate for not fully explained. These models including filamentary model, oxygen migration, charge trap-detrap, and cation migration. Each model may be applied for some combinations of electrodes and oxide materials.

1.5.1 Filament model

The filamentary model comes from the nature of oxide breakdown and integrity that the defects existing in an oxide bulk such as the interstitials and vacancies of oxygen and metals constitute the leakage current path, as depicted in Fig 1-18 [63]. This model has been proposed since 1970's and is one of the earliest models in resistive switching [64,65]. Recently, since nonvolatile memories have acquired a lot of attention, the further and more detailed studies have been carried out to investigate the possible resistive switching mechanisms. Among all these proposed models, it is the filamentary model that prevails in many of binary oxide films, such as TiO_2 [1,7,8,10,11,15], ZrO_2 [22,26], NiO [28,31,33] and Cu_xO [39,43], and some of the perovskite oxides such as V:$SrZrO_3$ [52], Cr:$SrZrO_3$ [66] and Cr:$SrTiO_3$ [67]. The most obvious evidences for the filamentary model are conductive atomic force microscopy (CAFM) mapping results and the cell-area-insensitivity of on-state. CAFM is one of the best tools to investigate the local conductivity throughout the film. B. J. Choi reported that by scanning the entire film surface with CAFM, only several conductive spots exist and account for the current conduction, as shown in Fig. 1-19 [2]. In addition, the on-state resistance is more insensitive to cell area due to the local conduction through the filaments instead of global conduction throughout a cell [28].

1.5.2 Oxygen migration

There are many switching behavior are attributed to the oxygen migration near electrode and resistive layer, this kind of layer cause Schottky barrier [15], Mott

transition [12], and the schematic diagram depicts the O^{2-} migration according to the voltage bias as shown in Fig, 1-20.

1.5.3 Charge trapping and detrapping model

The charge trapping and detraping model is wide-spreading especially in the material system of manganites [54-58] and perovskite oxides [70-73]. It is also applied to some binary oxides such as ZrO_2 [21,23,24] and Cu_xO [40,42]. This model can be further classified into two types in accordance with the distribution of traps, the interface-controlled and the bulk-controlled. The schematics for both mechanisms are illustrated in Fig. 1-21 and Fig. 1-22 respectively [63].

For interface-controlled trapping and detraping model, the Schottky barrier and the interface state at the interface of the electrodes and the oxide are prerequisite. A Schottky contact is formed at the interface of low work function metal and p-type semiconductor, and high work function metal and n-type semiconductor, respectively. The barrier height determines the conductivity in these systems and can be modulated by interface states, which are charged (discharged) after the injection (ejection) of electrons. It is this interface state pinning effect that modifies the Fermi level position and the barrier height, and consequently controls the resistive switching properties.

On the other hand, the bulk-controlled trapping and detraping model is ruled by the defect states playing a role of trapping centers in the oxide bulk. When the defect states are empty, the carriers are captured by these trapping centers and make little contribution to current conduction. After all the states are occupied, the carriers would be free to drift through the oxide. Besides, the occupied defect states create an internal

field that increases the bend banding (voltage drop) across the film, and further reduces the barrier height near the interface. Hence the resistance change is dominated in the bulk defect states. Generally the resistance ratio in samples of the bulk-controlled model is usually larger than that of interface-models because of greater conductivity difference between conducting (on) and insulating (off) states.

One of the major differences between trap and filamentary models is observed in current-voltage characteristics. Empirically, the change of current magnitude is relatively smooth at V_{on} and V_{off} in the trap-model predominant samples compared to those of filamentary models. This would be attributed to the different nature of gradual trapping/detraping and abrupt conducting path formation/rupture processes respectively. It should be noted that even the similar materials have different possible mechanisms because of the slight difference in the preparation process or chemical and physical properties, such as $Cr:SrZrO_3$ reported in [66] (filament) and [70] (trap), and ZrO_2 in [26] (filament) and [21] (trap), etc.

1.5.4 Cation migration

Solid-state electrolyte (SSE) is an emerging technology in RRAM technology. As implied by the name, the solid-state electrolyte provides a medium for ions to flow without being involved with any oxide breakdowns or the change in the medium structure. The basic structure for SSE RRAM is also metal-insulator-metal, MIM, with the top electrode of a more reactive metal, the insulator of an SSE, and the bottom electrode of a stable inert metal. As shown in Fig. 1-17, with a positive bias applied on the top metal, the oxidized reactive ions would penetrate into the SSE film, forming a conducting bridge and reach low resistance on-state. In the switching off

process, the same or reverse bias polarity can be applied by the mechanism of Joule heating or electrochemical reaction, depending on the magnitude of switching voltages and currents and the strength of conducting bridge [49]. Due to the nature of ion diffusion, many of the concepts are common as mentioned in the filamentary model.

Preparation method	References
RF magnetron sputter	ZrO_2[22], NiO[33,38], Cu_xO[41], Fe_2O_3[44], RAMO[54],
Reactive sputter	TiO_2[9], ZrO_2[18,21], NiO[27,34,36]
E-beam evaporator	ZrO_2[23,24], NiO[37]
Spin-coating	TiO_2[14,16]
Thermal oxidation	TiO_2[11-13], NiO[31,32], Cu_xO[39,40,42,43]
MOCVD	TiO_2[1]
ALD	TiO_2[4]
PEALD	TiO_2[5,7,8]
PLD	ZrO_2[20], RAMO[55,57,58], BSZT[70-73]
Melt-grown (FZ)	RAMO[53,56]

BSZT: (Ba,Sr)(Zr,Ti)O_3, RAMO: $R_{1-x}A_xMnO_3$

Table 1-1 List of preparation methods of resistance switching layer.

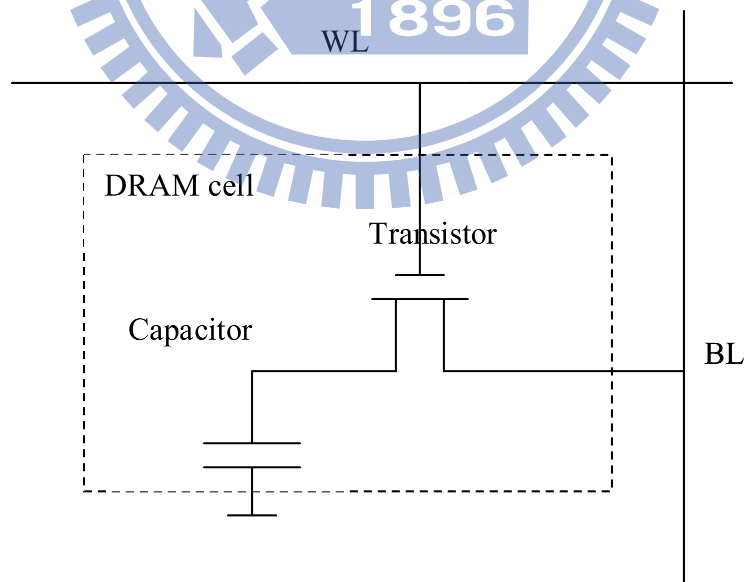


Fig. 1-1 The basic structure of DRAM

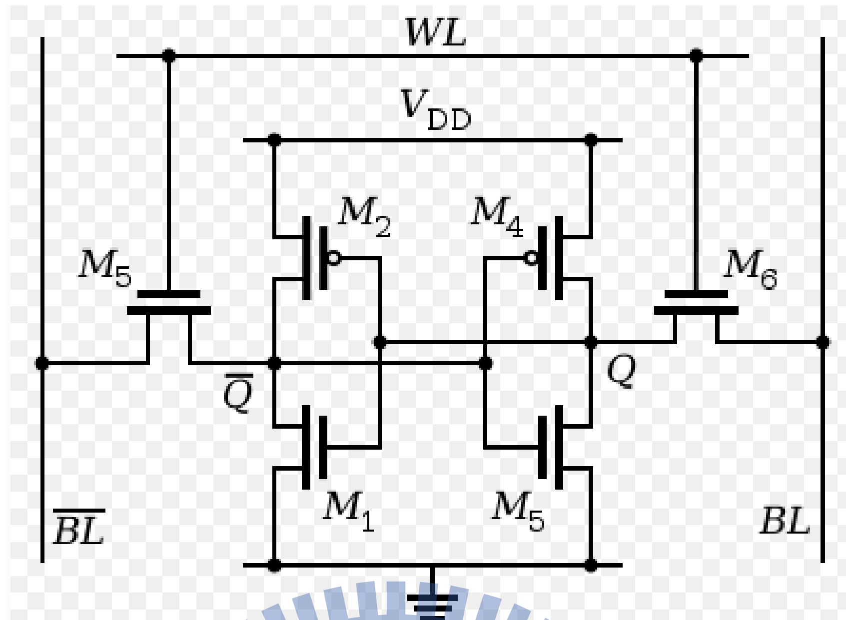


Fig. 1-2 The basic structure of SRAM

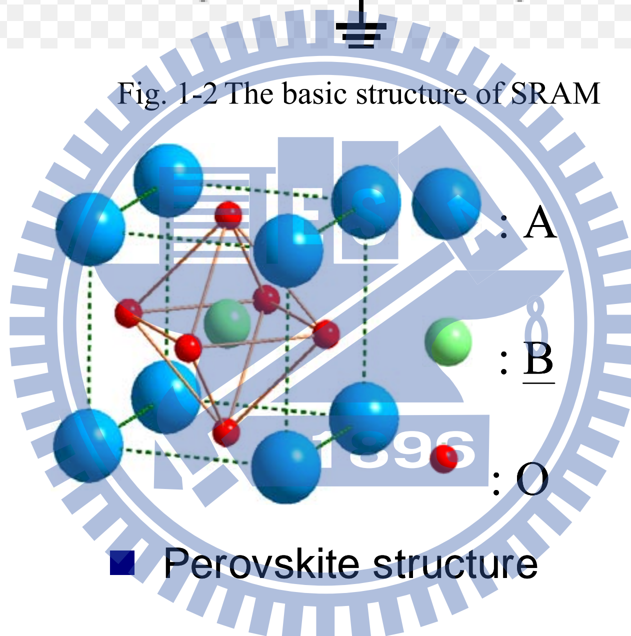


Fig. 1-3 The basic structure of ABO_3

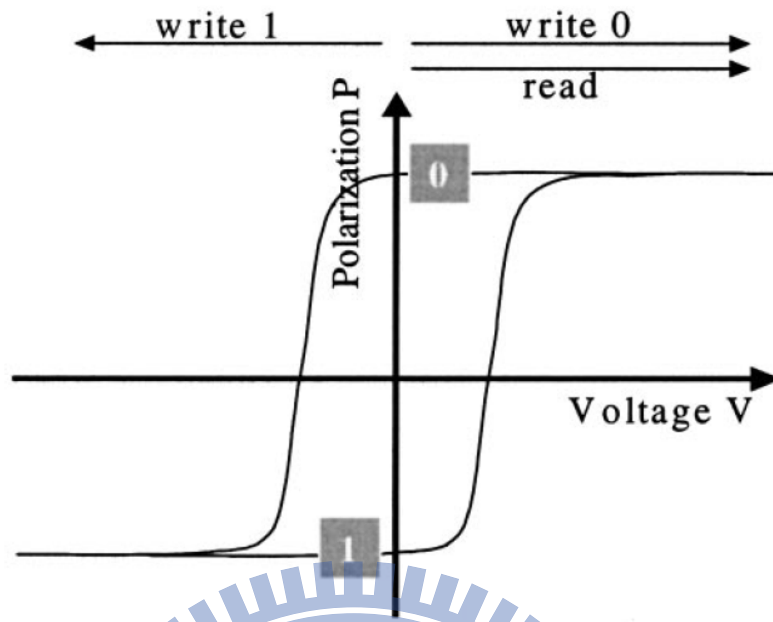


Fig. 1-4 The polarization hysteresis curve.

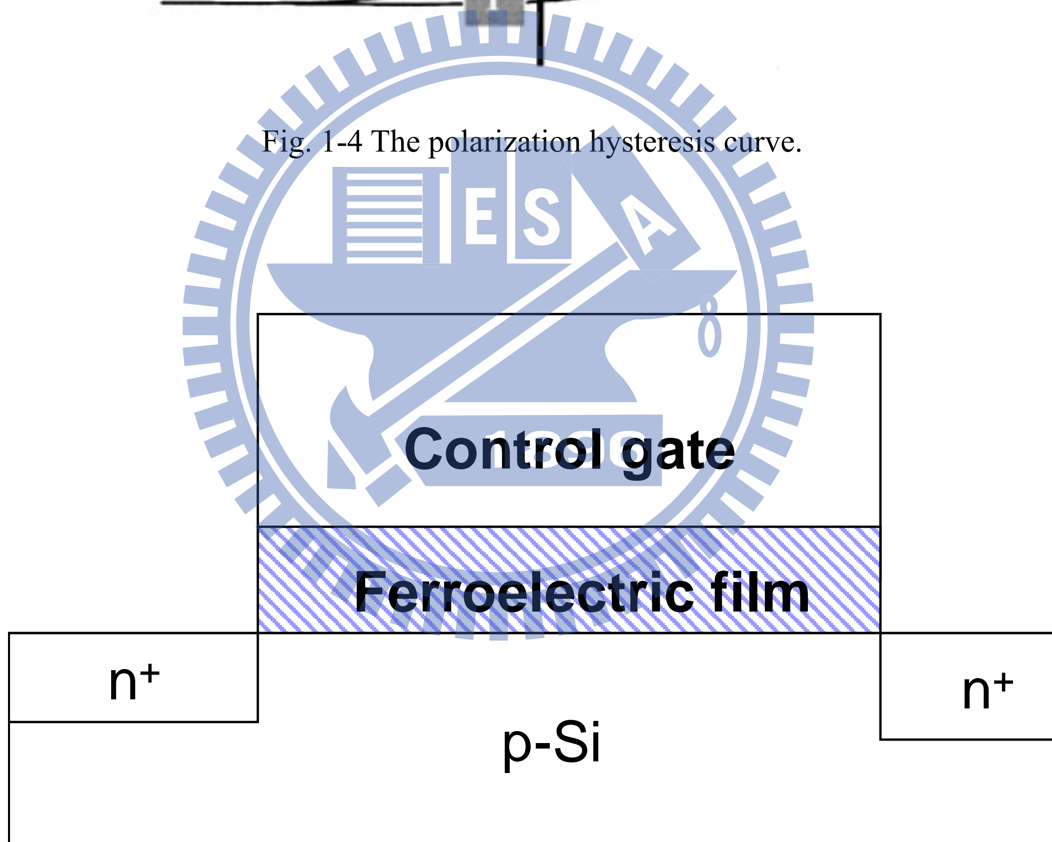


Fig. 1-5 MFSFET structure of FeRAM

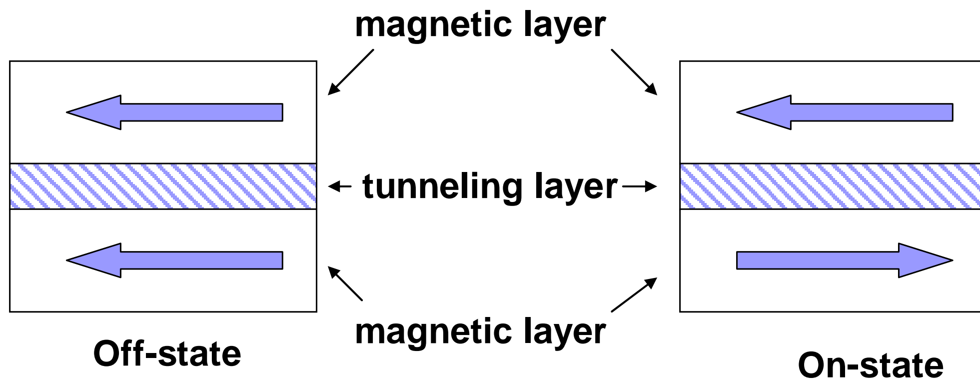


Fig. 1-6 Parallel is off-state and anti-parallel is on-state of MRAM.

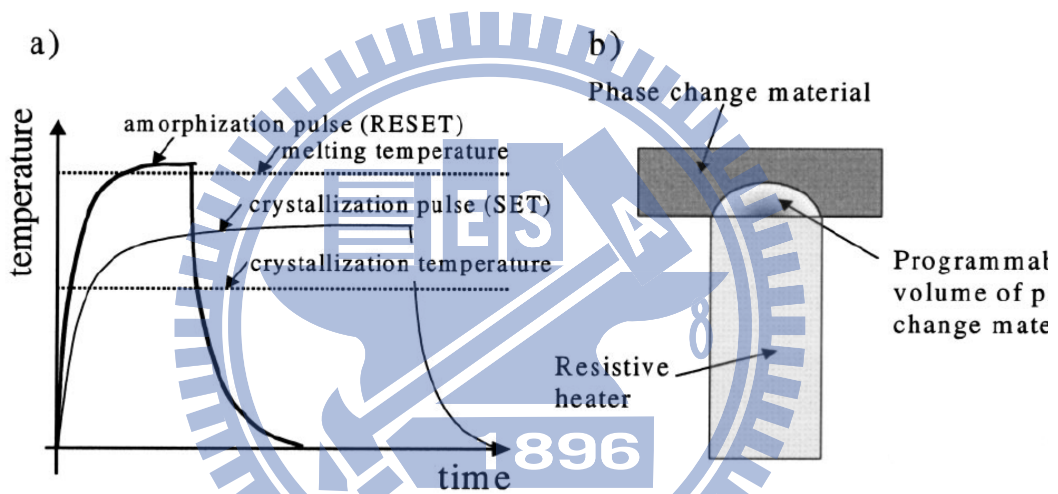
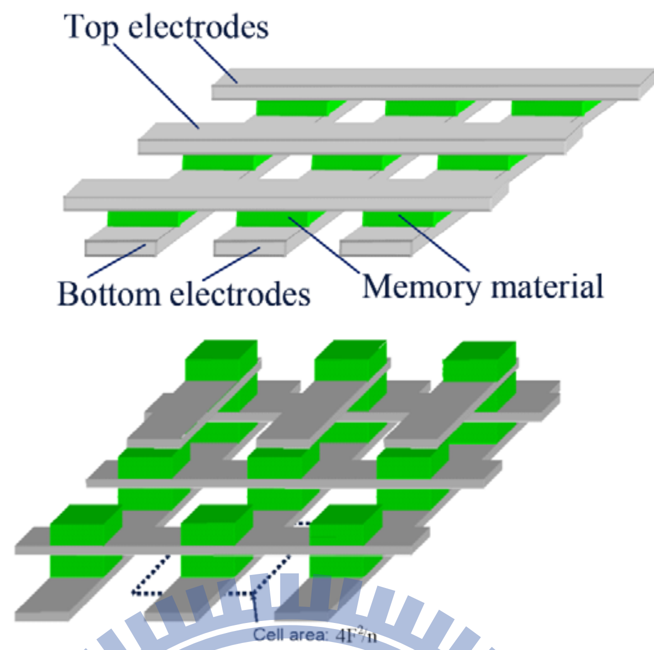


Fig. 1-7 (a) Temperature pulses required to switch a phase change material and (b) Simplified cross section of PCRAM [59]



2003 IEDM Sezi et al. **Infineon**

Fig. 1-8 Simple structure of RRAM [28]

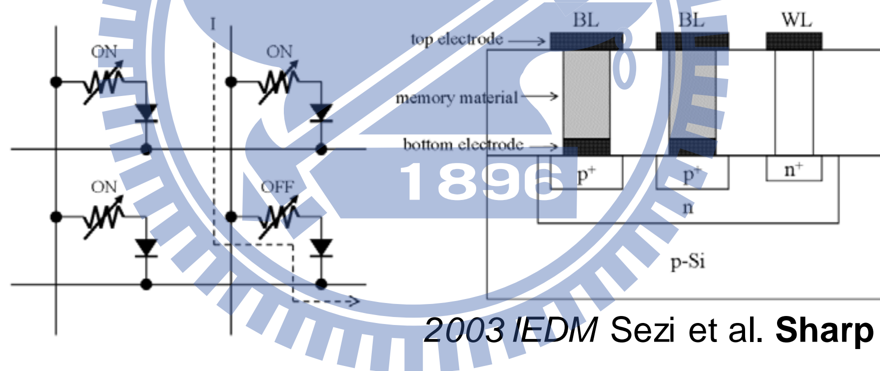
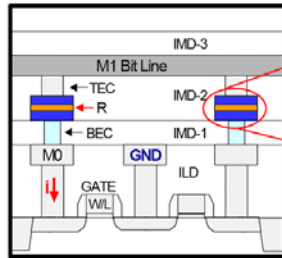
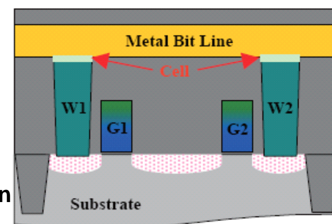


Fig. 1-9 1D1R structure of RRAM [86]

2004 IEDM Baek et al. **Samsung**



2007 VLSI-DT Ho et al. **MXIC**



2005 IEDM Chen et al. **Spansion**

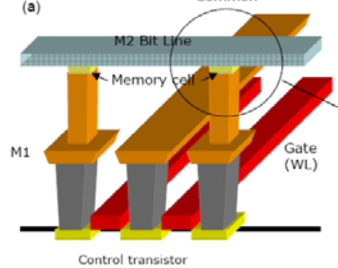


Fig. 1-10 1T1R structure of RRAM [86]

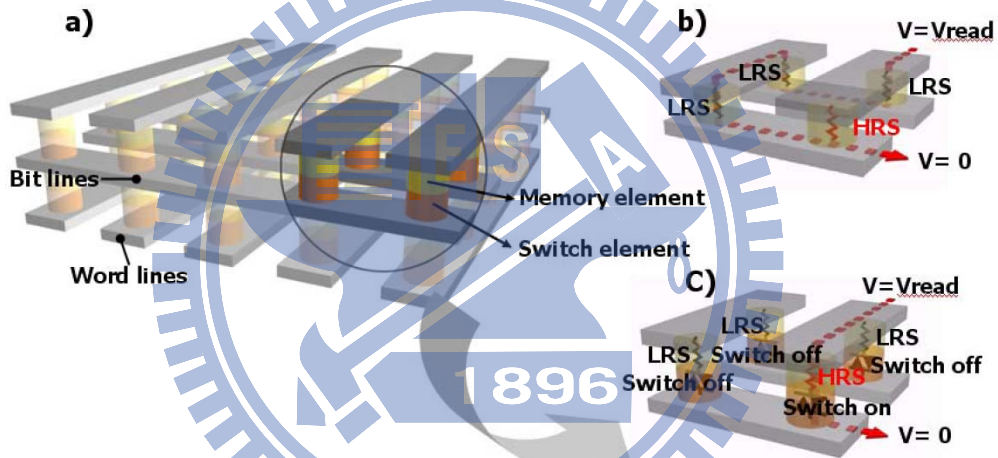


Fig. 1-11 (a) Generalized cross-point structure with memory and switching elements. (b) Reading interference without switch elements. (c) Rectified reading operation with switch elements. [81]

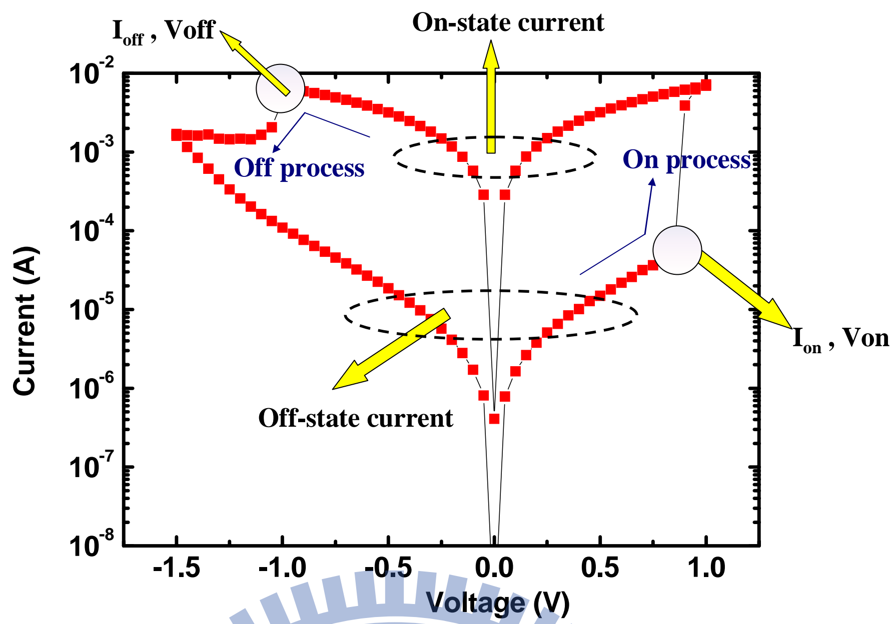


Fig. 1-12 Typical linear I-V curve of RRAM

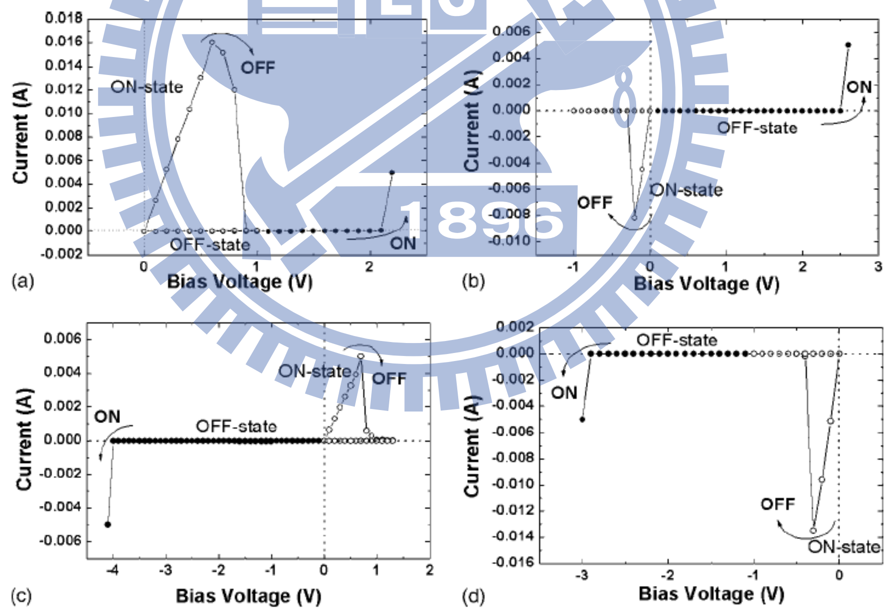


Fig. 1-13 Non-polar sweeping mode of RRAM.

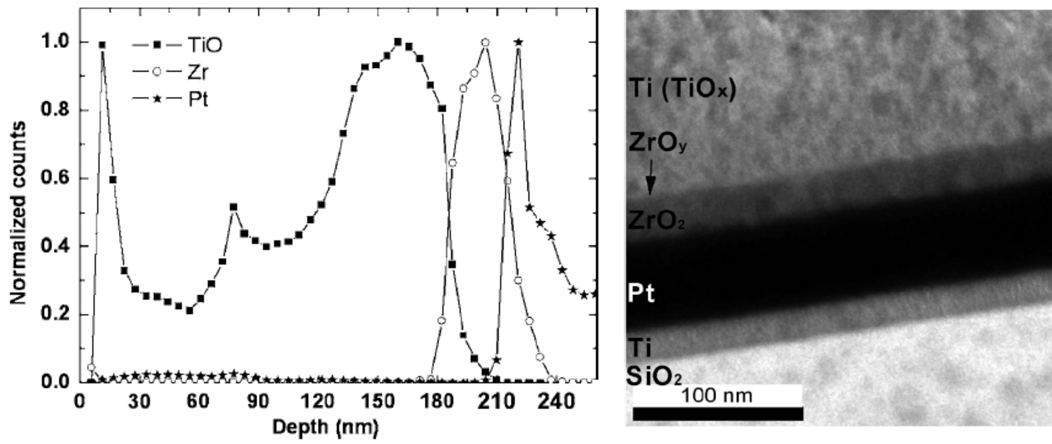


Fig. 1-14 Interface layer at the structure of Ti-ZrO_2-Pt. [28]

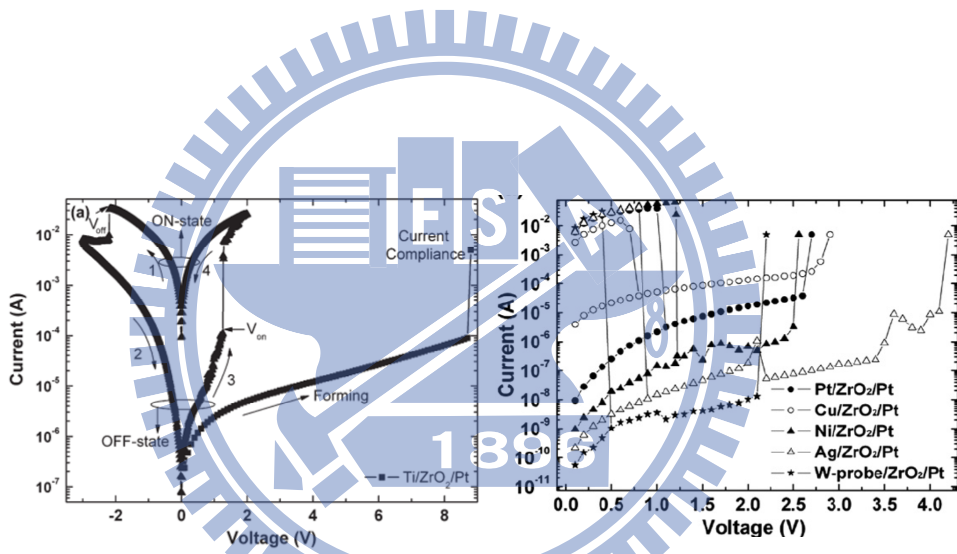


Fig. 1-15 Various top electrodes on the RRAM structure.
(a) Ti top electrode (b) Other top electrode

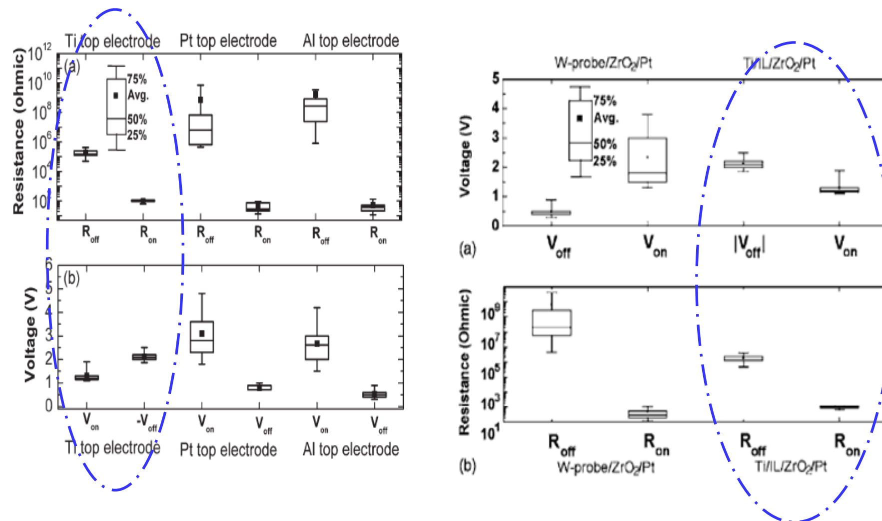


Fig. 1-16 Variation of various top electrodes on the RRAM structure.

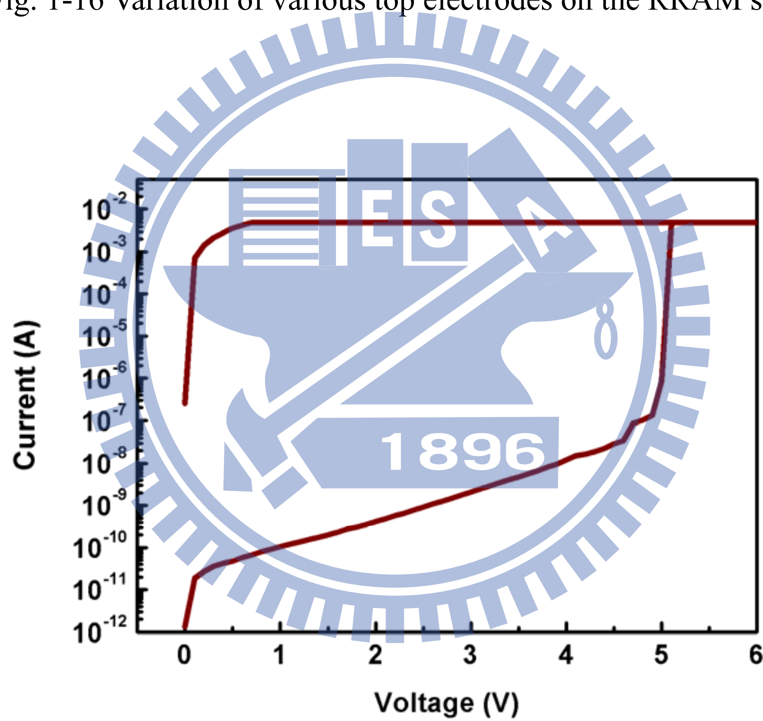


Fig. 1-17 Forming process of RRAM.

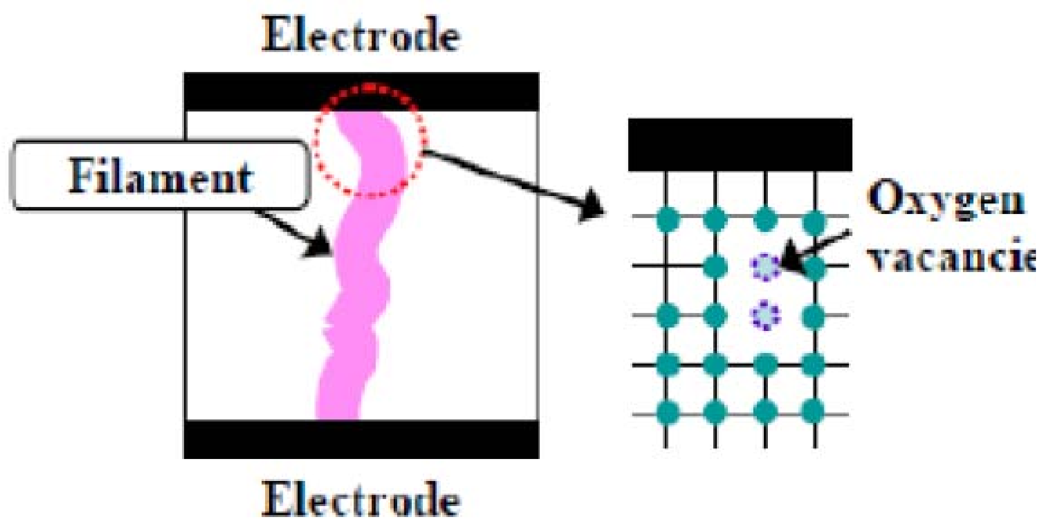


Fig. 1-18 Schematic of the filament in an oxide. [63]

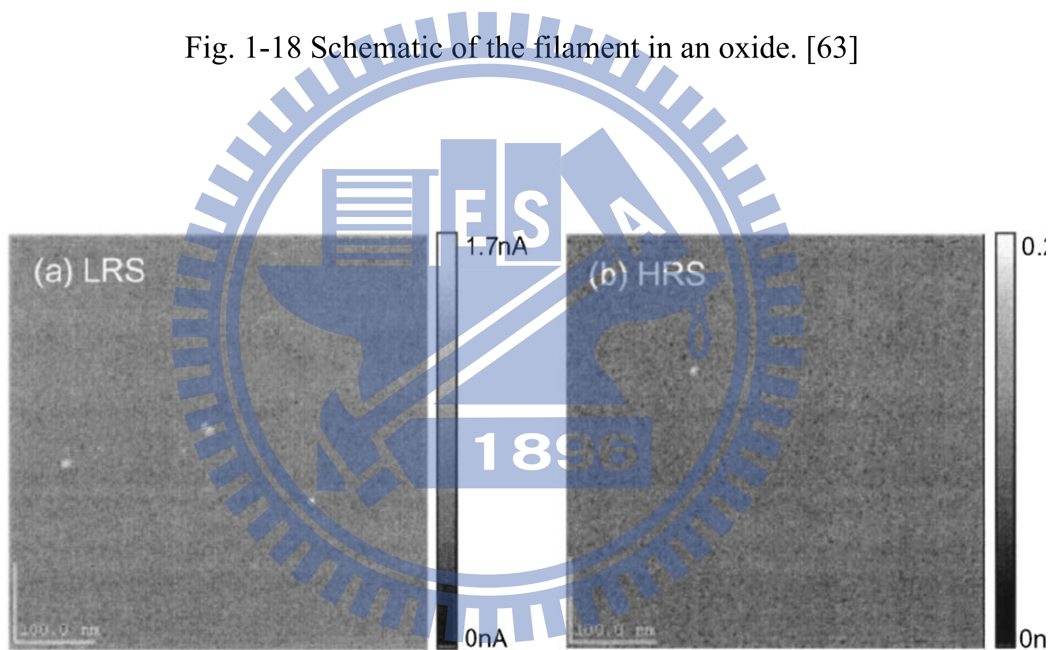


Fig. 1-19 Conductivity mapping results of the (a) on- and (b) off-state TiO_2 films, using conductive AFM (CAFM). The bright spots represent the conducting spots. [2]

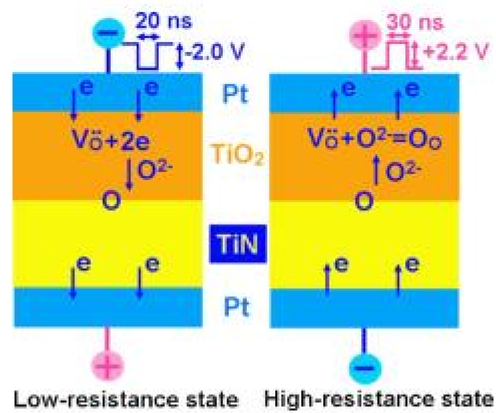


Fig. 1-20 Schematic pictures of ON-state and OFF-state of the specimen[12]

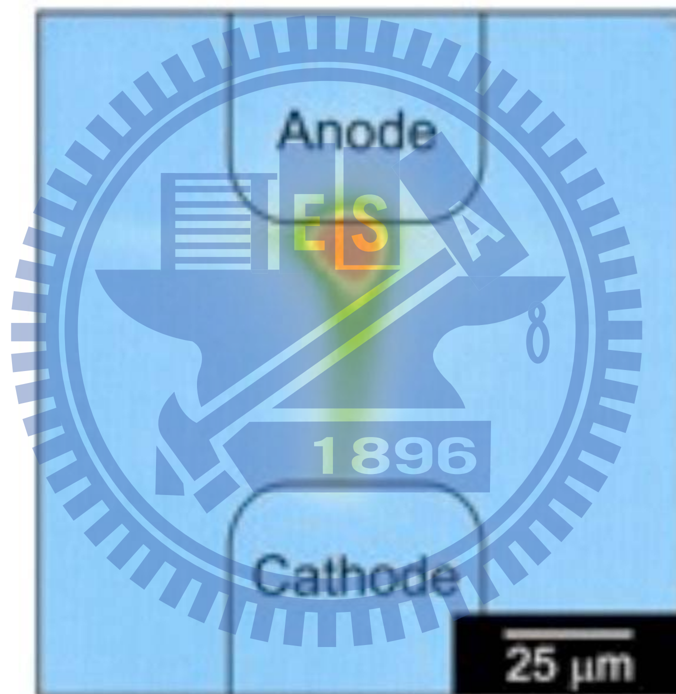


Fig. 1-21 Infrared thermal micrograph of the memory cell with a current of 5 mA at a voltage of ~30 V applied. In the color scale, blue and red represent room and elevated temperatures, respectively. [67]

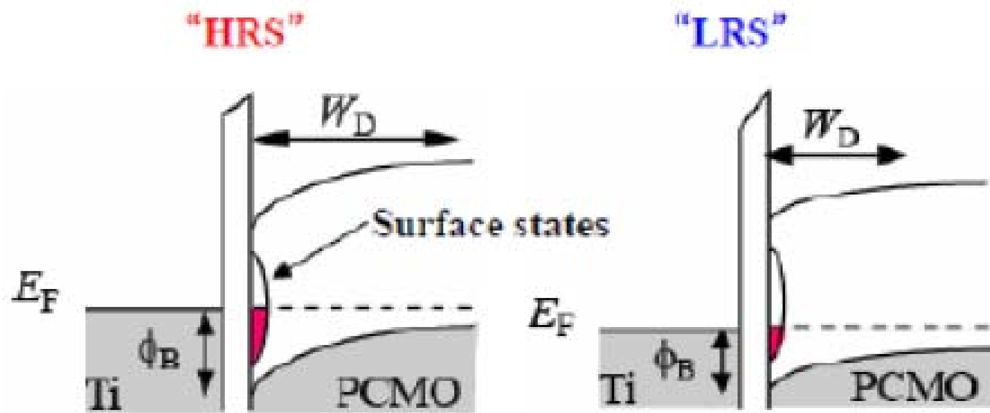


Fig. 1-22 Band diagram with the conditions of interface states for on state (LRS) and off state (HRS), respectively. [63]

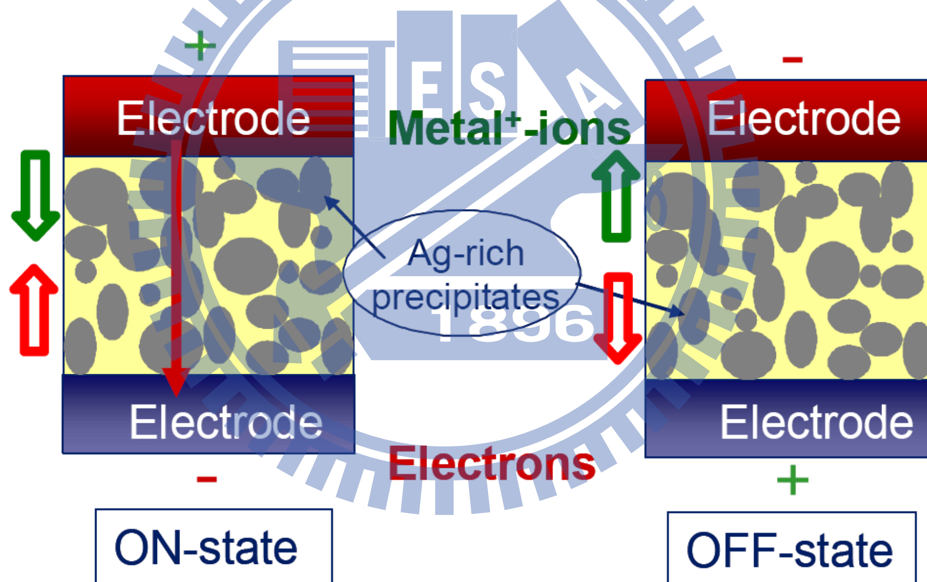


Fig. 1-23 Schematic of the switching mechanism in solid-state electrolytes. (a) On state: Redox reaction drives Ag ions in chalcogenide, resulting in a conductive bridge; (b) off state: Size and number of Ag-rich clusters is reduced, breaking the bridge. [77]

Chapter 2

Experiment details

2.1 Radio-frequency magnetron sputtering system

Sputtering system is widely used to make the thin film like metal, semiconductor, and dielectric for its characteristic of simple construction, easy operation and low cost. The ions can be used by the plasma bombard to deposit on the target, so we can use the sample to do the research of RRAM. The illustration of the RF sputtering system is shown in the Fig. 2-1, and the related main components are in the following description as below.

2.1.1 Main chamber system

The main chamber is consisted with a 3-inch sputtering magnetron gun with a shutter that can cover the ions bombard when the system operated at pre-sputter; a rotation holder that can set the sample to let the ions deposited on the sample, and the speed of the holder can be controlled by the DC motor; a heater that can control the temperature of the process.

2.1.2 Pressure control system

There are two kinds gauges are used in the sputter system, working in different pressure ranges. One is a low-vacuum gauges with a display range from 780 Torr to 0.1 mTorr, it can be used at the first step of vacuuming process. The second one is an

ion gauge with an analog display ranging from 10^{-3} to10^{-7} mTorr and used in high-vacuum to check if the base pressure of $1x10^{-5}$ mTorr is achieved. The high-vacuum ion gauge has to be turned off under low-vacuum to protect the functionality.

2.1.3 Vacuum system

There are two pumps in the sputtering process. The first is a rough pump that can be reach the vacuum from 760mTorr to 20mTorr, and the second is a turbo pump that will be used with the rough pump, and it can reach the high-vacuum of $1x10^{-5}$ mTorr,

2.1.4 Gas flow system

Mass flow controller (MFC) is used to control the gas flow delivered into the chamber and accurately controls the ratio among different gas ingredients. In this thesis, only Ar and O_2 are used in film deposition. Ar is the main gas for plasma generation, and O_2 has great influence on oxide film deposition.

2.1.5 Heating system

The temperature control system is made up of two thermal couples, a set of four quartz lamps and a temperature controller. One thermal couple is directly connected with the quartz lamps, and the other one is used to correct the temperature before sputtering, because the quartz lamps is set located above the sample holder, so the temperature is a little different between the quartz lamp and the sample holder. During heating process, the signal sensed by the thermal couple next to the lamp set would feedback to the controller to adjust the output power to the lamps.

2.1.6 RF plasma system

The power generator (13.56MHz) with one matching box, and the matching is used to adjust the impedance of the total network system for the minimum reflecting power.

2.2 Sample fabrication

The research of the RRAM is based on the Ti-ZrO_2-Pt MIM structure, but there are various processes to fulfill the investigation purpose at several research topic, including different process temperature, different thickness of the ZrO_2, different top electrode size. The fabrication processes would be described below respectively.

2.2.1 Basic structure

The structure of the sample with different processes of the ZrO_2 is illustrated in Fig. 2-2. Fig. 2-3 shows the process flow of the following steps. At first, the sample is cleaned by the RCA procedure, and then a 250-nm-thick SiO_2 is grown on 4-inch silicon wafer. The bottom electrode is deposited by a 20-nm Ti and 80-nm Pt, using the e-beam evaporation on SiO_2. After that, the oxidation layer is deposited by the radio-frequency sputter on the various processes. Finally, the top electrode layer is deposited by using the e-beam evaporation by the shadow mask pattern and the lithography.

2.2.2 RCA Clean

The RCA clean is the standard process to clean the silicon wafer before the

process steps. The purpose is for removing the contaminants from wafer, and the main steps are as followed. First, the wafer is submerged in the solution of 3:1 H_2SO_4:H_2O_2, for 10 min at around 80°C to remove organic contaminants from the surface of wafer, then in 1:100 HF:H_2O to etch chemical oxide produced in the previous step. It should be noted that each step was separated by DI water rinse for 5 min.

2.2.3 Growth of SiO_2

After RCA clean, 4-inch silicon wafers are sent into a furnace immediately for thermal oxidation, the surrounding environment is at 950°C for 30 min in O_2 and H_2 atmosphere. The wet oxidation is used by its high growth advantage, for the SiO_2 layer is only the role of the insulator layer, which is blocked the leakage current to the silicon base, and the thickness is to be expected around 250nm.

2.2.4 Deposition of bottom electrode

the bottom electrode is deposited by using the dual e-beam evaporation. First, a 20-nm Ti is deposited to be a adhesion layer, and then a 80-nm Pt is deposited on the in-situ Ti layer.

2.2.5 Deposition of resistive switching layer

A structure of ZrO_2 for resistive switching layer is fabricated. First, the ZrO_2 film is deposited by radio-frequency (RF) magnetron sputter system. During film deposition, each particular parameters of the working pressure, RF power, and gas flow were 10 mTorr, 150 W, and 2:1 Ar:O_2 with a total flow rate of 18 sccm. There are two respective factors that influent the ZrO_2, the factor is various depended on the

purpose we want to research, the description is as the following section.

2.2.5.1 Process temperature of resistive switching layer

First, the process temperature is considered, it is various from the room temperature (25°C) to 300°C based on the process deposition time is 60mins, and there are six different temperatures, 25°C, 100°C, 150°C, 200°C and 250°C respectively.

2.2.5.2 Process thickness of resistive switching layer

Second, the process deposition time is various from 30mins to 150mins based on the process temperature is 200°C, there are six different deposition time, 30mins, 60mins, 90mins, 120mins, 150mins respectively. The characteristics of these samples are investigated and discussed in chapter 3.

2.2.6 Deposition of top electrode

After the fabrication of resistance switching layer, the Ti top electrodes were prepared to form the structure of metal/resistive switching layer/metal. The Ti layer is deposited by the e-beam evaporation on ZrO_2 layer for 150nm, the top electrode is pattern by the shadow mask and the lithography.

2.2.6.1 Shadow mask

The top electrodes mentioned above are patterned by the shadow mask having

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the dot-shaped holes with diameters of 350, 250 and 150um, i.e. areas of $9.26x10^{-4}$, $4.91x10^{-4}$ and $1.77x10^{-4}$ cm^2, respectively.

2.2.6.2 Lithography

For the purpose of minus the size of the top electrode, it is used photo resistance to be the mask. The characteristic of this sample is used 60mins and 200°C. The process flow of the lithography is as following description in Fig 2-4. First, the positive photo resistance AZ4620 is used on the Photo Resist Spinner, the 1200rps for 5 seconds and 4000rps for 25 seconds. After that, the sample is put on the hot plate at 90°C and 5mins for soft bake. And then the mask that having the 10um x 10um square is exposed using the intense light for 45 seconds, this step is that the pattern can be print on the ZrO_2 layer. Finally, the sample is put in the AZ300 for 200 seconds to develop the pattern, and then rinse into the DI-water for 1 min. The thickness of the photo resistance should be around 2.1 um, and the next step is ready to deposit the top electrode.

The sample that has pattern is also deposited by Ti using the e-beam evaporation for 150nm, and then put it in the acetone for 1 min and rinse in the DI-water for 1 min. The purpose of this step is to lift-off for removing the photo resistance, so the top electrode is Ti can be sustained on the ZrO_2 layer, and the top electrode is 10um x 10um square.

2.3 Analyses and measurement

The analyses and measurement is used to do the research of this thesis, the description is following as next.

2.3.1 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is a microscopy technique that a beam of electrons is transmitted through an ultra thin specimen, interacting with the specimen as it passes through it. An image is formed from the electrons transmitted through the specimen, magnified and focused by an objective lens and appears on an imaging screen, a fluorescent screen in most TEMs, plus a monitor, or on a layer of photographic film, or to be detected by a sensor such as a CCD camera.

In material science/metallurgy the specimens tend to be naturally resistant to vacuum, but must be prepared as a thin foil, or etched so some portion of the specimen is thin enough for the beam to penetrate. Preparation techniques to obtain an electron transparent region include ion beam milling and wedge polishing. The focused ion beam (FIB) is a relatively new technique to prepare thin samples for TEM examination from larger specimens. Because the FIB can be used to micro-machine samples very precisely, it is possible to mill very thin membranes from a specific area of a sample, such as a semiconductor or metal. The

2.3.2 Electrical measurements

The electrical properties are measured, Agilent 4155C semiconductor parameter analyzer, E5250A low leakage switch and Agilent 81110A pulse/pattern generator, they are all controlled by a desktop computer with the Agilent VEE software.

The electrical measurements in this thesis were divided into several parts, consisting with endurance, pulse, retention, and stress. Those are for the purpose of memory device application and the fundamental switching properties.

2.3.2.1 Endurance test

Endurance is the key performance that memory devices must endure a large number of switching cycles to meet the operation requirements in many applications such as random access memory (RAM) and solid state disk (SSD) which both need many data write-in operation without any failures. In other words, this factor is the sample that whether it will be steady or not.

The tests of endurance are carried out by the Agilent 81110A, and the environment is at room temperature.

2.3.2.2 Pulse test

Although the Endurance test is important, but it is only statistic test, in a real commercial product, the switching is operated by the pulse. The shorter pulse width, the quicker write/erase speed can be operated, so the product is more attractive to the costumers.

The pulse is generated by the Agilent 81110A, which pulse width can be operated from the 6.65ns to 999ms.

2.3.2.3 Retention test

Retention is an essential performance for nonvolatile memory devices, standing

for the capability of retaining memory data for a long period without any data loss. For a commercially available nonvolatile memory product, the performance of retention is requested at least 10 years.

The retention test is carried out by the following description. First, the memory device is switched into on-state or off-state at room temperature r by DC bias. Next, the data state is read by applying a 0.3 V reading bias that small enough in order not to change the memory state, the sample will be read every once in a period of time.

2.3.2.4 Stress test

The stress test or non-destructive readout test is also an important factor for nonvolatile memory devices, in which memory data could not be changed in data reading process, and it is also a basic demand for nonvolatile memories. On the other hand, if random access memories have the property of non-destructive readout, the control circuit will not have to refresh which takes additional clock cycles to write the data back, giving rise to the increase in the operation speed.

The stress test is implemented by Agilent 4155C. After switched to on-state or off-state, the device is applied with 0.3 V bias for a long period to observe if the state would keep the same. If it can last for a long time, it can be said that the sample would not be disrupted by the other circuit when it is combine with other circuit in the commercial products.

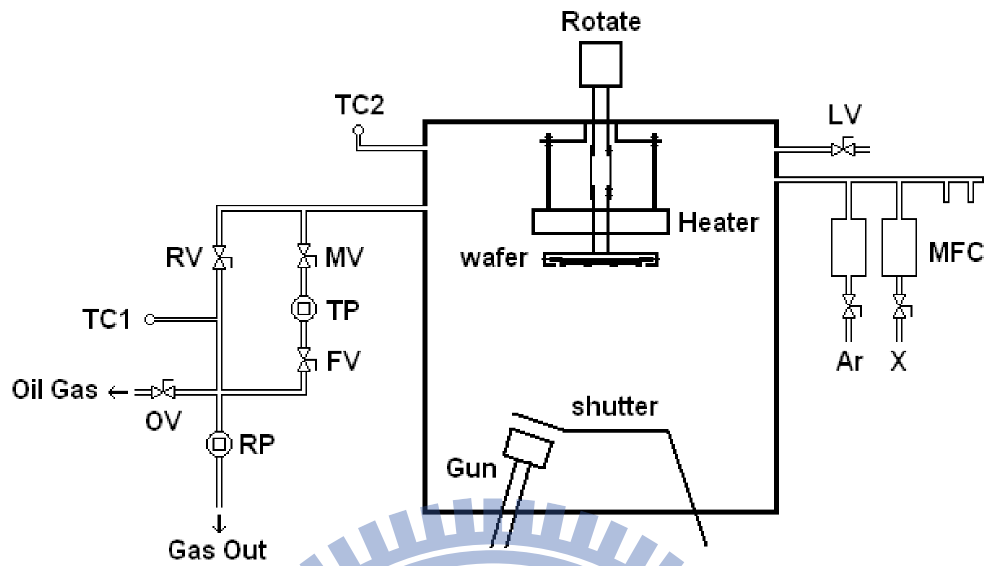


Fig. 2-1 The illustration of Radio-frequency magnetron sputter system

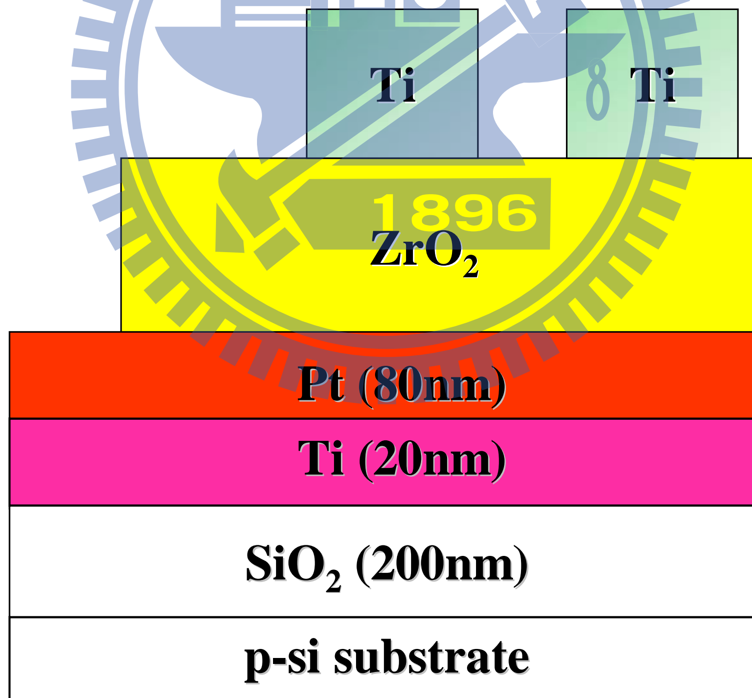


Fig. 2-2 The basic structure of the Ti-ZrO_2-Pt RRAM

Ti : E-beam evaporator with

shadow mask(350um,250um.150um)

ZrO_2 (RF sputter, $Ar:O_2$=12:6 ,

working pressure=10mtorr)

Process temperature:
25°C,100°C,150°C,200°C,250°C

Deposition time at 200°C :

30mins,60mins,90mins,

120mins,150mins

Pt/Ti : E-beam evaporator

SiO_2 : wet oxidation

Cleaned Si substrate (100)

Fig. 2-3 The process flow of making the Ti-ZrO_2-Pt RRAM

■Lithography: 10um diameter

Photoresistance:AZ4620
1200rps for 5s and 4000rps for 25s

↓

Soft bake : 90°C for 5mins

↓

Exposure on mask : 45s

↓

Develop the pattern : AZ300 for 200s

↓

Rinse in DI-water : 2mins

↓

Sputter Ti :150nm

↓

Lift-off : Acetone for 1 min and
DI-water for 1 min

Fig. 2-4 The process flow of lithography on top electrode

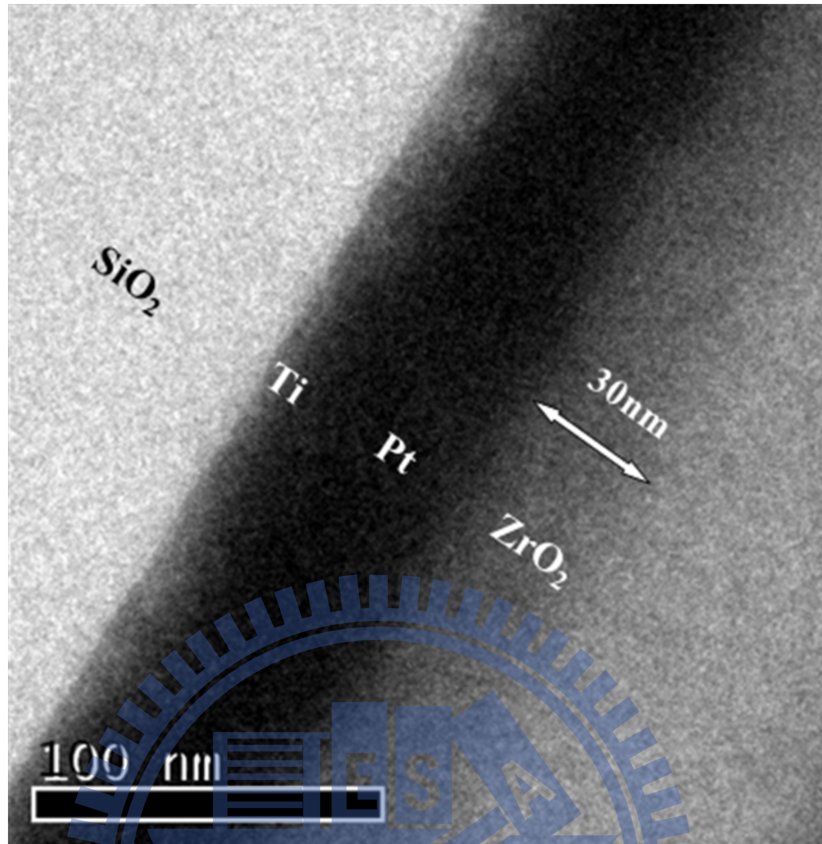


Fig. 2-5 TEM of ZrO_2 (60mins,200°C)

Chapter 3

Results and discussion

3.1 Various ZrO_2 process temperatures

In this section, the temperature of the process will be changed when the ZrO_2 is sputtered on the Ti/Pt bottom electrode, and the most suitable temperature for the experiment will be determined. The performance of the RRAM will also be described, including high speed switching pulse, high reliability endurance, stress and the retention.

3.1.1 Temperature effect

The resistive switching behavior is found in all kinds of temperature process that sputter ZrO_2, including room temperature (25°C) to the high temperature that RF sputter machine can stand (300°C). Although all of the temperature can be switched, there are still some different performances between the different temperatures. As the following description, the forming voltage、current of on-state and off-state、endurance、dynamic pulse switch will be showed some different.

At first, the ZrO_2-base RRAM is showed good characteristic [19][26], but the temperature effect is not described, so the purpose is to know what temperature is the most suitable for the experiment in the future. The ZrO_2 is based on the 60mins sputtering time, so the thickness is the same, and the changing factor is the process temperature. It can be seen that all the temperature (25°C, 100°C, 150°C, 200°C,

250°C) has the forming voltage as shown in Fig. 3-1~ Fig. 3-6 , and the initial resistance in Fig. 3-7 that pick up the point at 0.3V can be known that (100°C, 150°C, 200°C, 250°C) is almost not changed, and the 25°C, 300°C are much lower, because the thickness is the same, so the difference of this characteristic is major at the point of the process temperature, although the XRD cannot show too much different of the sample for the lattice factor is all amorphous, but we still can find the most suitable temperature as the following description by checking the electrical property.

First, all the sample is given a high voltage as high as 5V and the 5mA compliance current to forming the sample, this purpose is to turn on the filament that included interface layer and bulk layer. After that, the sample is given a negative 2.5V to turn the state into the off-state, and then given a positive 1.5V to turn the state into the on-state, there is no need to limit the current for the interface layer can be a good compliance current resistance [26], it called self-compliance when switching the device, it's one of a big advantage that RRAM using the structure of Ti top electrode on the ZrO_2.

3.1.2 I-V curve

The I-V curve of the different temperature is shown in Fig. 3-8~ Fig. 3-12, and the on-state and off-state current is also shown in Fig. 3-13. As the plot shown, the on-state current is almost the same, the value is around 1mA. But at the condition of 200°C, the current is steadier for its variation is smaller compared with other condition, and the off-state current is a little bit smaller than other condition. It's a advantage of this condition for the ratio will be bigger, and the smaller current, the better process for the RRAM when it is made on the smaller scale process as small as

the current 45nm process.

3.1.3 Statistic endurance test

The more cycles sample can operate, the more stability the sample can operate, for the DC sweep is the basic electrical property. Because all of the conditions can be successfully switch at bipolar mode (positive turn on and negative turn off), and the next step is to know what kinds of condition can have the best stability, the sample is to be test on the statistic endurance test, which is continuous switching until the sample is almost breakdown. The test method is at the first cycle to the 100th cycle, the data will be record, and after the 100th , all the data will be record the last 10 cycles in every 100 cycles. As the endurance plots shown in Fig. 3-14~ Fig. 3-18, the results show that the 200°C also has the best endurance ability in the table 3-1, and it can be achieved over 10000 cycle times, the performance is much better than other conditions, in other words, its stability is the best.

3.1.4 Dynamic pulse test

After the statistic endurance test, it should be know that whether the dynamic pulse test is as good as the statistic test, because the real device is operated in the pulse mode. The dynamic pulse test is operated in the Aiglent 81110A, the measure method is that after the sample is given a pulse, the read voltage is at 0.3V, and continuous read 5 times in the Fig. 3-19. The sample is focus on the condition of 200°C for its DC sweep is better among all the conditions. The test is operated at 10ns, 20ns, 50ns, which is much faster than the current flash memory for its speed is around

us level [78][79].

All of the sample is on the situation of +6V and -3V for the turn on and turn off voltage, the only changing factor is the pulse width. At first, the sample is test at the 10ns in the Fig. 3-20, the soft error can be seen during the switching, for the shorter pulse width, the shorter reaction time the device can be operated, so the turn-on and turn-off mechanism in the filament is not operated completely, that is the reason the performance of the shorter pulse width is not as good as the longer pulse width as following description.

The sample is operated at 20ns, but its performance is also showed that the soft error also appears in the window in the Fig. 3-21 After that, the sample is operated at the 50ns in the Fig. 3-22, and it can shown that at this speed, the window is clean during the 1000 cycle times, there is no soft error during the window, it's an improvement [74][75], on the other hand, the DC state will keep the same during the pulse test in Fig. 3-23. It showed that the Ti-ZrO_2-Pt RRAM structure is a potential next generation non-volatile memory, which is much faster than the flash memory.

3.1.5 Stress test

The 200°C, 60mins–base ZrO_2 is measured its stress ability, and the state is not change during the stress test that using the 0.3V to read the data. The on and off state are not changed during the 10000s stress test in Fig. 3-24. On the other hand, after the pulse test 1000 cycle times, the on-state and off-state will be lifted compared with the original stress test, for it stand the pulse voltage, but the state can still be keep the same.

3.1.6 Retention

Fig. 3-25 is the test for the retention, and it shows that the on-state and off-state can be kept until 10^6s at room temperature environment.

3.2 Different process thickness of ZrO_2

3.2.1 The motivation of different thickness

The mechanism of Ti-ZrO_2-Pt structure is bases on the $R_{rupture}$ layer is the major part of the filament that switching the on-state and off-state [19][26]. The Fig. 3-26 is showed that after depositing Ti top electrode, there will be a series resistance of interface layer that consist of TiOx and ZrOy, the thickness of this layer is determined by the thickness of the Ti top electrode, it should not related with what the thickness of the ZrO_2, and after forming process, the bulk layer is always conductivity no matter what the situation is on-state or off-state. During the off-state condition, the rupture layer will be appeared for the joule-heating effect caused by the oxygen ions, let the ZrOy become ZrO_2, and its resistance is much higher than the bilk layer for the bulk is meta-like, and the rupture layer will be insulator-like during the off-state condition, so the voltage of all the filament should be mostly drop at the rupture layer during the off-state. Even if the thickness is changed, because the resistance of the rupture layer i is much bigger than the bulk layer and interface layer, so the voltage drop should still be drop at the rupture layer, hence the off-state current should still be maintain the same or the difference is very few. If the state is on-state, the on-state current should also maintain the same for the bulk is metal-like, its resistance is much smaller compared with interface layer in the filament, so the resistance of the filament is not

affect by the different length of the bulk.

3.2.2 Electrical properties

3.2.2.1 Forming voltage

The Fig. 3-27~ Fig. 3-31 show that the forming voltage will be affected by the different thickness of the ZrO_2, the more thicker the ZrO_2, the larger the forming voltage needed to be used for the resistance is positive related with the thickness of the ZrO_2 as in the Fig. 3-32. After forming, the insulator-like ZrO2 bulk will be transformer into the metal-like ZrOy for the O^{2-} ions can be absorbed by Ti top electrode when using the positive voltage to forming.

3.2.2.2 I-V curve

The sputtered time is 30mins, 60mins, 90mins, 120mins, 150mins individually. The 30mins sample is too thin that if the span voltage is beyond -1.5V~+1V, it will be breakdown, so it is not in the following discussion. Fig. 3-33 shows that all of the condition is swept in the range of the -2.5V~+1.5V after forming, the negative voltage is for turn-off and positive one for turn-on. In table. 3-2, the turn-on voltage and turn-off voltage is almost the same for the difference is small enough for any sputtering time, and then the Fig. 3-34 is showed that the on-state current and off-state current is also almost the same. The result is showed that the switching part should be limited in a small part as the motivation mentioned above, because if the bulk is also involved in the off-state, the current should be decreased very much when the

thickness is sputtered-150mins compared with the sputtered-60mins. And the turn-on and turn-off voltage is the same in different conditions, so the characteristic of the interface layer and rupture layer can be known the same in the filament. In other words, the switching part is major in the rupture layer for the voltage will most drop at this part during the switching as the Fig. 3-35 showed.

3.3 Various voltage bias sweeping spans

3.3.1 Three kinds of spans

After knowing the different thickness characteristic, we can confine the major switching part of the filament in the middle of the interface layer and bulk layer, the sample is switched in the rupture layer. And then the sample is switched in three different spans, the three kinds of spans are -2.5V~+1.5V, -2.5V~+2.0V, -3.0V~+2.0V separately. In order to understand the characteristic of the rupture layer to be clearer, the performance will be changed by using the three different spans. Fig. 3-36~ Fig. 3-39 is showed the basic I-V curve of all the conditions. The static plot about the current of on-state and off-state is in the Fig. 3-40, and the turn-on and turn-off voltage is in the Fig. 3-41, we only pick up the Ti-ZrO_2 (200oC, 60mins)-Pt for the trend is the same in other temperature

First, Fig. 3-42 shows the span of -2.5V~+1.5V, -2.5V~+2.0V is compared, as the positive voltage increased, the turn-off voltage is also increased for the more positive voltage absorb the O^{2-}, the more negative voltage used to let the O^{2-} migrate toward the rupture layer to transfer the ZrOy become ZrO_2, so the filament can be broken by the joule heating within the rupture layer, hence the voltage is increased.

The current will also be increased for the larger positive voltage is used, the more O^{2-} be absorbed, and if the negative span is not changed, the amount of O^{2-} can be migrated into the rupture layer is the same, so the amount of joule heating is the same, hence the current is increased for the turn-on capability is larger than the turn-off capability when the span is compared with -2.5V~+2.0V and -2.5V~+1.5V.

Second, the -2.5V~+2.0V span compared with the -3.0V~+2.0V in the Fig. 3-43. The turn-on voltage will be increased when the larger negative voltage in used, because the more O^{2-} migrate toward the rupture layer, the more O^{2-} has to be absorbed to let the filament can be formed. The current will be also decrease for the power of the joule heating is much larger at larger negative voltage. The Fig. 3-44 shows that the different spans will affect the voltage and current at on-state and off-state.

3.3.2 Various ZrO_2 process thicknesses combine with three kinds of spans

Even in the three kinds of different spans, the on-state and off-state current is still keep almost the same, as the motivation we predict. Hence the switching part is at the rupture layer that proved again for its resistance is the biggest within the filament, so the voltage drop will at there mostly.

3.4 Size effect of Ti top electrode

3.4.1 Effect of forming current compliance on the ZrO_2-based devices

Above all of the description, the forming current is all set at 5mA, but if the

forming current is changed as in the Fig. 3-47, the forming current is 0.1mA, 0.5mA, 1mA, 5mA, 10mA separately, the on-state and off-state current will become bigger as the forming compliance increased, and the V_{on} and V_{off} has also the larger value when the forming becomes larger. In other words, the curve will become wider as a small tree grows. Hence, the plot can be predicted that the characteristic of the filament will be affected by different forming current, and if the current compliance is the same, the characteristic of the filament will be the same, like the size of the filament is the same, and vice versa.

The various current compliances can let the current become much smaller compared with the bigger compliance; hence maybe the future work can use the smaller compliance in the research. The other part of this section will use the same current compliance to ensure the filament can keep the same in the size effect research.

3.4.2 The motivation of size effect

The motivation of size effect can let us know whether the top electrode area will affect the current when the situation is turn-on or turn-off, and the Fig. 3-48 shows that the filament is supposed to be the trap-detrap at the interface state or filament-like faucet shape[74][69], because the I-V curve shape of the self-compliance is the same in both models in the figure, but there will be different when it talks about the trend of the on-state and off-state current. And we can use this to improve that it is filament-like as the above section described.

First, if it is the filament-like faucet shape, the on-state current should be the

same no matter what the area of the top electrode, because the filament is localize in a small area of the middle of the interface and bulk layer. And when the condition is turn-off state, the filament will be breakdown by joule heating, and the resistance of off-state has to calculate the whole bulk for the resistance is uniform [68], so the resistance of the off-state will be related with the area for the basic R=ρ*L / A (ρ: Conductivity, L: length of resistance, A: area of resistance). In other word, when the top area is scale down, the resistance of off-state should be increase, and the off-state current should be also decrease. The above phenomena should be obvious especially the top area scald down much by the lithography, because the minimum area of the shadow mask is only $1.77x10^{-4}$ cm^2, but the lithography can be scale down at about 10^{-6} cm^2. So the turn-on current will be the same, and the turn-off current will be decrease related with the decreasing top electrode.

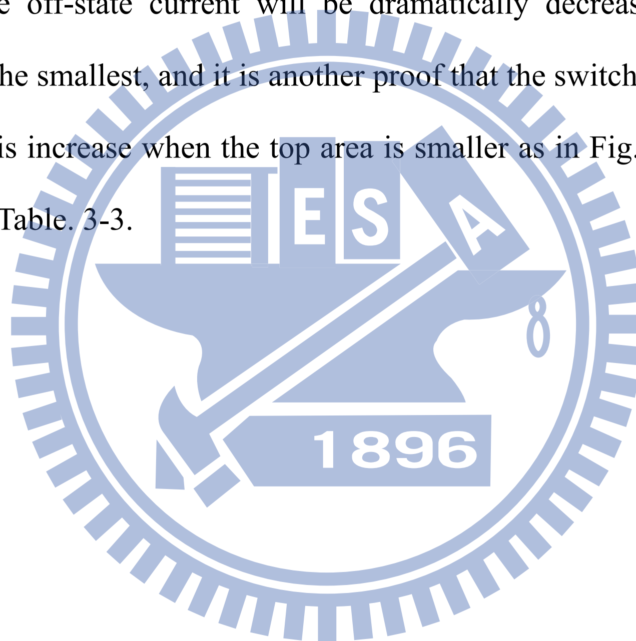
Second, if it is trap-detrap like at interface, the on-state and off-state current will both be decreased when the area of the top electrode area is decreased. For the basic R=ρ*L / A (ρ: Conductivity, L: length of resistance, A: area of resistance), resistance will be increased as area is decreased.

3.4.3 Electrical properties

The basic I-V curve of the different diameters is shown in the Fig. 3-49,endurance test is in the Fig. 3-50 and the Fig. 3-50 shows the on-state current is the same in the all kinds of various diameters situation, and the off-state current is decreasing, so this step can be proved that the on-state current is filament-like as the above assumption described. Fig. 3-51 shows that the Von will be also increased for the more smaller current in the off-state, the more voltage has to be used to let the filament can connect

to form a filament.

After that, we want to know the filament at the situation of off-state, the I_{off}, the power (Power = I_{off} x V_{off}) at the point I_{off}, V_{off} in Fig. 3-52~ Fig. 3-54, and three factors are the same, so we can predict that the breakdown situation is the same. In other words, the joule-heating situation in the filament is the same, so the characteristic of the filament at on-state is the same no matter what the area of the top electrode; it is suitable for the filament-like faucet model as in the Fig. 3-55. In another hand, the off-state current will be dramatically decreasing when the top electrode area is the smallest, and it is another proof that the switching is filament-like, so the resistance is increase when the top area is smaller as in Fig. 3-56. The sum up table is shown in Table. 3-3.



	Forming Voltage (V)	DC sweep			
		On state at 0.3V	Off state at 0.3V	On/Off Ratio at 0.3V	Endurance
		Current (mA)	Current (μA)	Average	Cycle times
25°C	2.5~4	1.21	33.3	22.8	2200
100°C	4~5	1.95	11.7	110	900
150°C	4~5.5	1.64	5.16	66	4000
200°C	4~5	1.04	4.53	114	10599
250°C	4~6	1.55	14.3	96	6100

Table. 3-1 The performance of all kinds of ZrO_2 process temperature

ZrO_2 (mins)	Forming voltage (V)	Turn-on voltage (V_{on})	Turn-off voltage (V_{off})
		-2.5V~1.5V	-2.5V~1.5V
60	3.5~4.8	0.9	-1.5
90	5~5.5	0.9	-1.4
120	4.5~6.8	0.85	-1.45
150	7~11	0.85	-1.5

Table. 3-2 The turn-on voltage and turn-off voltage

The diameter of the top electrode	On-state current (A)	Off-state current (A)	Turn-on voltage (V_{on})	Turn-off voltage (V_{off})
350um	7.31×10^{-4}	7.31×10^{-4}	0.93	0.68
250um	6.62×10^{-4}	5.65×10^{-5}	1.02	0.72
150um	6.44×10^{-4}	2.89×10^{-5}	0.88	0.68
10um	9.73×10^{-4}	5.53×10^{-6}	0.97	0.87

Table. 3-3 The turn-on voltage and turn-off voltage

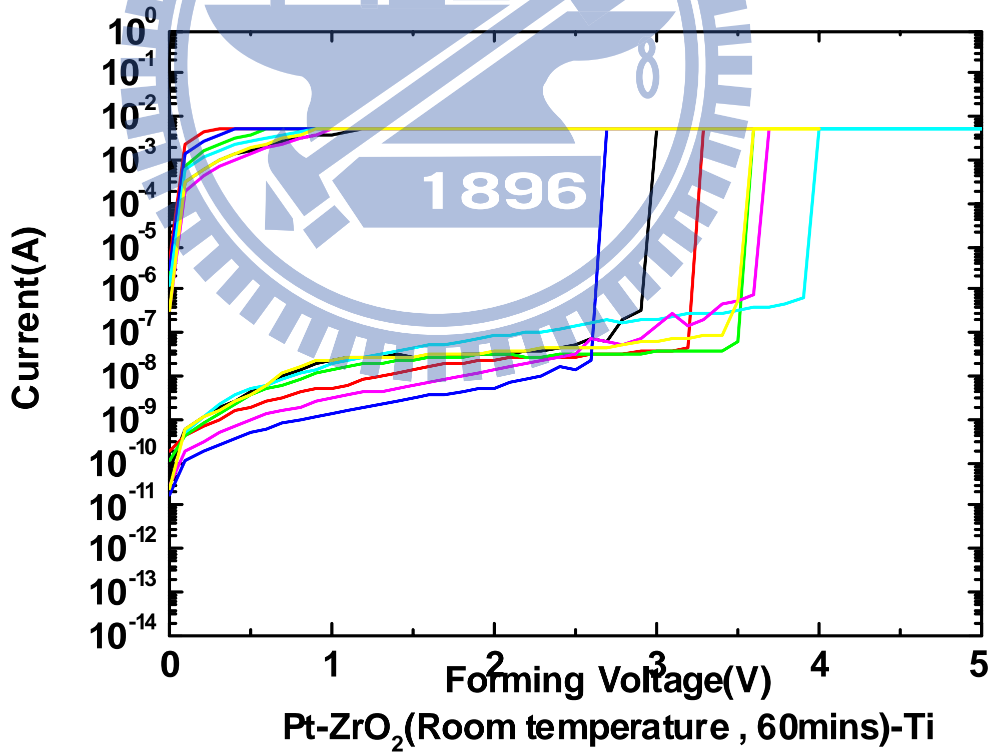


Fig. 3-1 Forming voltage of Ti/ZrO_2/ Pt structure with process temperature of 25°C.

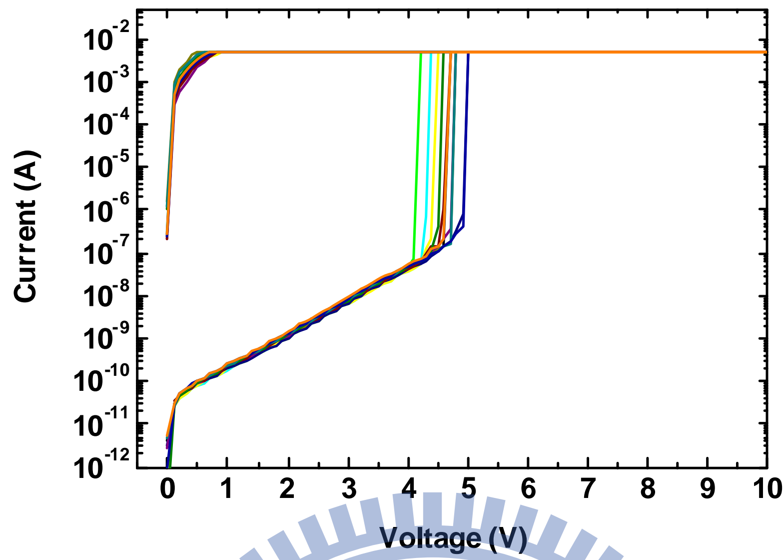


Fig. 3-2 Forming voltage of Ti/ZrO_2/ Pt structure with process temperature of 100^oC.

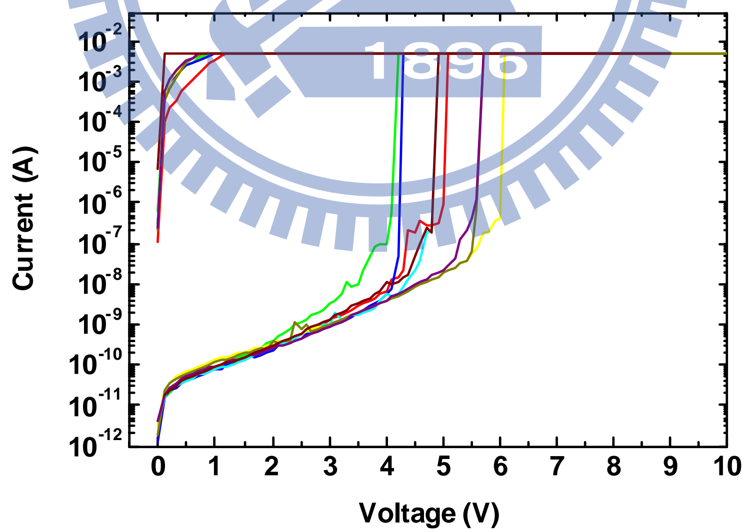


Fig. 3-3 Forming voltage of Ti/ZrO_2/ Pt structure with process temperature of 150^oC.

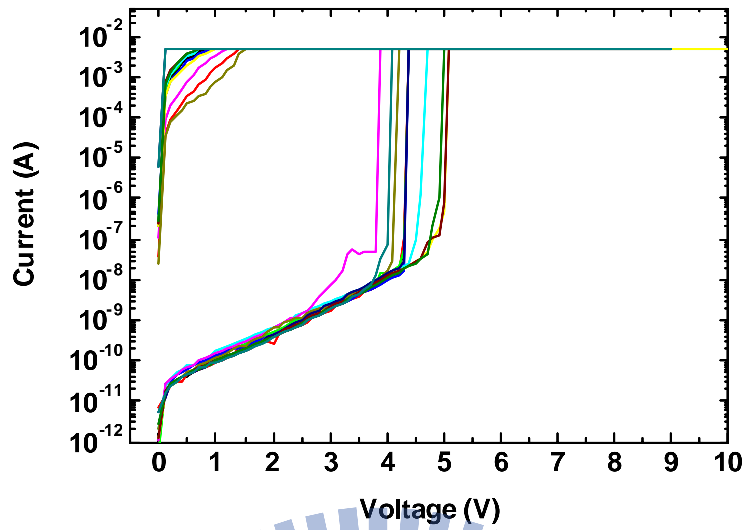


Fig. 3-4 Forming voltage of Ti/ZrO_2/ Pt structure with process temperature of 200^oC.

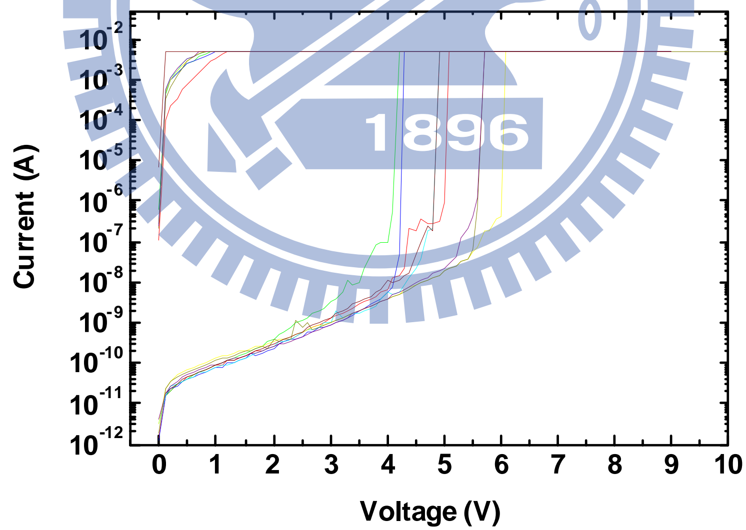


Fig. 3-5 Forming voltage of Ti/ZrO_2/ Pt structure with process temperature of 250^oC.

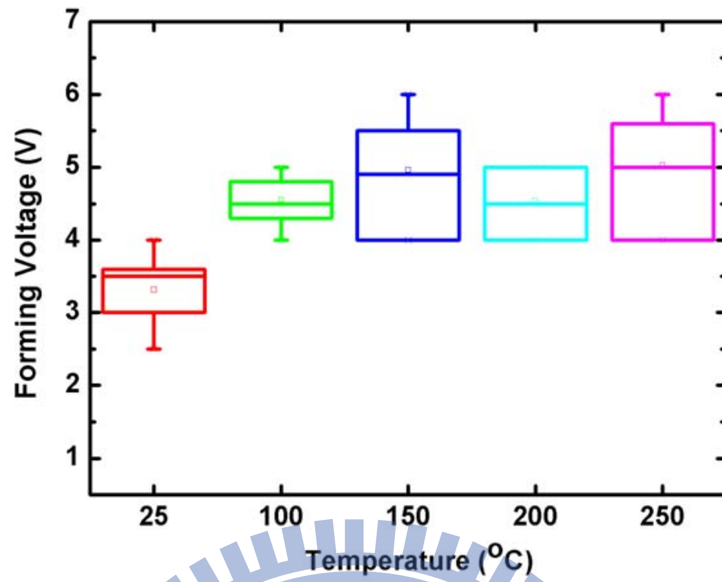


Fig. 3-6 Forming voltage of various ZrO_2 process temperature

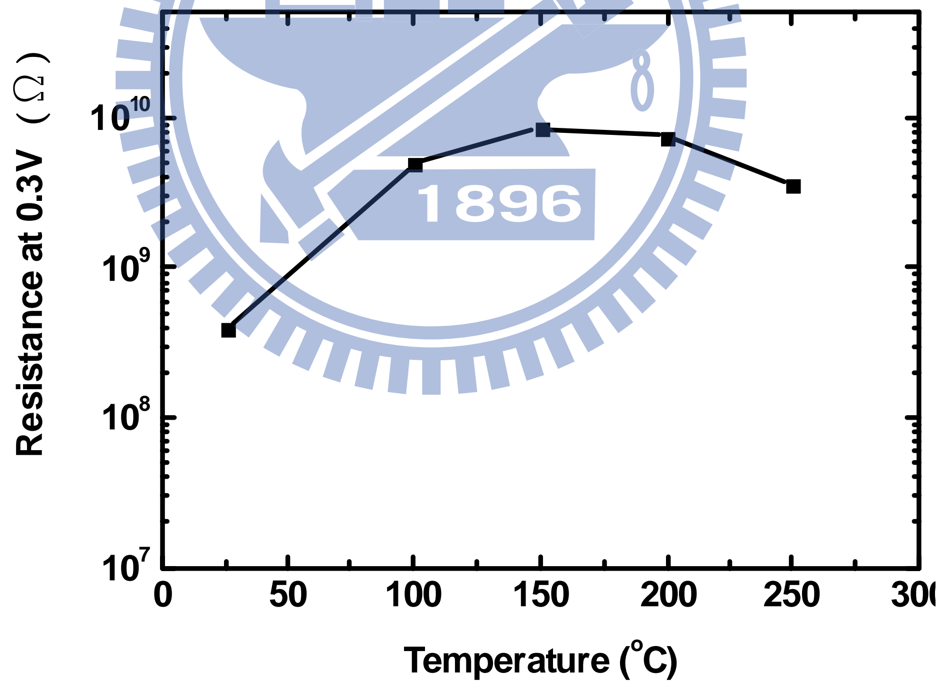


Fig. 3-7 Initial resistance of all kinds of temperature

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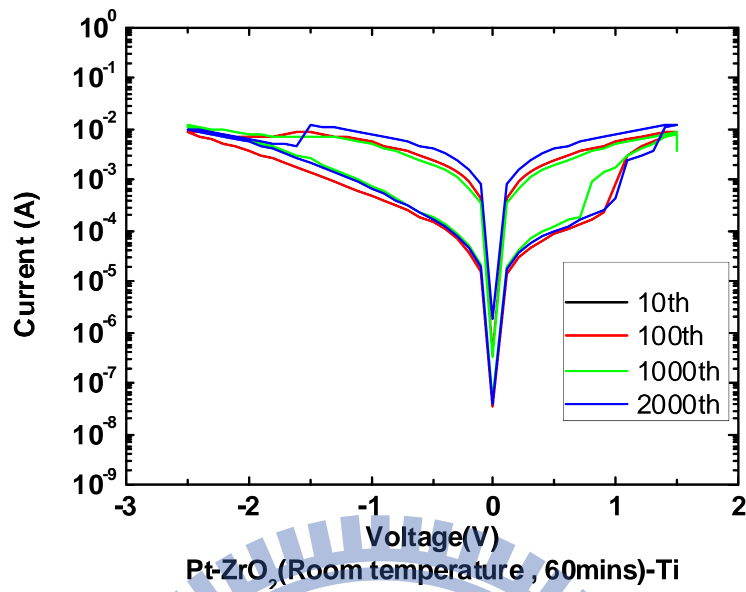

Fig. 3-8 I-V curve of $Ti/ZrO_2/ Pt$ structure with process temperature of 25°C.

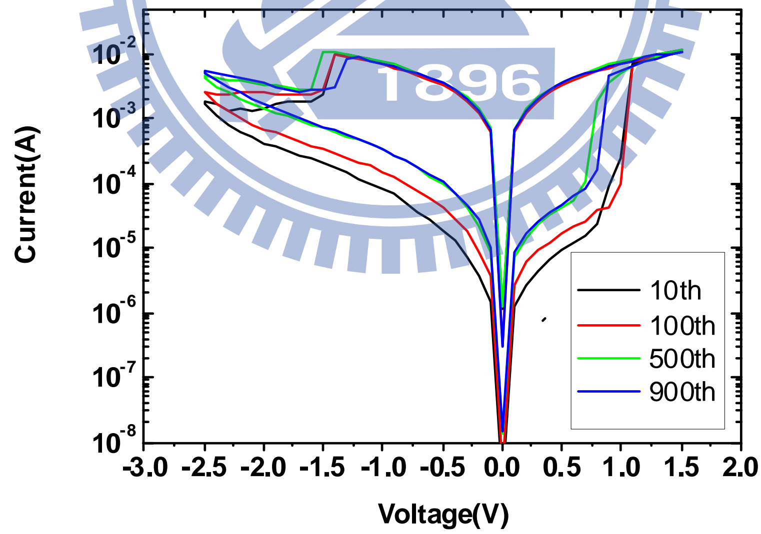

Fig. 3-9 I-V curve of $Ti/ZrO_2/ Pt$ structure with process temperature of 100°C.

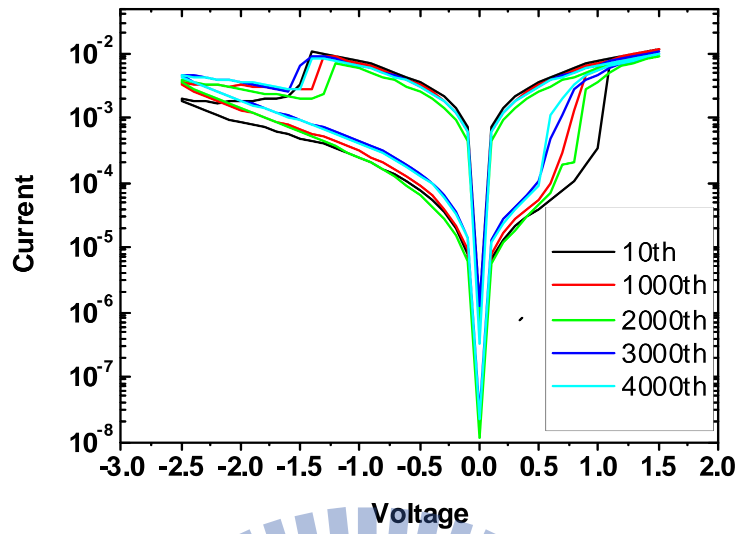

Fig. 3-10 I-V curve of Ti/ZrO_2/ Pt structure with process temperature of 150°C

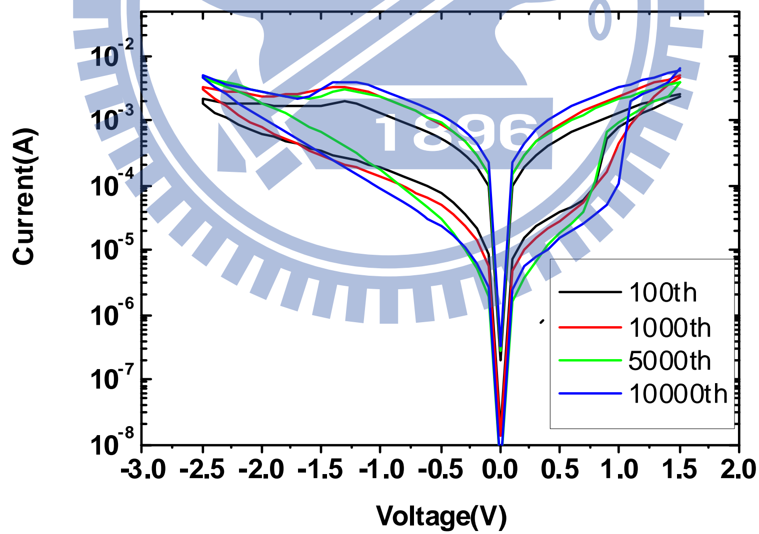

Fig. 3-11 I-V curve of Ti/ZrO_2/ Pt structure with process temperature of 200°C

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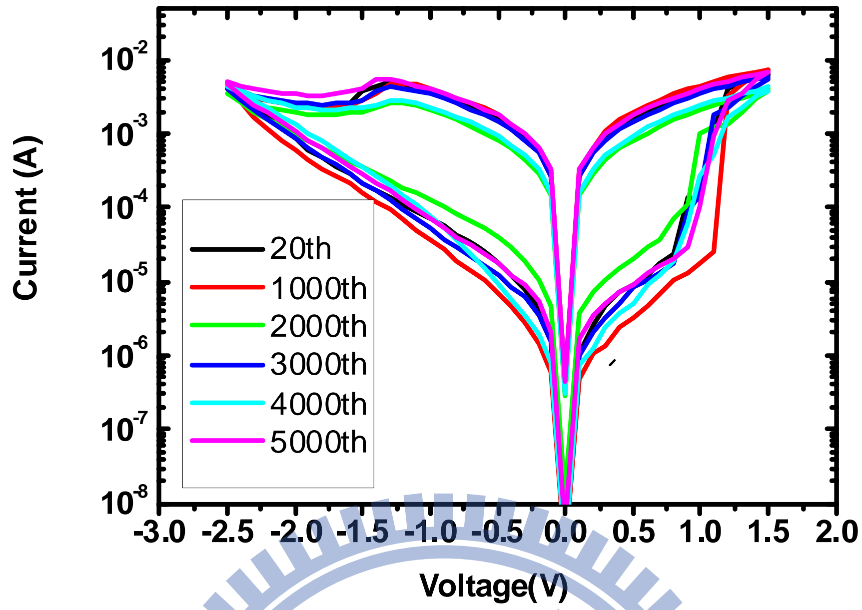


Fig. 3-12 I-V curve of Ti/ZrO_2/ Pt structure with process temperature of 250°C

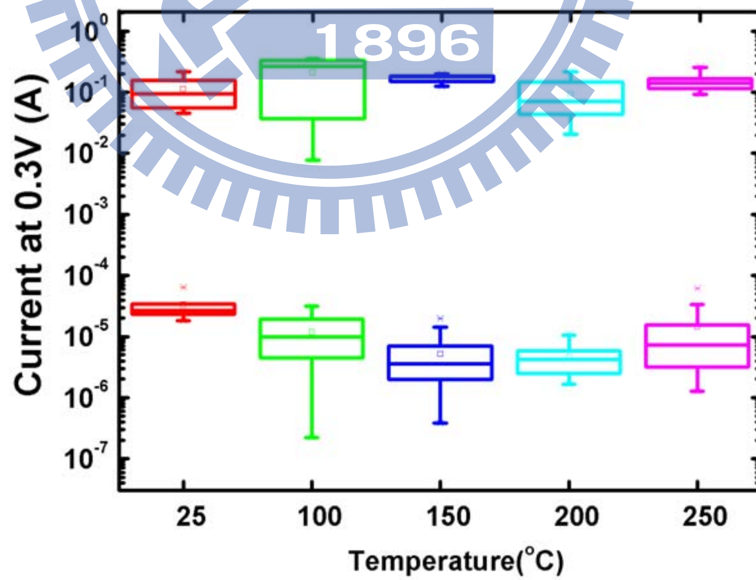


Fig. 3-13 On-state and off-state current of various process temperature

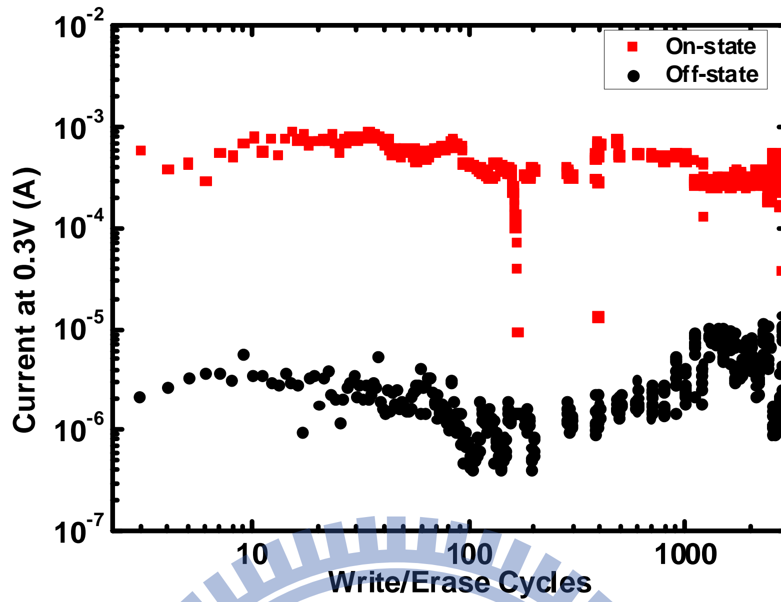


Fig. 3-14 Endurance of $Ti/ZrO_2/Pt$ structure with process temperature of 25°C

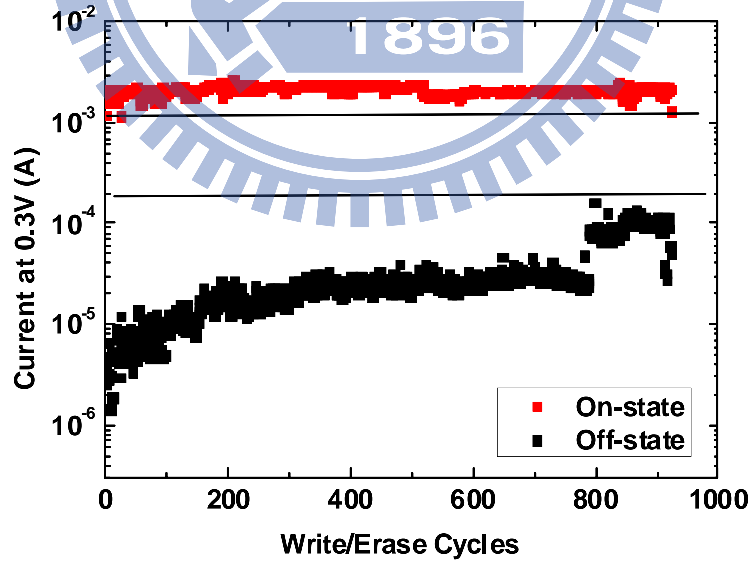


Fig. 3-15 Endurance of $Ti/ZrO_2/Pt$ structure with process temperature of 100°C

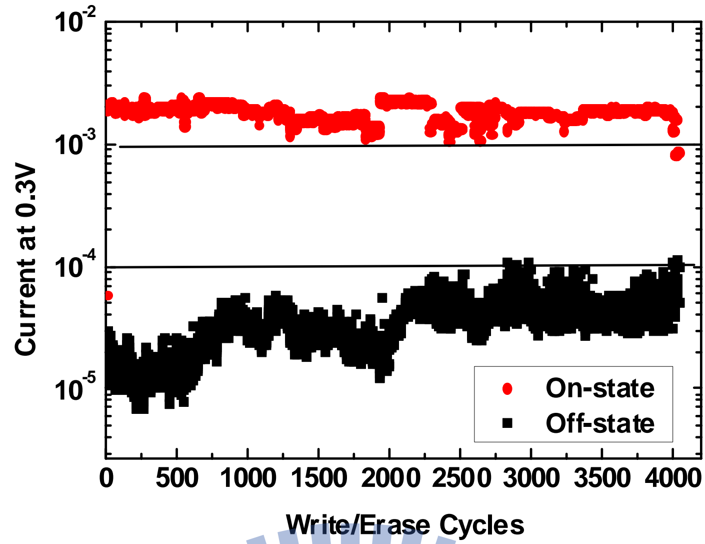


Fig. 3-16 Endurance of Ti/ZrO_2/ Pt structure width process temperature of 150°C

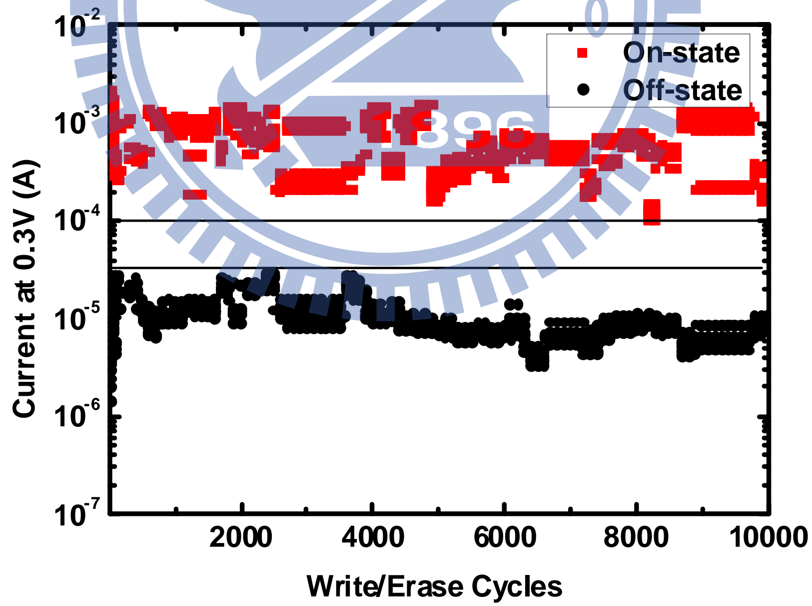


Fig. 3-17 Endurance of Ti/ZrO_2/ Pt structure with process temperature of 200°C

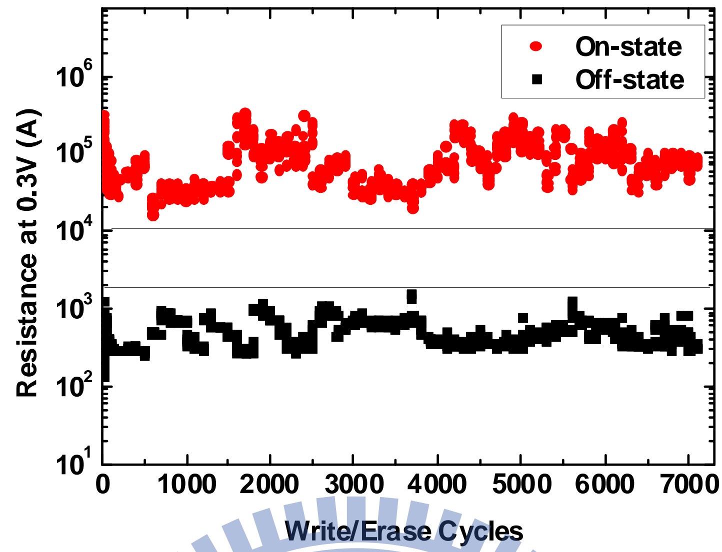


Fig. 3-18 Endurance of Ti/ZrO_2/ Pt structure with process temperature of 250°C

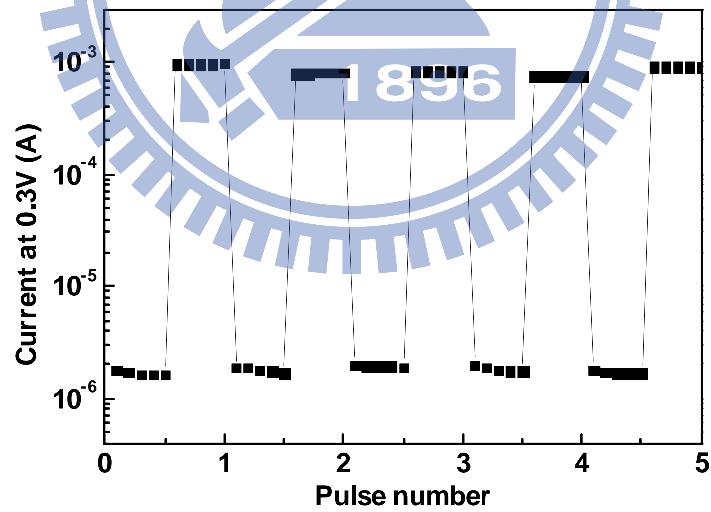


Fig. 3-19 The pulse is read at 0.3V for continuous 5 times

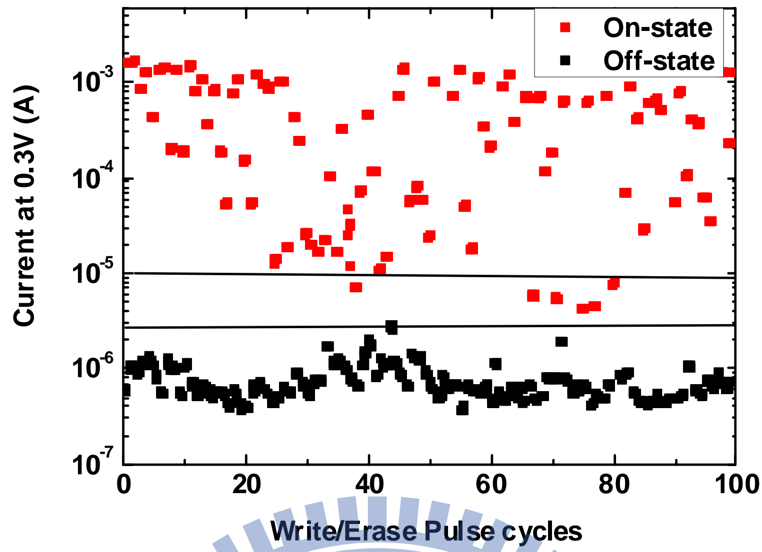


Fig. 3-20 Pulse width with 10ns of Ti/ZrO_2/ Pt structure with process temperature of 200°C

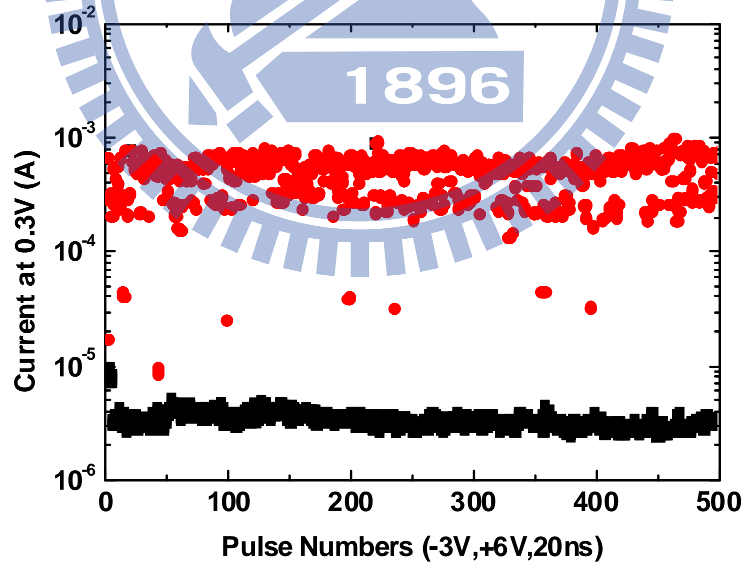


Fig. 3-21 Pulse width with 20ns of Ti/ZrO_2/ Pt structure with process temperature of 200°C

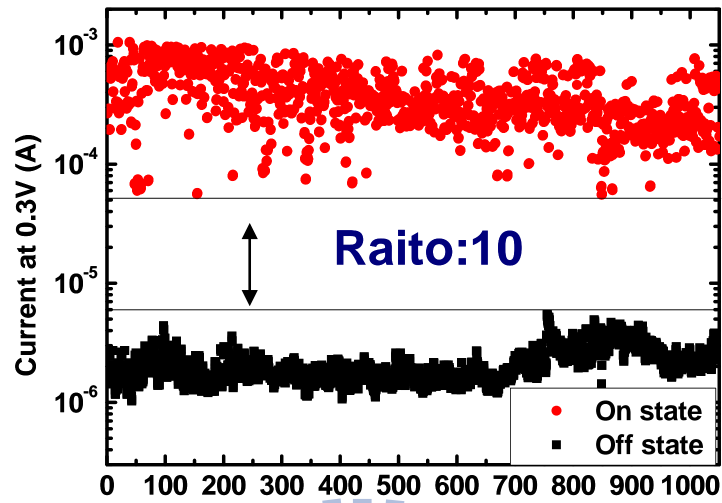


Fig. 3-22 Pulse width with 50ns of Ti/ZrO_2/ Pt structure with process temperature of 200°C

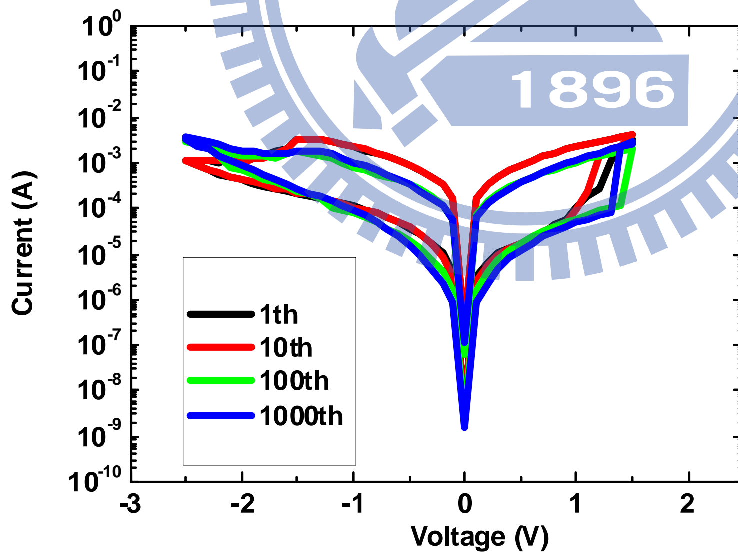


Fig. 3-23 Switching after pulse width with 50ns of Ti/ZrO_2/ Pt structure with process temperature of 200°C

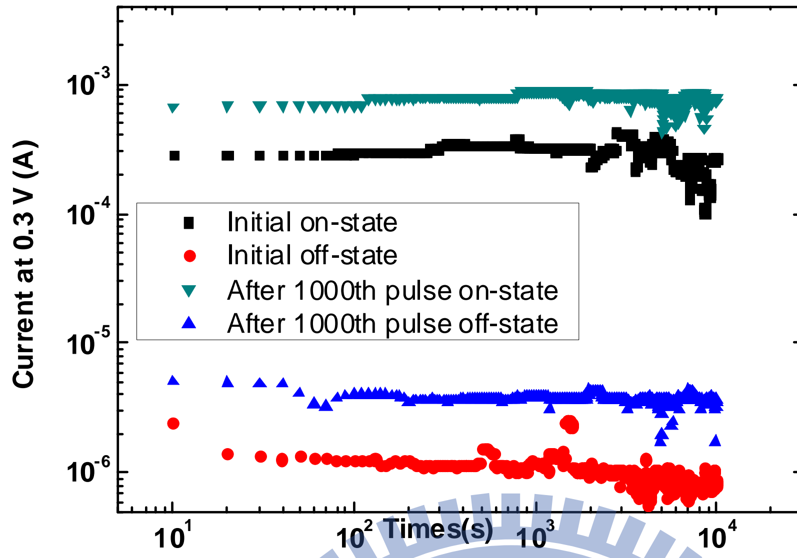


Fig. 3-24 Stress test of Ti/ZrO_2/ Pt structure with process temperature of 200°C

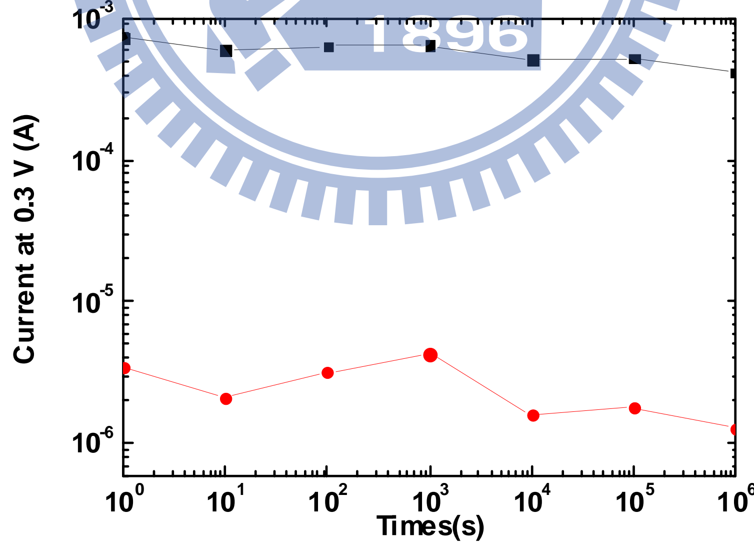


Fig. 3-25 Retention test of Ti/ZrO2/ Pt structure with process temperature of 200oC

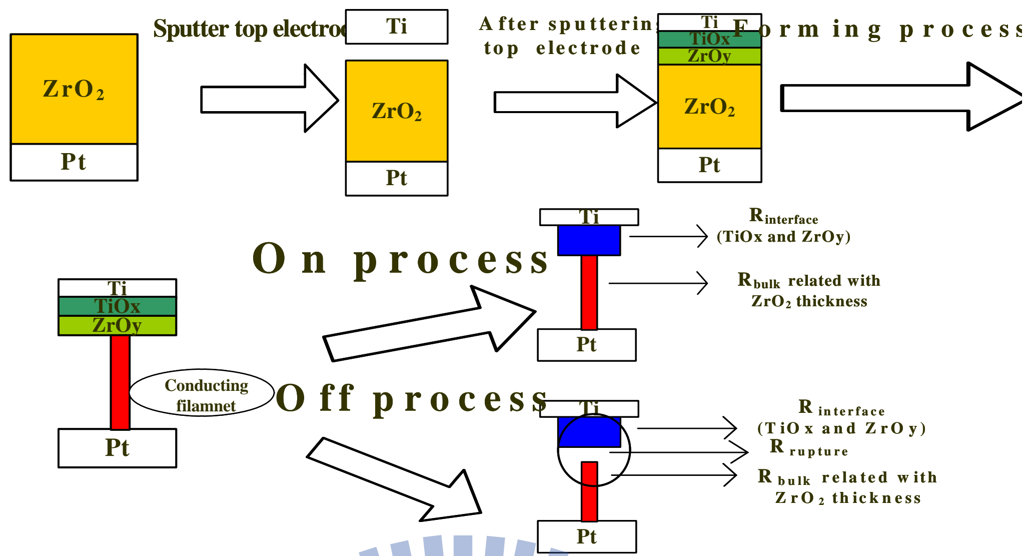


Fig. 3-26 The series resistance of Ti top electrode on the ZrO_2 film

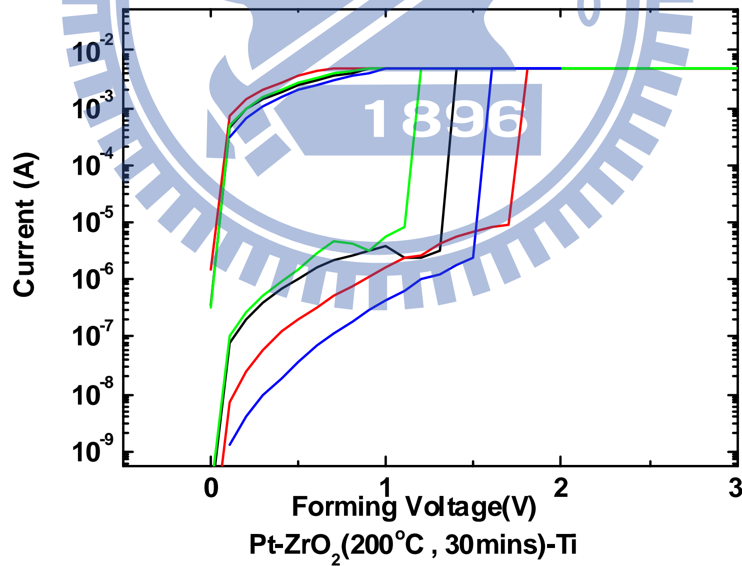


Fig. 3-27 Forming voltage of Ti/ZrO_2/ Pt structure with process thickness of 30mins

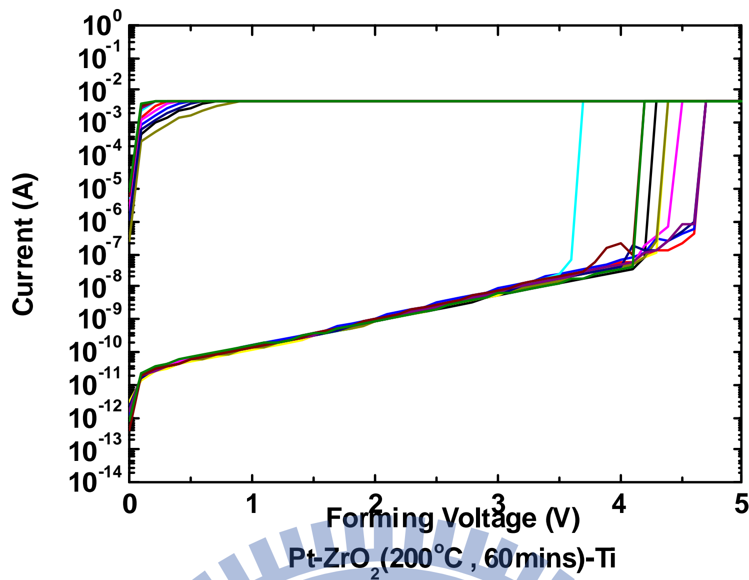


Fig. 3-28 Forming voltage of Ti/ZrO_2/ Pt structure with process thickness of 60mins

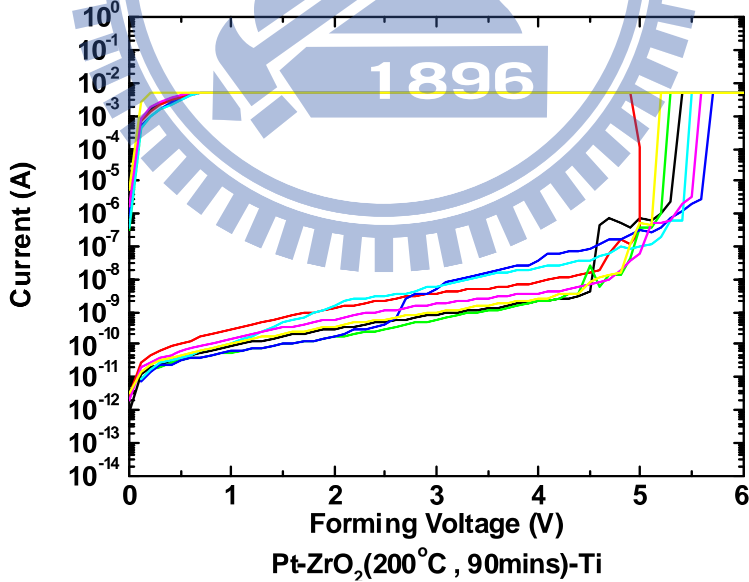


Fig. 3-29 Forming voltage of Ti/ZrO_2/ Pt structure with process thickness of 90mins

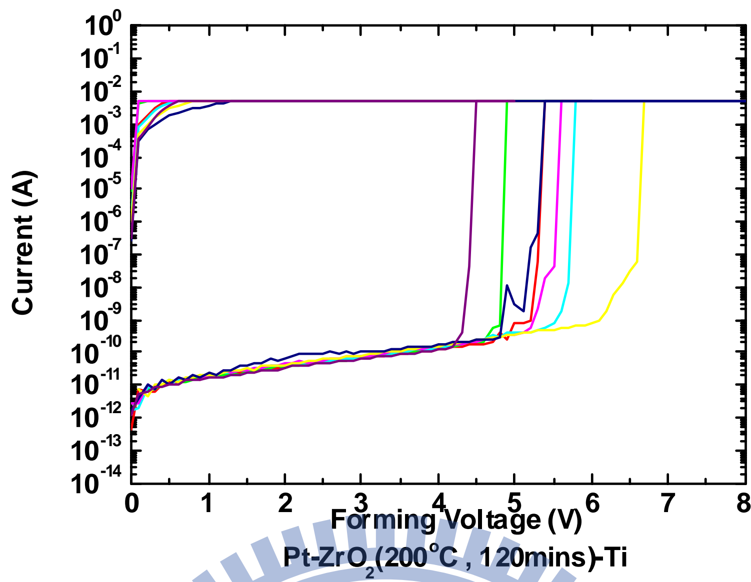


Fig. 3-30 Forming voltage of Ti/ZrO_2/ Pt structure with process thickness of 120mins

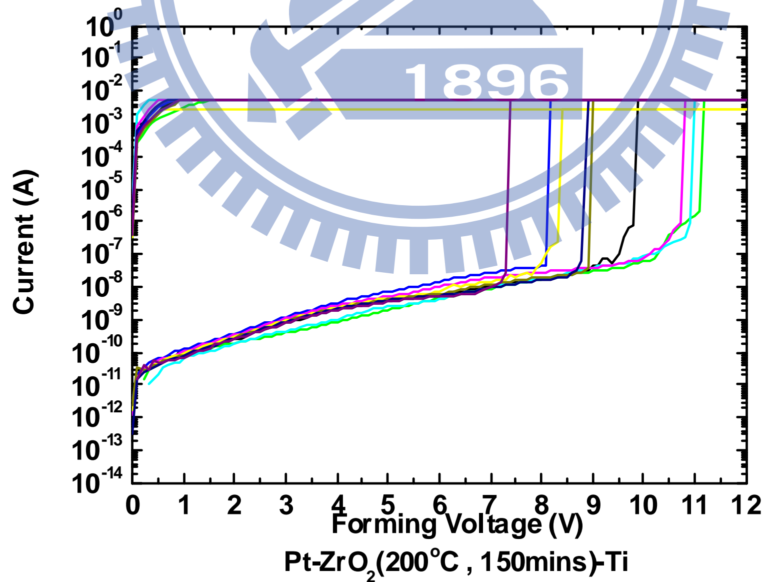


Fig. 3-31 Forming voltage of Ti/ZrO_2/ Pt structure with process thickness of 150mins

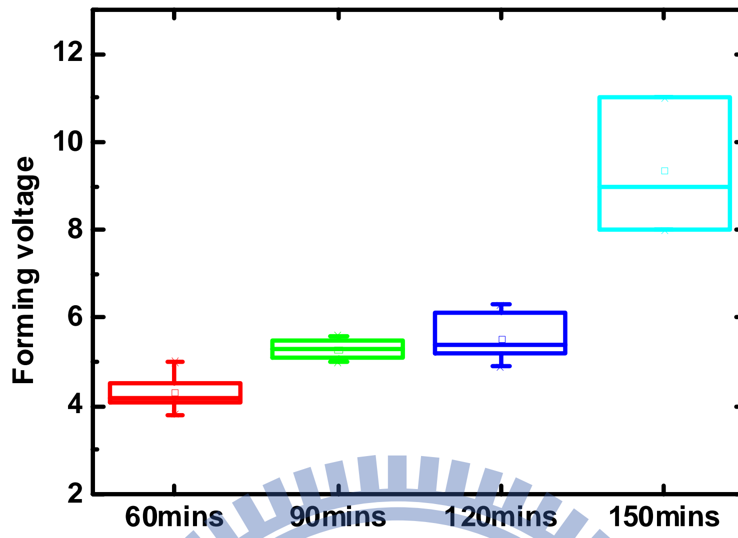


Fig. 3-32 Forming voltage of Ti/ZrO_2/ Pt structure with various process thicknesses

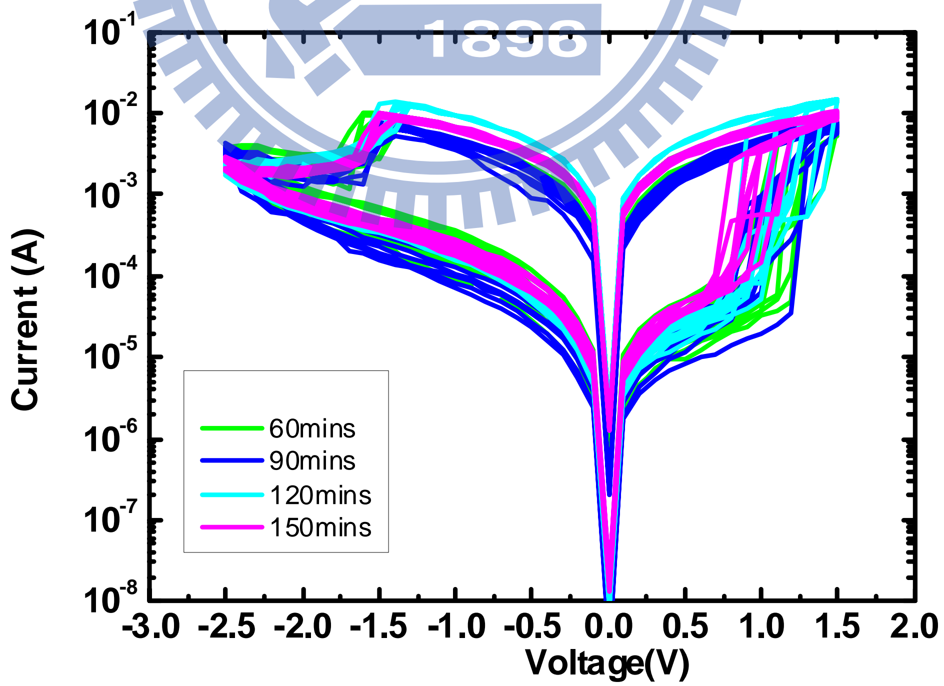


Fig. 3-33 I-V curve in all kinds of different ZrO_2 process thickness

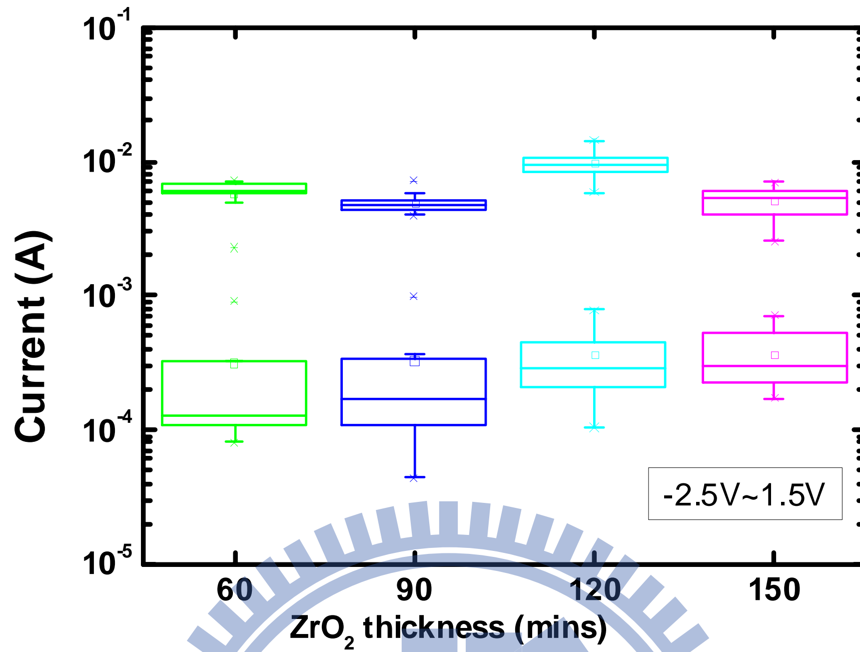


Fig. 3-34 The current of on-state and off-state at various thicknesses with span of-2.5V~+1.5V

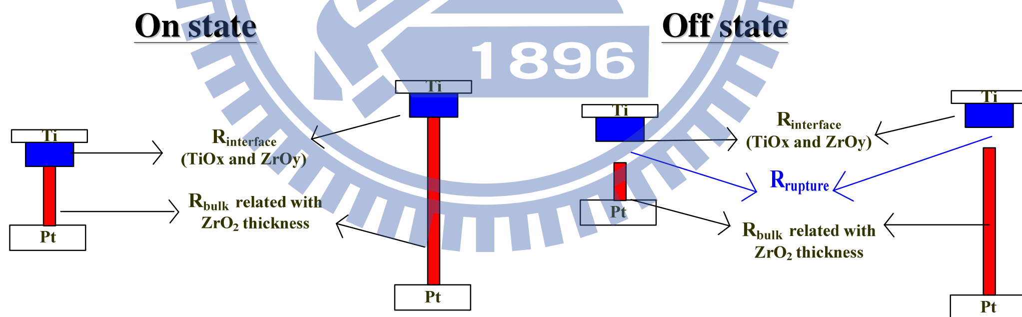


Fig. 3-35 The switching part is major in the rupture layer during the switching with different ZrO_2 thickness

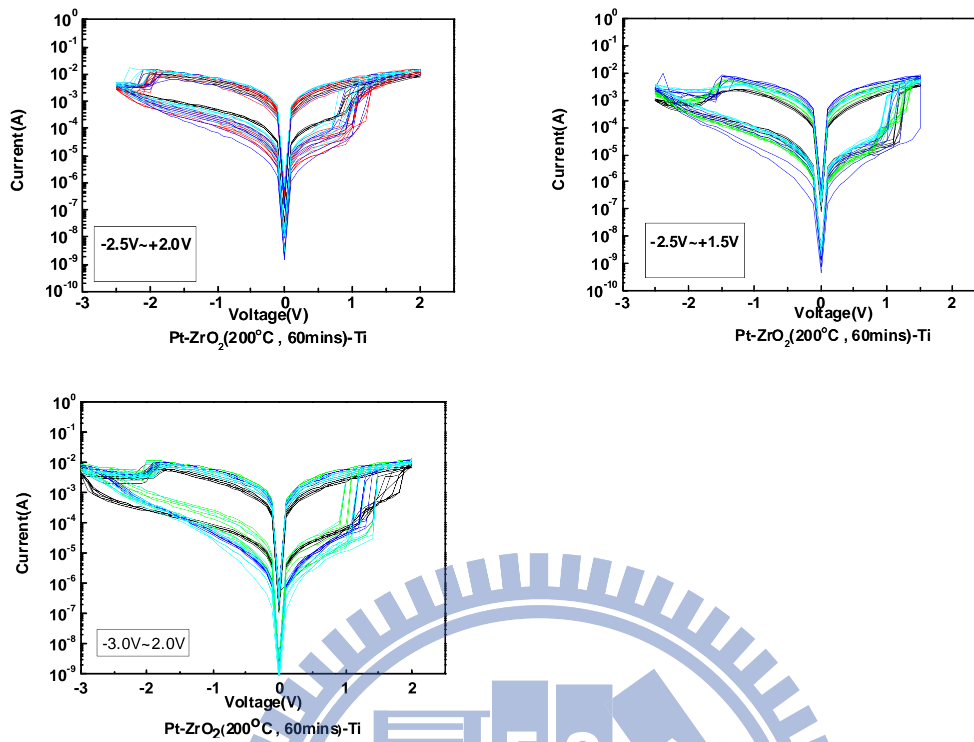


Fig. 3-36 Three kinds of spans of Ti/ZrO_2/ Pt structure with process thickness of 60mins

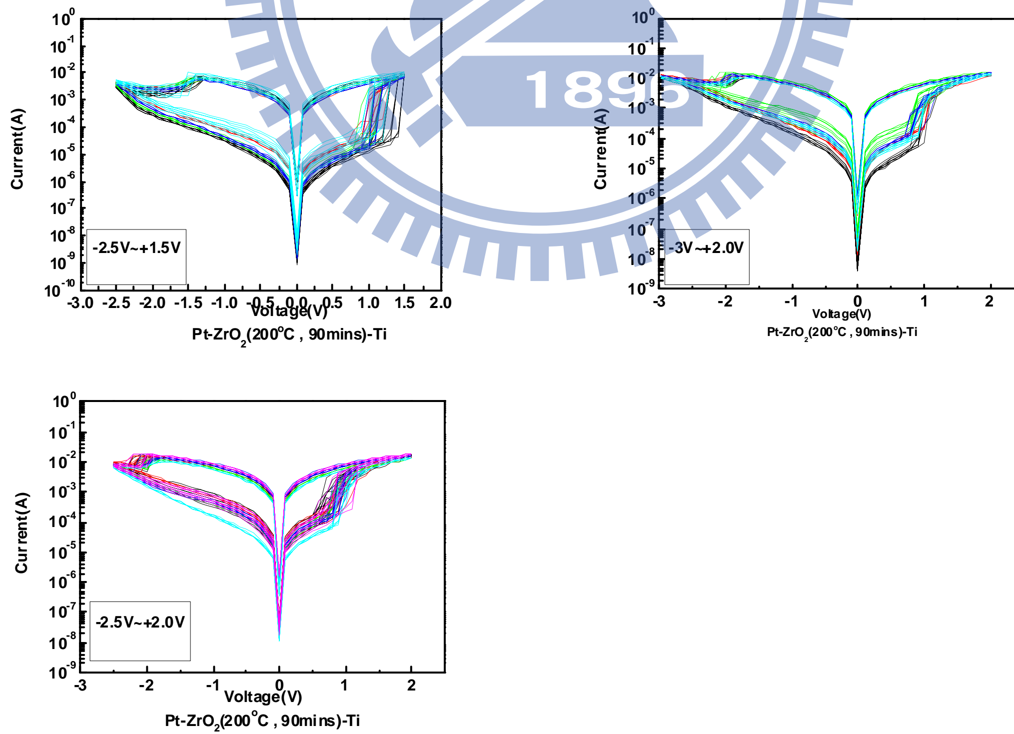


Fig. 3-37 Three kinds of spans of Ti/ZrO_2/ Pt structure with process thickness of 90mins

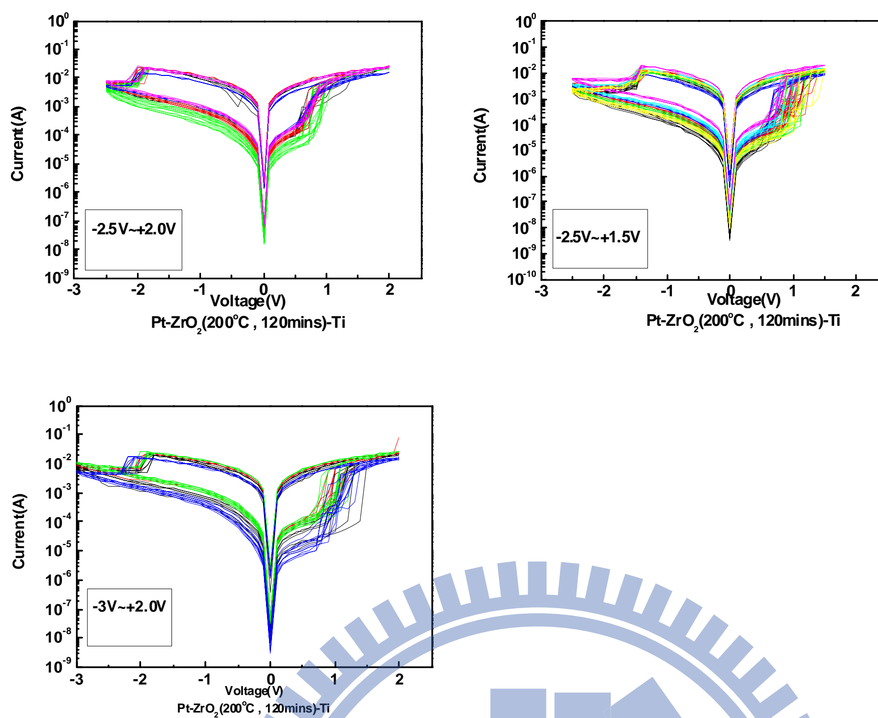


Fig. 3-38 Three kinds of spans of Ti/ZrO2/ Pt structure with process thickness of 120mins

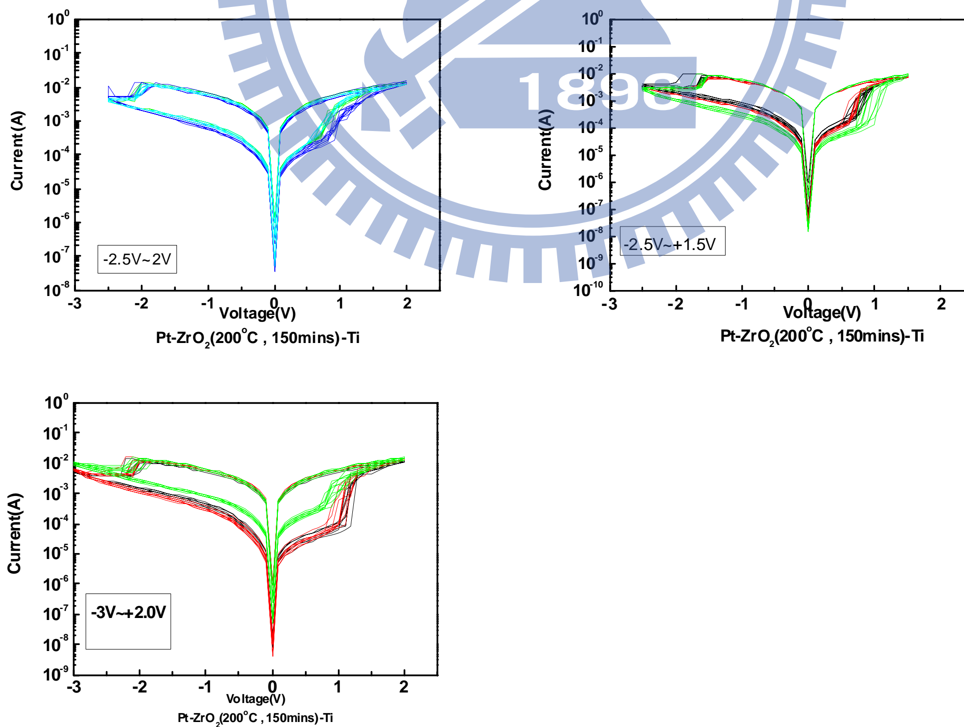


Fig. 3-39 Three kinds of spans of Ti/ZrO_2/ Pt structure with process thickness of 150mins

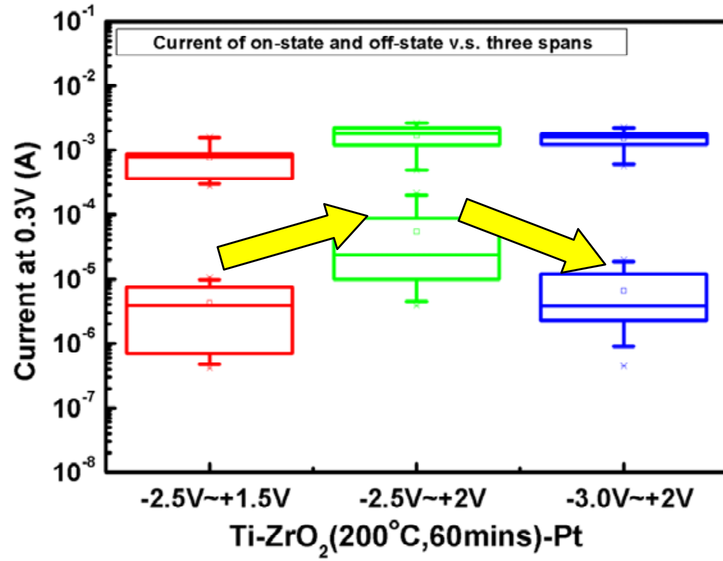


Fig. 3-40 On-state and off-state current of Ti/ZrO_2/ Pt structure with process thickness of 60mins

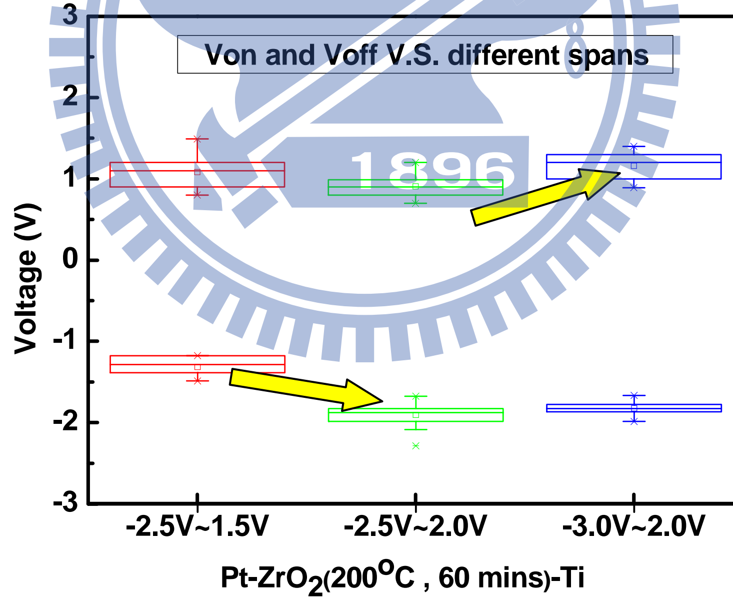


Fig. 3-41 Turn on and turn off voltage of Ti/ZrO_2/ Pt structure with process thickness of 60mins

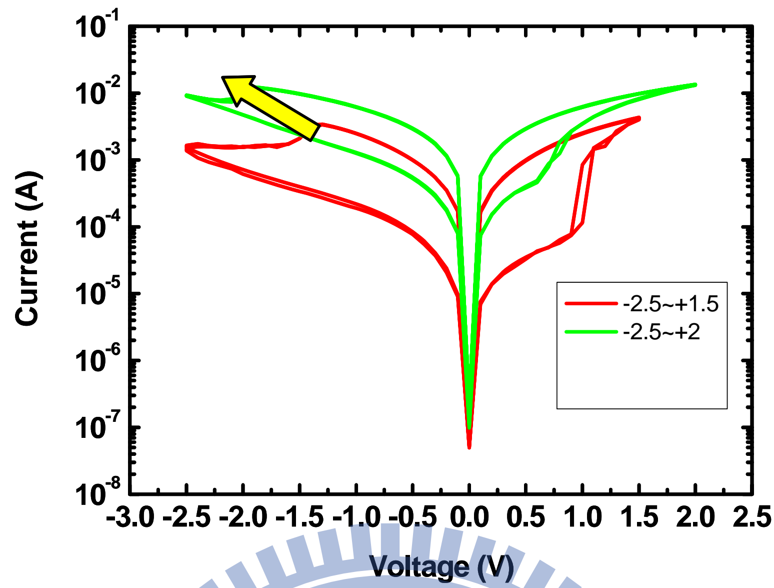


Fig. 3-42 The span of -2.5V~+1.5V, -2.5V~+2.0V is compared by I-V curve

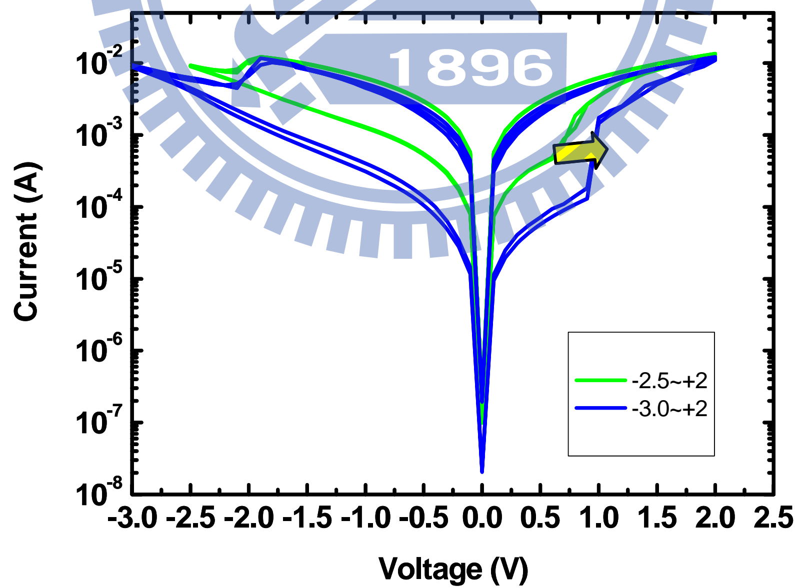


Fig. 3-43 The span of -2.5V~+2.0V, -3.0V~+2.0V is compared by I-V curve

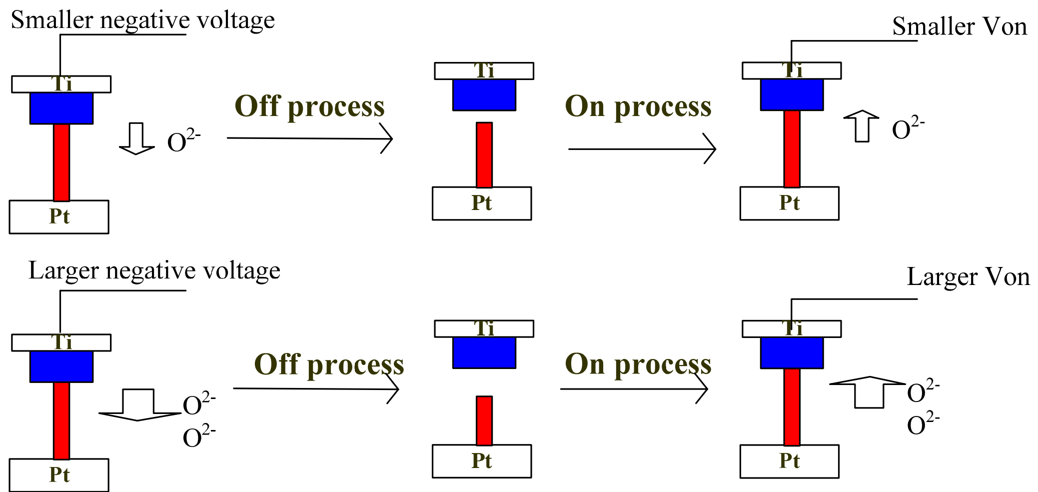


Fig. 3-44 The Von and Voff will be affected by the different span for the switching part is at rupture layer.

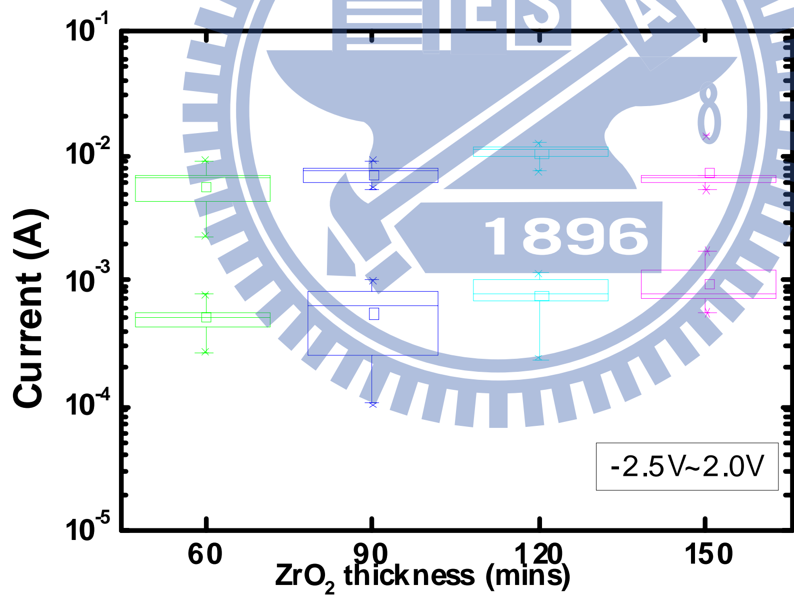


Fig. 3-45 The current of on-state and off-state at various thicknesses with span of-2.5V~+2.0V

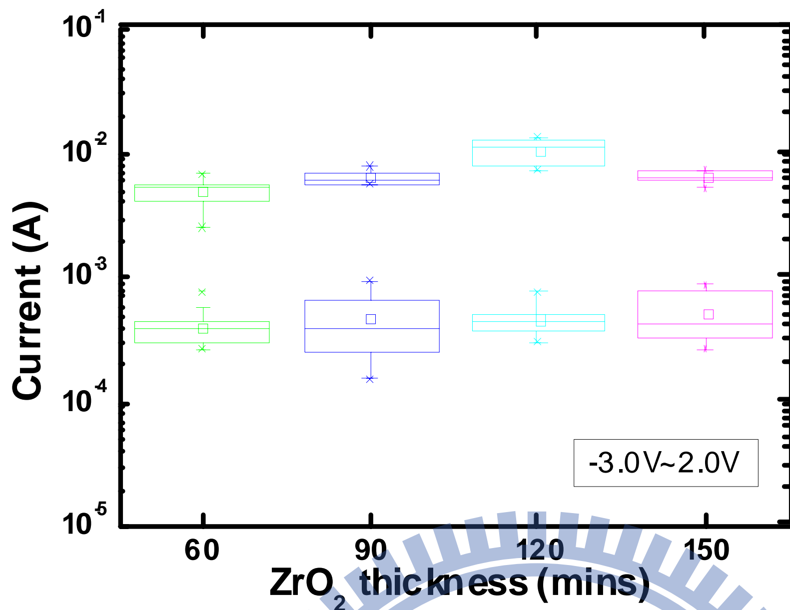


Fig. 3-46 The current of on-state and off-state at various thicknesses with span of-2.5V~+2.0V

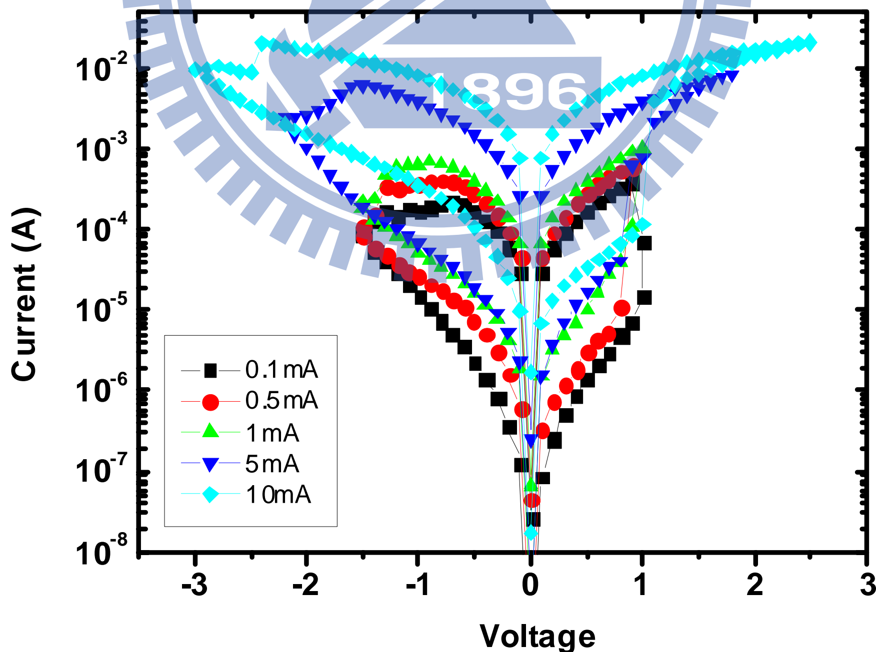
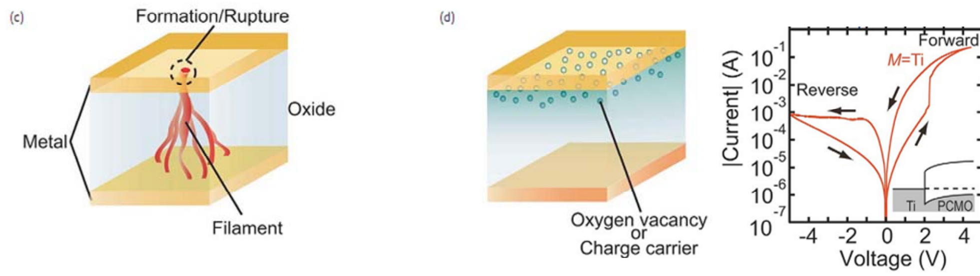


Fig. 3-47 The characteristic of the filament will be decided by the forming compliance



Ref: Sawa materials today

Fig. 3-48 The mechanism is supposed to be the filament-like faucet shape or trap-detrap at the interface state

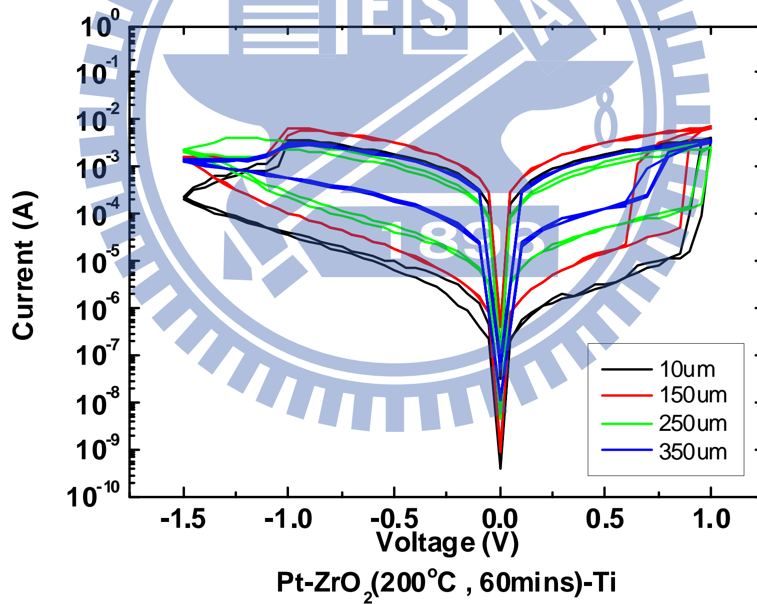


Fig. 3-49 The I-V curve in all kinds of diameters

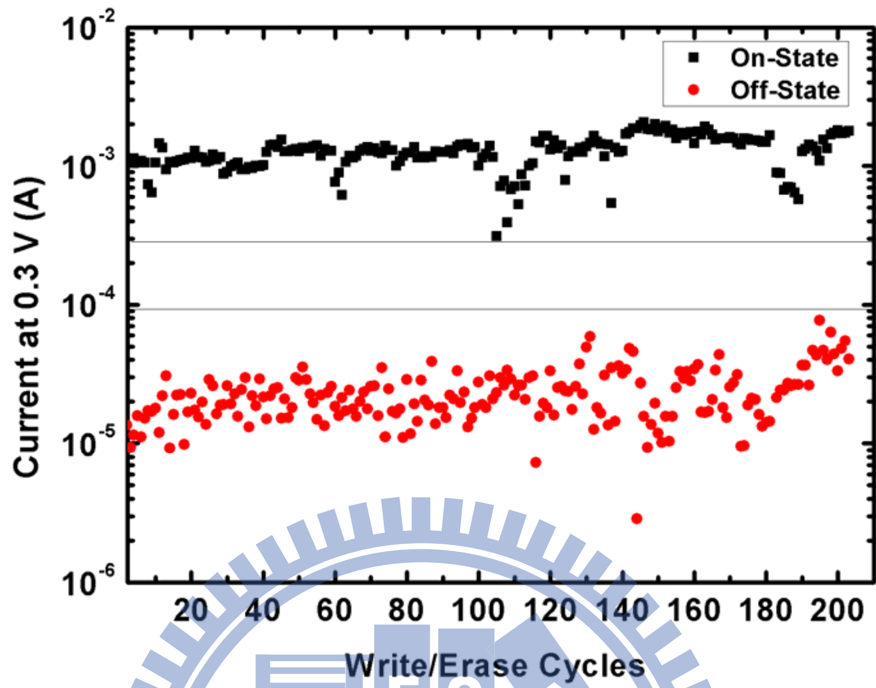


Fig. 3-50 The endurance of size effect

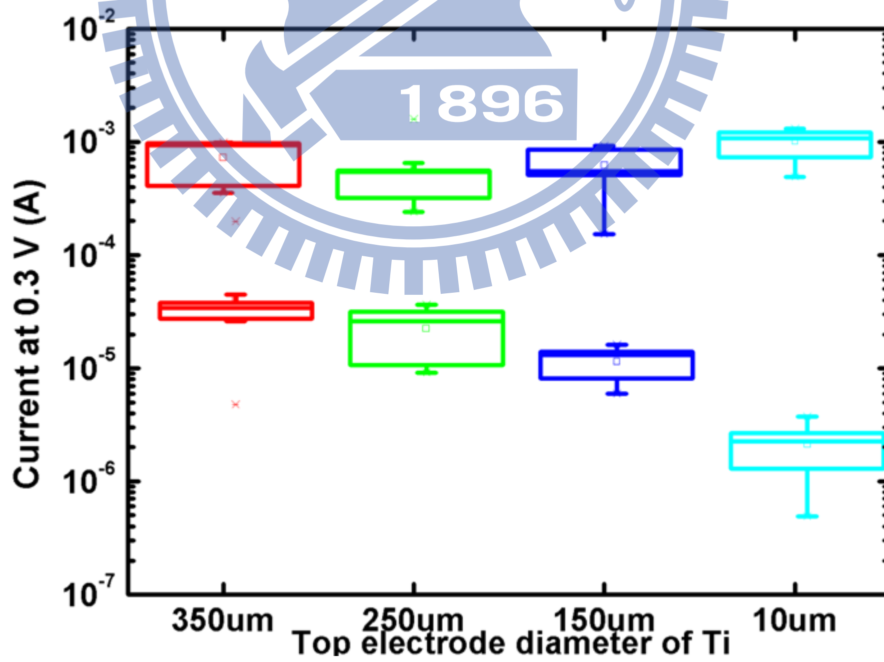


Fig. 3-51 The on-state and off-state current in all kinds of diameters

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Von

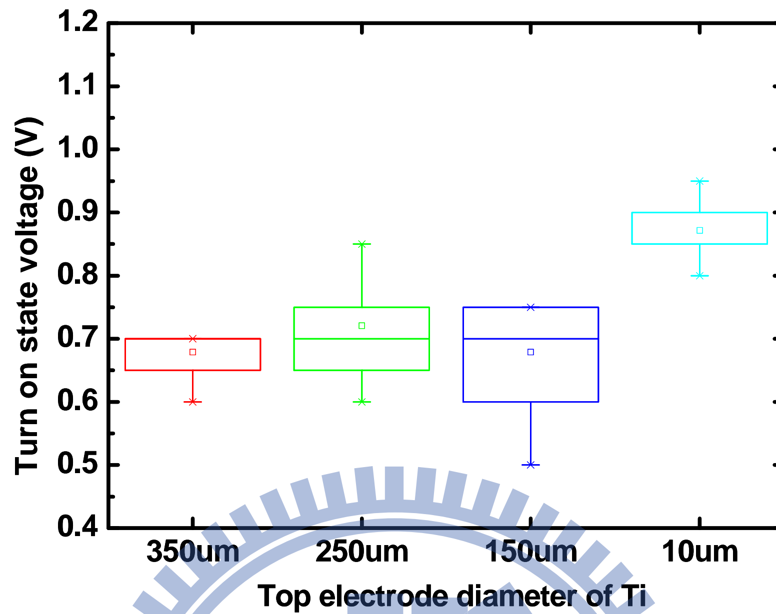


Fig. 3-52 The Von in all kinds of diameters

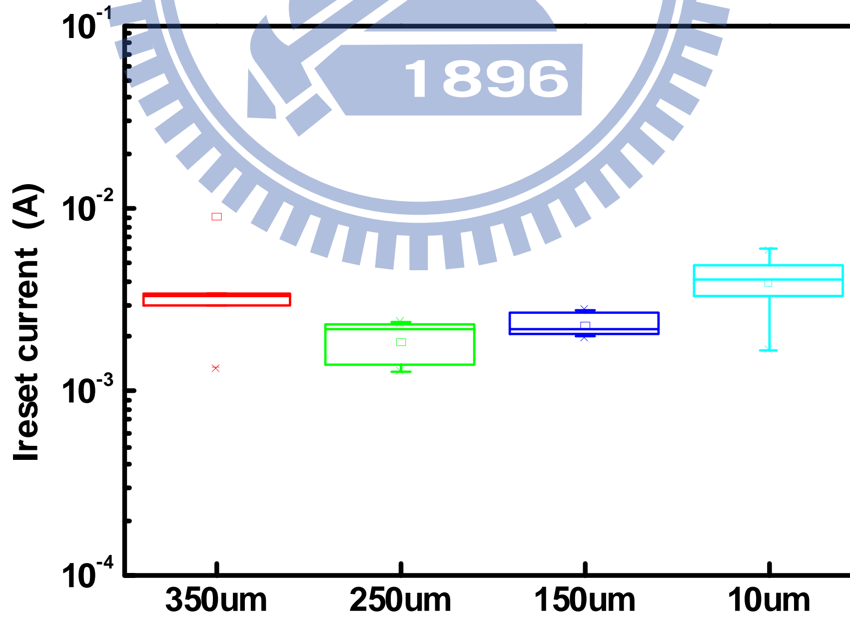


Fig. 3-53 The Ioff current at different diameter condition

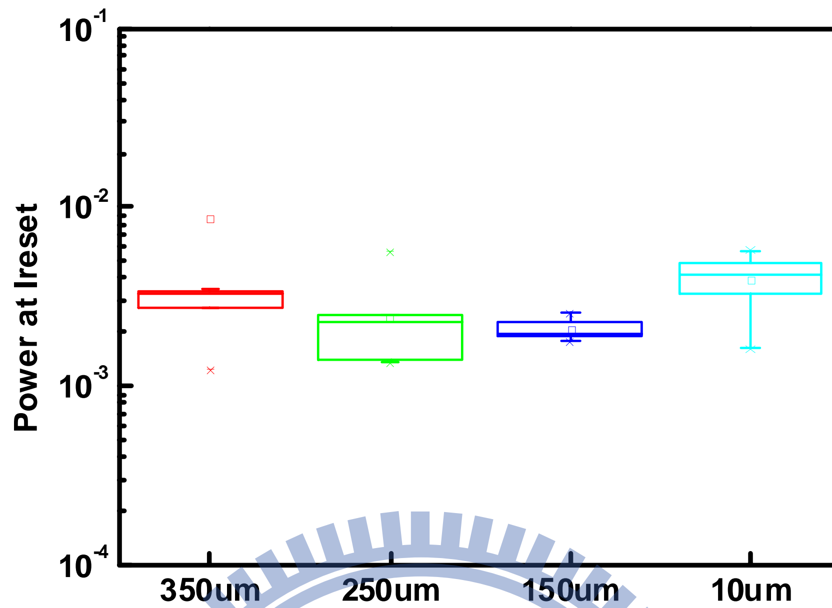


Fig. 3-54 The power at Ioff with different diameter condition

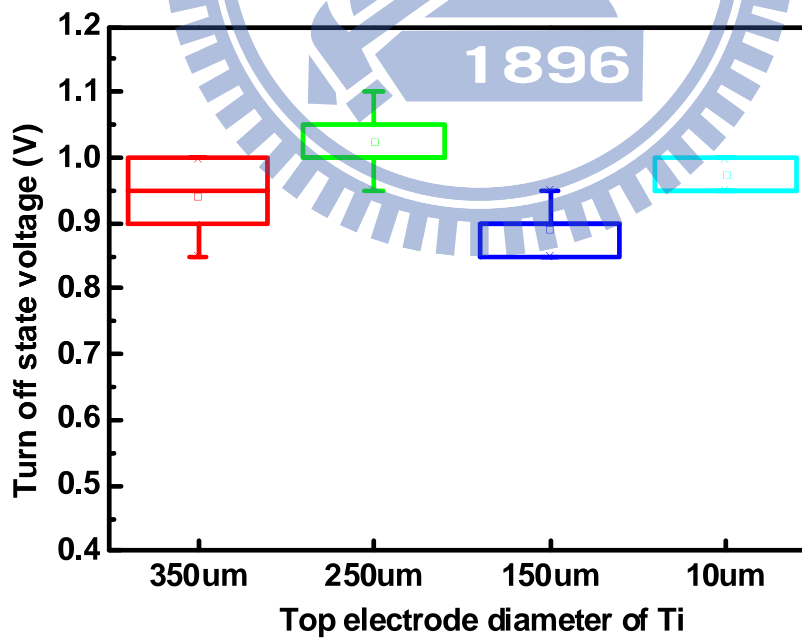
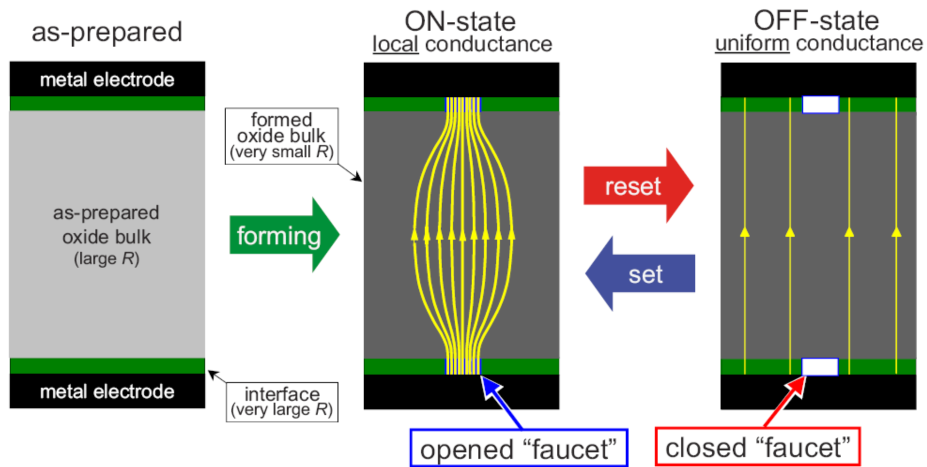


Fig. 3-55 The Voff with different diameter condition



Ref: Inoue et al., PRB 2008

Fig. 3-56 The same characteristic of the filament at on-state before off-state.

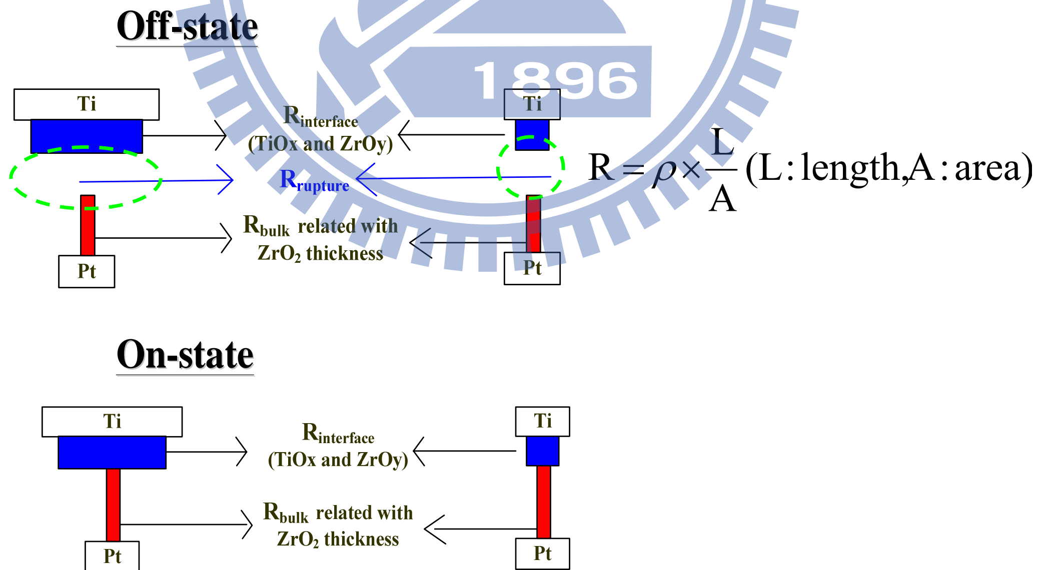


Fig. 3-57 The current of off-state and on-state in the size effect

Chapter 4

Conclusion

In this thesis, it has been shown that the performance and switching properties of ZrO_2 with Ti top electrode. We test the various temperatures when ZrO_2 is deposited to know which is the optimal value. For understanding the mechanism clearer, we deposited various thickness of the ZrO_2 first, using three kinds of spans, and changed the area of the top electrode.

At first, in order to decide the process temperature in this thesis, there are various temperatures which are from room temperature (25°C) to 250 ^{o}C, and the most suitable temperature is 200 ^{o}C. The performance is that endurance 10000 cycle times, 50ns pulse width can switch 1000 cycle times, retention test is 10^6 seconds and nondestructive readout test is over 10000 seconds.

Next, the time of ZrO_2 is deposited are 30mins, 60mins, 90mins, 120mins, and 150mins. Because the switching part is happen between the interface layer and bulk layer, so the voltage drop is almost at there when switching, hence the current is not related with the thickness of the bulk.

The third part is changing the three kinds of spans. It can explain why the trend of V_{on}, V_{off}, and the current of on-state and off-state can be changed based on the properties of Ti top electrode and ZrO_2 layer can form a switching layer. The V_{on} is increased at -3V~+2V compared with -2.5V~+2V, and the V_{off} is also increased at -2.5V~+2V compared with -2.5V~+1.5V. Because the switching is bipolar of positive

on and negative off, so the more positive voltage in span, the more current at switching; if the more negative voltage in span, the fewer current at switching.

The final part is changing the area of top electrode. Because we want to make sure the mechanism is filament or trap-detrap, and we can observe what the current is changed. The current of on-state is not related with the area of the top electrode for the filament is localized. The current of off-state is related with the area, because the off-state current is global in the filament, so the current is decreased when the area is smaller.

Finally, the above described results prove that the interface between electrode and oxide ions plays an essential role in RRAM switching. The oxygen reservoir sink at the interface layer, which is created by the strong oxygen absorption of Ti, and it can provide oxygen ions when off process. With negative bias applied on Ti top electrode, the oxygen ions are repelled out from the interface layer, and it can oxidize the filaments near the top electrode, returning the condition to off state. In summary, the oxygen-rich interface layer and the appropriate operation mode can improve the cell performance.

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