國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

隨機電報訊號量測法應用於前瞻CMOS元件應變技術引致的汲極電流不穩定性之研究

The Observation of Strain Induced Drain Current Instability in Advanced CMOS Devices Using Random Telegraph Noise Analysis

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中華民國 九十八 年 八 月

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碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master of Science

in Electronics Engineering

August 2009

Hsinchu, Taiwan, Republic of China.

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摘要

近年的可靠度研究中，施加應變會對CMOS元件造成的熱載子退化。對於n型MOSFET元件，介電層覆蓋式(CESL)元件(為單軸應變)有較佳的可靠度、性能表現和簡易的製程。而SiC在S/D 的結構提供了高的驅動電流。在p型MOSFET 元件中，單軸的應變結構SiGe在S/D及嵌入式擴散阻擋層(EDB)，有著良好的可靠度和效能。

本論文中，我們利用汲極電流隨機電報訊號量測法，觀察在前瞻應變矽元件，不同的應變技術所造成的缺陷以及可靠度的分析。首先，在應變n型及p型MOSFET元件中，經熱載子加壓後，造成的電流衰退，並在汲極端產生缺陷，此缺陷捕捉及釋放通道的載子，造成汲極電流的不穩定性。藉由載子的捕捉和釋放時間進行統計分析，可以獲得缺陷的特性。此外，透過單軸應變n型及p型MOSFETs 元件，我們探討了不同方向的應變技術所引致的汲極電流不穩定性。

從萃取出的電流振幅並加以正常化(normalized drain current

amplitude)進而觀察垂直應變和水平應變技術對於熱載子破壞所造成的退化影響。相較於對於SiGe S/D結構，介電層覆蓋式(CESL)元件中，此覆蓋層會在閘極介電層中額外的垂直應變結構，經熱載子破壞後會引致額外的載子散射現象；而SiGe只提供在S/D方向的壓縮應變，對於可靠度沒有額外的影響。最後，我們亦將此方法應用在SiC S/D結構元件上，因SiC亦只提供S/D方向的張力應變，無額外的應變在介電層中，此實驗結果可加以驗證之前的結果，與SiGe S/D結構類似，亦即其通道的應變效應，對於可靠度沒有額外的影響。

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ABSTRACT

Recent study on the reliability issues, the strained devices show a higher impact ionization rate, i.e., the device degradation is proportional to the current enhancement. For n-MOSFET devices, CESL (contact etching stop layer) strain (uniaxial) is much better in terms of reliability, performance, and process simplicity; SiC on source and drain structure shows high driving current ability. For p-MOSFET device, uniaxial structure with SiGe on source and drain with EDB (embedded diffusion barrier) seems to be promising in terms of its performance and reliability.

In this thesis, the hot-carrier stress induced oxide traps and its correlation with enhanced degradation in strained CMOS devices have been reported. First, the I_D-RTN (Drain Current Random Telegraph Noise) has been employed to study the stress induced slow traps in uniaxial strained n-MOSFETs and p-MOSFETs. The carrier trapping and detrapping effect in the gate dielectric can be observed. The drain current fluctuation is at low level when carrier is trapped and is at high level when carrier is detrapped. Through statistically extracting and calculating the capture and

emission time, we can figure out the trap properties. Secondly, different process-induced strain effect for n-MOSFETs and p-MOSFETs has been observed respectively. By extracting the normalized drain current amplitude from the drain current spectra, experimental results show that the vertical compressive strain generates extra oxide defects and induces more scattering after HC stress in CESL device.

This vertical strain in CESL also contributes to a non-negligible amount of extra devices degradation. While, SiGe S/D on p-MOSFET device shows different behavior in that the compressive strain along the channel shows no impact on its reliability. The process induced strain among different strained techniques can be investigated by the I_D-RTN measurement. Furthermore, the application to the study of the strained SiC on S/D has also been demonstrated. Results also show that the uniaxial strain in such device exhibits less impact on the device reliability. Therefore, this strained SiC device is similar to the SiGe S/D device in terms of the I_D-RTN characteristics.

Acknowledgements

碩士生活的兩年是短暫卻又充實的，交織著酸甜苦辣的實驗室日子。首先要感謝我的指導教授莊紹勳老師，莊老師不僅在研究上給予許多指導建議，教我應具有的研究精神跟態度，並在課業與生活上，也有許多的關懷，在此深表我對老師的感謝。

感謝家銘學長在實驗研究上的細心教導，並且給予我許多的建議跟指導，感謝建鴻、友良、易叡和文彥學長，給予學業跟實驗上的解答跟協助。還有感謝這兩年研究生涯的夥伴安舜、健宏、振鵬，在日常的生活中，因為有你們，讓實驗研究生活變得更加有趣，相信數年後再聚，定倍感溫馨。也感謝汪老師研究群的志昌、達達、小馬、佑亮、元元學長，彥君、子華學姐、以及阿標和阿杜，雖然在不同的研究群中，但實驗室有你們，使得乏味的實驗室生活更多采多姿。此外，也感謝學弟元宏、政穎、永涵、士嵩，感謝你們對實驗室的付出，使得學長姐們能專心於實驗研究上，真心的祝福你們明年可以順利畢業。總歸一句，感謝所有的夥伴，因為有你們，使我這兩年研究生活豐富且精彩，即使艱辛，仍充滿歡笑。

另外，在此也要感謝聯華電子在測試元件和儀器上的協助，讓本研究才得以順利完成。

最後要感謝我家人們，你們是我最大的精神支柱，有了你們的支持和鼓勵，讓我能堅持到現在。

謹將這份榮耀獻給培育我多年的父母親。

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Chapter 1
Introduction

1.1 The Motivation of this Work

Recent developments [1.1] in CMOS technology have highlighted the need in using the strain technique as a method to extend the scaling of CMOS device for high speed and low power logic applications. Several approaches among them, such as process-induced stress techniques, strained SiGe channel devices, substrate engineering, and hybrid substrate technology, have been utilized to improve device performance. Although the strained devices enhance the carrier mobility, their reliabilities become a serious issue as reported in [1.2] [1.3].

In the small area devices, carriers are trapped and detrapped stochastically by the traps in the gate dielectric would induce the drain current instability called I_D-RTN (Drain Current Random Telegraph Noise). The performance of ultra-scaled devices is highly affected by the local phenomenon.

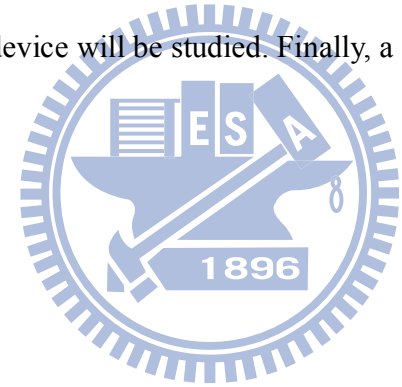
The I_D-RTN method is believed to be one of the great techniques to study the generated oxide traps via carrier trapping and detrapping. So far, the trap-related reliability issues in strained CMOS devices have not been well understood yet.

For the first time, in this thesis, we apply the I_D-RTN method to the observation of oxide traps in various n-MOSFETs and p-MOSFETs employing different process-induced strain. The impact of their strains on the device reliability will be investigated and

compared. Furthermore, the application to the SiC on S/D devices will be demonstrated.

1.2 Organization of the Thesis

The thesis is divided into six chapters. Chapter 1 is the introduction. Chapter 2 describes the experiment setups and the I_D-RTN mechanism. In chapters 3 and 4, we will first utilize the I_D-RTN method to observe the process-induced RTN behavior of strained n-MOSFETs and p-MOSFETs respectively. The hot carrier stress would be applied on the strained CMOS devices. Then, we will discuss the strain induced degradation for n-MOSFETs and p-MOSFETs with different strained techniques. In chapter 5, the application to the SiC S/D device will be studied. Finally, a summary and conclusion will be included in Chapter 6.



Chapter 2
Random Telegraph Noise Mechanism and Experimental Setup

2.1 Introduction

Recent developments in strained technology have heightened the need for the high performance CMOS devices. The charge pumping measurement can be used to measure the fast trap properties [2.1]. However, the charge pumping current becomes very small in the small area devices that would influence the experimental results for reliability. In order to discriminate the relationship between performance and reliability properties of the small size strained CMOS devices, we utilize the Drain Current Random Telegraph Noise (I_D-RTN) measurement technique in this work. In this chapter, the measurement setup and the physics of the drain instability will be described.

This chapter is divided into two sections. First, we will illustrate the fundamental experimental setup to characterizing strained CMOS devices. Second, the I_D-RTN technique used in this thesis will be introduced, and its fundamental theory will be described.

2.2 Experimental Setup

The experimental setup for the direct current I–V and the I_D-RTN measurement of semiconductor devices is illustrated in Fig. 2.1 and Fig. 2.2, respectively. Through the PC controlled instrument environment, the complicated and long-term characterization

procedure for analyzing the intrinsic and degradation in MOSFETs can be easily verified. As shown in Fig. 2.1, the characterization equipment, including semiconductor parameter analyzer (HP4156C), and cascade guarded thermal probe station, provides an adequate capability for measuring the device characteristics. In this method, the pulse generator is not included that would decreases the influence from the noise. In addition, the PC program used to control all the measurement process is HT-basic. The parameter analyzer is connected to the probe station directly without passing through the switch equipment. At the room temperature, the sampling mode is chosen and the V_{GS}, V_{DS} bias is selected to make the trap's energy level in the vicinity of the Fermi level. For the sampling rate, the minimum resolution is 1ms for the maximum 10^3 reading per second. If the interval time sets too larger than the capture and emission, the drain current fluctuation may not be observed. With sufficient fast sampling rates, we could detect the drain current fluctuation. Furthermore, I_D-RTN happens only during local gate bias so it is better to detect varying tight gate voltage step while sampling. In addition, the RTN phenomenon would be detected easily as the devices scaling down but the magnitude of the drain current decreases.

In order to extract the capture time, emission time, and drain current amplitude, we use the program statistically to take a large amount data. For the two-level drain fluctuation, we select a current which lies in the middle of the high and low current state to discriminate trap capturing or emitting carriers automatically and sum up every period of the time which is then divided by the number of events. In this manner, we can get the mean capture time, emission time, and also drain current amplitude efficiently without wasting too much time. As a result, we can observe the trap properties.

2.3 Theory of Drain Current Telegraph Noise

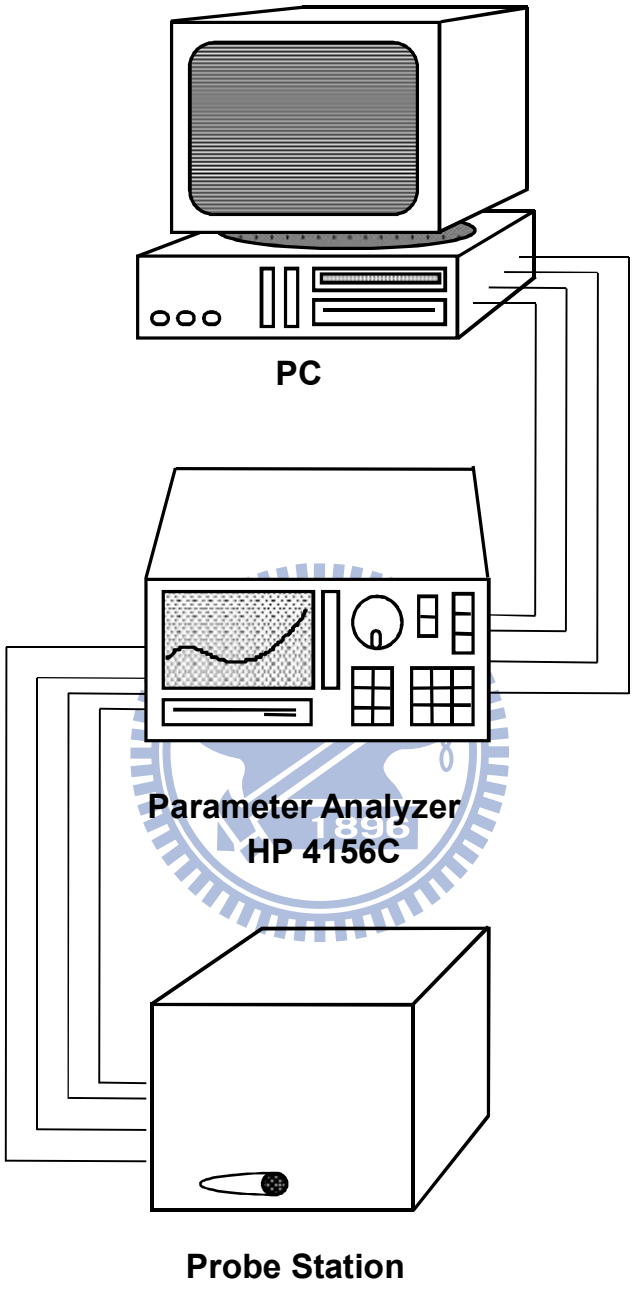
Figure 2.3(a) is the schematic showing the carrier trapping and detrapping through the oxide trap. In small devices, only trap energy within a few kT from the Fermi level would make current fluctuation where k and T are the Boltzmann constant and equilibrium temperature, respectively. So far, the drain current fluctuation is generally influenced by two effects: the number fluctuation of free channel carriers ΔN_s, and the mobility fluctuation $\Delta \mu$ described by [2.2][2.3].

$$\frac{\Delta I_d}{I_d} = \frac{\Delta N}{N} \pm \frac{\Delta \mu}{\mu} = -\frac{1}{W \cdot L}[\frac{1}{N} \pm \alpha\mu] \qquad (2.1)$$

in the strong inversion. Here N_s is the channel carriers per unit area and α is the scattering coefficient_while the sign in front of the mobility fluctuation is determined by the type of the trap (repulsive or attractive scattering center). For an acceptor type trap, the high level corresponds to the neutral state (no captured carrier) while the low level corresponds to the charged state. When the traps in the dielectric are empty and their energy level maintain at a level which is equal to that of the channel carriers or below, traps will capture carriers from the channel. When the carriers are trapped, they will increase the nearby potential and lower the current.

The three major parameters (capture time, emission time, and current amplitude) of the I_D-RTN are defined in Fig. 2.3(b), capture time τ_c is the average of the high time constants, emission time τ_e is the average of the low time constant and current amplitude ΔI_D is the magnitude of the drain fluctuation. The current amplitude, capture and emission time are the critical parameters of random telegraph noise phenomenon which

depend on the trap properties, such as trap depth into dielectrics, trap energy apart from conduction band (valance band if holes are captured and emitted).



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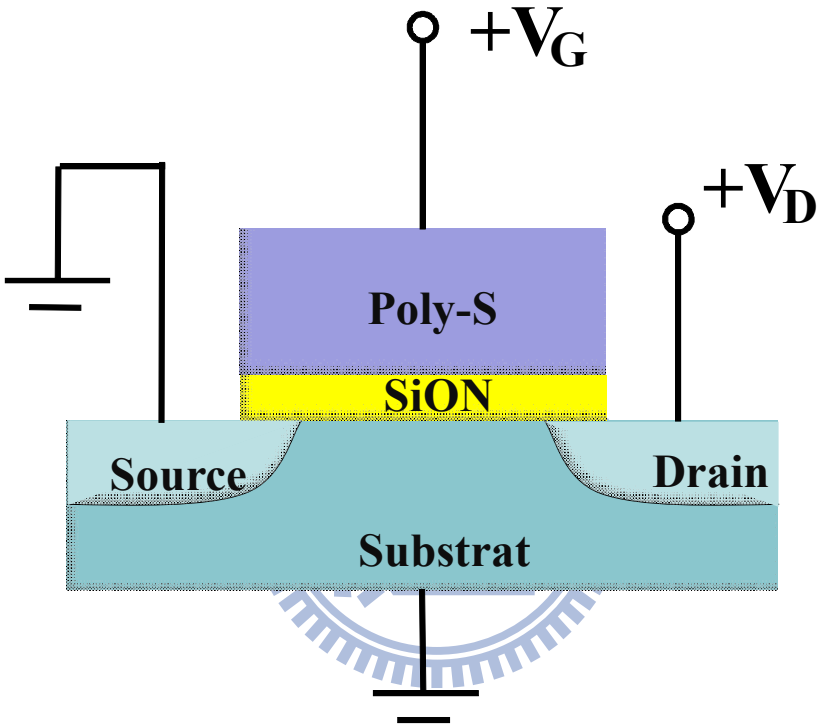


Fig. 2.2 The terminals setup for sampling by Analyzer HP4156C.

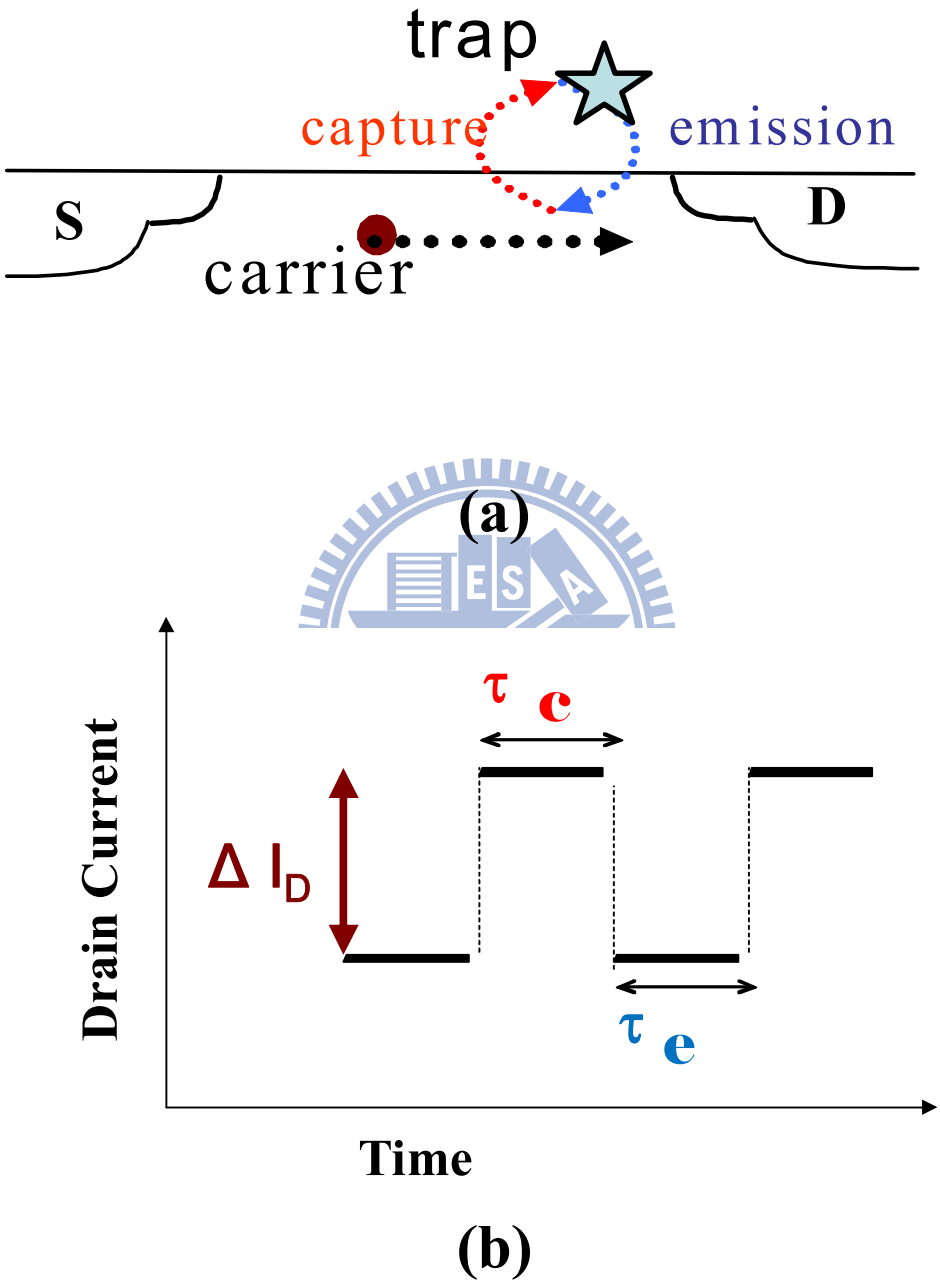


Fig. 2.3 (a) Carrier trapping and detrapping by the slow trap near the drain side. (b) Illustration of the three parameter of the RTN noise: capture time τ_c, emission time τ_e , and current amplitude ΔI_D.

Chapter 3
Random Telegraph Noise of Drain Current in n-MOSFETs

3.1 Introduction

Recently, researches have shown an increasing interest in the strain technology. Strained silicon technology is essential for the continuation for the scaling of MOSFET devices, owing to its high impact on carrier mobility and thus on drive current improvement [3.1]. When applied to the direction of the channel, tensile strain improves the performance of n-MOSFET devices, while compressive strain is beneficial for p-MOSFET devices. The local strain, such as capping layer, SiGe on S/D, and SiC on S/D are induced by the process. They are usually uniaxial strain. Compared to the global strain usually biaxial strain, the local strain has less dislocation issues.

As the devices being scaled, there are plenty of reliability issues in the strained devices. Besides, trapping of a single carrier charge in traps and related local modulation in carrier density and mobility will have a profound influence in the carrier density and mobility on the drain current. The drain current fluctuation will cause serious drawbacks on the small geometry devices.

In this chapter, the I_D-RTN "Drain Current Random Telegraph Noise" for the exploration of strain-induced slow trap properties is presented in strained n-MOSFETs. Single electron capture and emission could be observed. The analysis of the reliability will be introduced first in Section 3.3. Next, the analysis of drain current instability is

interpreted in Section 3.4. Based on the voltage dependence of single charge effect, the traps parameters are extracted and the strain process induced-effect will be also discussed.

3.2 Device Preparation

The devices were fabricated by the advanced 65nm CMOS technology at UMC. The schematic cross section diagram of n-MOSFET splits is shown in Fig. 3-1. In this figure, Fig. 3-1(a) is the bulk-Si device, and Fig. 3-1(b) is the CESL (contact etching stopping layer) capped device (uniaxial-strained). Both n-MOSFETs are <100> channel on (100) substrate. All these test devices have 14Å EOT gate oxide with SiON process and with the same dimension (W/L= 0.2/0.12um).

3.3 The Analysis of Reliability in n-MOSFETs

3.3.1 Introduction

The strain technologies can enlarge the mobility to achieve the significant driving current enhancement [3.2] [3.3] [3.4]. However, many technologies have been developed to boost the drive current; the reliability issues have been rarely studied. It is necessary to consider the effects for device characteristics involving uniaxial and biaxial strained effects for CMOS devices.

A large mobility enhancement would adversely affect the device reliability [3.5]. For n-MOSFETs, the CESL device becomes the most promising technology and the better reliability, especially with process simplicity. In 2006, S. S. Chung et al. [3.6] first

published a paper, in which they demonstrated for n-MOSFETs, tensile cap stressor device is much better in terms of reliability and performance. Based on the important results, we will further analyze the reliability issues of strain n-MOSFETs and investigate them by the I_D-RTN method after hot carrier stress. They are described in two parts. The first part is to investigate hot carrier degradation and the second part is to analyze the drain current instability after HC stress in bulk-Si and CESL devices. For hot carrier degradation, threshold voltage shift, drain current degradation and transconductance degradation would be observed by electric measurement. These stresses generate the interface trap and fixed oxide charges. For the drain current instability, the stress-induced traps' properties and the relationship between the strain and the I_D-RTN results would be studied.

3.3.2 Drain Current Degradation

The procedure of following experiment is shown in Fig. 3.2. Firstly, in the I_D-V_G step, the purpose is to get the basic semiconductor parameters and make sure the devices can work successfully .Then, the devices are subjected to the I_D-RTN analysis, to ensure that there is no current fluctuation in the fresh devices (i.e., no process induced traps). Then, we apply the hot carrier stress, to produce the oxide traps near the drain region which would show a two-level fluctuation of drain current. Subsequently, the I_D-RTN measurement is applied to the stressed devices. Under hot carrier stress with injecting hot electrons to destruct gate dielectrics, we could prevent the effect of changing temperature and measure RTN at once. Traps generation for apparent two-level fluctuations is hard to say happening on specific time and its dependence with time on different stress voltage is also not regular. In our measurement, after HC stress (V_{GS}= V_{DS}= 2.5V for 300sec), we

obtain significant RTN appearance in the linear region and continued subsequent analysis. We show the I_D-RTN measurement results for stressed devices and discussed the induced slow traps properties in the coming sections.

Figures 3.3 (a) and (b) show the drain current degradations before and after the HC stress. The drain current degradation in CESL device is 27.16% and in bulk is 15.62%. The CESL device shows large drain current degradation than bulk device, as result of its higher impact ionization rate (I_B/I_D) caused by the strain effect [3.7]. A large enhancement of the driving current will adversely degrade the device reliability.

3.4 The Analysis of I_D-RTN in n-MOSFETs

3.4.1 Drain Current Waveform

The stress induced slow oxide trap near the drain side which would cause the drain current instability (I_D-RTN) through the trapping and detrapping of channel carriers. The I_D-RTN measurements were performed in linear operation at a constant drain voltage V_{DS}= 0.05V for gate voltages V_{GS} between 0.3 - 1 V, in steps of 20mV using HP4156C. Fig. 3.4 and Fig. 3.5 show the different I_D-RTN wave spectra for bulk-Si and CESL devices respectively. The drain current amplitude is about 50nA.

3.4.2 Capture and Emission Time

Fig. 3.6 and Fig. 3.7show the mean capture and emission time gathered statistics from Fig. 3.4 and Fig. 3.5. The decrease of τ_c, as gate bias increases shows the acceptor type of the generated slow oxide trap [3.8]; and the capture time, τ_c, of the slow oxide

trap in the CESL device is larger than bulk-Si device in Fig. 3.6, which implies that the trap is deeper in CESL device is larger than the bulk-Si device. The magnitudes of emission time τ_e are both about 0.01~ 0.1 sec. While, the magnitudes of the emission time τ_e do not show much difference. From the dependency of τ_e, versus gate bias, the carrier in bulk-Si device detraps via Frenkel-Poole emission while carrier in CESL device detraps via trap-assisted-tunneling to the silicon substrate. Due to the thermal emission for the carrier in the bulk-silicon's trap, the emission time decreases as gate voltage increasing in Fig. 3.6. This implies that the bulk device's trap is near the Si/SiO_2 interface. While the carrier detraps through thermally assist tunneling to the Si for CESL device, emission time increases as gate voltage increases in Fig. 3.7. Furthermore, the trapping and detrapping events happen more frequently in CESL devices so the capture time over the emission time increases more quickly in CESL than bulk device in Fig. 3.8. This also assures that the HC stress produces more damage at the Si/SiO_2 for the CESL device and the trap is deeper in CESL device than bulk-Si device ones.

3.5 Discussion

According to the Shockley–Read–Hall statistics [3.9], the capture time τ_c is sensitive to the channel carrier density n, the average carrier velocity *v*, and the capture cross-section σ as Eq. (3.1), where

$$\tau_c = \frac{1}{nv\sigma} \tag{3.1}$$

and

$$\sigma = \sigma_0 \exp\left(-\frac{\Delta E_B}{kT}\right) \tag{3.2}$$

Here, σ is the capture cross section. Here, σ_0 is the cross-section prefactor, and ΔE_B is the thermal activation energy for capture. T and v are usually taken to be the equilibrium lattice temperature and average thermal velocity v_{th}. This approximation is invalid at large lateral electric field, and electron heating occurs and affects the electron capture time. As the gate bias increasing, the capture time would be decreased due to the increased carrier density in the channel. Emission time τ_e is given as Eq. (3.3) [3.10],

$$\tau_e = \frac{\exp[(E_F - E_T)/k_B T]}{g\sigma v n} \tag{3.3}$$

where g is the degeneracy factor. The term (E_F-E_T) represents the trap energy with respect to the Fermi energy. k_B is the Boltzmann constant.

3.5.1 Trap Depth

The relationship between the mean capture and emission times and trap parameters can be described as the following [3.11],

$$\ln\left(\frac{\tau_c}{\tau_e}\right) = -\frac{1}{kT}\left[(E_{Cd} - E_T) - (E_C - E_F) - \varphi_0 + q\psi_S + q\frac{Z_T}{EOT}(V_G - V_{FB} - \psi_S)\right] \tag{3.4}$$

$$\frac{d\ln\left(\frac{\tau_c}{\tau_e}\right)}{dV_G} = -\frac{q}{kT}\frac{Z_{eff}}{EOT} \tag{3.5}$$

where E_{Cd}, E_C, E_F, φ_0 and ψ_s are defined in Fig. 3.9. EOT is the effective oxide thickness

and V_{FB} is the flat-band voltage. We can estimate Z_{eff}, effective depth from substrate, from measurements of τ_c/τ_e by varying V_G. The trap depth is extracted from the slope of $ln(\tau_c/\tau_e)$ versus V_G as shown in Eq. 3.5. Z_{eff} is 1.09A for bulk device and 6.70A for CESL device shown in Fig. 3.10. The trap in CESL is deeper than the trap in bulk-Si. The characterized depth of generated traps in Fig. 3.10 shows that CESL device will cause more fluctuations, Fig. 3.5. This also assures that HC stress produces more damage in the Si/SiO_2 for the CESL and the trap location is deeper is deeper in CESL than in bulk-Si, Fig. 3.10.

3.5.2 Normalized Drain Current Amplitude

Fig. 3.11 and Fig. 3.12 show the drain current amplitude gathered statistics from Fig. 3.4 and Fig. 3.5 divided by the drain current and take plots as function of gate bias. At very low drain voltages in the strong inversion, the mobility fluctuations term $\Delta\mu/\mu$ plays a more dominant role than the number fluctuations $\Delta N_s/N$ [3.11], i.e.,

$$\frac{\Delta I_D}{I_D} = -\frac{1}{W_{eff} \times L_{eff}} \left(\frac{1}{N} \pm \alpha\mu\right) \tag{3.6}$$

Furthermore, the variation of the RTN amplitude $\Delta I_D/I_D$ is proportional to the normalized transconductance change g_m/I_D ratio[3.12]

$$\frac{dI_D}{I_D} = \frac{g_m}{I_D} \frac{q}{W_{eff} L_{eff} C_{ox}} \left(1 - \frac{x_T}{t_{ox}}\right) \tag{3.7}$$

(i.e., $\Delta I_D/I_D \ \alpha \ g_m/I_D$) in the bulk-Si device (Fig. 3.11); while the variation in CESL device changes rapidly (Fig. 3.12). The RTN is neither influenced by the change of

carrier fluctuation ΔN_s nor by the mobility $\Delta \mu$ [3.11]. Since a screened Coulomb scatter with very similar α values for comparable channel electron densities [3.11][3.13] , the $\Delta I_D/I_D$ roll-off quickly in CESL device reveals that an extra carrier scattering is induced. This will give rise to an additional mobility degradation of the CESL device after the HC-stress.

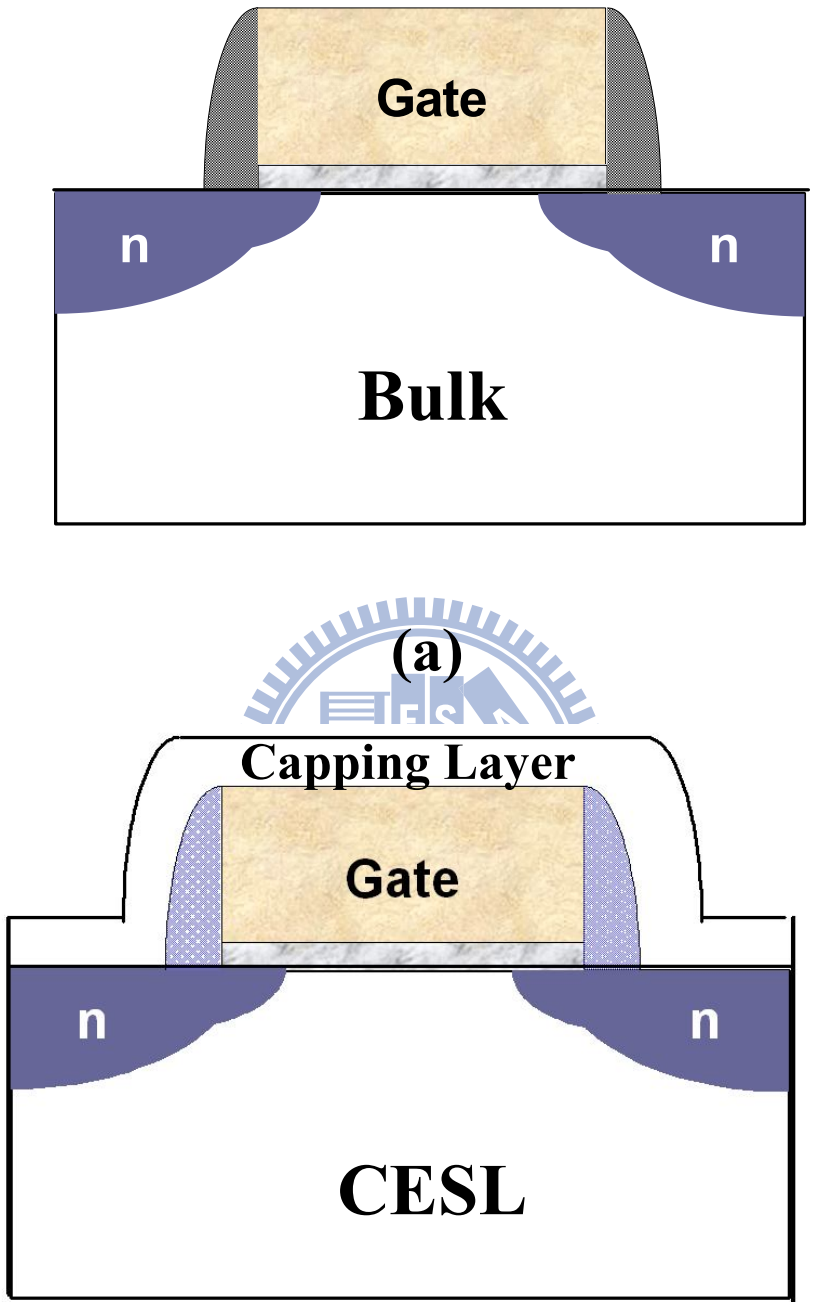


Fig. 3.1 The cross-section view of the experimental devices. (a) bulk-Si and (b) CESL (contact etching stopping layer) capped devices (uniaxial-strain). Both of them are <100> channel on (100) substrate.

Procedure

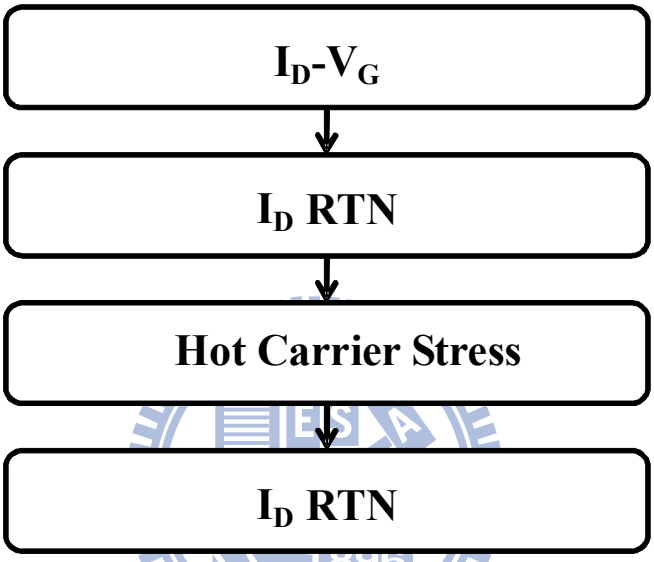


Fig. 3.2 The operating procedure of the following analysis for the devices.

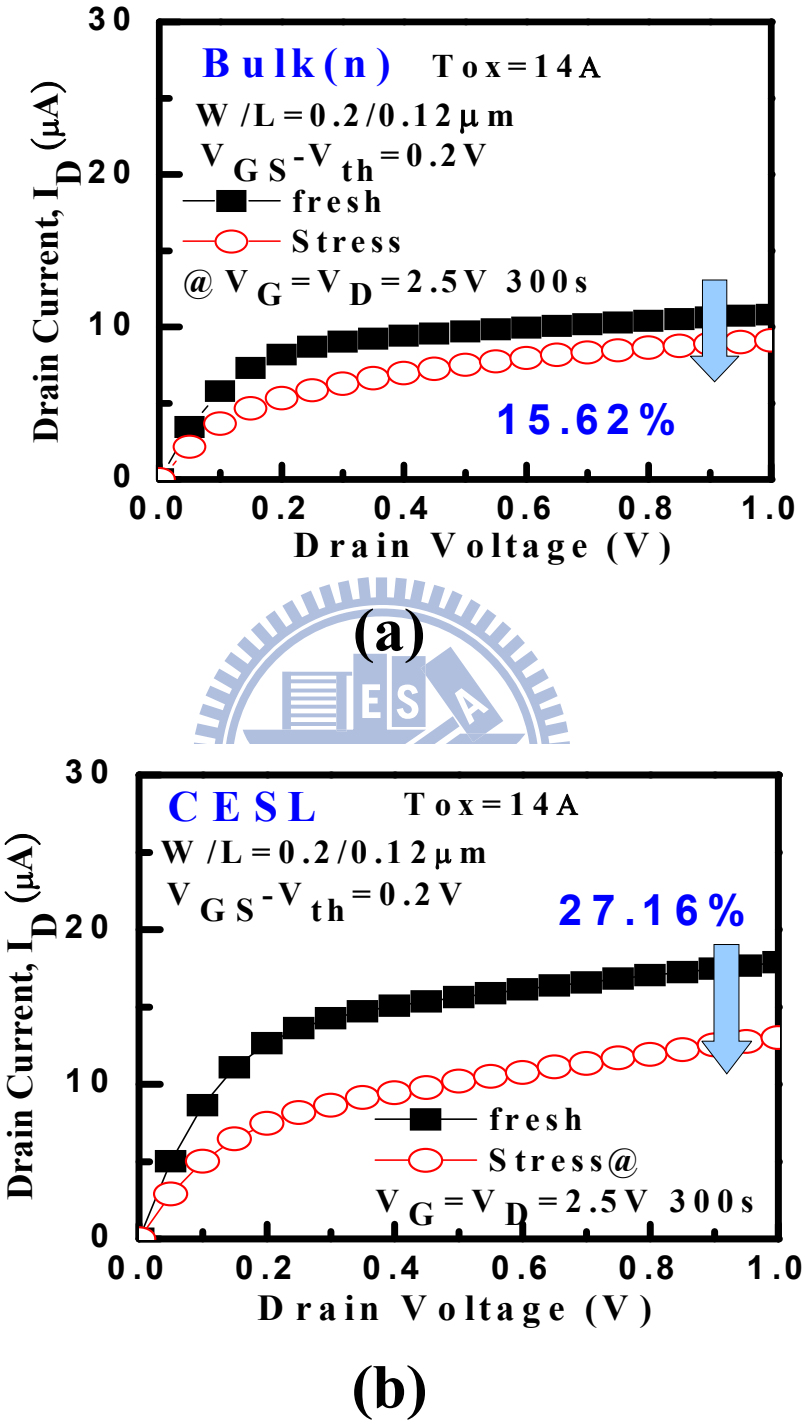


Fig. 3.3 The comparison of ID-VD characteristic in n-MOSFET devices before and after the HC stress, (a) bulk-Si and (b) CESL devices.

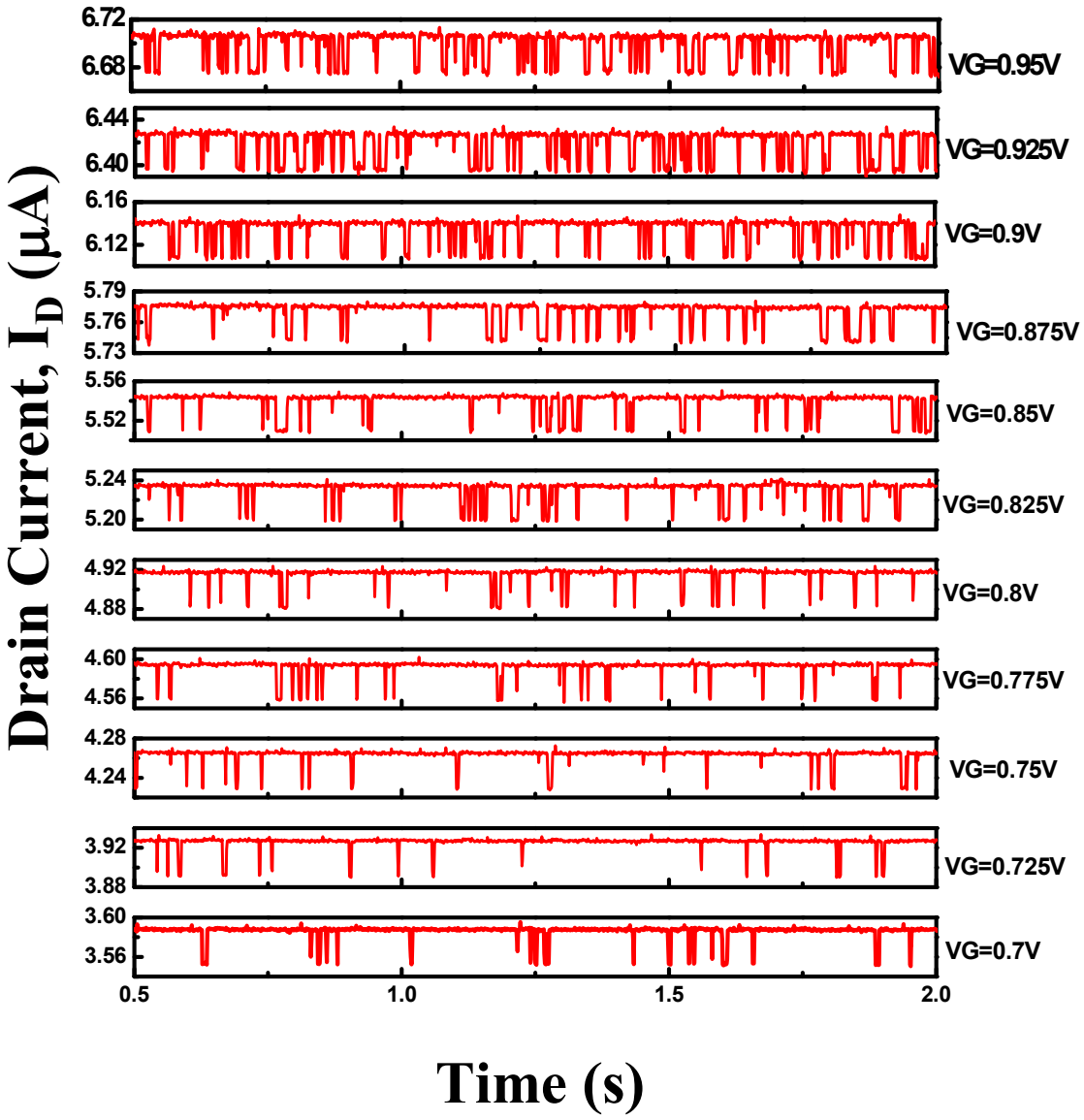


Fig. 3.4 Drain current waveform of bulk-Si device, T=25℃

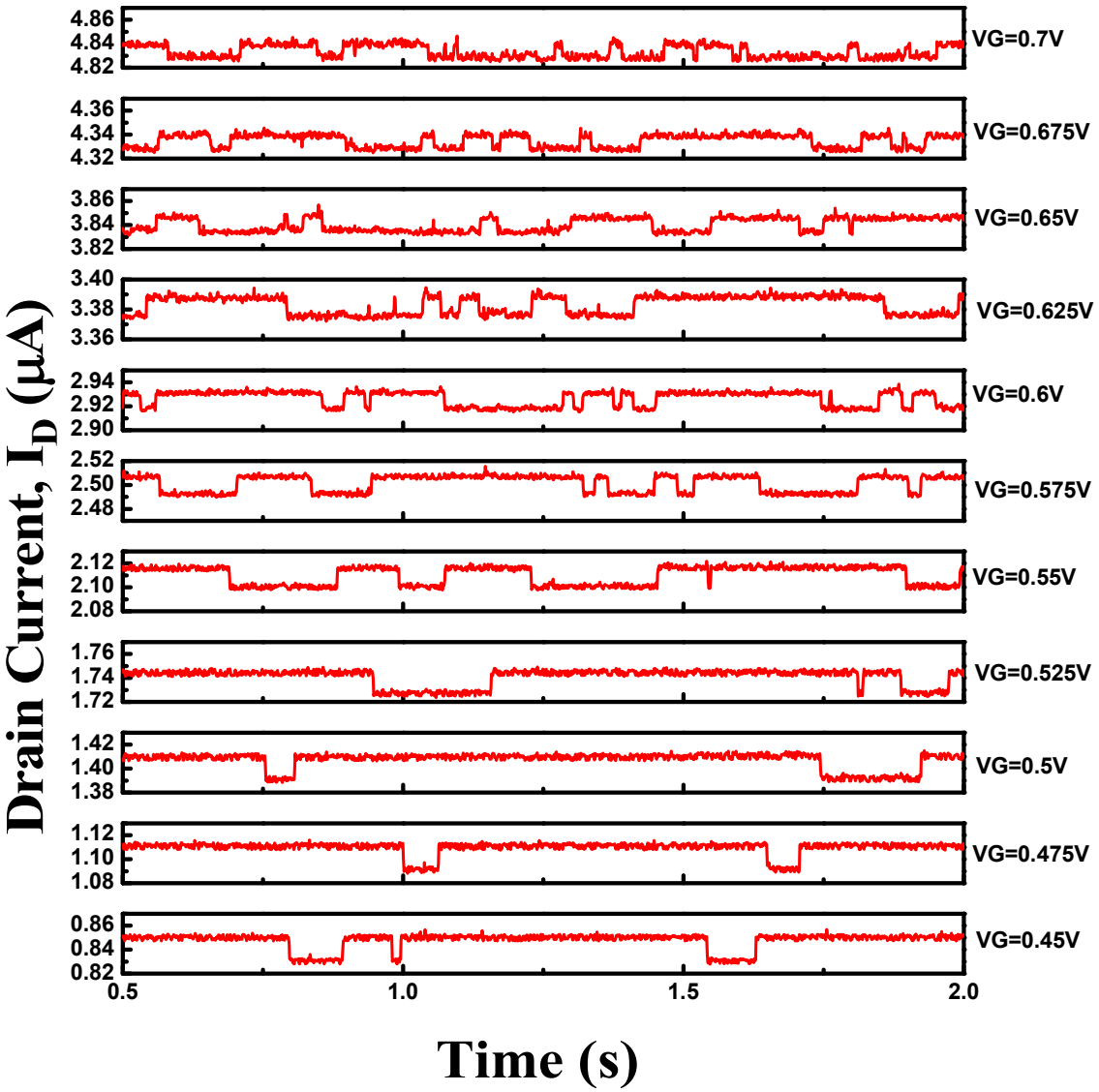


Fig. 3.5 Drain current waveform of CESL device, T=25℃

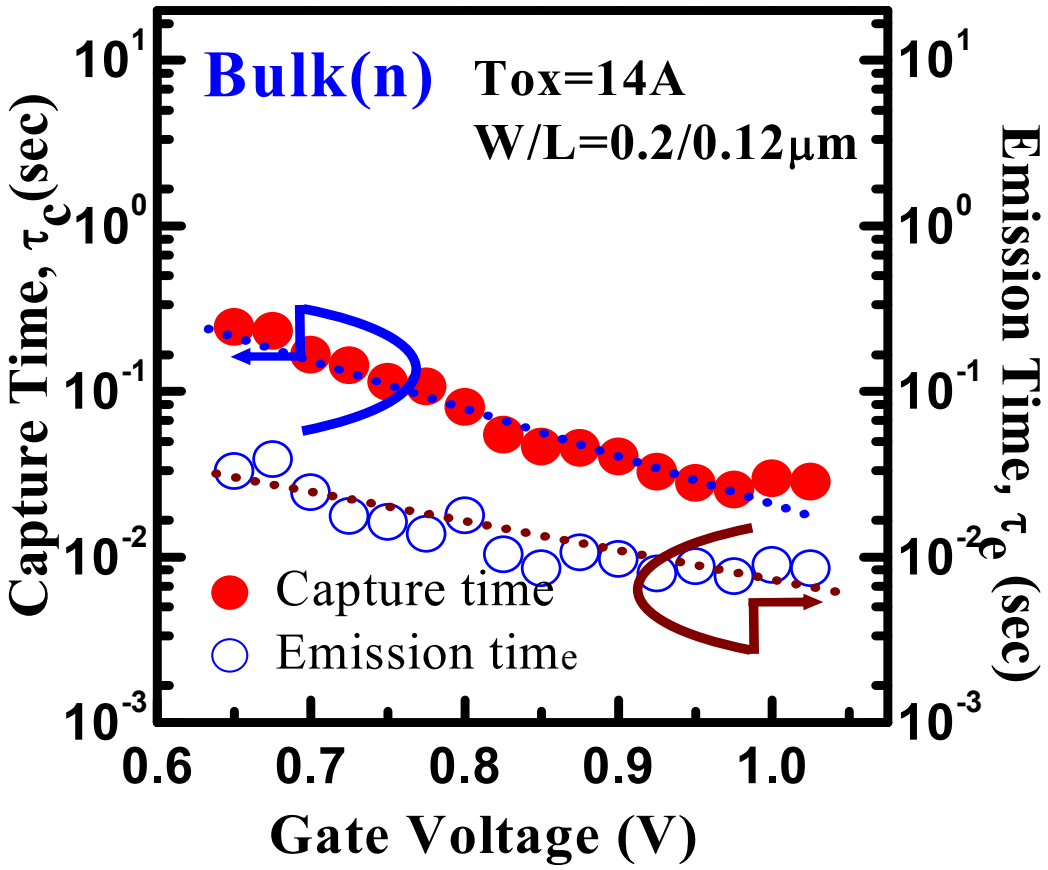


Fig. 3.6 Variation of capture time τ_c (filled symbol) and emission time τ_e (open symbol) as gate voltage increases for bulk-Si device.

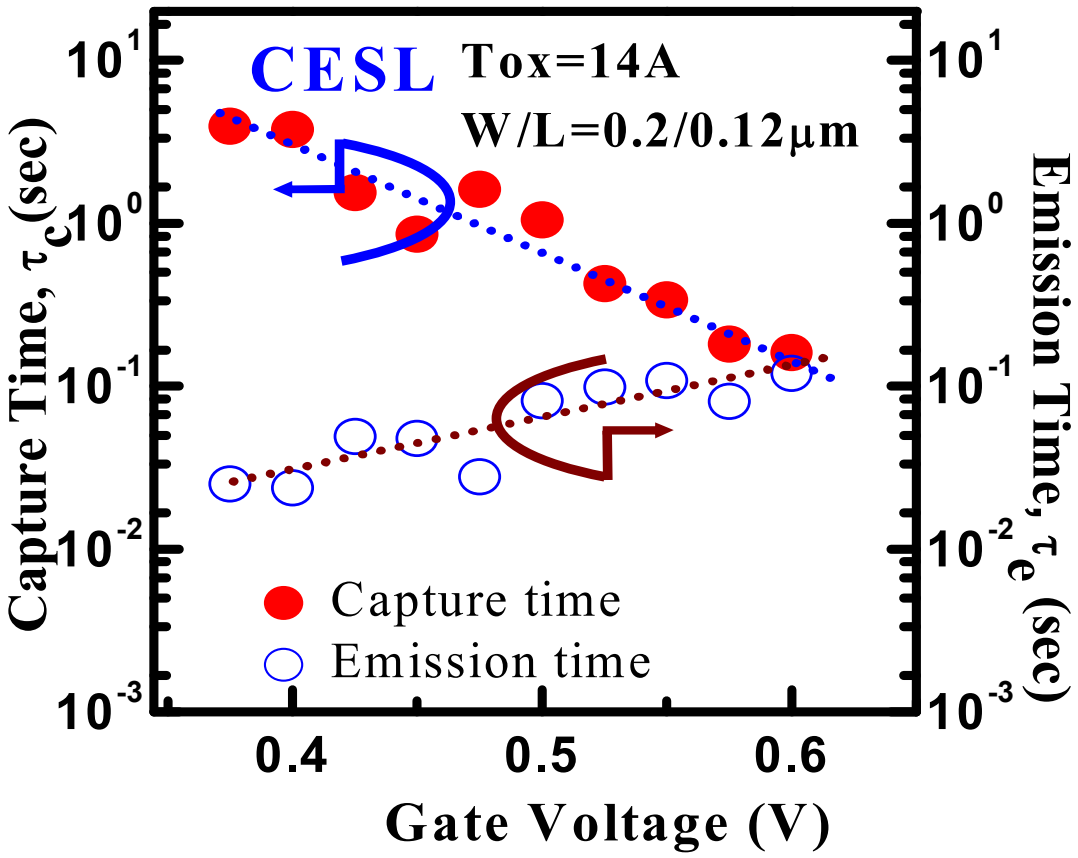


Fig. 3.7 Variation of capture time τ_c (filled symbol) and emission time τ_e (open symbol) as gate voltage increases for CESL device.

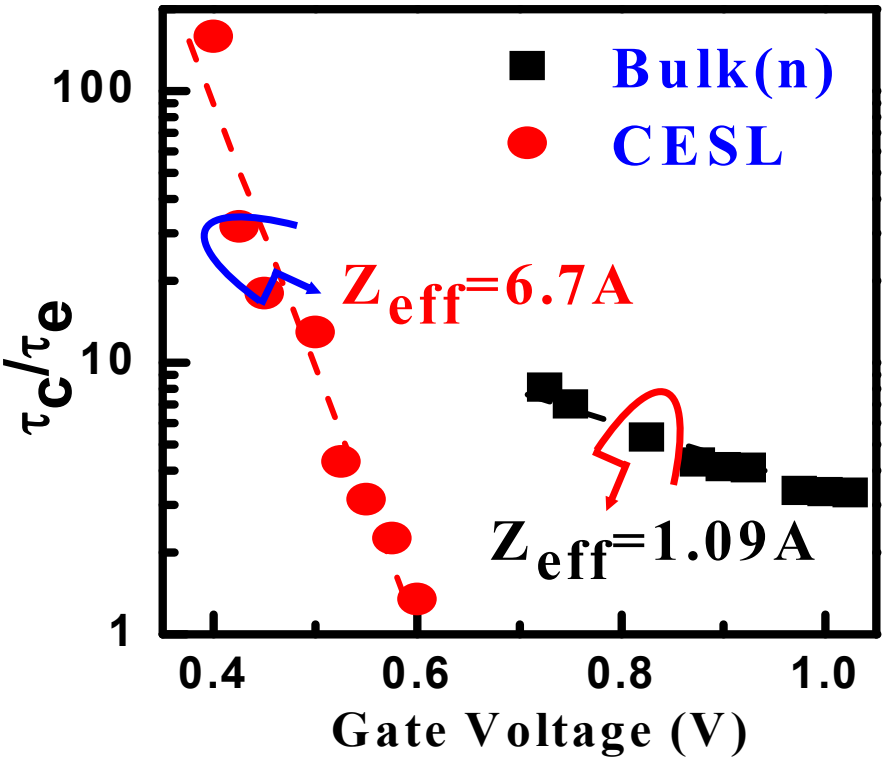


Fig. 3.8 Capture time over emission time versus gate voltage plots for n-MOSFETs.

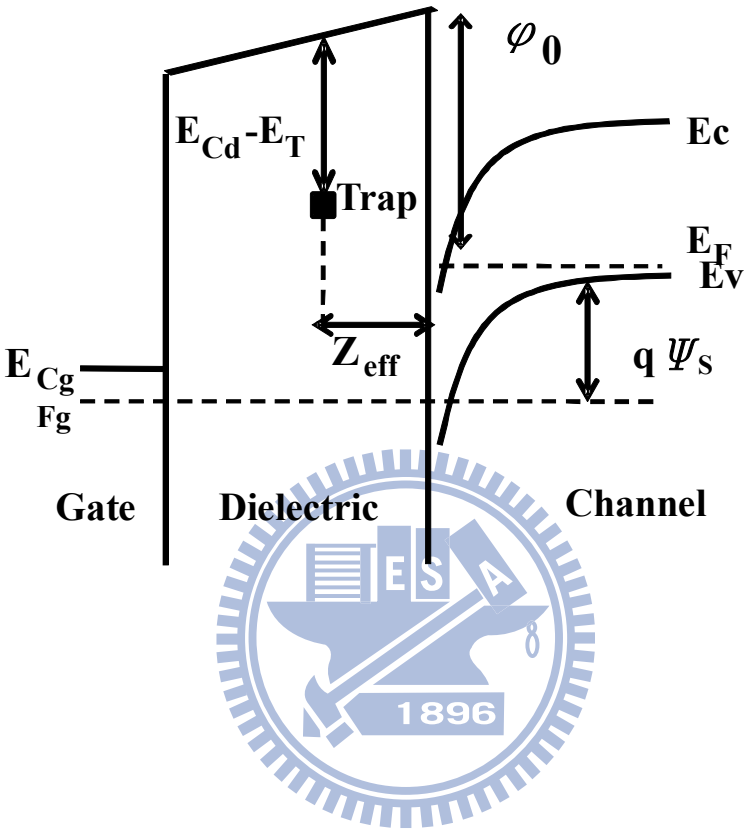


Fig. 3.9 Energy band diagram at the trap position in the channel.

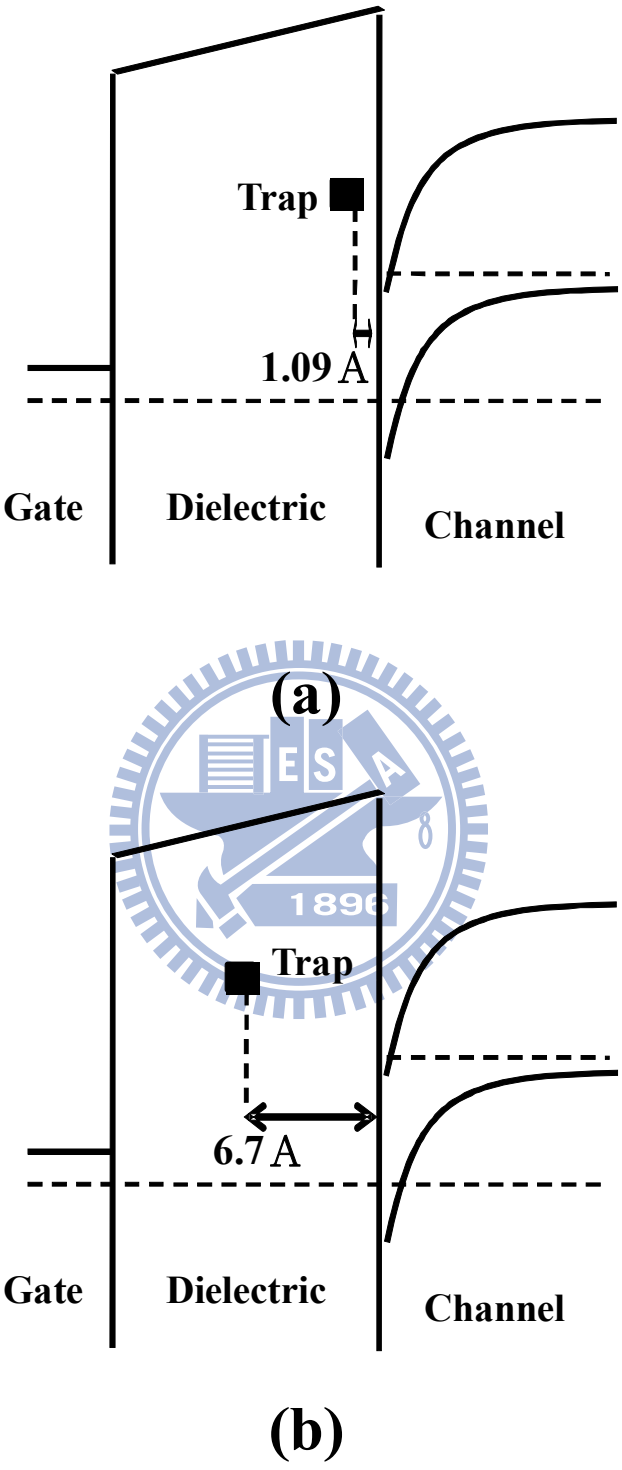


Fig. 3.10 The effective depth location for the two traps in, (a) bulk-Si and (b) CESL devices.

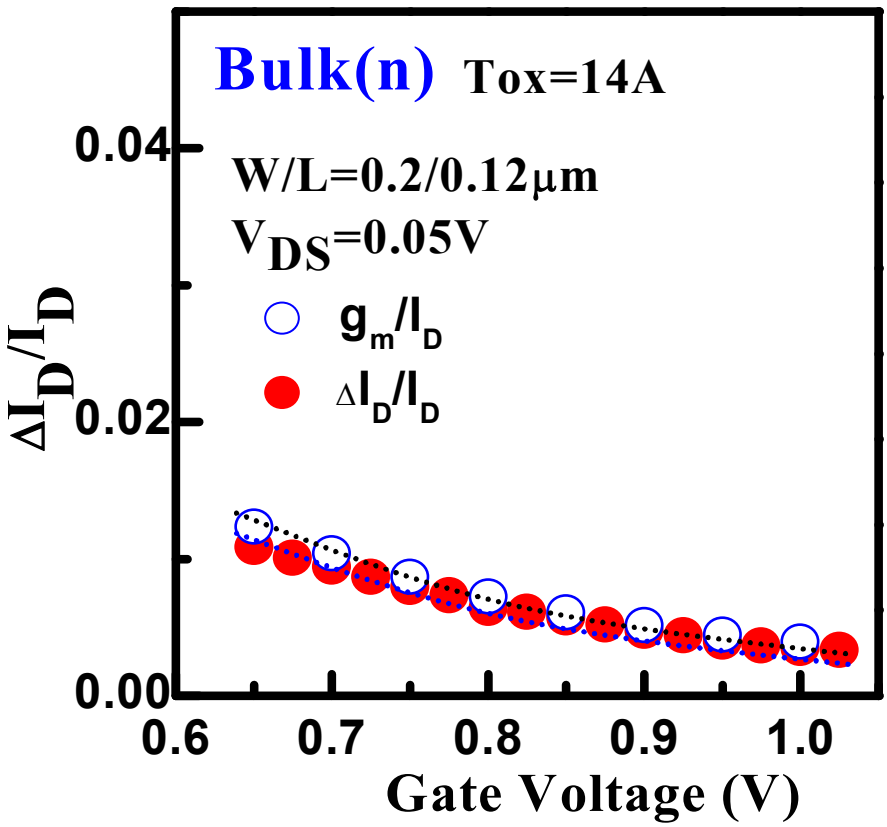


Fig. 3.11 Normalized RTN amplitude (filled symbol) and normalized conductance change (open symbol) versus gate voltage for bulk-Si device.

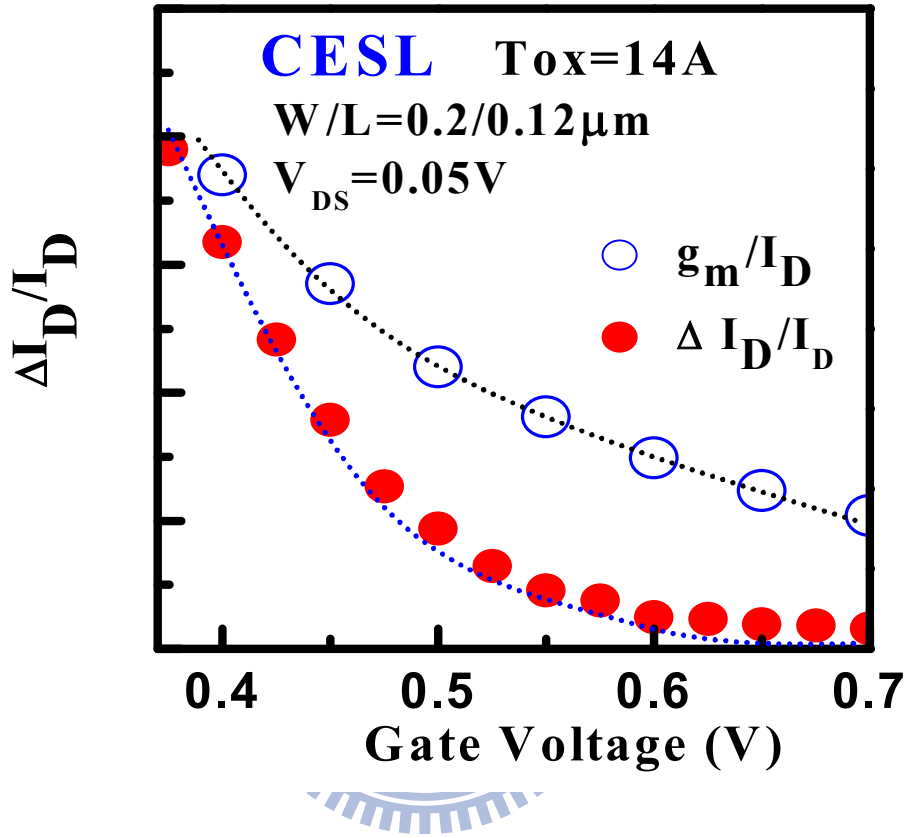


Fig. 3.12 Normalized RTN amplitude (filled symbol) and normalized conductance change (open symbol) versus gate voltage for bulk-Si device.

Chapter 4
Random Telegraph Noise of Drain Current in p-MOSFETs

4.1 Introduction

Mobility enhancement is a method to improve the CMOS devices performance with the scaling of the device size. The increase of carrier mobility is necessary to realize the high-speed CMOS devices. Recently, various strain technology have been utilized to enhance the drive current. It is necessary to understand the introduced uniaxial and biaxial strains in n-MOSFET or p-MOSFET devices. Initially, the typical mobility enhancement of n-type strained-Si is much larger than that of p-type devices. Several techniques have been further developed to enhance the p-MOSFET performance, i.e., SiGe on S/D device [4.1]. Materials with same crystal structure but different lattice are good candidates for strain engineering. The SiGe has been successfully incorporated in the source and drain of p-MOSFET devices to strain the channel compressively and increase the hole mobility. Furthermore, trapping of a single carrier charge in traps and related local modulation in carrier density and mobility exhibit a profound influence in the carrier density and mobility on the drain current. The drain current fluctuation will cause serious drawbacks on the small geometry devices.

In this chapter, the I_D-RTN "Drain Current Random Telegraph Noise" for the exploration of strain-induced slow trap properties is presented. Single electron capture and emission could be observed in strained p-MOSFETs. The analysis of the reliability will be introduced first in Section 4.3. Next, the analysis of drain current instability is

interpreted in Section 4.4. Based on the voltage dependence of single charge effect, the traps parameters are extracted and the strain process induced-effect will also be explained.

4.2 Device Preparation

The schematic cross sections of p-MOSFET splits are shown in Fig. 4-1. In this figure, Fig. 4-1(a) is the bulk-Si device, and Fig. 4-1(b) is the SiGe on source/drain device (uniaxial-strain) with EDB (Embedded Diffusion Barrier). Both p-MOSFETs are <110> channel on (100) substrate. All these test devices have 14Å EOT of SiON gate oxide and with the same dimensions, W/L = 0.2/0.12 μm. The I_D-RTN was investigated in bulk and SiGe on S/D pMOSFET devices fabricated using a conventional CMOS process flow.

4.3 The Analysis of Reliability in p-MOSFETs

4.3.1 Introduction

For many strained approach to enhance the carrier mobility, the reliabilities are still a serious issue. The biaxial strained SiGe-channel device provides good drive current enhancement, it suffers from the Ge-outdiffusion such that exhibits worse reliability. The SiGe on S/D device is a promising structure for p-MOSFET design since it keeps at about the same reliability as the SiGe-channel ones while exhibits a much higher performance. In contrast, SiGe-channel has a major concern with lattice misfit [4.2]. Besides, for p-MOSFET devices, the SiGe on S/D device with EDB [4.3] is the most promising in terms of performance and reliability.

In this section, we analyze the reliabilities of strained p-MOSFET devices and investigate them by the I_D-RTN method after hot carrier stress. We divide the contents into two main sections. The first part is to investigate hot carrier degradation and the second part is to analyze the drain current instability for p-MOSFETs. In hot carrier degradation, threshold voltage shift, drain current degradation, and transconductance degradation would be observed by electric measurement. These stresses generate the interface trap and fixed oxide charges. For the drain current instability, the stress-induced traps' properties and the relationship between the strain and the I_D-RTN results would be understood. Finally, the comparison for the strained n- and p-MOSFETs would be discussed according to the previous result.

4.3.2 Drain Current Degradation

Similar experimental procedures have been conducted for SiGe S/D device and bulk-Si p-MOSFET devices. After the hot carrier stress (V_{GS}=V_{DS}= -2.5V 300sec), Figs. 4.2 (a) and (b) show that the drain current degradation before and after the HC-stress. The drain current degradation in SiGe on S/D device is 16% and in bulk-Si device is 7.44%. The SiGe on S/D device shows large drain current degradation than bulk device, resulting from its higher impact ionization caused by the strain and the Ge out-diffusion [4.4]. The SiGe on S/D device has a larger impact ionization rate and Ge out-diffusion near the drain region which gives rise to larger drain current degradation than bulk device, caused by the impact ionization rate, the SiGe on S/D devices have a worse I_D degradation, i.e., worse immunity for hot-carrier stress.

4.4 The Analysis of I_D-RTN in p-MOSFETs

4.4.1 Drain Current Waveform

The stress induced slow oxide trap near the drain side which would cause the drain current instability (I_D-RTN) through trapping and detrapping the carriers in channel. The I_D-RTN measurements were performed in linear operation at a constant drain voltage V_{DS}= -0.05V for gate voltages $|V_{GS}|$ between 0.3 - 1 V, in steps of 20mV using HP4156. Fig. 4.3 and Fig. 4.4 show the different I_D-RTN wave spectra for bulk-Si and SiGe on S/D device respectively. The drain current amplitude is about 50nA.

4.4.2 Capture and Emission Time

From Fig. 4.3 and Fig. 4.4, we analyzed the capture and emission time for the two devices. In Fig. 4.5 and Fig. 4.6, as the gate bias increases, the capture time, τ_c decreased due to a larger carrier concentration in the channel. While the emission time, τ_e decreased with increasing gate bias which means that the carrier detraps through thermally assist tunneling to the Si. The magnitudes of τ_c and τ_e are both about 0.01~0.1 sec. As a result, both devices show similar behavior of the capture and emission of holes.

4.5 Discussion

4.5.1 Trap Depth

The relationship between the mean capture and emission times and trap parameters can be described as Eq. 3.4. The trap depth is extracted from the slope of $ln(\tau_c/\tau_e)$ versus V_G as shown in Eq. 3.5. Z_{eff} is 9.59A for bulk-Si device and 10.39A for SiGe on S/D

device shown in Fig. 4.7. Also, the depths of generated oxide traps location are about the same (~10A) in Fig. 4.8 for both devices so the capture time over the emission time take no difference in the two oxide traps (Fig. 4.7).

4.5.2 Normalized Drain Current Amplitude

The normalized change of the I_D-RTN amplitude is proportional to the normalized conduction change for both devices (Fig. 4.9 and Fig. 4.10). This implies that the generated slow oxide trap in SiGe on S/D follows the same mechanism as that of bulk device.

4.6 The Comparison Between n- and p-MOSFETs

4.6.1 Introduction

The hot carrier degradation of the CMOS devices with various strain technologies were enhanced by high lateral acceleration and larger impact ionization current. The worst case of hot carrier degradation occurs at V_{GS}= V_{DS} condition and the degradation will follow the trend of impact ionization rate and effective mobility. In addition to the discussion on the reliabilities of uniaxial strained CMOS devices, for the first time, the I_D-RTN for the strained-Si devices is analyzed. In order to identify the differences of previous experimental results, the strain effects in CESL device and SiGe on S/D devicecan be identified by Fig. 4.11. The capping layer in the n-MOSFET devices provides the tensile strain along the channel direction and also the compressive strain along the vertical direction [4.5]. The SiGe on S/D devices inducing the compressive strain along the channel region gives rise to the hole mobility enhancement.

4.6.2 Charge Pumping Measurement

The charge pumping (CP) measurement is efficient for the reliability characterization. However, the charge pumping measurement can't be used reliably in the small size devices due to the small charge pumping current and the gate leakage current. Recently a low leakage IFCP measurement for COMS devices has been developed [4.6] to get more reliable results. In order to investigate the interface's degradation information, we used the low leakage IFCP measurement for the stressed devices.

4.6.2.1 Experimental Results

We took charge pumping measurements which can be used to calculate the information of the degradation for the interface only. As a figure of merit, in Fig. 4.12, for the comparison the degradation caused by the interface 1.26 times larger in CESL device than in bulk-Si device, while the I_D degradation shows a factor of 1.69 times larger for CESL device comparing to the bulk-Si device in Fig. 4.13 .

As a result, the difference of 1.69 and 1.26 will give a difference of 0.43 times of the total drain current degradation. This is the contribution from the strain in the vertical direction as show in Fig. 4.11.

4.6.3 I_D-RTN: Normalized Drain Current Amplitude

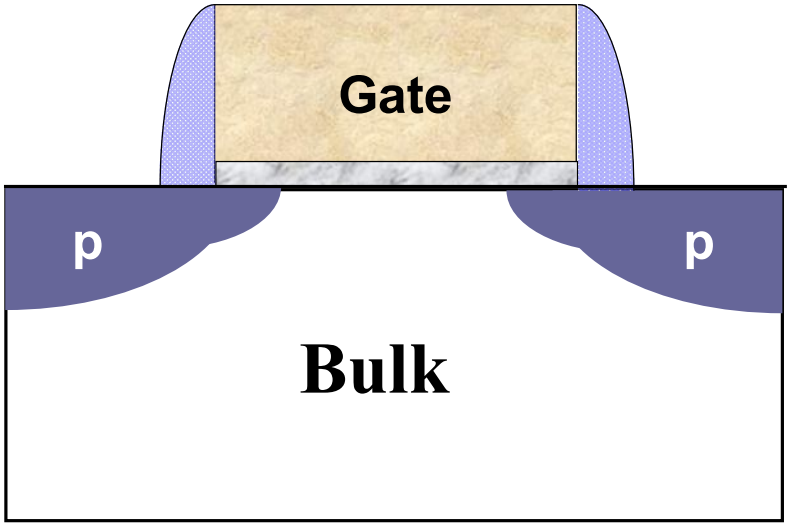
Under the strong inversion, for comparable N_s (carrier concentration), $\Delta I_D/I_D$

(normalized current amplitude) should be proportional to the mobility [4.7]. From Fig. 4.14, the $\Delta I_D/I_D$ roll-off more quickly in the CESL device compared to the bulk-Si device, while the SiGe on S/D device and bulk-Si device show comparable trend. Because of the extra vertical strains in the CESL device gate dielectric (Fig. 4.11), this would cause more scattering and degrade the Si/SiO_2 interface quality after the HC stress.

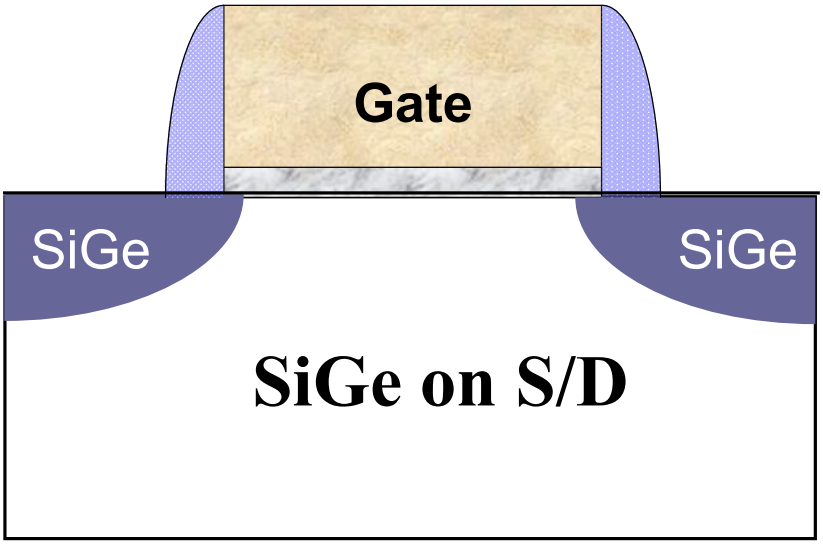
4.6.4 Discussion

The vertical strain on the gate oxide causes higher mobility degradation in CESL device than bulk-Si device, in poly-Si gated devices. We believe that the drain current degradation between n-MOSFET and p-MOSFET could be due to the extra strain stress on the gate dielectric.

The vertical strain causes about 0.43 times of the total drain current degradation (~one-quarter of the total degradation). As a result: (1) the strain techniques can enhance the device performance while on the contrary they show poorer got carrier reliabilities, (2) more scattering is induced by the CESL strain (as observed in n-MOSFET) which can induce the mobility degradation and make worse the device reliability.

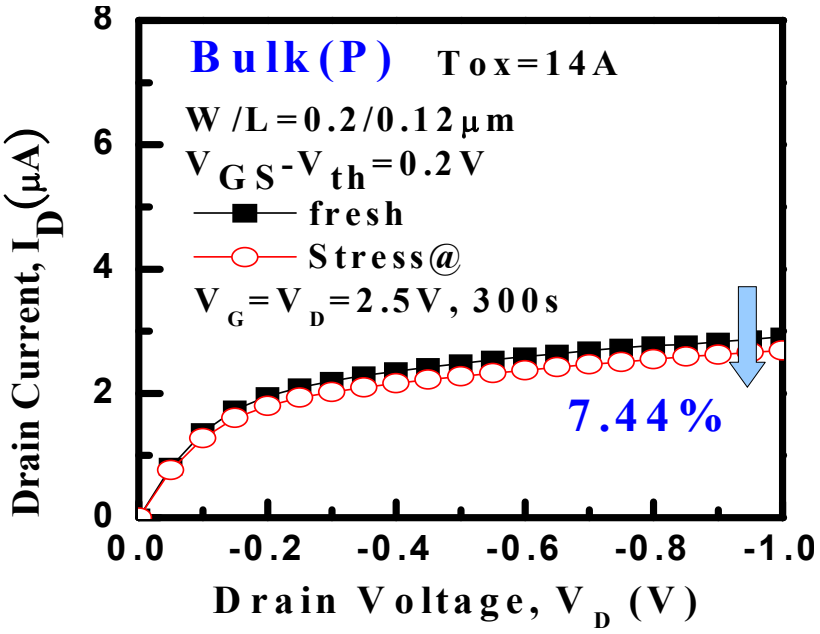


(a)

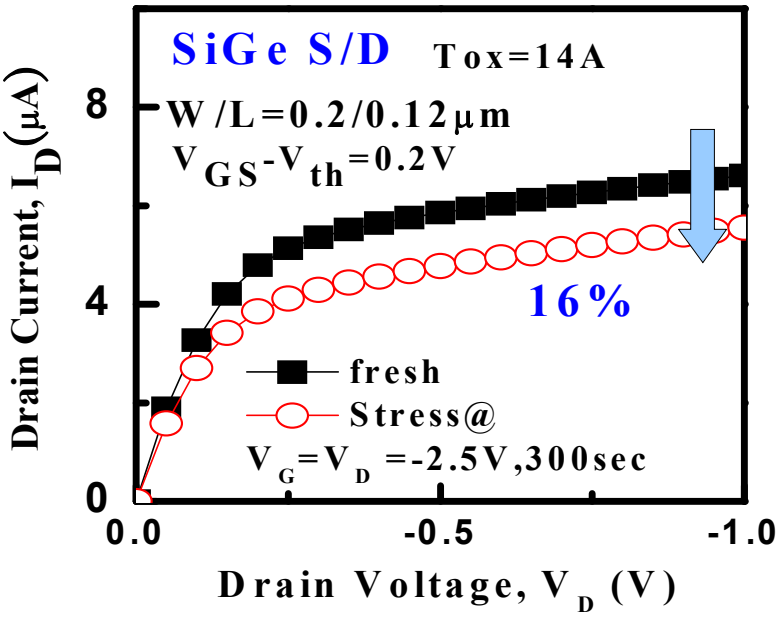


(b)

Fig. 4.1 The cross-section view of the experimental devices, (a) bulk-Si and (b) SiGe on S/D device (biaxial-strain). Both of them are <110> channel on (100) substrate.



(a)



(b)

Fig. 4.2 The comparison of ID-VD characteristic in p-MOSFET devices before and after the HC stress, (a) bulk-Si and (b)SiGe S/D devices.

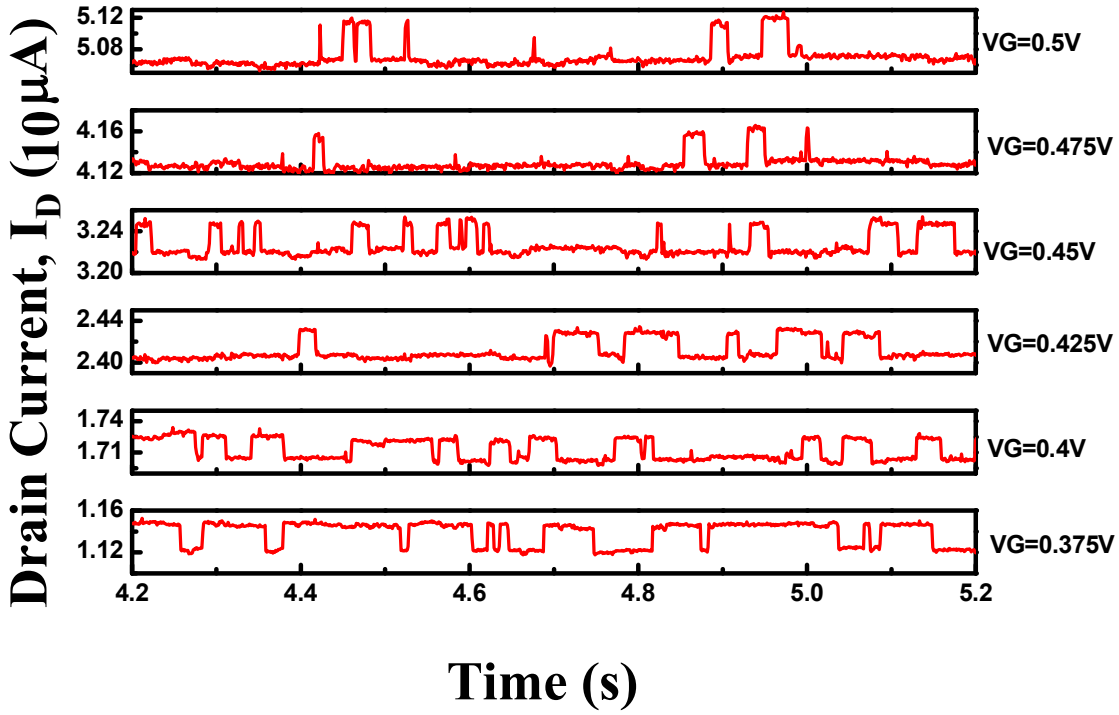


Fig. 4.3 Drain current waveform of bulk-Si device, T= 25℃.

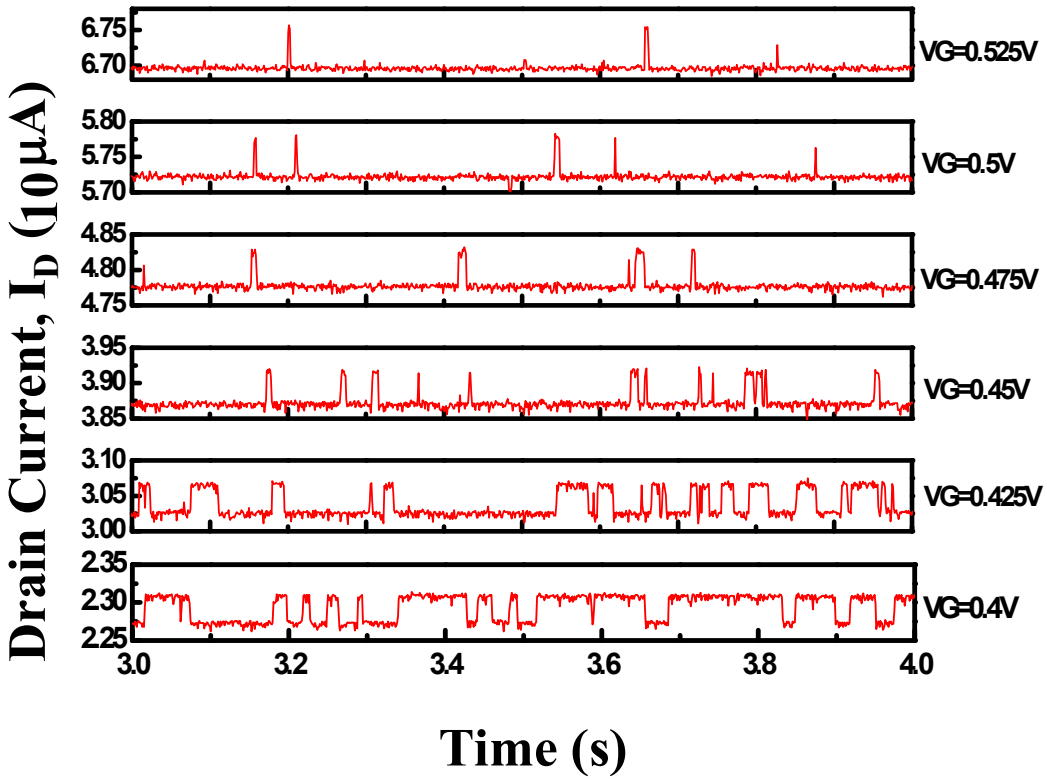


Fig. 4.4 Drain current waveform of SiGe S/D device, T= 25℃.

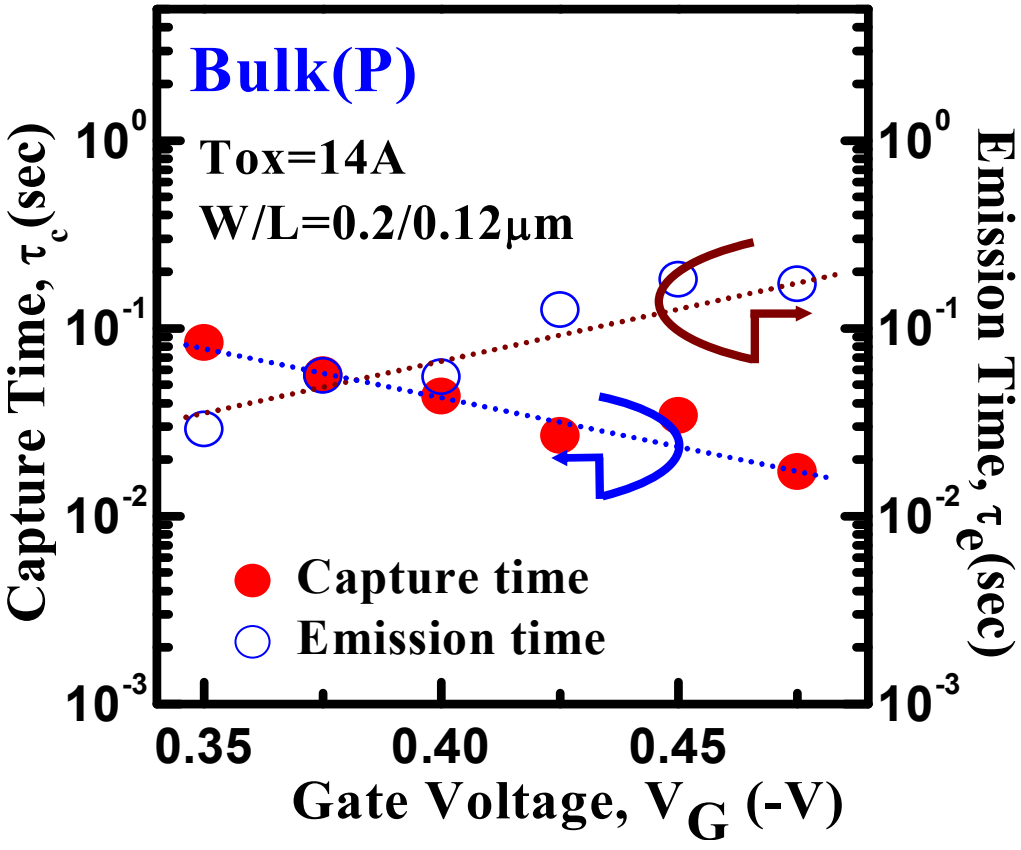


Fig. 4.5 Variation of capture time τ_c (filled symbol) and emission time τ_e (open symbol) as gate voltage increases for bulk-Si device.

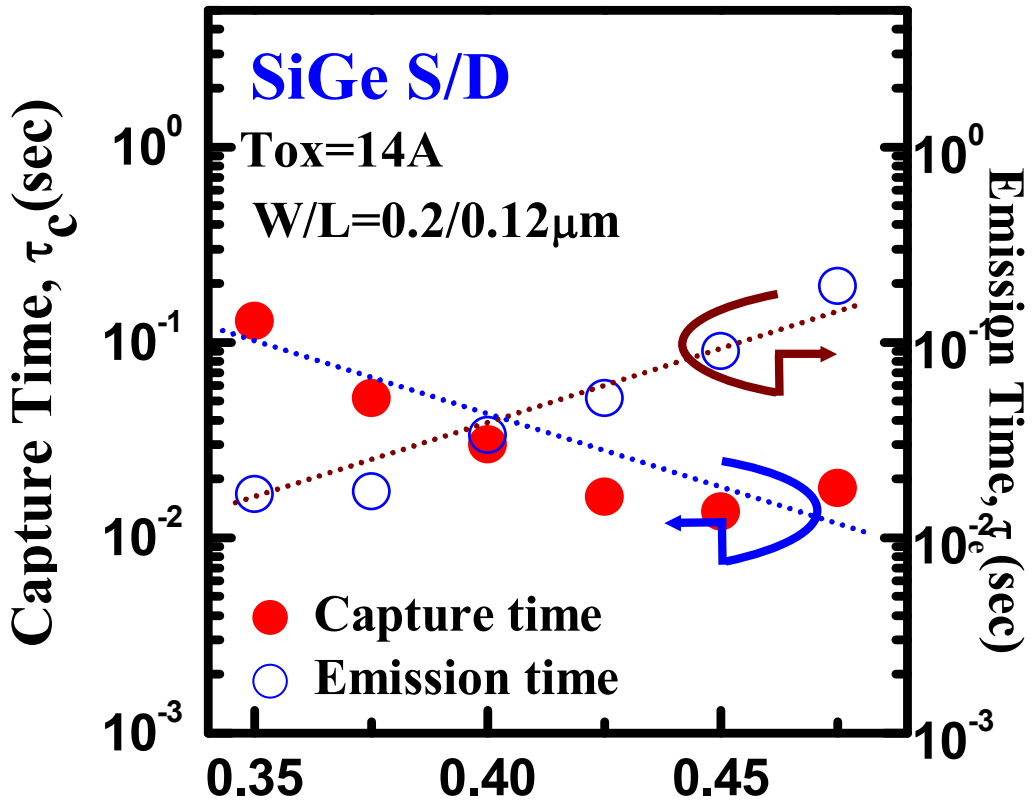


Fig. 4.6 Variation of capture time τ_c (filled symbol) and emission time τ_e (open symbol) as gate voltage increases for SiGe on S/D device.

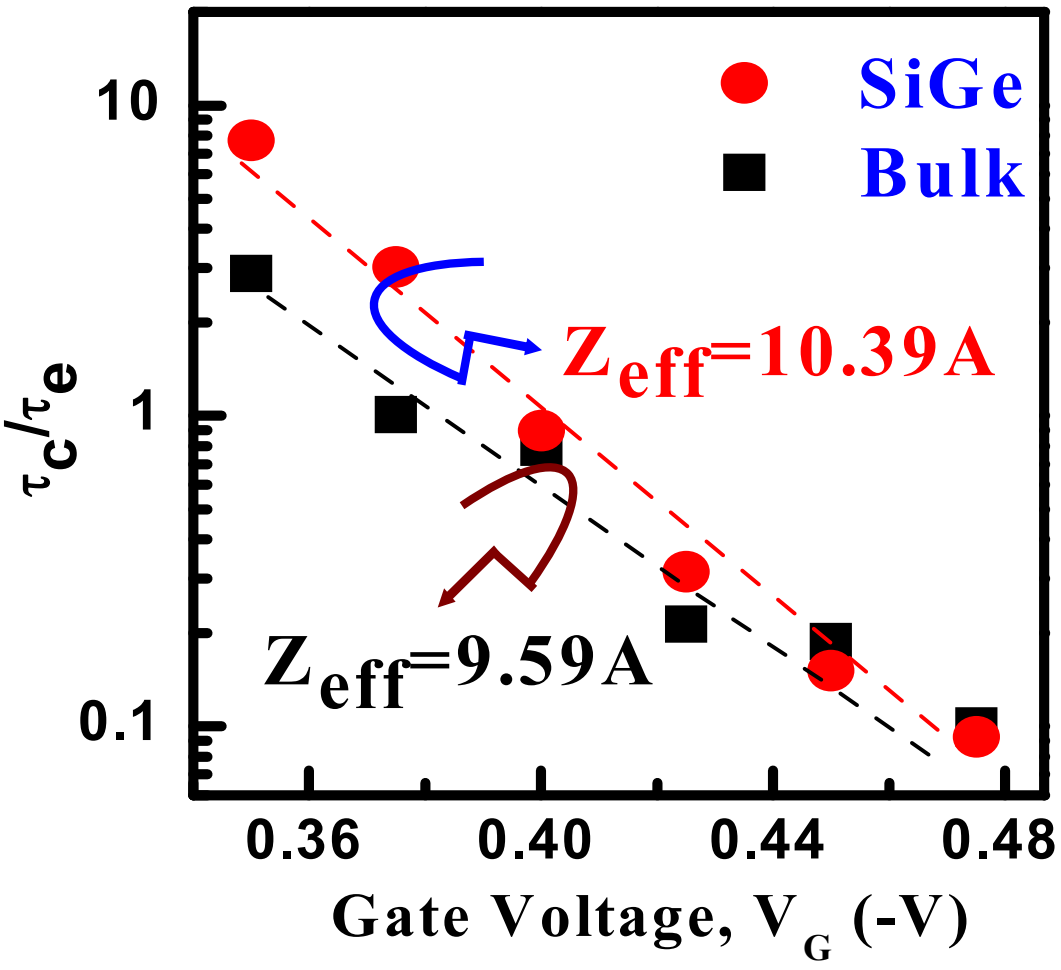


Fig. 4.7 Capture time over emission time versus gate voltage plots for p-MOSFETs.

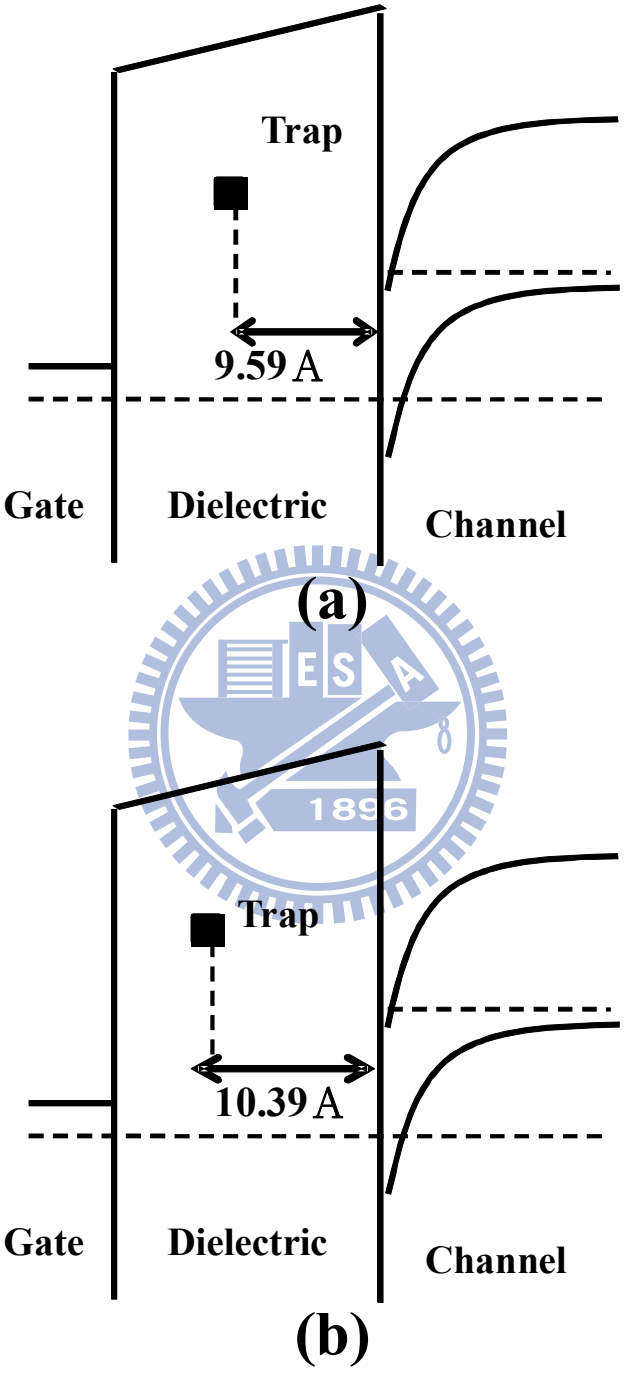


Fig. 4.8 The effective depth location for the two traps in, (a) bulk-Si and (b) SiGe on S/D devices.

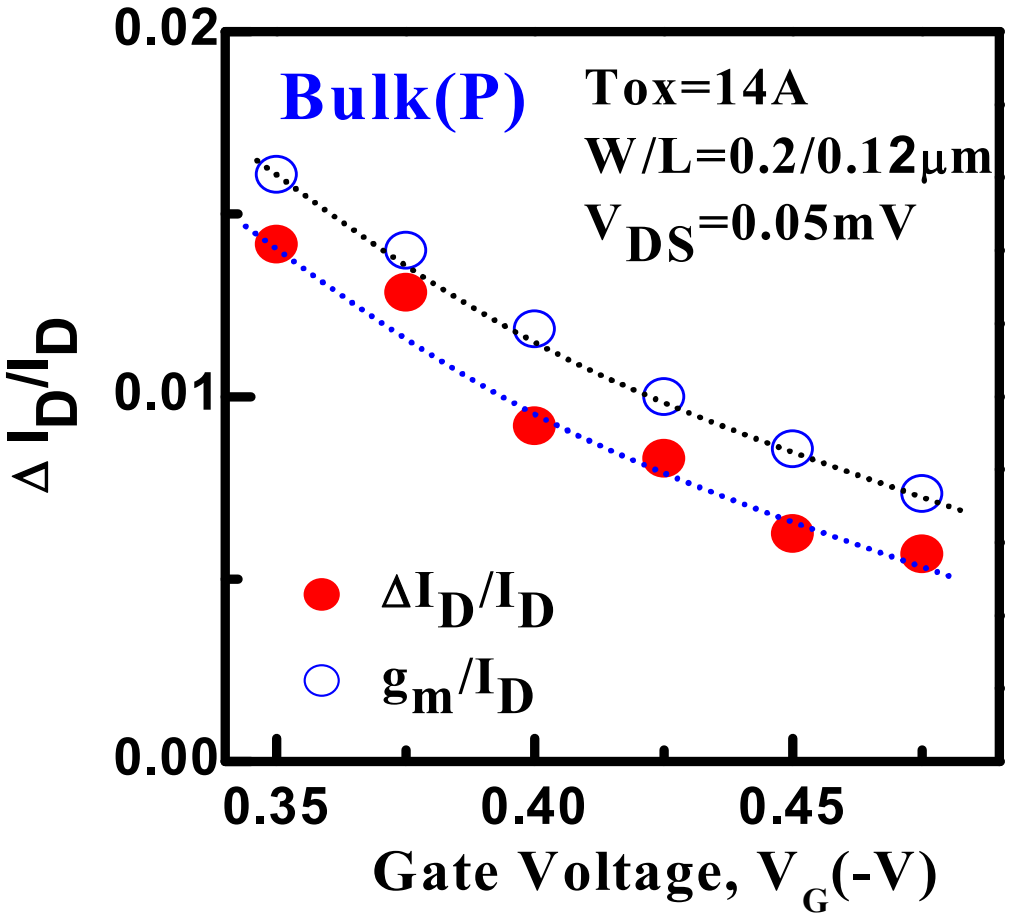


Fig. 4.9 Normalized RTN amplitude (filled symbol) and normalized conductance change (open symbol) versus gate voltage for bulk-Si device.

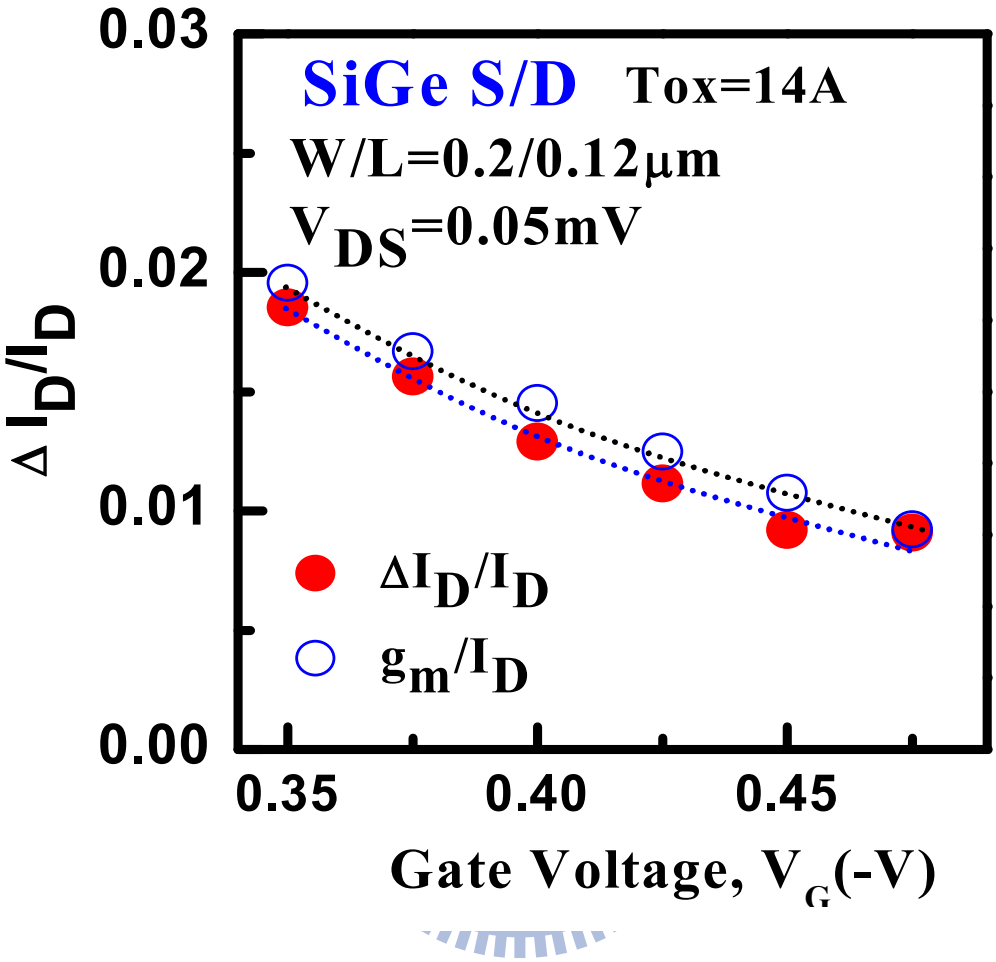


Fig. 4.10 Normalized RTN amplitude (filled symbol) and normalized conductance change (open symbol) versus gate voltage for SiGe on S/D device.

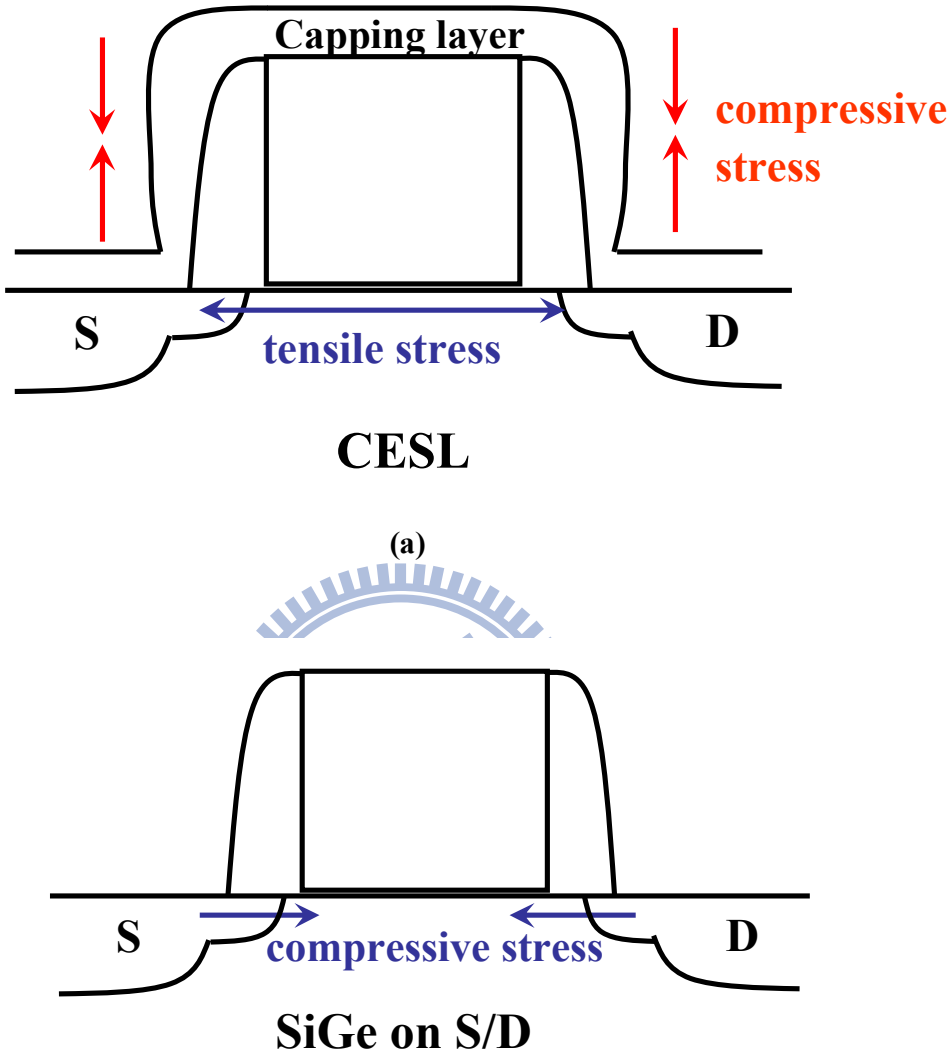


Fig. 4.11 Illustration of the various strains for (a) CESL and (b) SiGe on S/D devices.

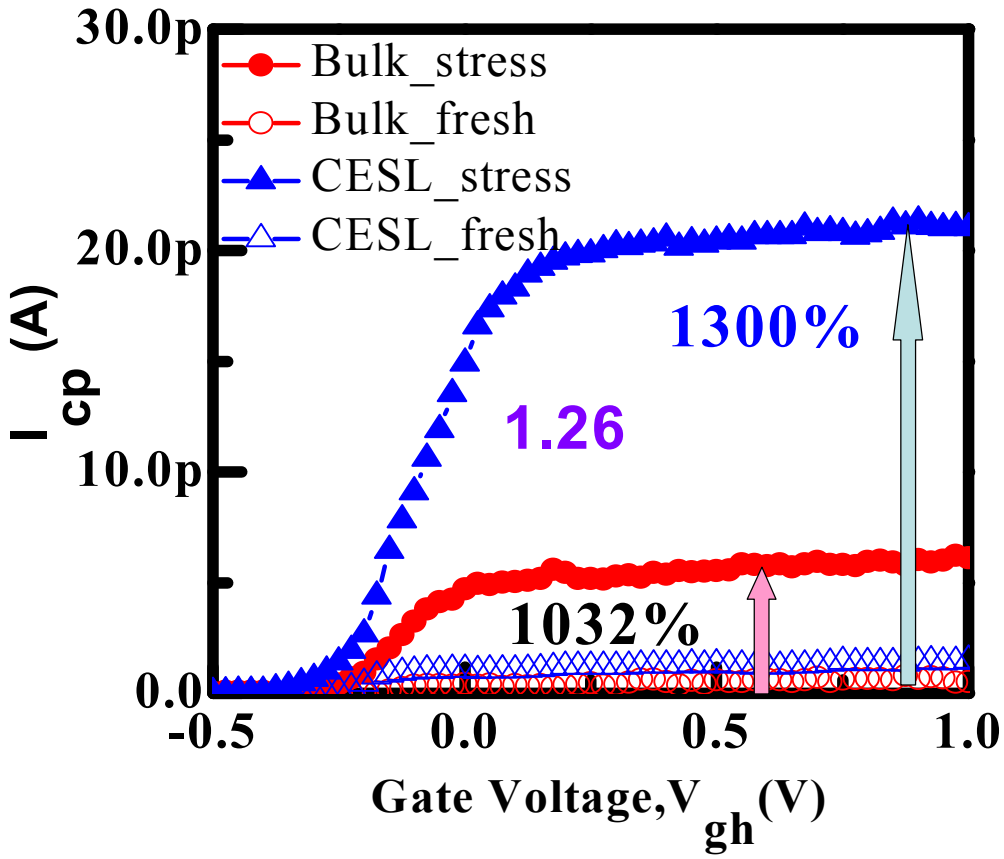


Fig. 4.12 Comparison of charge pumping current for bulk-Si and CESL devices

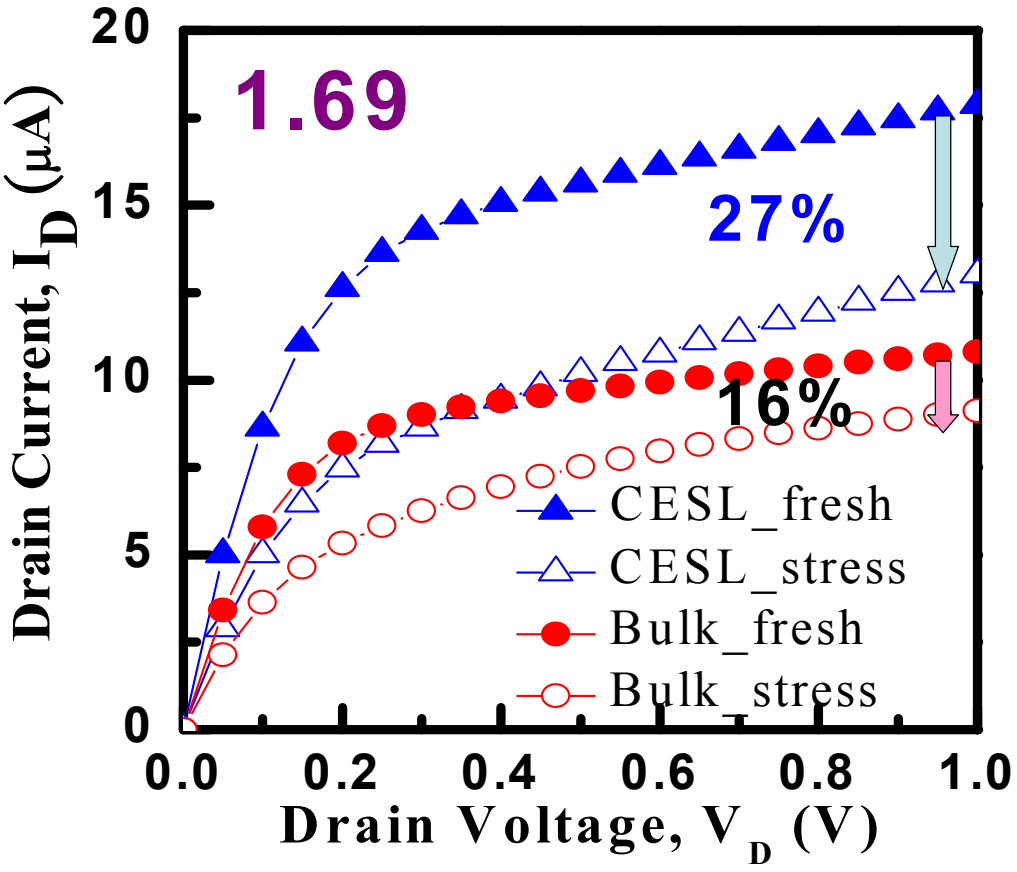


Fig. 4.13 Comparison of drain current degradation for bulk-Si and CESL devices.

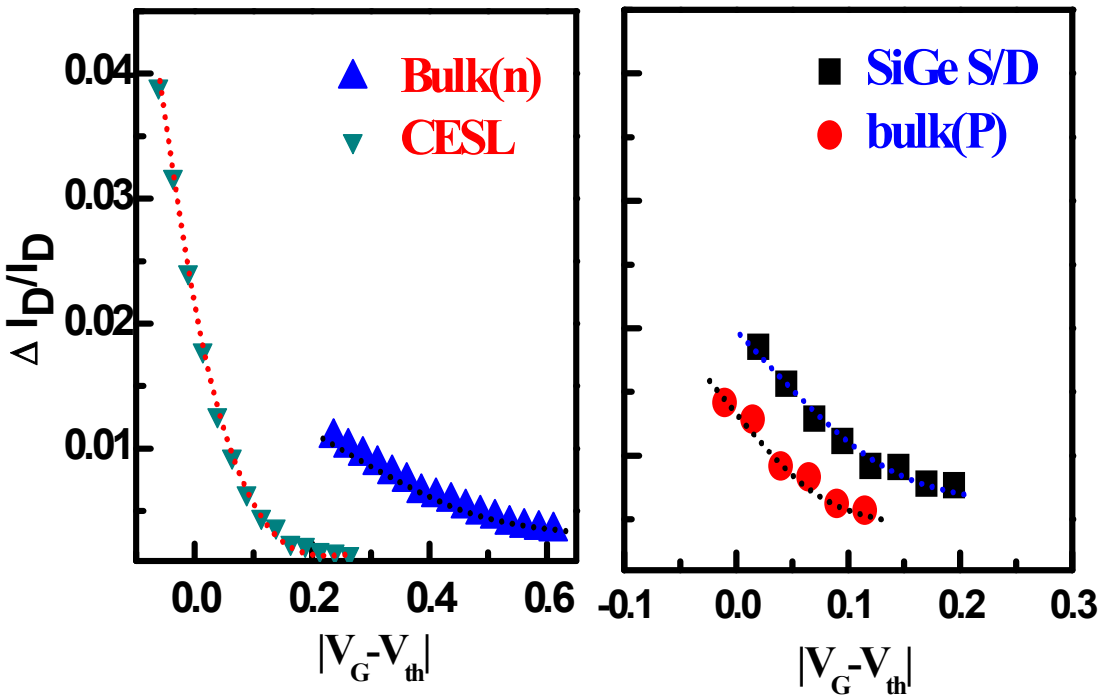


Fig. 4.14 Normalized current amplitude versus overdrive voltage. (left) n-MOSFETs (right) p-MOSFETs. Note that the huge drop for CESL device is caused by the vertical strain in CESL device.

Chapter 5
Application to Strained SiC Devices

5.1 Introduction

Strained silicon channel has become an essential component of modern high-performance CMOS technology. In order to overcome the MOSFET device scaling difficulties, various strained-Si schemes have become essential components for 45 nm and beyond. Recently, strained n-MOSFET with embedded Si:C on source and drain has received much interest owing to its good scalability for gate length small than 40nm [5.1]. With the same lattice constant that is smaller than Si, silicon carbon alloy (Si:C) embedded in the source and drain can provide tensile strain along the channel direction and enhance the electron mobility for n-MOSFET. The SiC on S/D is a superior stressor compared to SMT and shows better scalability for high performance thin-oxide short channel n-MOSFET [5.2] [5.3].

In this chapter, the application to the SiC device would be illustrated by the I_D-RTN method. The experiment results would also be discussed and compared with the pervious chapters' result.

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5.2 Device Preparation

The devices were fabricated by the advanced 40nm technology. The schematic cross section diagram of n-MOSFET splits is shown in Fig. 5-1. In this figure, Fig. 5-1(a) is the bulk-Si device, and Fig. 5-1(b) is the SiC on S/D device (uniaxial-strain). Both

n-MOSFETs are <100> channel on (100) substrate. All these test devices have 12Å EOT gate oxide with SiON process and with the same dimension (W/L= 0.2/0.04um).

5.3 The Analysis of Reliability in SiC devices

5.3.1 Introduction

Comparing to the bulk device, the SiC on S/D device shows good drive current and enhancement of channel mobility. Although SiC on S/D device is an alternative for high current enhancement, its off-state junction leakage is a serious problem for reliability [5.4]. In this chapter, we take similar analysis in the SiC on S/D device for the HC reliability issues and the I_D-RTN experiments after hot carrier stress. In the first part, the HC reliability results would be investigated. In the second part, the I_D-RTN in bulk-Si and SiC on S/D devices would be studied for the stress-induced traps' properties and the relationship between the strain's directions.

5.3.2 Drain Current Degradation

The HC stress condition is V_{GS}= V_{DS}= 2V 500sec for the two samples. Fig. 5.2 shows that the drain current degradation before and after the HC-stress. The drain current degradation in bulk is 8.06% and in SiC on S/D device is 11.9%. The drain current degradation is enhanced in the SiC on S/D device comparing to the bulk devices, as result of its higher impact ionization caused by the strain.

5.4 The Analysis of I_D-RTN in SiC Devices

5.4.1 Drain Current Waveform

The stress induced slow oxide trap near the drain side which would cause the drain current instability (I_D-RTN) through trapping and detrapping of the channel carriers. The I_D-RTN measurements were performed in the linear operation at a constant drain voltage V_{DS}= 0.05V for gate voltages V_{GS} between 0.64~0.78 V, in steps of 20mV using HP4156. Fig. 5.3 and Fig. 5.4 show the different I_D-RTN wave spectra for bulk-Si and SiC on S/D device respectively. The drain current amplitude is about 100nA.

5.4.2 Capture and Emission Time

The extracted capture time and emission are shown in Fig. 5.5and Fig. 5.6. We can see the similar behavior of the capture and emission of electrons in the two devices.

5.5 Discussion

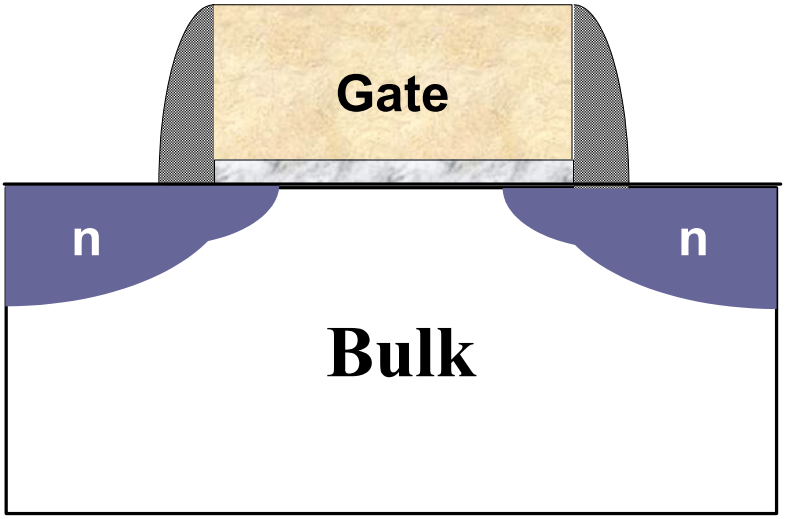
5.5.1 Depth

Also, from the τ_c/τ_e(versus Vg curve), Fig. 5.7, we can calculate the effective trap depth Z_{eff} from the slope. The depth in bulk is about 5.15A and in SiC on S/D device is about 8.45A. The trap location is deeper in SiC on S/D device than in bulk-Si , as shown in Fig. 5.8 which implies that HC stress produces more damage in the Si/SiO_2 for the SiC on S/D device.

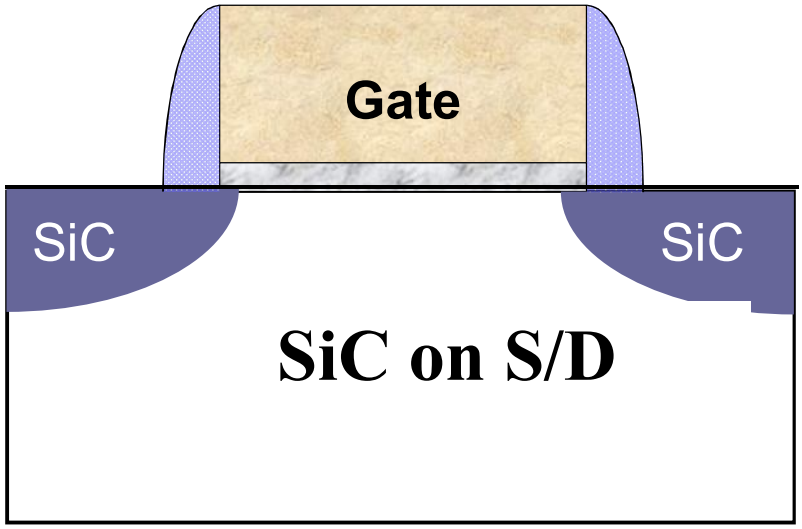
5.5.2 Normalized Drain Current Amplitude

The RTN amplitude, ΔI_D divided by the I_D becomes the normalized current amplitude. From Fig. 5.9 and Fig. 5.10, the normalized current amplitude is proportional to the normalized conductance change, gm/I_D in the bulk-Si device and SiC on S/D device which implies that the generated slow oxide trap in SiGe on S/D device follows the same mechanism as that of the bulk device. In the SiC on S/D device, the SiC on S/D device will induce the tensile strain along the channel direction to enhance the electron mobility.

As a result, although both CESL and SiC on S/D devices use the uniaxial strain technology to enhance the mobility, there is no extra vertical strain in SiC on S/D device gate dielectric to cause more scattering and degrade the Si/SiO_2 interface quality. As a result, the normalized I_D-RTN amplitudes have the same trend for SiC on S/D and bulk-Si devices.

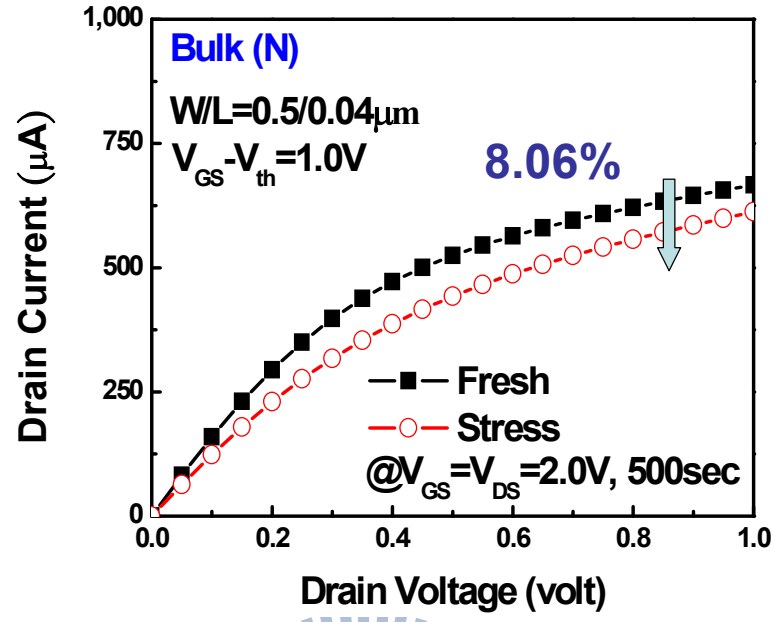


(a)

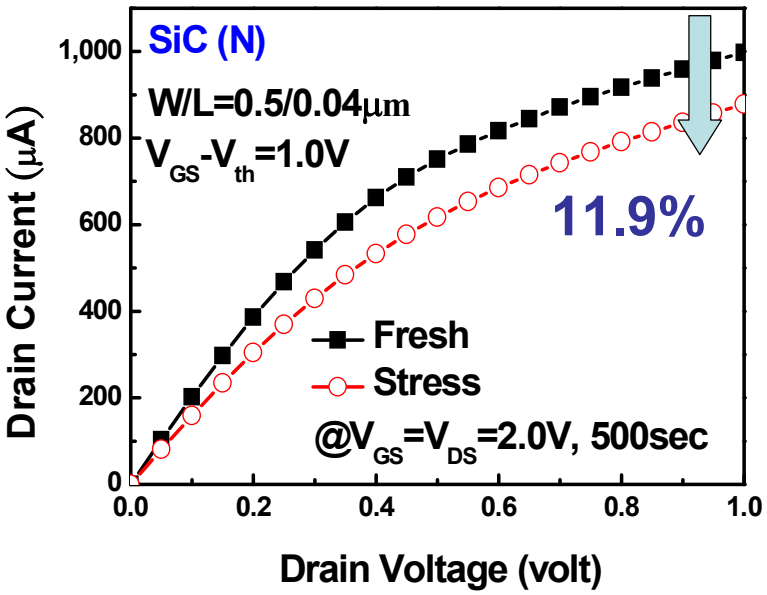


(b)

Fig. 5.1 The cross-section view of the experimental devices, (a) bulk-Si and (b) SiC on S/D devices (uniaxial-strain). Both of them are <100> channel on (100) substrate.



(a)



(b)

Fig. 5.2 The comparisons of ID-VD characteristic in n-MOSFET devices before and after the HC stress, (a) bulk-Si and (b) SiC on S/D devices.

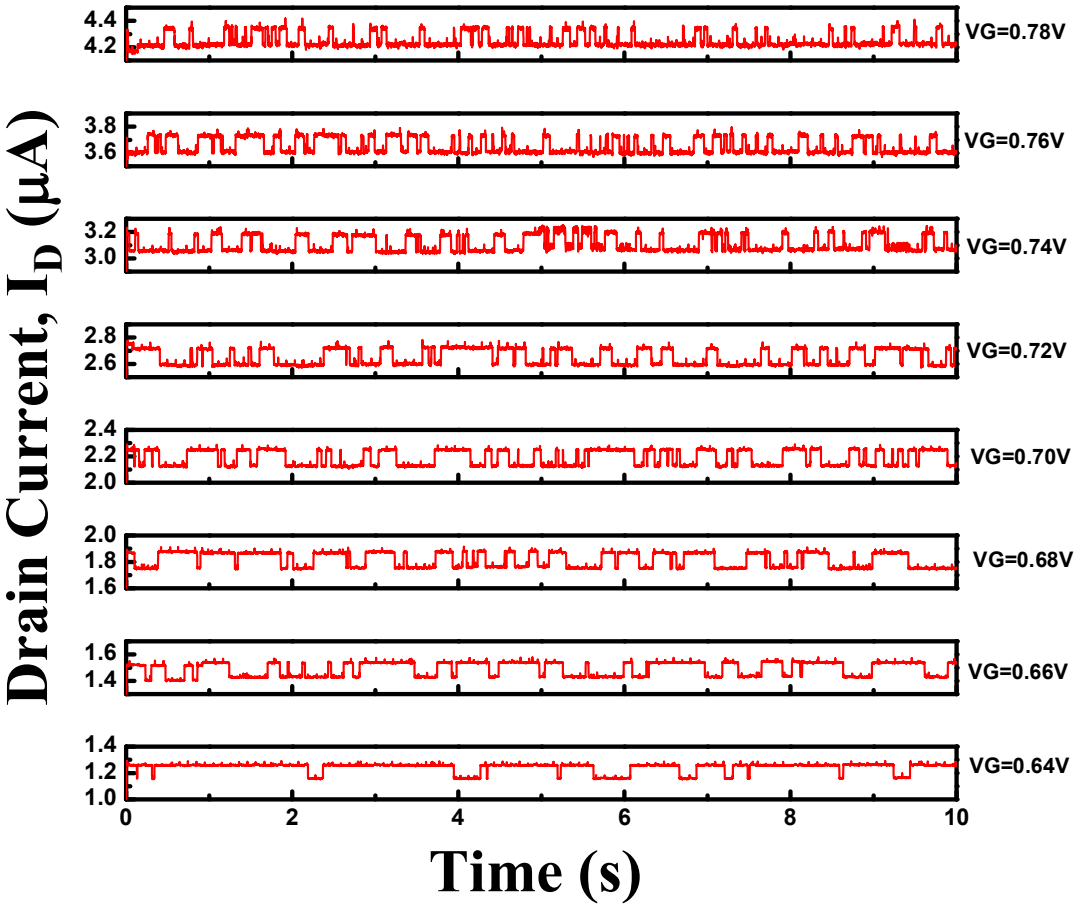


Fig. 5.3 Drain current waveform of bulk-Si device, T=25℃.

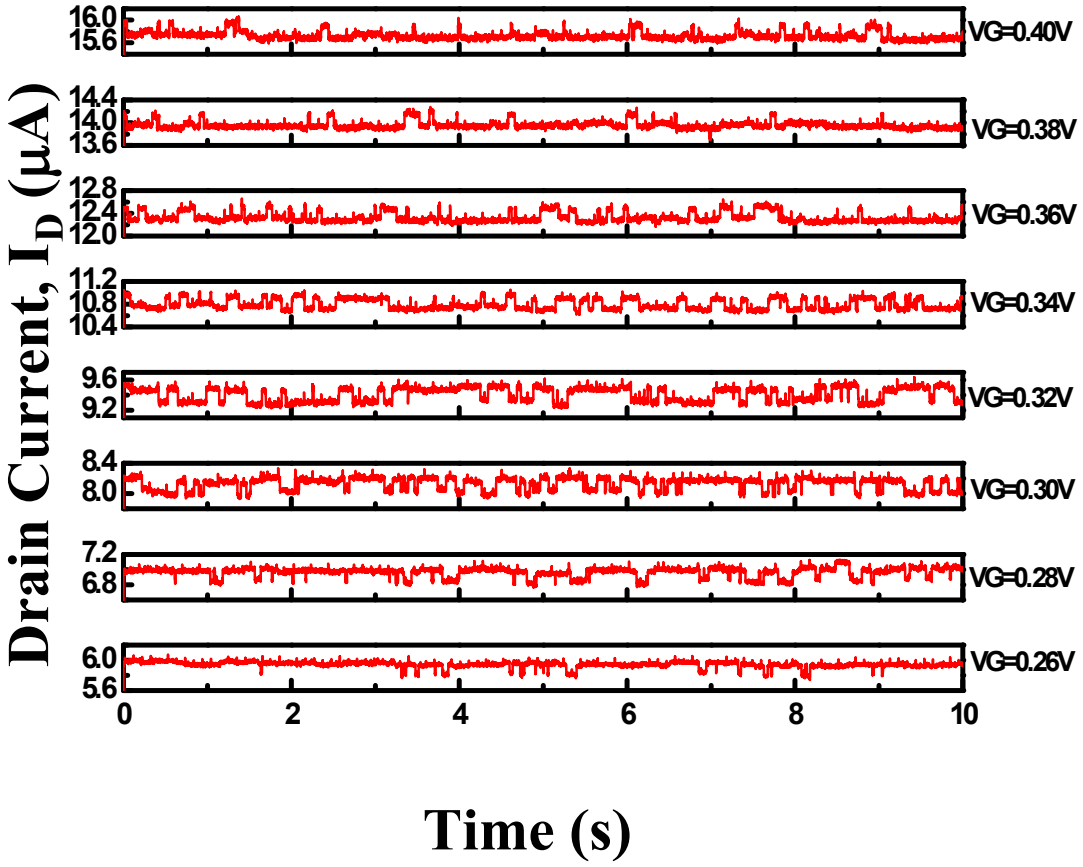


Fig. 5.4 Drain current waveform of SiC on S/D device, T=25℃.

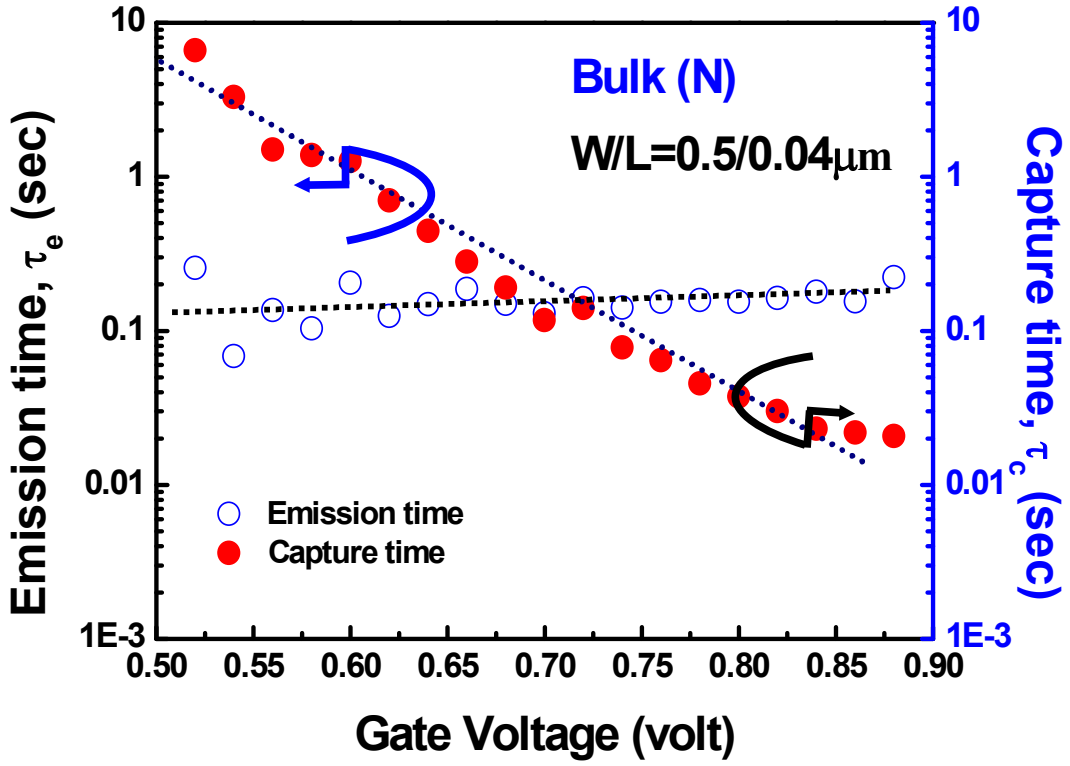


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Fig. 5.5 Variation of capture time τ_c (filled symbol) and emission time τ_c (open symbol) as gate voltage increases for bulk-Si device.

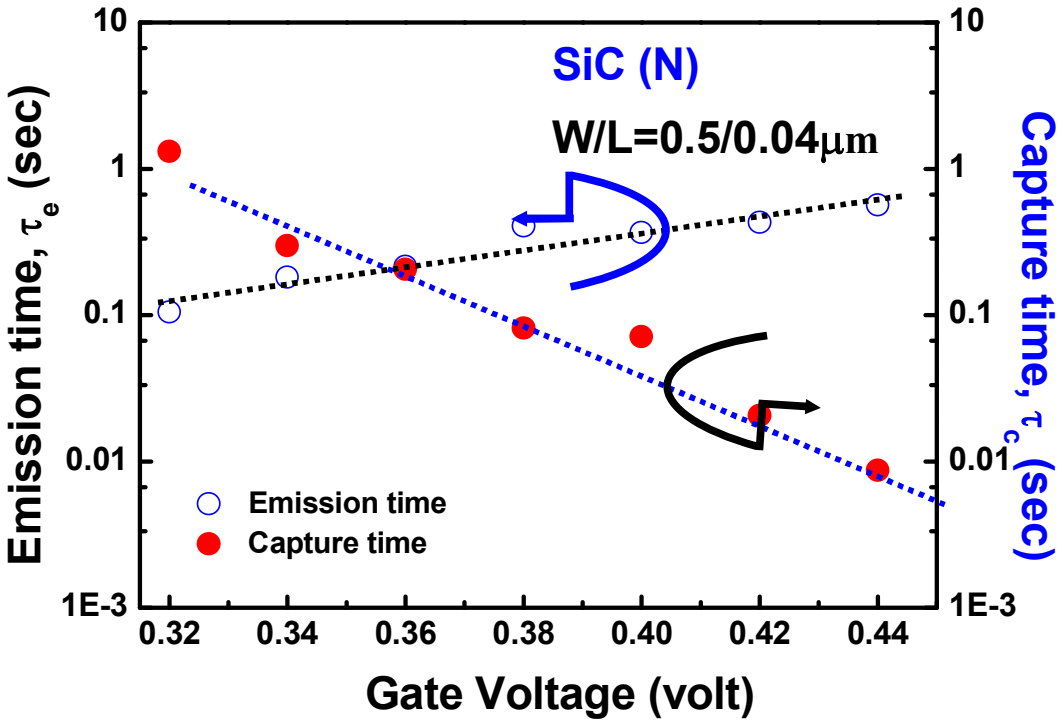

Fig. 5.6 Variation of capture time τ_c (filled symbol) and emission time τ_e (open symbol) as gate voltage increases for SiC on S/D device.

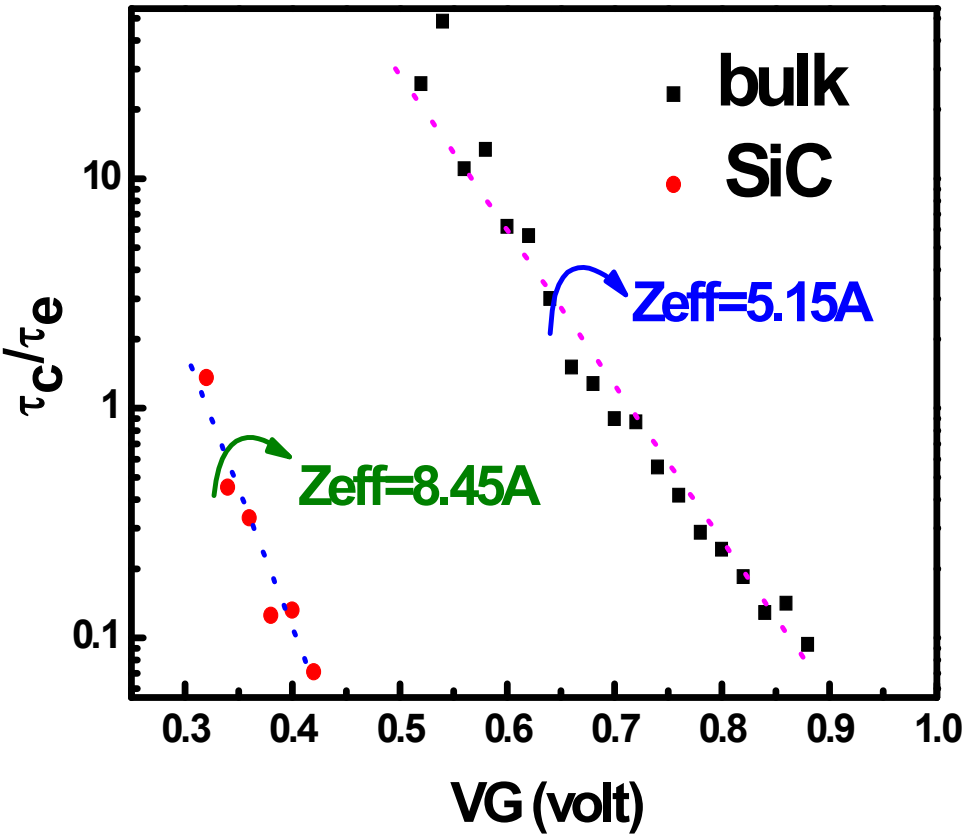

Fig. 5.7 Capture time over emission time versus gate voltage plots for n-MOSFETs.

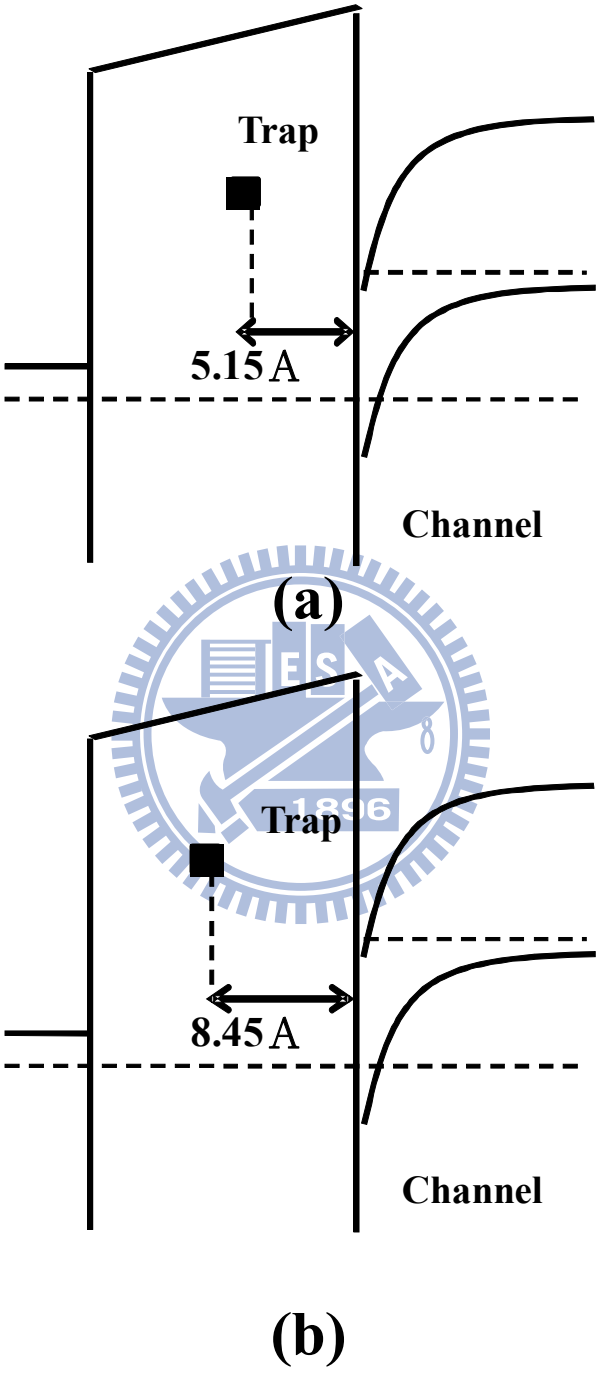

Fig.5.8 The effective depth location for the two traps in, (a) bulk-Si and (b)SiC on S/D devices.

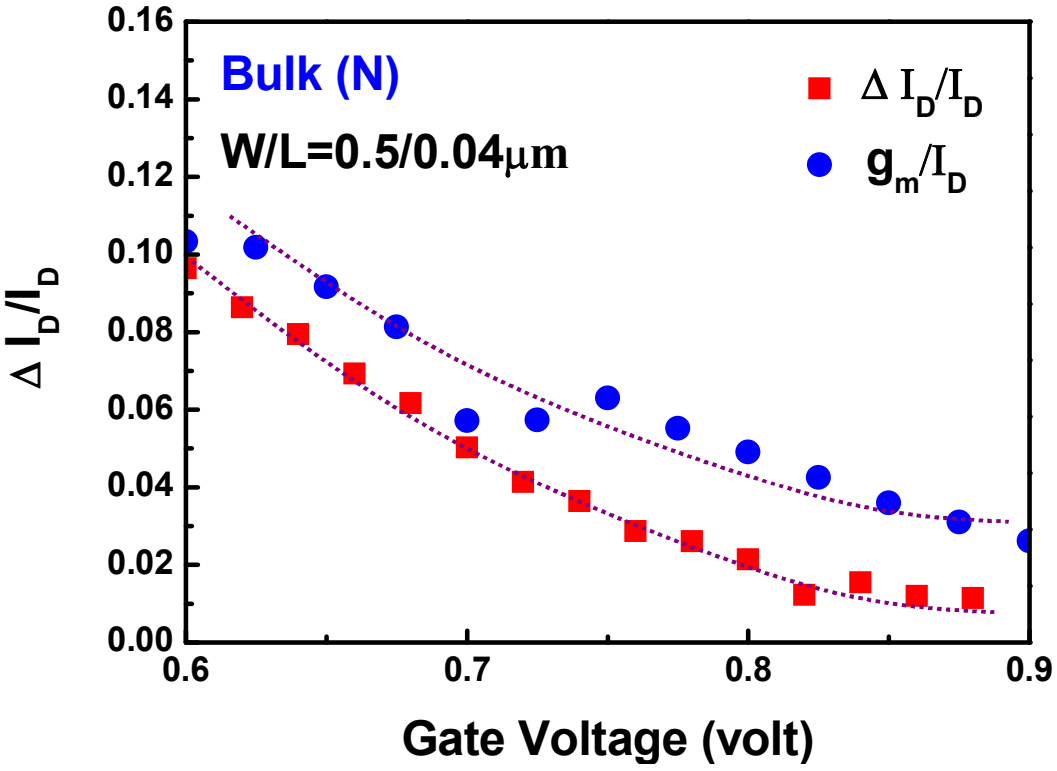

Fig. 5.9 Normalized RTN amplitude (square symbol) and normalized conductance change (circle symbol) versus gate voltage for bulk-Si device.

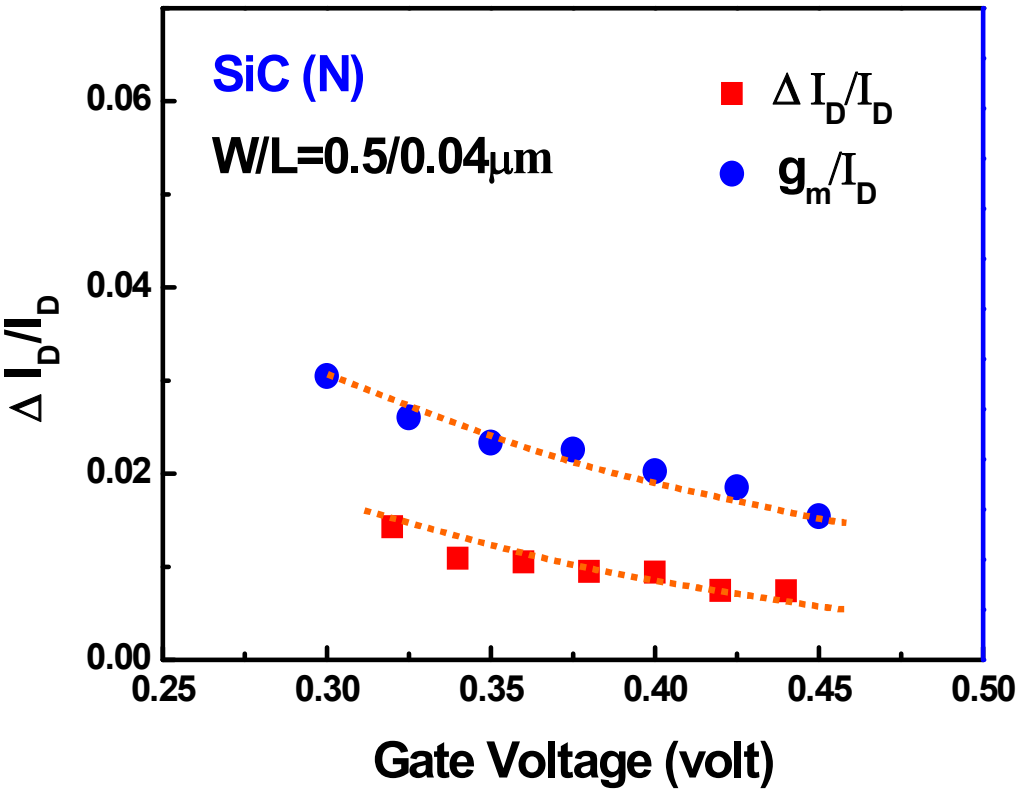

Fig. 5.10 Normalized RTN amplitude (square symbol) and normalized conductance change (circle symbol) versus gate voltage for SiC on S/D device.

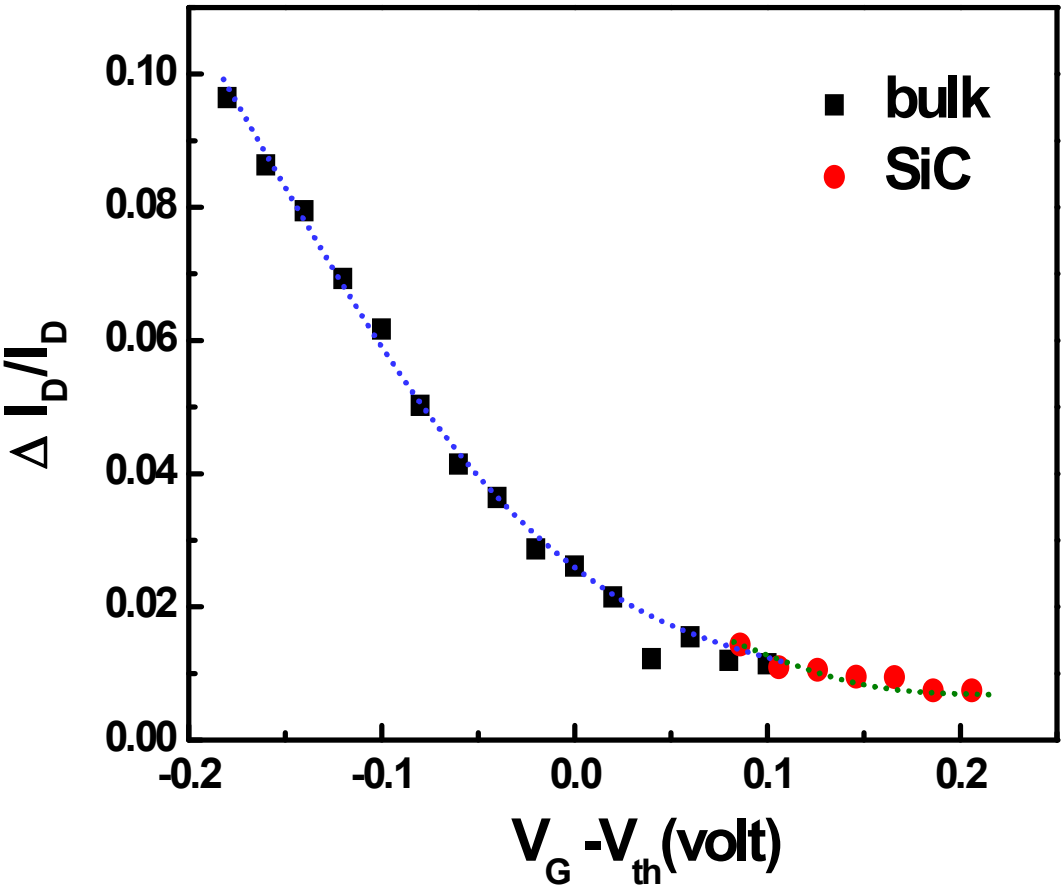

Fig. 5.11 Normalized current amplitude versus overdrive voltage for bulk-Si and SiC on S/D devices.

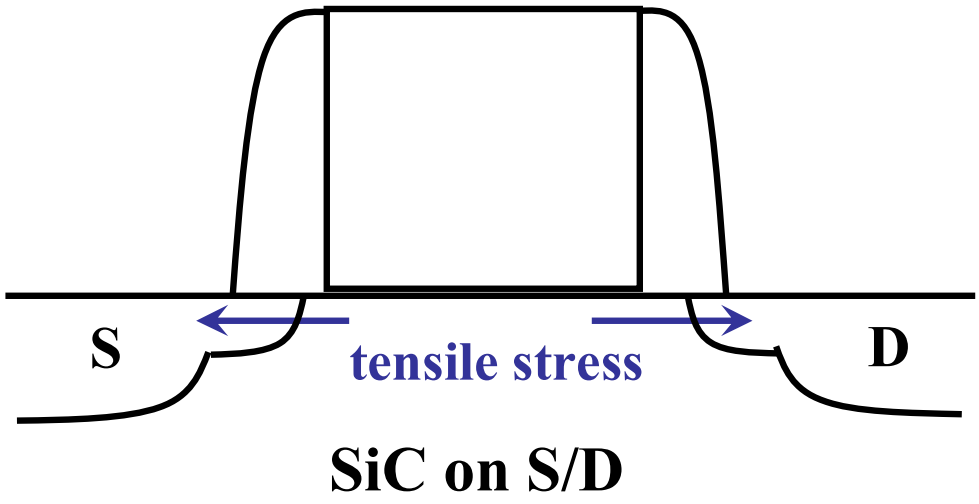

Fig. 5.12 Illustration of the strain direction for SiC on S/D device.

Chapter 6
Summary and Conclusion

In this thesis, we are the first to examine the strain-induced trap behavior in MOS devices using the I_D-RTN technique [6.1]. The process induced strain among different strained techniques can be investigated by the I_D-RTN measurement. The hot carrier stress which induces the current degradation and produces the slow oxide traps are studied for both uniaxial strained n- and p-MOSFETs.

First, the strain induced drain current instability is investigated in the thesis. The oxide traps properties in the stained CMOS devices are analyzed. Then, different process-induced strain effects for uniaxial strained n-MOSFETs and p-MOSFETs have been observed respectively. Experimental results show that, in the CESL devices, vertical compressive strain generates extra oxide defects and induces more scattering after HC stress. The strain techniques would improve the carrier mobility but their hot carrier reliabilities become poorer. Furthermore, the application to the SiC on S/D devices also shows that the uniaxial strain in such device exhibits less impact on the device reliability. Therefore, this strained SiC device is similar to the SiGe S/D device in terms of the I_D-RTN characteristics. As a result, the CESL strain can induce more scattering effect that would contribute to a non-negligible amount of extra device degradation.

In summary, the hot-carrier induced oxide trap and its correlation with enhanced degradation in strained CMOS devices have been justified by the I_D-RTN technique. By utilizing the approach, the I_D-RTN slow oxide trap produced by the HC stress can be measured in both strained n- and p-MOSFETs. The extra degradation coming from the

stress of CESL device shows a significant amount of the mobility as well as the drain current degradation by the vertical strain. This method also provides a way to measure the slow traps that charge pumping can not achieve (i.e., charge pumping can measure the fast trap only.)

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